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Memorandum No. UCB/ERL M98/48

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Position Sensing for Electrostatic Micropositioners

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B.ENG. (Chulalongkorn University) 1991
M.S. (University of California, Berkeley) 1995

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY of CALIFORNIA, BERKELEY

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Spring 1998

The dissertation of Naiyavudhi Wongkomet is approved:

Professor Bernhard E. Boser, Chair	Date 15 July 1998
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Professor Albert A. Pisano	Date 6 July 98

University of California, Berkeley

1998

Capacitive Position Sensing for Micropositioners

by

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Abstract

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Professor Bernhard E. Boser, Chair

This research investigates the design of capacitive position sensing circuits for electrostatic micropositioners. The goals of this investigation are to understand the interaction among the micropositioners, the driving circuits, and the position sensing circuits, to explore fundamental limitations of capacitive position sensing, and to utilize position sensing circuits to implement feedback loops to improve the dynamics of micropositioners. A dual-stage servo system for magnetic disk drives is used as the framework of this research.

At the circuit level, capacitive position sensing schemes for monolithic implementations are discussed. A technique of interfacing three-terminal sense elements to fully-differential sensing electronics is presented. The fundamental resolution imposed by the amplifier thermal noise is studied. A circuit technique that enables the sensing circuit to potentially achieve the fundamental resolution is proposed.

At the integration level, methods of sharing a single set of electrodes between the high voltage drive of the micropositioner and the precision low-voltage sensing

signal are presented. Issues related to the interface between capacitive position sensing and electrostatic actuation are investigated and their solutions are presented.

To demonstrate the feasibility of the design techniques developed in this research, a prototype capacitive position sensing circuit for micropositioners has been designed. An experimental electrostatic positioning system utilizing this sensing circuit has a position sensitivity of 35mV/μm, an offset of approximately 10mV, a thermal noise floor of 0.19Angstrom/$\sqrt{Hz}$ or approximately 3.4nm in 25kHz bandwidth, and a feedthrough-limited resolution of 10nm for maximum driving voltages ±10V. A simple feedback loop utilizing the position sensing circuit and a lead filter reduces the micropositioner settling time from over 100msec to 0.7msec.

Bernhard Boser 15 July 1998

Professor Bernhard E. Boser, Chair Date

Acknowledgments

I extend my sincere appreciation to Professor Bernhard Boser for his guidance and support throughout the study of this research. His constructive critique has been crucial to the success of this research. Many thanks go to Professor Paul Gray and Professor Albert Pisano for invaluable suggestions and for reading this thesis. Along with Professors Boser, Gray, and Pisano, I would like to thank Professor Roger Howe for serving on my qualifying examination committee. In addition, I want to thank Professor Roberto Horowitz and Dr.Long-Sheng Fan of IBM's Almaden Research Center for their numerous inputs.

The collaboration and discussion with fellow students have been very valuable. Without Dave Horsley, I would not have a micropositioner to test the circuit. Also, I am thankful for his help with the feedback loop design. Darrin Young, my office neighbor, has always been helpful on circuit and any other issues. My stay at Berkeley would have been less interesting without him. I would like to thank Mark Lemkin and Bill Clark for bringing me up to speed when I started this research. I thank Andy Abo for sharing his ideas on correlated double sampling and kT/C noise cancellation. In addition, I would like to thank Arnold Feldman for his suggestions on amplifier design and circuit layout. Other colleagues who have always been supportive and made life in 550 Cory so enjoyable include Jeff Ou, George Chien, Keng-Long Fong, Monico Ortiz, Edwin Chan, Eugene Cheung, Seema Butala, Colby Boles, Ichabod Nguyen, Crist Lu, Chris Rudell, Thomas Cho, Dave Cline, Greg Uehara, Todd Weigandt, Keith Onodera, Cindy Baringer, Adam Eldredge, Xue-Song Jiang, Joe Seeger, and Pramote Piriyapoksombat. In addition to my colleagues, I would like to thank the staffs of the EECS Department and the Berkeley Sensor and Actuator Center (BSAC)—Heather Brown, Ruth Gjerde, Sheila Kelly, Joel Nice, Marilyn Abbink, and Elise Allison.

Very special thanks go to all my friends at Berkeley and around the world for making my stay at Berkeley such a wonderful experience. In alphabetical order, they are Aied, Ann, Alice, Bank, Bee, Ben, Bernice, Byrd, Chai, Chin, Chom, Christine, Dao, David, Den, DJ, Ekapon, Gal, Gob, Golf, Gordon, Hal, Hansel, Jain, Janice, Jeng, Jenny, Jia, Jia-Zhen, Joe, John, Joy, Jump, June, Kaeo, Kaew, Katherine, Kob, Kok, Kong, Kristina, Krit, Kuk, Lily, Lord, Lynn, Maew, Michelle, Muk, Nam, Nop, Oat, Ood, Oh, Pae, Pam, Patr, Pitt, Puey, Pui, Purt, Rath, Rico, Rob, Ruj, San, Sopon, Suwat, Tee, Teresa, Tip, Tukta, Wai-Yee, Wahn, Wayne, and Yoon. In addition, I am grateful to Orr for her love and support, and for always being there for me.

Finally, I would like to thank my parents, my sister, my brother for their continuing support.

This research was supported by Defense Advanced Research Project Agency.

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Chapter 1

Introduction

1.1 Motivation

Micropositioners are attractive in applications such as magnetic and optical data storage, and optical alignment because they provide high accuracy and high bandwidth actuation at a low cost. Micropositioners are typically employed in feedback loops to improve the positioning accuracy and the dynamics, and to reduce the sensitivities to fabrication tolerances. This research focuses on the design of capacitive position sensing circuits for electrostatic micropositioners and the utilization of the sensing circuit to implement a feedback loop.

Among the means to drive and measure the position of micropositioners, electrostatic actuation and capacitive position sensing are attractive because they are compatible and do not require any extra processing step or material, thus avoiding adding complexities to the fabrication process. This research extends capacitive position sensing, which has been employed in other micromachined applications such as inertial sensors and pressure sensors, to interface with the electrostatic actuation of micropositioners, thus permitting sharing a single set of electrodes between sensing and driving.

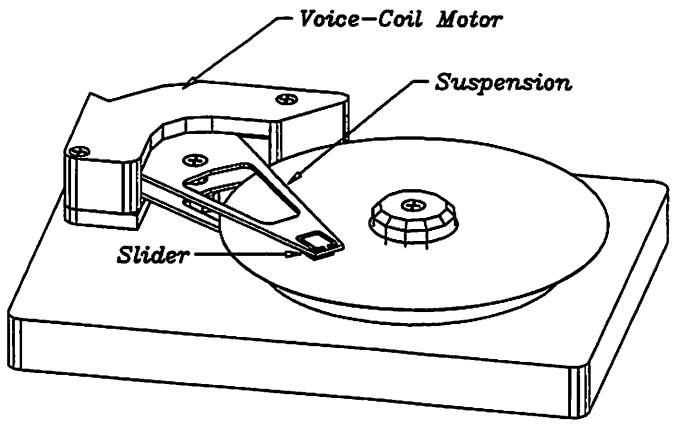


Fig. 1.1: Servo-positioning mechanism of a conventional disk drive. (Courtesy of D. Horsley, UC Berkeley.)

The framework of this research is a magnetic disk drive application [1]. In this application, micropositioners are used as the secondary actuators in dual stage positioning mechanisms to improve the tracking accuracy and bandwidth. The goal of this implementation is to achieve an areal density of 10Gbit/in^2. To reach this goal, a disk drive must have a track density of approximately 25,000 tracks per inch (tpi)—a three- to four-fold increase over current track densities of 6000 to 8000 tpi. A track density of 25,000 tpi will require a track pitch of 1 μm, a servo tracking accuracy of 100nm, and a servo loop bandwidth of approximately 2kHz [1], [2].

Fig. 1.1 shows the servo-positioning mechanism of a conventional disk-drive. The read-write element is embedded in a ceramic slider which is bonded to a gimbal at the end of the stainless steel suspension. An electromagnetic voice-coil motor (VCM) attached to the other end of the suspension moves the slider radially across the disk. The servo bandwidth of this conventional approach is limited to less than a kilohertz by mechanical resonances in the suspension, while the DC tracking accuracy is reduced by stiction in the bearings of the suspension arm [2].

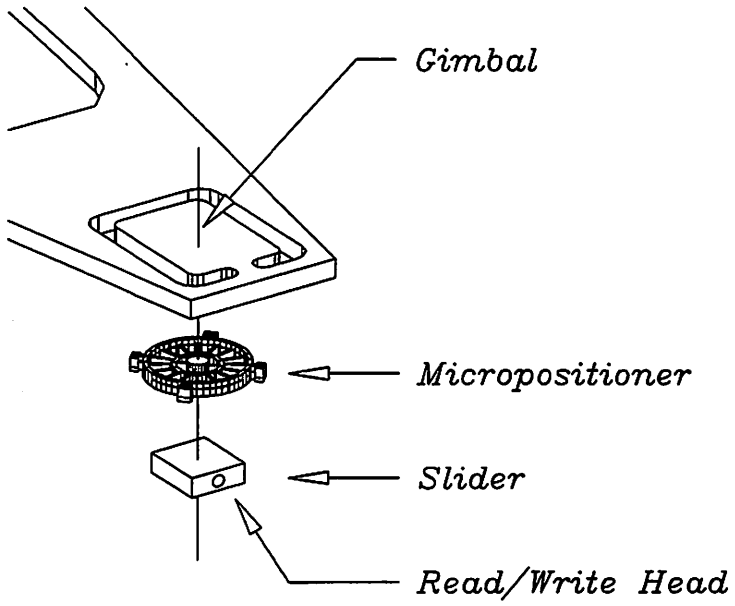


Fig. 1.2: A dual-stage servo-positioning mechanism. The micropositioner is employed to provide fine and high-bandwidth positioning. (Courtesy of D. Horsley, UC Berkeley.)

Improvements in tracking accuracy and bandwidth can be achieved by employing a dual stage positioning mechanism using a conventional VCM for coarse positioning and a high bandwidth secondary actuator for fine positioning [2]. To date, three types of secondary actuators have been proposed: an actuated suspension [3], an actuated head [4], and an actuated slider [5], [6], [7]. In the last approach, the slider is moved by a micropositioner mounted between the slider and the gimbal of a conventional suspension as shown in Fig. 1.2. This approach has two advantages [7]. First, the use of the micropositioner does not significantly affect the fabrication processes of the head, the slider, and the suspension. Second, the micropositioners are batch-fabricated, thus providing a low cost solution.

In this application, the micropositioner is required to move a pico-slider, which weighs around one milligram, at 10 to 30 times of the acceleration of gravity. Thus, the micropositioner must be capable of generating forces in the range of a few hundred micronewtons [5]. Additionally, a travel range of a few microns is needed to

Table 1.1: Requirements of the servo system, the micropositioner, and the position sensing circuit for the magnetic disk drive application.

Required force	200-300μN
Maximum driving voltage	80V or ±40V
Maximum displacement	±2μm
Tracking accuracy	100nm
Position sensing resolution	10nm
Servo bandwidth	2kHz
Sensing bandwidth	25kHz
Sensing frequency	< 1MHz

cover several disk tracks. From the system perspective, it is required that such forces and travel range are achieved with driving voltages smaller than 80 volts or ±40V.

The requirements of the servo system, the micropositioner, and the position sensing circuit for this application are summarized in Table 1.1. As a rule of thumb in servo system design, the position sensing resolution of 10nm is ten times better than the tracking accuracy. Likewise, the position sensing bandwidth of 25kHz is approximately ten times higher than the servo bandwidth. The sampling frequency should not be higher than one megahertz to avoid interference with the read channel of the disk drive, which extends from a few megahertz up to several hundreds megahertz. To facilitate sharing the electrodes between sensing and driving, the sensing circuit must be capable of interfacing with the 80V or ±40V driving voltages. Additionally, to ensure low cost, the sensing circuit must be fabricated in a conventional low-voltage CMOS technology.

1.2 Thesis Organization

Chapter 2 reviews various configurations of electrostatic micropositioners and discusses their effects on magnitudes and linearities of capacitance variations and actuation forces. Second-order effects in electrostatic actuation are explained.

In Chapter 3, two commonly used capacitance sensing techniques which are suitable for monolithic integration—a synchronous detection circuit and a switched-capacitor sensing circuit—are examined. Pseudo-differential technique is introduced. The use of coupling capacitors to interface the sensing circuit to the high-voltage drive of the micropositioner is discussed.

Chapter 4 investigates nonidealities in the sensing electronics and propose that correlated double sampling can be used to remove these errors. Afterwards, the optimization of the amplifier thermal noise and the resolution improvement due to the use of correlated double sampling to cancel the kT/C noise are presented.

Chapter 5 explores issues related to the interface between capacitive position sensing and electrostatic actuation, namely the sensing charge leakage, feedthrough, voltage-dependent capacitance at the rotor node, sense-force error, and gain variations and offsets due to coupling capacitors and off-chip parasitics. Techniques which facilitate the integration of the sensing and driving circuits are proposed.

Chapter 6 describes prototype implementations and experimental verifications of a position sensing circuits and a closed-loop electrostatic micropositioner. Measurement results are also presented. Finally, the conclusion is given in Chapter 7.

Chapter 2

Electrostatic Micropositioners

2.1 Introduction

This chapter gives an overview of electrostatic micropositioners. The concept of driving and sensing the micropositioner electrostatically is attractive because no additional processing step or material is required in the fabrication process. Furthermore, the driving and the sensing can share a single set of electrode, thus eliminating the need for another structural or interconnect layer. To understand the fundamentals and to facilitate the discussion in the following chapters, the electrical model, the mechanical model, and the electromechanical coupling mechanisms of electrostatic micropositioners will be introduced in this chapter. In particular, we will discuss the effects of configurations of micropositioners on the magnitudes and linearities of actuation forces and capacitance variations. Negative electrostatic spring, pull-in instability, and voltage nonlinearity in electrostatic actuation will be elaborated. Finally, we will use the obtained results to establish a model describing the behavior of micropositioners.

First, we will look at the fundamental of electrostatic actuation and capacitive sensing. Electrostatic forces exist when there is a voltage difference between two

capacitor plates. Electrostatic forces are attractive with the magnitude equal to the rate of change of the energy with the displacement,

$$F = \frac{\partial E}{\partial x} = \frac{\partial}{\partial x}\left(\frac{CV_{dr}^2}{2}\right) \qquad \text{(Eq 2-1)}$$

where V_{dr} is the bias voltage between the two capacitor plates. In general, large and tall structures with small gaps and high voltages yield large electrostatic forces. Electrostatic forces, however, are nonlinear functions of voltages and, usually nonlinear functions of displacements also.

Typically, sense elements in micropositioners can be approximated as parallel-plate capacitors. Neglecting fringing fields, the capacitance of two parallel plates is

$$C = \frac{\varepsilon_o \varepsilon_r A}{x} \qquad \text{(Eq 2-2)}$$

where A is the overlapping area of the two plates, x is the gap between the two plates, ε_o is the electric permittivity of vacuum, and ε_r is the relative dielectric constant of the medium between the two plates. In practice, the error due to neglecting the fringing fields is small when the gap x is at least four times smaller than the width of the parallel plates [8].

2.2 Micropositioner Configurations

Lateral comb, transverse comb, and parallel-plate structures are common configurations for micropositioners. In this section, we will discuss their electromechanical properties by focusing on the magnitudes and linearities of actuation forces and capacitance variations. The results from this section are summarized in the design examples shown in Table 2.1.

Table 2.1: Design examples of micropositioners utilizing different structures. Given parameters are shown in unshaded boxes, while the results are shown in shaded boxes.

Parameters	Lateral Comb	Transverse comb	Parallel-plate
Required force ($\frac{\partial C_S}{\partial x}\frac{V_{dr}^2}{2}$)	300μN		
Driving voltage (V_{dr})	80V		
dC_S/dx	94fF/μm		
Gap between electrodes (g, x_o)	2μm		
Structure thickness (t)	10μm		N.A.
Number of electrodes (N)	2100	100	N.A.
Electrode length	10μm	42.4μm	N.A.
Electrode pitch	4μm		N.A.
Area	290x290μm^2	130x130μm^2	206x206μm^2
C_S	929fF	187fF	188fF
Maximum displacement	~electrode length	$x_o/3$	$x_o/3$
Nonlinearity in dC_S/dx	none	$\sim(\Delta x/x_o)^2$	$\sim\Delta x/x_o$

2.2.1 Lateral Comb Structure

A lateral comb structure [5], as conceptually shown in Fig. 2.1, is actuated by the fringing electric fields at the tip of the comb fingers. The two stators and the moving element of the structure form a capacitive half-bridge whose differential sense capacitance can be described as

$$C_{S1}, C_{S2} = \frac{\varepsilon N t(x_o \pm \Delta x)}{g} \qquad \text{(Eq 2-3)}$$

where t is the thickness of the structure, x_o is the nominal overlapping of the electrodes and is approximately the length of the electrodes, g is the gap between the electrodes of the moving element and the stator, and N is the number of the electrodes. From Eq. 2-3, the capacitance variation as a function of displacement Δx and the electrostatic force can be calculated as

$$\frac{dC_S}{dx} = \frac{\varepsilon N t}{g} = \frac{C_{S0}}{x_o} \qquad \text{(Eq 2-4)}$$

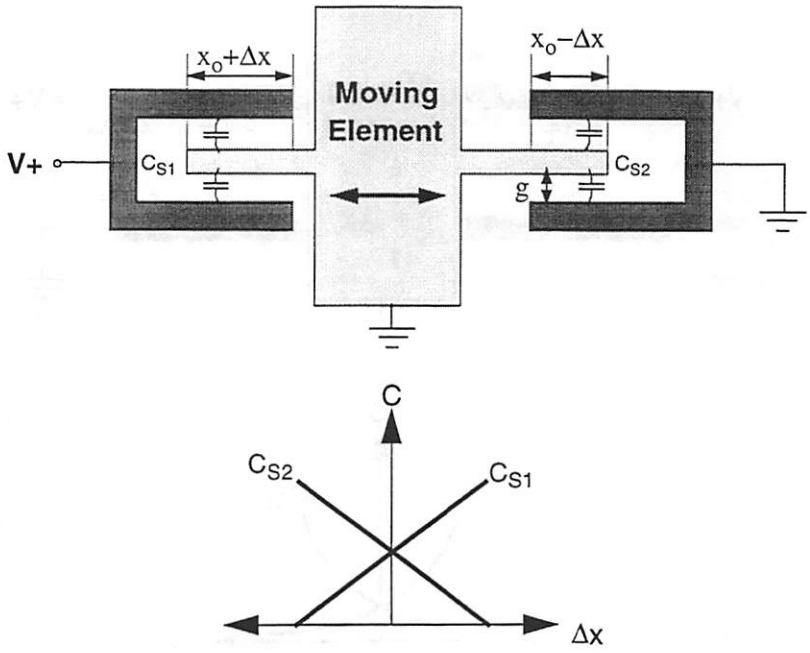


Fig. 2.1: A simplified lateral comb structure and its capacitance variation as a function of displacement

and

$$F = \frac{\partial C}{\partial x} \cdot \frac{V_{dr}^2}{2} = \left(\frac{\varepsilon N t}{2g}\right) V_{dr}^2, \qquad \text{(Eq 2-5)}$$

respectively, where C_{S0} is the nominal capacitance. To maximize the capacitance variation and the actuation force, the structure thickness and the number of the electrodes should be maximized, while the gap between electrodes should be minimized. And since the capacitance variation and the force, to the first order, are independent of the length of the electrodes, the electrodes should be short to save the die area. This is evident in the micropositioner described in reference [5].

A lateral comb structure is attractive because the magnitude of the force and the capacitance variation is not a function of the displacement Δx. Its drawback, however, is the smaller forces and dC/dx compared to a similarly sized transverse comb structure.

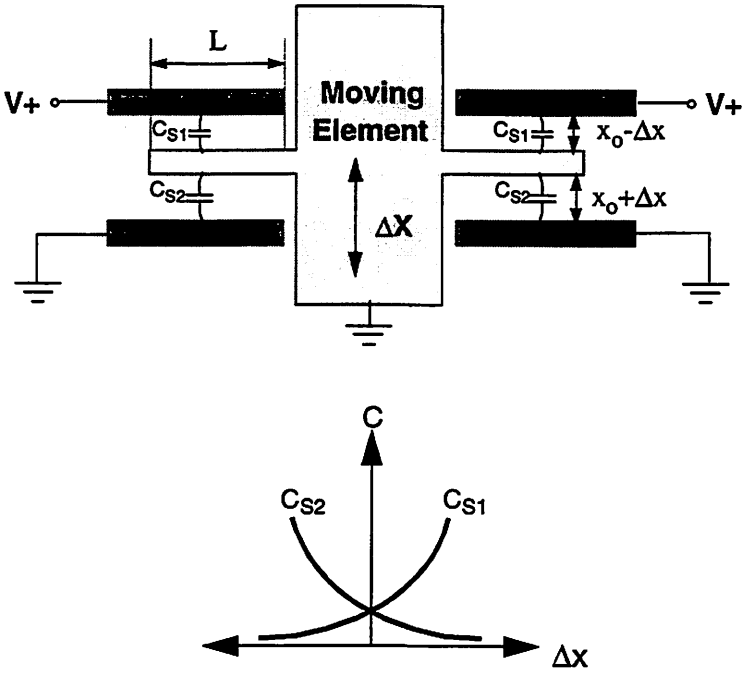


Fig. 2.2: A simplified transverse comb structure and its capacitance variation as a function of displacement

2.2.2 Transverse Comb Structure

By utilizing the electric fields of the total length of the parallel electrodes rather than the fringing fields at the tips, a transverse comb structure achieves larger actuation forces and dC/dx than a similarly sized lateral comb structure. The differential sense capacitance, capacitance variation, and electrostatic force of a transverse comb structure can be written, respectively, as

$$C_{S1}, C_{S2} = \frac{\varepsilon NtL}{(x_o \pm \Delta x)}, \qquad \text{(Eq 2-6)}$$

$$\left|\frac{dC_S}{dx}\right| = \frac{\varepsilon NtL}{x^2} = \frac{C_S(x)}{x}, \qquad \text{(Eq 2-7)}$$

and

$$F = \left(\frac{\varepsilon NtL}{2x^2}\right)V_{dr}^2, \qquad \text{(Eq 2-8)}$$

where t is the thickness of the structure, L is the overlapping of the electrodes and is approximately the length of the electrodes, x_o is the nominal gap between the moving

and the stationary electrodes, and N is the number of electrodes. Comparing Eq. 2-7 to Eq. 2-4 and Eq. 2-8 to Eq. 2-5 shows that, for the same number of electrodes, capacitance variations and actuation forces of a transverse comb structure are larger than those of lateral comb structures by L/x, or the ratio between the length and the gap of electrodes. In practice, lateral comb structures have a large number of short electrodes, thus reducing the differences to smaller than L/x.

As shown in Eq. 2-8, a transverse comb structure has a nonlinear relationship between the capacitance variation and the displacement Δx. Using Taylor series expansion, the capacitance variation as a function of the displacement is

$$\Delta C_S = C_{S1} - C_{S2} = \frac{2\varepsilon NtL}{x_o} \cdot \left(\frac{\Delta x}{x_o} + \left(\frac{\Delta x}{x_o}\right)^3 + \left(\frac{\Delta x}{x_o}\right)^5 + \ldots \right). \qquad \text{(Eq 2-9)}$$

Because the even-order terms are cancelled by the differential characteristics of the sense capacitor, the nonlinearity in capacitance variation is dominated by the third-order term,

$$\text{Nonlinearity in } \frac{dC}{dx}\ (\%) \approx \left(\frac{\Delta x}{x_o}\right)^2 \bullet 100\% \qquad \text{(Eq 2-10)}$$

For large displacements, the nonlinearity becomes significant and must be considered in the design of the position sensing circuit and the servo system. As an example, a transverse comb micropositioner with a nominal gap of 10μm [7] has a nonlinearity of 40nm for an actuation range ±2μm. In comparison, the required position resolution of the magnetic disk drive application described in Chapter 1 is 10nm. A solution is to pre-calculate the nonlinearity and subtract it from the measured position in the digital domain.

In addition to the nonlinearity in capacitance variation, a transverse comb structure, according to Eq. 2-7, generates forces that are functions of the displacement. This results in the negative electrostatic spring and the so-called pull-in instability. Both of which will be discussed in Section 2.4

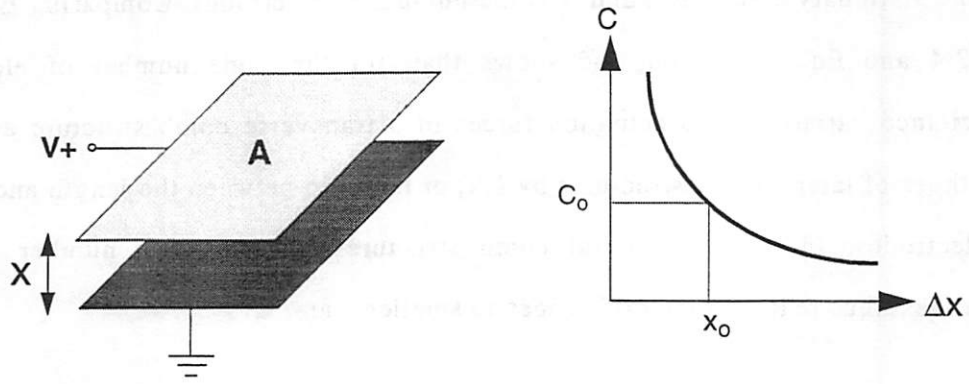


Fig. 2.3: A parallel-plate structure and its capacitance change as a function of displacement

2.2.3 Parallel-Plate Structure

A parallel-plate structure, as shown in Fig. 2.3, is needed for actuation in the z-axis, or the axis perpendicular to the substrate. Similarly to a transverse comb structure, a parallel-plate structure is actuated by the electric field of the whole parallel plates. Hence, this type of structure has capacitance variations and actuation forces which are nonlinear functions of displacements, and exhibits negative electrostatic spring and pull-in instability.

The sense capacitance, capacitance variation, and electrostatic force of a parallel-plate structure can be written, respectively, as

$$C_S = \frac{\varepsilon A}{x}, \qquad \text{(Eq 2-11)}$$

$$\left|\frac{dC_S}{dx}\right| = \frac{\varepsilon A}{x^2} = \frac{C_S(x)}{x}, \qquad \text{(Eq 2-12)}$$

and

$$F = \left(\frac{\varepsilon A}{2x^2}\right)V^2. \qquad \text{(Eq 2-13)}$$

where A is the area of the parallel plates and g is the gap between the two plates.

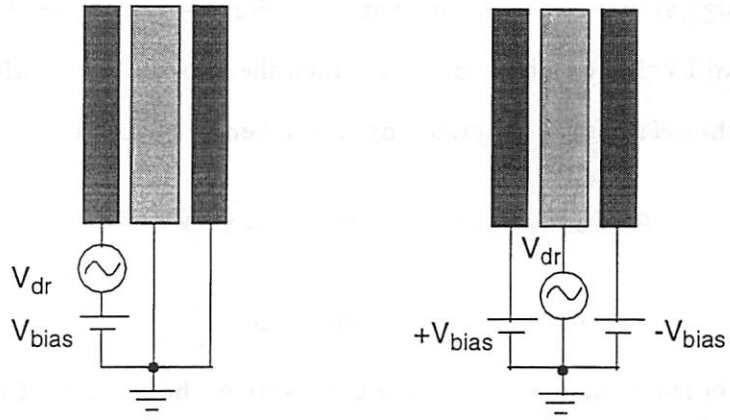


Fig. 2.4: Signal linearization schemes as discussed in [2]. a) Small signal linearization scheme. b) Large signal linearization scheme.

Due to the limited number of structural layer, a parallel-plate structure typically forms a single-ended sense capacitor and needs a reference capacitor such as an unreleased structure to remove the offset in the position sensing signal. Being single-ended, the nonlinearity in capacitance variation is higher than that of a transverse comb structure because of the uncancelled even-order terms. Hence, the nonlinearity is dominated by the second-order term and is equal to

$$\text{Nonlinearity in } \frac{dC}{dx}\,(\%) \approx \frac{\Delta x}{x_o} \bullet 100\% \qquad \text{(Eq 2-14)}$$

2.3 Voltage Nonlinearity

Electrostatic forces, according to Eq. 2-1, are nonlinear functions of voltage. Reference [2] discusses two linearization schemes for electrostatic forces. The small signal scheme, as shown in Fig. 2.4a, superimposes a small control voltage on a large DC biasing voltage. This scheme has two restrictions: the control voltage is limited to smaller than the bias voltage and the large initial DC bias causes asymmetrical movement.

The large signal linearization scheme in Fig. 2.4b alleviates both problems and allows the control voltage to be even larger than the bias voltage while maintaining the linear relationship. The force generated by this scheme is equal to

$$F = \alpha(V_{bias} + V_{dr})^2 - \alpha(V_{bias} - V_{dr})^2, \qquad \text{(Eq 2-15)}$$

$$= 4\alpha V_{bias} V_{dr} \qquad \text{where } \alpha = \frac{1}{2}\cdot\frac{\partial C_S}{\partial x}. \qquad \text{(Eq 2-16)}$$

For transverse comb structures, the force constants on both sides of the structures are not equal because they are functions the displacement; hence, Eq. 2-15 becomes

$$F = \alpha_1(V_{bias} + V_{dr})^2 - \alpha_2(V_{bias} - V_{dr})^2, \qquad \text{(Eq 2-17)}$$

where α_1 and α_2 are the force constants of the two sides. Subsequently, Eq. 2-17 can be approximated as

$$F \approx 4\alpha_o\left(V_{bias}V_{dr} + \frac{\Delta x}{x_o}(V_{bias}^2 + V_{dr}^2)\right) \qquad \text{where } \alpha_o = \frac{\varepsilon NtL}{2x_o^2}. \qquad \text{(Eq 2-18)}$$

2.4 Electrostatic Spring and Pull-In Instability

As described earlier, transverse comb structures and parallel-plate structures have actuation forces that are functions of the displacement. This results in the negative electrostatic spring [8], [9] and the so-called pull-in instability [8], [10], [11].

Because the magnitude of the electrostatic force increases as the gap between the two plates decreases, its effect can be viewed as an 'negative spring'. The electrostatic spring constant can be calculated by differentiating the force equation with respect to position. According to Eq. 2-1,

$$k_e = \frac{dF}{dx} = -\frac{\varepsilon NtL}{x^3}V_{dr}^2 = -\frac{C_S(x)}{x^2}V_{dr}^2. \qquad \text{(Eq 2-19)}$$

Since the electrostatic spring force subtracts from the mechanical spring force, it can be used to lower the effective spring constant and the resonant frequency of the mechanical structures, as will be shown in Section 2.5.

The pull-in instability occurs when the negative electrostatic spring constant becomes larger than the mechanical spring constant, thus causing the two plates of the structure to snap to each other. For parallel-plate structures or transverse comb structures biased as shown in Fig. 2.4a, the pull-in instability occurs when the displacement of the structure is equal to one-third of the nominal gap. For transverse comb structures biased as shown in Fig. 2.4b, the pull-in instability becomes a function of the bias voltage. For large enough voltages, the pull-in instability can occur at nominal position, thus limiting the maximum displacement to zero [8]. A constant charge driving scheme utilizing an appropriate feedback network is being developed to overcome the pull-in instability and allows transverse comb structures to move by more than one-third of the nominal gap [10].

2.5 Micropositioner Modeling

The displacement x of a micropositioner can be described as a function of the driving force F_{dr} using the mass-spring-damper model shown in Fig. 2.5 as

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + k_m x = F_{dr} \qquad \text{(Eq 2-20)}$$

where k_m is the mechanical spring constant, b is the damping coefficient due to the surrounding gas ambient and the internal dissipation of the spring, and m is the mass of the moving element. This mechanical model has an equivalent electrical model which is also shown in Fig. 2.5.

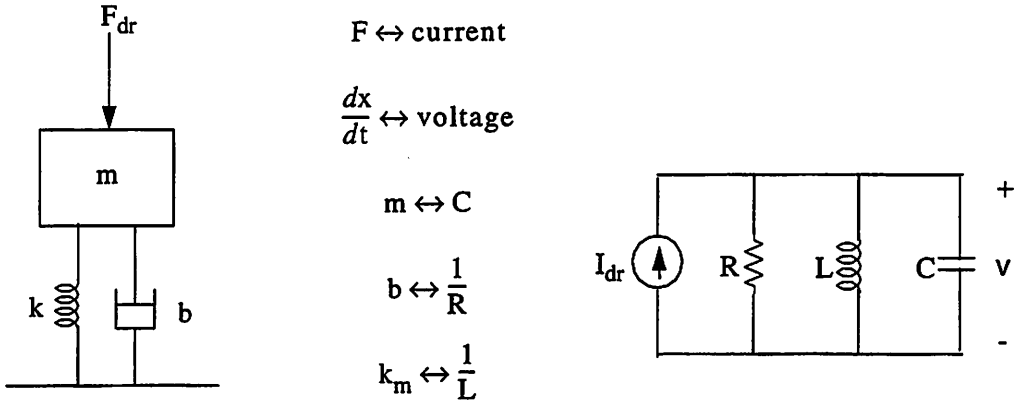


Fig. 2.5: A mass-spring-damper model and its electrical equivalent model

To demonstrate the effects of negative electrostatic spring, we will derive the transfer function of a transverse comb structure. By substituting the linearized driving force in Eq. 2-18 into Eq. 2-20,

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + (k_m - k_e(V_{bias}^2 + V_{dr}^2))x = (k_v V_{bias})V_{dr} \qquad \text{(Eq 2-21)}$$

where $k_e = \frac{4\alpha_o}{x_o}$ is the approximated electrostatic spring constant, $k_v = 4\alpha_o$ is the voltage-to-force gain, and α_o is equal to $\frac{\varepsilon NtL}{2x_o^2}$. For $V_{dr} \ll V_{bias}$,

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + (k_m - k_e V_{bias}^2)x \approx (k_v V_{bias})V_{dr} \qquad \text{(Eq 2-22)}$$

Solving for the displacement using Laplace transform yields the second-order transfer function

$$\frac{X(s)}{V_{dr}(s)} = \frac{\frac{k_v V_{bias}}{\omega_n^2 m}}{\left(\frac{s}{\omega_n}\right)^2 + \frac{s}{\omega_n Q} + 1} \qquad \text{(Eq 2-23)}$$

with the natural frequency

$$\omega_n = \sqrt{(k_m - k_e V_{bias}^2)/m} \qquad \text{(Eq 2-24)}$$

and the quality factor

$$Q = \frac{\sqrt{(k_m - k_e V^2_{bias})m}}{b} = \omega_n m/b. \qquad \text{(Eq 2-25)}$$

Eq. 2-24 and Eq. 2-23 shows that the negative electrostatic spring can be used to reduce the resonant frequency and increase the DC gain of the micropositioner. Excluding the negative electrostatic spring, micropositioners typically have resonant frequencies in the kilohertz range and quality factors much higher than one.

An example of micropositioner is described in Section 6.2.

2.6 Summary

In this chapter, micropositioner configurations have been reviewed. Their effects on magnitudes and linearities of capacitance variations and actuation forces have been discussed. For similarly sized structures, a transverse comb produces capacitance variations and actuation forces that are several times larger than those of a lateral comb. A transverse comb, however, has capacitance variations and actuation forces which are functions of displacement. The first one can limit the linearity in capacitive position sensing, while the latter one results in negative electrostatic spring and pull-in instability. The electromechanical model shows that the negative spring can be used to reduce the resonant frequency and increase the DC gain of a micropositioner. In contrast, the pull-in instability limits the maximum displacement of the structure to less than one-third of the gap.

Chapter 3

Capacitive Position Sensing for Micropositioners

3.1 Introduction

Traditionally, capacitive position sensing has been employed in sensor applications. In this research, we extend capacitive position sensing to interface with the electrostatic actuation of micropositioners. To ensure low cost, coupling capacitors are utilized to shield the high-voltage drive, thus allowing the sensing circuit to be fabricated in a conventional low-voltage technology.

In this chapter, we will first discuss two capacitance sensing techniques that are suitable for monolithic integration. Next, techniques to interface the three terminals of a capacitive half bridge to fully-differential sensing electronics will be described. The last section, and the core of this chapter, focuses on incorporating coupling capacitors with the sensing circuit. Guidelines on how to choose coupling capacitors and their impact on position resolution will be presented.

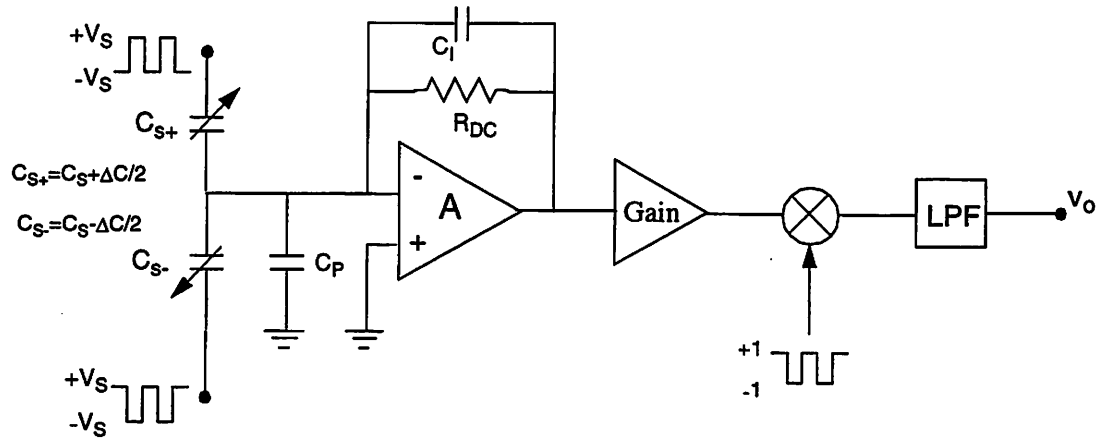


Fig. 3.1: An implementation of the synchronous detection scheme

3.2 Capacitance Sensing Techniques

Synchronous detection and switched-capacitor sensing schemes are two common capacitance sensing techniques in monolithic implementations. This is because—compared to other techniques such as LC oscillators, relaxation oscillators, and impedance measurement—they have signal transfer functions which are independent of the parasitic capacitance, offer high resolution, and do not require components with high quality factor. In this section, we will derive the signal and noise transfer function, and investigate the strengths, weaknesses, and fundamental sensing resolution of both schemes. Finally, it should be mentioned that, while the rest of this document focuses more on the switched-capacitor sensing scheme, the problems and techniques presented, except for the kT/C noise and correlated double sampling, are applicable to both schemes.

3.2.1 Synchronous Detection Scheme

The concept of synchronous detection is to reduce the impedance of the sensing capacitance by modulating it with a high frequency sensing voltage. Fig. 3.1

shows an implementation of the synchronous detection scheme. In this implementation, two out-of-phase high frequency sensing signals are applied to the sense capacitors. If the sense capacitors differ, an amount of charge proportional to the mismatch and the amplitude of the sensing voltage will be integrated by the charge integrator, thus resulting in an output voltage which is a function of the mismatch of the sense capacitors. The high frequency output voltage is then amplified and demodulated down to baseband by the synchronous demodulator. Next, the low-pass filter removes the offset and the 1/f noise of the electronics which is modulated up to high frequency by the demodulator. This offset and 1/f noise removal technique is commonly known as chopper stabilization. To set the DC voltage level at the amplifier input, which is a high impedance node, a large resistor is connected between the amplifier input and the output node. Sensitivities to parasitic capacitance is eliminated by the virtual ground condition at the amplifier input. An alternative implementation of the synchronous detection scheme uses a buffer [12] instead of the charge integrator as shown in this circuit.

The signal transfer function of the synchronous detection circuit in Fig. 3.1 is

$$v_o = \frac{\Delta C}{C_I} \cdot V_s \qquad \text{(Eq 3-1)}$$

where V_S is the amplitude of the sensing voltage. The output noise of this circuit, assuming that noise from the front-end amplifier and the DC-setting resistor dominates, is

$$\frac{\overline{v^2_{on}}}{\Delta f} = \left(\frac{2C_S + C_I + C_P + C_{IP}}{C_I}\right)^2 \cdot \frac{\overline{v^2_n}}{\Delta f} + \left|\frac{1}{j\omega C_I}\right|^2 \cdot \frac{4kT}{R_{DC}}, \qquad \text{(Eq 3-2)}$$

where $\overline{v^2_n}/\Delta f$ is the input-referred spectral density of the amplifier thermal noise and C_{IP} is the amplifier input capacitance.

Compared to the switched-capacitor sensing scheme, which will be discussed in the following section, the synchronous detection scheme does not suffer from the

kT/C sampling noise and noise folding, and avoids complicated clocking scheme. However, the synchronous detection scheme has two important drawbacks. First, the DC-setting resistor typically needs to be in the range of mega-ohms to ensure low current noise and to avoid a null in the frequency response due to charge leakage. In monolithic implementations, large resistors require large die area and have large parasitic capacitance which can lower the resolution, slow down the circuit, and add another pole to the amplifier frequency response. For example, the commercial accelerometer ADXL-50 requires a 3-megaohm DC-setting resistor fabricated with a special resistor layer available in that process. Alternatives to a large resistor include back-to-back connected diodes and a MOS resistor biased to ensure high resistance. Although these alternatives require smaller die area, their parasitic capacitances still contribute the additional pole.

Second, synchronous detection is not suitable for applications which involve feedback loops because the low-pass filter adds phase delay to the loop transfer function. For a digital control loop [13], a low-pass filter might not be needed inside the loop, but the high-frequency feedback signal applied to the moving element can propagate through the sensing circuit, as shown in Fig. 3.2, and results in a feedforward zero which degrades the measurement accuracy and the stability of the feedback loop.

3.2.2 Switched-Capacitor Sensing Scheme

Switched-capacitor circuits replace resistors by capacitors and switches. This results in smaller die area and much better matching and tracking. In a switched-capacitor sensing circuit, the sense capacitor is reset to ground or a reference level in each cycle, thus eliminating the need for a large resistor to set the DC level. The feedback feedthrough is eliminated by allocating a separate phase for the feedback operation. Furthermore, switched-capacitor sensing circuits offer more flexibility in the system integration because of the ability to allocate separate phases for different

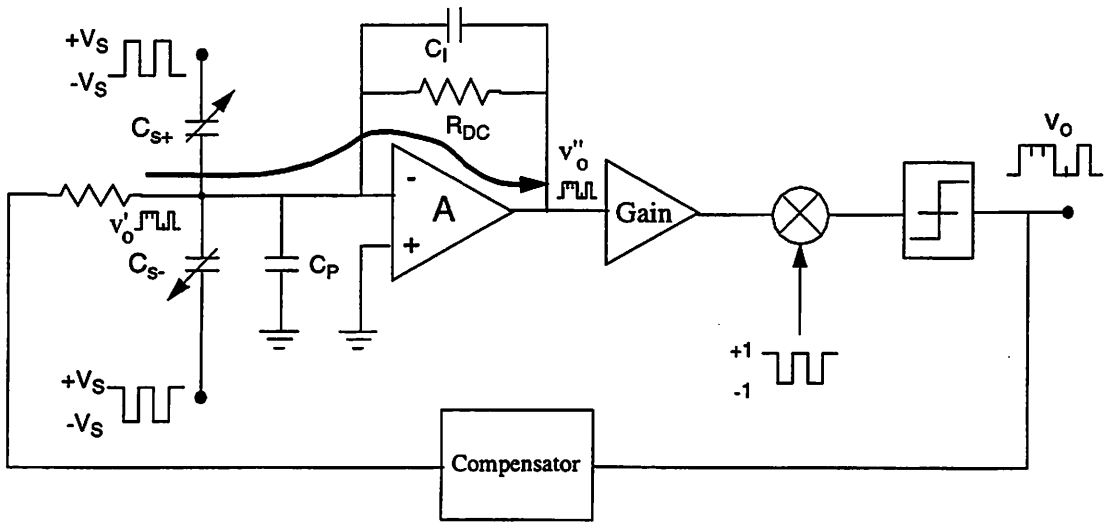


Fig. 3.2: A digital control loop utilizing a synchronous detection circuit. The high-frequency feedback applied to the common node can propagate through the sensing circuit, resulting in a feedforward zero.

operations such as sensing, driving, feedback, comparison, and digital signal processing.

Fig. 3.3 shows a typical implementation of the switched-capacitor sensing scheme. This circuit is identical to a switched-capacitor gain stage, except that the input is a capacitance variation instead of a voltage variation. During the reset phase, the sense capacitors, the integrating capacitor, and the amplifier are reset to ground or a reference level. During the sensing phase, the sensing voltages $\pm V_S$ are applied to the sense capacitors. An amount of charge proportional to the mismatch in sense capacitors C_{S+} and C_{S-} and the sensing voltage is integrated on C_I and produces an output voltage, which is then sampled by C_L. The signal transfer function of this circuit is

$$v_o = \frac{\Delta C}{C_I} \cdot V_s \qquad \text{(Eq 3-3)}$$

and identical to that of the synchronous detection circuit given in Eq. 3-1.

There are two thermal noises associated with this sensing circuit: the sampling noise due to switch S_1 or the kT/C noise and the amplifier noise sampled by the load

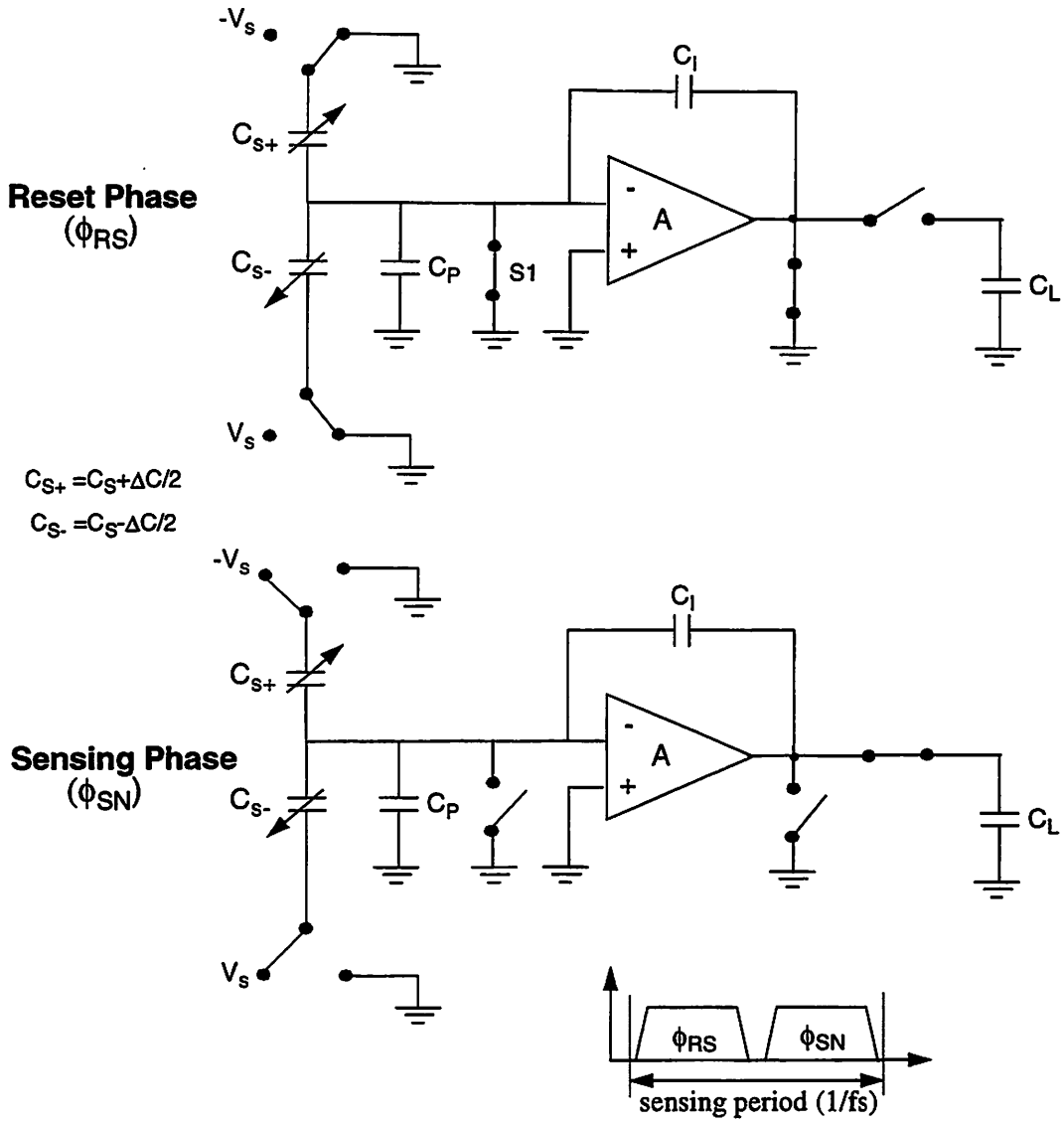


Fig. 3.3: A typical implementation of the switched-capacitor sensing scheme.

capacitance C_L. The derivation of these noises are given in Appendix 1 with the results stated below. The output-referred spectral density of the kT/C noise is

$$\frac{\overline{v_{kT/C}^2}}{\Delta f} = \frac{1}{f_s} \cdot \left(\frac{C_T}{C_I}\right)^2 \cdot \frac{kT}{C_T} \qquad \text{(Eq 3-4)}$$

where $C_T=2C_S+C_I+C_P+C_{IP}$ is the total capacitance at the amplifier summing node. And the spectral density of the amplifier noise sampled by the load capacitance C_L is

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \left(\frac{C_T}{C_I}\right)^2 \cdot \frac{\overline{v_n^2}}{\Delta f} \cdot \frac{f_u}{f_s} \cdot \frac{\pi}{2} \qquad \text{(Eq 3-5)}$$

where $\overline{v_n^2}/\Delta f$ is the input-referred spectral density of the amplifier thermal noise and f_u is the closed-loop bandwidth of the amplifier.

3.2.3 Sensing Resolution

Fundamentally, the resolution of a position sensing circuit is limited by the thermal noise of the sensing electronics or Brownian motion of the sense element. In practice, nonidealities often prevent the sensing circuit from achieving the fundamental resolution. Nevertheless, the fundamental sensing resolution provides us a benchmark to compare the achieved resolution to the fundamental limit and to compare the merits of different sensing techniques.

The sensing resolution is defined as the position or capacitance variation that results in an output signal which has a signal-to-noise ratio of one,

$$\sqrt{\overline{v_{no}^2}} = v_o = \frac{dv_o}{dC} \cdot \Delta C_{min} = \frac{dv_o}{dC} \cdot \frac{dC}{dx} \cdot \Delta x_{min} \qquad \text{(Eq 3-6)}$$

where $\sqrt{\overline{v_{no}^2}}$ is the output noise voltage of the sensing circuit. Rearranging this equation in terms of capacitance resolution and the position resolution,

$$\Delta C_{min} = \frac{\sqrt{\overline{v_{no}^2}}}{\frac{dv_o}{dC}} \qquad \text{(Eq 3-7)}$$

and

$$\Delta x_{min} = \frac{\Delta C_{min}}{\frac{dC}{dx}} = \frac{\sqrt{\overline{v_{no}^2}}}{\frac{dv_o}{dC} \cdot \frac{dC}{dx}}. \qquad \text{(Eq 3-8)}$$

Since this research focuses on the design of the sensing circuit, we will assume that the contribution from Brownian motion is negligible compared to the thermal noise of the sensing electronics. For the synchronous detection circuit described in Section

3.2.1, the capacitance resolution can be calculated from the signal and the noise transfer functions in Eq. 3-1 and Eq. 3-2, assuming a large R_{DC} to minimize its noise contribution, as

$$\sqrt{\frac{\overline{\Delta C_{min}}}{\Delta f}} = (2C_S + C_I + C_P + C_{IP}) \cdot \sqrt{\frac{\overline{v_n^2}}{\Delta f}} \cdot \frac{1}{V_s}. \qquad \text{(Eq 3-9)}$$

For the switched-capacitor sensing circuit described in Section 3.2.2, the resolution can be calculated from the signal and noise transfer functions in Eq. 3-3 to Eq. 3-5 as

$$\sqrt{\frac{\overline{\Delta C_{min}}}{\Delta f}} = \frac{1}{V_s} \cdot \sqrt{\left(\frac{kTC_T}{f_s}\right)_{\frac{kT}{C}} + \left(\frac{C_T^2 \overline{v_n^2} f_u \frac{\pi}{2}}{f_s}\right)_{opamp}} \qquad \text{(Eq 3-10)}$$

where the first term is due to the kT/C noise of switch S_1, the second term is due to the amplifier thermal noise, and C_T is equal to $2C_S+C_I+C_P+C_{IP}$. In the next chapter, it will be shown that the kT/C noise term, which is typically the dominant thermal noise source in micromachined applications, can be eliminated by correlated double sampling. Taking into account the kT/C noise cancellation and the factor-of-two amplifier noise increase due to double sampling, Eq. 3-10 becomes

$$\sqrt{\frac{\overline{\Delta C_{min}}}{\Delta f}} = \frac{1}{V_s} \cdot \sqrt{\left(\frac{C_T^2 \overline{v_n^2} f_u \pi}{f_s}\right)_{opamp}}. \qquad \text{(Eq 3-11)}$$

Comparing the sensing resolution of switched-capacitor sensing circuits to that of the synchronous detection circuits yields,

$$\frac{\Delta C_{min,\ swcap}}{\Delta C_{min,\ sync\ detection}} = \sqrt{\frac{\pi f_u}{f_s}}. \qquad \text{(Eq 3-12)}$$

This ratio is typically in the order of three to four due to the noise folding and the double sampling, thus suggesting that the fundamental resolution of switched-capacitor sensing circuits is three to four times lower than that of synchronous detection circuits.

To illustrate the exceptional fundamental resolution of capacitive position sensing, an example is given for a switched-capacitor sensing circuit. For $C_S=C_I=1pF$,

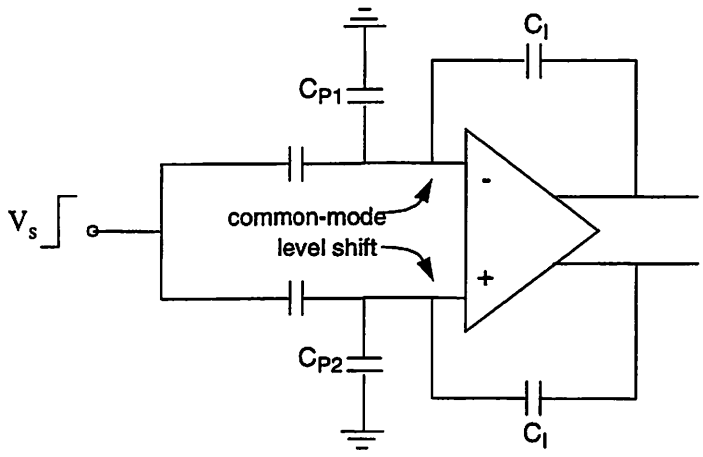


Fig. 3.4: A pseudo-differential switched-capacitor circuit and the input common-mode level shift due to the applied sensing voltage.

$C_P+C_{IP}=5pF$, $\sqrt{v_n^2}/\Delta f = 5nV/\sqrt{Hz}$, $f_u/f_s=3$, and $V_s=1V$, the capacitance sensing resolution, according to Eq. 3-11, is $1.23 \cdot 10^{-19}fF/\sqrt{Hz}$. With a $dC/dx=100fF/\mu m$, the position sensing resolution is $1.23 \cdot 10^{-12}m/\sqrt{Hz}$, approximately a factor of 200 smaller than the classical diameter of a hydrogen atom.

To conclude, the switched-capacitor sensing scheme eliminates the need for DC-setting resistor and offers flexibility in system integration through multi-phase operations. On other hand, it has a lower fundamental resolution and requires more complicated clocking scheme.

3.3 Pseudo-Differential Topology

Fully differential topology is desirable because it reduces noise coupling and feedthrough (See Section 5.3), improves power-supply rejection ratio, eliminates even-order harmonics, and improves dynamic range by doubling the output swing. In micromachined applications, fully differential topology normally cannot be achieved because differential sense capacitors, such as that of comb structures, have one common electrode. A solution is to use the pseudo-differential topology shown in Fig. 3.4. In

this topology, the sensing voltage is applied to the common node of the differential capacitors, while the other two electrodes are connected to the amplifier summing nodes, thus allowing the use of fully-differential sensing electronics.

The drawback of the pseudo-differential circuit in Fig. 3.4 is the shift of the amplifier input common-mode level when the sensing voltage is applied. This complicates the amplifier design by requiring a large input common-mode range. Furthermore, with the loss of the virtual ground condition, the signal transfer function becomes a function of the parasitics at the amplifier summing node.

From Eq. A2-5 and Eq. A2-9 in Appendix 2, the input common-mode shift is approximately

$$V_{icm} \approx \frac{C_S}{C_T} \cdot V_s \qquad \text{(Eq 3-13)}$$

where $C_T=C_S+C_I+C_P+C_{IP}$. Because of the input common-mode shift, the signal transfer function becomes

$$V_o \approx \{-\Delta C_S(C_I + C_P + C_{IP}) + \Delta C_P \cdot C_S\} \cdot \frac{V_s}{C_I C_T} \qquad \text{(Eq 3-14)}$$

Compared to the transfer functions given in Eq. 3-1 and Eq. 3-3, the capacitive-to-voltage gain becomes a function of the parasitics C_P, which is not a well-controlled parameter. Besides, the parasitic mismatch ΔC_P, which can be much larger than the sense capacitance variation ΔC_S, produces an additional offset term.

A new circuit technique called "input common-mode feedback" (IPCMFB) is introduced to solve this problem. This circuit was implemented in reference [13] and can be shown conceptually in Fig. 3.5. Similarly to the output common-mode feedback circuit, the IPCMFB amplifier monitors the input common-mode level and applies a correction charge through C_X to restore the input common-mode level. With the input common-mode shift eliminated, there is no need for an amplifier with a large input common-mode range and the signal transfer function is reverted to the initial ones

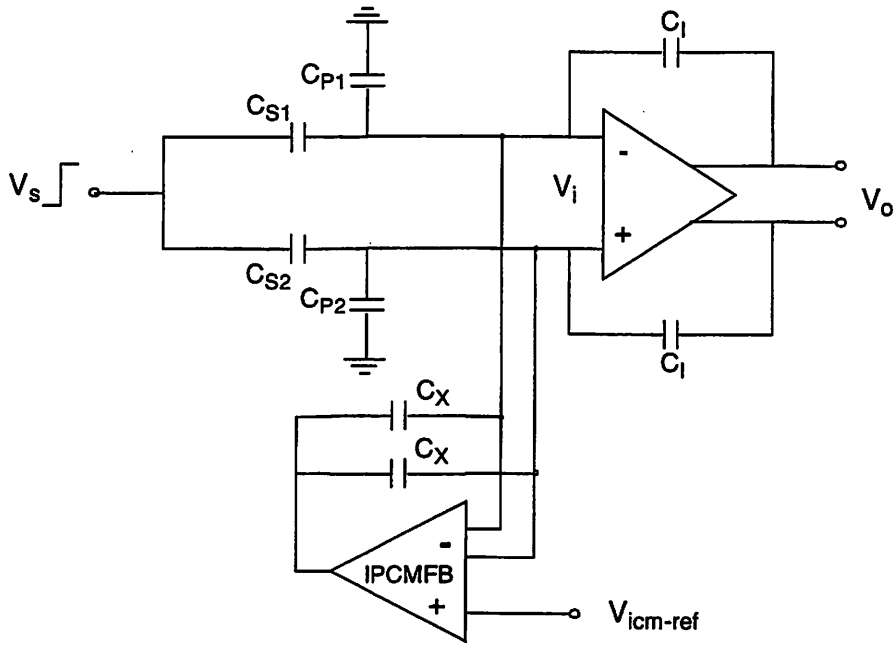


Fig. 3.5: A pseudo-differential switched-capacitor circuit with an input common-mode feedback circuit to eliminate the input common-mode shift

given in Eq. 3-1 and Eq. 3-3. The drawback of the IPCMFB circuit, however, is the added circuit complexities, extra capacitance at the summing node, and cascaded settling of the input and output common-mode feedback circuit [8].

3.4 High-Voltage Interface of the Sensing Electronics

To generate sufficient forces, micropositioners are typically driven by voltages much higher than those normally used in conventional integrated circuits. For instance, in the dual-stage servo system for magnetic disk drives, micropositioners are driven by voltages as high as 80V or ±40V. This suggests that, for the driving and the sensing to share a single set of electrodes, the sensing circuit needs to interface with the high-voltage drive of the micropositioner. In this section, we will discuss the use of coupling capacitors to shield the sensing circuitry from the driving voltages, thus allowing the sensing circuit to be fabricated in a conventional low-voltage process.

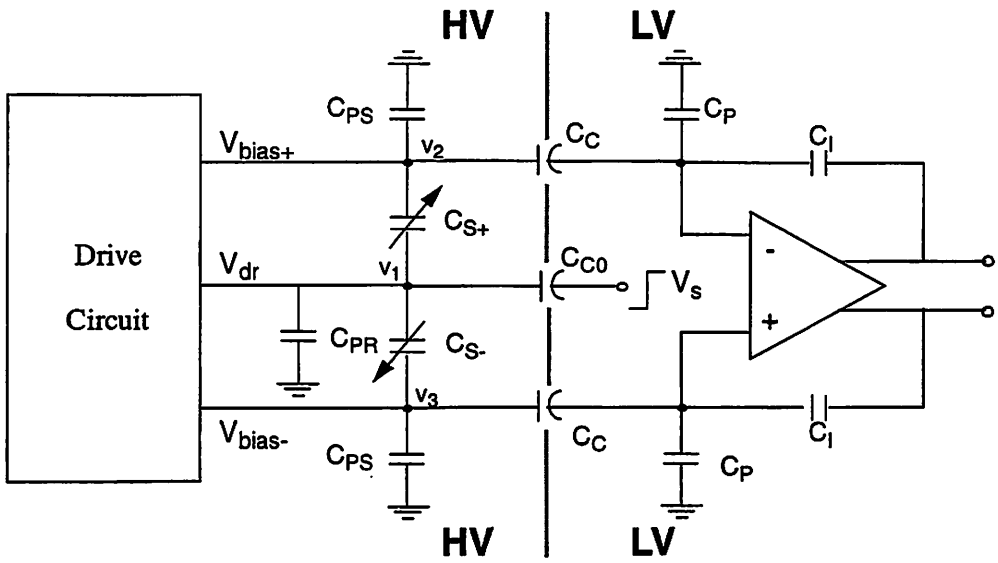


Fig. 3.6: Coupling capacitors are inserted between the charge integrator and the micropositioner to shield the sensing circuit from the high-voltage drive of the micropositioner.

3.4.1 Coupling Capacitors

Fig. 3.6 shows an interface between driving and position sensing. The driving voltages are applied to the micropositioner at nodes v_1, v_2, and v_3. The coupling capacitors C_{C0} and C_C are inserted between the charge integrator and the micropositioner to shield the sensing circuit from the driving voltages. The DC voltage at the amplifier summing nodes is established by reset switches or resistors, depending on the sensing circuit implementations.

A key consideration in implementing the coupling capacitors is the oxide breakdown because coupling capacitors need to shield the driving voltages of the micropositioner. For thermally grown oxide (SiO_2), an oxide field of 7×10^6 V/cm generally leads to irreversible breakdown. To allow some safety margin, oxide fields are usually limited to about 3×10^6 V/cm [14].

Table 3.1: A comparison of poly-poly and metal-metal capacitors from a 1.2-μm CMOS process

	Poly-poly capacitor	Metal-metal capacitor
Oxide thickness (Angstrom)	700	7500
Breakdown voltage (E_{ox}=3x10^{6}V/cm)	21V	225V
Capacitance per unit area	0.49fF/μm^2	0.046fF/μm^2
Bottom-plate parasitics to actual capacitance ratio	0.15	0.78

Table 3.1 compares poly-poly and metal-metal capacitors from a 1.2-μm CMOS process. Metal-poly capacitors are not considered because of their generally higher nonlinearity. Despite much smaller area and bottom-plate parasitics of poly-poly capacitors, metal-metal capacitors are needed in this application because of the high-voltage drive of the micropositioner. Compared to poly-poly capacitors, metal-metal capacitors require ten times more area and have five times larger bottom-plate parasitics. These penalties can be reduced in processes with more than two layers of metal by stacking all the metal layers to implement the coupling capacitors. Additionally, to avoid the driving voltages from modulating the bottom-plate parasitic capacitance and causing a gain error, the driving voltages should be connected to the top plates of the coupling capacitors or the bottom-plates need to be shielded by a layer underneath such as poly.

3.4.2 Modified transfer function

In this section, we will derive the transfer function of the capacitance sensing circuit with coupling capacitors. To keep the transfer function intuitive, the input

common-mode shift of the amplifier is assumed to be zero. For typical parameters, the error due to this approximation is approximately a 20-percent overestimation of the transfer function.

Due to the capacitive voltage divider between C_{C0} and the rest of the capacitance at the rotor node, the step voltage at node V_1 due to the applied step sensing voltage V_S is approximately

$$V_1 \approx \left(\frac{C_{C0}}{C_{C0} + C_{PR} + \frac{2C_S(C_{PS} + C_C)}{C_S + C_{PS} + C_C}} \right) \cdot V_S \ . \qquad \text{(Eq 3-15)}$$

Since $C_{PS}+C_C$ is typically much larger than C_S, this equation can be approximated as

$$V_1 \approx \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S} \right) \cdot V_S \ . \qquad \text{(Eq 3-16)}$$

Again, the capacitive voltage dividers between C_S and the rest of the capacitance at the stator nodes reduce the steps at node V_2 and V_3 to

$$V_2, V_3 \approx \left(\frac{C_S \pm \Delta C_S/2}{C_S + C_C + C_{PS}} \right) \cdot V_1 \ . \qquad \text{(Eq 3-17)}$$

Since we assume no input common-mode voltage shift, the amplifier summing nodes are virtual ground nodes. Hence, the output voltage of the charge integrator is equal to

$$V_o = -(V_2 - V_3) \cdot \frac{C_C}{C_I} \ . \qquad \text{(Eq 3-18)}$$

Substituting Eq. 3-16 and Eq. 3-17 in Eq. 3-18 yields

$$V_o = \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S} \right) \cdot \left(\frac{C_C}{C_C + C_{PS} + C_S} \right) \cdot \frac{-\Delta C_S}{C_I} \cdot V_S \ . \qquad \text{(Eq 3-19)}$$

Comparing Eq. 3-19 to Eq. 3-1 and Eq. 3-3 shows that the signal attenuation due to the coupling capacitors is equal to

$$\delta = \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S} \right) \cdot \left(\frac{C_C}{C_C + C_{PS} + C_S} \right) \qquad \text{(Eq 3-20)}$$

where the first term is due to the capacitive voltage divider at the rotor node and the second term is due to the charge divider from C_S to the amplifier summing node. According to this result, the attenuation can be minimized by choosing

$$C_{C0} \gg 2C_S + C_{PR} \quad \text{and} \quad C_C \gg C_S + C_{PS}. \qquad \text{(Eq 3-21)}$$

Increasing the signal coupling by using large coupling capacitors, however, do not always result in higher resolution because of increasing parasitics and noise, as will be shown in the following section.

3.4.3 Optimal Coupling Capacitance

Determining the size and the bottom-plate connection of coupling capacitors involves several tradeoffs. Our strategy is to initially find the optimal configuration and size of coupling capacitors in term of resolution, then impose other constraints such as die area and loading to the micropositioner driving circuits.

By examining the circuit in Fig. 3.6, the top plate of C_{C0} should be connected to node V_1 to avoid adding the bottom-plate parasitics to C_{PR}. The bottom plate of C_C, however, can be connected in either direction. If the bottom plate of C_C is connected to the high-voltage node, the bottom-plate capacitance adds to the parasitics C_{PS} thus reducing the signal coupling and increasing the load to the driving circuit. Additionally, a shielding layer must be added underneath to prevent the high voltage from forming an inversion layer underneath the bottom plate. On the other hand, if the bottom plate is connected to the charge integrator, the bottom-plate capacitance adds to the parasitics at the summing node thus increasing the noise gain and slowing down the amplifier.

The capacitance resolution of switched-capacitor sensing circuits with coupling capacitors can be calculated from Eq. 3-19 and Eq. 3-11. For a circuit which the bottom plate of C_C is connected to the charge integrator,

$$\Delta C_S \approx \left(\frac{C_{C0} + C_{PR} + 2C_S}{C_{C0}}\right) \cdot \left(\frac{C_C + C_{PS} + C_S}{C_C}\right) \cdot \frac{(C_C + C_{CP} + C_P + C_I)}{V_S} \cdot \sqrt{\overline{v_n^2} \frac{f_u \pi}{f_s 2}} \qquad \text{(Eq 3-22)}$$

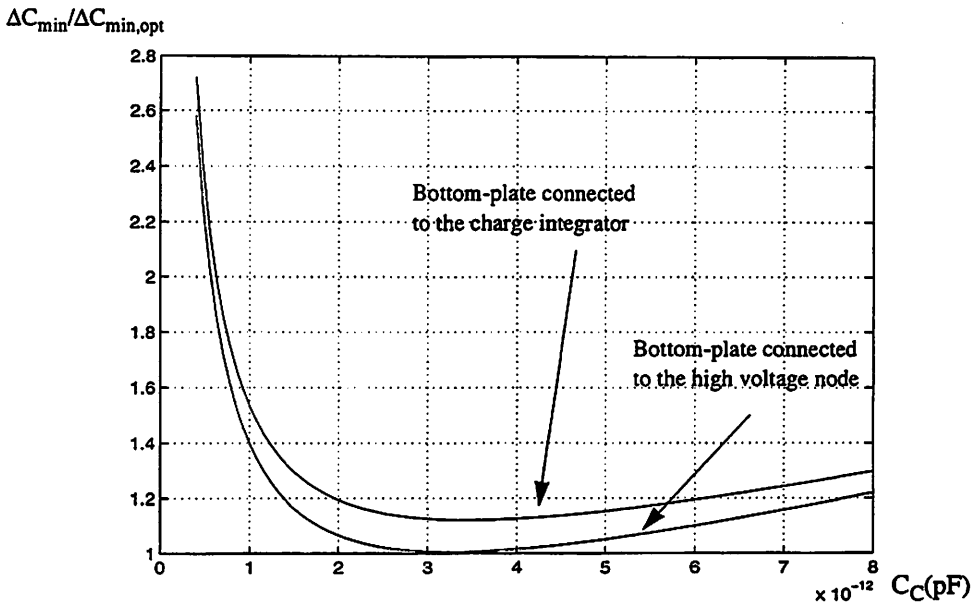


Fig. 3.7: Relationships between capacitance sensing resolution and the size of coupling capacitors C_C for C_S=C_I=1pF, C_P=2pF, and C_{PS}=7pF

where C_{CP} is the bottom-plate parasitics of C_C and C_P is other parasitics at the amplifier summing node. For a circuit which the bottom plate of C_C is connected to the high voltage node

$$\Delta C_S \approx \left(\frac{C_{C0}+C_{PR}+2C_S}{C_{C0}}\right)\cdot\left(\frac{C_C+C_{CP}+C_{PS}+C_S}{C_C}\right)\cdot\frac{(C_C+C_P+C_I)}{V_S}\cdot\sqrt{\overline{v_n^2}\,\frac{f_u\pi}{fs\,2}} \quad \text{(Eq 3-23)}$$

The results from Eq. 3-22 and Eq. 3-23 suggest that the coupling capacitor C_{C0} should be as large as possible. This is because C_{C0} increases the signal coupling without increasing the noise. The maximum value of C_{C0} is generally limited by the die area requirement and the loading to the rotor driving circuit. Large C_C, in contrary, increase both the signal coupling and noise. The noise increase is due to the increase in capacitance at the amplifier summing node, which in turn increases the noise gain from the amplifier input to the output by reducing the feedback factor. Relationships between the capacitance resolution and coupling capacitor C_C of both bottom-plate configurations are shown in Fig. 3.7 for typical parameters. In the implementation described in Chapter 6, the bottom-plates of C_C are connected to the charge integrator,

despite slightly lower resolution, because connecting the bottom-plates to the high voltage nodes increases the loading to the driving circuit and reduces the capacitive-to-voltage gain.

For metal-metal capacitors, the ratio between C_C and C_{CP}, as shown in Table 3.1, is approximately one. Using this assumption, the optimal C_C can be calculated from Eq. 3-22 as

$$C_{C,\,opt} = \sqrt{\frac{(C_S + C_{PS})(C_P + C_I)}{2}}. \qquad \text{(Eq 3-24)}$$

For typical parameters—C_S=1pF, C_I=1pF, C_P=2pF, and C_{PS}=7pF, the optimal C_C is 3.46pF, a large but attainable size in monolithic integration. With V_S=5V, $\sqrt{\overline{v_n^2}}$ = 10nV/$\sqrt{\text{Hz}}$, f_u/f_s=5, C_{PR}=10pF, and C_{C0}=C_C, the capacitance resolution, according to Eq. 3-22, is 0.82 aF/$\sqrt{\text{Hz}}$, which is adequate for the magnetic disk drive application.

Neglecting the increase in noise, the reduction in capacitance resolution due to the coupling capacitors is equal to the signal attenuation factor given in Eq. 3-20. Substituting C_{C0}, C_C, C_{PR}, C_{PS}, and C_S from the previous example into Eq. 3-20 yields a factor of 15 reduction in capacitance resolution. To reduce this penalty, parasitic capacitances C_{PR} and C_{PS} should be minimized while the coupling capacitor C_{C0} should be maximized.

3.4.4 ESD Protection

Even though the input devices of the front-end amplifier are shielded from the micropositioner driving voltages by the coupling capacitors, an electrostatic discharge or a sudden change in the driving voltage, particularly while the sensing circuit is not being operated, can still create a high voltage at the gates of input devices, resulting in gate oxide breakdown. In contrast to typical circuits, ESD protection circuits cannot be added at the high-voltage plates of the coupling capacitors because the driving voltages

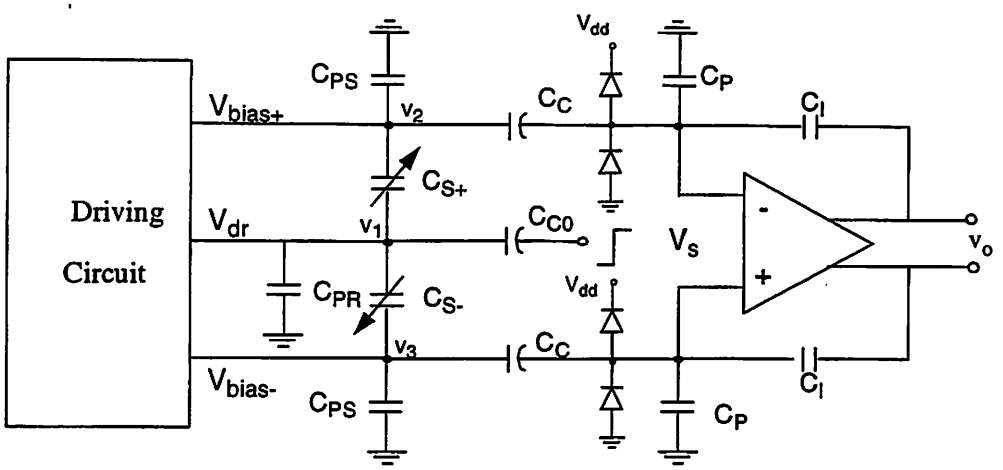


Fig. 3.8: ESD protection circuits are added at the amplifier summing nodes to protect the input devices of the amplifier.

will cause the protection circuits to turn on. The solution, as shown in Fig. 3.8, is to add protection circuits at the amplifier summing nodes. Since the electrostatic discharge is partially shielded by the coupling capacitor, the protection circuits can be scaled down to minimize the parasitics at the amplifier summing nodes.

3.5 Summary

Synchronous detection scheme and switched-capacitor sensing scheme are attractive in monolithic implementations because they can achieve high resolution without requiring components with high quality factor and are insensitive to parasitics. Comparisons between the two techniques conclude that the switched-capacitor sensing scheme fundamentally has two to four times lower resolution than the synchronous detection scheme, but offers several advantages such as the elimination of the DC-setting resistor and its noise contribution, the absence of feedback feedthrough in a high-frequency digital control loop, and more flexibility in system integration.

Pseudo-differential topology, instead of fully-differential topology, is employed in capacitance sensing circuits because sense capacitors typically have only three terminals. The drawback of this topology is the shift of the amplifier input common-mode level, which requires an amplifier with a large input-common mode range and causes the signal transfer function to become a function of the parasitics at the amplifier summing node. To alleviate this problem, a circuit technique called "input common-mode feedback" (IPCMFB) has been proposed.

In typical applications, the micropositioner driving voltages can be as large as tens or hundreds of volts in order to generate sufficient forces. To allow the position sensing circuit to be fabricated in a conventional CMOS process, coupling capacitors are needed to shield the sensing circuit from the high-voltage drive of the micropositioner. To minimize the reduction in capacitance-to-voltage gain and resolution, the bottom-plate connection and the size of the coupling capacitors must be chosen carefully. Due to constraints such as die area, power consumption, and loading to the micropositioner driving circuit, the reduction in resolution by a factor of ten or more is not uncommon.

Chapter 4

Nonidealities in the Sensing Electronics

4.1 Introduction

In practice, various nonidealities prevent position sensing circuits from achieving the fundamental resolution described in the last chapter. Nonidealities associated with position measurement of micropositioners can be classified into two groups. The first group, which will be discussed in this chapter, is associated with the sensing electronics. In microsensors, these nonidealities often are the factors limiting the sensing resolution. In micropositioners, these nonidealities tend to dominate when the driving voltages are small. The second group, which will be discussed in the next chapter, is associated with the integration of the position sensing and the high-voltage driving. These nonidealities typically dominate at large driving voltages, especially in micropositioners which utilize single sets of electrodes for both sensing and driving.

The discussion in this chapter will focus on switched-capacitor sensing circuits. Nevertheless, all of the results, except for the correlated double sampling and the kT/C noise cancellation, are applicable to synchronous detection circuits. We will begin from investigating sources of errors in switched-capacitor sensing circuits, namely the amplifier offset and 1/f noise, the switch charge injection, and the kT/C

noise. Then, we will demonstrate that correlated double sampling, which are normally used to attenuate the first two, can be extended to attenuate the latter two. With the kT/C noise removed, the amplifier thermal noise becomes the dominant thermal noise source and needs to be optimized. Finally, noise improvement due to the kT/C cancellation will be calculated.

4.2 Errors in Switched-Capacitor Sensing Circuits

Compared to the synchronous detection scheme, the switched-capacitor sensing scheme introduces switch charge injection and kT/C noise due to switching operations. These errors combining with the amplifier offset and 1/f noise decrease the sensing resolution. In this section, we will investigate these errors and available techniques to eliminate them.

4.2.1 Amplifier Offset

In MOS amplifiers, offsets are caused by mismatches in the device dimension and the threshold voltage, and can be reduced by using large devices and common-centroid layout. The offset in a carefully designed MOS amplifier is in the range of a few millivolts and typically overwhelm the output signal of the sensing circuit. As an example, a switched-capacitor sensing circuit with $C_S=C_I=1pF$, $C_P+C_{IP}=5pF$, and $V_S=1V$, produces an output of $10\mu V$ for a sense capacitance variation of 10aF. Meanwhile, an amplifier offset of 5mV produces an output-referred offset of 35mV, a factor of 3,500 larger than the signal. To eliminate the offset, an offset cancellation technique such as chopper stabilization or correlated double sampling is needed.

4.2.2 Amplifier 1/f noise

For a MOS transistor biased in the saturation region, the 1/f noise is inversely proportional to the frequency and the gate capacitance of the device,

$$\frac{\overline{v_{1/f}^2}}{\Delta f} = \frac{K_f}{WLC_{ox}f} \qquad \text{(Eq 4-1)}$$

A typical value for K_f is 1×10^{-24} to $3 \times 10^{-24} V^2F$ for NMOS. Depending on the process, K_f for PMOS can be smaller by a factor of two or more [15].

A parameter typically used to describe 1/f noise is the '1/f noise corner'. The 1/f noise corner is defined as the frequency in which the 1/f noise has the same energy as the thermal noise. For a square-law device, the 1/f noise corner is

$$f_c = \frac{3\mu K_f V_{dsat}}{8kTL^2} \qquad \text{(Eq 4-2)}$$

where μ is the mobility of the device. The 1/f noise corner is generally in the megahertz range for devices with channel length in the order of 1μm.

Typically, 1/f noise is reduced by using PMOS devices or large devices. These techniques, however, do not work well in micromachined applications because mechanical signals concentrate in the low frequency range and often extend down to DC, thus requiring extremely large devices to suppress the 1/f noise. Since 1/f noise is essentially a slowly varying amplifier offset, offset-cancellation techniques can partially remove the 1/f noise. For example, chopper stabilization attenuates the 1/f noise by shifting it to high frequency, while correlated double sampling has a shaping function which attenuates noise at low frequencies.

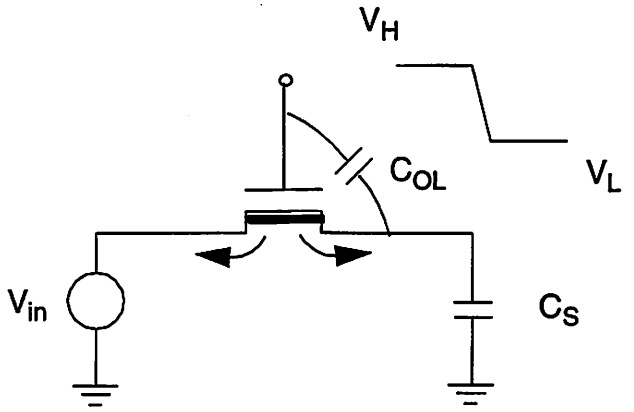


Fig. 4.1: Charge injection and clock feedthrough mechanisms in a MOS switch

4.2.3 Switch Charge Injection

Channel charge injection and clock feedthrough are two errors associated with the turning off process of a MOS switch. Generally, both of them are referred to as charge injection. For the switch in Fig. 4.1, the error charge on the sampling capacitor C_S for fast switching conditions can be approximated as

$$\Delta Q_{out} \approx -\left(\frac{C_{OL}C_S}{C_{OL}+C_S}(V_H - V_L)\right) - \frac{Q_{CH}}{2} \qquad \text{(Eq 4-3)}$$

$$\approx -\left[C_{OL}(V_H - V_L) + \frac{WLC_{ox}(V_H - V_{in} - V_{th})}{2}\right] \qquad \text{(Eq 4-4)}$$

where the first term is due to the clock feedthrough and the second term is due to the channel charge injection. As an example, for V_H=5V, V_L=0V, V_{in}=0V, V_{th}=1V, C_{ox}=1fF/μm^2, W=25μm, L=1μm, LD=0.1μm, the charge error due to the clock feedthrough is 12.5fC and that due to the charge injection is 50fC. These charge errors are orders of magnitude larger than the signal charge, $\Delta C \cdot V_S$, from the sense capacitors, which can be as small as atto-coulombs.

Several techniques to cope with the charge injection and the clock feedthrough have been studied. A typical approach is to use a combination of differential circuits

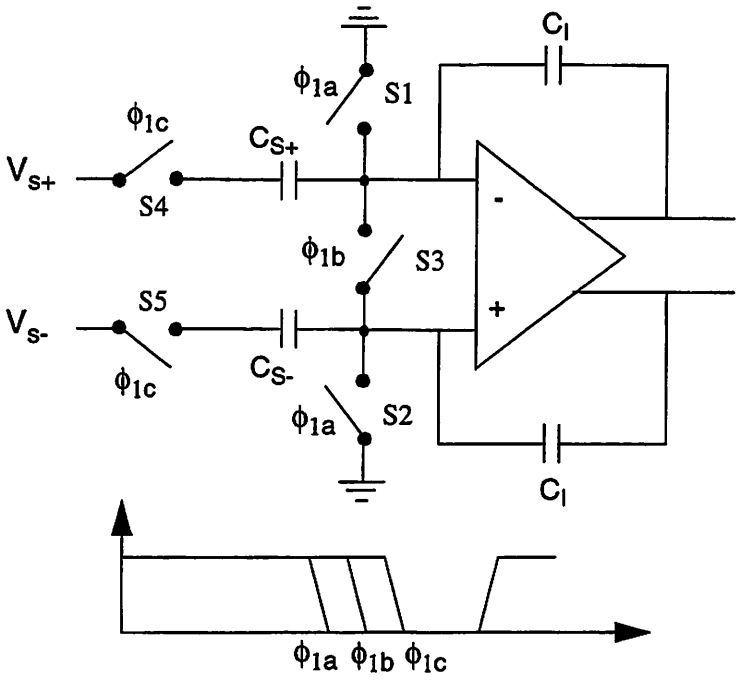


Fig. 4.2: A differential circuit with bottom-plate sampling and a center switch.

with bottom-plate sampling and a center switch as shown in Figure 4.2. This circuit uses switch S_3 to equalize any mismatch in charge injection between switch S_1 and S_2 and relies on even charge injection from switch S_3 in both source and drain directions. This scheme works well, except in applications such as micropositioners, where the mismatch between C_{S+} and C_{S-} can be significant. The mismatch in C_{S+} and C_{S-} results in different impedances when looking from the source and the drain of switch S_3. This, in turns, creates an uneven charge injection from switch S_3, which is a function of the capacitance variation. Similarly to the offset and 1/f noise, chopper stabilization or correlated double sampling can attenuate this uneven charge injection.

4.2.4 kT/C Noise

In switched-capacitor sensing circuits, kT/C noise is often larger than the amplifier thermal noise. Typically, kT/C noise can be reduced by increasing the size of

Table 4.1: A summary of errors in switched-capacitor circuits and means to attenuate them. '**x**' signifies that the means is effective.

Error type	Chopper stabilization	Correlated double sampling	Other techniques
Offset	X	X	Large geometry Common-centroid layout
1/f noise	X	X	Large geometry Long channel length PMOS device
Charge injection and clock feedthrough	X	X	Bottom-plate sampling Dummy switches
kT/C noise	N.A.	X	Large sampling capacitors High sensing frequency

the sampling capacitors. This, however, is not feasible in micromachined applications because the sense capacitance is usually limited to hundreds of femtofarads by the size restriction of the sense element. The other alternative to reducing the kT/C noise is to increase the sampling frequency. According to Eq. 3-4, the sampling frequency must be increased by 10 times in order to reduce the kT/C noise by 10dB. Such a large increase in the sampling frequency is not desirable because of increasing complexities in system design and high power consumption. Correlated double sampling, as will be discussed in the next section, can cancel the kT/C noise without increasing the sampling frequency.

Now that we have discussed these four errors, we will summarize the available means to attenuate these errors in Table 4.1.

4.3 Correlated Double Sampling

In this section, we will discuss the use of correlated double sampling (CDS) to eliminate the errors associated with switched-capacitor sensing circuits as discussed earlier in the last section. Correlated double sampling was first proposed in references [16] and [17] for charge-coupled device (CCD) applications. In switched-capacitor circuits, CDS has traditionally been used to cancel the amplifier offset and 1/f noise, but not the switch charge injection and the kT/C noise [18]-[21]. This is mainly because switch charge injection can be minimized through the use of differential signal path and bottom-plate sampling, and kT/C noise can be reduced by increasing the capacitor size. In micromachined applications, the sense capacitor size is limited by the fabrication technology and is usually in the range of hundreds of femtofarads. Furthermore, as discussed in Section 4.2.3, charge injection in a differential circuit can be uneven because of large variations in sense capacitance. Therefore, the needs to extend CDS to cancel charge injection and kT/C noise become apparent.

Since switch charge injection and kT/C noise occur when the sampling switch is opened and remain constant until the next cycle, a sensing phase can be added to a conventional correlated double sampling circuit to sample these errors [22], [23]. This concept can be illustrated by the circuit in Fig. 4:3. During the reset phase ϕ_{RS}, all capacitors and the amplifier are reset. At the end of ϕ_{RS}, the switch S_1 and S_2 are opened. The charge injection and kT/C noise is contributed by switch S_1. During ϕ_{SN1}, the amplifier offset and 1/f noise, charge injection, and kT/C noise are amplified by the amplifier and stored on the holding capacitor C_H. At the end of ϕ_{SN1}, switch S_3 is opened. During ϕ_{SN2}, the sense capacitor is reconnected to the sensing voltage V_S. The amplifier output, which contains both the signal and the error, is subtracted by the error voltage previously stored in C_H. Since all the errors remain virtually unchanged during ϕ_{SN1} and ϕ_{SN2}, the output voltage v_o contains only the signal.

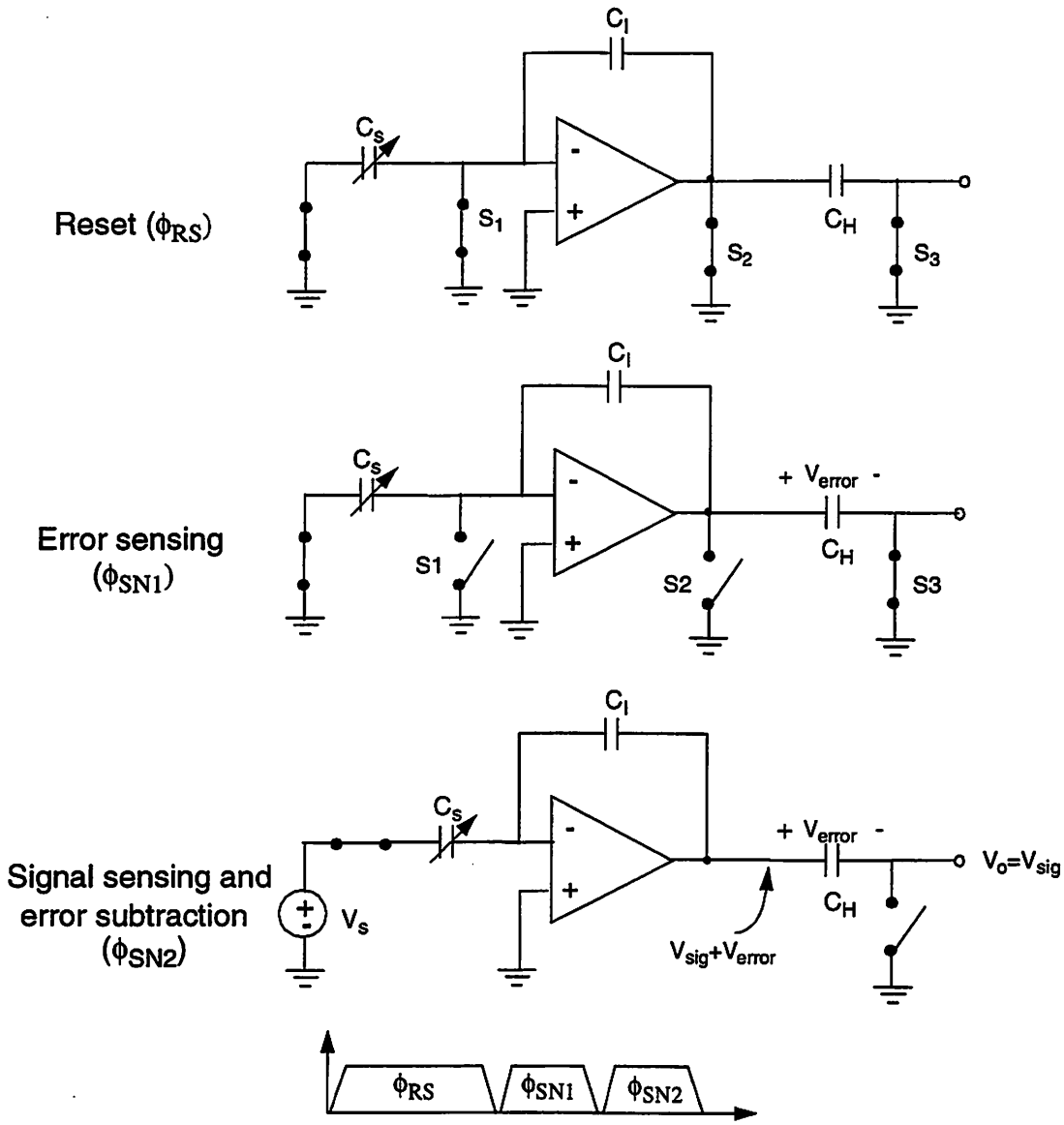


Fig. 4.3: Operations of a switched-capacitor sensing circuit with correlated double sampling. The error is stored on C_H at the amplifier output.

Correlated double sampling, to the first order, eliminates the offset, charge injection, and kT/C noise. The 1/f noise, on the other hand, is attenuated by a noise shaping function. The noise shaping function, assuming a duty cycle of 25% for each sensing phase, is

$$H_{CDS}(z) = 1 - z^{-1/4} \qquad \text{(Eq 4-5)}$$

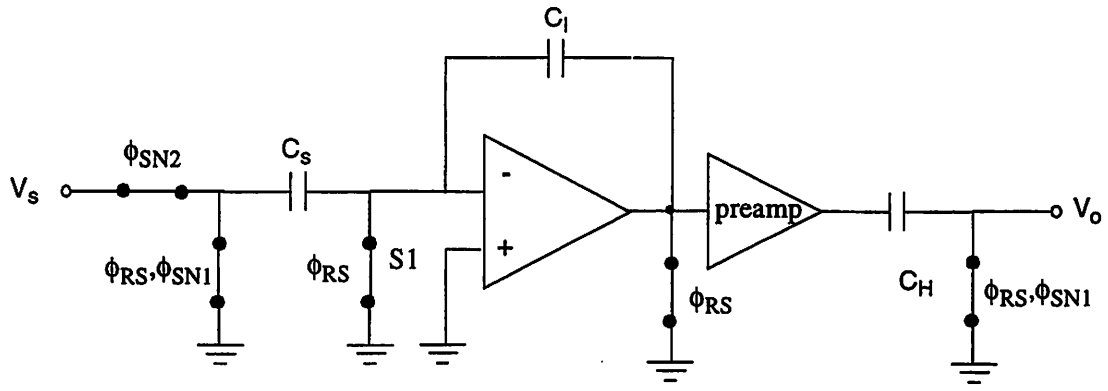


Fig. 4.4: A capacitance-sensing front-end circuit in which the errors from both the charge integrator and the preamplifier are attenuated by correlated double sampling.

Mapping from the z-domain into the frequency domain by substituting $z = e^{j\omega T}$ and then calculating the magnitude of the noise shaping function yield

$$\left|H_{CDS}(e^{j\omega T})\right|^2 = 4\sin^2\left(\frac{\omega T}{8}\right) \qquad \text{(Eq 4-6)}$$

This shaping function shows that correlated double sampling suppresses noise at around DC, $4f_s$, $8f_s$,..., where $f_s=1/T$ is the clock frequency. Since 1/f noise has a spectral density inversely proportional to the frequency while the noise shaping function of correlated double sampling is proportional to the frequency square, the 1/f noise is largely eliminated when the 1/f noise corner frequency is smaller than the sampling frequency. One drawback of applying correlated double sampling, however, is the increase in amplifier thermal noise because of the double sampling and the higher amplifier bandwidth due to the shorter available settling time.

In micromachined applications, a preamplifier is usually added after the front-end sensing circuit, or the charge integrator, because the output signal of the charge integrator is very small, often in the range of microvolts. Due to the small input signal, the preamplifier also needs correlated double sampling to attenuate its errors. Fig. 4.4 shows an implementation in which correlated double sampling is performed at

the preamplifier output, thus attenuating the error of both the charge integrator and the preamplifier.

It should be noted that the circuits in Fig. 4.3 and Fig. 4.4 can only drive a small capacitive load. To drive a large load or a non-capacitive load, a buffer is needed. Additionally, the load capacitance of these circuits must be voltage independent to avoid modulating the capacitive voltage dividing ratio and thus creating a distortion.

4.4 Optimization of Amplifier Thermal Noise

In the last section, we have discussed the use of correlated double sampling technique to attenuate the amplifier offset and 1/f noise, the switch charge injection, and the kT/C noise. With all these errors attenuated, the amplifier thermal noise becomes the fundamental resolution limiting factor and needs to be optimized.

The optimization of the amplifier thermal noise is based on the following assumptions:

- Switches in the signal path contribute negligible amount of noise. Typically, the bandwidths of the switches are chosen to be several times higher than that of the amplifier to avoid adding additional poles. This results in a noise contribution of the switches that is much smaller than that of the amplifier.

- The amplifier is a single-stage type. Single-stage amplifiers are typically used in switched-capacitor circuits because of their high speed and simplicity.

- Sense capacitance C_S and the parasitic capacitance C_P are considered fixed variables since they are primarily determined by the fabrication process of the sense element.

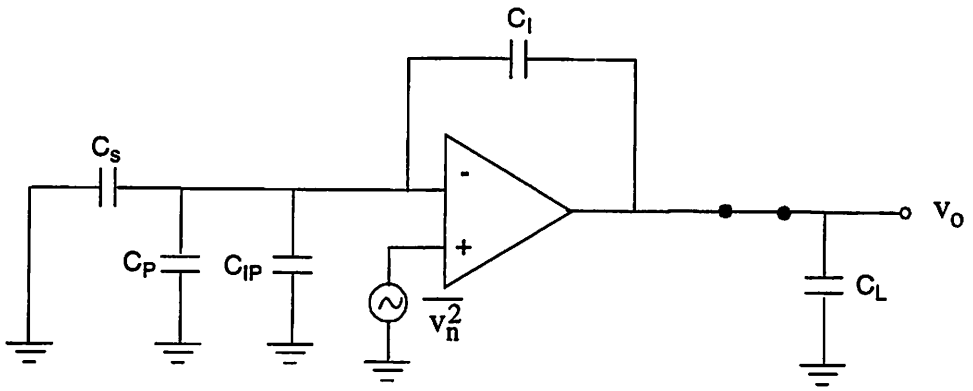


Fig. 4.5: A switched-capacitor sensing circuit during the sensing phase with the amplifier noise shown at the amplifier input node.

- The amplifier closed-loop bandwidth is determined by the sampling frequency and the settling requirement. Any excess bandwidth is avoided because it produces unnecessary noise folding.

- In this noise optimization process, the integrating capacitor is initially chosen to be an arbitrary but reasonable value. After the optimization is completed, the integrating capacitance is modified, if necessary. Afterwards, the noise optimization can be reiterated.

Fig. 4.5 shows a charge integrator during the sensing phase. The input-referred thermal noise of the amplifier can be written as

$$\overline{v_n^2} = \frac{8kT}{3g_m} \cdot n_f \cdot \Delta f \qquad \text{(Eq 4-7)}$$

where $8kT/3g_m$ is the thermal noise of the input transistor and n_f is the ratio of the total amplifier noise to the input transistor noise. In a properly designed amplifier, the input devices are the main noise contributors; hence, n_f is approximately two due to the input source-coupled pair.

The output-referred noise spectral density of this charge integrator is

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \left(\frac{C_S + C_I + C_P + C_{IP}}{C_I}\right)^2 \cdot \frac{\overline{v_n^2}}{\Delta f} \qquad \text{(Eq 4-8)}$$

where C_{IP} is the input capacitance of the amplifier. With C_S, C_I, and C_P fixed as stated in the assumptions, the charge integrator output noise becomes a function of only the amplifier input capacitance and the input-referred thermal noise of the amplifier, $\overline{v_n^2}$. The thermal noise, according to Eq. 4-7, can be reduced by increasing the transconductance of the input devices. Increasing the transconductance, however, requires increasing either the saturation voltage of the input devices, which in practice is limited by the supply voltage and the output swing, or enlarging the input devices [24]. Larger input devices increase the amplifier input capacitance which results in the reduction in the feedback factor. Smaller feedback factor means high noise gain from the amplifier input to the output. For amplifiers with small input devices, the increase in transconductance dominates and the output-referred noise is decreased. For amplifiers with large input devices, the reduction in feedback factor dominates and output-referred noise is increased.

The optimal size for the input devices can be calculated by going through the following steps. For a MOS transistor in the saturation region, the transconductance of the device can be related to the cutoff frequency f_T, the frequency where the magnitude of the common-source current gain falls to unity, as

$$g_m = 2\pi f_T C_{GS} \qquad \text{(Eq 4-9)}$$

where C_{GS} is the gate capacitance of the device and is equal to the amplifier input capacitance C_{IP}. Substituting Eq. 4-9 into Eq. 4-7 and Eq. 4-7 into Eq. 4-8 yields

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \frac{(C_S + C_I + C_P + C_{IP})^2}{C_{IP} C_I^2} \cdot \frac{4kTn_f}{3\pi f_T}. \qquad \text{(Eq 4-10)}$$

To find the optimal amplifier size, Eq. 4-10 is differentiated with respect to C_{IP}

$$\frac{\overline{dv_{ns}^2}}{dC_{IP}} = 0 \quad \rightarrow \quad C_{IP,\,opt} = C_S + C_I + C_P. \qquad \text{(Eq 4-11)}$$

This result states that, for a given saturation voltage, the amplifier input devices should have a gate capacitance equal to the summation of all other capacitances at the summing node.

Substituting the optimal input device size and the amplifier noise into the capacitance sensing resolution given in Eq. 3-11,

$$\frac{\Delta C_{min,\,opt}}{\sqrt{\Delta f}} = \frac{1}{V_s}\cdot\sqrt{\frac{16kTn_f(C_S + C_I + C_P)f_u}{3f_s f_T}}. \qquad \text{(Eq 4-12)}$$

In switched-capacitor circuits, the amplifier closed-loop bandwidth, f_u, is related to the sampling frequency, the settling accuracy, and the duty cycle as

$$f_u = \frac{1}{2\pi\tau} = \frac{1}{2\pi}\cdot\left(\frac{m}{n_\tau f_s}\right)^{-1} \qquad \text{(Eq 4-13)}$$

where τ is the amplifier time constant, n_τ is the number of settling time constant, and m is the duty cycle of each sensing phase.

Substituting Eq. 4-13 into Eq. 4-12 provides the final result

$$\frac{\Delta C_{min,\,opt}}{\sqrt{\Delta f}} = \frac{1}{V_s}\cdot\sqrt{\frac{8kTn_f n_\tau(C_S + C_I + C_P)}{3\pi m f_T}}. \qquad \text{(Eq 4-14)}$$

This result suggests that small parasitic capacitance C_P, small integrating capacitor C_I, and short channel devices with high f_T improve the optimal capacitance resolution of the sensing circuit. Even though this equation implies that small sense capacitance C_S improves the capacitance resolution, it actually reduces the position resolution due to smaller dC_S/dx.

After the size and transconductance of the amplifier input devices is determined, the next step is to determine a proper load capacitance C_L to achieve the required amplifier bandwidth. The required load capacitance can be calculated from Eq. A1-5 of Appendix 1 as

$$C_L = \frac{C_I}{(C_S + C_I + C_P + C_{IP})}\left(\frac{g_m}{2\pi f_u} - (C_S + C_P + C_{IP})\right). \qquad \text{(Eq 4-15)}$$

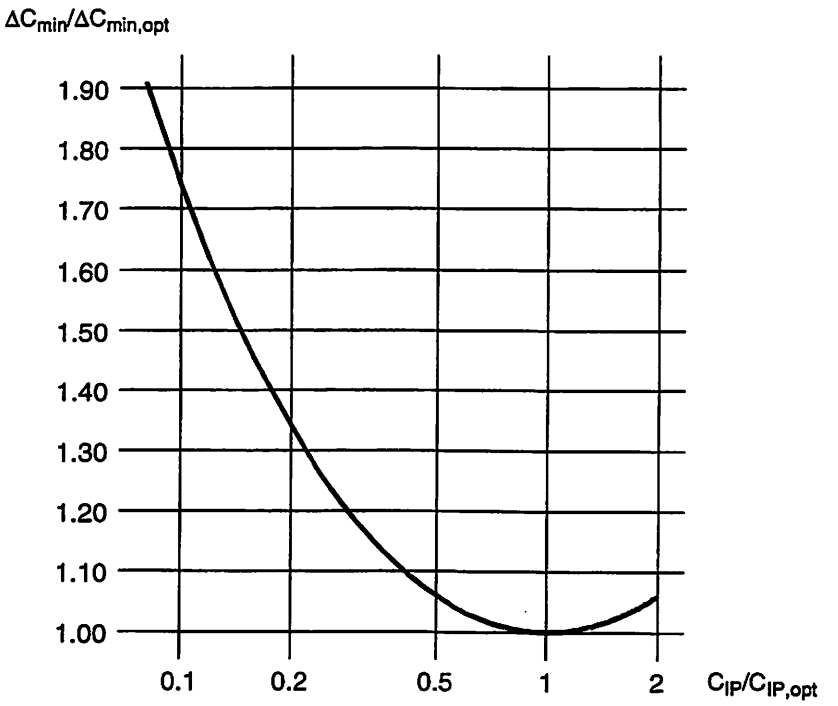


Fig. 4.6: This plot shows the capacitance sensing resolution as a function of the size of the amplifier input devices. The curve is very shallow in both directions from the optimal point, increasing rapidly only for very small $C_{IP}/C_{IP,opt}$

Substituting g_m from Eq. 4-9, f_u from Eq. 4-13, and the optimal input capacitance from Eq. 4-11 yields

$$C_{L,\,opt} \approx \frac{\pi m C_I f_T}{n_\tau f_s}. \qquad \text{(Eq 4-16)}$$

If the actual load capacitance is larger than this value, the noise optimization can be reiterated with a larger integrating capacitor or a larger-than-optimal amplifier should be used. As shown in the plot in Fig. 4.6, the use of a larger-than-optimal amplifier results in a very small increase in capacitance resolution. If the actual load capacitance is smaller than the value given in Eq. 4-16, the noise optimization should be reiterated with a smaller integrating capacitor. As a matter of fact, small integrating capacitors are preferred because, according to Eq. 3-3 and Eq. 4-14, the capacitance-to-voltage gain increases and the capacitance sensing resolution decreases with smaller integrating capacitor.

To demonstrate the noise and the resolution improvement due to correlated double sampling, an example is given in Table 4.2. In this example, kT/C noise cancellation combined with the amplifier noise optimization improves the capacitance resolution by more than a factor of six. Unfortunately, noise optimization often results in very large input devices with very high bias currents. To alleviate this problem, a smaller-than-optimal input devices can be used. Fig. 4.6 shows that the sensing resolution is fairly insensitive to C_{IP}, for C_{IP} larger than ten percent of $C_{IP,opt}$. For C_{IP} as small as ten percent of $C_{IP,opt}$, the sensing resolution increases from the optimal value by only a factor of 1.7. Applying the 'one-tenth rule' to the example in Table 4.2 results in a factor-of-ten reduction in the size and bias current of the input devices.

In conclusion, the amplifier noise can be minimized at the expense of size and power consumption of the amplifier. As the amplifier input device is made larger (higher transconductance), the input-referred noise decreases, while the noise gain to the output increases due to the lower feedback factor. The optimal amplifier has an input capacitance C_{IP} equal to $C_S+C_I+C_P$. The optimal amplifier, unfortunately, is often too large and consumes too much power. A suboptimal amplifier with C_{IP} as small as ten percents of $C_{IP,opt}$ offers a more reasonable size and power consumption with a noise penalty of less than a factor of two.

Ultimately, it should be reminded that this noise optimization technique is also applicable to synchronous detection circuits.

4.5 Noise Improvement Due to kT/C Noise Cancellation

In this section, we will examine the noise improvement due to the kT/C noise cancellation of correlated double sampling (CDS). In the derivation of the noise improvement factor, we will assume that kT/C noise, which typically dominates, is the only thermal noise source for a circuit without CDS. For a circuit with CDS, the

Table 4.2: An example to illustrate the noise improvement and input device sizing due to correlated double sampling.

Parameters	Values
C_S	1pF
C_I	0.1pF
C_P	5pF
f_T	2GHz
f_s	1MHz
n_f	2
n_τ	8
m	0.25
V_S	1
$C_{IP,opt}$	6.1pF
$C_{L,opt}$	9.8pF
ΔC_{min}	$2.62 \cdot 10^{-20} fF/\sqrt{Hz}$
ΔC_{min} (without CDS)	$1.71 \cdot 10^{-19} fF/\sqrt{Hz}$
Input device bias current*	~30mA
Using $C_{IP}=0.1C_{IP,opt}$ and $C_I=0.2pF$	
$C_{IP,opt}$	0.62pF
$C_{L,opt}$	4pF
ΔC_{min}	$4.86 \cdot 10^{-20} fF/\sqrt{Hz}$
Input device bias current*	~3mA

* The bias current is calculated using typical parameters and bias conditions for devices with 1μm channel length.

amplifier thermal noise is assumed to be optimized as discussed in the last section, and approximately doubled due to the double sampling of an uncorrelated white noise.

The noise improvement factor, which is essentially the resolution improvement, is defined as

$$\text{Noise improvement} = \sqrt{\frac{2v_{kT/C}^2}{v_{opamp}^2}} = \frac{\sqrt{2} \cdot \Delta C_{min,\,kT/C}}{\Delta C_{min,\,opamp}} \qquad \text{(Eq 4-17)}$$

where the square root of two in the kT/C noise term is due to the differential signal paths. Substituting ΔC_{min} due to the kT/C noise from Eq. 3-10 and ΔC_{min} due to the amplifier thermal noise from Eq. 4-14 yields

$$\text{Noise improvement} \approx \sqrt{\frac{3\pi m f_T}{2 n_f n_\tau f_s}} \propto \sqrt{\frac{f_T}{f_s}}. \qquad \text{(Eq 4-18)}$$

If a suboptimal amplifier according to the previously discussed 'one-tenth rule' is applied, the noise improvement is reduced by a factor of 1.7; therefore,

$$\text{Noise improvement (suboptimal)} \approx \sqrt{\frac{\pi m f_T}{2 n_f n_\tau f_s}}. \qquad \text{(Eq 4-19)}$$

For a typical circuit where m=25%, n_f=2, n_τ=8, and f_T/f_s=1000, correlated double sampling, according to Eq. 4-18 and Eq. 4-19, improves the sensing resolution by 8.5 and 4.9 times, respectively.

Three conclusions can be drawn from Eq. 4-18 and Eq. 4-19. First, the noise improvement is not a function of the sense capacitance. This implies that, as long as the amplifier input devices is properly sized according to Eq. 4-11, correlated double sampling improves noise regardless of the sense capacitance values. This is because the kT/C noise and the optimized amplifier thermal noise are approximately the same functions of C_S. Second, the noise improvement factor is a function of f_T/f_s. Intuitively, this is because kT/C noise is inversely proportional to the sampling frequency, while the optimized amplifier noise is inversely proportional to the cutoff frequency f_T of the devices. To achieve a meaningful improvement, the device cutoff frequency f_T should be at least 50 times higher than the sampling frequency f_s. For lower ratio of f_T to f_s, the improvement, according to equation Eq. 4-18, becomes too small to justify the added complexities. Third, correlated double sampling is an attractive alternative to reducing the kT/C noise by increasing the sampling frequency. This is because, in order to match the factor-of-8.5 improvement of CDS as shown in the above example, the sampling frequency must be increased by a factor of 70. Such a large increase in

Table 4.3: The effects of parameters in the position sensing interface on the position sensing resolution.

Parameters	Change in parameters	Reduction in Δx_{min}
C_S	2x	$\sqrt{2}$ - 2x
C_P	0.5x	$<\sqrt{2}$x
f_T	2x	$\sqrt{2}$x
V_s	2x	2x
x_o	0.5x	2x
dC/dx	2x	$\sqrt{2}$ - 2x

sampling frequency significantly increases the power consumption and the difficulty in circuit design.

4.6 Maximizing Position Sensing Resolution

In this section, we will use the result of the amplifier thermal noise optimization to calculate the ultimate position sensing resolution for given technologies. The obtained result provides us with a guideline to utilize or develop technologies that will bring about higher sensing resolution. Besides, this result can be used as a benchmark to compare the achievable resolution to the fundamental limit.

The relationship between the displacement and the capacitance variation of a sense element, according to Eq. 3-6, is

$$\Delta x = \frac{\Delta C}{dC/dx} \qquad \text{(Eq 4-20)}$$

Substituting this relationship into Eq. 4-14 yields

$$\Delta x_{min,\,opt} = \sqrt{(C_S + C_I + C_P) \cdot \frac{4kTn_f n_\tau}{3\pi m f_T}} \cdot \frac{x_o}{C_S \cdot V_s} \qquad \text{(Eq 4-21)}$$

Substituting the parameters from Table 4.2 and assuming a transverse comb structure with a nominal gap x_0 of 2μm, the position sensing resolution is $9.72 \cdot 10^{-14}\text{m}/\sqrt{\text{Hz}}$. Furthermore, the effects of parameters in Eq. 4-21 on the position sensing resolution are summarized in Table 4.3.

4.7 Summary

This chapter proposes that correlated double sampling (CDS), which has traditionally been used to remove the amplifier offset and attenuate the 1/f noise, can be extended to cancel the switch charge injection and kT/C noise due to switching operations. With the kT/C noise removed, the amplifier thermal noise becomes the dominant noise source and needs to be optimized. This is achieved by selecting the input devices so that the amplifier input capacitance is equal to the sum of all other capacitances at the summing nodes. With the amplifier noise optimized, analytical results show that the kT/C noise cancellation reduces the thermal noise of the sensing circuit by as much as 20dB. The expense of the noise optimization, however, is typically an increase in power consumption of the amplifier. Finally, analytical results show that large and tall sense elements with small gaps, small parasitic capacitance, short channel-length devices, and large sensing voltage improve the position resolution.

Chapter 5

Integration of Position Sensing and High-Voltage Driving Circuits

5.1 Introduction

Integration of the position sensing with the driving circuits is the most challenging task in designing position sensing circuits for electrostatic micropositioners. The issue is exacerbated when the driving and the sensing operations share a single set of micropositioner electrodes because the two signals, which are several orders of magnitude difference in amplitude, are superimposed. This ultimately results in the position sensing resolution being limited by nonidealities associated with the integration of the two circuits rather than the fundamental limits imposed by the thermal noise of the sensing electronics.

This chapter explores the interface between the two circuits and discuss techniques that prevent undesired couplings between the two signals. Section 5.2 discusses the leakage of the sensing charge into the output of the driving circuit. Section 5.3 investigates feedthrough, or the spurious coupling of the driving signal into the sensing signal. Section 5.4 examines the variation in the position sensing transfer function as a result of the voltage-dependent capacitance at the rotor node. On the contrary to Sections 5.3 and 5.4 which deal with the coupling of the driving signal into

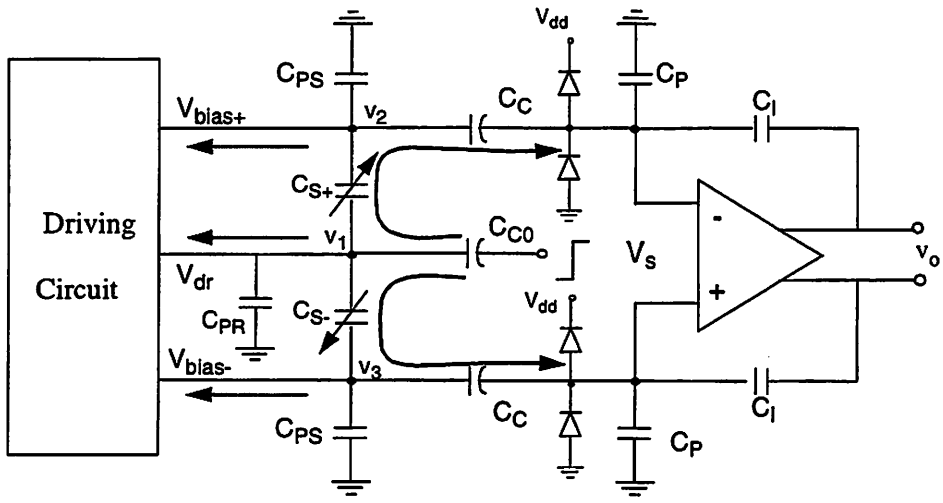


Fig. 5.1: The interface between the micropositioner, the driving circuit, and the sensing circuit. The arrows illustrate the flow of the sensing charge. If the driving circuit has low output impedance, the sensing charge can leak into the driving circuit.

the sensing signal, Section 5.5 discusses the position error due to superimposing the sensing signal on the driving signal. Finally, Section 5.6 analyzes offsets and gain variations in the sensing circuits caused by variations and mismatches of coupling capacitors and parasitics at the electrodes of the micropositioners.

5.2 Sensing Charge Leakage

When the sensing and the driving circuits share a single set of electrodes, the sensing charge could leak into the low-impedance outputs of the driving circuit, as illustrated in Fig. 5.1. For example, if the driving circuit utilizes ideal voltage sources to drive the micropositioner, all the sensing charge will flow into the driving circuit. To minimize the sensing charge leakage, the impedance looking into the output of the driving circuit must be high. This can be achieved by adding resistors or switches at the output of the driving circuit.

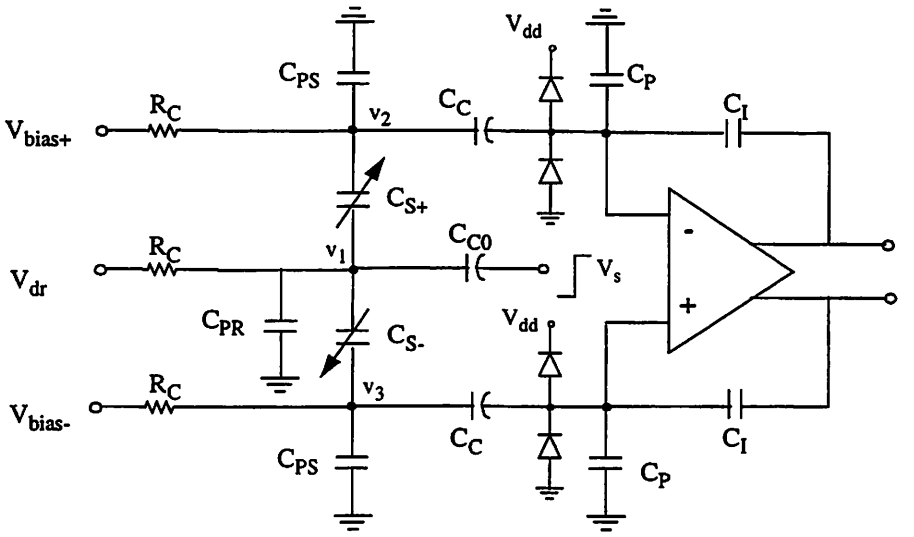


Fig. 5.2: Coupling resistors are added between the output of the driving circuit and the micropositioner to block the sensing charge from leaking into the driving circuit.

5.2.1 Coupling Resistors

As shown in Fig. 5.2, the coupling resistors R_C are connected at the output of the driving circuit to increase the output impedance of the driving circuit, thus reducing the leakage of the sensing charge into the driving circuit. The coupling resistors form a low-pass filter for the driving signal and a high-pass filter for the sensing signal. Assuming that the output impedance of the driving circuit is small, the corner frequencies of the two filters can be approximated as

$$f_{LPF} \approx \frac{1}{2\pi} \cdot \frac{1}{R_C(C_{C0} + 2C_S + C_{PR})} \qquad \text{(Eq 5-1)}$$

and

$$f_{HPF} \approx \frac{1}{2\pi} \cdot \frac{(C_{C0} + 2C_S + C_{PR})}{R_C C_{C0}(2C_S + C_{PR})}, \qquad \text{(Eq 5-2)}$$

respectively. To ensure that the driving signal is not attenuated by the low-pass filter,

$$f_{LPF} > f_{dr,\,max} \qquad \text{(Eq 5-3)}$$

where $f_{dr,max}$ is the driving bandwidth. To minimize the sensing charge leakage, the sensing frequency must be several times higher than the high-pass corner frequency,

$$f_{HPF} \ll f_s . \qquad \text{(Eq 5-4)}$$

According to Eq. 5-1 and Eq. 5-2, the ratio between the two corner frequencies is

$$\frac{f_{HPF}}{f_{LPF}} \approx \frac{(C_{C0} + 2C_S + C_{PR})^2}{C_{C0}(2C_S + C_{PR})} . \qquad \text{(Eq 5-5)}$$

Combining this result with Eq. 5-3 and Eq. 5-4 yields

$$\frac{f_s}{f_{dr,\,max}} \gg \frac{(C_{C0} + 2C_S + C_{PR})^2}{C_{C0}(2C_S + C_{PR})} . \qquad \text{(Eq 5-6)}$$

As an example, for C_{C0}=3.5pF, C_S=1pF, C_{PR}=10pF, and a driving bandwidth of 2kHz, the coupling resistors R_C, according to Eq. 5-1 and Eq. 5-3, must be at least 0.8 megaohms and the ratio between the sensing frequency and the driving bandwidth, according to Eq. 5-6, must be much larger than 5.7 times.

In monolithic implementations, the maximum values of the coupling resistors can be limited by the die area and the associated parasitics. A possible improvement is to replace the coupling resistor with a resistive T-network as shown in Fig. 5.3. Because of the additional degrees of freedom, the T-network offers more flexibility in choosing the low-pass and the high-pass corner frequencies and potentially allows the use of smaller resistors.

5.2.2 Coupling Switches

In switched-capacitor sensing circuits, the coupling resistors can be replaced by switches. The switches serve two purposes. First, they decouple the driving and the sensing circuits during the sensing period. Second, they create a time-division system in which the driving and the sensing operations are separated in time. As illustrated in Fig. 5.4, while the sensing circuit is reset, the driving switches are closed and the driving voltage of the micropositioner is updated. During the sensing period, the

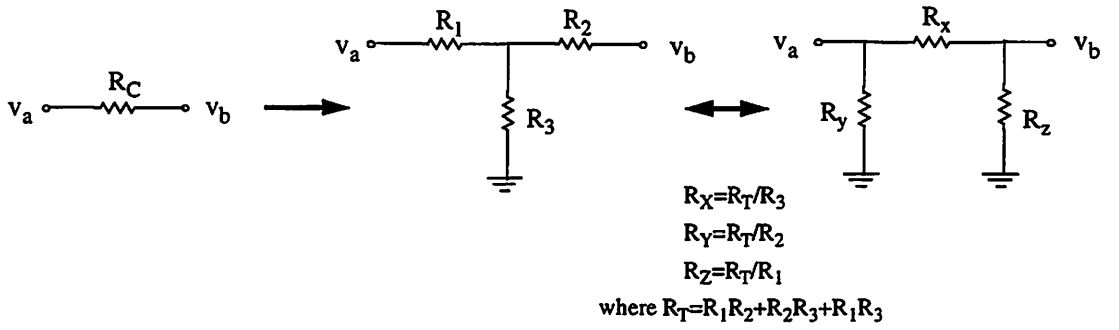


Fig. 5.3: The coupling resistor R_C can be replaced by a resistor T-network. The equivalent π-network of the T-network is shown on the right side.

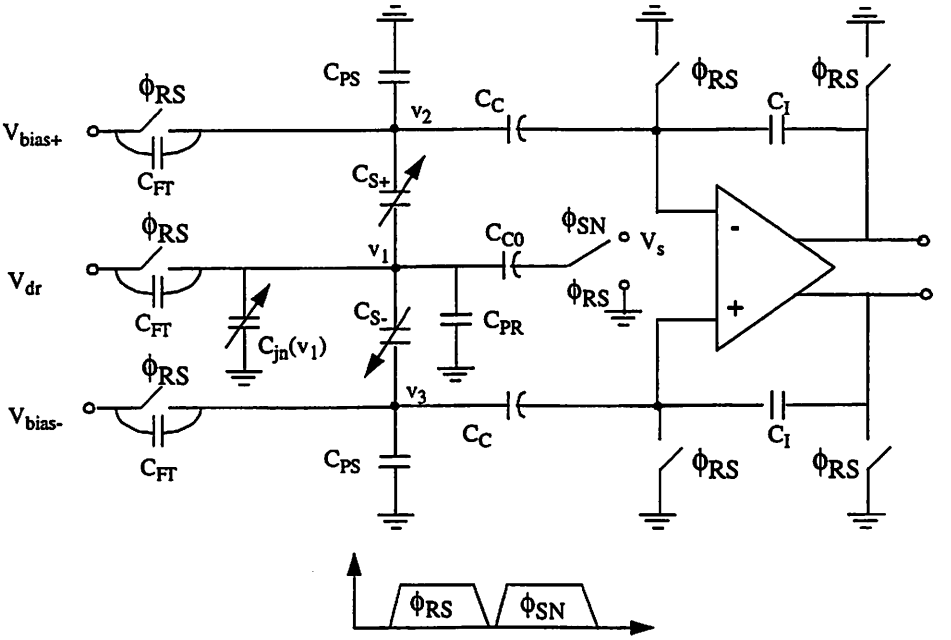


Fig. 5.4: Coupling resistors are replaced by the switches, which decouple the driving circuit from the sensing circuit during the sensing period.

driving switches are opened and the two circuits are decoupled. For ideal switches, the feedthrough capacitance, or C_{FT}, are equal to zero; therefore, the driving and the sensing circuits are entirely separated. In practice, the feedthrough capacitance results in the coupling of the driving signal into the sensing signal, as will be discussed in Section 5.3.

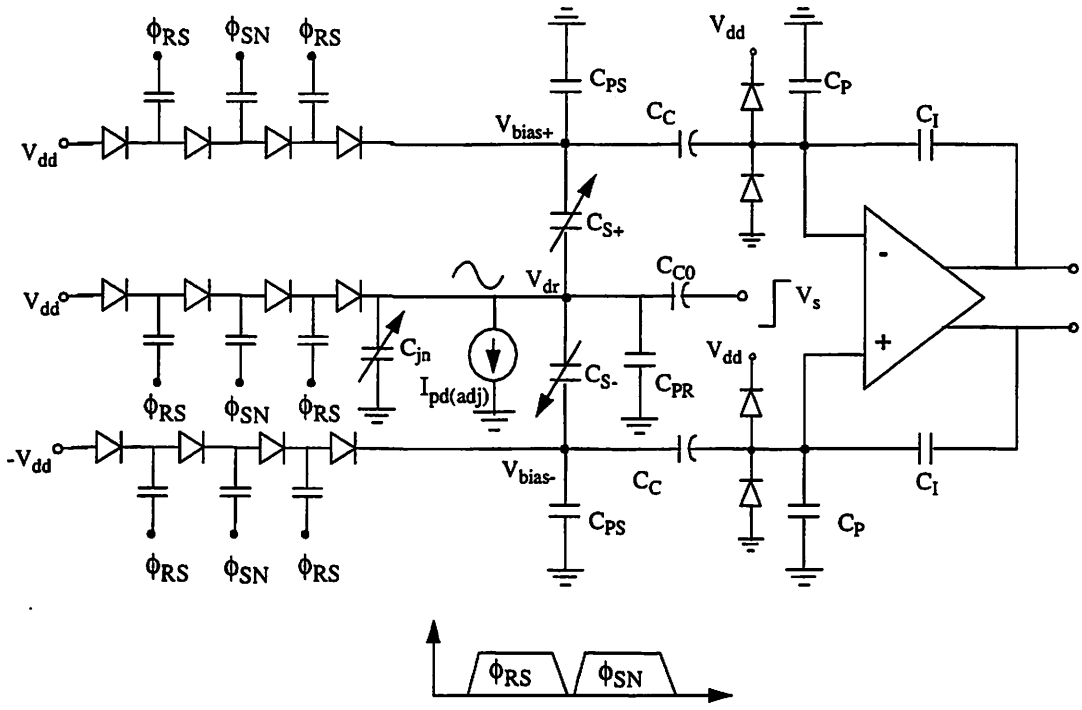


Fig. 5.5: Charge pumps generate the driving voltages for the micropositioner and also function as switches to decouple the driving and the sensing circuits during the sensing phase.

The advantages of the switches are the first-order isolation between the sensing and the driving circuits and the much smaller die area compared to the coupling resistors. Unfortunately, generating the control signals for the switches can be complicated because of the high voltages involved. This problem is exacerbated in the rotor switch because the driving voltage V_{dr} can vary rail-to-rail, or from V_{bias+} to V_{bias-}. Furthermore, the driving voltage can modulate the junction capacitance of the rotor switch, or C_{jn} in Fig. 5.4. This, in turns, changes the capacitance-to-voltage gain of the sensing circuit. This issue is further discussed in Section 5.4.

To avoid the difficulty in generating the high-voltage control signals for the switches, charge pumps [25], [26] should be used to implement the driving circuit because their output stages function similarly to switches. A charge pump—a proposed technique to generate high voltages for the micropositioner from a low-voltage supply— consists of cascaded stages of diodes and capacitors driven by two

out-of-phase clock signals. In the example in Fig. 5.5, the micropositioner is driven by three three-stage charge pumps. The output of the charge pump at the rotor is regulated by an adjustable current source I_{pd} in order to generate the time-varying driving voltage V_{dr} for the rotor. The pull-down current source I_{pd} is needed because a charge pump can only pump charges in the direction of increasing the output voltage.

Examining the operation of the charge pump reveals that when the one of the clock phases becomes low, the following diodes are reverse biased and functions as an open switches. Hence, by driving the charge pump with the same clock as the sensing circuit as shown in Fig. 5.5, the last diodes of the charge pumps can be used to isolate the driving and the sensing circuit similarly to the switches in Fig. 5.4. In addition to turning off the diode, the pull-down current source must be turned off and have a high output impedance while the sensing operation is being performed. Furthermore, the pull-down current source must be bootstrapped to ensure that any associated junction capacitance is biased by a constant voltage (See an example in Fig. 5.10).

5.3 Feedthrough

Feedthrough, as conceptually shown in Fig. 5.6, is the spurious coupling of the driving signal into the sensing signal. Since the driving voltage is typically several orders of magnitude larger than the position signal, feedthrough is an important issue and often is the factor limiting the resolution of the sensing circuit. Additionally, feedthrough can degrade the stability of a closed-loop system. Feedthrough with the same polarity as the position signal adds a pair of complex conjugated zeros which draw the closed-loop poles closer to the imaginary axis. Feedthrough with the opposite polarity to the position signal adds a pair of real zeros, one in the left-half plane and one in the right-half plane, which can cause the system to become unstable. Typically, the allowable feedthrough is determined by the position resolution requirement. Hence, this criteria will be used in the following discussion.

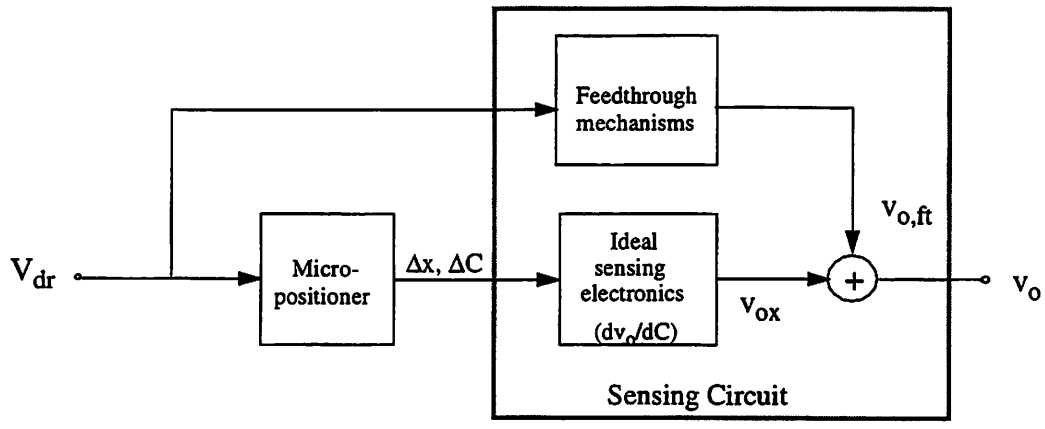


Fig. 5.6: A conceptual diagram of the micropositioner and the position sensing circuit. Feedthrough is modeled as the transfer function H_{FT}.

For a sampled-data system such as a switched-capacitor sensing circuit, feedthrough is usually a function of the variation in the driving voltage during the sensing period; therefore, the feedthrough transfer function is shaped by the differentiation function $1 - z^{-m}$ and can be written as

$$\frac{V_{o,ft}(z)}{V_{dr}(z)} = (1 - z^{-m}) \cdot H_{FT}(z) \qquad \text{(Eq 5-7)}$$

where $V_{o,ft}$ is the feedthrough component in the output voltage as shown in Fig. 5.6, H_{FT} is the feedthrough transfer function, and m is the ratio of the sensing period to the total clock period. Mapping from the z-domain into the frequency domain and assuming that the driving frequency is much smaller than the sensing frequency yields

$$\frac{V_{o,ft}(f)}{V_{dr}(f)} \approx \left(\frac{2\pi f_{dr} m}{f_s}\right) \cdot H_{FT}(f) \quad . \qquad \text{(Eq 5-8)}$$

To ensure that feedthrough does not degrade the position sensing accuracy,

$$v_{o,ft(max)} < v_{o(min)} \cdot \qquad \text{(Eq 5-9)}$$

Substituting Eq. 5-8 into Eq. 5-9 and rearranging the terms yield

$$H_{FT} \cdot \frac{f_{dr}}{f_s} < \frac{(v_{o(min)})}{2\pi m \cdot V_{dr,max}} \qquad \text{(Eq 5-10)}$$

$$= \frac{\left(\Delta x_{min} \cdot \frac{dC}{dx} \cdot \frac{dv_o}{dC}\right)}{2\pi m \cdot V_{dr,\,max}}. \qquad \text{(Eq 5-11)}$$

The obtained result will be used in Section 5.3.2, where the means to reduce feedthrough will be discussed.

5.3.1 Sources of Feedthrough

In this section, we will discuss sources of feedthrough and divide them into two categories according to their mechanisms.

5.3.1.1 Direct Feedthrough

Direct feedthrough is defined as the coupling of the driving signal V_{dr} into the sensing signal at the rotor node and usually is the main contributor of feedthrough. For the circuits in Fig. 5.2 and Fig. 5.3, the transfer function of direct feedthrough is calculated from Eq. 3-17 and Eq. 3-18 as

$$H_{FT} = \gamma_{FT} \cdot \left(\frac{C_C}{C_C + C_{PS} + C_S}\right) \cdot \frac{\Delta C_S}{C_I} . \qquad \text{(Eq 5-12)}$$

For circuits using coupling resistors as in Fig. 5.2, γ_{FT} is equal to one. For circuits using coupling switches as in Fig. 5.3, γ_{FT} or the switch feedthrough is ideally zero. In practice, the feedthrough of the coupling switches, or γ_{FT}, can be as high as -40dB due to the feedthrough capacitors, or C_{FT} as shown in Fig. 5.3 [27].

Eq. 5-12 also suggests that direct feedthrough is proportional to the mismatch in the sense capacitance, or ΔC_S. Intuitively, this is because if the differential signal paths are matched, feedthrough will appear equally on both signal paths and become a common-mode signal. Hence, the worst-case transfer function is

$$H_{FT(max)} = \gamma_{FT} \cdot \left(\frac{C_C}{C_C + C_{PS} + C_S}\right) \cdot \frac{\Delta C_{S(max)}}{C_I} , \qquad \text{(Eq 5-13)}$$

$$= \gamma_{FT} \cdot \left(\frac{C_C}{C_C + C_{PS} + C_S} \right) \cdot \frac{\Delta x_{max} \cdot \frac{dC}{dx}}{C_I} \quad . \qquad \text{(Eq 5-14)}$$

For typical parameters—Δx_{max}=2μm, dC/dx=50fF/μm, C_C=3.5pF, C_{PS}=7pF, C_S=C_I=1pF,

$$H_{FT(max)} = 0.03 \cdot \gamma_{FT} \quad . \qquad \text{(Eq 5-15)}$$

5.3.1.2 Indirect Feedthrough

Indirect feedthrough is defined as the feedthrough which is caused by parasitics and nonidealities such as coupling through power supply and ground networks, coupling between bond wires, and substrate coupling. Because of its nature, deriving the transfer function of indirect feedthrough is complicated and the result is highly dependent on the circuit implementation. With precautions such as fully-differential sensing electronics and symmetrical circuit layout, indirect feedthrough is expected to be smaller than direct feedthrough.

5.3.2 Minimizing Feedthrough

In this section, we will assume that the feedthrough transfer function, or H_{FT}, is given and will investigate techniques that minimize the effects of feedthrough. Table 5.1 summarizes these techniques.

Increasing the position sensing gain, or $\frac{dv_o}{dC}$., makes the feedthrough appear relatively smaller. However, the increase in the position sensing gain must not be offseted by the increase in the feedthrough transfer function. For direct feedthrough, this can be achieved by increasing the coupling capacitor C_{C0} and the sensing voltage V_S and minimizing the parasitic capacitances C_{PR} and C_{PS}.

In theory, an effective approach to eliminate feedthrough is to characterize the feedthrough transfer function and perform a subtraction to remove the feedthrough

Table 5.1: A summary of techniques to reduce feedthrough

Techniques	Description/comments
Maximizing position sensing gain	Limited by the size of coupling capacitors,parasitics,etc. Can increase feedthrough, if not done properly.
Cancellation	Rely on tight control over fabrication tolerances.
Frequency separation	Require very high sensing frequency. Interference with the read channel of disk drives.
Correlated triple sampling (CTS)	Add an additional order of feedthrough shaping function, thus requiring smaller sensing frequency.
Chopper stabilization	Modulate feedthrough to outside the signal band. Need to combine with correlated double sampling to remove kT/C noise.

component from the sensing signal. In practice, this technique relies extremely on tight control over fabrication tolerances. This problem is exacerbated if the micropositioner, the high-voltage driving circuit, and the sensing circuit are not integrated monolithically because the values of external parasitics are not well-controlled. Furthermore, drift or long-term stability reduces the effectiveness of this method.

The frequency separation approach reduces the feedthrough by minimizing the variation in the driving voltage during the sensing period. This approach, however, requires a very high sensing frequency. To decrease the sensing frequency requirement, correlated triple sampling can be utilized to achieve a second-order feedthrough shaping. Chopper stabilization, however, is potentially the most effective method to minimize feedthrough because feedthrough is modulated to outside the signal band, thus allowing it to be removed by a low-pass filter.

In the following subsections, the frequency separation, correlated triple sampling, and chopper stabilization techniques will be discussed in details.

5.3.2.1 Frequency Separation

As discussed earlier, feedthrough is normally a function of the variation in the driving voltage during the sensing period; hence, it can be reduced by choosing the sensing frequency to be much higher than the driving frequency. The minimum ratio between the sensing frequency and the driving frequency which reduces feedthrough to below position resolution is calculated from Eq. 5-11 as

$$\frac{f_s}{f_{dr}} > H_{FT} \cdot \frac{2\pi m \cdot V_{dr,\,max}}{\Delta x_{min} \cdot \frac{dC}{dx} \cdot \frac{dv_o}{dC}} \quad . \qquad \text{(Eq 5-16)}$$

As an example, we substitute the transfer function of direct feedthrough (Eq. 5-14) and dv_o/dC (Eq. 3-19) into Eq. 5-16,

$$\frac{f_s}{f_{dr(max)}} > \frac{\gamma_{FT} \cdot (2\pi m A_{dr(max)}) \cdot (C_{C0} + C_{PR} + 2C_S) \cdot SNR}{C_{C0} V_S} \quad . \qquad \text{(Eq 5-17)}$$

For typical parameters—C_S=1pF, C_{C0}=3.5pF, C_{PR}=10pF, SNR=46dB, $A_{dr,max}$=80V, m=0.25, V_S=5V,

$$\frac{f_s}{f_{dr(max)}} > 22000 \cdot \gamma_{FT} \quad . \qquad \text{(Eq 5-18)}$$

For circuits using coupling resistors, γ_{FT} is equal to one and

$$\frac{f_s}{f_{dr(max)}} > 22000 \, . \qquad \text{(Eq 5-19)}$$

For circuits using coupling switches, γ_{FT} can be as high as -40dB [27],

$$\frac{f_s}{f_{dr(max)}} > 220 \, . \qquad \text{(Eq 5-20)}$$

In practice, high sensing frequencies should be avoided because they increase the power consumption and complicate the system design. Furthermore, in magnetic disk drive applications, the sensing frequency should not be higher than one megahertz to avoid interfence with the read channel, which normally extends from a few megahertz up to a few hundred megahertz. According to Eq. 5-19 and Eq. 5-20 and a driving bandwidth of 2kHz, the sensing frequency must be at least 44MHz and 440kHz

for circuits using coupling resistors and coupling switches, respectively. Hence, to avoid the interference, coupling switches and frequency separation must be used in combination. The experimental results from the prototype described in Chapter 6, however, show that feedthrough is still the factor limiting the resolution, despite using coupling switches and a sensing frequency of 1MHz. This is likely due to the slewing and incomplete settling in the rotor driving circuit. Because of this reason, it is necessary to investigate other methods which offer better rejection of feedthrough.

5.3.2.2 Correlated Triple Sampling

The concept of correlated triple sampling (CTS) is to make three measurements instead of two measurements as in correlated double sampling (CDS). Unlike the 1/f noise which is attenuated by the $1-z^{-m}$ shaping function of CDS, feedthrough requires the extra sampling of CTS to attain the same shaping function.

The operations of correlated triple sampling are best explained by examining the output of the sensing circuit shown in Fig. 5.7. This circuit is a generic switched-capacitor sensing circuit which can perform CDS or CTS by employing appropriate output decoder and switching sequence of switch S_1. To simplify the explanations, two approximations will be made: the amplifier settling time is much shorter than each sensing period (ϕ_{SN}) and the bandwidth of driving voltage is much smaller than the sensing frequency. Furthermore, we will define that α is the capacitance sensing transfer function, H_{FT} is the feedthrough transfer function, and ΔV_{dr} is the change in the driving voltage during each sensing period. For the circuit in Fig. 5.7a,

$$\alpha = \left(\frac{C_{C0}}{C_{C0}+C_{PR}+2C_S}\right)\cdot\left(\frac{C_C}{C_C+C_{PS}+C_S}\right)\cdot\frac{\Delta C_S}{C_I}\cdot A_v \qquad \text{(Eq 5-21)}$$

Using these assumptions and definitions, the voltages at the input of the decoder at different time in Fig. 5.7b to Fig. 5.7d can be written as

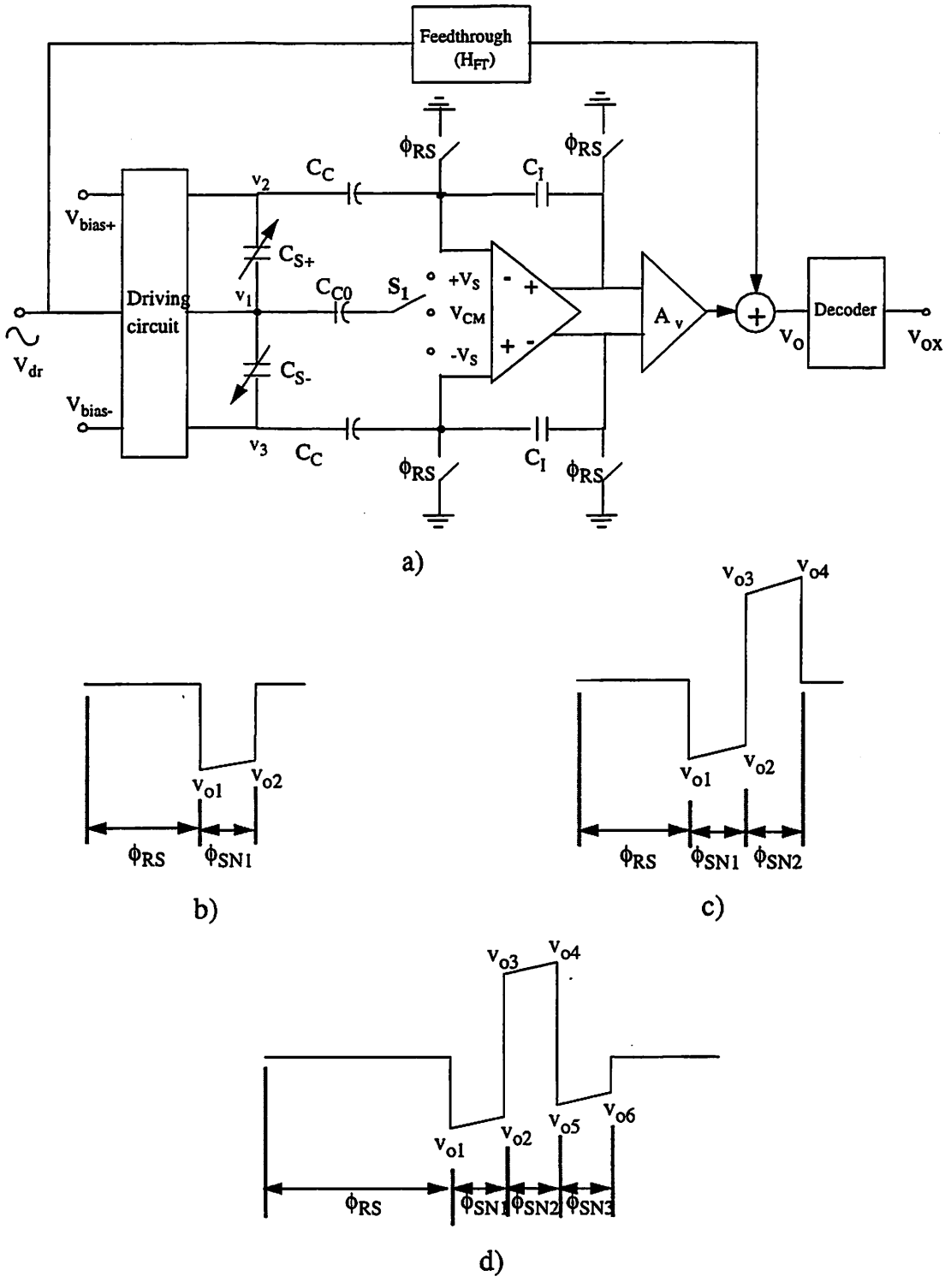


Fig. 5.7: a) A generic switched-capacitor sensing circuit with a decoder at the output to perform CDS or CTS. Feedthrough is modeled as transfer function H_{FT}. b) to d) show outputs v_o of circuits without CDS, with CDS, and with CTS, respectively.

$$v_{o1} = \alpha(-V_S) \quad \text{(Eq 5-22)}$$

$$v_{o2} = \alpha(-V_S) + H_{FT}(\Delta V_{dr1}) \quad \text{(Eq 5-23)}$$

$$v_{o3} = \alpha(V_S) + H_{FT}(\Delta V_{dr1}) \quad \text{(Eq 5-24)}$$

$$v_{o4} = \alpha(V_S) + H_{FT}(\Delta V_{dr1} + \Delta V_{dr2}) \quad \text{(Eq 5-25)}$$

$$v_{o5} = \alpha(-V_S) + H_{FT}(\Delta V_{dr1} + \Delta V_{dr2}) \quad \text{(Eq 5-26)}$$

$$v_{o6} = \alpha(-V_S) + H_{FT}(\Delta V_{dr1} + \Delta V_{dr2} + \Delta V_{dr3}) \quad \text{(Eq 5-27)}$$

Next, we will derive the decoder output v_o of each circuit. For a sensing circuit without correlated sampling (Fig. 5.7b), the decoder output is

$$v_{ox} = v_2 = -\alpha V_S + H_{FT}(\Delta V_{dr1}) . \quad \text{(Eq 5-28)}$$

With correlated double sampling (Fig. 5.7c), the decoder output is

$$v_{ox,CDS} = v_4 - v_2 = 2\alpha V_S + H_{FT}(\Delta V_{dr2}) . \quad \text{(Eq 5-29)}$$

With correlated triple sampling (Fig. 5.7d), the decoder output is

$$v_{ox,CTS} = (v_6 - v_4) - (v_4 - v_2) = -4\alpha V_S + H_{FT}(\Delta V_{dr3} - \Delta V_{dr2}) . \quad \text{(Eq 5-30)}$$

The results from Eq. 5-28 and Eq. 5-29 show that a sensing circuit with correlated double sampling yields the same feedthrough transfer function as a circuit without correlated double sampling. Only correlated triple sampling, as shown in Eq. 5-30, provides further attenuation of feedthrough. The feedthrough transfer function of a circuit with CTS can be calculated from Eq. 5-30 as

$$\frac{V_{o,ft}(z)}{V_{dr}(z)} = (1 - z^{-m})^2 \cdot H_{FT}(z) \quad \text{(Eq 5-31)}$$

and

$$\frac{V_{o,ft}(f)}{V_{dr}(f)} \approx \left(\frac{2\pi f_{dr} m}{f_s}\right)^2 \cdot H_{FT}(f) . \quad \text{(Eq 5-32)}$$

In comparison, the feedthrough transfer function of a circuit without CTS is given in Eq. 5-7 and Eq. 5-8. In frequency domain, the improvement due to CTS is equal to $\left(\frac{f_s}{2\pi f_{dr} m}\right)$. As a result, Eq. 5-10 and Eq. 5-18 become

$$H_{FT} \cdot \left(\frac{f_{dr}}{f_s}\right)^2 < \frac{\left(\Delta x_{max} \cdot \frac{dC}{dx} \cdot \frac{dv_o}{dC}\right)}{(2\pi m)^2 \cdot V_{dr,\,max} \cdot SNR} \qquad \text{(Eq 5-33)}$$

and

$$\frac{f_s}{f_{dr(max)}} > 118 \cdot \sqrt{\gamma_{FT}}\,, \qquad \text{(Eq 5-34)}$$

respectively. For circuits using coupling resistors, γ_{FT} is equal to one and

$$\frac{f_s}{f_{dr(max)}} > 118\,. \qquad \text{(Eq 5-35)}$$

For circuits using coupling switches with γ_{FT} of -40dB [27],

$$\frac{f_s}{f_{dr(max)}} > 11.8\,. \qquad \text{(Eq 5-36)}$$

Comparing Eq. 5-35 to Eq. 5-19 and Eq. 5-36 to Eq. 5-20 shows that correlated triple sampling lowers the frequency separation requirements by factors of 186 and 18.6, respectively.

5.3.2.3 Chopper Stabilization

The principle of chopper stabilization is illustrated in the block diagram in Fig. 5.8. This diagram demonstrates that chopper stabilization can eliminate feedthrough in addition to the 1/f noise. Unlike correlated triple sampling which shapes and attenuates feedthrough, chopper stabilization modulates feedthrough up to the chopping frequency, f_c. Therefore, by choosing the chopping frequency to be at least twice the driving bandwidth, feedthrough is modulated to outside the signal band and can be removed by a low-pass filter. To ease the requirements of the low-pass filter and to reduce the phase delay induced by the filter, the chopping frequency should be several times higher than twice the driving bandwidth,

$$f_c \gg 2 \cdot f_{dr,\,max}\,. \qquad \text{(Eq 5-37)}$$

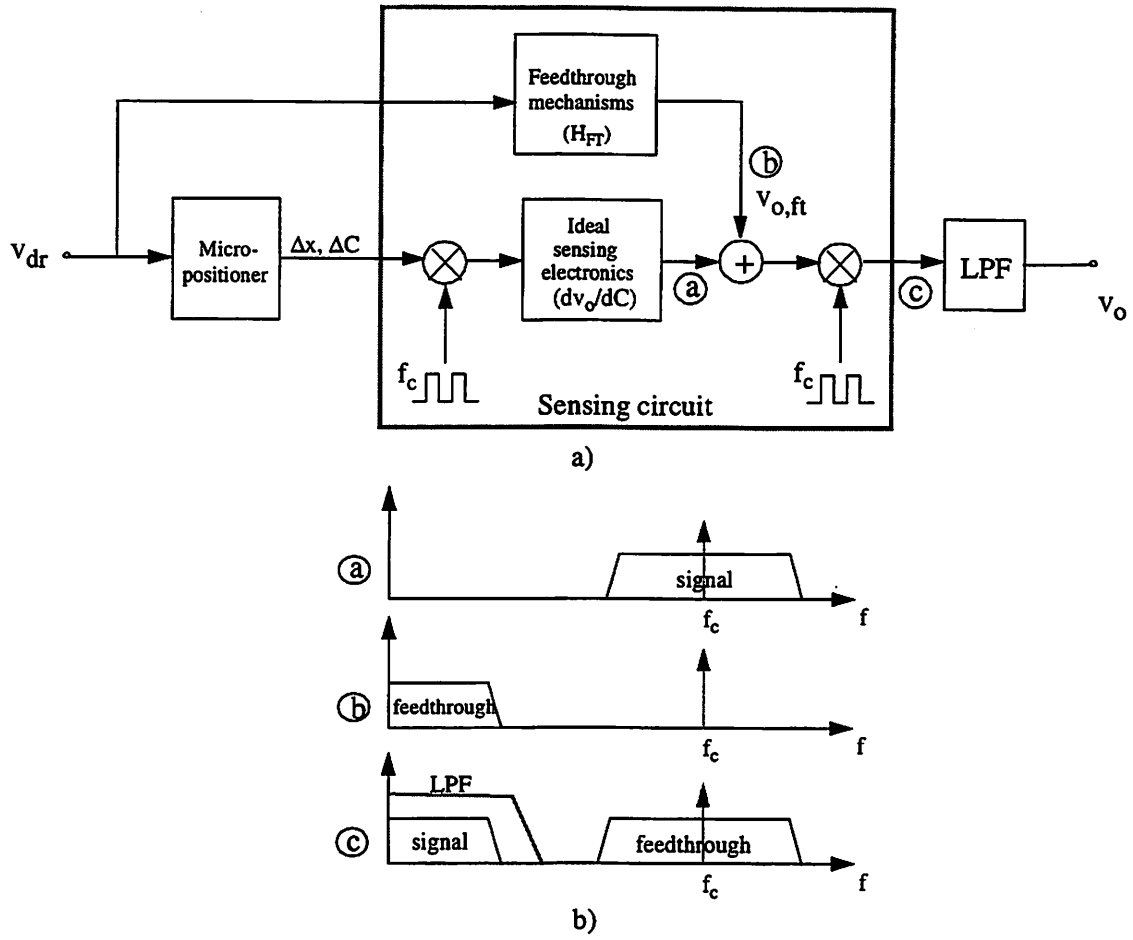
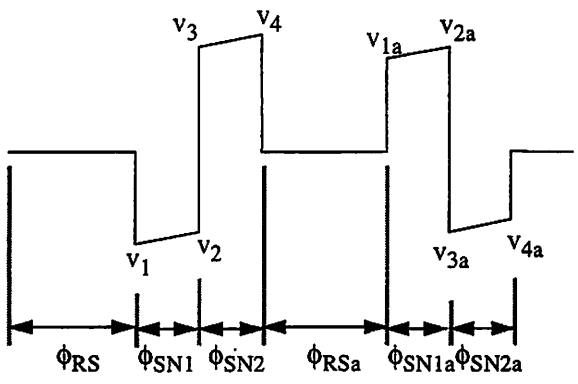


Fig. 5.8: a) A conceptual diagram showing how chopper stabilization can be used to eliminate feedthrough. b) Power spectrum of the signal and feedthrough at different nodes.

In addition, the demodulation should be performed after considerable gain has been added to the sensing signal in order to minimize the feedthrough which couples in after the demodulator.

Chopper stabilization can be implemented in different forms.The synchronous detection scheme discussed in Section 3.2.1 is inherently a chopper stabilizer. For switched-capacitor sensing circuits, chopper stabilization can be implemented by alternating between positive and negative sensing voltage V_S from period to period. This technique results in a chopping frequency equal to one-half of the sensing



Phase	Connections of switch S_1
ϕ_{RS}	V_{CM}
ϕ_{SN1}	$-V_S$
ϕ_{SN2}	$+V_S$
ϕ_{RSa}	V_{CM}
ϕ_{SN1a}	$+V_S$
ϕ_{SN2a}	$-V_S$

Fig. 5.9: Output v_o of the circuit in Fig. 5.7 over two-consecutive periods when both chopper stabilization and correlated double sampling are implemented.

frequency. Furthermore, chopper stabilization can be used in combination with correlated double sampling to eliminate both kT/C noise and feedthrough. Fig. 5.9 shows the output v_o of the circuit in Fig 5.7 when implementing both chopper stabilization and correlated double sampling.

5.4 Voltage-Dependent Capacitance

Driving circuits for micropositioners often have voltage-dependent junction capacitance connected to the outputs at the rotor nodes. Unlike feedthrough which adds to the position signal, voltage-dependent capacitance at the rotor node modulates the position sensing transfer function by varying the capacitive voltage dividing ratio,

$$v_o = f(\Delta C_S, \Delta C_{PR}(V_{dr})) \qquad \text{(Eq 5-38)}$$

To facilitate the discussion, the capacitance-to-voltage transfer function from Eq. 3-19 is repeated here

$$H_{CV} = \frac{v_o}{\Delta C_S} = -\left(\frac{C_{C0}}{C_{PR}+C_{C0}+2C_S}\right)\cdot\left(\frac{C_C}{C_C+C_{PS}+C_S}\right)\cdot\frac{V_S}{C_I} \qquad \text{(Eq 5-39)}$$

From Eq. 5-39, the variation in the transfer function is equal to

$$\Delta H_{CV} = \frac{dH_{CV}}{dC_{PR}} \cdot \Delta C_{PR} = \frac{-H_{CV}}{(C_{PR} + C_{C0} + 2C_S)} \cdot \Delta C_{PR} \cdot \quad \text{(Eq 5-40)}$$

To assure that the variation in the transfer function, or ΔH_{CV}, causes an output error which is smaller than the position resolution,

$$(\Delta C_{S,\max} \cdot (H_{CV} + |\Delta H_{CV}|)) - (\Delta C_{S,\max} \cdot H_{CV}) < \frac{v_{o,\max}}{SNR} \quad \text{(Eq 5-41)}$$

or

$$|\Delta H_{CV}| < \frac{H_{CV}}{SNR} \cdot \quad \text{(Eq 5-42)}$$

Substituting Eq. 5-40 into Eq. 5-42 yields

$$|\Delta C_{PR}| < \frac{(C_{PR} + C_{C0} + 2C_S)}{SNR} \cdot \quad \text{(Eq 5-43)}$$

As an example, for C_{PR}=10pF, C_{C0}=3.5pF, C_S=1pF, and SNR=46dB, ΔC_{PR} must be less than 72.5fF.

Due to the large variations in the driving voltage, ΔC_{PR} can be larger than 72.5fF. To avoid this problem, the output devices at the rotor node should be bootstrapped to ensure that the variation of the junction capacitance is smaller than the value given by Eq. 5-43. As illustrated in Fig. 5.10, the bootstrapping buffer should be connected to V_{dr} via a switch instead of the rotor node to avoid adding its nonlinear input capacitance back to the rotor node. An alternative to bootstrapping is to characterize the variation in the capacitance and perform a self-calibration to compensate for the variation in the capacitive-to-voltage gain.

5.5 Sense-Force Error

In the last two sections, we discussed problems caused by the driving voltages. In this section, we will discuss the opposite. For a micropositioner with single set of electrodes, the sensing voltage which is superimposed on the driving voltage causes the

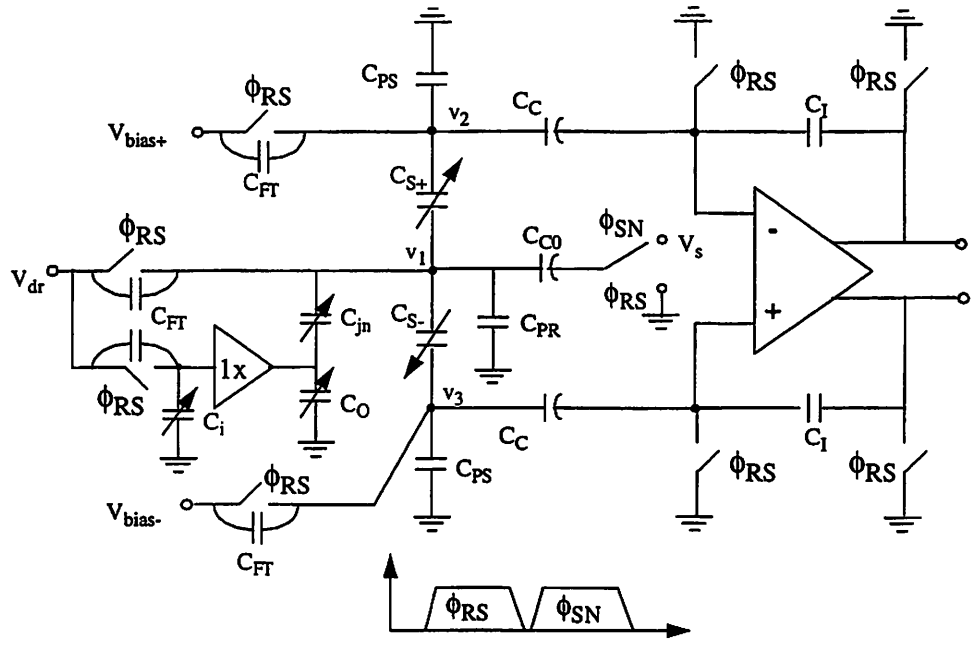


Fig. 5.10: The voltage-dependent capacitance C_{jn} is bootstrapped by a buffer. The input of the buffer is connected to V_{dr} instead of the rotor node to avoid adding its nonlinear input capacitance to the rotor node.

micropositioner to oscillate at the sensing frequency. This position error is commonly called 'sense-force error' and is described in reference [28] for capacitive position sensing for microsensors.

For micropositioners, the amplitude of the oscillation must be restricted to be smaller than the required position accuracy. For a sensing frequency much higher than the resonant frequency of the micropositioner, the position error can be obtained from Eq. 2-23 and Eq. 3-16 as

$$\frac{x_{error}}{V_S} = \frac{a_o f_N^2}{f_s^2} \cdot \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S} \right) \propto \frac{f_N^2}{f_s^2} \qquad \text{(Eq 5-44)}$$

where

$$a_o = \frac{dx}{dV_{dr}} = \frac{k_v V_{bias}}{\omega_N^2 m} \qquad \text{(Eq 5-45)}$$

is the DC gain of the micropositioner, k_v is the voltage-to-force gain, ω_N is the resonant frequency, m is the mass of the moving element, and V_{bias} is the stator bias voltages.

This equation suggests that the sensing frequency must be several times higher than the natural frequency of the micropositioner in order to minimize the position error. As an example, for a micropositioner and a sensing circuit with a_0=0.1μm/V, C_{C0}=3.5pF, C_{PR}=10pF, C_S=1pF, V_S=5V, the sensing frequency must be at least 11 times higher than the natural frequency of the micropositioner to reduce the position error to within 1nm.

5.6 Variations and Mismatches in Coupling Capacitors and Off-Chip Parasitics

Derivations in Section 3.4.2 show that C_{C0}, C_C, C_{PR}, and C_{PS} form capacitive dividers in the signal path; therefore, variations of these capacitors modifies the dividing ratio, thus producing gain errors. The sensitivity of the position sensing transfer function, or H_{CV}, to the capacitance variations is defined as

$$S_C^{H_{CV}} = \frac{C}{H_{CV}} \cdot \left(\frac{dH_{CV}}{dC}\right) \cong \frac{\Delta H_{CV}/H_{CV}}{\Delta C/C} \quad . \qquad \text{(Eq 5-46)}$$

By substituting H_{CV} from Eq. 5-39 into Eq. 5-46,

$$S_{C_{C0}}^{H_{CV}} = \frac{C_{PR}+2C_S}{C_{PR}+C_{C0}+2C_S}, \qquad \text{(Eq 5-47)}$$

$$S_{C_{PR}}^{H_{CV}} = \frac{-C_{PR}}{C_{PR}+C_{C0}+2C_S}, \qquad \text{(Eq 5-48)}$$

$$S_{C_C}^{H_{CV}} = \frac{C_{PS}+C_S}{C_C+C_{PS}+C_S}, \qquad \text{(Eq 5-49)}$$

$$S_{C_{PS}}^{H_{CV}} = \frac{-C_{PS}}{C_C+C_{PS}+C_S}. \qquad \text{(Eq 5-50)}$$

These four equations suggest that maximizing C_{C0} and C_C and minimizing C_{PR} and C_{PS} reduce the sensitivities to capacitance variations. Due to the die area and parasitics constraints, C_{C0} and C_C are usually smaller than C_{PR} and C_{PS} and the magnitudes of

these sensitivities are normally in the range of 0.5 to 0.8. This implies that the variations in these capacitors must be limited to approximately the same order as the allowable gain error.

Examining the position sensing circuit for micropositioners reveals that mismatches in coupling capacitors C_C and parasitic capacitor C_{PS} produce output offsets. The offsets due to these mismatches can be calculated from Eq. 3-16 to Eq. 3-18 as

$$\frac{\Delta V_o}{\Delta C_C} \approx \frac{C_S(C_S + C_{PS})}{C_I(C_S + C_C + C_{PS})^2} \cdot \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S}\right) \cdot V_S \qquad \text{(Eq 5-51)}$$

and

$$\frac{\Delta V_o}{\Delta C_{PS}} \approx \frac{-C_S C_C}{C_I(C_S + C_C + C_{PS})^2} \cdot \left(\frac{C_{C0}}{C_{C0} + C_{PR} + 2C_S}\right) \cdot V_S \,. \qquad \text{(Eq 5-52)}$$

Compared these offset transfer function to the position sensing transfer function yields

$$\frac{\Delta V_o/\Delta C_C}{\Delta V_o/\Delta C_S} \approx \frac{-C_S(C_S + C_{PS})}{C_C(C_S + C_C + C_{PS})} \,. \qquad \text{(Eq 5-53)}$$

and

$$\frac{\Delta V_o/\Delta C_{PS}}{\Delta V_o/\Delta C_S} \approx \frac{C_S}{(C_S + C_C + C_{PS})} \,. \qquad \text{(Eq 5-54)}$$

For C_S=1pF, C_C=3.5pF, and C_{PS}=7pF, the sensitivities to ΔC_C and ΔC_{PS} are 19.9% and 8.7% of the sensitivity to ΔC_S, respectively. For a capacitor matching of 0.5%, ΔC_C is equal to 17.5fF and the offset due to ΔC_C is equivalent to ΔC_S of 3.5fF. For C_{PS}, the mismatch can be as large as several hundred femtofarads depending on the assembly technique and the implementation of the high-voltage driving circuit. Assuming a ΔC_{PS} of 100fF, the offset due to ΔC_{PS} is equivalent to ΔC_S of 8.7fF. Unlike the offset due to the sensing electronics, offsets due to mismatches in C_C and C_{PS} cannot be attenuated by correlated double sampling or chopper stabilization and usually dominate the overall offset.

Table 5.2: A summary of techniques to reduce the gain variation and offset. ('**x**' signifies that the means is effective.)

Techniques	Gain variation	Offset
Large coupling capacitors	x	x
Monolithic implementation of the driving circuit, flip-chip bonding, chip-on-board, etc.	x	x
Common-centroid layout of C_C		x
Calibration and trimming	x	x
Micropositioner with two sets of stators	x	x

Table 5.2 summarizes techniques that can be used to reduce the gain variation and offset. First, Eq. 5-47 to Eq. 5-50 suggest maximizing C_{C0} and C_C, and Eq. 5-53 and Eq. 5-54 suggest maximizing C_C. Second, implementing the driving circuit monolithically and utilizing assembly techniques such as flip-chip bonding and chip-on-board reduce parasitics and result in a better-controlled and better-matched parasitics. The outcome is a higher and more precise gain and a smaller offset. Third, the mismatch in C_C can be minimized by a proper layout such as the common-centroid geometry. Next, offset and gain variation can be reduced by trimming or by post-processing operations such as digital calibration. Lastly, a micropositioner with two sets of stator electrodes, as will be discussed in the Appendix 3, eliminates the need for coupling capacitors to shield the driving voltage. Therefore, the signal attenuation due to capacitive voltage divider, gain error, and offset are eliminated.

5.7 Summary

In this chapter, we have investigated issues related to the interface between capacitive position sensing and electrostatic actuation, namely the sensing charge leakage, feedthrough, voltage-dependent capacitance at the rotor node, sense-force error, and gain variations and offsets due to coupling capacitors and off-chip parasitics. Among these issues, feedthrough is the most critical one because the driving signals are often four to five orders of magnitude larger than the position signals. Ideally, feedthrough can be eliminated by utilizing coupling switches to isolate the driving and the sensing circuits during the sensing period. In practice, nonidealities contribute to feedthrough which cannot be removed by this technique. Techniques to further reduce the feedthrough includes frequency division, correlated triple sampling, chopper stabilization, and modeling and subtracting the error from the output. Among these techniques, chopper stabilization is potentially the most effective method because it translates feedthrough to outside the signal band and does not rely on any modeling.

In addition to feedthrough, voltage-dependent capacitance at the rotor node must be minimized to avoid modulating the sensing transfer function. Increasing the output impedance of the driving circuit by using large resistors or switches minimizes the leakage of the sensing charge. Sense-force error may be reduced to negligible levels by choosing the sensing frequency to be much higher than the natural frequency of the micropositioner. Gain variations and offsets due to coupling capacitors and off-chip parasitics can be reduced by a combination of techniques summarized in Table 5.2.

Chapter 6

Prototype Design and Measurement Results

6.1 Introduction

This chapter describes a prototype implementation and experimental verification of a closed-loop electrostatic micropositioner for a disk drive application. The target specifications are listed in Table 6.1. These specifications are modified from those presented in Table 1.1 to reflect the limited force constant of the micropositioner used in this experiment.

As we have seen in the previous chapters, a position sensing circuit for a micropositioner cannot be developed as an independent building block because its design is closely linked to the design of the micropositioner and the high-voltage driving circuit. In this chapter, all the building blocks that are required to implement a closed-loop electrostatic positioning system as shown in Figure 6.1 will be described. We will begin with the description of the micropositioner. This is followed by the design of the high-voltage driving circuit, the position sensing circuit, and the feedback controller, respectively. Finally, the measurement results will be presented.

Table 6.1: Target specifications for the closed-loop electrostatic positioning system.

Parameters	Values
Maximum force	80μN
Maximum driving voltage	±40V
Maximum displacement	±1μm
Position accuracy	10nm
Bandwidth	1kHz
Position sensing sensitivity	~50mV/μm

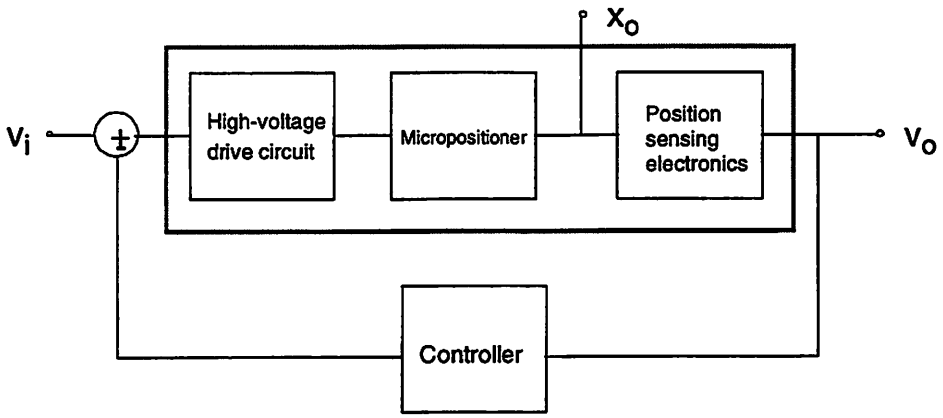


Fig. 6.1: Block diagram of a closed-loop electrostatic positioning system.

6.2 Micropositioner

Several electrostatic micropositioners [5]-[7] have been developed for the magnetic disk drive application described in Chapter 1. The experiment described in this chapter, however, employs the micropositioner described in reference [7]. Figure 6.2 shows an SEM of this micropositioner with a pico-slider bonded to the moving element, or the rotor. This micropositioner utilizes a transverse comb structure with a

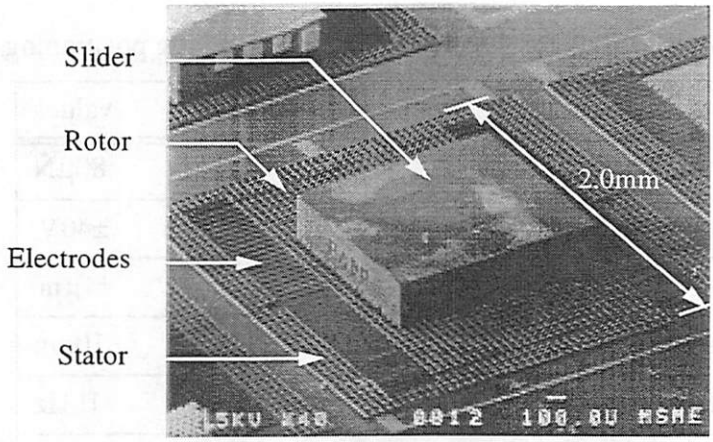


Fig. 6.2: An SEM of the 2.2mmx2.0mm micropositioner used in this study. A 1.2mmx1.0mmx0.3mm slider is mounted on top of the rotor. (Courtesy of D. Horsley, UC Berkeley.)

Table 6.2: Parameters of the micropositioner with a slider payload and stator bias voltages of ±40 V· [7]

Parameters	Source*	Value
Nominal gap (μm)	D	10
Structure thickness (μm)	D	20
Total capacitance (fF)	C	330
dC/dx (fF/μm)	C	68
Rotor mass, m (μg)	I	44
Pico slider mass, m_s (μg)	I	1600
Voltage-to-force gain, k_v (nN/V^2)	I	50
Mechanical spring constant, k_m (N/m)	I	29
Electrostatic spring constant, k_e ($N/m/V^2$)	I	$5.9 \cdot 10^{-3}$
Damping coefficient, b (N/(m/s))	I	$1.03 \cdot 10^{-4}$
Voltage-to-position DC gain (μm/V)	M	0.10
Resonant frequency, ω_r (Hz)	M	550
Quality factor, Q	M	55

*: D=Designed Value, C=Calculation, M=Measurement, I=Inferred from measurements

single set of electrodes for both electrostatic actuation and capacitive position sensing. Table 6.2 summarizes the parameters of the micropositioner.

6.3 Position Sensing Circuit

In order to achieve the required position resolution and dynamic range with the micropositioners described in references [5], [6], [7], the prototype position sensing circuit is designed to measure capacitance variations between 0.5fF and 350fF for nominal sense capacitances up to 2.5 pF. Meanwhile, parasitics at the rotor (C_{PR}) and the stator nodes (C_{PS}) are estimated to be as large as 10pF and 7pF, respectively.

Fig. 6.3 shows a simplified circuit and clock diagram of the sensing circuit. The circuit consists of three stages: a front-end capacitance sensing circuit or a charge integrator, a preamplifier, and an output buffer. The circuit incorporates the following concepts that have been discussed in the previous chapters: switched-capacitor sensing scheme (Section 3.2.2), pseudo-differential topology (Section 3.3), high-voltage shielding capacitors (Section 3.4), correlated double sampling (Section 4.3), time-division technique (Section 5.2.2), and frequency separation (Section 5.3.2).

The operations of the circuit are divided into three phases. The reset phase, or ϕ_{RS}, has a duty cycle of 50%, while each of the sensing phase (ϕ_{SN1} and ϕ_{SN2}) has a duty cycle of 25%. During ϕ_{RS}, the charge integrator and the preamplifier are reset, and the driving circuit is connected to the micropositioner, which is modeled as the capacitor C_S. At the end of ϕ_{RS}, the driving circuit is disconnected from the micropositioner, and the charge integrator and the preamplifier are released from the reference voltage. During ϕ_{SN1}, the offset, 1/f noise, switch-charge injection, and kT/C noise of the charge integrator and the preamplifier are stored on C_H. At the end of this phase, the top plate of C_H is released from the reference. During ϕ_{SN2}, the sensing voltage is applied by reconnecting C_{C0} from $-V_S$ to $+V_S$. The output of the preamplifier,

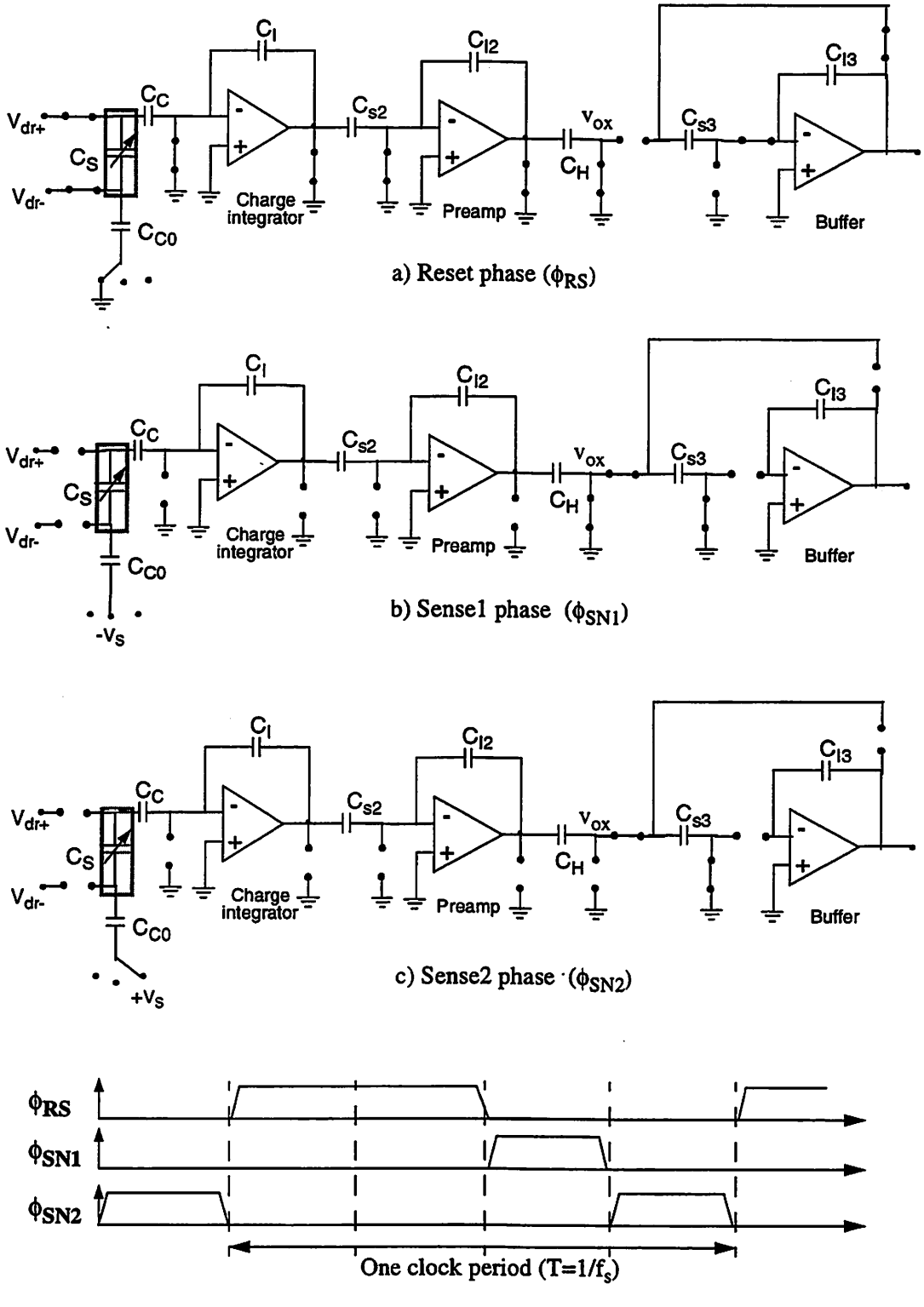


Fig. 6.3: Simplified diagram of the position sensing circuit showing operations during the three phases.

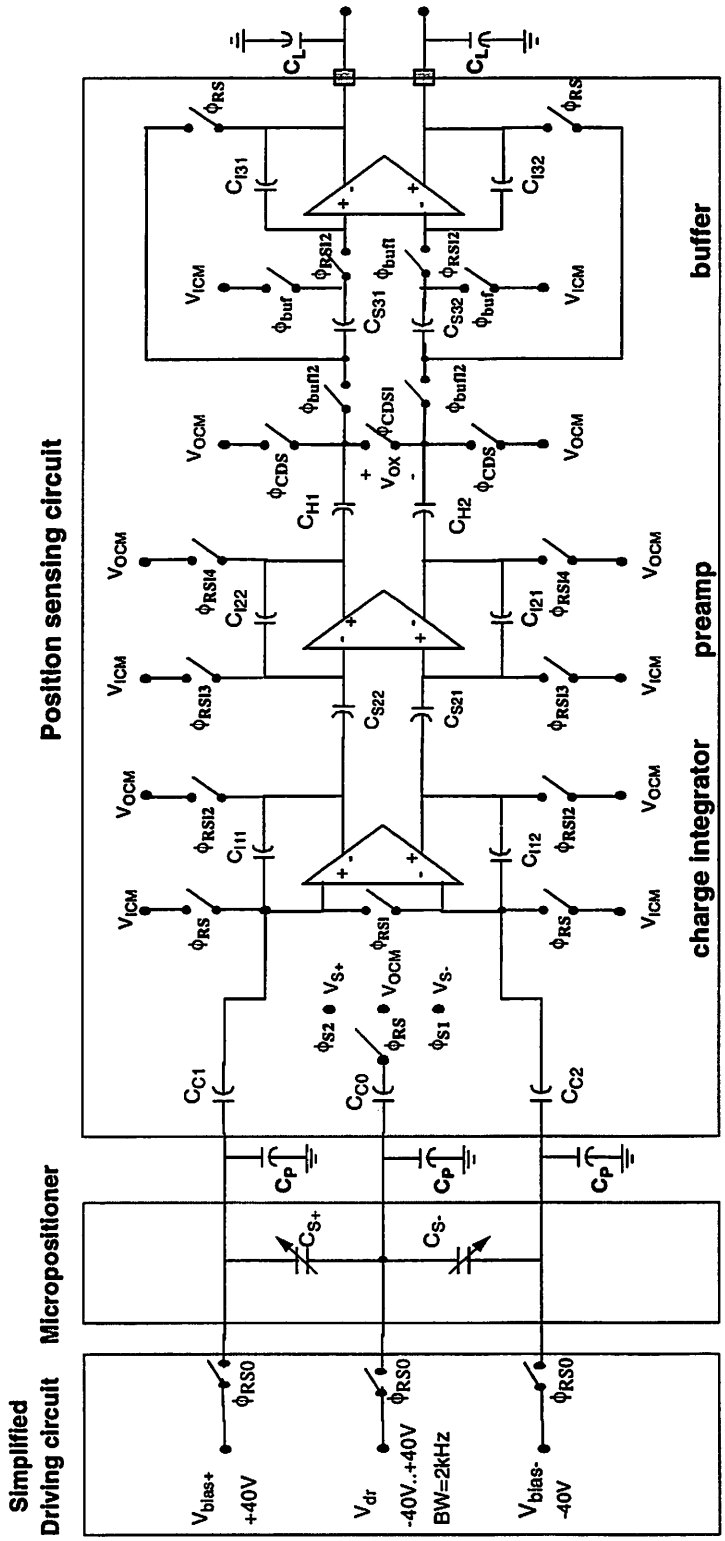


Fig. 6.4: Complete circuit diagram of the prototype position sensing circuit

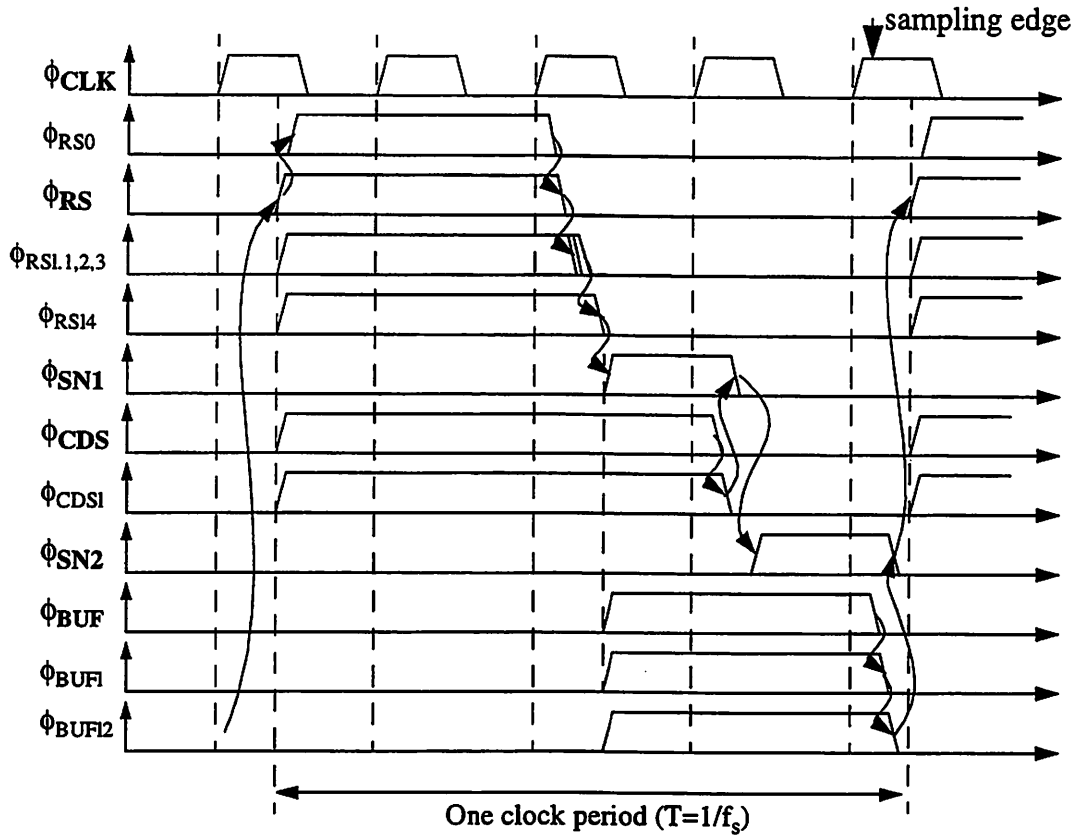


Fig. 6.5: Complete clock diagram of the prototype sensing circuit. Delays and non-overlappings are indicated with arrows.

which contains both the signal and the error, is subtracted by the error voltage previously stored in C_H. Since the errors remain virtually unchanged during ϕ_{SN1} and ϕ_{SN2}, the output voltage v_{ox} contains only the signal. Meanwhile, the buffer samples the output v_{ox} during ϕ_{SN2} and performs evaluation during ϕ_{RS}.

The complete circuit and clock diagrams are shown in Fig. 6.4 and Fig. 6.5, respectively. The clock diagram in Fig. 6.5 shows ϕ_{CDS}, ϕ_{BUF}, and early and delay phases in addition to the three phases described earlier. ϕ_{CDS} spans the same period as both ϕ_{RS} and ϕ_{SN1}, while ϕ_{BUF} spans the same period as both ϕ_{SN1} and ϕ_{SN2}. The non-overlapping, early, and delay phases are needed to ensure proper operations and minimize switch charge injection.

The prototype was fabricated in a 1.2-μm 5-V double-poly double-metal n-well CMOS process, has a total die area of 2.2x2.2mm^2, and dissipates 26mW. The operating frequency is chosen as 1MHz due to three reasons. First, to attenuate the 1/f noise by correlated double sampling (Eq. 4-6), the sampling frequency must be at least in the same order as the 1/f noise corner of the devices, which is approximately 1MHz for minimum length devices in this process. Second, the discussion of feedthrough in Section 5.3 demonstrates that a higher separation between sensing and driving frequency provides a larger attenuation of feedthrough. Third, the sampling frequency should not be higher than one megahertz to avoid interference with the read channel of the disk drive, which extends from a few megahertz up to several hundreds megahertz.

In the following sections, we will describe the design of each building block of the prototype sensing circuit.

6.3.1 High-Voltage Interface

To allow the sensing electronics to be fabricated in a conventional low-voltage technology, the sensing circuitry must be shielded from the driving voltages of the micropositioner, which can be as high as ±40V. This can be achieved by utilizing coupling capacitors as described in Section 3.4.

Fig. 6.6 shows the high-voltage interface of the sensing circuit along with the micropositioner and the high-voltage driving circuit. The driving circuit incorporates output switches which are driven by the reset clock ϕ_{RS0}. These switches restrict the driving voltage to be updated only while the sensing circuit is reset and decouple the driving circuit from the sensing circuit during the sensing period. This time-division technique was discussed in Section 5.2.2.

Metal-metal coupling capacitors are inserted between the charge integrator and the micropositioner to shield the sensing circuit from the driving voltages. The

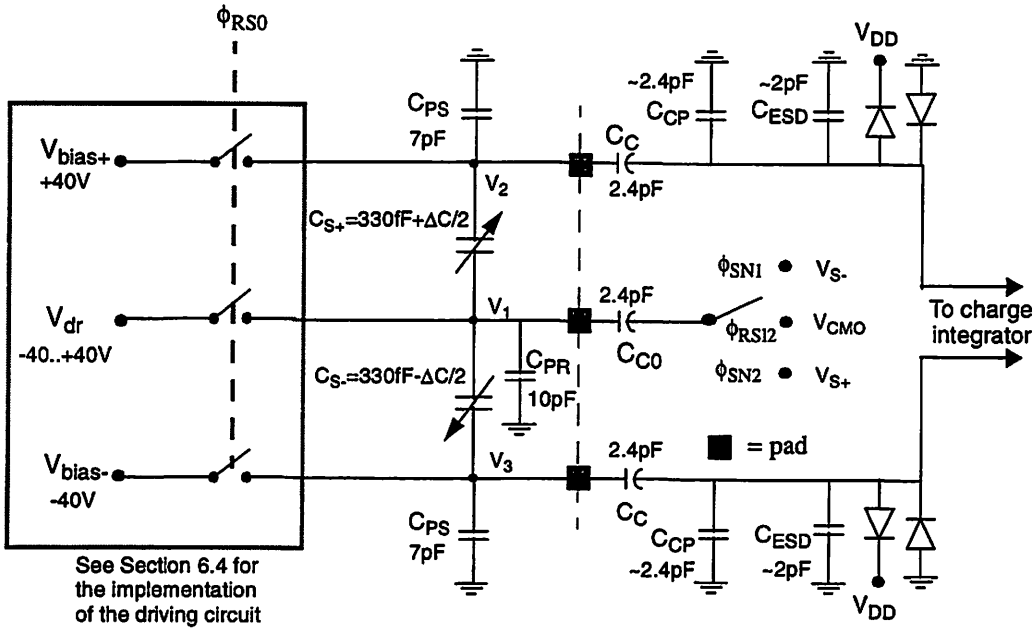


Fig. 6.6: Circuit diagram of the high-voltage interface

oxide thickness of 7500 Angstroms between the two metal layers permits driving voltages as high as 225 volts, without exceeding the oxide breakdown field of $3x10^6$V/cm. The top-plates of the coupling capacitors are connected to the high voltage nodes to avoid adding bottom-plate parasitics to the loads of the high-voltage driving circuit. This configuration, however, adds bottom-plate parasitics of C_C to the charge integrator summing nodes, thus resulting in a reduction in the feedback factor, and increases in noise and power consumption. Nevertheless, Eq. 3-22, Eq. 3-23, and the plot in Fig. 6.7 shows that the reduction in resolution is only approximately ten percent compared to connecting the bottom plates to the high-voltage nodes.

All the coupling capacitors are chosen, according to Eq. 3-22, as 2.4pF to achieve the required capacitance resolution for estimated parasitics at the rotor (C_{PR}) of 10pF and parasitics at the stator (C_{PS}) of 7pF. According to Fig. 6.7, even though the coupling capacitors C_C of 2.4pF are 30 percent smaller than the optimal value, the

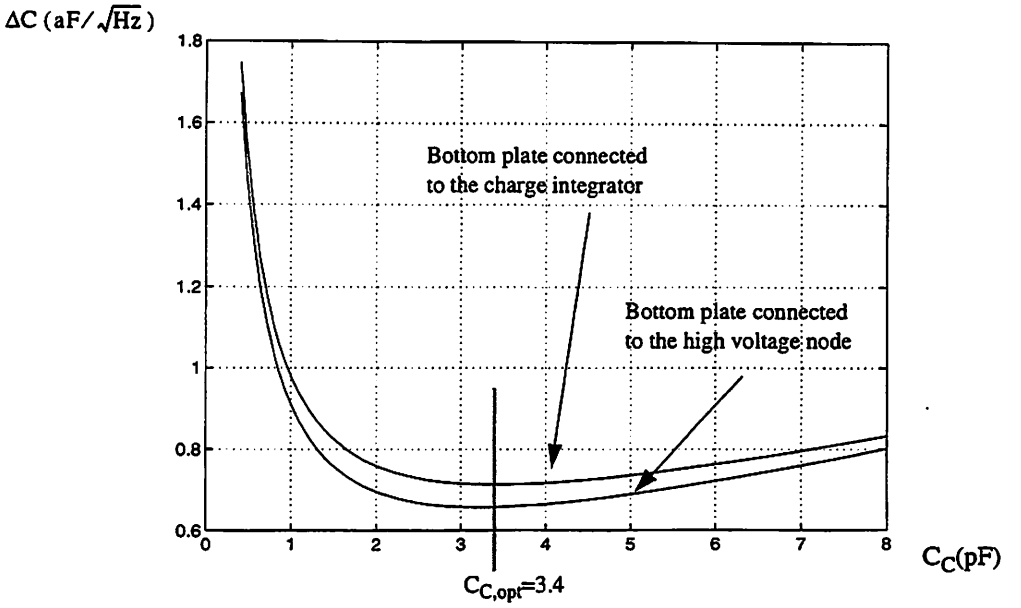


Fig. 6.7: Relationships between capacitance sensing resolution and the size of coupling capacitors C_C for C_S=0.33pF, C_I=1pF, C_{ESD}=2pF, C_{PR}=10pF, C_{PS}=7pF, V_S=5V, f_u/f_s=7, $C_{CP}=C_C$, and an amplifier input-referred noise of 4nV/$\sqrt{Hz}$.

resolution decreases by only ten percent. Higher resolution, if needed, can be achieved by using larger C_{C0} and optimal C_C.

Furthermore, ESD protection devices are added at the inputs of the charge integrator to protect the amplifier input devices from an electrostatic discharge or a sudden change in the driving voltage while the sensing circuit is not being operated. Unlike typical circuits, ESD protection devices cannot be located at the pads, or the top-plate of the coupling capacitors, because they would be turned on by the high-voltage drive of the micropositioner. These devices add approximately 2pF of parasitic capacitance to the charge integrator summing nodes.

6.3.2 Charge Integrator and Preamplifier

Fig. 6.8 shows the circuit diagram of the charge integrator and the preamplifier. Correlated double sampling (Section 4.3) is performed at the output of the preamplifier using error-storage capacitors C_H and a few switches. This particular CDS

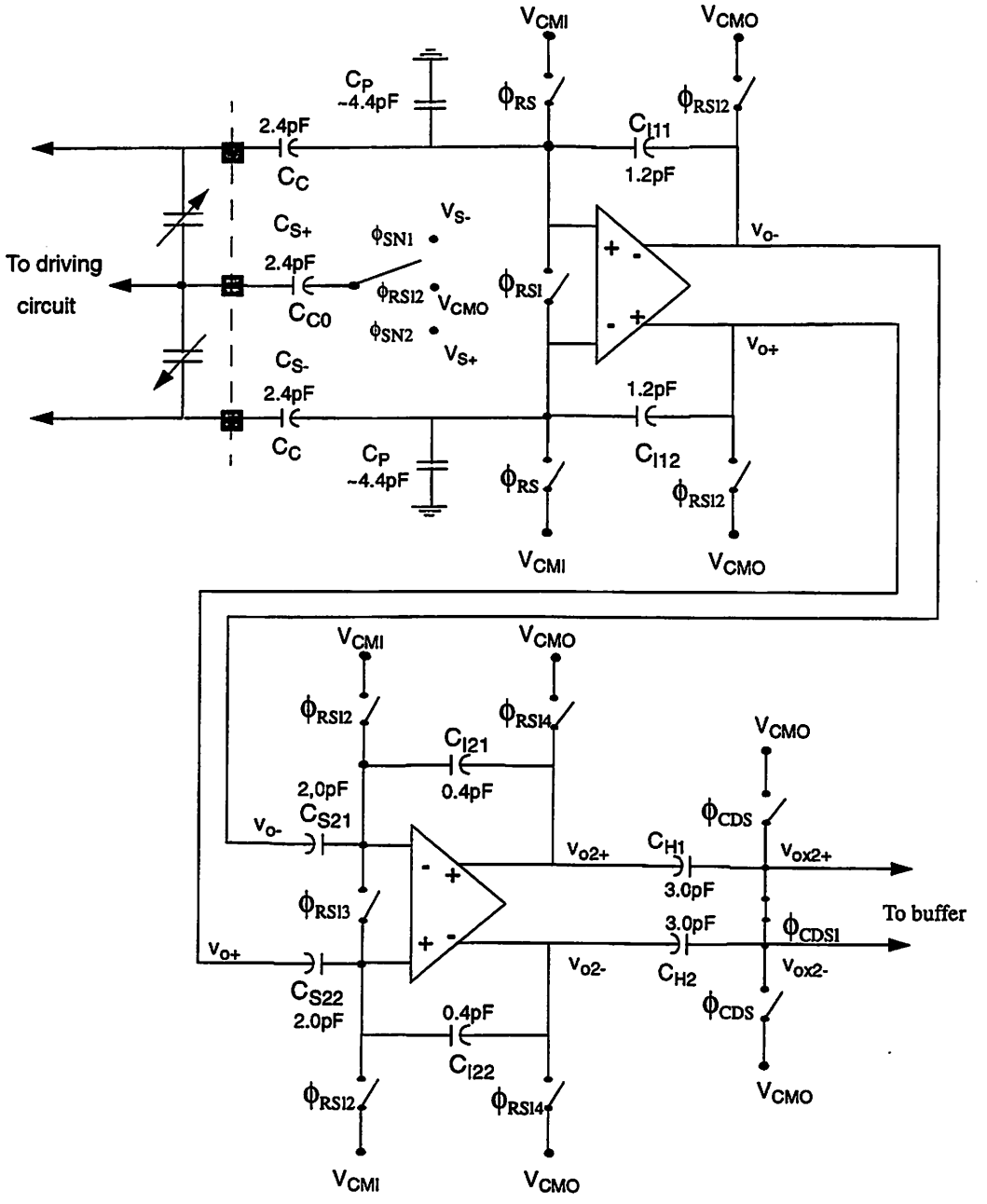


Fig. 6.8: Circuit diagram of the charge integrator, preamplifier, and the error-storage capacitor (C_H) for correlated double sampling.

scheme attenuates the offset, 1/f noise, switch-charge injection, and kT/C noise of both the charge integrator and the preamplifier with minimal increase in circuit and clock complexities.

The operations of the charge integrator, the preamplifier, and CDS was explained earlier in this section. In contrast to the simplified circuit shown in Fig. 6.3, the reset switches of the charge integrator and the preamplifier are opened in consequence when ϕ_{RS} and its delay phases go high in order to minimize the charge injection. Additionally, because V_{S-} is typically the ground voltage and V_{S+} is typically the supply voltage, C_{C0} is connected to V_{CMO}, which is approximately half the supply voltage, during the reset phase to equalize the negative and positive sensing pulses, thus avoiding adding an offset to the micropositioner driving voltage V_{dr}.

For the charge integrator, the total parasitic capacitance at each summing node is approximately 7pF—contributed mainly by the coupling capacitor C_C, its bottom-plate parasitics, and the ESD protection devices. Choosing an integrating capacitor of 1.2pF yields a feedback factor of 1/7, a reasonable trade-off between signal gain, noise, and amplifier bandwidth. For the preamplifier, the sampling capacitors and the integrating capacitors are chosen as 2.0pF and 0.4pF, respectively, to achieve a gain of five and the same feedback factor as the charge integrator. The error-storage capacitors C_H are chosen as 3pF to achieve a high signal coupling to the sampling capacitors of the buffer, C_{S3}. For C_{S3} equal to 0.5pF, the voltage transfer ratio is roughly 0.8, reducing the effective gain of the preamplifier to 4.0. By choosing similar load capacitances and feedback factors for the charge integrator and the preamplifier, identical amplifiers can be used in both stages. Despite using the pseudo-differential topology, the input common-mode shift (Section 3.3) of the charge integrator is not an issue. This is because small signal coupling through the coupling capacitors results in a common-mode shift of only 100mV. Furthermore, the offset and gain error due to the input common-mode shift is much smaller than those due to the variations and mismatches of off-chip parasitics C_{PR} and C_{PS}.

In switched-capacitor sensing circuits, the amplifier DC gain and settling accuracy are typically determined from the dynamic range of the system. In the

prototype application, the dynamic range is calculated from the maximum sensing range of 2μm and the resolution of 10nm, and is equal to 200 or 46dB. Taking into account the offset due to the amplifiers and the external parasitics C_{PS} and C_{PR} which could be a few times larger than the signal, the amplifiers in the prototype are designed for a dynamic range of 1000 or 60dB. To avoid nonlinearities due to the variation in the amplifier gain and settling accuracy, the amplifier must have a gain of at least 1000 and a settling accuracy better than 1/1000 or 0.1%. For a first-order system and ignoring slewing, a settling of 0.1% translates into a settling of seven time constants. For the charge integrator and the preamplifier which settle in cascade, each stage must settle to nine time constants in order to achieve the same settling accuracy. In this implementation, the amplifiers for both stages are identical and have closed-loop bandwidths of approximately 7MHz and settle to ten time constants during both ϕ_{SN1} and ϕ_{SN2}.

In Section 4.4, we have shown that, in order to achieve the highest sensing resolution for a given technology, the gate capacitance of the amplifier input device must be equal to all other capacitances at the summing node ($C_{IP} = C_T' \approx C_C + C_{CP} + C_{ESD} + C_I$). This optimization, however, is not practical in this prototype because of a very large C_T' of approximately 8.2pF. The amplifier described in Section 6.3.5 demonstrates that an amplifier with relatively small input devices can achieve the required input-referred noise of $4nV/\sqrt{Hz}$ and the required resolution of $1aF/\sqrt{Hz}$ (See Table 6.3). Using this amplifier which has $C_{IP} \approx C_T'/40$, the resolution improvement due to kT/C noise cancellation of correlated double sampling is 6dB, according to the noise calculation in Appendix 1. In comparison, an optimal amplifier with $C_{IP} \approx C_T'$ yields another 10dB improvement in resolution at the expense of 40 times increase in power consumption.

Table 6.3: A summary of the required amplifier noise calculation. Key results are shown in shaded rows.

Parameters	Values
Δx_{min}	10nm
dC/dx	68fF
Sensing bandwidth	25kHz
Required ΔC_{min}	4.3aF/$\sqrt{Hz}$
Designed ΔC_{min}	1aF/$\sqrt{Hz}$
C_S	0.33pF
C_I	1.2pF
C_C, C_{C0}, C_{CP}	2.4pF
C_{PR}	10pF
C_{PS}	7pF
C_{ESD}	2pF
f_u/f_S	7
V_S	5
Using Eq. 3-22, and assuming $C_{IP}<<C_C+C_{CP}+C_{ESD}+C_I$ and 3dB noise penalty due to CDS	
Amplifier input-referred noise	<4.0nV/$\sqrt{Hz}$

6.3.3 Output Buffer

This prototype position sensing circuit requires an output buffer because the output of the correlated double sampling circuit (v_{ox}) has a small load-driving capability and is valid only for a small portion of the clock cycle. The operation of the switched-capacitor output buffer shown in Fig. 6.4 can be explained as follows. During ϕ_{BUF}, the sampling capacitor C_{S3} samples the output v_{ox}. During ϕ_{RS} of the next clock period, C_{S3} is reconnected across the integrating capacitor C_{I3} to update the charge stored on C_{I3}. Since C_{I3} is always connected across the amplifier, the output of the buffer circuit, unlike those of the first two stages, is available during the whole clock period. This buffer circuit is suitable for driving large loads because the amplifier only

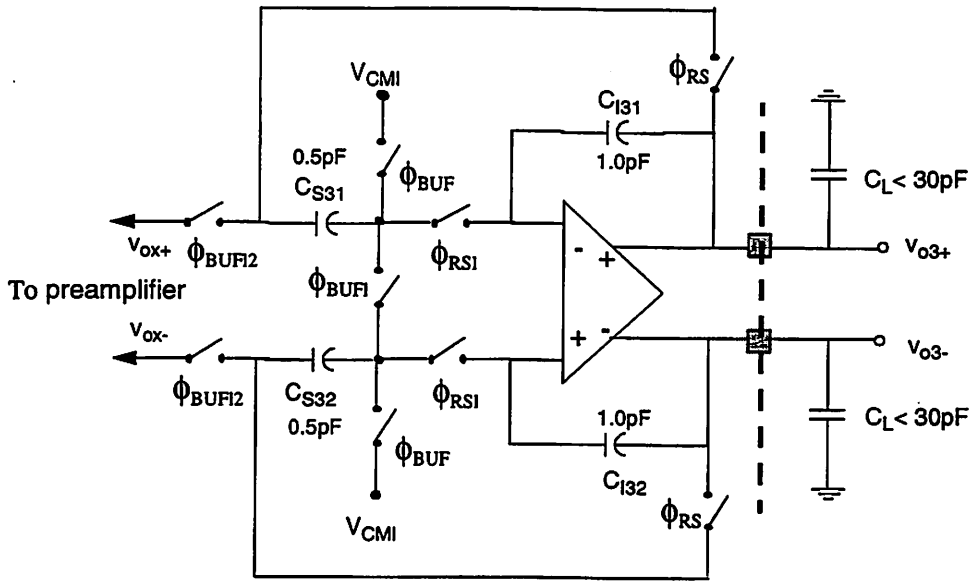


Fig. 6.9: Circuit diagram of the output buffer

needs to supply the load current and not the amplification and because of the small output steps due to oversampling.

In addition to the sinc function of the zero-order hold operation, this circuit performs low-pass filtering to attenuate noise at frequencies above the sensing bandwidth. The low-pass filtering can be illustrated from its transfer function,

$$H(z) = \frac{C_S z^{-1/2}}{(C_S + C_I) - C_I z^{-1}} \qquad \text{(Eq 6-1)}$$

By mapping from the z-domain into the frequency domain, the magnitude response of the buffer circuit, including the zero-order hold, can be calculated as

$$|H(e^{j\omega T})| \approx \frac{\left(\frac{C_I}{C_S + C_I}\right)}{\sqrt{1 + \left(\frac{C_I}{C_S + C_I}\right)^2 - \frac{2C_I \cos\omega T}{C_S + C_I}}} \cdot \frac{\sin(\pi f / f_s)}{\pi f / f_s} \qquad \text{(Eq 6-2)}$$

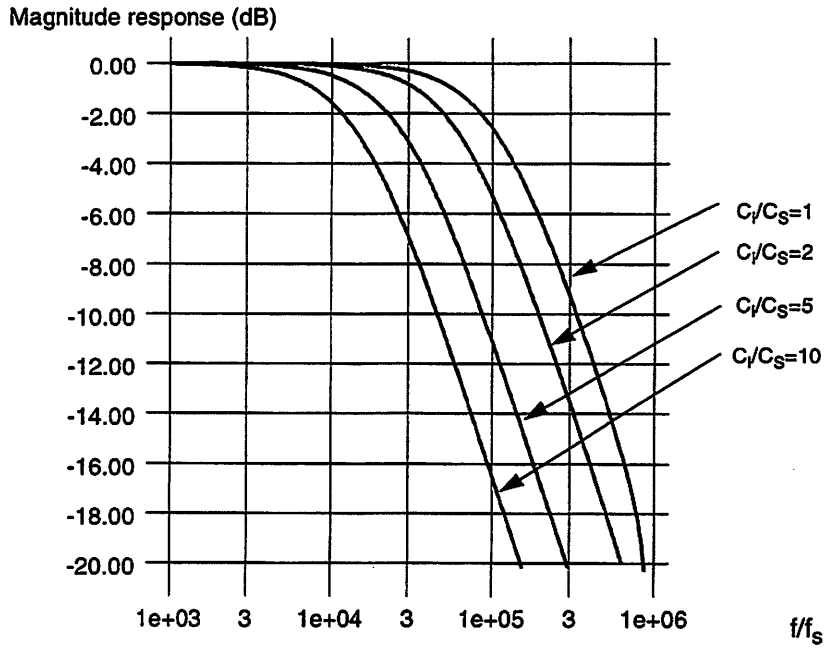


Fig. 6.10: The magnitude of the transfer function of the output buffer for different ratios of C_I and C_S

Fig. 6.10 shows magnitude responses of this circuit for different ratios of C_I and C_S. In this prototype, a C_I-to-C_S ratio of two is chosen to limit the attenuation at the edge of the 25kHz sensing bandwidth to less than 0.5dB.

An amplifier similar to that of the charge integrator and preamplifier but with the current and device sizes scale by 0.5 is used in the buffer circuit. For C_I=1pF and C_S=0.5pF, the amplifier feedback factor is approximately 0.9. With a load capacitance of 30pF, the amplifier has a closed-loop bandwidth of 2.9MHz and settles to approximately nine time constants during ϕ_{RS}.

6.3.4 Self-Test circuit

The position sensing circuit includes a self-test circuit as shown in Fig. 6.3 allowing it to be tested before assembly with the micropositioner and the high-voltage circuitry. Ideally, the self-test circuit should produce a capacitance variation similarly

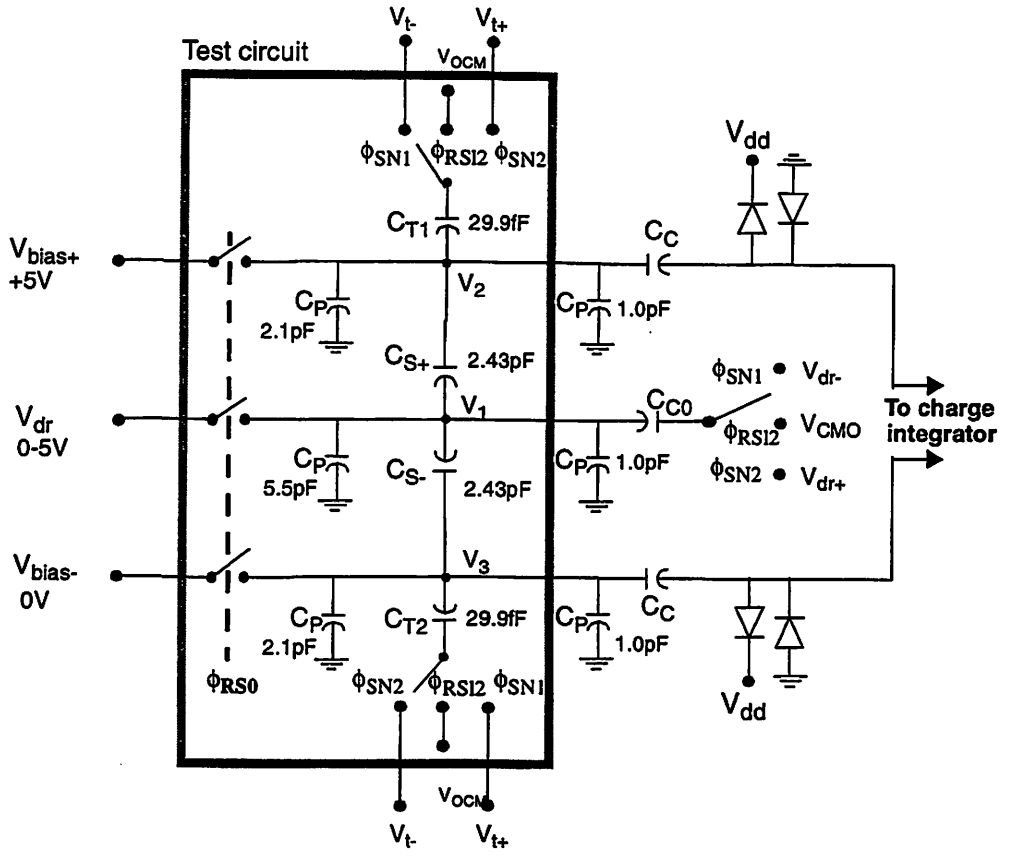


Fig. 6.11: Circuit diagram of the self-test circuit included in the prototype sensing circuit

to the micropositioner. A CMOS process, however, does not have a high quality variable capacitor. To solve the problem, small fixed capacitors C_{T1} and C_{T2} are connected to varying test voltages V_{t+} and V_{t-} to generate dummy charges in the order of femto-coulombs. V_{bias+}, V_{bias-}, and V_{dr} and the switches are added to simulate the micropositioner driving voltages. However, these voltages are limited to only between the supply and ground of the sensing circuit. Additionally, C_S and C_P are added as dummy sense capacitance and parasitic capacitance.

The test charge generated by connecting C_{T1} and C_{T2} between V_{OCM}, V_{t+}, and V_{t-} is

$$\text{Test charge} = 2(V_{t+} - V_{t-})C_T = 2(0 \rightarrow 5V)30fF = 0 \rightarrow 300fC \qquad \text{(Eq 6-3)}$$

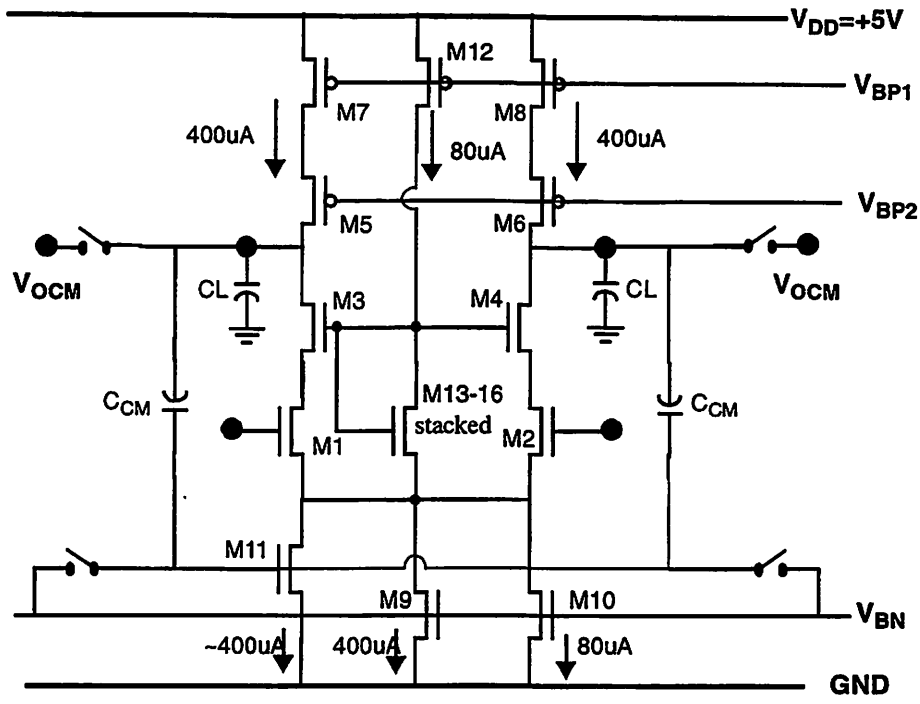
This amount of charge is equivalent to a capacitance variation of up to 300fF for a sensing voltage V_S of five volt and 20% coupling ratio from V_S to the micropositioner rotor node.

6.3.5 Amplifier design

In this prototype, telescopic amplifiers [29] are chosen in all three stages because they are fast and simple, and have low-noise. To realize the required DC-gain of 1000, the amplifiers utilize PMOS devices with longer-than-minimum channel lengths. The maximum output swing of approximately ±1V is easily achieved with a supply voltage of five volts. The amplifier shown in Fig. 6.12 is used in both the charge integrator and the preamplifier. A similar amplifier with half the bias current and half the device size and a different output common-mode feedback circuit are used in the buffer stage.

The amplifier input and output common-mode voltages are chosen at 1.8V and 2.6V, respectively, to maximize the output swing. The NMOS cascode devices are biased locally by M_{12} to M_{16} to track the input common-mode voltage [29], [30]. Because the 1/f noise is eliminated by correlated double sampling, there is no need to use large devices for the input transistors and the PMOS current sources (M_7 and M_8). The amplifier device size and the specifications are summarized in Fig. 6.12.

Dynamic common-mode feedback circuits [31] are employed because they do not require any extra power consumption and do not reduce the output swing. For the charge integrator and the preamplifier, the common-mode feedback capacitors C_{CM} are refreshed by connected directly to the references V_{OCM} and V_{BN} during the reset phase as shown in Fig. 6.12. For the output buffer, in which the amplifier output must be valid at all time, the common-mode feedback capacitors C_{CM} cannot be connected directly to the references, but instead are refreshed by another pair of 0.4pF capacitors [29], [31]. It should be noted that only approximately half of the tail current source is biased by



Transistor	W/L	V_{DSAT}
M_1-M_4	160/1.2	0.2
M_5-M_8	400/2	0.3
M_{10},M_{11}	160/2	0.3
M_9	32/2	0.3
M_{12}	80/2	0.3
M_{13}-M_{16}	17/1.2	N. A.

A_{DC}	>2000
Input common-mode voltage	1.8V
Output common-mode voltage	2.6V
Maximum output swing	4.0V
Open-loop band-width (C_L=4pF)	>60MHz
Input-referred noise	4.1 nv/rt.Hz
C_{CM}	1.2pF
Power	4.4mW

Fig. 6.12: Schematics, device sizes, and specifications of the amplifier used in the charge integrator and the preamplifier

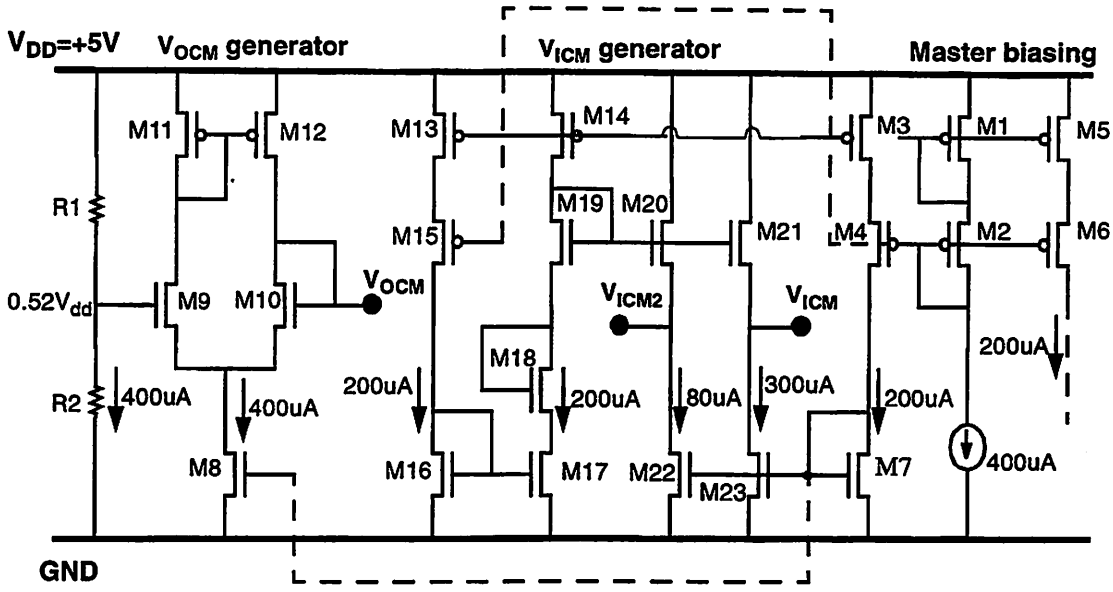
the common-mode feedback circuit to improve the stability of the common-mode feedback loop.

6.3.6 Bias Circuit

In this prototype, all the bias voltages are generated on-chip from an external reference current. The bias circuit of the prototype sensing circuit comprises of the master bias circuit, the input common-mode voltage (V_{ICM}) generator, the output common-mode voltage (V_{OCM}) generator, and the amplifier bias circuit. The first three are shown in Fig. 6.13, while the last one is shown in Fig. 6.14.

The master bias circuit (M_1 to M_6) mirrors the external 400μA reference current to the V_{ICM} generator, V_{OCM} generator, and the amplifier bias circuit. The output common-mode voltage is set by the voltage divider R_1 and R_2 at $0.52V_{DD}$, or 2.60 volt, to maximize the amplifier output swing. The output of the voltage divider is then buffered by a differential pair in a unity-gain feedback loop (M_8 to M_{12}). Meanwhile, the input common-mode level is generated by M_{17} and M_{18}, which replicate the tail current source and the input devices of the amplifier. The gate voltage of M_{18} is buffered by M_{19} to M_{21} to generate V_{ICM} and V_{ICM2}. V_{ICM2} is used by the bias circuit shown in Fig. 6.14, while V_{ICM} is used by the rest of the circuit.

All the transistors in the amplifier bias circuit shown in Fig. 6.14 carry 200μA current, half that of the amplifier in the charge integrator and the preamplifier. V_{BP1} and V_{BN} are generated using conventional current mirrors. The cascode devices M_2, M_4, M_5, M_9, M_{10} force the V_{DS} of M_1, M_3, M_6, M_7, M_8 to be equal to that of the devices in the amplifiers. To maximize the output swing of the amplifiers, V_{BP2} is generated by a high-swing cascode bias circuit. This implementation [32], like other implementations [30], [33], utilizes transistors in the triode region by choosing $(W/L)_{12}$ to be larger than $(W/L)_{11}$.



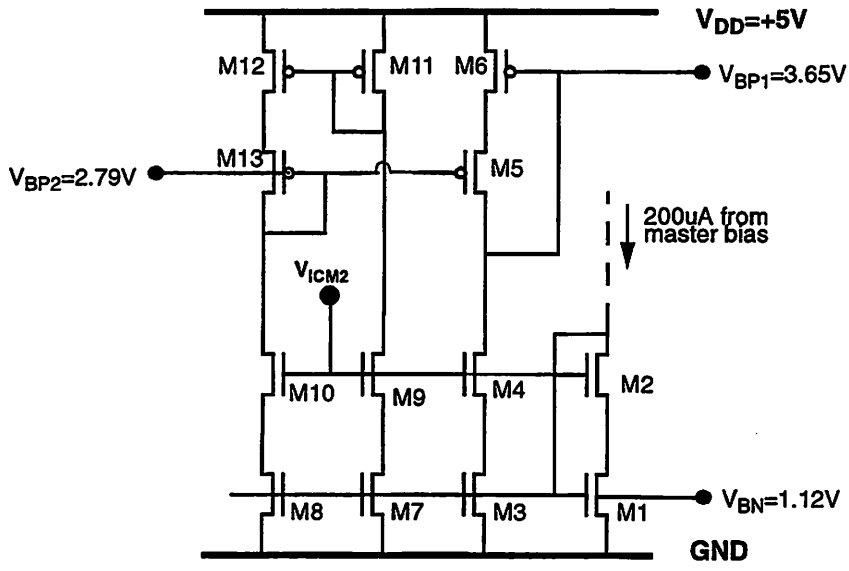
Transistor	W/L
M_1-M_2	300/3
M_3-M_6	150/3
M_7	80/3
M_8	160/3
M_9-M_{12}	150/3
M_{13}-M_{15}	150/3
M_{16}	15/2

Transistor	W/L
M_{17}	17/2
M_{18}	80/1.2
M_{19}	50/2
M_{20}	20/2
M_{21}	75/2
M_{22}	32/3
M_{23}	120/3

Fig. 6.13: Schematics and device sizes of the master bias circuit and the input and output common-mode voltage generators.

6.3.7 Switches

In this prototype, all switches except those at the amplifier summing nodes are CMOS switches. NMOS switches can be used at the amplifier summing nodes because of the low input common-mode voltage of 1.8 volt. All of the switches that are not in the signal path are chosen to achieve seven time-constant settlings, while those in the



Transistor	W/L
M_1, M_3, M_7, M_8	80/2
M_2, M_4, M_9, M_{10}	80/1.2
M_5, M_6, M_{13}	200/2
M_{11}	40/2
M_{12}	46/2

Fig. 6.14: Schematics and device sizes of the amplifier bias circuit

signal paths are chosen to settle to ten time constants in order not to interfere with the amplifier settling.

6.3.8 Clock Generation Circuit

According to Fig. 6.5, the prototype sensing circuit utilizes five main clock phases (ϕ_{RS}, ϕ_{SN1}, ϕ_{SN2}, ϕ_{CDS}, and ϕ_{BUF}) and nine late phases, not including the complementary phases for PMOS devices. All these clock phases are generated on-chip from an external reference clock. As shown in Fig. 6.15, the reference ϕ_{CLK} has a frequency four times the sampling frequency. Two T-flipflops divide the frequency of ϕ_{CLK} by two and four to generate ϕ_{CLK2} and ϕ_{CLK3}, respectively. ϕ_{CLK}, ϕ_{CLK2}, and

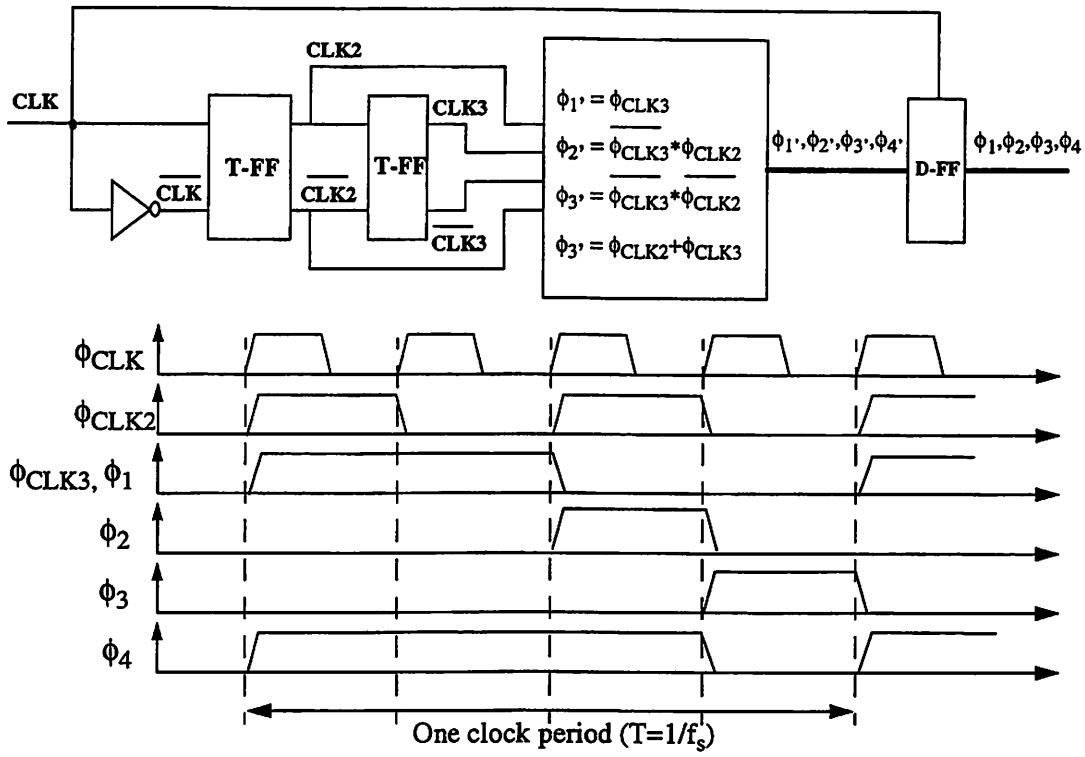


Fig. 6.15: Block diagram of the master clock circuit and the associated clocks.

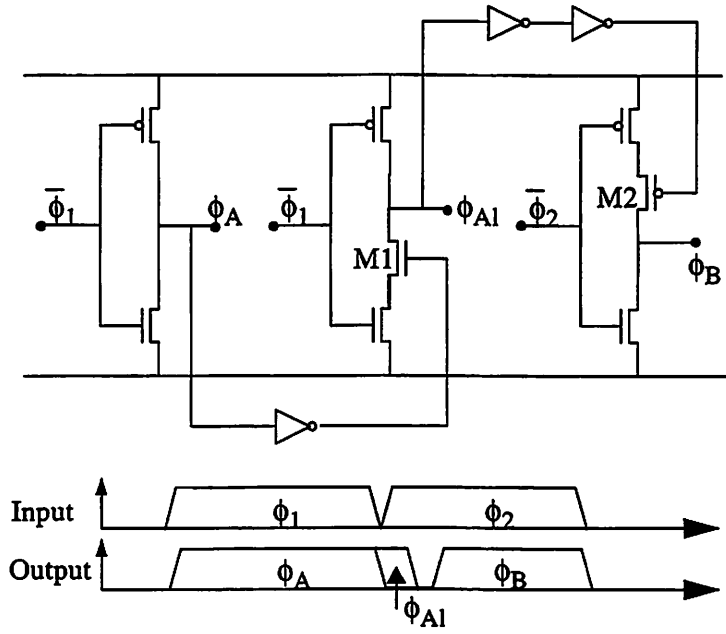


Fig. 6.16: This example shows how a delay phase (ϕ_{A1}) and a non-overlapping phase (ϕ_B) can be generated.

ϕ_{CLK3} are then combined by logic operations and aligned the edges by D-flipflops to generate ϕ_1 to ϕ_4.

Next, ϕ_1 to ϕ_4— which are almost identical to ϕ_{RS}, ϕ_{SN1}, ϕ_{SN2}, and ϕ_{CDS}, respectively, except for the delays and non-overlappings— are used to synthesize all the clock phases shown in Fig. 6.3. The late phases and non-overlapping phases are generated using circuits similar to the one shown in Fig. 6.16 [30]. In this example, M_1 is added in series with the NMOS in the inverter to ensure that the falling edge of ϕ_{RSl} is delayed after that of ϕ_{RS}, thus generating a late-phase. Similarly, M_2 guarantees that the rising edge of ϕ_{SN} is delayed after the falling edge of ϕ_{RSl}, thus creating non-overlapping phases.

6.3.9 Layout

The prototype was designed in a 1.2-μm 5-V double-poly double-metal n-well CMOS process and was fabricated by Orbit Semiconductor. The die photograph is shown in Fig. 6.17. The total die area is 2.2x2.2mm^2.

To separate digital circuits from the sensitive analog circuits, the clock generation circuit is located in the upperright corner, as far away from the charge integrator as possible. It should be noted that the clock generation circuit, which contains more than half of the total number of transistors, consumes only a small die area. Guard rings are used throughout to minimize couplings to and from the substrate. Differential transistors, switches, and signal paths are laid out close to each other and in the non-mirror symmetry fashion to ensure matching and identical noise couplings. The capacitors are laid out in multiple units of 0.4pF or 0.5pF to improve matching.

During the test mode, the self-test circuit is connected to the coupling capacitors via bondwires shown in the upperleft side of the die in Fig. 6.17. In actual

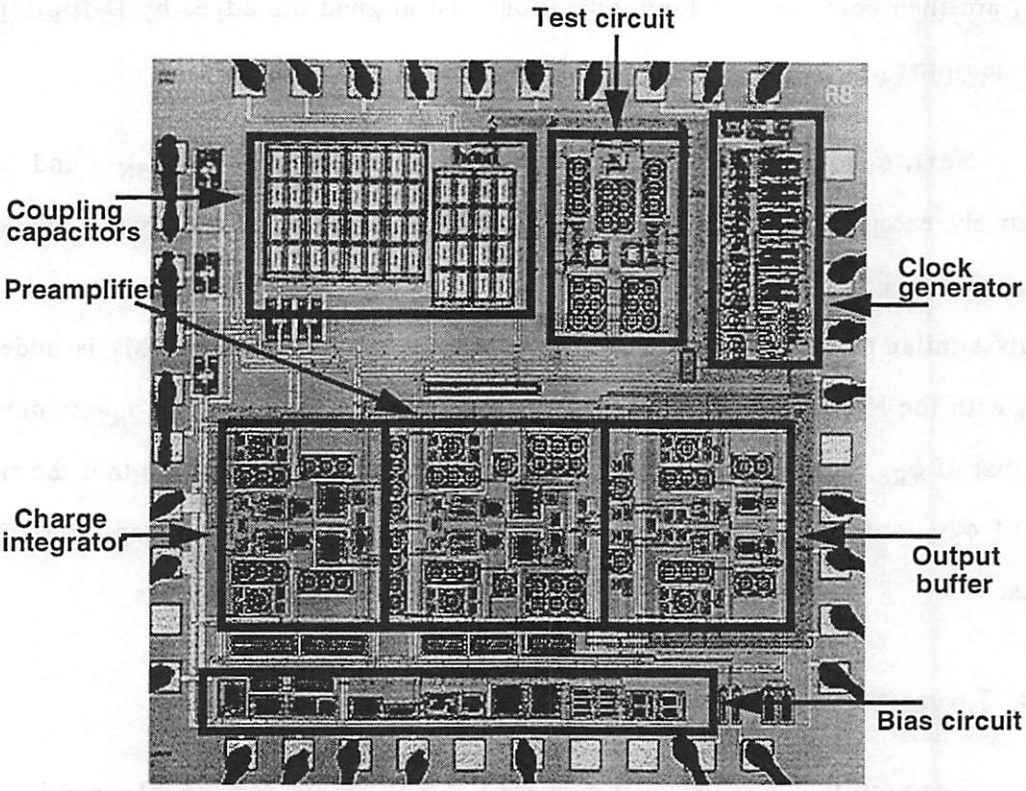


Fig. 6.17: Die photograph of the position sensing circuit

operations, these bondwires are broken to prevent the high-voltage drive of the micropositioner from damaging the test circuit.

6.4 High-voltage driving Circuit

The function of the driving circuit is to bias the two stators of the micropositioner with +40V and -40V bias voltages, to drive the rotor rail-to-rail with a bandwidth of at least 2kHz, and to provide a high-impedance output during the sensing phase of the position sensing circuit. Fig. 6.18 illustrates the schematics of the high-voltage driving circuit and its interface with the micropositioner and the position sensing circuit. The driving circuit consists of two stator bias circuits and a rotor driving circuit. All of which are designed from off-the-shelf components.

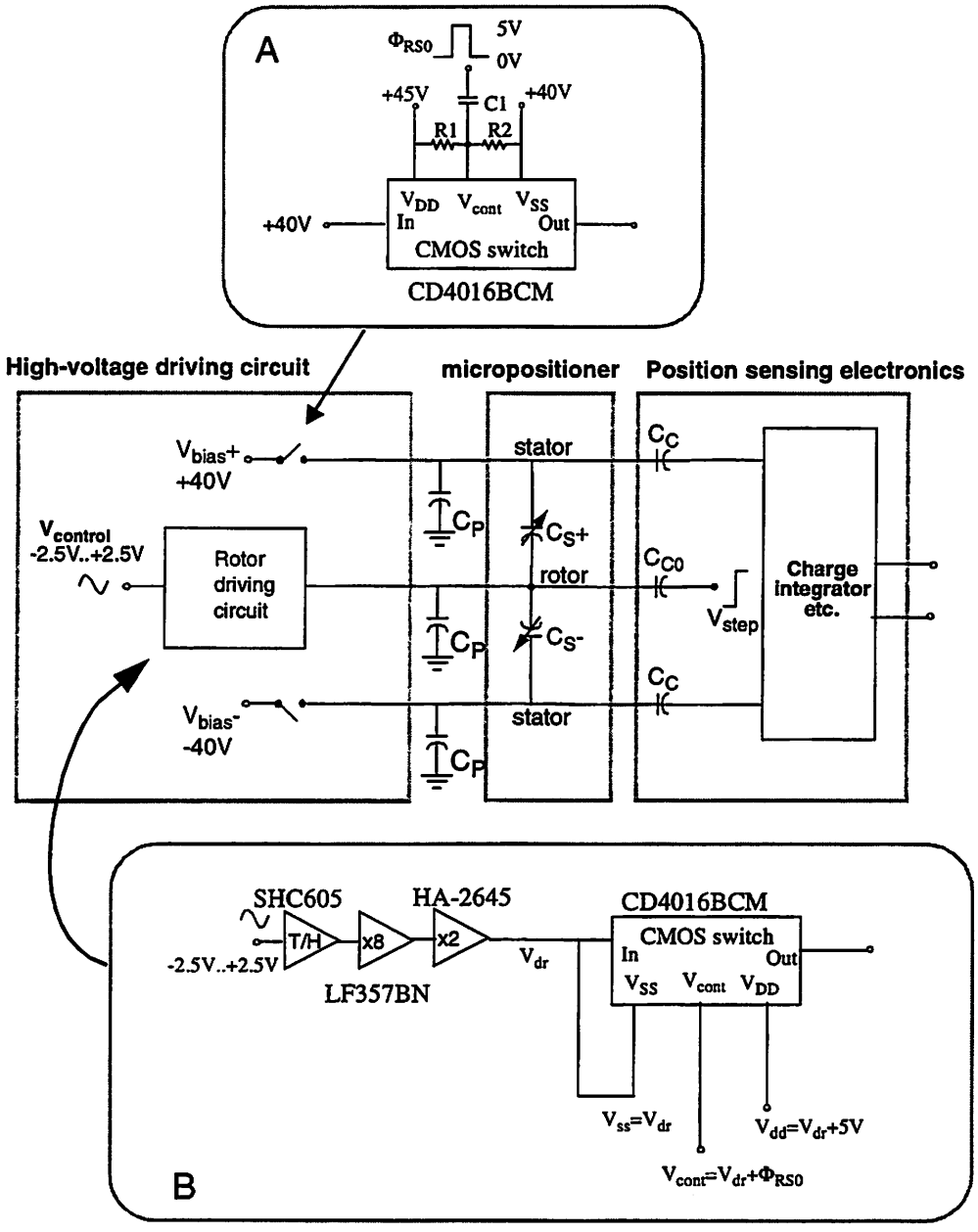


Fig. 6.18: Schematics of the micropositioner driving circuit

The driving circuit utilizes three switches at the stators and at the rotor to decouple itself from the rest of the circuit during the sensing phase, and is synchronized to the sensing circuit via clock ϕ_{RS0}. Clock ϕ_{RS0}, as shown in Fig. 6.5, is generated specifically for the driving circuit to ensure that any change in the voltage on the micropositioner electrodes occurs while the sensing circuit is reset. Since high-voltage

devices are normally slow and have large parasitics, floated and bootstrapped low-voltage devices are used throughout the driving circuit.

The stator bias circuit is shown in Inset A of Fig. 6.18. The high voltage biases are supplied from voltage regulators. The switch is a floated low-voltage CMOS switch. The gate is biased at approximately $0.4(V_{DD}-V_{SS})+V_{SS}$ using large resistors R_1 and R_2, and the control clock ϕ_{RS0} is AC-coupled to the gate via the capacitor C_1.

The rotor driving circuit is more complicated than the stator bias circuit because the rotor driving voltage can vary from V_{bias+} to V_{bias-}. Its implementation is shown in Inset B of Fig. 6.18. The ±2.5V input signal is amplified by a gain of 16 to achieve a maximum swing of ±40V. The track-and-hold further reduces couplings from the driving circuit into the sensing circuit by holding the voltage in the rotor circuit constant during the sensing period. The CMOS switch at the output is floated and bootstrapped by supply and gate voltages that track the rotor driving voltage, thus allowing the use of a low-voltage switch and eliminating any voltage-dependent capacitance of the switch.

6.5 Position Feedback Controller

Typical micropositioners exhibit very lightly damped resonance, implying that the operating bandwidth must be several times below the resonant frequency in order to achieve an acceptable setting performance [7]. A feedback loop as illustrated in Fig. 6.20 can be used to increase the micropositioner bandwidth and damping at the expense of DC gain. For a second-order system, the closed-loop DC gain and the natural frequency, which is approximately the bandwidth, are related to their open-loop values as

$$A_{cl}\omega^2_{n,cl} = A_{ol}\omega^2_{n,ol} \qquad \text{(Eq 6-4)}$$

Our strategy is to choose the loop gain to achieve the desired closed-loop bandwidth, then use phase-lead compensation to yield a desired phase margin. The micropositioner described in Section 6.2 has a DC gain of 0.1μm/V for bias voltages of ±40V, a natural frequency at 550Hz, and a damping factor of $9.1 \cdot 10^{-3}$ or a quality factor of 55. To achieve a closed-loop bandwidth of approximately one kilohertz, a loop gain of 1.8 is needed. Next, a lead compensator with a zero at 400Hz and a pole at 5.6kHz is chosen to achieve a 60-degree phase margin. The transfer function of the controller can then be written as

$$H(s) = \left(\frac{1.8}{16 \times 0.1\mu m/V \times \frac{dC}{dx} \times \frac{dv_o}{dC}} \right) \cdot \left(\frac{\frac{s}{2\pi(500)} + 1}{\frac{s}{2\pi(5600)} + 1} \right) \qquad \text{(Eq 6-5)}$$

where dC/dx is the capacitance variation as a function of the displacement of the micropositioner and dv_o/dC is the capacitance-to-voltage gain of the sensing circuit. This controller can be easily implemented using an operational amplifier, two resistors and two capacitors. Utilizing this controller in the feedback loop reduces the micropositioner DC gain to 0.035 μm/V, while increases the bandwidth and the damping factor to 1000Hz and 0.46, respectively.

6.6 Measurement Results

The measurement results are described in two parts. The first part focuses on the position sensing circuit, while the second one focuses on the closed-loop positioning system.

6.6.1 Sensing Electronics

By utilizing the self-test circuit described in Section 6.3.4, the position sensing circuit can be tested before assembly with the micropositioner and the high-

Table 6.4: Measurement results of the prototype position sensing circuit utilizing the self-test circuit.

Parameters	Measured values	Predicted values
Output offset voltage	-10mV	
Sensitivity $\left(\frac{V_o}{V_{t+}-V_{t-}}\right)$	59mV/V or 0.98mV/fC	64mV/V
Thermal noise floor	-123dBV/$\sqrt{Hz}$	-125dBV/$\sqrt{Hz}$
1/f noise corner	100Hz	100Hz
Total noise (1Hz-25kHz Band-width)	120μV	97μV
Total harmonic distortion (THD)	< -57dB	
Dynamic range	>64dB	76dB
Power consumption	26mW (26mW)	

voltage driving circuit in a five-volt environment. The measurement results are summarized in Table 6.4 with the output noise spectral density shown in Fig. 6.13.

From the measurements, all the bias voltages are within 10% of the designed values. The output offset of -10mV is contributed by mismatches of the capacitors in the self-test circuit, mismatches of the coupling capacitors and their parasitics, and the offset in the buffer amplifier. The measured sensitivity is 10% below the simulated values likely due to the variation in C_{T1} and C_{T2} which are used to generate the test charge (see Fig. 6.11). Fig. 6.19 shows the calculated and the measured noise spectrum, which are within 3dB of each other across the bandwidth. The drop in noise floor above 10kHz is due to the low-pass filtering of the output buffer. The 1/f noise corner at 100Hz is due to the 1/f noise from the output buffer. Without the correlated double sampling, the 1/f noise from the charge integrator would dominate the output noise spectrum with a 1/f noise corner around 1MHz. Total harmonic distortion is better than 57dB and is limited by the linearity of the signal generator. The measured dynamic range is 64dB, calculated from the maximum output of ±295mV produced by the self-

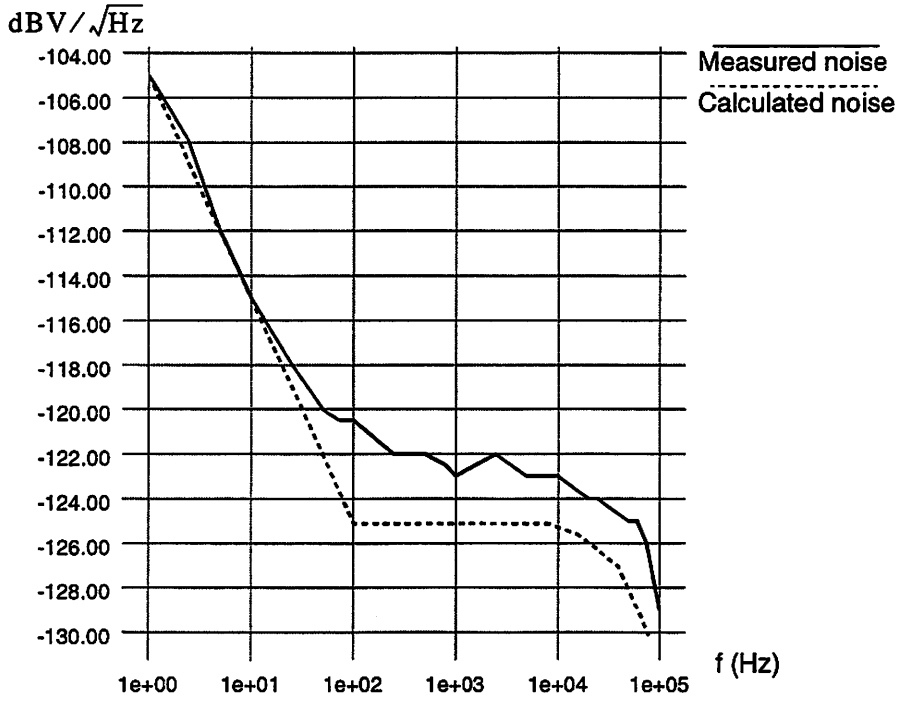


Fig. 6.19: Output noise spectral density of the prototype sensing circuit.

test circuit and the total noise in 25kHz bandwidth. Considering that the sensing circuit has a simulated output swing of ±1.2V, the dynamic range can potentially be as high as 76 dB.

This prototype confirms the kT/C noise cancellation by correlated double sampling. The measured thermal noise of -123dBV/$\sqrt{\text{Hz}}$, though higher than the predicted value of -125dBV/$\sqrt{\text{Hz}}$, is still 4dB lower than the combined kT/C and amplifier thermal noise of -119dBV/$\sqrt{\text{Hz}}$. For details in noise calculations, see Appendix 1.

6.6.2 Electrostatic Positioning System

In this part, a closed-loop electrostatic micropositioner is implemented and its response is compared to that of an open-loop micropositioner. The micropositioner and the electronics are assembled on a printed circuit board with the simplified schematics shown in Fig. 6.20.

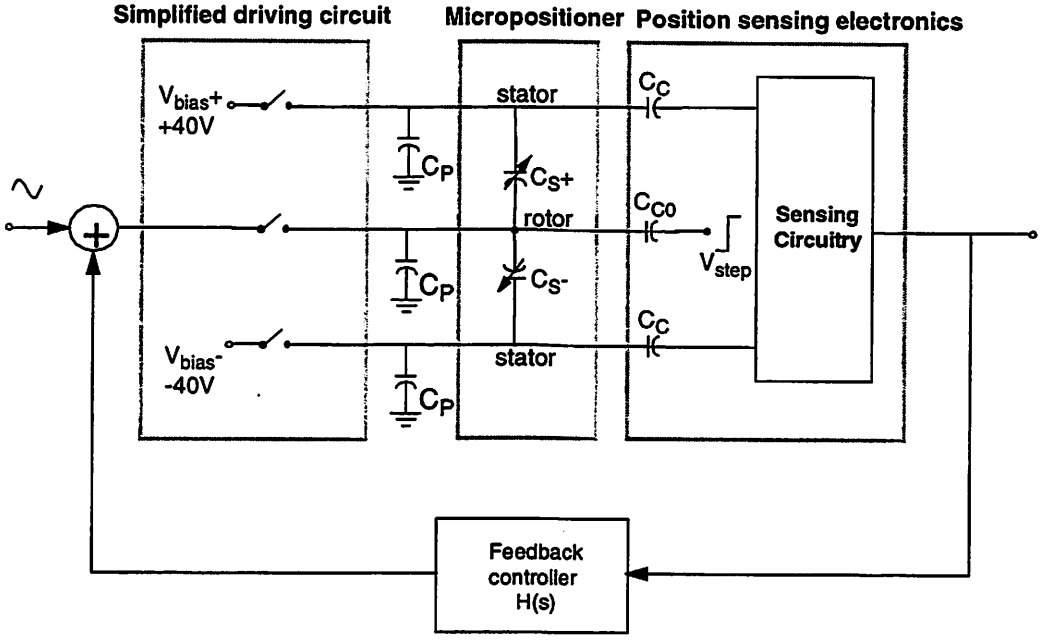


Fig. 6.20: The implementation of the closed-loop electrostatic micropositioner.

Preliminary measurements showed that parasitic capacitances of the testing board and the driving circuit are larger than anticipated and result in a capacitive-to-voltage gain which is approximately 3.5 times smaller than expected. To compensate for this signal attenuation, an external 9pF capacitor is added in parallel with the coupling capacitor C_{C0} as shown in Fig. 6.21. Additionally, a large offset in the order of 40mV caused by mismatches in C_{PS} and C_{SP} are reduced to about 10mV by adding a 500fF trimming capacitor in parallel with one of the C_{PS}.

The open-loop frequency response of the micropositioner measured by the position sensing circuit is shown in Figure 6.22. The peak at 550Hz illustrates the resonant frequency and a quality factor Q of approximately 55. By comparing the measurement to the reference measured by a laser doppler vibrometer (LDV) and use an estimated dC/dx of 68fF/μm for the micropositioner, the capacitance-to-voltage gain is calculated as 0.51mV/fF.

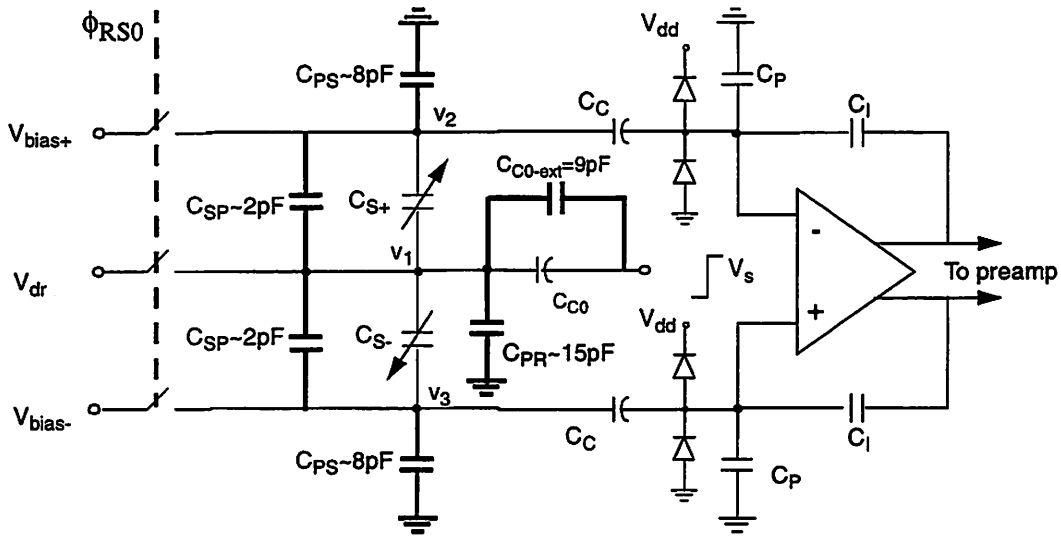


Fig. 6.21: An electrostatic positioning interface showing the off-chip parasitic capacitances and the additional coupling capacitor. The parasitics are approximated from measurement results using Eq. 3-16 to Eq. 3-19.

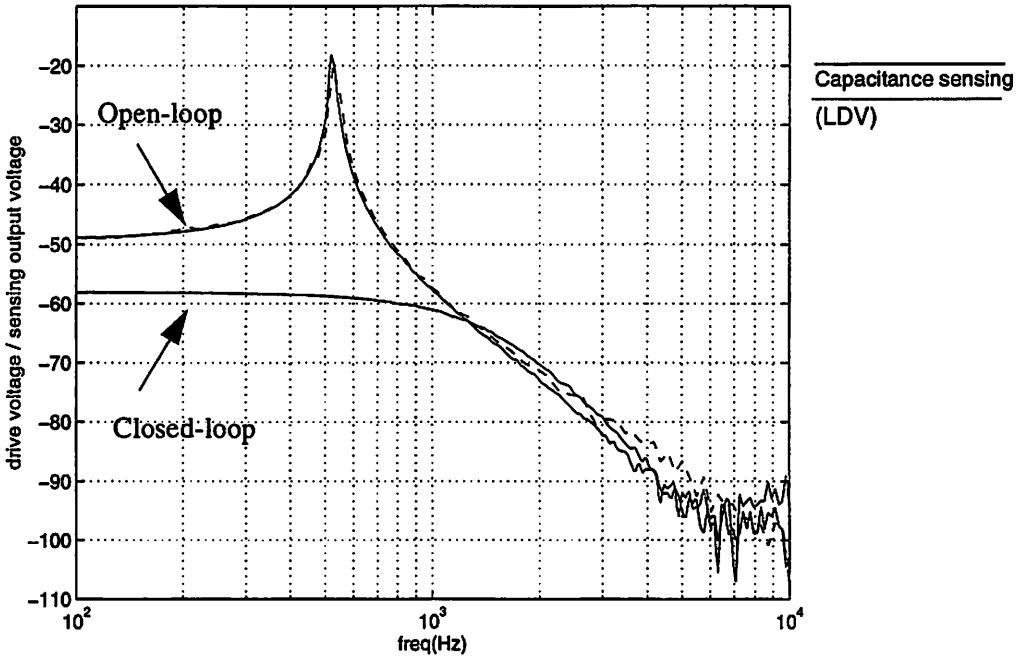


Fig. 6.22: Open- and closed-loop frequency response of the prototype micropositioner with a picoslider payload. The capacitive position measurement (solid line) is compared to the reference measured by an LDV (dashed line)

Feedthrough, or the coupling of the driving signal into the position sensing circuit can be seen as the deviation from the reference at the low signal level at high frequencies. Feedthrough was further investigated by replacing the micropositioner with fixed capacitors. Measurements show that the magnitude of the feedthrough transfer function increases with frequency, but remains relatively constant with amplitude for driving voltages V_{dr} smaller than ±10V. For V_{dr}<±10V, the magnitude of the feedthrough transfer function remains below –90dB, or approximately 40dB smaller than the position signal at low frequencies. For larger driving voltages, feedthrough increases rapidly likely due to the slewing and incomplete settling in the rotor driving circuit. Since the position error due to feedthrough for a driving voltage of ±10V is approximately 10nm, the prototype position sensing system achieves the required 10nm resolution only for driving voltages smaller than ±10V. In comparison, the position resolution due to the electronic noise is 3.4nm in 25kHz bandwidth. Therefore, feedthrough is the factor limiting the position resolution and the maximum driving voltage.

Figure 6.22 also shows the closed-loop frequency response of the micropositioner. With the use of the phase-lead controller, the micropositioner DC gain decreases from 0.1μm/V to 0.035μm/V, while the -3dB bandwidth increases from 780Hz to 1000Hz, and the damping factor increases from 0.009 to one. Fig. 6.23 shows the response of the micropositioner to a 100Hz ±6.4V square-wave input. The micropositioner settles to 10nm or 2% within 0.7msec. Without the feedback loop, the micropositioner exhibits excessive ringing behavior as shown in Fig. 6.24 and requires approximately 120msec to settle.

Table 6.5 summarizes the measured results of this electrostatic positioning system.

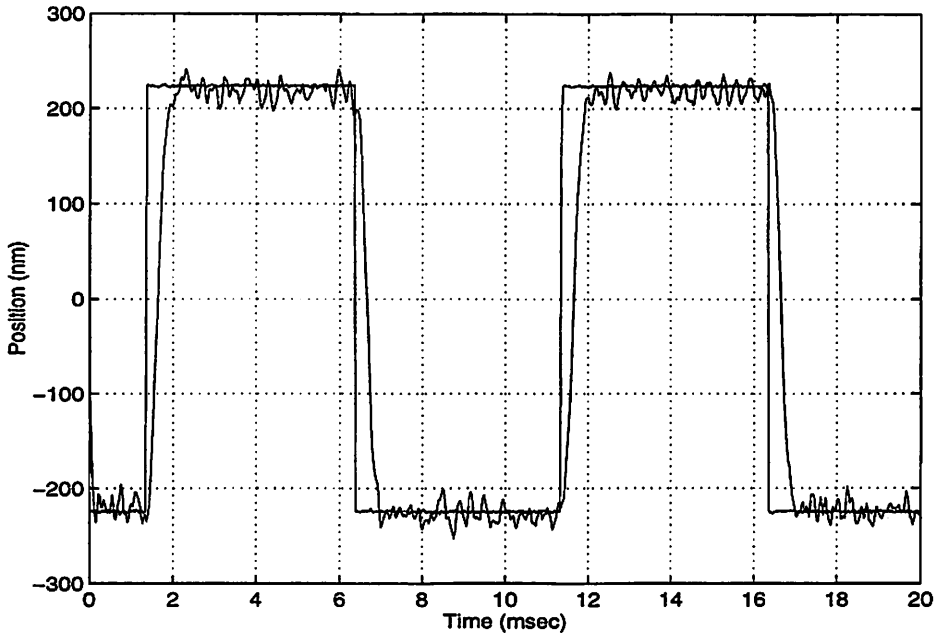


Fig. 6.23: A closed-loop step response of the micropositioner to a 100Hz ±6.4V square-wave input. The micropositioner settles to 10nm in 0.7msec.

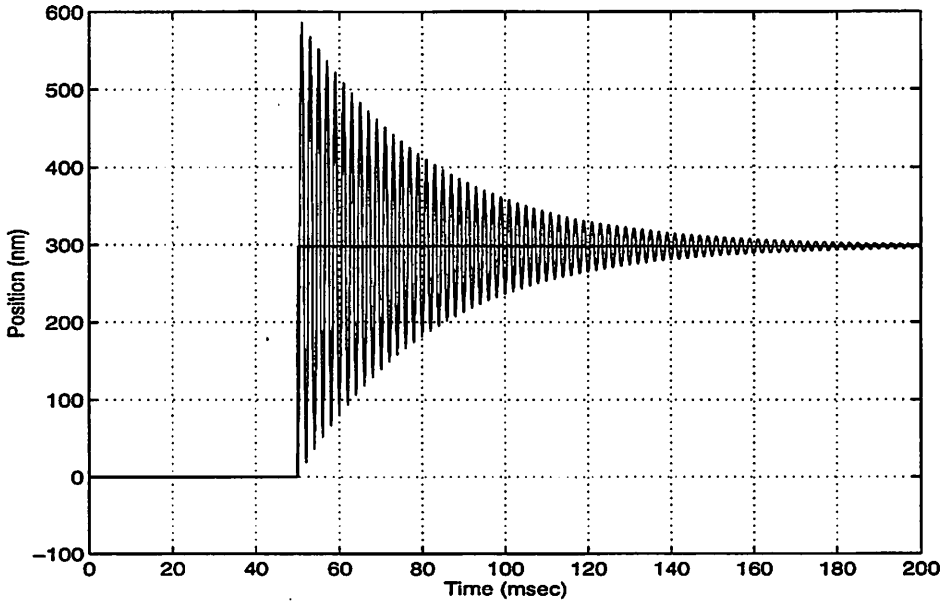


Fig. 6.24: An open-loop response of the micropositioner to a 3V step input. This plot is obtained from a simulation rather than the measurement because of the very long acquisition time.

Table 6.5: Specifications of the electrostatic positioning system.

Parameters	Measured results		Design goals
	Open-loop	Closed-loop	
Stator bias voltage	±40V		±40V
dx/dV_{dr}	0.1μm/V	0.35μm/V	
Bandwidth	780Hz	1000Hz	1000Hz
Damping factor	0.009	1.0	
Settling time (2%)	120ms	0.7ms	
Maximum driving voltage (limited by feedthrough)	±10V		±40V
Maximum displacement	±1μm	±0.35μm	±1μm
Maximum force	20μN	~20μN	80μN
Position readout sensitivity (dv_o/dx)	35mV/μm 0.51mV/fF		~50mV/μm
Offset	~10mV ~0.29μm		
Position accuracy (limited by feedthrough)	10nm		10nm
Noise floor	0.19Angstrom/ $\sqrt{Hz}$ 1.28aF/$\sqrt{Hz}$		
1/f noise corner	100Hz		
Noise floor in 25kHz bandwidth (1Hz - 25kHz)	3.4nm 0.23fF		

6.7 Summary

In this chapter, we have described a prototype implementation and experimental verification of a closed-loop electrostatic positioning system. The system consists of a micropositioner, a capacitive position sensing circuit, a high-voltage driving circuit, and a feedback controller.

The prototype position sensing circuit, which is the main focus of this research, is a switched-capacitor sensing circuit. The circuit utilizes pseudo-differential topology, correlated double sampling, high-voltage shielding capacitors, frequency separation technique, and the time-division concept; all of which were discussed previously in this document. The circuit was fabricated in a 1.2-μm CMOS process, has a die area of $2.2x2.2mm^2$, and dissipates 26mW from a five-volt supply. The high-voltage driving circuit employs coupling switches to decouple itself from the micropositioner and the sensing circuit during the sensing phase. Floated or bootstrapped low-voltage components are used in the driving circuit to avoid large parasitics of high-voltage devices and to avoid modulating voltage-dependent junction capacitance. The feedback controller utilizes a simple lead filter to increase the bandwidth and the damping factor of the micropositioner.

The prototype electrostatic positioning system has a position sensitivity of 35mV/μm, an offset of approximately 10mV, a thermal noise floor of 0.19Angstrom/$\sqrt{Hz}$ or approximately 3.4nm in 25kHz bandwidth, and a feedthrough-limited resolution of 10nm for driving voltages smaller than ±10V. With the feedback loop, the bandwidth of the micropositioner increases from 780Hz to 1000Hz and the damping factor increases from 0.009 to one. The result is a reduction in settling time from 120msec to 0.7msec. Because the driving voltage is limited to ±10V by feedthrough, the maximum placement and the maximum force are approximately four times smaller than the design goals.

Offset and signal attenuation due to off-chip parasitics and feedthrough remain to be solved in future research. These two issues will be further discussed in Section 7.2.

Chapter 7

Conclusions

7.1 Results

This research investigates the design of capacitive position sensing circuits for electrostatic micropositioners and demonstrates the use of feedback loops to improve the dynamics of micropositioners. An experimental closed-loop electrostatic micropositioner achieves a bandwidth of 1.0kHz, a 2% settling time of 0.7msec, a feedthrough-limited resolution of 10nm, a maximum displacement of ±0.35μm, and a position measurement sensitivity of 35mV/μm.

The contributions of this research maybe divided into two areas: fundamental limitations of capacitive position sensing and the integration of electrostatic actuation and capacitive position sensing. In the first area, The fundamental resolution imposed by the amplifier thermal noise is studied. Circuits techniques that enable the sensing circuit to potentially achieve the fundamental resolution are presented. Pseudo-differential topology allows the use of fully-differential electronics, thus improving the coupling noise, power-supply, and feedthrough rejection. Correlated double sampling (CDS), which has traditionally been used to remove the amplifier offset and attenuate the 1/f noise, is extended to cancel the switch charge injection and kT/C noise due to

switching operations. Analyses suggest that the combination of the kT/C noise cancellation and the amplifier thermal noise optimization reduces the thermal noise in the sensing circuit by as much as 20dB. The concept of kT/C noise cancellation is verified by the prototype position sensing circuit.

In the area of system integration, this research focuses on utilizing a single set of electrodes for both electrostatic actuation and capacitive position sensing. The sharing of electrodes enables the use of micropositioners with only one set of electrodes, thus simplifying the fabrication process by requiring only one structural layer. On the other hand, the electronics becomes more complicated because the high voltage drive of the micropositioner and the precision low-voltage sensing signal are superimposed on each other. To allow the position sensing circuit to be fabricated in a low-cost conventional CMOS process, on-chip coupling capacitors are proposed as the means to shield the sensing circuitry from the high-voltage drive. Issues related to the interface—namely the sensing charge leakage, feedthrough, voltage-dependent capacitance at the rotor node, sense-force error, and gain variations and offsets due to coupling capacitors and off-chip parasitics—are investigated. Among these issues, feedthrough, or the spurious coupling of the driving signal into the sensing signal, is the most critical one because the driving signals are often four to five orders of magnitude larger than the position signals. Ideally, feedthrough can be eliminated by utilizing coupling switches to isolate the driving and the sensing circuits during the sensing period. In practice, nonidealities contribute to feedthrough which cannot be removed by this technique. Techniques to further reduce the feedthrough includes frequency division, correlated triple sampling, chopper stabilization, and post cancellation.

The concepts and techniques presented in this document are utilized in the implementation of a closed-loop electrostatic micropositioner. Measurement results demonstrate that the position accuracy is limited by the gain reduction and offset due to

off-chip parasitics and feedthrough. In addition, feedthrough limits the dynamic range of the system by restricting the maximum driving voltage, and thus the maximum displacement and actuation force.

7.2 Future work

To improve the position accuracy and the dynamic range, the following techniques should be incorporates in future implementations of closed-loop electrostatic micropositioners.

a) Higher-Level of Integration

Capacitive position sensing is not suitable for PCB-level integration because large and mismatched off-chip parasitic capacitance, as described in Section 5.6, attenuates the position sensing gain and produces large offsets. This is verified in the current implementation where an additional coupling capacitor is required to compensation the gain attenuation and a trimming capacitor is needed to reduce the offset. To mitigate these problems, the high-voltage driving circuit should be implemented monolithically. Furthermore, assembly techniques which minimize parasitics such as flip-chip bonding and chip-on-board are needed for the integration of the micropositioner, the driving circuit, and the sensing circuit.

b) Correlated triple sampling and chopper stabilization

In the current implementation of the closed-loop electrostatic micropositioner, the rise in feedthrough at driving voltages larger than ±10V is likely due to the slewing and incomplete settling of the amplifier driving the rotor switch. At lower driving voltages, other nonidealities such as coupling switch leakage, voltage-dependent capacitance at the rotor node, and substrate coupling possibly contribute to the feedthrough. To solve the feedthrough problem, capacitive position sensing circuits that

are more immuned to feedthrough are needed. This can be achieved by utilizing correlated triple sampling (CTS) or chopper stabilization. As described in Section 5.3, correlated triple sampling attenuates feedthrough with a shaping function similar to that of the 1/f noise in correlated double sampling. Chopper stabilization, on other hand, modulates feedthrough up to $f_s/2$, thus allowing the feedthrough to be attenuated by a low-pass filter. These two techniques are very attractive because they can be realized with a minimal increase in hardware complexity.

Appendix 1

Noise in Switched-Capacitor Sensing Circuits

Thermal noise of the switched-capacitor sensing circuit shown in Fig. A1-1 consists of the sampling noise of switch S1 or the kT/C noise and the amplifier thermal noise sampled by the load capacitance. The operation of this circuit, which is often called a charge integrator, can be explained as followings. During the reset phase, all the capacitors and the amplifier are reset to ground or a reference. At the end of the reset phase, the switch S_1 at the input of the amplifier opens first. Next, the switches S_2 and S_3 are opened at the end of phase ϕ_{RSI}. This switch opening sequence, called bottom-plate sampling, eliminates signal-dependent charge injection from the switches. During the sensing phase, one plate of the sense capacitor is connected to the sensing voltage. The charge $Q=C_S V_S$ then flows into the integrating capacitor C_I and results in an output voltage $V_o=C_S V_S/C_I$.

A. kT/C Noise

According to Fig. A1-1b when the switch S_1 opens, switch sampling noise at the amplifier summing node is equal to

$$\overline{v^2_{\frac{kT}{C},\,input}} = \frac{kT}{C_T} \qquad \text{where } C_T = C_S + C_I + C_P + C_{IP} \qquad \text{(Eq A1-1)}$$

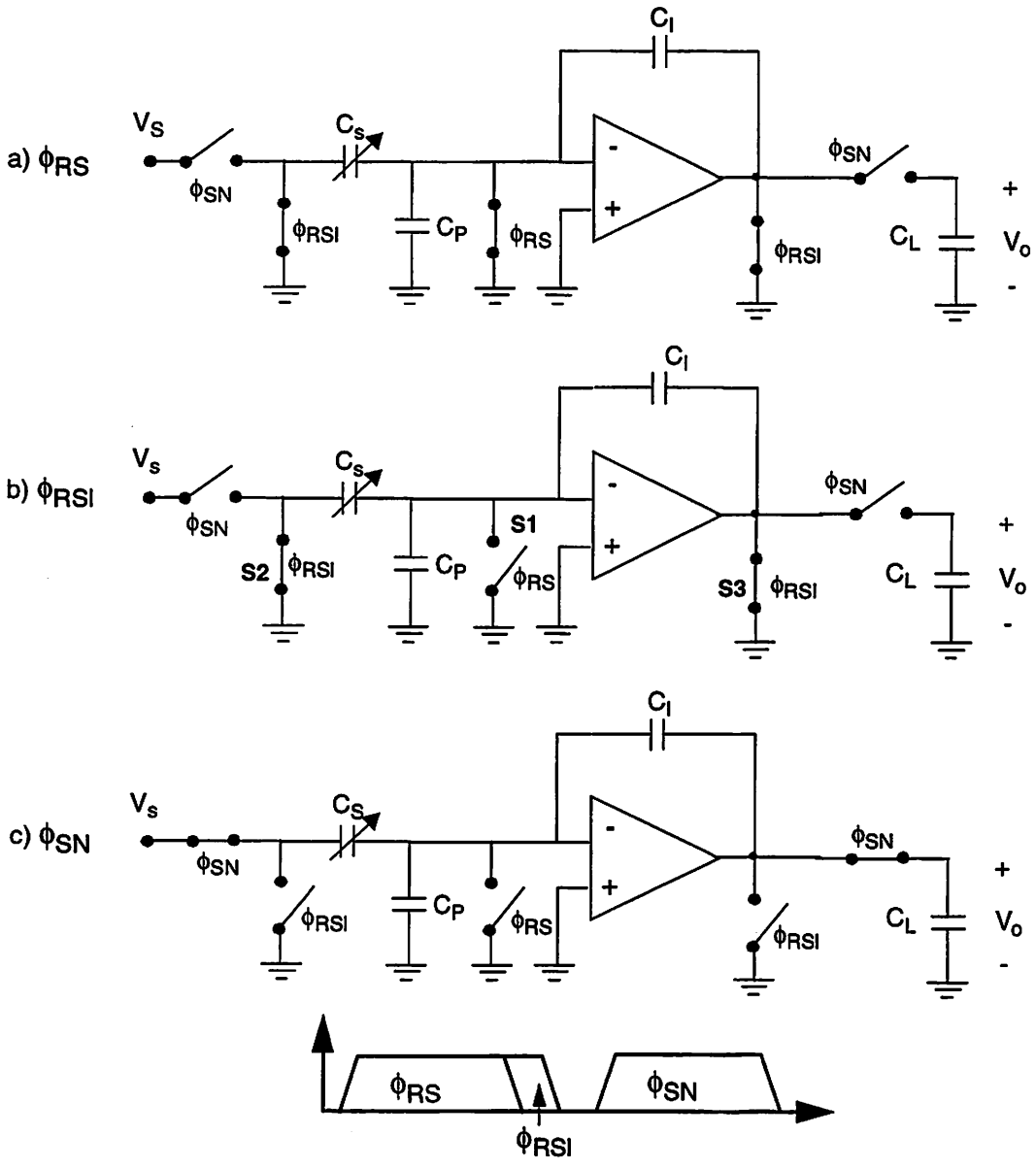


Fig. A1-1: A switched-capacitor sensing circuit and its switching operations.

where C_{IP} is the amplifier input capacitance. The kT/C is referred to the output by multiplying with the feedback factor, $f=C_I/C_T$, of the amplifier

$$\overline{v_{\frac{kT}{C}}^2} = \frac{1}{f^2} \cdot \frac{kT}{C_T} = \left(\frac{C_T}{C_I}\right)^2 \frac{kT}{C_T}. \qquad \text{(Eq A1-2)}$$

For fully-differential circuits, kT/C noise doubles due to the switches in the differential signal paths.

B. Amplifier Thermal Noise

In this section, we will derive the amplifier thermal noise and show that it can be written in the form of $\gamma \cdot kT/C_L$ where γ is a modification factor and C_L is the load capacitance of the amplifier.

Two assumptions will be used in the following noise calculation. First, the noise contributions from switches S_2 and S_3 are negligible. This assumption is valid when the bandwidths of the switches are much larger than the amplifier closed-loop bandwidth. Second, the amplifier is a single-stage type such as a folded cascode or a telescopic amplifier. Single-stage amplifiers are typical in switched-capacitor circuits because of their high speed and simplicity.

The total output-referred noise of the amplifier can be calculated by multiplying the amplifier input-referred noise with the inverse square of the feedback factor and integrating over the whole bandwidth.

$$\overline{v_{opamp}^2} = \int_0^\infty \frac{1}{f^2} \cdot \overline{v_n^2} df \quad . \qquad \text{(Eq A1-3)}$$

For a single-pole amplifier, the equivalent noise bandwidth is equal to $\pi/2$ times the amplifier bandwidth [33]. Therefore, Eq. A1-3 becomes

$$\overline{v_o^2} = \frac{1}{f^2} \cdot \overline{v_n^2} \cdot f_u \cdot \frac{\pi}{2} \qquad \text{(Eq A1-4)}$$

where f_u is the closed-loop bandwidth of the amplifier. For a single-stage amplifier, the closed-loop bandwidth f_u is

$$f_u = \frac{1}{2\pi}\frac{g_m f}{C_{LT}} = \frac{1}{2\pi}\frac{g_m f}{C_L + \frac{C_I(C_S + C_P + C_{IP})}{C_T}} = \frac{1}{2\pi}\frac{g_m}{\frac{C_L}{f} + (C_S + C_P + C_{IP})} \qquad \text{(Eq A1-5)}$$

where C_{LT} is the total capacitance at the amplifier output node and $C_T=C_S+C_I+C_P+C_{IP}$ is the total capacitance at the amplifier input node.

The input-referred thermal noise $\overline{v_n^2}$ of the amplifier is

$$\overline{v_n^2} = 4kT\frac{2}{3g_m}\cdot n \qquad \text{(Eq A1-6)}$$

where g_m is the transconductance of the input transistor and n is the ratio of the total amplifier noise to the input transistor noise.

Substituting f_u, the amplifier input-referred thermal noise, and the feedback factor in Eq. A1-4 yields

$$\overline{v_o^2} = \left(\frac{C_T}{C_I}\right)^2 \cdot \frac{\frac{2}{3}kTn}{\frac{C_L}{f} + (C_S + C_P + C_{IP})} \qquad \text{(Eq A1-7)}$$

$$= \left(\frac{C_T}{C_I}\right)^2 \cdot \frac{\frac{2}{3}kTn}{\frac{C_L C_T}{C_I} + (C_T - C_I)}. \qquad \text{(Eq A1-8)}$$

In sensing circuits for micromachined applications, C_I is typically in the same order as C_S and usually much smaller than C_T and C_L. Therefore, Eq. A1-8 can be approximated as

$$\overline{v_o^2} \approx \left(\frac{C_T}{C_I}\right)^2 \cdot \frac{\frac{2}{3}kTn}{\frac{C_L C_T}{C_I}} \qquad \text{(Eq A1-9)}$$

$$= \left(\frac{2}{3}n\frac{C_T}{C_I}\right)\cdot\frac{kT}{C_L} = \gamma\cdot\frac{kT}{C_L} \qquad \text{(Eq A1-10)}$$

where

$$\gamma = \frac{2}{3}n\frac{C_T}{C_I} = \frac{2n}{3f}. \qquad \text{(Eq A1-11)}$$

For an ideal case of one-transistor amplifier and a feedback factor of one, γ is equal to 2/3. This implies that, ideally, the amplifier thermal noise sampled by the load capacitance can be smaller than the conventional kT/C noise of a capacitor and a switch. In practice, γ ranges from two to ten.

C. Thermal Noise in the Prototype Position Sensing Circuit

In this section, we will calculate the output-referred thermal noise of the prototype sensing circuit. In this calculation, noise of the buffer is neglected because it is much smaller than noise of the first two stages.

The output-referred amplifier thermal noise of the charge integrator and the preamplifier is

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \left(\frac{1}{f^2}\cdot\frac{\overline{v_n^2}}{\Delta f}\cdot A_{pre}^2 + \frac{1}{f^2}\cdot\frac{\overline{v_n^2}}{\Delta f}\right)\cdot A_{CDS}^2\cdot\frac{f_u}{f_s}\cdot\frac{\pi}{2}\cdot 2 \qquad \text{(Eq A1-12)}$$

where $\overline{v_n^2}$ is the input-referred amplifier thermal noise, f is the feedback factor, A_{pre} is the preamplifier gain, A_{CDS} is the voltage transfer ratio of the error-storage capacitor C_H, f_u the closed-loop bandwidth, f_s is the sensing frequency, and the factor of two is due to the double sampling of CDS. As described in Section 6.3.2, both stages utilizes identical amplifiers and have the same feedback factors and closed-loop bandwidths.

Substituting the appropriate values into Eq. A1-12 yields

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \left(\frac{1}{7^2}\cdot 16\times 10^{-18}\cdot 5^2 + \frac{1}{7^2}\cdot 16\times 10^{-18}\right)\cdot 0.8^2\cdot 7.1\cdot\frac{\pi}{2}\cdot 2 \qquad \text{(Eq A1-13)}$$

$$\sqrt{\frac{\overline{v_{opamp}^2}}{\Delta f}} = 571\text{nV}/\sqrt{\text{Hz}} = -125\text{dBV}/\sqrt{\text{Hz}} \qquad \text{(Eq A1-14)}$$

In comparison, the output-referred kT/C noise of both stages, if not cancelled by the correlated double sampling, is equal to

$$\frac{\overline{v_{kT/C}^2}}{\Delta f} = \left(\frac{1}{f^2}\cdot\frac{kT}{C_T}\cdot A_{pre}^2 + \frac{1}{f^2}\cdot\frac{kT}{C_T}\right)\cdot A_{CDS}^2\cdot\frac{1}{f_s}\cdot 2 \qquad \text{(Eq A1-15)}$$

$$= \left(\frac{1}{7^2}\cdot\frac{kT}{8.4\text{pF}}\cdot 5^2 + \frac{1}{7^2}\cdot\frac{kT}{2.8\text{pF}}\right)\cdot 0.8^2\cdot\frac{1}{10^6}\cdot 2 \qquad \text{(Eq A1-16)}$$

$$\sqrt{\frac{\overline{v_{kT/C}^2}}{\Delta f}} = 993\text{nV}/\sqrt{\text{Hz}} = -120\text{dBV}/\sqrt{\text{Hz}} \qquad \text{(Eq A1-17)}$$

Combining the amplifier thermal noise from Eq. A1-14 with the kT/C noise from Eq. A1-17 yields the total noise,

$$\sqrt{\frac{\overline{v_{kT/C}^2}}{\Delta f} + \frac{\overline{v_{opamp}^2}}{\Delta f}} = 1.15\mu V/\sqrt{Hz} = -119dBV/\sqrt{Hz}. \qquad \text{(Eq A1-18)}$$

Subtracting Eq. A1-14 from Eq. A1-18 yields a noise improvement of 6dB due to the kT/C noise cancellation of correlated double sampling.

According to the measurements shown in Section 6.6.1, the output noise of the prototype sensing circuit is $-123\,dBV/\sqrt{Hz}$, 2dB higher than the calculated value, but still 4dB lower than the total noise given in Eq. A1-18. Therefore, the concept of using correlated double sampling to cancel kT/C noise is verified.

Appendix 2

Transfer Function of Pseudo-Differential Circuits

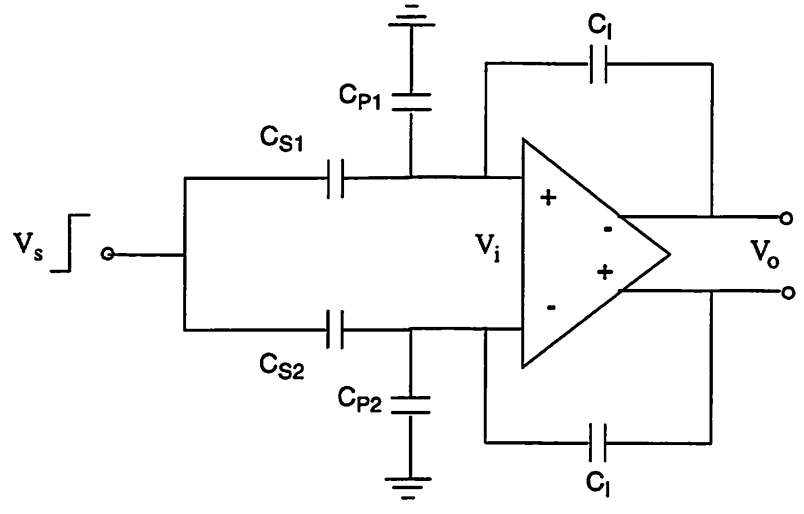


Fig. A2-1: A capacitance sensing circuit with pseudo-differential topology.

This appendix derives the transfer function of a capacitance sensing circuit with pseudo-differential topology as shown in Fig. A2-1. A few assumptions and notations are stated below:

- The amplifier has high gain; therefore, the input differential voltage ($V_{i\text{-}diff}$) is equal to zero.

- The output common-mode level is monitored and restored to the correct level by an output common-mode feedback (CMFB) circuit.
- $C_{S1}=C_S+\Delta C_S/2$, $C_{S2}=C_S-\Delta C_S/2$, $C_{P1}=C_P+\Delta C_P/2$, $C_{P2}=C_P-\Delta C_P/2$.

Before deriving the transfer function, we will qualitatively discuss the change in the input and output common-mode level. Initially, after the sensing voltage V_S is applied, the input and output common-mode level are shifted by the respective capacitive dividing ratios. The output common-mode level is then restored to the correct level by the CMFB circuit; in the process, the input common-mode level is shifted again to the final level. The transfer function can be calculated once the final input common-mode level is known.

Initially, the step sensing voltage V_S causes the amplifier input common-mode level to shift by

$$V_{icm\text{-}ini} = \alpha \cdot V_s \qquad ; \alpha = \frac{C_S}{C_S + C_P + C_{IP} + \frac{C_I C_L}{C_I + C_L}} . \qquad \text{(Eq A2-1)}$$

The initial input common-mode shift results in the output common-mode shift of

$$V_{ocm\text{-}ini} = \beta \cdot V_{icm\text{-}ini} \qquad ; \beta = \frac{C_I}{C_I + C_L} . \qquad \text{(Eq A2-2)}$$

The CMFB circuit then restores the output-common mode to the correct level, thus resulting in the final input common-mode of

$$V_{icm\text{-}final} = V_{icm\text{-}ini} - \gamma \cdot V_{ocm\text{-}ini} \qquad ; \gamma = \frac{C_I}{C_I + C_S + C_P + C_{IP}} = \frac{C_I}{C_T} \qquad \text{(Eq A2-3)}$$

$$= \alpha(1 - \beta\gamma) \cdot V_s \qquad \text{(Eq A2-4)}$$

$$= \delta \cdot V_s \qquad ; \delta = \alpha(1 - \beta\gamma) < 1 . \qquad \text{(Eq A2-5)}$$

Using the charge conservation principle, the transfer function can be calculated as follows

$$V_{od} = \frac{1}{C_I}((\Delta Q_{C_{S2}} - \Delta Q_{C_{S1}}) + (\Delta Q_{C_{P1}} - \Delta Q_{C_{P2}})) \quad \text{(Eq A2-6)}$$

$$= \frac{1}{C_I}\{(V_s - V_{icm\text{-}final}) \cdot (C_{S2} - C_{S1}) + V_{icm\text{-}final} \cdot (C_{P1} - C_{P2})\} \quad \text{(Eq A2-7)}$$

$$= \{-\Delta C_S \cdot (1 - \delta) + \Delta C_P \cdot \delta\} \cdot \frac{V_s}{C_I} \quad \text{(Eq A2-8)}$$

For C_I much smaller than C_L and C_T,

$$\delta \approx \frac{C_S}{C_T} \quad \text{(Eq A2-9)}$$

where C_S/C_T is typically in the order of one-twentieth to one-fifth. In comparison, the transfer function of a single-ended circuit as shown in Section 3.2 has δ equal to zero. Eq. A2-8 indicates that the capacitance-to-voltage gain of a pseudo-differential circuit becomes a function of the parasitics. Additionally, the mismatch in parasitics C_P causes an offset voltage as a result of the loss of virtual ground condition at the amplifier summing nodes. These two drawbacks of pseudo-differential circuit are eliminated to the first order by using an input common-mode feedback circuit, as discussed in Section 3.3.

Appendix 3

Micropositioner with Two Sets of Stators

A micropositioner with two sets of stators for sensing and driving [34], if permitted by the fabrication process, is attractive because it helps reduce signal attenuation and offset, and potentially feedthrough. In contrast to common beliefs, splitting the stator electrodes into two sets reduces the realizable force by only a small amount because only a small number of electrodes need to be allocated for the position sensing. This is because a micropositioner with two sets of stators, as shown in Fig. A3.1, eliminates the need for coupling capacitors and potentially yields a factor of ten or more increase in the capacitance-to-voltage gain; hence, only a small number of the total electrodes have to be allocated for the sensing operation in order to achieve a similar resolution.

In Fig. A3.1a, a micropositioner with two sets of stators allows the coupling capacitors C_C and the high voltage switches at the stators to be removed. With the removal of C_C, the parasitics C_{PS}, which are now connected to the virtual ground nodes at the amplifier inputs, no longer contributes to the signal attenuation or offset. Additionally, by increasing the stator bias voltages, it is possible to limit the rotor driving voltage V_{dr} to within the supply range of the sensing electronics. This permits the rotor driving circuit to be fabricated in a conventional process along with the

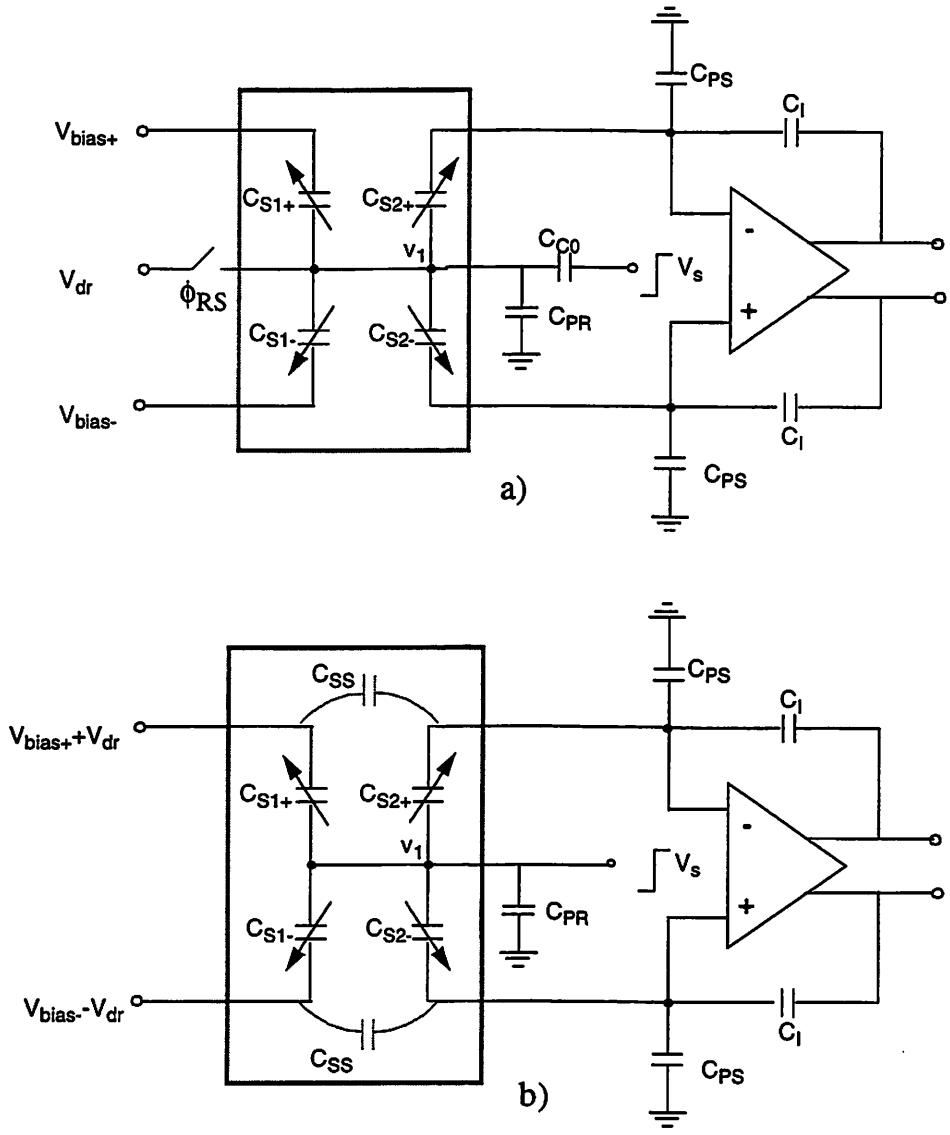


Fig. A3.1: Two sensing and driving configurations for micropositioners with two sets of stators.

sensing circuit and further simplifies the high-voltage driving circuit to only generating two constant stator bias voltages, V_{bias+} and V_{bias-} [35].

In Fig. A3.1b, a rearrangement of the stator driving voltages permits all the coupling capacitors to be eliminated. The expense is an increase in complexity of the driving circuit. With the elimination of all coupling capacitors, the parasitics C_{PS} and

C_{PR} no longer contribute any signal attenuation or offset. Feedthrough is potentially reduced because the driving and the sensing signal paths are almost separated, except for the parasitic coupling such as C_{SS} shown in Fig. A3.1.

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