MICROELECTROMECHANICAL DEVICES AND FABRICATION TECHNOLOGIES FOR RADIO-FREQUENCY ANALOG SIGNAL PROCESSING

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Darrin Jun Young

Memorandum No. UCB/ERL M99/24

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

MicroElectroMechanical Devices and Fabrication Technologies for Radio-Frequency Analog Signal Processing

by

Darrin Jun Young

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Committee in charge:

Professor Bernhard E. Boser

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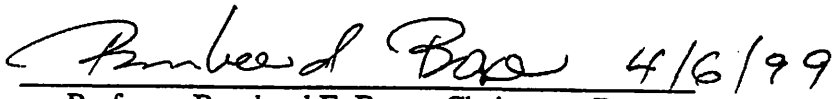
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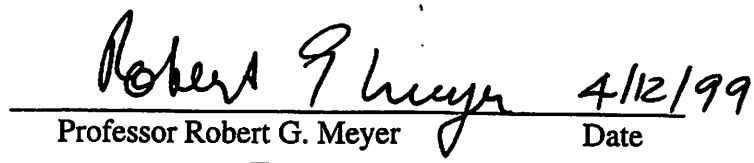
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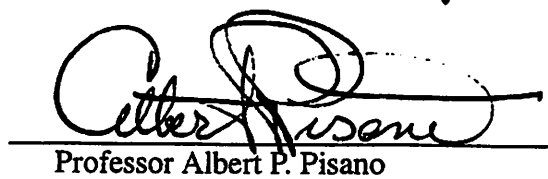
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Professor Albert P. Pisano Date

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1999

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Abstract

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Professor Benhard E. Boser, Chair

The proliferation of wireless services creates a pressing need for compact and low cost RF transceivers. Modern sub-micron technologies provide the active components needed for miniaturization but fail to deliver high quality passives needed in oscillators and filters. This dissertation demonstrates procedures for adding high quality inductors and tunable capacitors to a standard silicon integrated circuits. Several voltage-controlled oscillators operating in the low Giga-Hertz range demonstrate the suitability of these components for high performance RF building blocks.

Two low-temperature processes are described to add inductors and capacitors to silicon ICs. A 3-D coil geometry is used for the inductors rather than the conventional planar spiral to substantially reduce substrate loss and

hence improve the quality factor and self-resonant frequency. Measured Q-factors at 1 GHz are 30 for a 4.8 nH device, 16 for 8.2 nH and 13.8 nH inductors. Several enhancements are proposed that are expected to result in a further improvement of the achievable Q-factor.

This research investigates the design and fabrication of silicon-based IC-compatible high-Q tunable capacitors and inductors. The goal of this investigation is to develop a monolithic low phase noise radio-frequency voltage-controlled oscillator using these high-performance passive components for wireless communication applications. Monolithic VCOs will help the miniaturization of current radio transceivers, which offers a potential solution to achieve a single hand-held wireless phone with multistandard capabilities.

IC-compatible micromachining fabrication technologies have been developed to realize on-chip high-Q RF tunable capacitors and 3-D coil inductors. The capacitors achieve a nominal capacitance value of 2 pF and can be tuned over 15 % with 3 V. A quality factor over 60 has been measured at 1 GHz. 3-D coil inductors obtain values of 4.8 nH, 8.2 nH and 13.8 nH. At 1 GHz a Q factor of 30 has been achieved for a 4.8 nH device and a Q of 16 for 8.2 nH and 13.8 nH inductors.

A prototype RF voltage-controlled oscillator has been implemented employing the micromachined tunable capacitors and a 8.2 nH 3-D coil inductor. The active electronics, tunable capacitors and inductor are fabricated on separated silicon substrates and wire bonded to form the VCO. This hybrid approach is used to avoid the complexity of building the prototype oscillator. Both passive components are fabricated on silicon substrates and thus amenable to monolithic integration with standard IC process. The VCO achieves a -136 dBc/Hz phase noise at a 3 MHz offset frequency from the carrier, suitable for

most wireless communication applications and is tunable from 855 MHz to 863 MHz with 3 V.

Bernhard E. Boser 4/6/99

Professor Bernhard E. Boser, Chair Date

I dedicate this dissertation to my family.

Acknowledgments

I extend my sincere appreciation to Professor Bernhard Boser for his continuing support and guidance through my seven-year Ph.D. program at Berkeley. He has provided me the opportunity, freedom and constructive critique so that I can successfully complete this research work. I am also deeply indebted to Professor Donald Pederson who provided me an opportunity to start my graduate school study at Berkeley and guided me through my early years including the M.S. degree program. Many thanks go to Professor Robert Meyer and Professor Albert Pisano for their invaluable suggestions and for reading this dissertation. I am also grateful to Professor Roger Howe and Professor Charles Stone for serving on my qualifying examination committee. Special thanks go to Professor Roger Howe for many of his invaluable suggestions and help.

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Chapter 1

Introduction

1.1 Motivation

The increasing demand for wireless communication applications, such as cellular telephony, cordless phone, wireless data networks, two-way paging, global positioning system, etc., motivates a growing interest in building miniaturized wireless transceivers with multistandard capabilities. Such transceivers will greatly enhance the convenience and accessibility of various wireless services independent of geographic location. Miniaturizing current single-standard transceivers, through a high level of integration, is a critical step towards building transceivers that are compatible with multistandards. Highly integrated transceivers, compared to conventional designs, will also result in reduced package complexity, power consumption, and cost.

At present, most radio transceivers rely on a large number of discrete frequency-selection components, such as radio-frequency (RF) band-pass filters, intermediate-frequency (IF) channel-selection filters, RF voltage-controlled

oscillators (VCOs), quartz crystal oscillators, solid-state switches, etc., to perform the necessary analog signal processing. These off-chip devices occupy the majority transceiver area, severely hindering the miniaturization. In recent years a substantial amount of research has been devoted to develop new transceiver architectures that minimize the need for off-chip components. For example, direction conversion (zero-IF) [1], low-IF [2], quasi-IF [3] and direct sub-sampling down-conversion [4] architectures have been proposed, all of which attempt to eliminate the need for the IF channel-selection filters and possibly the RF image-rejection band-pass filters. However, currently these alternative approaches have not achieved performance on par with conventional designs. In addition, many discrete devices are still required in these new architectures. Integrating the off-chip components, therefore, remains a critical step towards building multistandard transceivers.

MicroElectroMechanical (MEM) technology, commonly referred as micromachining technology, offers a potential solution to integrate the discrete frequency-selection components onto silicon substrates. Off-chip macroscopic devices can be replaced by on-chip microelectromechanical versions. Band-pass filters at RF and IF, low-frequency low-noise oscillators intended for reference signal generators, and RF switches have been demonstrated through this technology with a size reduction of a few orders of magnitude, illustrated in Chapter 2. These devices, however, have not achieved performance on par with conventional counterparts. Further research efforts are still needed to enhance the performance.

Micromachining technology is also attractive for implementing on-chip high-quality RF variable capacitors and inductors, which are not available in

conventional integrated circuit (IC) technology, thus enabling the monolithic integration of RF low phase noise voltage-controlled oscillators with a performance matching that of conventional VCOs. The quality factor (Q) of these passive components ultimately determines an oscillator phase noise performance, a key parameter in a high-performance wireless communication system.

This research focuses on the design and fabrication of silicon-based on-chip variable capacitors and inductors, and RF VCOs using these passive components and meeting the performance requirements for typical wireless communication applications. New device structures and fabrication technologies based on surface-micromachining technologies will be proposed. The fabrication processes are fully compatible with standard IC technology; hence, the proposed devices are amenable to monolithic integration with active devices, allowing RF low phase noise VCOs to be realized in a complete monolithic form. With the continuing research effort and progress to integrate off-chip transceiver components with high performance through micromachining process, this technology will become an enabling technology to ultimately achieve multistandard transceivers for future personal telecommunications.

1.2 Thesis Organization

Chapter 2 describes a broad overview of microelectromechanical technologies developed for wireless communications. The need for multistandard miniature wireless transceivers is first illustrated. Current cellular phone implementations are then presented along with the size-reduction bottlenecks. Solutions for miniaturization based on micro-

machined transceiver components are reviewed with their advantages and drawbacks. Finally, a MEM-based highly-integrated wireless transceiver architecture with multistandard capabilities is envisioned.

In Chapter 3, the application of RF low phase noise VCOs is illustrated with requirements for typical wireless systems. Conventional VCO implementations based on a ring-oscillator topology and an electrically tunable resonator, LC tank circuit, are illustrated with advantages and drawbacks of each approach. The monolithic LC-based topology is chosen for this study with specified passive component requirements for achieving the low phase noise and tuning range for typical wireless applications.

Chapter 4 focuses on the design and fabrication of a micromachine-based all-aluminum variable capacitor. Measurement results from the fabricated devices will be presented with suggested improvements on device design and fabrication process.

Chapter 5 describes the design and fabrication of a monolithic three-dimensional coil inductor which achieves performance matching that of discrete counterparts. Inductors measurement results will be presented. Future improvements on device design and fabrication process will be proposed.

Chapter 6 presents the analysis of LC-tuned oscillators. The classical phase noise in a conventional LC oscillator is illustrated. However, in a micromachine-based LC-tuned oscillator an additional phase noise is generated due to the mechanical thermal vibration of the tunable capacitors. This phase noise is then manifested with proposed suppression methods.

Chapter 7 presents the design and measurement results of two prototype microma-

chine-based RF low phase noise VCOs. The electronic circuitry is fabricated in a 0.8 μm CMOS technology. The passive components and active electronics are realized on separate silicon substrates and interfaced through a chip-on-board approach to avoid the complexity of building the prototype VCOs. The oscillator topology, electronics design, measurement setup and performances are illustrated.

The last chapter, Chapter 8, recapitulates the major results of this study, and concludes with suggestions for future research.

Chapter 2

MicroElectroMechanical Technologies for Wireless Communications

2.1 Introduction

This chapter describes a broad overview of microelectromechanical (MEM) technologies developed for wireless communications. It first presents the importance and need for hand-held multistandard wireless transceivers followed by an illustration of a current cellular phone implementation, thus manifesting the significance of transceiver size reduction and also illustrating the miniaturization bottleneck. Microelectromechanical technologies are then proposed as a potential solution for miniaturizing transceivers. This is illustrated through that a number of critical radio components, which hinder current transceiver size reduction, can be realized with MEM technologies, and potentially replace off-chip counterparts presently employed in wireless transceivers, thus significantly reducing the size. The advantages and drawbacks of each proposed MEM device is also discussed. Finally a micromachine-based highly-miniaturized multistandard wireless transceiver architecture is envisioned for future personal telecommunications.

2.2 Global Wireless Communications

Wireless communications have been expanding rapidly all over the world during the last decade. The most popular applications include personal cellular telephony, cordless phone, two-way paging, wireless data network, global positioning system, etc. These wireless technologies have provided convenient access to telecommunications. However, as wireless services keep expanding, the number of different communication standards also increases. Various cellular telephony and cordless phone standards have been developed and adopted in different and the same countries. For example, most European countries rely on Global System for Mobile Communication (GSM) standard for cellular telephony and Digital European Cordless Telecommunications (DECT) standard for cordless phone application. On the other hand, countries such as U.S., Canada, Japan, etc. employ different standards, for example, PCS, AMPS, PDC, CTO, and JCT, for the same wireless applications. There are currently at least twenty standards available for personal wireless services. This number will likely keep increasing as more frequency bands get allocated for wireless applications. Furthermore, all the standards differ substantially from each other with respect to their carrier frequency, modulation scheme, bandwidth, channel spacing, transmission power, etc. As a result, different wireless communication transceivers are required with respect to various standards depending upon geographic location or service, limiting the accessibility of wireless communication devices supporting only a single standard.

It is, therefore, extremely desirable to develop a low-cost, palm-sized, hand-held wireless unit that can incorporate many communication standards for

each type of service [5]. This will allow, for example, a single phone to perform the functions of cellular phone and cordless phone compatibly with various standards in the world; thus overcoming the above limitations. Miniaturizing current wireless transceivers has become a critical step towards this goal because it will enable a large number of transceivers, each with a reduced size, to be placed into a same space as a present wireless phone for multistandard operation.

2.3 Current Cellular Phone Implementation

The main bottleneck of miniaturizing current wireless transceivers is the need for numerous off-chip frequency-selection components. Figure 2.1 presents a photo of a typical current cellular phone.

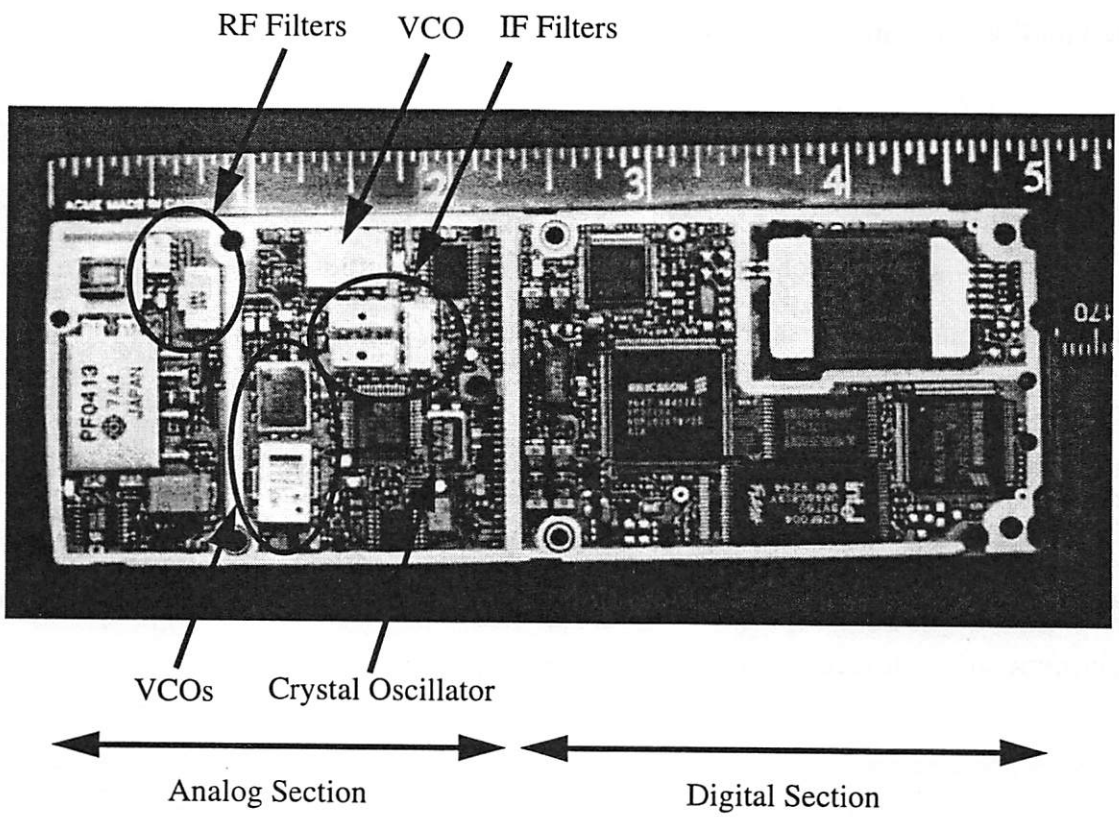


Figure 2.1: Current Cellular Phone (*Courtesy of Ericsson*)

This unit mainly consists of two sections, the front-end analog signal path and the back-end digital signal processing. The digital portion does not hinder the miniaturization because it can be programmed for multistandard operation, and ultimately integrated in a single chip through a high level integration. For example, a complete integrated digital section for a GSM transmitter with a total area of 5.1 mm^2 was recently demonstrated [6]. Further size reduction is expected with the continuing technology scaling. By contrast, the analog signal path severely limits the ultimate transceiver miniaturization because of a large number of discrete bulky components required to perform the analog signal processing. These off-chip components mainly consist of RF filters, RF voltage-controlled oscillators, channel-selection surface acoustic wave (SAW) filters, crystal oscillator, receive/transmit switches. Most of them are highlighted in Figure 2.1. As can be seen, they occupy the majority analog area compared to the small active analog electronics.

The off-chip components are not only expensive, but also designed for only one frequency band and one particular communication standard. Furthermore, device technology scaling is not expected due to the physics of these components. Consequently, a multistandard wireless phone, based upon current implementation technologies, will demand a multiple analog hardware (one for each standard), resulting in an increased cost, size, and weight. Therefore, miniaturizing these off-chip analog signal processing components has become the key challenge for realizing future low-cost, small-size communication devices with multistandard capabilities.

2.4 Wireless Transceiver Architectures

A conventional super-heterodyne radio architecture has been widely adopted to implement current wireless transceivers because of its robust performance [7]. Figure 2.2 presents this radio architecture, where many off-chip components, shaded in dark color, are required for the implementation.

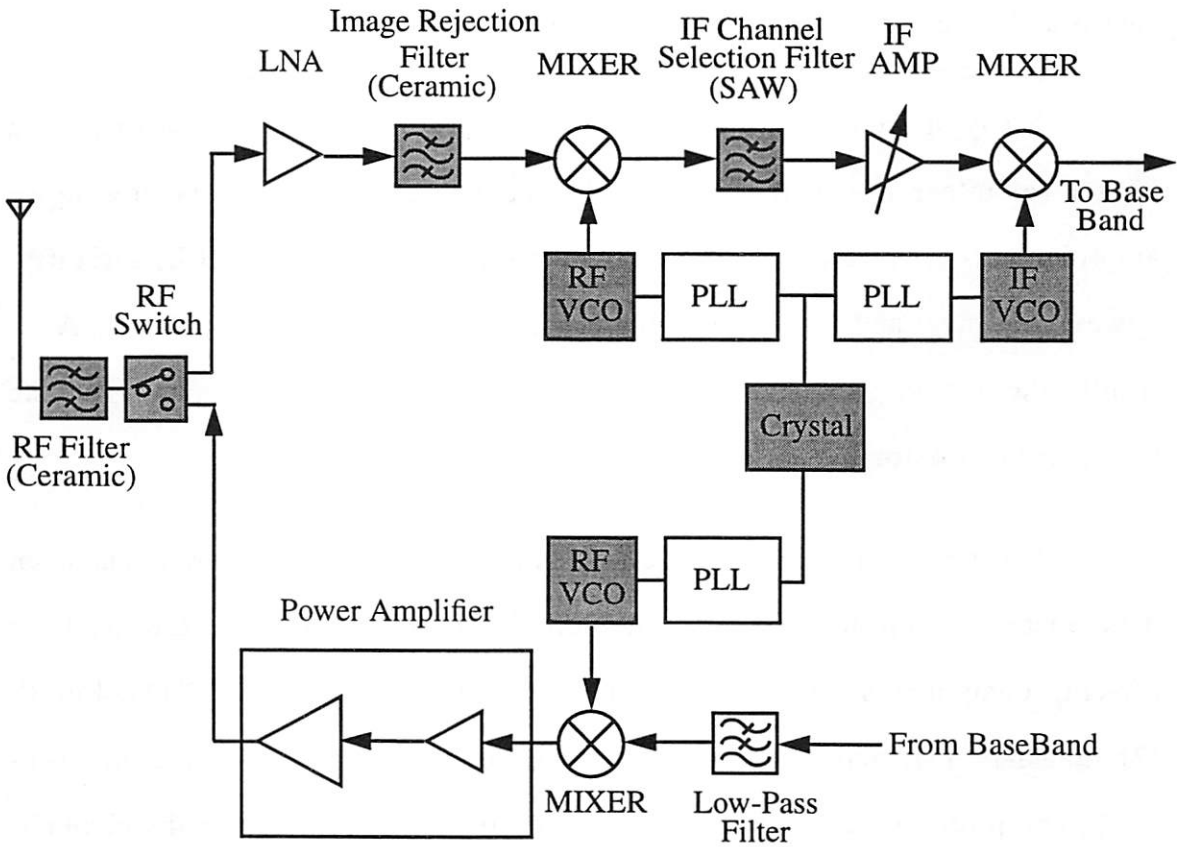


Figure 2.2: Super-heterodyne Radio Architecture

Discrete semiconductor solid-state switches are used to select the signal path between the receiver and transmitter. A ceramic band-pass filter and image rejection filter pass through the desired frequency band before the first frequency down conversion step takes place. A SAW filter selects the desired channel at the IF band prior to the second demodulation process. External VCOs with a crystal reference signal are required to perform the frequency synthesis at both RF and IF. All these frequency-selection components are essential for the robust and successful operation of the transceiver.

Many of the active devices in this system can be miniaturized through a high level integration using standard IC technology, including the low noise amplifier (LNA), mixers, VCO active electronics, synthesizer (PLL) circuitry, power amplifier, and baseband signal processing circuits [8, 9, 10, 6]. As a result, the off-chip passive components cause a severe bottleneck for the transceiver miniaturization.

During the recent years, a substantial amount of research has been devoted to develop new radio architectures that would minimize the need for off-chip components. For example, the direct conversion (zero-IF) [1], low-IF [2], quasi-IF [3], and direct sub-sampling down-conversion [4] architectures have been proposed, all of which attempt to eliminate the need for the channel-selection SAW filters and possibly the RF image-rejection filters. However; to date these alternative approaches have not achieved a performance on par with the super-heterodyne architecture, mainly due to practical issues in operations. In particular, the direction-conversion designs are hindered by random DC offsets which vary according to spatial movements of a transceiver. The low-IF approach partially suppresses the DC-offset problem. A new problem, however,

of image rejection of the relatively close-in image frequency is introduced. The quasi-IF architecture, achieving similar advantages as the low-IF design, cannot provide an adequate dynamic range for many wireless applications. The sub-sampling designs suffer from severe noise aliasing and jitter problems. Furthermore, all the proposed architectures do not achieve a truly miniaturized transceiver because they still rely on discrete RF band-pass filters, VCOs, crystal reference signal, solid-state switches. For these reasons, super-heterodyne architectures are still widely preferred and employed by the vast majority of wireless transceiver manufactures. Therefore, miniaturizing all the off-chip frequency-selection components currently required in the super-heterodyne architectures appears to be a viable solution that will ultimately achieve a multistandard wireless phone with a robust performance.

2.5 MicroElectroMechanical-Based RF Devices

MicroElectroMechanical technology, commonly referred as micromachining technology, offers a potential solution for miniaturizing the current wireless transceivers. Off-chip macroscopic components can be replaced by on-chip microelectromechanical versions. Band-pass filters at RF and IF, low-frequency low-noise oscillators intended for reference signal generators, RF switches have been demonstrated through this technology with a size reduction of a few orders of magnitude, thus favorable for miniaturizing wireless transceivers. This section presents a general overview of micromachine-based frequency-selection components developed for wireless applications, and also manifests their advantages and drawbacks.

2.5.1 RF Bandpass Filters

RF Band-pass filters centered around GigaHertz frequencies with a typical bandwidth of 5% of the center frequency, an insertion loss of a 1 to 2 dB, and good selectivity are critical to perform the desired frequency band selection and image rejection functions in a wireless transceiver. These filters operating at such high frequencies are commonly constructed using dielectric ceramic resonators with a typical dimension of 10 mm × 5 mm × 3 mm. These dimensions are determined by the operating frequency and permittivity of the ceramic material, thus a device size reduction is not expected. However, recent progresses in micromachining and thin-film deposition technologies have produced on-chip vibrating mechanical resonators based on unique characteristics of certain piezoelectric thin films.

Figure 2.3 presents the schematic of one such resonator. It is a thin-film bulk acoustic resonator (FBAR), consisting of a deposited piezoelectric film sandwiched between two metal electrodes in a similar fashion to quartz crystals; all suspended on a silicon nitride membrane constructed through a micromachining bulk etching technology.

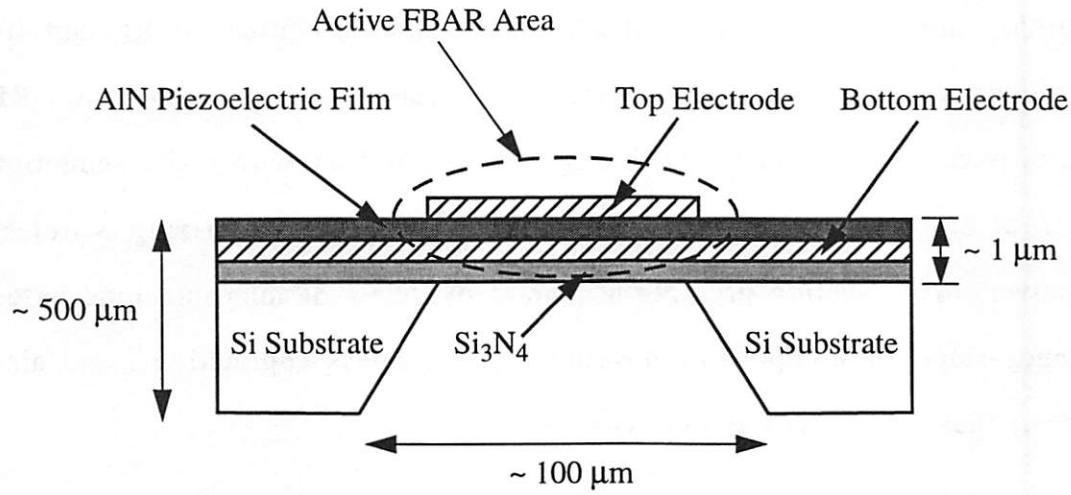


Figure 2.3: Thin-Film Bulk Acoustic Resonator

The membrane acoustically isolates the active FBAR area from the substrate, critical for ensuring a low insertion loss and a high filter selectivity. Aluminum nitride (AlN) and zinc oxide (ZnO) materials are typically employed as the piezoelectric films. These films can achieve an acoustic resonant frequency up to GigaHertz with a thickness on the order of one micrometer. With the micromachining and thin film deposition technologies, miniaturized high-performance filters based upon this type of resonators have been demonstrated for wireless communication applications with a size reduction of at least one oder of magnitude [11, 12], thus attractive for potentially replacing the off-chip counterparts.

One major drawback of this approach, however, is that the resonator frequency response is strongly depended upon the piezoelectric film thickness, which varies randomly in a deposition process. Such a variation may severely limit the applications of these filters especially with a bandwidth being a small fraction of the center frequency. A convenient and effective method for trimming and tuning is not yet available and needs to be developed to overcome the limitation.

2.5.2 IF Bandpass Filters

Highly-selective band-pass filters at IF band are crucial components in wireless transceiver designs. These filters only select the desired channel and reject energies at all other frequencies, thus greatly reducing the dynamic range requirements for the subsequent stages. The filter center frequency is typically between 10% to 20% of the RF carrier frequency, usually determined by the receiver image rejection requirement [5]. For example, a 100 MHz IF is

commonly chosen for a 1 GHz wireless application. The bandwidth, however, is a small fraction compared to the center frequency. A 200 KHz channel bandwidth, for example, is defined for GSM. Therefore, the filter has a large quality factor (Q) of at least 500. It is not feasible to implement a such high-Q filter with currently available on-chip spiral inductors and capacitors because of their limited Q values. In particular, the inductors have Q values around 5. An active electronic implementation is also not feasible because these IF filters operate at frequencies well beyond the capabilities of current integrated filter IC technologies. As a result, discrete SAW filters are demanded to fulfill the requirements but with a large size of typically 10 mm × 5 mm × 2 mm.

Surface micromachining technology has achieved highly miniaturized high-Q filters at low IFs. Figure 2.4 shows a schematic of a microresonator-based filter [13].

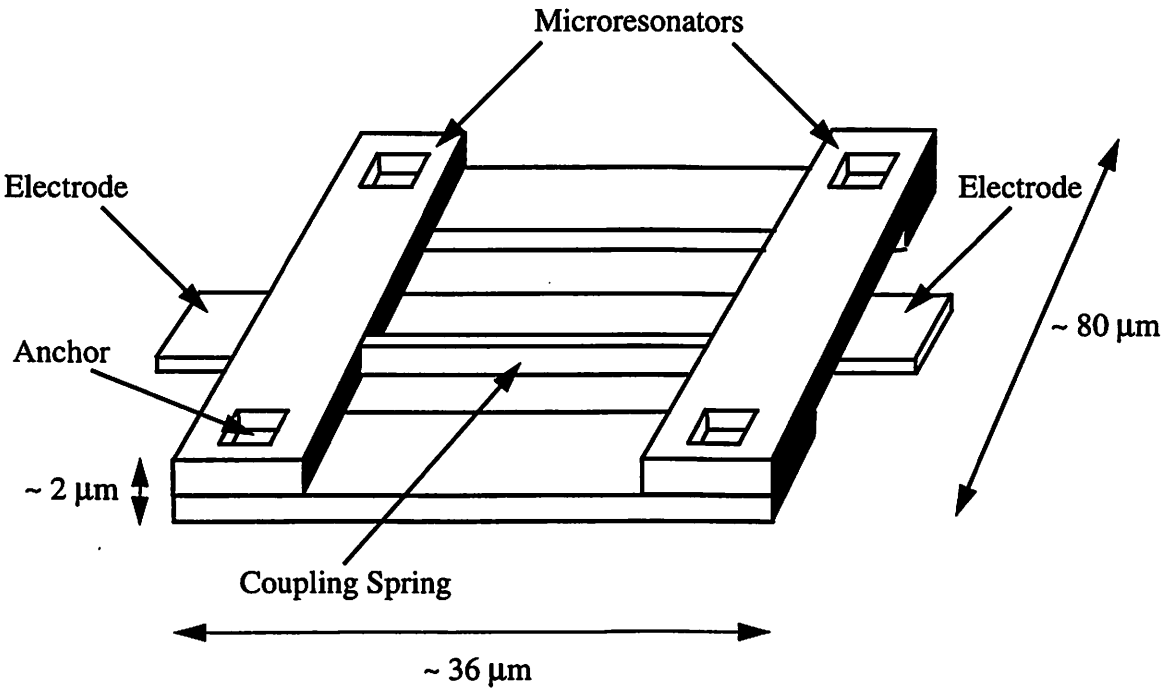


Figure 2.4: Microresonator-based IF filter

The device is fabricated in a polycrystalline silicon surface micromachining technology. The two air-bridge microresonators are coupled through a spring to achieve the desired filtering response. This type of filter has demonstrated with frequency up to 14.5 MHz, bandwidth on the order of 0.2% of the center frequency, and insertion loss less than 1 dB with a total area about 36 μm × 80 μm [13], representing four orders of magnitude in area reduction. Although these filters have not operated up to the typical 100 MHz intermediate frequency band, research efforts are being devoted to increase the operating frequency.

As with other technologies, micromachine-based resonators also have certain drawbacks in addition to their advantages. The micromachined filters need to operate in a vacuum environment around 50 μTorr in order to achieve a high quality factor, resulting in an increased package complexity [14]. The devices may also have a limited dynamic range and power handling capability [15]. The resonant frequency is strongly depended upon the dimensions and characteristics of the deposited film. Therefore, a reliable tuning method is needed in order to overcome the process variation effect and inherent temperature sensitivity. Furthermore, the high temperature micromachining processing steps are not fully compatible with standard IC technology. Consequently, a modified IC fabrication process is usually required [16, 17, 18], increasing the fabrication complexity and possibly reducing the yield. Further research efforts are needed to address these limitations before the ultimate commercialization of this type of filters.

2.5.3 Reference Signal Generators

A low noise reference signal generator is a critical component, along with a voltage-controlled oscillator, for implementing a frequency synthesizer in a wireless transceiver design. The synthesizer output signal spectral purity is determined by that of the reference signal within the synthesizer loop bandwidth [19]. Therefore, a low noise performance is a critical requirement for high-performance wireless applications.

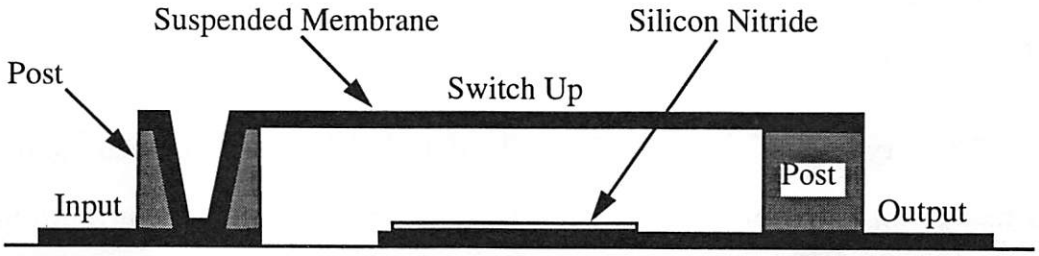
External quartz crystal oscillators are usually employed to serve as the low noise and low drift reference signal source. These oscillators typically operate around 10 MHz with an extremely low phase noise (a measure of spectral purity) of -140 dBc/Hz at 1 KHz offset frequency due to the high Q value (above 10^6) for the quartz crystal. The oscillator phase noise will be further discussed in the next chapter. The external crystal oscillators typically have a dimension of 8 mm × 5 mm × 2 mm. The lateral dimension is mainly determined by the size of a quartz piece cut along a desired orientation.

Micromachine-based flexural-mode mechanical resonators, on the other hand, have demonstrated a high quality factor over 80000 in a 50 μTorr vacuum [14]. The close-in phase noise of an oscillator using the resonator is inversely proportional to the resonator Q factor, as explained in detail in the next chapter. As a result, a high-Q micromechanical resonator-based oscillator, with a total area of 420 μm x 230 μm, has achieved an operation at 16.5 KHz with a clean spectral purity close to the carrier signal [20]. However, the limited power handling capability of the micromachined resonator will result in a degraded phase noise performance away from the carrier frequency, severely hindering its application as a reference signal generator. In addition, these oscillators have

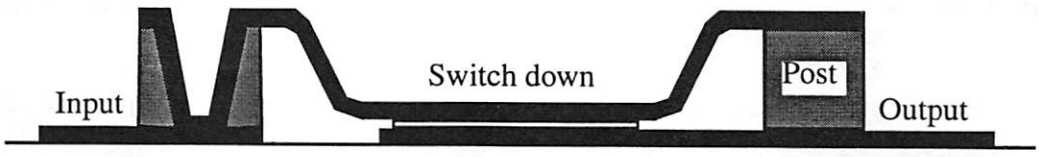
the same drawbacks as described in the previous section because of the micromechanical resonators employed in these devices. Therefore, further research efforts are demanded to enhance the performance.

2.5.4 RF Switches

The microelectromechanical RF switch is another potentially attractive miniaturized component offered by micromachining technologies. This device is intended to replace the off-chip counterparts switching between the receiver and transmitter signal path. They can also be used for tuning antennas, phase shifters, and filters. Figure 2.5 presents the cross-sectional schematic of an RF microswitch [21].



(a)



(b)

Figure 2.5: Micromechanical RF Switch: (a) Switch up, (b) Switch down

It consists of a conductive membrane, typically made of aluminum or gold alloy, suspended above a coplanar electrode by a 4 μm air gap. For RF or microwave applications, actual metal-to-metal contact is not necessary; rather, a step change in the plate-to-plate capacitance also realizes the switching function. Therefore, a thin silicon nitride layer with a thickness on the oder of 1000 Å is deposited above the bottom electrode. When the switch is in on-state, the membrane is high resulting in a small plate-to-plate capacitance; hence, a less high-frequency signal coupling (high isolation) between the two electrodes. The switch in the off-state, however, provides a large capacitance due to the thin silicon nitride layer, thus causing a strong signal coupling or less insertion loss. The dielectric layer also prevents the direct metal-to-metal contact when the membrane is pulled down from an electrostatic actuation, minimizing the welding or sticking problems commonly existing in direct contact switches [22, 23].

This type of micromechanical switches have achieved superior performance, in isolation and insertion loss, compared to those conventionally implemented with PIN diodes or GaAs FETs. Their small size, typically 200 μm × 200 μm, is attractive and critical for the transceiver miniaturization. Furthermore, unlike the solid-state counterparts, these devices consume zero power when activated and are also extremely linear, thus making them favorable for implementing low-power low-distortion wireless communication systems.

Besides all the attractiveness, the switches also have certain drawbacks. They are much slower than the solid-state devices. The typical switching speed is on the order of a few microseconds, compared to the nanosecond switching offered by their discrete counterparts. This may limit their use in high speed switching applications. A high actuation voltage, between 20 V and 60 V in

current designs, is required. Therefore, a separate power supply is demanded, increasing the system complexity. Although the nitride layer eliminates the metal-to-metal direct contact, the switches are still somewhat prone to stiction due to dielectric charging.

Micromachining technologies have provided a number of potential solutions for miniaturizing the discrete components currently employed in wireless transceivers although each proposed solution still needs to be further improved. Replacing the discrete low-noise radio-frequency voltage-controlled oscillators by on-chip versions, however, has not been addressed so far. In this research, we will explore how to miniaturize the low noise RF VCOs through the use of micromachining technologies. The subsequent chapters will emphasize on this topic.

2.6 Future MEM-Based Wireless Transceivers

With the continuing research effort and progress to integrate off-chip transceiver components with high performance through micromachining process, this technology will enable the realization of multistandard miniaturized wireless transceivers for future telecommunications. The MEM-based components can potentially replace the off-chip counterparts currently employed in transceivers, resulting in a size reduction of a few orders of magnitude. This will allow multistandard transceivers to be implemented within a current cellular phone size. Figure 2.6 illustrates a simplified multistandard architecture possible for the future receiver. The transmitter could be implemented in a similar manner.

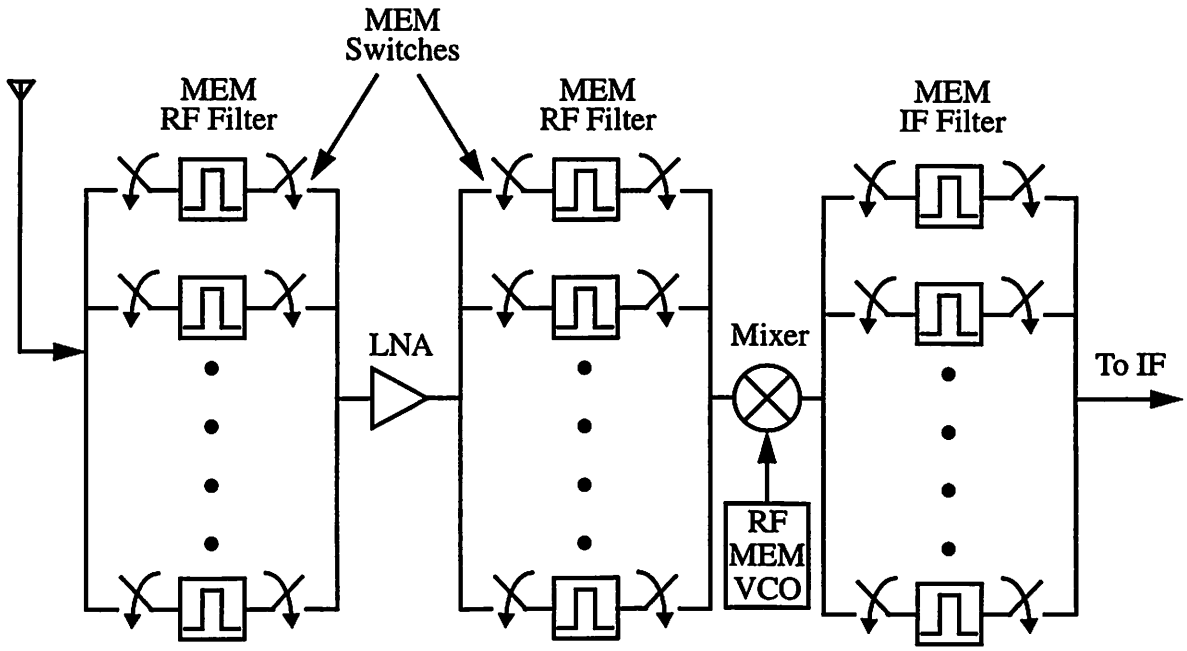


Figure 2.6: Proposed MEM-Based Multistandard Receiver Architecture

In this configuration, an array of micromachine-based RF and IF band-pass filters are centered at various frequencies (one for each standard). Each filter path is controlled by micromachined switches based upon the corresponding communication standard in use, thus achieving the multistandard capability. For the illustration purpose, only one LNA, mixer, and MEM-based VCO are shown in this architecture before the first IF stage. However, in reality an array of active electronics can be employed for multistandard functions.

All the MEM-based miniature components have been demonstrated on silicon substrates. Their processing steps, however, may not be fully compatible with standard IC technology, thus a modified integrated fabrication process is

often required as discussed in the previous section. It is, therefore, not clear at the current state whether a single-chip monolithic transceiver will provide a better performance and lower cost compared to a multi-substrate approach, where MEM-based components are fabricated on a separated substrate than the active electronics and finally interfaced together through techniques similar to Multi-Chip-Module (MCM) approaches. However, regardless the processing constraints, either approach would ultimately provide a highly miniaturized multistandard wireless transceiver, further enhancing the accessibility for future wireless communications.

2.7 Summary

As wireless services keep expanding, an increased number of communication standards will be developed. Therefore, a miniaturized multistandard transceiver is highly desirable for enhancing the wireless accessibility for personal telecommunications. Current cellular phones are mostly implemented based upon a super-heterodyne architecture, and this architecture is likely to be further employed due to its robust performance. However, a large number of discrete frequency-selection components, including band-pass filters at RF and IF, voltage-controlled oscillators, a crystal reference signal generator, RF switches are required in this configuration for analog signal processing. These off-chip components are much bigger compared to the active electronics and are dedicated to only one frequency band, thus severely hindering the size reduction for achieving a multistandard transceiver.

Microelectromechanical technologies, on the other hand, offer an potential solution for the miniaturization because most of the discrete

components currently employed in transceivers can be miniaturized through these technologies by a few orders of magnitude. As a result, they are favorable for transceiver size reduction and achieving wireless phones with multistandard capabilities. As with other novel technologies, MEM-based devices also have certain drawbacks such as process incompatibility with standard IC technology, increased package complexity, performance variation due to processing, devices degradation due to the mechanical nature, etc. Therefore, solutions to the above limitations need to be developed before the ultimate commercialization of MEM-based multistandard wireless transceivers.

Chapter 3

Low-Noise Radio-Frequency Voltage-Controlled Oscillator

3.1 Introduction

This chapter presents a general background on low-noise radio-frequency voltage-controlled oscillators. Its application in a wireless transceiver is first presented along with a description of an oscillator phase noise. The impact of an RF oscillator phase noise on transceiver system performance is then illustrated, followed by presenting VCO phase noise requirements for typical wireless communication applications.

Conventional VCO implementations based on a ring-oscillator topology and an electrically tunable resonator, LC tank circuit, are described with advantages and drawbacks of each approach. Finally, requirements of on-chip passive components, the inductors and variable capacitors, for achieving a low phase noise RF VCO for cellular telephony applications are presented.

3.2 RF VCOs for Wireless Communications

An RF VCO produces a single-tone in power spectrum with its frequency varied through an external controlling voltage source. This component plays a key role in a wireless communication transceiver. A wireless transceiver mainly performs two functions, reception and transmission. In the reception mode, an RF VCO is used to convert the high-frequency incoming signal to a low-frequency band, where further signal processing techniques are applied to extract the desired information, for example human voice or data. In the transmission mode it performs the opposite function, converting the low-frequency information onto a high-frequency carrier and transmitting though the air medium. Figure 3.1 presents a simplified receiver architecture typically used in wireless transceivers for illustration purpose.

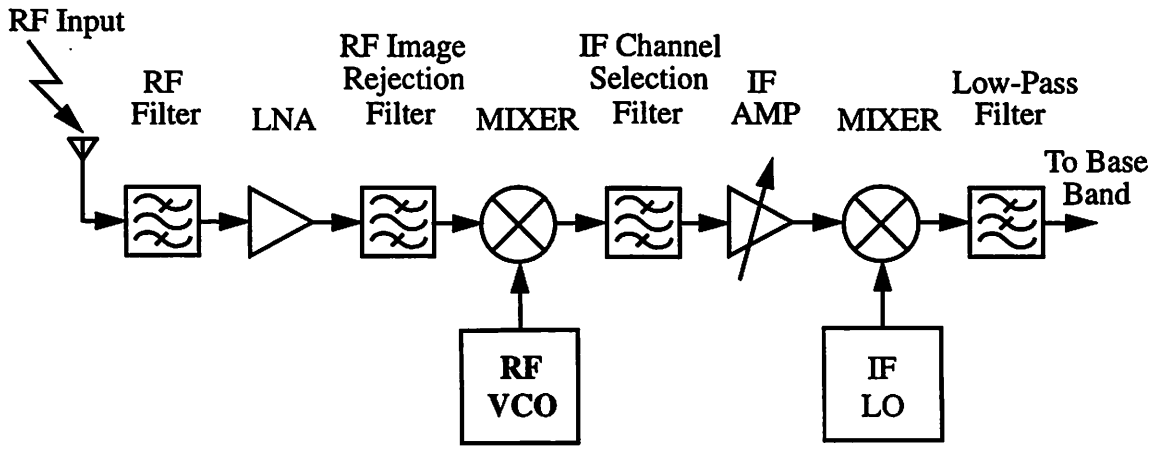


Figure 3.1: RF Receiver Front-End

The RF incoming signal at the antenna is first filtered through a band-pass filter and amplified by a LNA. The signal is then passed through a RF image-rejection filter and demodulated down to an IF band by mixing with the output signal from the RF VCO. The IF channel-selection filter selects the desired channel which, through a similar demodulation process, is further converted down to a reduced frequency, typically DC, for base-band signal processing.

The frequency response of the IF channel-selection filter is centered at a fixed frequency, typically 10% to 20% of the carrier frequency usually determined by the receiver image-rejection requirement. Therefore, the VCO has to be tuned with respect to a desired RF channel such that the frequency difference matches the predetermined IF frequency. For example, if the desired channel is centered at 900 MHz, the VCO needs to be tuned to either 1 GHz or 800 MHz for a 100 MHz IF.

The minimum tuning range of an RF VCO for a common wireless application is typically a small fraction of the carrier frequency, around 3%. For example, the GSM standard covers 890 MHz to 915 MHz, DCS-1800 and PCS-1900 require a tuning range of 1710 MHz-1785 MHz and 1850 MHz-1910 MHz respectively. However, manufacturing limitations would introduce device and parasitics mismatch, resulting in a shifted oscillator output frequency. To overcome this problem, either a trimming technique is required [24] or the VCO tuning range needs to be widened, reaching about 5% of the carrier frequency. As will be illustrated in the later sections, extending the VCO tuning range for a reduced supply voltage application has become increasingly difficult.

3.3 VCO Phase Noise Introduction

In addition to VCO tuning, the phase noise performance is another key parameter for high-performance communication systems because the phase noise of an oscillator would ultimately determine the selectivity of a wireless transceiver, which is explained in detail in the following section. An ideal VCO produces a single-tone in its power spectrum with the entire output power concentrated at the center frequency of f_o, as shown in Figure 3.2, and the center frequency can be tuned through an external controlling voltage source.

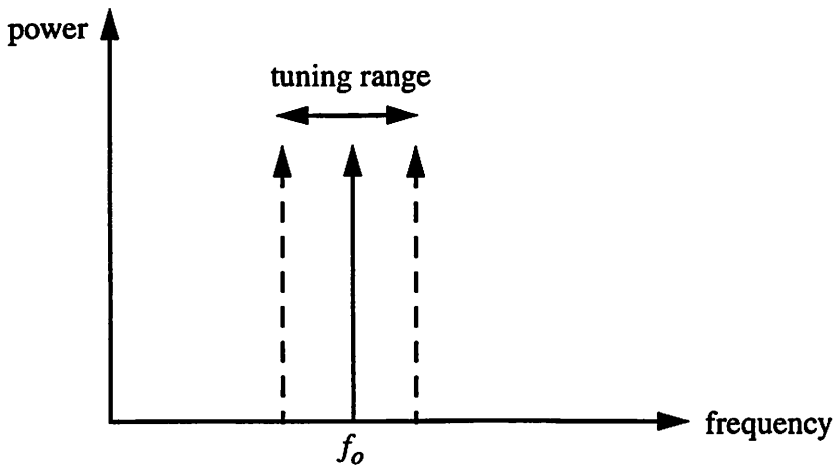


Figure 3.2: Ideal VCO Power Spectrum

However, in reality a VCO output signal has power spread in the vicinity of the center frequency causing non-zero spectral width. This is due to the thermal noise generated by the active electronics and resonator loss within an oscillator [25, 26]. Figure 3.3 presents a typical oscillator output power spectrum. The frequency, f_m, is an offset frequency from the oscillator center frequency, f_o. Phase noise is usually specified in dBc/Hz at a given offset frequency, where dBc refers to the noise power level in dB relative to the carrier

power; hence, an oscillator phase noise at a given offset frequency can be found from the ratio of the noise power in a 1-Hz bandwidth to the carrier power.

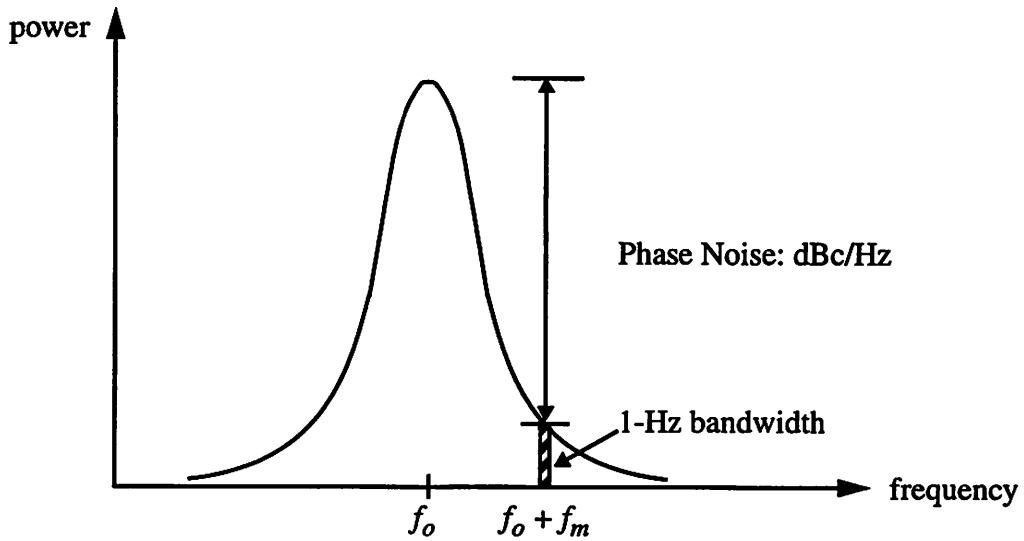


Figure 3.3: Typical VCO Power Spectrum

In Figure 3.3 this will be the ratio of the rectangle area with 1-Hz bandwidth at the offset frequency, f_m, to the carrier power at f_o. Thus, in an ideal VCO this ratio will correspond to a phase noise of negative infinity dBc/Hz at any non-zero offset.

In a typical oscillator, phase noise decreases as the offset frequency increases before reaching the white noise floor [26]. High-performance wireless systems, such as cellular telephony applications, demand VCOs to achieve a required phase noise at certain given offset frequencies to ensure an adequate selectivity of the transceiver.

3.4 Impact of Phase Noise on Transceiver System Performance

The two critical performance factors for a radio transceiver are sensitivity and selectivity. The sensitivity is a measure of the smallest RF signal

that can be received at the input antenna and still results in a recovered output with a required signal to noise ratio, or bit error rate (BER) for the case of digital communication system. The ability to recover the incoming RF signal over a wide dynamic range is important for a radio transceiver because the smallest recoverable signal determines the maximum transmission range for a given transmission power. Another reason is the fact that the frequency response of a transmission channel between a transmitter and a receiver often has a widely varied response with deep notches, which can cause a very large signal attenuation even for a small physical distance of separation. In mobile wireless applications this response can also vary rapidly with time.

The sensitivity of a radio receiver is ultimately limited by the noise introduced from the components, both passive and active that make up the system. A key performance specification for the system and its individual components is the noise figure (NF), defined as the signal to noise ratio at the input of a component over that at the output. This ratio is always greater than unity, or positive when expressed in dB. An improved sensitivity is always achieved through a low-noise design, but often at the expense of an increased power consumption [27]. Stringent NF specifications are imposed for various components in a radio transceiver in order to obtain a good sensitivity required for high-performance wireless communication systems [10, 28].

The other key parameter for a wireless transceiver is the selectivity, or the ability to receive one particular channel of interest in the presence of neighboring interferers. This is particularly important for wireless applications where the transmitter of a desired signal may be very distant physically while the interfering signals are in close proximity. This problem, called the "near-far"

problem, means that there are always practical situations which result in much stronger signals in adjacent channels or even other frequency bands than that of a desired channel. Therefore, it is crucial to design a receiver with a high selectivity to ensure a reliable reception. The phase noise in an RF oscillator plays a critical role to determine the selectivity because it can cause some of the energy in the adjacent channels to mix into the desired channel. This phenomenon is illustrated in Figure 3.4.

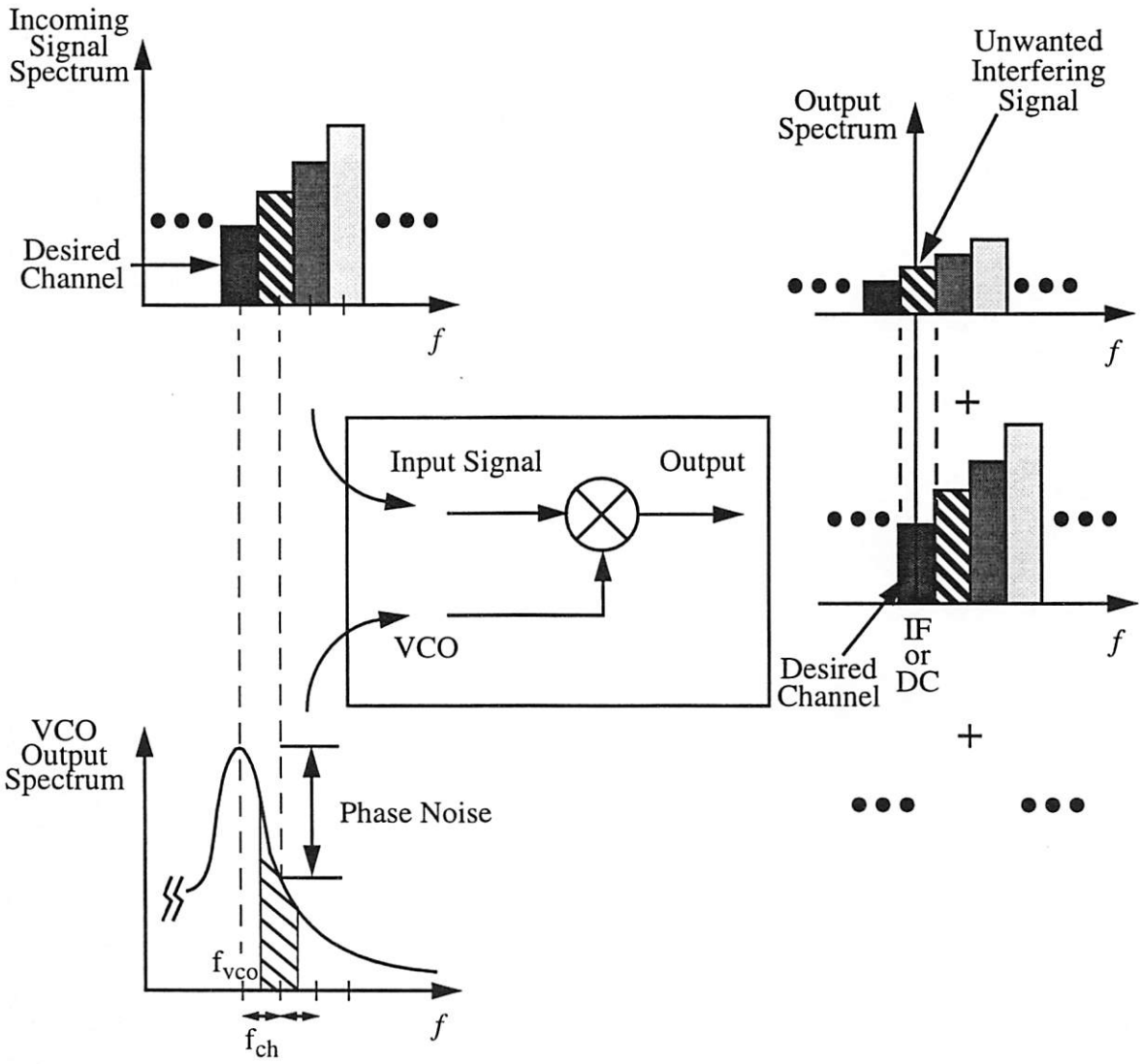


Figure 3.4: Selectivity Degradation Due to VCO Phase Noise

In this simplified receiver diagram, an incoming RF signal is mixed with the VCO to produce a copy of the input spectrum shifted to a lower frequency band, either a predetermined IF or baseband depending upon the receiver architecture. The incoming spectrum in this example consists of a small desired signal and three large neighboring interferer signals. If the RF VCO spectrum were perfectly sharp with all the power centered at f_{VCO}, then the output of the mixer would just be one shifted copy of the input spectrum without any energy from the adjacent channels mixed into the desired channel. However, in practice the power of a VCO is spread into the adjacent frequencies around the carrier resulting in a phase noise. The energy in the sideband of the oscillator spectrum also mixes with the incoming signal, producing unwanted and shifted copies of the incoming spectrum. For example, the energy at one channel away from the VCO center frequency will mix with the energy in the first undesired adjacent channel to produce an unwanted interference signal which is directly on top of the desired channel, resulting in a degraded receiver selectivity. It is, therefore, crucial to minimize the oscillator phase noise to suppress this undesired mixing effect, ensuring a good selectivity for a wireless system.

3.5 Typical VCO Phase Noise Requirements

In a typical wireless application, the "near-far" problem always results in much stronger interfering signals in the adjacent channels than that of a desired channel. Figure 3.5 illustrates the received RF incoming signal spectrum for a GSM cellular telephony. In this example, the desired signal power of -98 dBm is more than ten millions times (70 dB) smaller than the strongest interfering signal with a power level of -23 dBm at 3 MHz away and beyond.

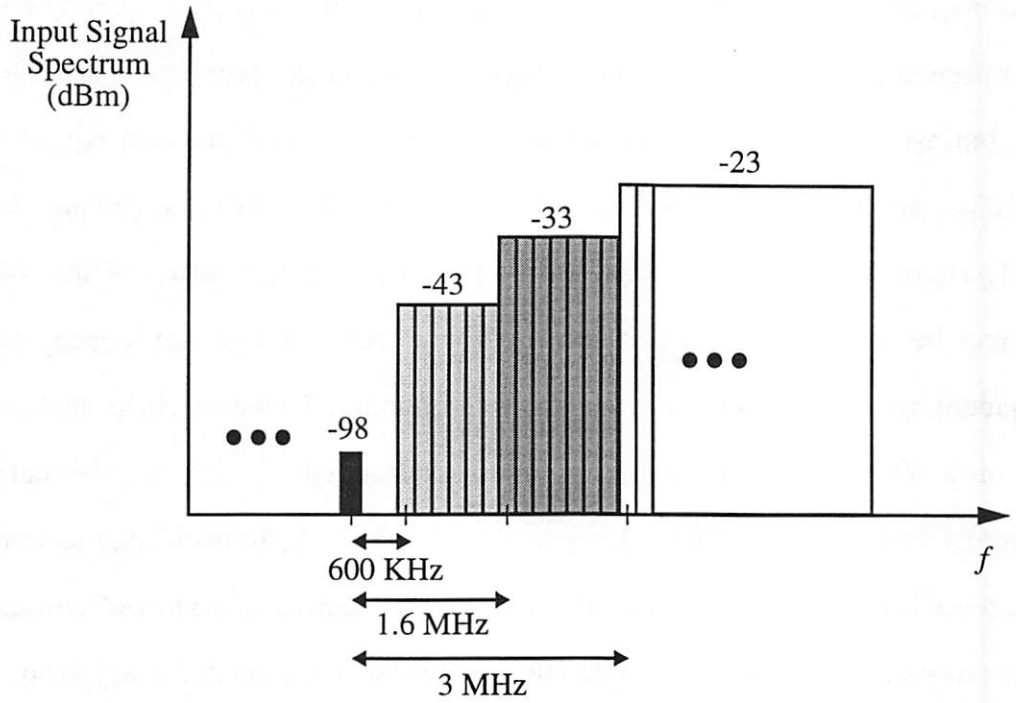


Figure 3.5: GSM Input Signal Spectrum

In order to satisfy the receiver selectivity requirement, the oscillator phase noise has to be low enough that any interfering signals will be small compared to the desired signal after the mixing operation. How small the final interfering signal needs to be depends on the signal to interferer ratio required at the receiver output for achieving an acceptable BER. For example, a 9 dB of signal to interferer ratio is required for GSM transceivers to obtain a BER of 0.01, corresponding to an adequate selectivity. Applications relying on different modulation techniques may demand different signal to interferer ratios for a certain BER.

An oscillator output power is typically spread over a range of frequencies. To determine the total power within a given neighboring channel, the power spectral density of an oscillator is integrated over the noise bandwidth of that channel. For most oscillators output spectrum, this is approximated as the product of the power spectral density at a channel center in dBc/Hz and the channel noise bandwidth in Hz. The mixing result of this oscillator noise power with the corresponding neighboring channel interferer power must fall below the required receiver signal to interferer ratio.

The oscillator phase noise required for GSM transceivers is determined below and also manifested in Figure 3.6. This approach is also applicable to other typical wireless communication standards. In the GSM example, the first interferer signal power of -43 dBm is at 600 KHz away from the -98 dBm desired signal. Therefore, a total of phase noise of -64 dBc within that neighboring channel is allowed for obtaining a signal to interferer ratio of 9 dB at the receiver output. That is -64 dBc relative to the carrier power; 9 dB for the required signal to interferer ratio and 55 dB for the difference in incoming power levels. For GSM standard, the noise bandwidth per channel is 152 KHz; therefore demanding a phase noise spectral density of -116 dBc/Hz at 600 KHz away from the oscillator center frequency.

The receiver selectivity requirement must be satisfied for all interfering conditions, including the -33 dBm and -23 dBm interferer signals at 1.6 MHz and 3 MHz away from the desired channel respectively. Consequently, the oscillator must also achieve a phase noise of -126 dBc/Hz and -136 dBc/Hz at 1.6 MHz and 3 MHz offset frequencies respectively. For typical oscillators the phase noise decreases at 20 dB per decade with the offset frequency from the

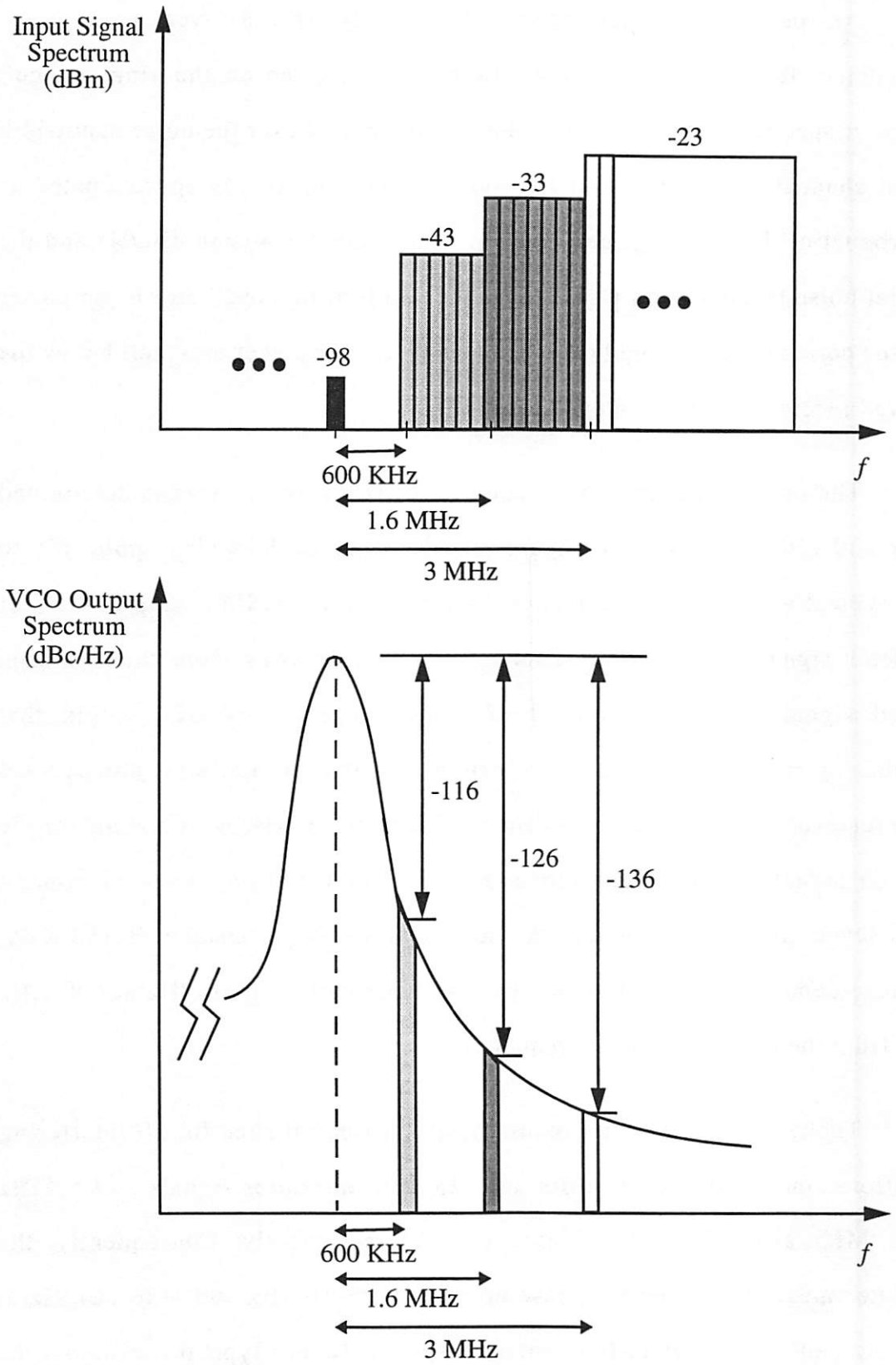


Figure 3.6: VCO Phase Noise Requirement for GSM

carrier. Therefore, a critical phase noise of -136 dBc/Hz at 3 MHz must be achieved in order to satisfy the worst case interfering condition. Furthermore, the worst case condition is meant to be satisfied with only one interferer present at a time for GSM; hence, the neighboring channel interferers will not all be present simultaneously. This assumption validates the phase noise calculations above without considering the superposition effect.

A conventional wireless receiver, such as the one shown in Figure 3.1, employs two oscillators. It is most difficult to achieve the required phase noise performance for the first oscillator operating at a high frequency. On the other hand, the second oscillator produces an inherently reduced phase noise due to the lower oscillation frequency. Furthermore, the channel-selection SAW filter at the IF band will suppress the interfering power significantly before the second frequency translation step, greatly relaxing the phase noise requirement for the second oscillator.

Table 1 lists the required oscillator phase noise performance for a number of wireless communication applications. The oscillator phase noise for cellular telephony applications is typically 25 dB more stringent than that of the cordless phone applications such as DECT standard. This is because a cordless phone usually operates in a less hostile environment compared to that of a cellular phone. There is one base station associated with each phone in close proximity, and interfering signals are weak due to other transmitters being physically far away.

Applications	Center Frequency	Channel Spacing	Critical Phase Noise Specification
GSM mobile receiver	~ 900 MHz	200 KHz	-136 dBc/Hz @ 3 MHz offset
PCS 1900 mobile receiver	~ 1900 MHz	200 KHz	-133 dBc/Hz @ 3 MHz offset
DCS 1800 mobile receiver	~ 1800 MHz	200 KHz	-131 dBc/Hz @ 3MHz offset
DECT mobile receiver	~ 1700 MHz	1.728 MHz	-111 dBc/Hz @ 3.4 MHz offset

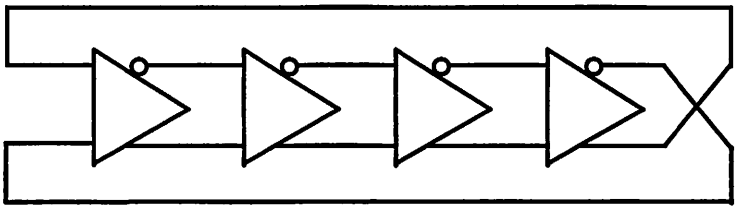
Table 3.1: Phase Noise Requirement Table for Typical Wireless Applications

3.6 Conventional VCO Implementations

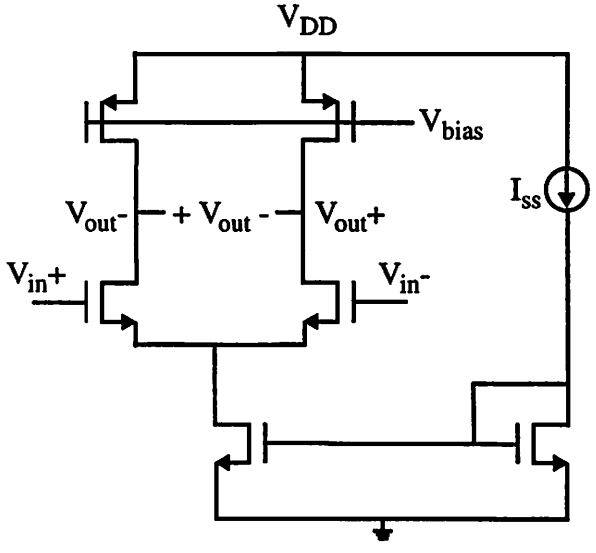
There are two common design approaches to implement voltage-controlled oscillators at radio frequencies: one is based upon a ring oscillator topology, and the other relies on an electrically tunable resonator. Each approach has certain advantages and drawbacks with respect to performance and integration compatibility.

3.6.1 Ring-Oscillator-Based VCOs

The ring oscillator topology offers a monolithic solution for implementing RF VCOs. Figure 3.7 presents a typical ring oscillator architecture, consisting of a chain of inverters with the last stage output fed back to the first stage input. In this example an even number of inverters, four stages, are used to cause an instability resulting in an oscillation. This architecture also provides quadrature differential outputs, attractive for image-band rejection.



(a)



(b)

Figure 3.7: Ring-Oscillator-Based VCO: (a) Topology (b) Typical Differential Delay Cell

The oscillation frequency, f_o, can be expressed as in Equation (3-1), where N is the number of stages in the oscillator, and T_d is the delay time of each stage.

$$f_o = \frac{1}{2NT_d} \tag{3-1}$$

A large oscillation frequency can be achieved through minimizing the number of stages and delay time, and frequency can be tuned by varying each stage delay. This can be achieved through controlling the tail current in every delay cell. A ring-oscillator-based VCO, for example, can achieve a tuning range from 750 Hz to 1.2 GHz under 3V [29]. The large tuning range results in a reduced sensitivity to process variations.

The VCO architecture does not require any electrical resonating elements. It only relies on active devices such as CMOS FETs. Consequently, the oscillator is extremely attractive for a monolithic implementation using a standard CMOS processing technology, providing a low cost solution.

Aside from the advantages from the ring-oscillator-based VCO design including high speed, large tuning range, simplicity, and low cost, the poor phase noise from this type of oscillator severely hinders it applications for high-performance wireless communication systems. A typical achievable phase noise is only on the order of -80 dBc/Hz at 100 KHz offset frequency from a 1 GHz carrier with a reasonable power consumption, which corresponds to -111 dBc/ Hz at 3.4 MHz offset frequency. This level of performance is barely suitable for cordless phone applications, but it falls well short from the stringent requirements for cellular telephony.

This particular oscillator architecture is responsible for the poor phase noise outcome. In a ring oscillator, the timing perturbation, or timing jitter, of one delay cell changes the starting switching point of the next cell, and this effect keeps passing onto the subsequent stages, resulting in a net rms timing jitter, $\Delta t_{osc\text{-}rms}$, for each cycle of oscillation. The timing jitter in each delay stage is caused by the thermal noise from the active devices in the delay cell. The thermal noise varies the zero-crossing points of the output waveform over a certain time range as shown in Figure 3.8.

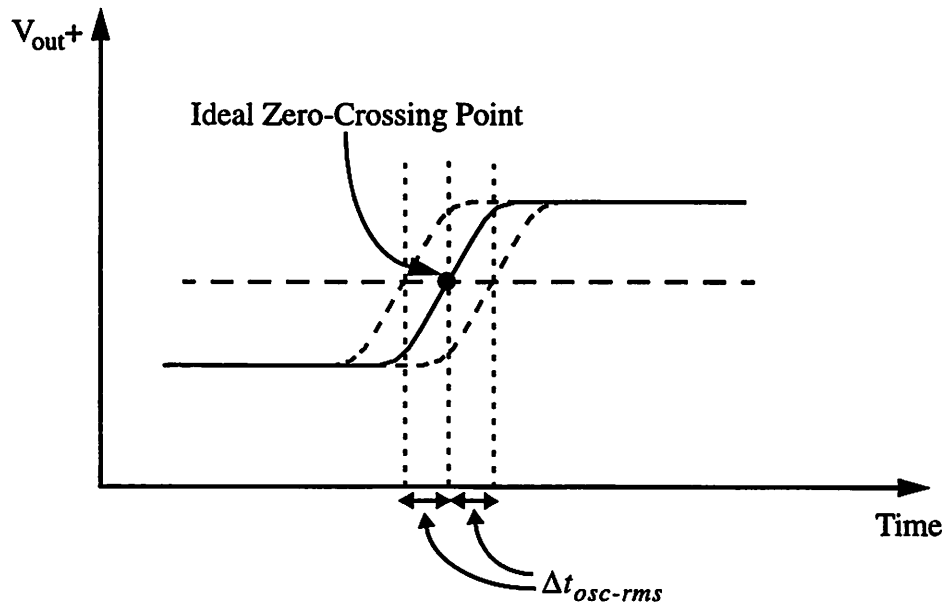


Figure 3.8: A Typical Output Waveform With Timing Certainty

The time-domain uncertainty introduces a phase fluctuation of the oscillator waveform resulting in a phase noise. This phase noise can be expressed as:

$$S_{\theta}(f_m) = \frac{\Delta t_{osc-rms}}{T_o}\left(\frac{f_o}{f_m}\right)^2, \tag{3-2}$$

where T_o is the nominal period of oscillation, f_o is the corresponding center frequency, and f_m is the offset frequency of interest. The detailed derivation of the equation can be found in [30]. In this expression, the phase noise decays at 20 dB per decade as the offset frequency increases, as predicted and observed in a numerous oscillators [31, 26, 32]. It is also inversely proportional to T_o because an oscillator with a large nominal period is less susceptible to a given timing jitter; hence, a less phase fluctuation for a lower phase noise.

Each delay cell in a ring oscillator, presented in Figure 3.7, suffers from a large timing perturbation because all the active devices conduct current at the zero-crossing points of the output waveform, generating a maximum amount of noise current at the output, causing the worst case timing jitter[32].

Increasing the slew rate of the differential amplifier inside a delay cell will minimize this timing jitter because of a sharper transition behavior in the output waveform. This will demand an increased amplifier tail current, causing a large power dissipation. A new phase noise expression based upon this criterion can be derived from equation (3-2) and presented as:

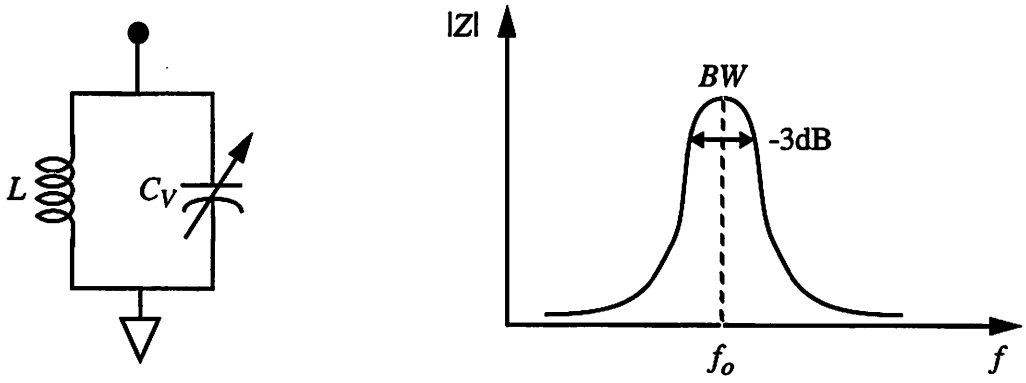
$$S_\theta(f_m) = \frac{FkT}{I_{SS}(V_{GS}-V_T)}\left(\frac{f_o}{f_m}\right)^2, \tag{3-3}$$

where I_{ss} is the amplifier tail current, V_{GS}-V_T is the saturation voltage for the input transconductance devices, and F is a design-dependent noise factor. From equation (3-3), it is apparent that the phase noise is independent of the device speed such as the f_T of the transistors; hence, little improvement is expected from future technology scaling. On the other hand, the phase noise would

decrease by 10 dB for every decade increase in the tail current. Therefore, in order to achieve a low phase noise suitable for cellular telephony applications as illustrated in table 1, a power consumption on the order of a few watts is usually required for an RF ring oscillator. A such level of power dissipation is too high to be considered for any wireless applications.

3.6.2 LC-Tank-Based VCOs

Another common approach to implement an RF VCO is to employ a tunable electrical resonator. A typical resonator can be constructed using a combination of a passive inductor and a variable capacitor as shown in Figure 3.9 (a).



(a) (b)

Figure 3.9: (a) Resonator Architecture (b) Resonator Frequency Response

This parallel structure has a band-pass frequency response depicted in Figure 3.9 (b) with the center frequency expressed in Equation (3-4).

$$f_o = \frac{1}{2\pi\sqrt{LC_V}} \tag{3-4}$$

By varying the capacitance value either electrically or mechanically, a tunable resonator can be realized. The finite impedance at the resonator center frequency is caused by the loss in the LC network, such as the resistive loss of the components, not drawn in this figure.

Figure 3.10 presents a general VCO topology that relies on a tunable electrical resonator.

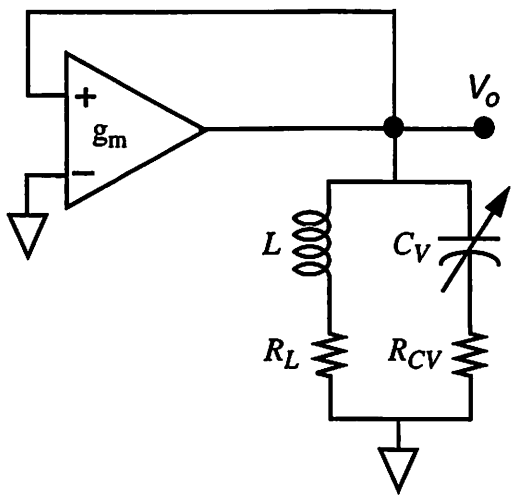


Figure 3.10: LC-Resonator-Based VCO Topology

The oscillator consists of a transconductance amplifier driving a parallel LC network with the amplifier output fed back to the input in a positive manner. The R_L and R_{CV} represent the resistive loss in the inductor and variable capacitor

respectively. An oscillation will develop at V_o when the overall loop gain matches or exceeds unity at a particular frequency, provided that the total loop phase shift is 360°. The oscillation frequency should be determined by the resonant frequency of the loaded LC network if designed properly. The detailed oscillator design considerations will be presented in Chapter 6. A series combination of an inductor and a variable capacitor can also be used to implement an RF VCO [33]. However, for the discussion in this section, the parallel LC network is chosen as the example.

A variable oscillator frequency can be achieved through tuning the resonator center frequency. In order to obtain a 5% tuning range for typical cellular applications, a capacitance variation of at least 10% is required. This tuning range has become increasingly challenging to achieve with the continuing power supply reduction for most low power wireless applications.

The key advantage of the LC-tank-based approach is the low phase noise achievable from the oscillator. Intuitively the LC resonator, with a band-pass frequency response, will reject thermal noise contributed from the active electronics away from the resonance, resulting in a suppressed sideband noise power; hence, a reduced phase noise. The sharper the resonator response, the lower the oscillator phase noise. The selectivity of the resonator is characterized by a parameter, commonly referred as the quality factor, Q. This factor is defined as the ratio between the resonator center frequency and -3dB bandwidth shown in Figure 3.9 (b); hence, a high Q factor will indicate a sharp resonator. The Q factor is inherently associated with the resonator loss, as will be illustrated in the next section.

The phase noise of this type of oscillator, assuming thermal noise is the only noise source from the active circuits, can be expressed as in Equation (3-5) [31], where f_o is the oscillator center frequency, f_m is the offset frequency of interest, P_{rf} is the oscillator RF output power, Q is the quality factor of the loaded resonator, kT is the thermal power, and F is the device excess noise factor.

$$S_\theta(f_m) = \frac{FkT}{2Q^2P_{rf}}\left(\frac{f_o}{f_m}\right)^2 \tag{3-5}$$

This expression carries a great deal of similarity compared to the ring-oscillator phase noise in Equation (3-3). The phase noise in both implementations is inversely proportional to the offset frequency and power dissipation. To achieve a large RF output power in a LC-based oscillator, an increased DC power is usually required. The key difference, however, is that the phase noise of the LC oscillator is inversely proportional to an additional factor, Q^2, because of the resonator used to construct this type of oscillator. Therefore, it results in a significant improvement in the phase noise performance. It is apparent from the above expression that the phase noise is reduced by 20 dB for every decade increase in the resonator Q value. For example, a LC oscillator with a Q of 30 would produce a 20 dB lower phase noise than that of an oscillator with a Q of 3, provided all other parameters are kept equal. Current RF VCOs used in cellular phones all rely on high-Q LC resonators. A resonator with a Q value close to 20 achieves a phase noise below -136 dBc/Hz at 3 MHz offset frequency suitable for typical wireless communications such as GSM cellular telephony application[10].

A high-Q resonator is also desirable for low power applications because it can achieve the same phase noise performance with a reduced RF output power. This is a key advantage for hand-held wireless communication devices where a long battery life time is a critical competitive advantage. Therefore, high-Q resonators are the crucial components for building RF VCOs that achieve the required stringent low phase noise while keeping the power consumption minimum.

The main drawback of this approach is that the high-Q resonators cannot be easily achieved monolithically because high-Q passive inductors and variable capacitors are not readily available in any standard IC process. As a result, discrete passive components with high enough Q values are demanded to implement the low phase noise VCOs. These off-chip devices increase package complexity, undesired parasitics, overall system area, and ultimately the cost [34]. Therefore, it is extremely desirable to replace these discrete components with on-chip high-Q counterparts, leading towards a complete monolithic implementation for future multistandard wireless transceivers.

3.7 Typical Requirements for On-Chip Passive Components

Most wireless communication applications currently operate within the frequency range from 900 MHz to about 2 GHz. Through Equation (3-4), any arbitrary values for an inductor and a capacitor can be used to form a resonator with its center frequency located within this frequency band. In a practice, however, only a certain range of passive components can be employed for such high-frequency applications. This limitation is mainly caused by the constraints

on the passive inductance values which are useful at these frequencies, as explained below.

RF passive inductors typically demand values ranging from 1 nH to 10 nH. This is because any inductor with a value much less than 1 nH is sensitive to the interconnect inductance. For example, an on-chip interconnect with a 5 μm width and a 100 μm length contributes roughly 0.1 nH inductance, and a metal trace on-board with a 3 mil (~75 μm) width and 1 mm length results in about 0.3 nH inductance. A large inductor, on the other hand, is less sensitive to the interconnect inductance. However, it reduces the component self resonant frequency, resulting in a capacitive behavior at the RF frequencies of interest. Therefore, inductance values are usually limited below 10 nH for applications in excess of 1 GHz [5]. Consequently, the corresponding capacitor values ranging from 2 pF to 5 pF are required to implement the LC resonators. These values are readily available either from discrete devices or on-chip implementations with self resonant frequency well above the operating frequency band.

In addition to the component values, the quality factors for these components are crucial in RF low noise VCO applications. Typical LC resonators with Q factors close to 20 are demanded for cellular telephony applications such as GSM [10, 34].

A parallel LC resonator in Figure 3.10 can be transformed into an equivalent configuration as shown in Figure 3.11,

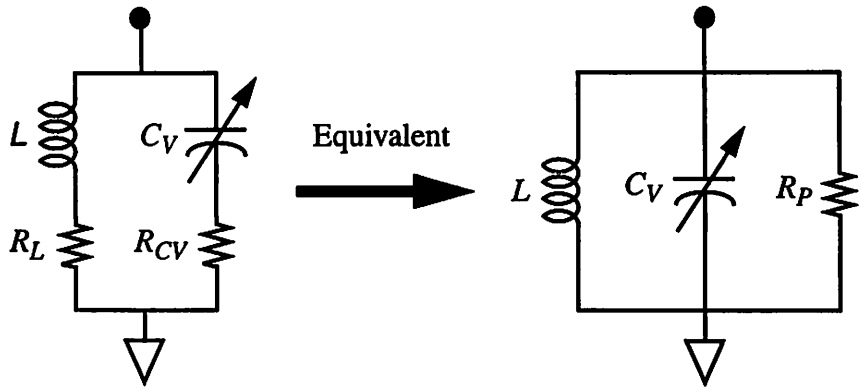


Figure 3.11: Equivalent Transformation of LC Resonator

where R_p is the effective parallel resistor associated with the passive components and can be expressed in Equation (3-6),

$$R_p = \left(Q_L^2 + 1\right)R_L \| \left(Q_{CV}^2 + 1\right)R_{CV} \tag{3-6}$$

where Q_L and Q_{CV} are the quality factors for the inductor and variable capacitor respectively, and they can be determined as:

$$Q_L = \frac{\omega L}{R_L} \quad \text{and} \quad Q_{CV} = \frac{1}{\omega C_V R_{CV}}. \tag{3-7}$$

Thus, for given component values it is crucial to minimize the device series resistance loss in order to achieve high Q factors. For large Q_L and Q_{CV}, R_p can be approximated in the expressions below.

$$R_p = Q_L^2 R_L \| Q_{CV}^2 R_{CV} \quad \text{or} \quad R_P = \frac{(\omega L)^2}{R_L} \| \frac{1}{(\omega C_V)^2 R_{CV}} \tag{3-8}$$

The quality factor for the LC resonator can be further determined in Equation (3-9).

$$Q_{\text{resonator}} = \frac{R_P}{\omega L} = R_P \omega C_V \tag{3-9}$$

Thus, a large R_p through minimizing R_L and R_{CV} will result in a high Q factor for the LC resonator. In order to achieve a resonator with a required Q factor, from Equations (3-8) and (3-9) it can be shown that each passive component must achieve a Q value of at least that of the resonator. In a practical situation, for example, a 5 nH inductor with a Q of 30 and a 5 pF capacitor with a Q of 60 are typically employed to achieve a 1 GH resonator with a Q factor of 20. It is important not to degrade the quality factor of the loaded resonator due to the active electronics loading. Otherwise, passive components with even higher Q factors are demanded to compensate the loading loss, making a more challenging task to obtain a low oscillator phase noise.

Most VCOs are tuned through a variable capacitor rather than a variable inductor. Semiconductor PN junction capacitors have been widely used as the tunable capacitors by varying the reverse-biased junction depletion width [35]. A common capacitance versus bias-voltage (CV) plot is shown in Figure 3.12. The capacitance decreases as the reverse-bias voltage increases. In a typical application, a 5% VCO frequency tuning range requires at least 10% capacitance variation under a 3 V supply. Thus with an oscillation amplitude of 1 V, a tuning voltage of only 2 V is available because forward biasing the silicon junction capacitors will result in a significant phase noise reduction. With the continuing power supply reduction for low power applications, this tuning requirement has become increasingly difficult to accommodate.

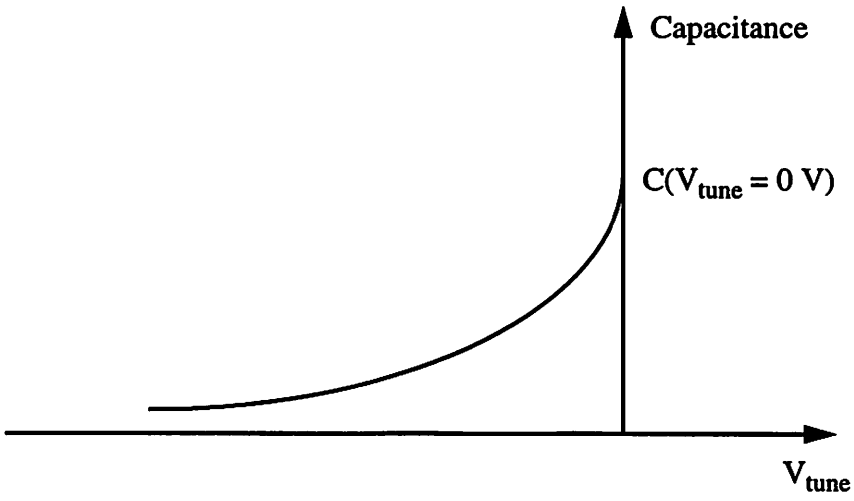


Figure 3.12: Typical CV Plot

Currently silicon on-chip passive components have limited quality factors. The monolithic spiral inductors, for example, have Q values about only 3 at 1 GHz due to the metal trace resistance and substrate loss at RF frequencies. The silicon series resistance also limits the junction variable capacitor Q below 10 at the same frequency. These values are far below the requirements for cellular telephony applications as described previously. In the next two chapters, new device structures and fabrication technologies based on microelectromechanical technologies are proposed to realize silicon-based on-chip passive components that achieve the cellular requirements.

3.8 Summary

An RF VCO is a critical component in a wireless transceiver. The oscillator phase noise, caused by electronic thermal noise and resonator loss, directly affects the transceiver selectivity. Phase noise requirements for cellular

telephony applications are usually much more stringent than that for cordless phone applications due to the hostile operation environment. A conventional VCO based upon a ring oscillator topology is attractive for a monolithic implementation, providing a low cost solution. However, its poor phase noise performance is inadequate for wireless applications. On the other hand, a VCO relying on a high-Q LC resonator produces a low phase noise suitable for cellular telephony applications. The drawback of this approach is that high-Q passive components, making up the resonators, are not readily available in standard IC technologies. Current on-chip components, such as spiral inductors and silicon junction capacitors, have Q values far below the cellular requirements. Therefore, currently discrete high-Q components are demanded for implementations, resulting in an increased package complexity, undesired parasitics, overall system area, and cost. Therefore, it is extremely desirable to develop new device structures and fabrication technologies to achieve on-chip high-Q passive components for implementing complete monolithic RF low phase noise VCOs for future multistandard cellular telephony applications.

Chapter 4

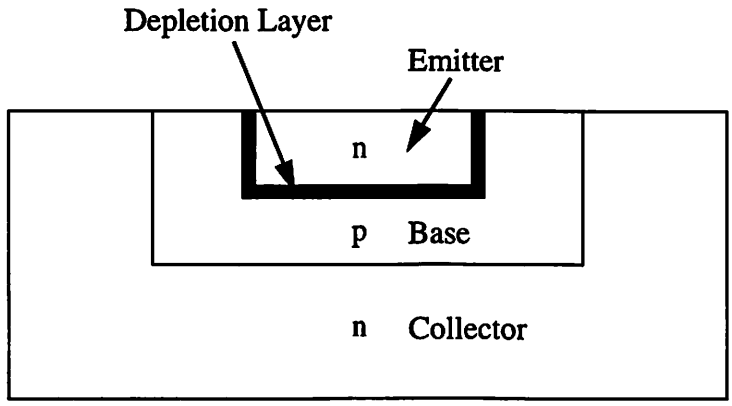
Surface Micromachined Variable Capacitors

4.1 Introduction

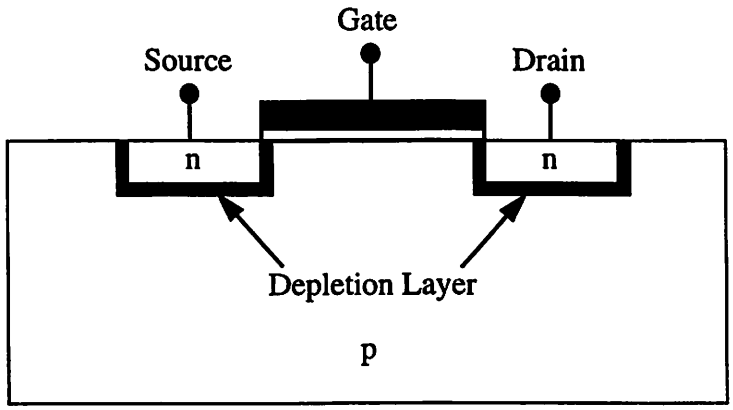
This chapter describes a surface micromachined variable capacitor intended for tuning RF low phase noise VCOs for cellular telephony applications. It first presents an overview of conventional monolithic variable capacitors currently available in standard IC process. Drawbacks associated with these capacitors are explained. Then a surface micromachined variable capacitor is proposed to substantially improve the performance. Device characteristics and design considerations are illustrated. The fabrication technology is outlined, and measurement results from fabricated devices are presented. Finally, future improvements for micromachined variable capacitors are proposed.

4.2 Conventional On-Chip Variable Capacitors

On-chip silicon PN junction capacitors have been widely used as monolithic variable capacitors for low-performance VCO applications [36, 37, 38]. These devices are typically made of a base-emitter junction capacitor in a bipolar junction transistor (BJT) or junction capacitors between the substrate and source or drain in a metal oxide semiconductor field-effect transistor (MOSFET), as illustrated in Figure 4.1. Varying the reverse-biased junction voltage changes the depletion layer thickness, thus resulting in a capacitance variation.



a: Variable Capacitor in a NPN BJT



b: Variable Capacitor in a NMOS

Figure 4.1: Silicon PN Junction Variable Capacitors

The tuning range of these variable capacitors is a strong function of supply voltage and becomes increasingly limited with the continuing power supply reduction. Furthermore, the devices severely suffer from the excessive silicon resistive losses, resulting in a low quality factor. The typical Q values are below 10 at Gigahertz frequencies, hindering their applications for high-performance wireless communication systems.

Recently a MOS accumulation-mode capacitor was proposed as an alternative on-chip variable capacitor in a CMOS process[39]. Figure 4.2 presents the cross section view of the device.

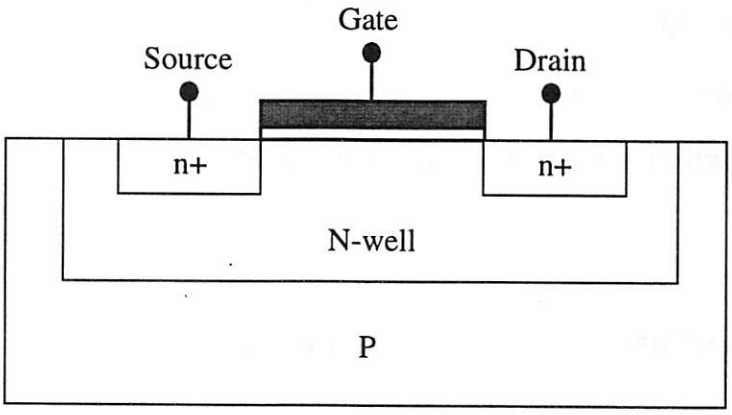


Figure 4.2: MOS Accumulation-Mode Variable Capacitor

The structure is similar to an N-channel MOSFET with the exception of being fabricated in an N-well instead of a normal P-substrate. This approach eliminates the parasitic PN-junction capacitances at the source and drain, which would otherwise limit the tuning range. Furthermore, the N-well provides a lower resistance than the conventional P-substrate due to the increased carrier mobility. The variable capacitance is obtained through the gate-to-bulk capacitance which is a function of the gate bias voltage. Fabricated devices have

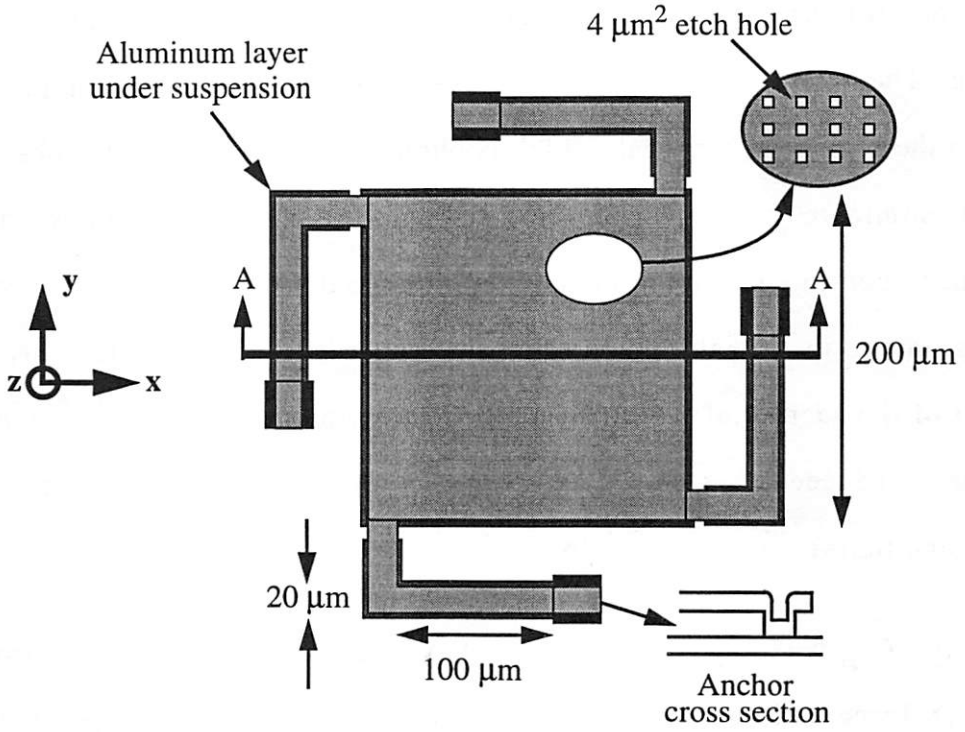
obtained a Q factor around 20 at 1 GHz, limited by the resistive losses from the N-well and polycrystalline silicon (polysilicon) gate. Although this approach offers an approximately twofold improvement in Q value, the achieved performance is far below the requirements for cellular telephony applications with Q factors of at least 60. In the next section, a surface micromachine-based all-aluminum variable capacitor is proposed to achieve the high-Q cellular requirements.

4.3 Micromachined Variable Capacitor Design

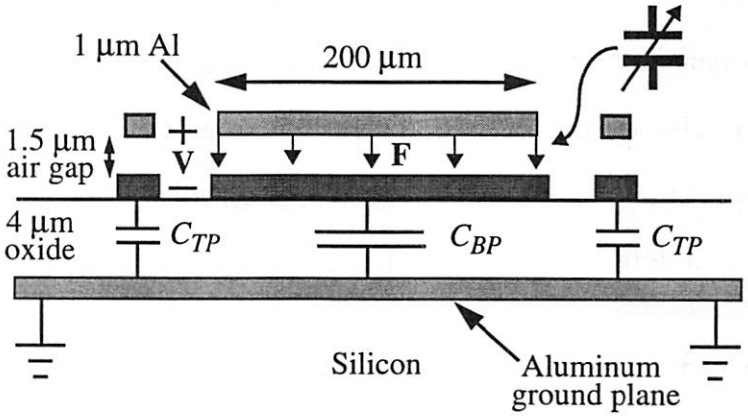
Micromachining technology offers an attractive solution to realize on-chip high-Q variable capacitors. This section presents the device description and design considerations. The capacitor electromechanical characteristics are also illustrated.

4.3.1 Micromachined Variable Capacitor Description

Figure 4.3 presents the top and cross section views of a micromachined variable capacitor. It consists of a 1 μm-thick aluminum plate suspended in air nominally 1.5 μm above the bottom aluminum layer and anchored with four mechanical folded-beam suspensions acting as springs. The folded suspensions have the advantage of being free to expand or contract if residual stress is present in the structure, thus relaxing the film stress and hence reducing warpage [40]. The symmetry avoids a systematic tilt of the device. Etch holes of 2 μm by 2 μm size spaced 10 μm apart ensure a complete removal of the sacrificial material for releasing the microstructure.



a: Top View



b: Cross Section

Figure 4.3: Micromachined Variable Capacitor

The chosen plate size of 200 μm by 200 μm and 1.5 μm nominal air gap result in a nominal capacitance value of approximately 200 fF. Thus a large capacitance value can be obtained through a parallel connection of multiple devices, as will be illustrated in Section 4.5. These capacitor dimensions represent a compromise between the achievable capacitance value and the

maximum structure size that can be fabricated reliably without excessive warping. The warping is mainly caused by the thermal expansion mismatch between the sacrificial material, which is photoresist in the current process, and the top aluminum layer. The elevated temperature during the deposition and subsequent cooling to the room temperature further contribute to a built-in strain gradient in the aluminum film and cause the structure to warp after removal of the sacrificial layer. Difficulties in removing the sacrificial material preclude a reduced air gap despite the potential for an increased capacitance density and tuning voltage reduction.

A DC bias voltage applied across the capacitor results in an electrostatic pull-down force and consequent reduction of the air gap. The suspended plate can be pull down at most by one-third of the original gap size before the pull-down force exceeds the mechanical restoring force causing the plate to be pulled all the way to the substrate. This deflection range corresponds to a maximum 50% increase in the capacitance value. The electrostatic pull-in instability will be manifested in detail in Section 4.3.2.

Figure 4.3 (b) also shows the parasitic capacitances, C_{TP} and C_{BP}, between the top and bottom plates of the variable capacitor and the substrate. They not only reduce the tuning range, but can also lower the quality factor of the overall capacitor if these capacitors have low Q factors. Section 4.3.4 discusses ways for alleviating these effects.

Despite the better mechanical properties and the vast experiences with polysilicon microstructure fabrication [41], aluminum is chosen as the structural material in the variable capacitor design for the following reasons. First, its low

sheet resistance is critical to minimize the ohmic losses and guarantee an adequate quality factor even at high frequencies. The second key advantage of aluminum is the low processing temperature of only 150 °C for the proposed fabrication procedure, as will be demonstrated in Section 4.4. Because of this low thermal budget, the variable capacitors can be fabricated on top of wafers with completed electronic circuits without degrading the performance of active devices. This is particularly crucial in applications such as RF where the availability of the most recent IC technology is a key competitive advantage. The inferior mechanical properties of aluminum compared to polysilicon are not critical for VCO applications because the suspended microstructure does not call for a large displacement or a high mechanical quality factor.

4.3.2 Electrostatics

Electrostatic forces have been extensively used as the driving force for microelectromechanical actuators and resonators [20, 21] and also as feedback forces for inertial sensors such as accelerometers and gyroscopes [42, 43]. This force is also used to vary the capacitance value of the micromachined variable capacitor as shown in the previous section. The electrostatic force exists when there is a voltage difference between two conductor plates. They are attractive with a magnitude equal to the rate of change of the stored electrical energy with respect to displacement.

Figure 4.4 presents two parallel conductor plates with a voltage, V, applied across them.

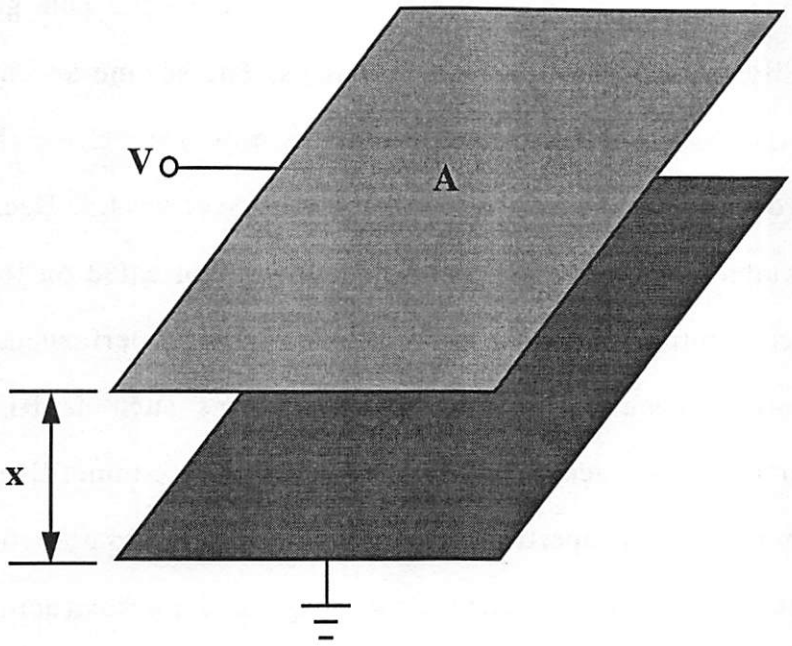


Figure 4.4: Parallel Conductor Plates

The resulting electrostatic force can be found through Equation (4-1):

$$F = \frac{\partial E}{\partial x} = \frac{\partial}{\partial x}\left(\frac{CV^2}{2}\right), \tag{4-1}$$

where E is the total electrical energy stored between the plates, C is the parallel-plate capacitance and can be expressed as:

$$C = \frac{\varepsilon_r \varepsilon_o A}{x}, \tag{4-2}$$

with fringing fields neglected, where A is the overlapping area of the parallel-plate, x is the gap in between, ε_o is the electric permittivity of vacuum, and ε_r is the relative dielectric constant of the medium between the plates. In practice, the error due to neglecting the fringing fields is small when the gap, x, is at least four times smaller than the width of the parallel plates [44].

From Equations (4-1) and (4-2), the electrostatic force can be determined by the following expression:

$$F = \frac{\varepsilon_r \varepsilon_o A}{2x^2} V^2. \tag{4-3}$$

This force, therefore, is a nonlinear function of the plate gap and applied voltage. Because the magnitude of the electrostatic force increases as the gap decreases, its effect can be viewed as an 'negative spring' [45]. The electrostatic spring constant thus can be found by differentiating the force equation with respect to position as shown in Equation (4-4).

$$k_e = \frac{\partial F}{\partial x} = -\frac{\varepsilon_r \varepsilon_o A}{x^3} V^2 \tag{4-4}$$

Since the electrostatic spring force subtracts from the mechanical spring force, it can be used to lower the effective spring constant and hence the resonant frequency of the mechanical structure. When the electrical spring becomes comparable to the mechanical spring, the resonant frequency starts to drop rapidly with small increases in the applied voltage. The pull-in voltage, or the voltage at which the resonant frequency drops to zero, occurs when the electrical spring constant is equal to the mechanical spring constant. The position at which the pull-in instability takes places can be found by equating Equation (4-3) with the mechanical restoring force:

$$k_m(x_o - x) = \frac{1}{2}\frac{\varepsilon_r \varepsilon_o A}{x^2} V^2, \tag{4-5}$$

where k_m is the mechanical spring constant, and x_o is the original parallel-plate gap with zero deflection. From Equation (4-5) the equilibrium voltage at position x is given by:

$$V(x) = \sqrt{\frac{2k_m(x_o - x)x^2}{\varepsilon_r \varepsilon_o A}}. \tag{4-6}$$

Differentiating this voltage with respect to position and setting the result to zero, Equation (4-6) is found to have a maximum value when x is equal to $(2/3)x_o$. Thus the corresponding pull-in voltage can be calculated as:

$$V_{pull-in} = \sqrt{\frac{8k_m x_o^3}{27\varepsilon_r \varepsilon_o A}} = \sqrt{\frac{8k_m x_o^2}{27C_o}}, \tag{4-7}$$

where C_o is the capacitance with zero deflection. Once the applied voltage exceeds $V_{pull\text{-}in}$, or the plate deflection is beyond $(1/3)x_o$, the electrostatic pull-down force cannot be balanced by the mechanical restoring force, causing the suspended plate to be pulled all the way to the substrate. This represents a maximum capacitance increase of 50% without parasitic effects.

4.3.3 Mechanical Suspension

Mechanical suspension design is a critical factor for micromachined variable capacitors. The suspensions need to be insensitive to the residual stress present in the film, compliant along the desired axis, and also robust enough to survive mechanical shocks. For the current design the folded suspensions shown in Figure 4.1 have been chosen because they are free to expand or contract if

residual stress exists in the structure, thus relaxing the stress and also reducing the warpage.

The suspensions are also designed to be compliant enough along the desired axis, the z-axis, as shown in Figure 4.3. In RF transceivers, the DC tuning voltage is typically limited to 3.3 V or less by the supply voltage, assuming there is not any AC signal present. Thus with a 1.5 μm nominal air gap and a 200 μm by 200 μm plate size, a mechanical suspension spring constant, k_m, of 3.8 N/m is required for a 3.3 V $V_{pull\text{-}in}$ according to Equation (4-7). This corresponds to a mechanical resonant frequency of approximately 30 KHz. Thus by designing the suspension with an increased compliance, a reduced tuning voltage requirement can be accommodated. This presents an important advantage over the conventional varactor diodes, which have a tuning range that is a strong function of the supply voltage. The mechanical variable capacitor is, therefore, attractive for low-power RF applications with the continuing supply voltage reduction. Various suspension compliances can be achieved through appropriately dimensioning the suspension as illustrated below. The suspension employed in the current design can sustain a large mechanical shock. To crash the suspended plate onto the substrate at a zero bias condition, a calculated acceleration over 6000 g is required. This level of shock resistance is well above the requirements for most personal portable wireless communication devices.

Figure 4.5 shows the top view of one of the four suspension beams for the variable capacitor.

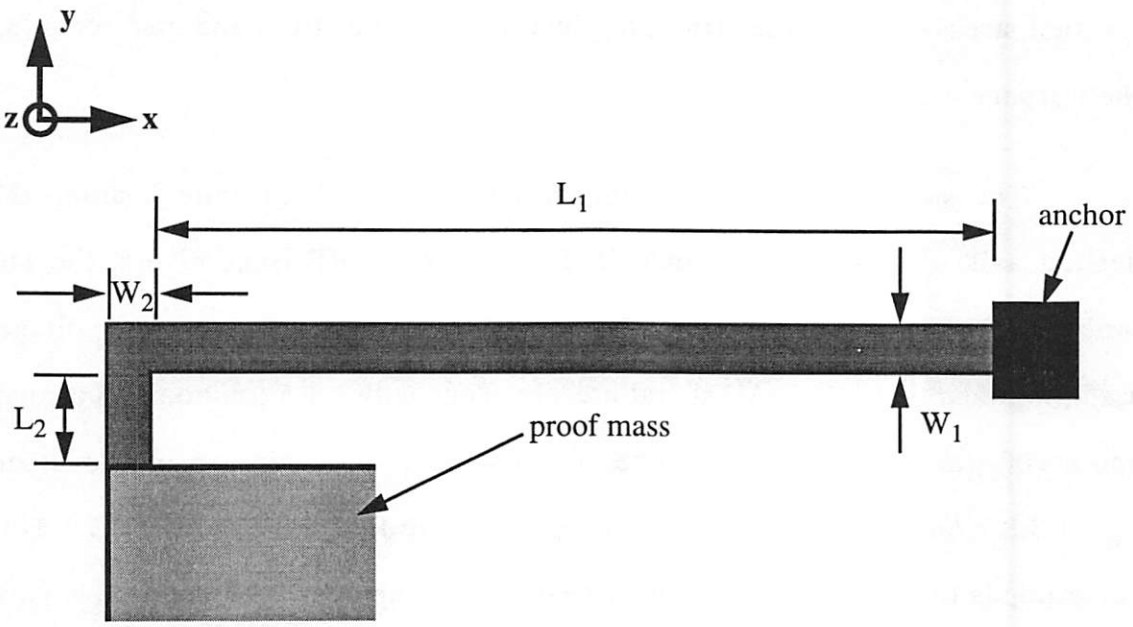


Figure 4.5: Suspension Beam

The spring constant for this suspension along the z-axis can be found in Equation (4-8) for $L_1/L_2 >> 1$ [46], where E is the Young's modulus of aluminum material, and t is the suspension beam thickness.

$$k_z = EW_1\left(\frac{t}{L_1}\right)^3 \tag{4-8}$$

From Equation (4-8) it can be seen that the spring constant is linearly proportional to the beam width and highly depended upon the beam length and thickness. Therefore, by varying the suspension dimension, different beam stiffness can be obtained for various tuning voltages. A beam width reduction by a factor of four, for example, results in a twice reduction of the required tuning voltage. The same effect can be achieved through either increasing or decreasing the beam length or thickness by 1.26 times respectively.

The total mechanical spring constant for the structure, k_m, is thus the sum of four suspension spring constants as expressed by:

$$k_m = 4k_z. \tag{4-9}$$

Assuming the aluminum Young's modulus of 70 GPa and t of 1 μm, L_1 of 100 μm and W_1 of 20 μm are thus chosen to achieve a total spring constant of 3.8 N/m. A 20 μm size is selected for both L_2 and W_2 in this design to satisfy the assumption of $L_1/L_2 >> 1$.

4.3.4 Parasitics Effects

The parasitic capacitances, C_{TP} and C_{BP}, between the top and bottom plates of the variable capacitor and the substrate are shown in Figure 4.1 (b). In a typical VCO application, the bottom plate of the capacitor is grounded and C_{BP} is therefore shorted. However, the top-plate parasitics, C_{TP}, appears in parallel with the variable capacitor. This not only reduces the tuning range, but can also lower the quality factor of the overall capacitor because C_{TP} suffers from the substrate resistive loss resulting in a low Q value. These problems are alleviated with a separated aluminum layer directly on the silicon substrate isolated from the capacitor bottom-plate with a 4 μm thick oxide. The thick oxide minimizes the value of the parasitic capacitances. The aluminum layer shields the parasitics from the lossy substrate, thus ensuring a high Q factor.

In this design the bottom-plate aluminum extends from the anchors under the suspensions up to the edge of the movable plate, as shown in Figure 4.1 (a). This conservative design has been chosen to prevent the capacitors from shorting out when the suspensions touch the bottom plate. However, this results

in a relatively large parasitic capacitance of 220 fF for the four suspensions and thus substantially reduces the tuning range. The capacitor shorting has been found not to be a problem in fabricated devices. Therefore, an improved layout shown in Figure 4.6 can be used for future designs, resulting in a reduction of C_{TP} to approximately 70 fF limited by the anchors parasitic capacitances and an additional increase of variable capacitance by about 100 fF.

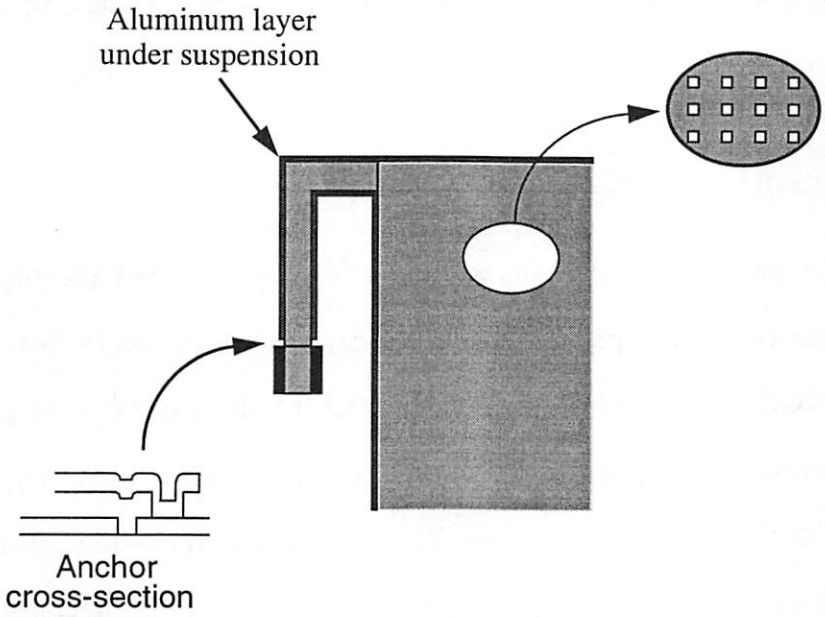


Figure 4.6: Proposed New Layout

4.3.5 Micromechanical Characteristics

The micromachined variable capacitor can be modeled as a mass-spring-damper system, as illustrated in Figure 4.7. The displacement of the capacitor proof mass, x, can be described as a function of the electrostatic driving force, F, as:

$$m\frac{\mathrm{d}^2 x}{\mathrm{d}t} + b\frac{\mathrm{d}x}{\mathrm{d}t} + k_m x = F, \tag{4-10}$$

where m is the mass of the moving element, and b is the damping coefficient due to the surrounding gas ambient and the internal dissipation of the system.

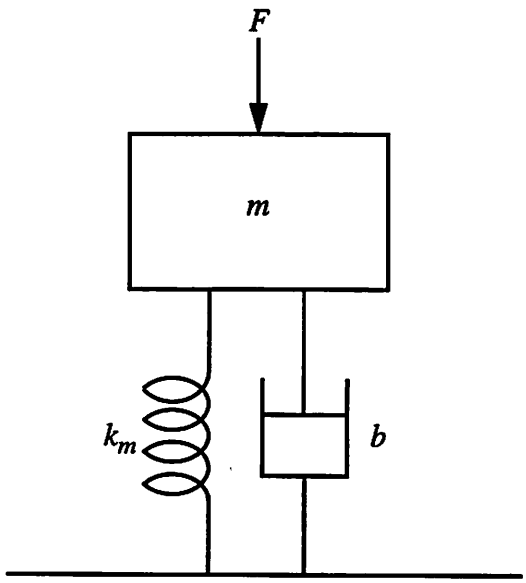


Figure 4.7: Mass-Spring-Damper Model

Since this equation is linear, it can be transformed into the Laplace domain to obtain the following frequency response between the displacement $X(s)$ and input force $F(s)$:

$$\frac{X(s)}{F(s)} = \frac{1}{ms^2 + bs + k_m} = \frac{\frac{1}{m}}{s^2 + \frac{\omega_n}{Q_M}s + \omega_n^2}, \tag{4-11}$$

where ω_n is the resonant frequency of the micromachined structure and determined as $\sqrt{k_m/m}$, Q_M is the structure mechanical quality factor and expressed as $(\omega_n m)/b$. Equation (4-11) can be further plotted on a logarithmic scale shown in Figure 4.8. It can be seen that for frequencies below ω_n, the ratio of displacement to force is approximately equal to $1/k_m$. At the resonance the

position change is amplified by a factor of Q_M. For frequencies above ω_n the response drops at 40 dB per decade.

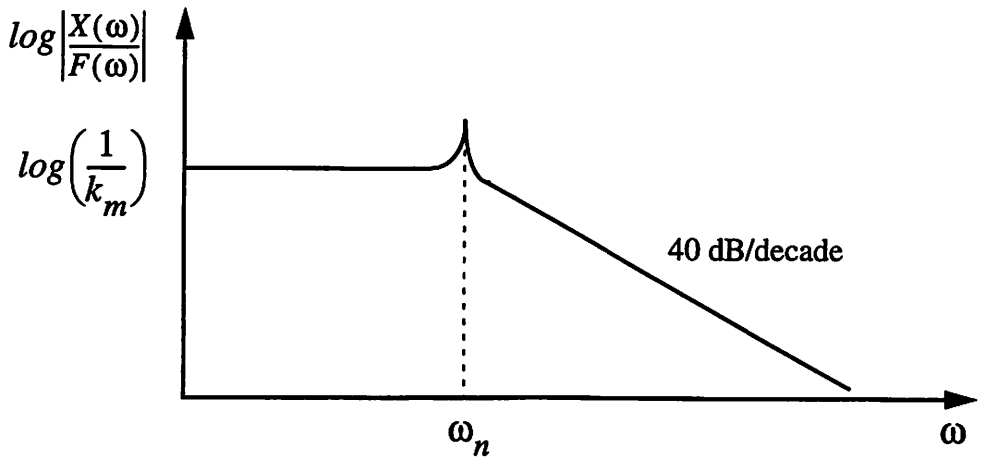


Figure 4.8: Frequency Response of Displacement Over Input Force

The capacitor air gap is, therefore, virtually constant for input force at frequencies beyond ω_n. Because the RF frequency of interest is almost six orders of magnitude larger than the mechanical resonant frequency, the variable capacitor is independent of RF signals. This characteristic results in an extremely linear behavior compared to the conventional varactor diodes, attractive for low-distortion filtering applications. The capacitor has another key advantage, which is that the device does not have the potential problem of becoming forward-biased. Consequently it can sustain a large RF signal amplitude, an advantage for achieving a low VCO phase noise and for tuning wireless transmitters with high output power requirements.

4.3.6 Mechanical Thermal Noise

The proof mass of a micromachined variable capacitor exhibits minute random vibrations due to collisions with molecules from the surrounding gas.

These collisions generate a noise force commonly known as the Brownian noise in mechanical systems. The basic principle that governs this mechanical thermal noise analysis is illustrated by the Equipartition Theorem [47]: the thermal energy of a system in equilibrium is $\frac{1}{2}k_BT$ for each quadratic energy storage mode, where k_B is the Boltzman's constant, 1.38×10^{-23}(J/K), and T is the absolute temperature. In a mass-spring-damper system, the quadratic energy storage modes are the spring potential and kinetic energies. Thus, the variance of the noise displacement, $\overline{x_n^2}$, resulting from the thermal agitation can be found by:

$$\frac{1}{2}k_m\overline{x_n^2} = \frac{1}{2}k_BT \ . \tag{4-12}$$

This thermal agitation of the proof mass causes a capacitance variation, thus resulting in an additional output frequency jitter, or phase noise, when the capacitors are used for VCO tuning as will be explained in Chapter 6.

The Brownian noise effect can be modeled as a noise force generator acting at the same location as the damper in a system. Figure 4.9 illustrates the addition of this noise force to the mass-spring-damper system.

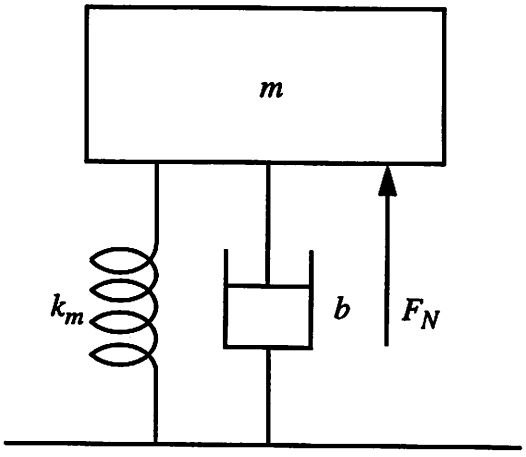


Figure 4.9: Mass-Spring-Damper System with Noise Force

The fluctuating noise force has a white spectral density given by [47]:

$$F_N = \sqrt{4k_BTb} \ [N/\sqrt{Hz}]. \tag{4-13}$$

Based on Equation (4-11), the displacement noise power spectral density, $\overline{X_n^2(\omega)}$, can be computed as:

$$\overline{X_n^2(\omega)} = \frac{4k_BTb}{k_m^2\left[\left(1-\frac{\omega^2}{\omega_n^2}\right)^2+\frac{1}{Q_M^2}\frac{\omega^2}{\omega_n^2}\right]}. \tag{4-14}$$

Figure 4.10 plots this spectral density on a logarithmic scale for illustration.

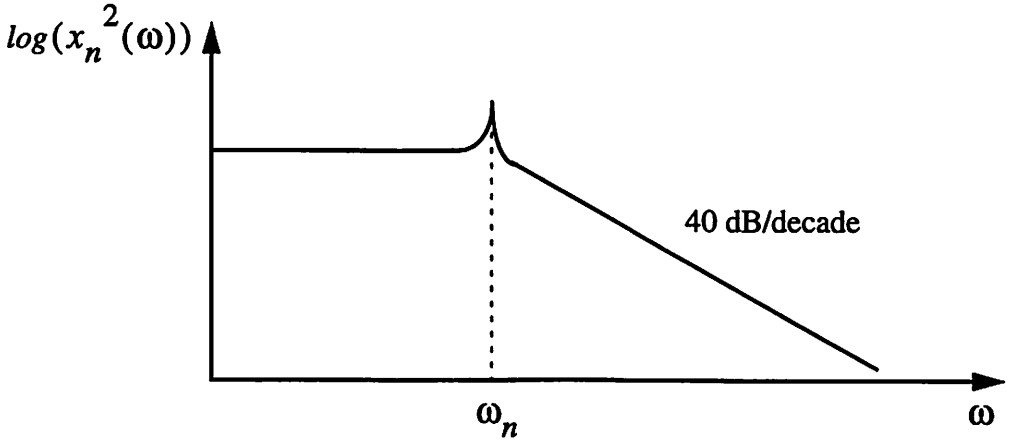


Figure 4.10: Displacement Noise Spectral Density

For frequencies below and above ω_n, Equation (4-14) evaluates approximately $4k_BT/mQ_M\omega_n^3$ and $4k_BT\omega_n/mQ_M\omega^4$ respectively. At the resonance it is $4k_BTQ_M/m\omega_n^3$. Since in a typical micromachined variable capacitor design, the movable structure mass and mechanical spring constant are constrained by the fabrication technology and tuning voltage requirement, Q_M is therefore the only parameter through which the spectral density can be altered significantly.

Increasing Q_M through decreasing the damping coefficient concentrates the thermal noise at ω_n while reducing it elsewhere as shown in Figure 4.11.

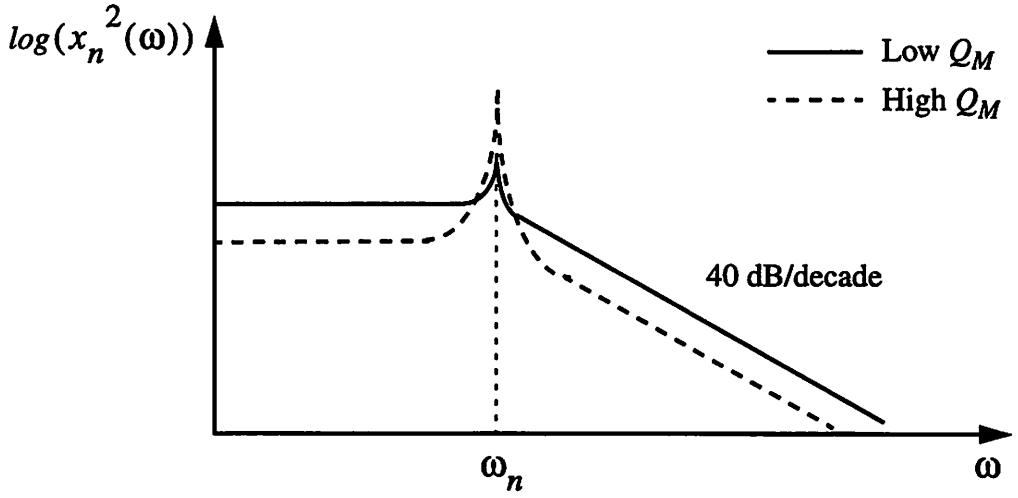
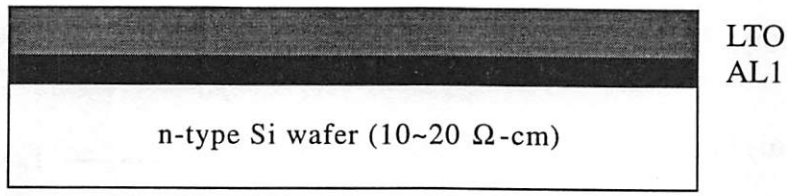


Figure 4.11: Effect of Q_M on Displacement Noise Spectral Density

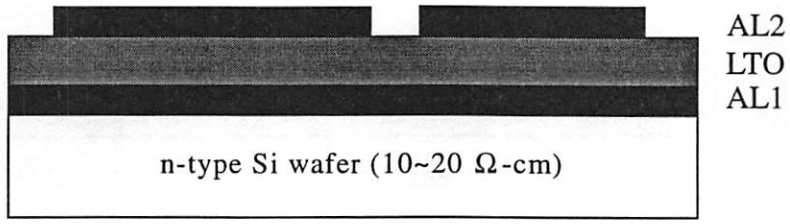
The impact of this noise on the phase noise of a micromachined VCO will be explained in Chapter 6.

4.4 Fabrication Process

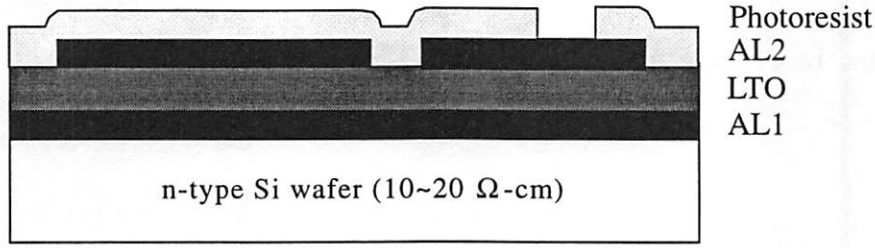
This section presents the fabrication technology for building micromachined variable capacitors. The experimental devices have been fabricated on a bare silicon wafer. Figure 4.12 illustrates the process flow.


LTO
AL1
n-type Si wafer (10~20 Ω-cm)

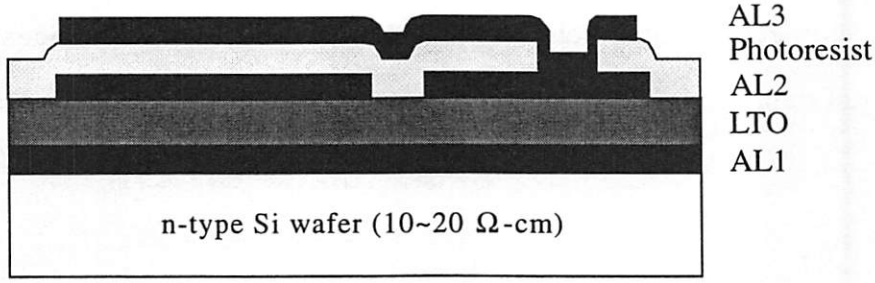
(a)


AL2
LTO
AL1
n-type Si wafer (10~20 Ω-cm)

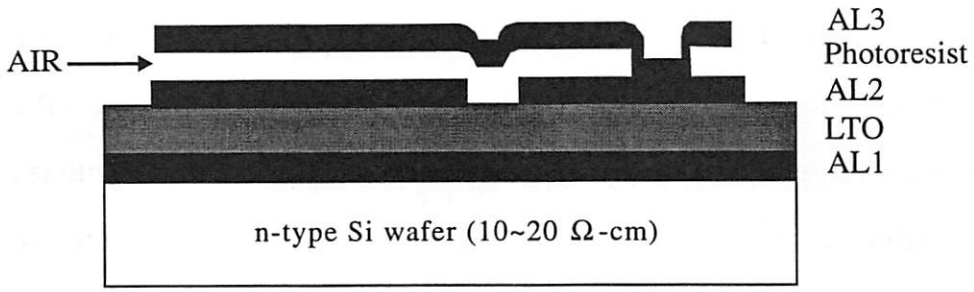
(b)


Photoresist
AL2
LTO
AL1
n-type Si wafer (10~20 Ω-cm)

(c)


AL3
Photoresist
AL2
LTO
AL1
n-type Si wafer (10~20 Ω-cm)

(d)



(e)

Figure 4.12: Fabrication Process Flow
(a) Ground Plane (1 μm Aluminum) and LTO Deposition
(b) First Aluminum Layer Deposition (1 μm) and Patterning
(c) Photoresist Sacrificial Layer (1.5 μm)
(d) Second Aluminum Layer (1 μm) with Anchor
(e) Released Structure After Etching Photoresist

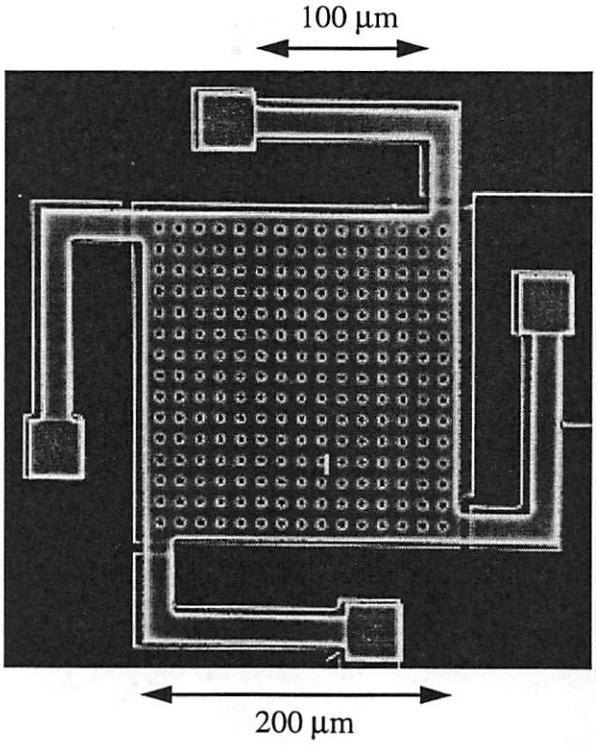
First, a 1 μm thick aluminum film is sputtered onto the bare silicon wafer to form a low resistance ground plane. Next, a 4 μm low-temperature oxide is deposited (Figure 4.12a). The bottom plate of the capacitor and interconnect trace consist of another 1 μm thick sputtered aluminum film (Figure 4.12b). A wet etching step is chosen to pattern this layer since the lateral dimensions of the structure are not critical. Next a 1.5 μm thick photoresist is deposited as a sacrificial layer. This material offers an excellent control of thickness and uniformity. Furthermore, it is photo-definable and easy to process. Contact windows to the bottom aluminum are opened in the resist (Figure 4.12c). It is then baked at 120 °C for 45 minutes to prevent an out-gassing during the subsequent deposition of the top aluminum layer. An increased baking time will result in a hardening of the resist and consequent difficulties in its removal. The final 1 μm aluminum layer is sputtered at a reduced power level and also wet etched since a plasma dry etch will cause the sacrificial layer outgassing. This

layer forms anchors to the bottom aluminum inside the contact windows through the resist. (Figure 4.12d). In addition, it is also deposited on all interconnect traces to lower the resistance, not shown in this figure. At this point, the wafers are coated with a 1 μm thick photoresist to protect against particulates during dicing. After dicing and removal of particulates, the protective resist is first etched away using a direct reactive iron etch. The sacrificial layer is then removed with an oxygen-based dry etch in a barrel reactor which offers an increased lateral etch rate, thus releasing the capacitor top-plate (Figure 4.12e).

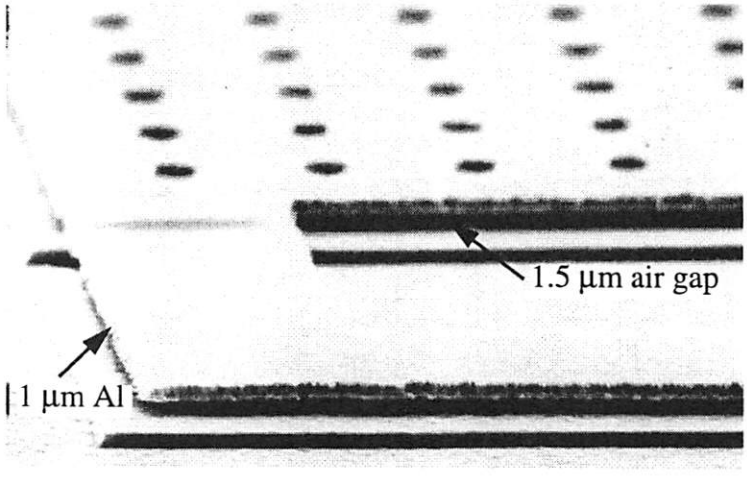
The oxygen gas pressure and plasma power must be set properly to ensure a complete removal of the resist and prevent the aluminum film from warping significantly. The structure heats up to approximately 150 °C during the 180-minute long etch. An optimal pressure of 500 mTorr and 150 W power have been determined experimentally. The dry etching process virtually eliminates the problem of the structure sticking to the substrate. This is an important advantage over the wet release procedure typically used with the polysilicon microstructures. Because of the low processing thermal budget, the variable capacitors can be fabricated on top of wafers with completed electronic circuits without degrading the performance of active devices. This is particularly crucial in applications such as RF where the availability of the most recent IC technology is a key competitive advantage.

4.5 Measurement Results

Figure 4.13 shows SEM micrographs of a single tunable capacitor.



a: Top View



b: Cross Section

Figure 4.13: SEMs of Fabricated Micromachined Capacitors

An optical inspection reveals doming of the capacitor top-plate. The plate center and four corners are approximately 0.5 μm above and below the nominal gap of 1.5 μm respectively. Figure 4.14 presents a parallel connection of four variable capacitors achieving a nominal capacitance value of 2 pF, designed for implementing an experimental VCO described in Chapter 7.

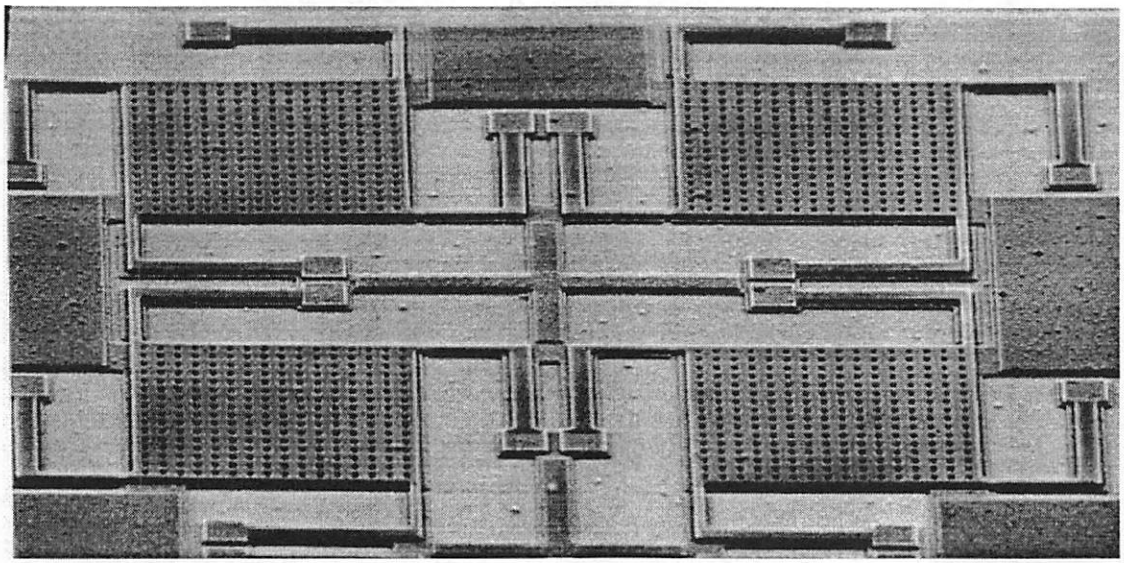


Figure 4.14: Four Parallel Microstructures

With a 3 V tuning voltage, the capacitance value can be varied between 2.04 pF to 2.35 pF. This corresponds to a tuning range of 15% shown in Figure 4.15.

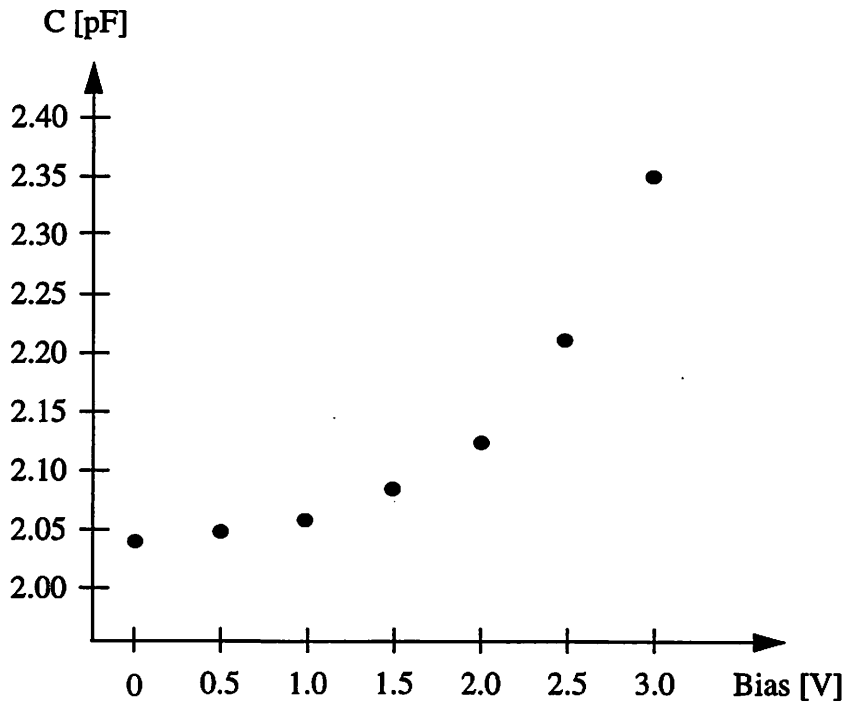


Figure 4.15: C-V Measurement

This tuning range is limited by the parasitic capacitances described in Section 4.3.4 and can be extended through appropriate layout changes as illustrated in Figure 4.6.

Aside from the capacitance, the quality factor is the most important electrical parameter of the structure. It is most accurately determined with an S-parameter measurement. Figure 4.16 shows the measured S11 curve in a Smith Chart for the four parallel capacitors. The S11 curve follows closely the lower-half of the unit circle as is expected for a capacitor. At 1 GHz the series resistance is 1.2 Ω corresponding to a Q value of 62, limited by the resistive loss in the interconnect traces.

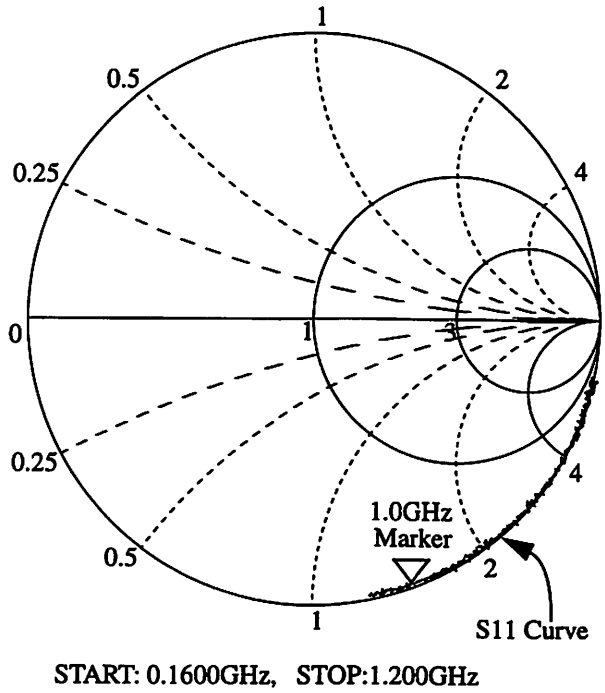


Figure 4.16: Measured S11 in a Smith Chart

This quality factor matches or exceeds that of discrete varactor diodes and is at least an order of magnitude larger than the Q value of a typical junction capacitor implemented in a standard IC process.

4.6 Proposed Device Improvements

It is desirable to further improve the quality factor and reduce the tuning voltage for the micromachined variable capacitors. An improved Q value will reduce the VCO power consumption for the same phase noise performance. This improvement can be accomplished by replacing aluminum structural material with an even lower resistivity metal such as copper. Copper has been introduced as a standard interconnect metal for integrated circuit processes [48].

Copper has also been used to fabricate micromachined actuators [49]. This material can be easily deposited by electroplating or electroless plating. Furthermore, it has a significant advantage in being low stress compared to sputtered aluminum film when the plating conditions are appropriately controlled. Large suspended microstructures up to a few millimeters size have been demonstrated [49]. An increased structure size will reduce the tuning voltage for a given compliance. This introduces another degree of freedom to achieve a low tuning voltage.

In devices fabricated so far, an air gap is the only insulating layer between the capacitor two plates. It thus causes a metal-to-metal short when the plates get into physical contact, resulting in a metal welding destroying the device permanently. An additional dielectric material such as oxide or nitride deposited on top of the bottom capacitor plate is necessary to eliminate this damaging effect.

The parallel-plate capacitor has a maximum theoretical tuning range of 50%, limited by the electrostatic snapping action of the device. Although the achieved tuning range is adequate for typical monolithic VCO applications, an increased range beyond this limitation is highly desirable for tuning front-end filters for multiband operations. New device structures relying on different operating principles are needed to further extend the tuning range.

Lateral-comb-drive variable capacitors [50] and zipper varactors [51] have achieved an increased tuning range between 100% to 200%. However, these devices require a large tuning voltage, 15 V to 35 V, and have been demonstrated only in silicon material resulting in low quality factors similar to

that of conventional silicon junction variable capacitors. Copper structures based upon the similar operating principles are very attractive for achieving both high Q values and a large tuning range. Future design improvements are required to further reduce the tuning voltage.

4.7 Summary

An aluminum micromachined variable capacitor is proposed as a tuning element for RF low phase noise VCOs for cellular telephony applications. Aluminum is selected as the structural material for its low sheet resistance, critical for obtaining a high Q value at high frequencies. Its low processing temperature makes the capacitors amenable to a monolithic integration in a standard IC process without sacrificing performance of active devices.

An appropriate dimensioning of the suspension permits a low tuning voltage, a key advantage over the conventional varactor diode. The devices are also extremely linear and does not have the potential problem of becoming forward-biased due to the mechanical behavior, thus attractive for low-distortion signal filtering and high power applications. Despite all the advantages the micromachined capacitors suffer from mechanical thermal vibration, thus causing an additional output frequency jitter, or phase noise, when used for VCO tuning. This effect will be manifested in detail in Chapter 6.

The fabricated devices achieve a 15% tuning range for a 3 V tuning voltage, limited by the parasitic capacitances. An S-parameter measurement shows a quality factor of 62 at 1 GHz and is limited by the resistive loss in the interconnect traces. An improved performance in Q value and tuning range are

expected by employing copper as the structural material and new device topologies.

Chapter 5

Three-Dimensional Monolithic Coil Inductors

5.1 Introduction

This chapter describes three-dimensional (3-D) coil inductors fabricated on silicon substrates, targeted for use in monolithic high-performance wireless communication circuits. It starts with an overview of conventional on-chip spiral inductors currently available in a standard IC process and illustrates the key limitations hindering the performance of these devices. Then a new solution based upon a 3-D coil inductor structure is proposed to alleviate the conventional limitations, resulting in a significantly improved performance. Device characteristics and fabrication technology are described. Measurement results from fabricated inductors are presented. Finally, future processing improvements for the 3-D coil inductors are proposed.

5.2 Conventional Monolithic Inductors

On-chip spiral inductors are widely used as monolithic inductors in many RF applications [52, 53, 54]. Figure 5.1 presents a top view of a typical spiral inductor, which consists of a winding metal trace deposited on top of a semiconductor substrate.

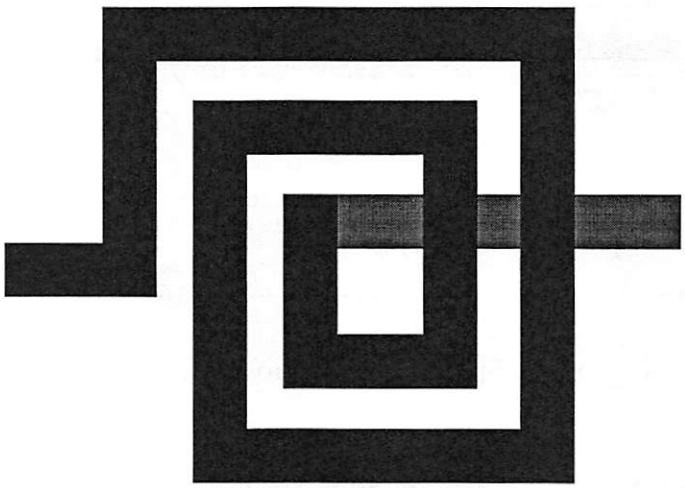


Figure 5.1: Spiral Inductor

The device normally occupies an area of a few hundred micrometers square, achieving inductance values between 1 nH and 10 nH [55]. In a standard IC process, aluminum or copper is used for the spiral trace with a typical thickness between 2 μm and 5 μm. This is commonly achieved through connecting multiple levels of interconnects [56].

While many RF circuits make use of on-chip spiral inductors, the poor quality factors, around 3 at 1 GHz, preclude their use for functions where high Q is critical such as low phase noise RF VCOs, low-loss impedance matching

networks, and high-efficiency power amplifiers. The low Q values are mainly caused by the substrate loss and metal resistive loss at high frequencies. The substrate loss can be explained in Figure 5.2, which illustrates the cross section of the spiral inductor shown in Figure 5.1.

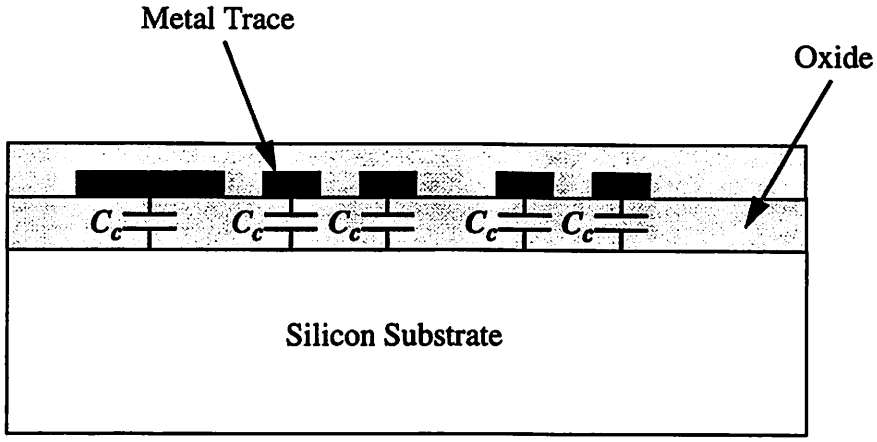


Figure 5.2: Spiral Inductor Cross Section View

The inductor metal traces are isolated from the silicon substrate by a silicon oxide layer with a typical thickness between 1 μm and 5 μm. These metal traces are thus capacitively coupled to the substrate through C_cs. They allow high-frequency currents, ideally flowing inside the spiral inductor, to flow into the substrate, causing resistive power dissipation resulting in a reduced quality factor. Furthermore, the high-frequency current circulating inside the spiral trace generates a magnetic field penetrating through the substrate as depicted in Figure 5.3. The field direction is determined by the current direction. This magnetic field in turn produces an eddy current in the substrate, introducing another loss contributor to further lower the quality factor. The field lines also penetrate through the spiral metal traces producing a counteracting magnetic field. This effect reduces the total inductance value; hence, the Q factor.

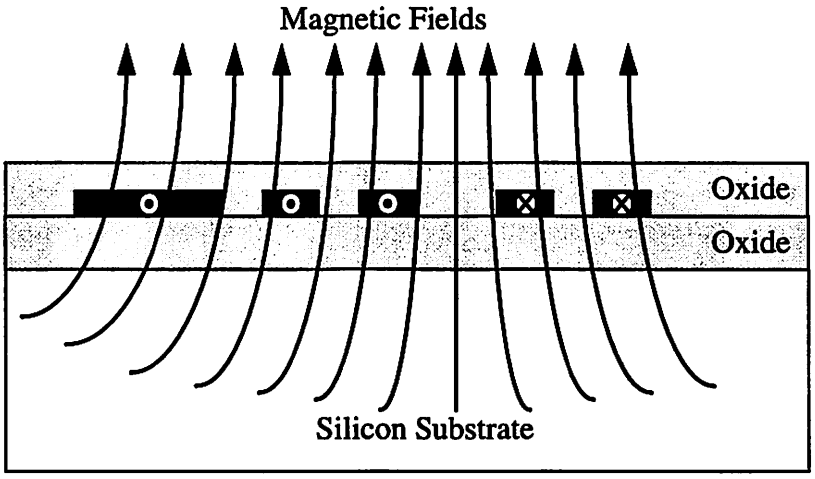


Figure 5.3: Magnetic Field inside Spiral Inductor

To minimize substrate loss due to the capacitive coupling, spiral inductors fabricated on silicon wafers with the substrate partially removed underneath were proposed as shown in Figure 5.4 [57].

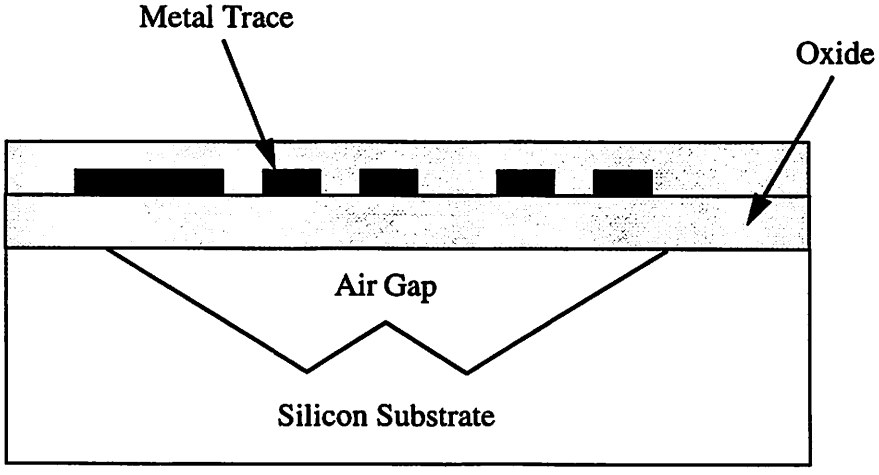


Figure 5.4: Spiral Inductor with Partial Substrate Removed

This approach substantially reduces the coupling capacitance, leading to an improved Q value around 5 at 1 GHz limited, however, by metal resistive loss in the aluminum trace. Replacing aluminum interconnects with copper will further reduce the resistive loss, thus improving the Q value. Partially etching the silicon substrate while protecting the nearby integrated electronics, however, remains a major concern for IC integrity and reliability.

Recently, a patterned ground shield was employed between a spiral inductor and silicon substrate to enhance the Q performance by 33% through decoupling the inductor from the substrate [58]. However, the shielded inductor suffers from a reduced self-resonant frequency due to the increased device parasitic capacitance, hindering their use for multi-Gigahertz applications. In the next section, a new solution based upon a surface three-dimensional coil inductor is proposed. The device avoids the limitations from the conventional spiral inductors and hence achieves high Q values and self-resonant frequencies required for wireless communication applications.

5.3 Three-Dimensional Coil Inductors

Figure 5.5 presents an SEM micrograph of a fabricated 3-D coil inductor on a silicon substrate. The fabrication process will be outlined in Section 5.4. This device consists of four-turn 5 μm thick and 50 μm wide copper traces electroplated around an insulating core. The core has a cross section area of approximately 650 μm by 500 μm. Compared to spiral inductors, this geometry minimizes the coil area which is in close proximity to the substrate and hence the capacitive coupling. Thus it results in a reduced substrate current loss at high frequencies and also an increased self-resonant frequency.

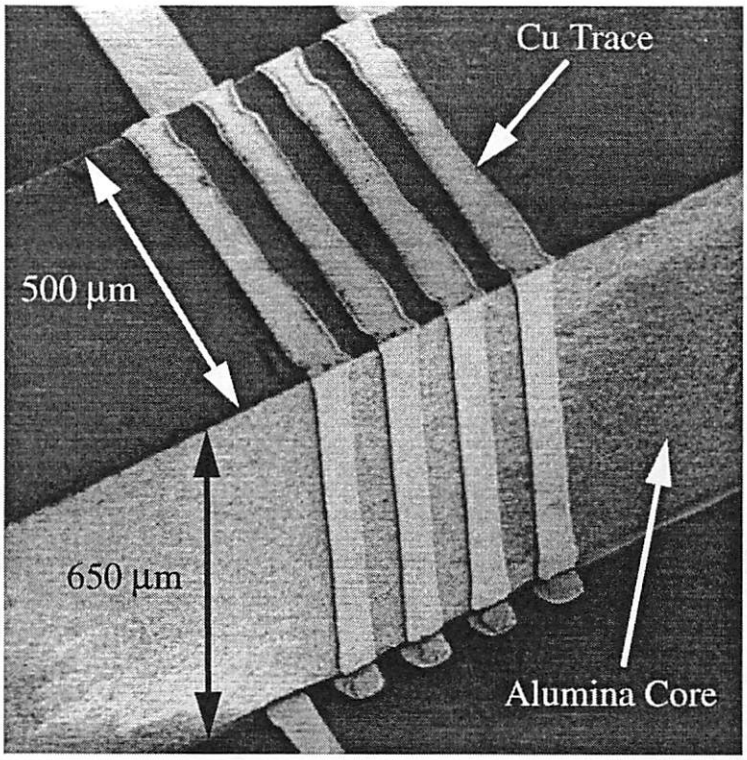


Figure 5.5: SEM of a Fabricated 3-D Coil Inductor

Furthermore, the magnetic field lines of this 3-D coil inductor are mostly distributed in the air around the device rather than penetrating the silicon substrate as shown in Figure 5.6, substantially lowering the induced eddy current and thus ensuring a high Q at high frequencies. The resulting field also significantly minimizes the counteracting magnetic field that exists in conventional spiral inductors.

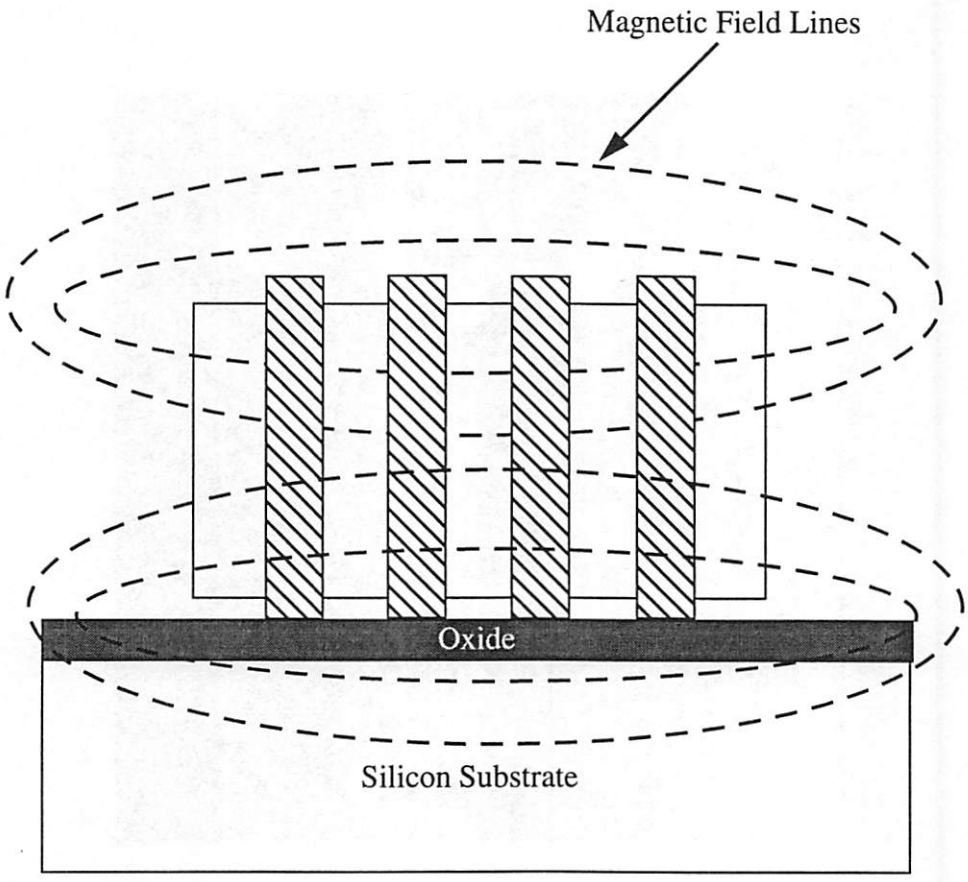


Figure 5.6: 3-D Coil Inductor Magnetic Field Distribution

Copper is selected as the trace metal for its low sheet resistance, critical for achieving a high Q factor, and its deposition simplicity through an electroplating process illustrated in Section 5.4. The 5 μm trace thickness is selected for this design because of the copper skin depth around 2.4 μm at 1 GHz. An increased metal thickness will further minimize the resistance. However, thicker metal traces are not used due to current processing constraints discussed in the following section. The 50 μm metal width represents a compromise between the trace resistance and capacitance to the substrate. A 50

μm line spacing is used to avoid processing difficulties in this conservative design.

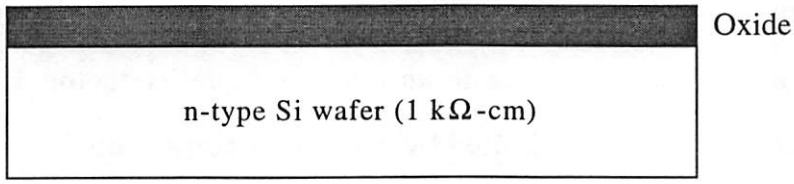
Alumina is chosen as the core material because of its negligible loss tangent at high frequencies with a typical value around 30×10^{-4} at 1 GHz [59], another key parameter to ensure a high Q. The core width of 500 μm is found experimentally to be the minimum that avoids tilting during its attachment to the bottom copper traces. Its height of 650 μm is limited by the thickness of a commercially available alumina sheet. A higher 3-D structure will achieve a larger inductance value without significantly increasing the capacitance coupling to substrate, thus leading to an improved quality factor. However, the ultimate device height will be limited by packaging constraints.

With the device dimensions described above, three types of inductors with one, two and four turns are fabricated through the experimental process. Because the device cross-section dimension is large compared to the length, the classical formula for solenoidal inductance calculation cannot be applied directly. The inductance values are thus estimated by using Maxwell 3D Field Simulation [60]. The simulation predicts approximately 4 nH, 7.5 nH and 13.5 nH for the three designs, which match closely to the measured values as presented in Section 5.5. These inductance values are adequate for RF applications at Gigahertz frequencies. Due to the limitation of the simulator, the 3-D inductors are simulated without including any substrate effects. Thus, the simulated device resistances only represent the metal trace resistances, which are approximately 0.4 Ω, 0.86 Ω and 1.8 Ω for the one, two and four-turn designs at 1 GHz respectively, corresponding to ideal Q factors of 63, 55 and 47. The simulation setup is shown in Appendix B. The measured inductor Q factors,

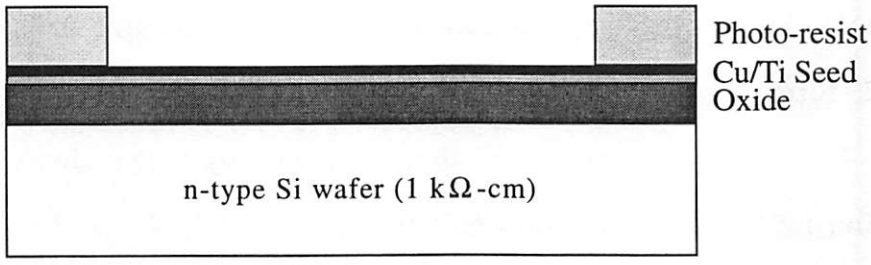
however, are less than the ideal values due to additional contact resistances and substrate effects as described in Section 5.5.

5.4 Fabrication Process

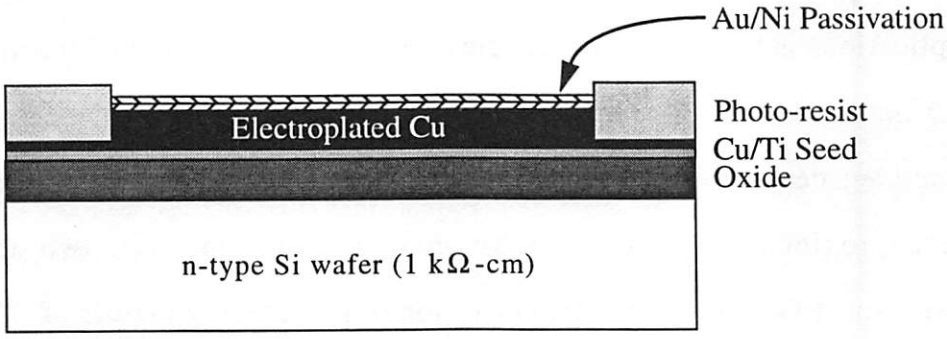
This section presents the fabrication technology for implementing the three-dimensional coil inductors. The experimental devices have been fabricated on a bare silicon wafer. Figure 5.7 illustrates the process flow.



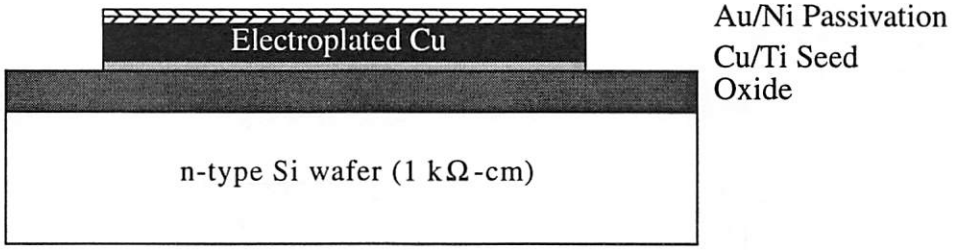
(a)



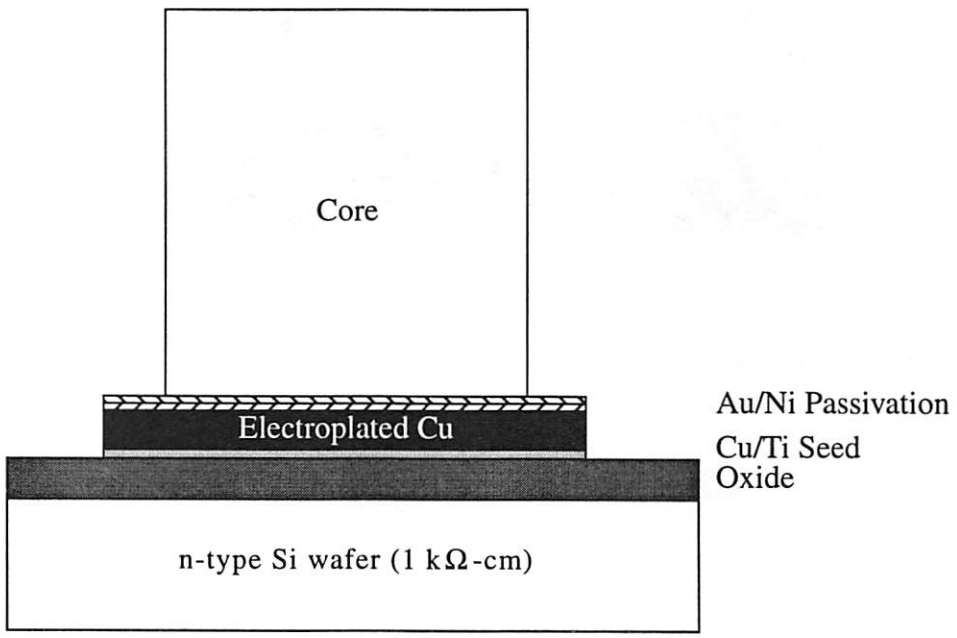
(b)



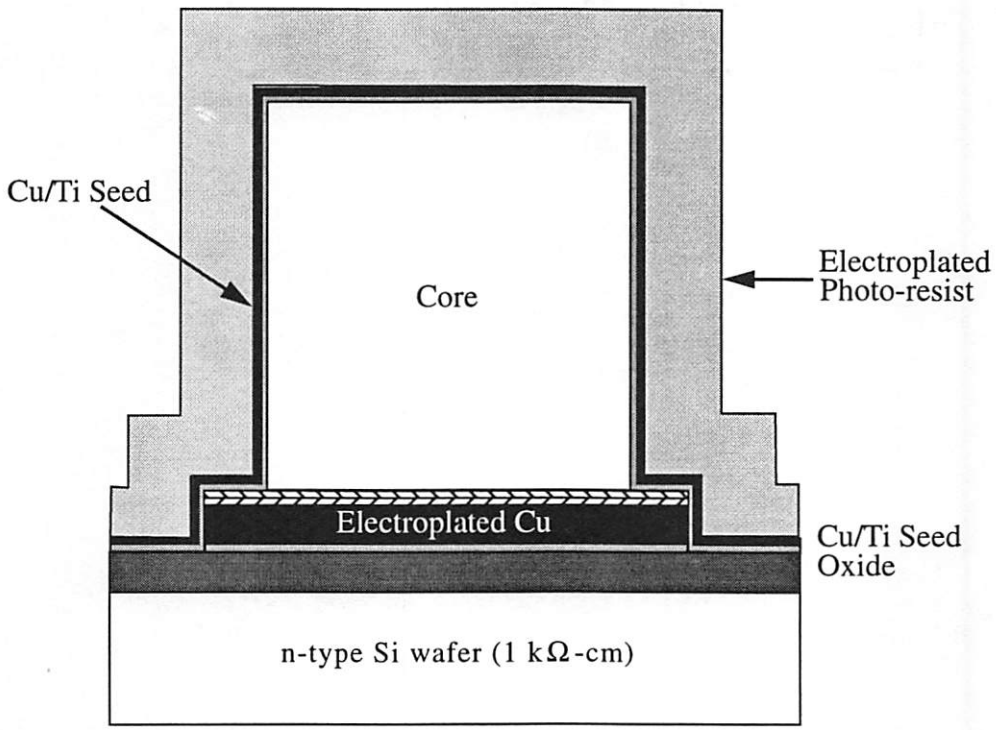
(c)


Electroplated Cu
n-type Si wafer (1 kΩ-cm)
Au/Ni Passivation
Cu/Ti Seed
Oxide

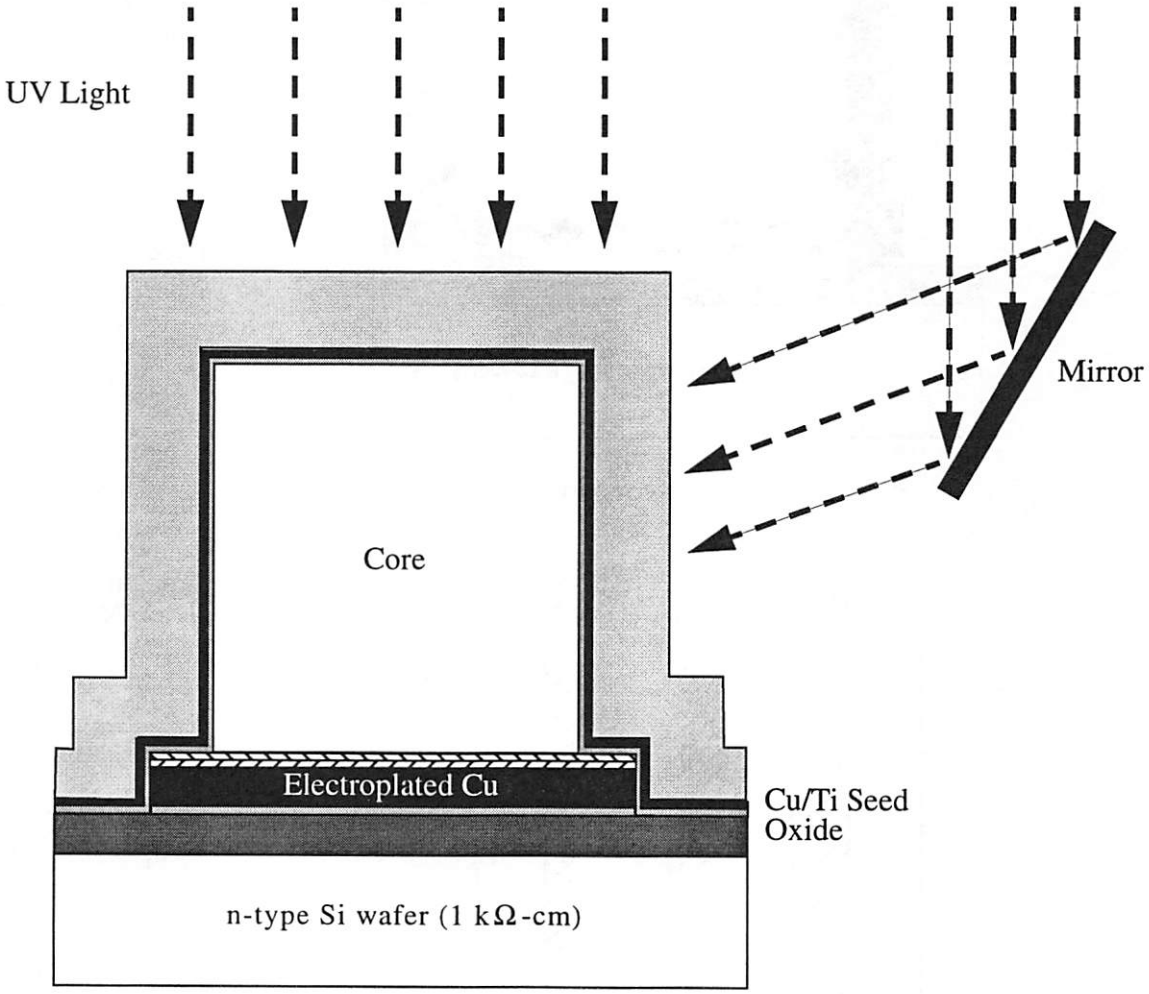
(d)


Core
Electroplated Cu
n-type Si wafer (1 kΩ-cm)
Au/Ni Passivation
Cu/Ti Seed
Oxide

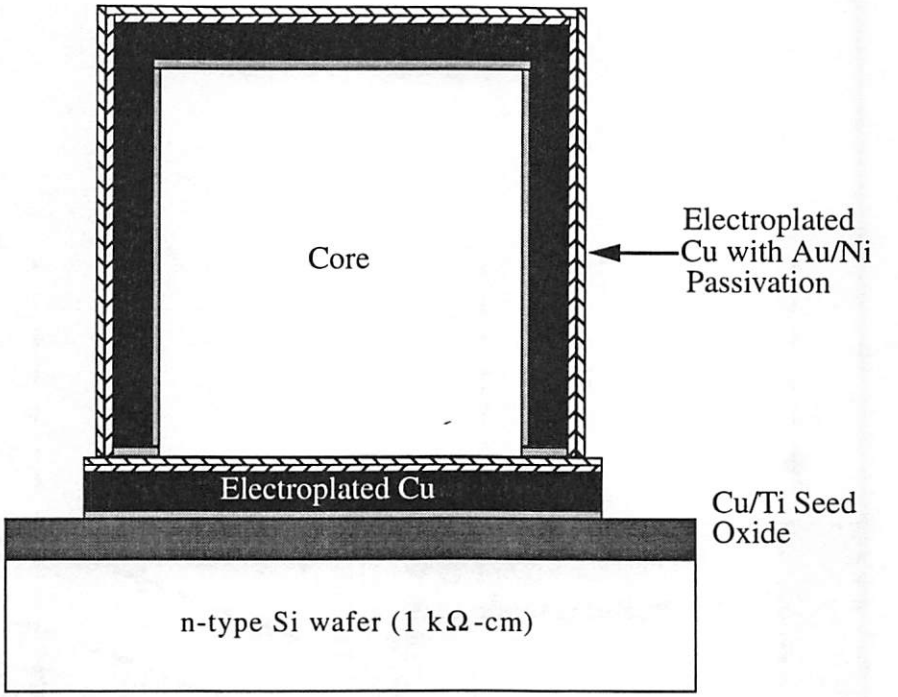
(e)


Cu/Ti Seed
Core
Electroplated
Photo-resist
Electroplated Cu
Cu/Ti Seed
Oxide
n-type Si wafer (1 kΩ-cm)

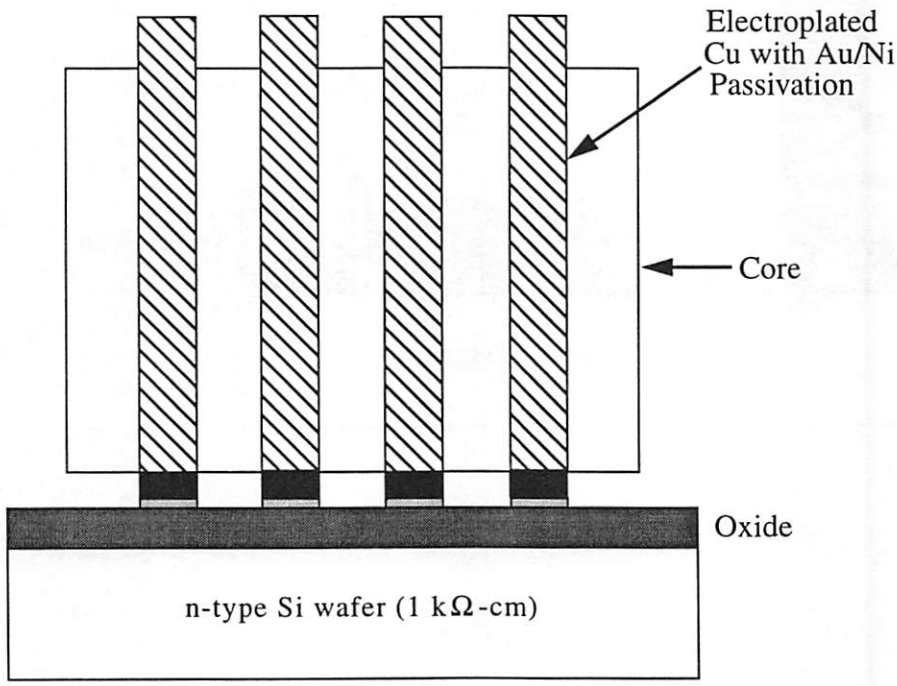
(f)


UV Light
Mirror
Core
Electroplated Cu
Cu/Ti Seed
Oxide
n-type Si wafer (1 kΩ-cm)

(g)



Cross Section



Side View

(h)

Figure 5.7: Fabrication Process Flow

First, the wafer is passivated with a 5 μm thick low-temperature oxide (Figure 5.7a). This layer isolates the 3-D inductor to be fabricated on top away from the silicon substrate. An increased oxide thickness will further minimize the capacitive coupling. However, a 5 μm thickness is chosen because it represents a typical thickness available in a standard IC process.

Then the bottom traces of the inductor are fabricated. For this purpose, a 500 Å titanium and 3000 Å copper seed layer are sputtered and covered by a 8 μm thick electroplated photoresist. This photoresist layer, however, can also be deposited through a spin-on technique. The 8 μm thickness is chosen due to the current photolithography constraint, thus limiting the thickness of the electroplated copper. The pattern of the bottom metal traces are transferred photolithographically. Contacts are opened after developing the resist (Figure 5.7b). This step is followed by a selective electroplating of 5 μm copper traces. To prevent oxidation, the copper is passivated with two 1000 Å layers of electrolytic nickel and gold (Figure 5.7c). Finally the photoresist and copper/ titanium seed layer are removed with a wet etch step, leaving the bottom metal traces of the inductor on the substrate (Figure 5.7d).

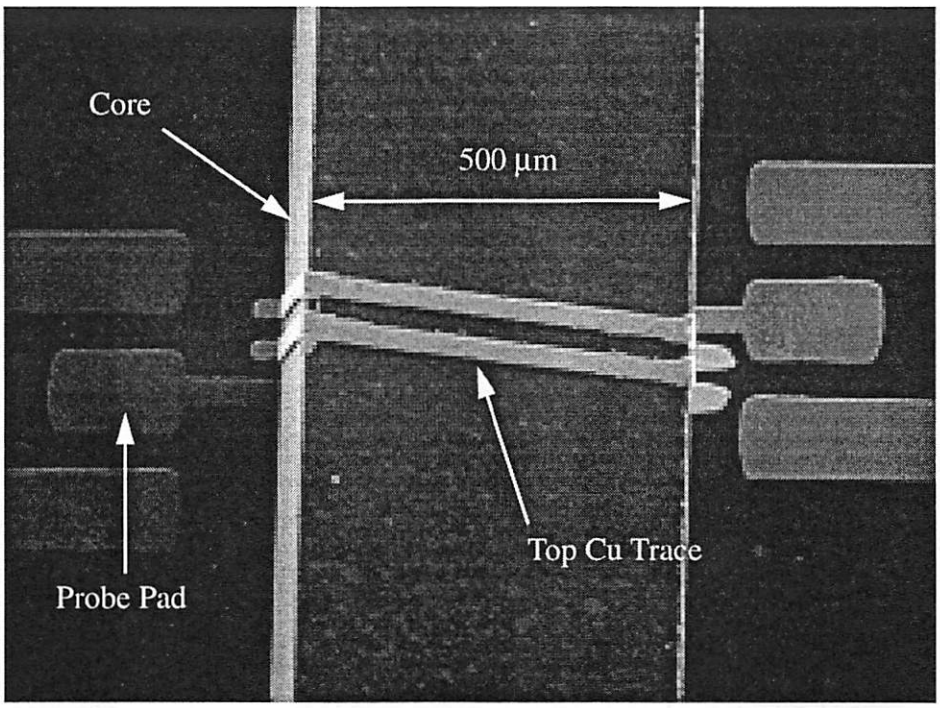
The core of the inductor is formed from an alumina sheet, which is diced into 500 μm wide strips. A 2% width accuracy is achieved by using a thin diamond grit blade on a commercial dicing saw. The strips are then manually centered on the bottom copper traces and baked at 170 °C for 30 seconds, resulting in an adhesion to the substrate through adhesive materials placed at both ends of the core (Figure 5.7e). This manual placement technique is employed for fabricating the prototype devices. Batch fabrication methods for implementing the inductor cores will be outlined in Section 5.6.

To fabricate the copper traces on the side and the top of the alumina core, the same process as for the bottom traces is used (Figure 5.7f). The photoresist electroplating step here, however, is critical because it can conformally cover a complex surface such as the inductor core. The resist is exposed with a three-dimensional maskless direct-write laser lithography tool as illustrated in Figure 5.7g [61]. The laser beam can directly expose the resist on top of the core, and it is reflected by a mirror system to expose the sidewall. After developing the laser-exposed resist, 5 μm thick copper traces are then electroplated along the sidewall and on top of the core. Electrolytic nickel and gold are deposited afterwards to prevent copper oxidation, followed by etching away photoresist and copper/titanium seed layer to complete the fabrication process. The final inductor is illustrated in Figure 5.7h.

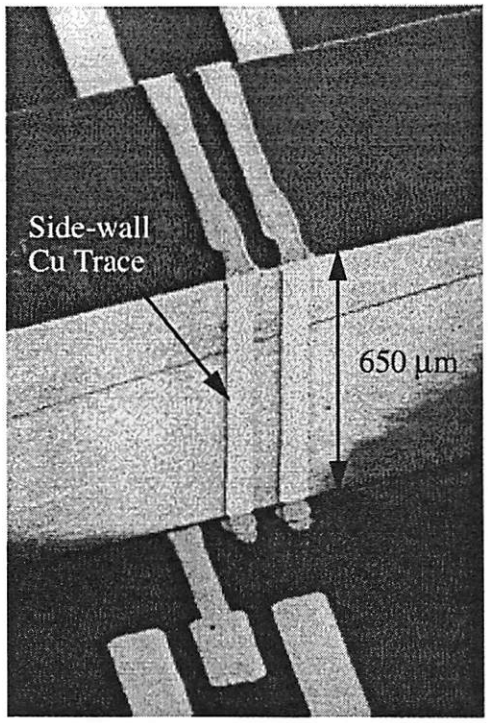
Because of the low processing temperature, the inductor can be fabricated on top of wafers with completed electronics without sacrificing the active device performance. This is particularly crucial in RF applications where the availability of the most recent IC technology is a key competitive advantage.

5.5 Measurement Results

Figure 5.8 shows SEM micrographs of a fabricated two-turn 3-D inductor. The coil area above the silicon substrate is approximately 250 μm by 500 μm, comparable to that of a typical spiral inductor achieving a similar value. The two sets of ground-signal-ground probe pads are employed for measuring the device two-port S-parameters.



Top View



Side View

Figure 5.8: SEMs of a Two-Turn 3-D Coil Inductor

Figure 5.9 presents the measured quality factor and inductance value as a function of frequency after de-embedding the parasitics from the probe pads. The device achieves an 8.2 nH inductance value with a Q factor of 16 at 1 GHz. This quality factor is substantially higher than that of a typical spiral inductor.

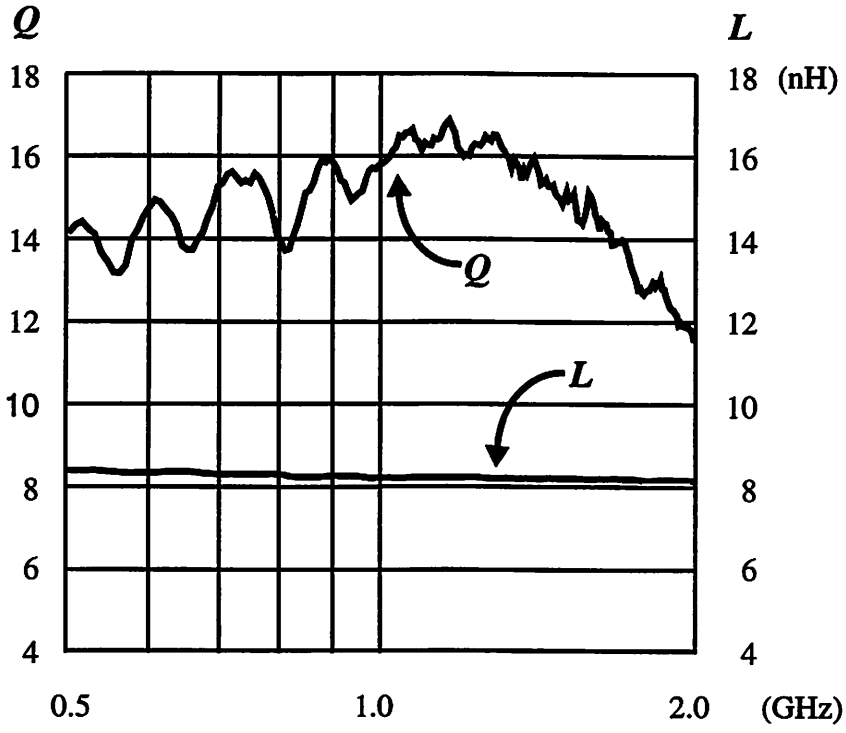


Figure 5.9: Measured Q and L for Two-Turn Coil Inductor

Figure 5.10 shows an SEM of a one-turn 3-D coil inductor achieving an inductance of 4.8 nH with a high Q value of 30 at 1 GHz, as illustrated in Figure 5.11. This performance matches or exceeds that of discrete counterparts and is at least an order of magnitude larger than that of a conventional spiral inductor implemented in a standard IC process.

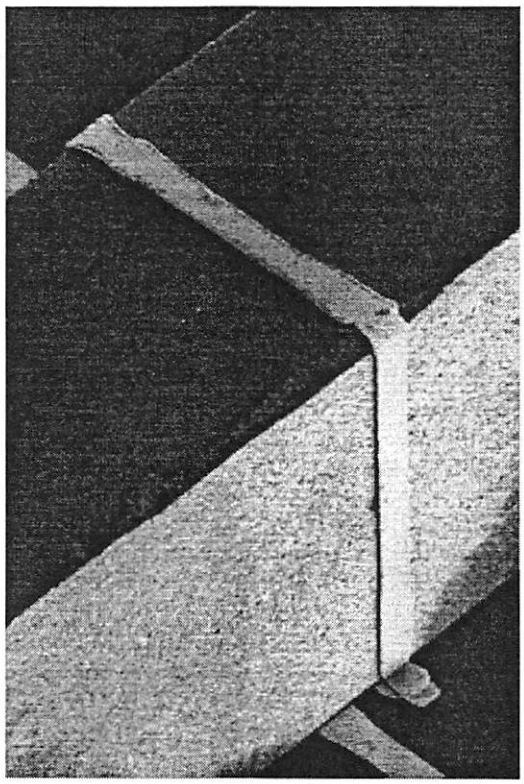


Figure 5.10: SEM of a One-Turn 3-D Coil Inductor

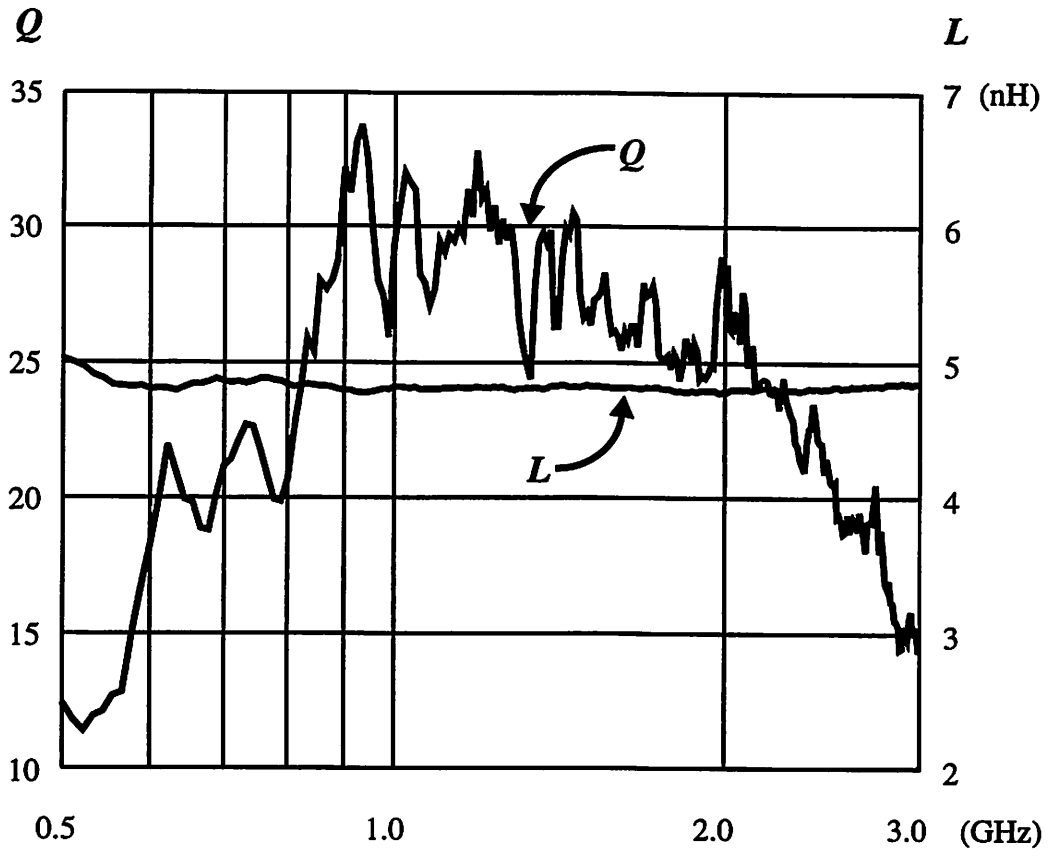


Figure 5.11: Measured Q and L for One-Turn Coil Inductor

Table 5.1 summarizes the performance of the fabricated inductors. The achieved performance represents a substantial improvement offered by the 3-D structures compared to the conventional spiral inductors. The devices are, therefore, suitable for building high-performance wireless communication circuits such as low phase noise RF VCOs, low-loss matching networks, and high-efficiency power amplifiers.

	one-turn	two-turn	four-turn
Inductance	4.8 nH	8.2 nH	13.8nH
Q @ 1 GHz	30	16	16
f_{res}	> 10 GHz	> 10 GHz	> 5 GHz
Silicon Area	150 μm x 500 μm	250 μm x 500 μm	450 μm x 500 μm

Table 5.1: Performance Summary Table for Fabricated 3-D Coil Inductors

The current fabrication process, however, does not yield reliable contacts between the vertical and bottom metal traces due to a finite air gap between the alumina core and bottom traces, resulting in open connections in some fabricated devices. A number of functional components also exhibit an increased contact resistance degrading the Q values. The new batch fabrication methods proposed in the following section will eliminate this problem, leading to a further improved device performance and yield.

5.6 Proposed Device Improvements

The current process of manually forming alumina cores is incompatible with batch fabrication. It also causes a finite air gap between the core and the bottom metal trace, resulting in a low yield. This problem can be eliminated with the following proposed new processing techniques. Liquid aerogel can potentially be used as an alternative material for the inductor core since it is an insulator and has a low loss tangent at high frequencies. This material can be poured into a mold which defines the core dimensions and is properly aligned to the substrate wafer. After drying the aerogel and removing the mold, inductor cores are formed without any air gap underneath them.

A 3-D air-core coil inductor can also be achieved by using a sacrificial polyimide core. Polyimide materials can be deposited up to a thickness around a hundred micrometers by using spin-on techniques and patterned photolithographically to form contact holes, through which vertical metal traces can be electroplated. After completing the coil connections, the polyimide core can be etched away through an oxygen-based plasma dry etch, resulting in an air-core coil inductor. These proposed fabrication methods are not only compatible with batch fabrication using standard IC processing equipment, but can also improve the device yield and performance.

5.7 Summary

The 3-D high-Q coil inductors are proposed as the key components to implement monolithic high-performance wireless communication circuits. The key advantage of the 3-D microstructure is to minimize the device capacitive coupling to the substrate and the eddy current loss, thus achieving a superior performance compared to the conventional spiral inductors. While experimental devices have been fabricated on bare silicon wafers, all fabrication steps are compatible with standard IC technology, thus amenable to monolithic integration with active devices.

The fabricated devices have obtained inductance values adequate for implementing RF ICs. An S-parameter measurement shows that a high quality factor up to 30 has been achieved at 1 GHz. This matches or exceeds the performance of discrete counterparts and is at least an order of magnitude larger than that of a conventional spiral inductor. Improved device yield and performance are expected through the proposed processing modifications.

Chapter 6

LC Oscillator Analysis

6.1 Introduction

This chapter presents the analysis of a LC-tuned oscillator. Oscillator design considerations including a reliable oscillation start-up and a well-behaved steady-state oscillation amplitude and frequency are described. The classical phase noise in a conventional LC oscillator is illustrated. However, in a micromachine-based LC-tuned oscillator an additional phase noise is generated due to the mechanical thermal vibration of the tunable capacitors. This phase noise is then explained. Finally, a comparison is made between the two phase noises with proposed suppression methods.

6.2 Oscillator Design Considerations

In this section, a sinusoidal oscillator based upon a parallel LC-tuned tank is analyzed. The oscillator design considerations including a reliable

oscillation start-up and a well-behaved steady-state oscillation amplitude and frequency are presented.

6.2.1 Oscillator Start-Up

The basic requirement for a sinusoidal oscillation build-up is the existence of a pair of complex conjugate poles:

$$P_{1,2} = \alpha \pm j\beta, \tag{6-1}$$

in the right half of the s-plane; that is α must be larger than zero. The system is then unstable about its operating point and produces a growing sinusoidal signal:

$$V(t) = V_o e^{\alpha t} cos(\beta t), \tag{6-2}$$

when subjected to an excitation (due to power supply turn-on transients or noise in the circuit), where V_o is determined by the system initial conditions. The amplitude of this signal will continue to grow until it starts to limit due to the system nonlinearities or other limiting mechanisms.

An oscillation build-up can be predicted from the initial linear behavior of an oscillator by using a feedback model or a negative resistance model. One model is preferred over the other depending upon the oscillator configuration. In this section, the feedback model approach is chosen for the parallel LC-tuned oscillator analysis.

Figure 6.1 shows a general representation of an oscillator feedback method.

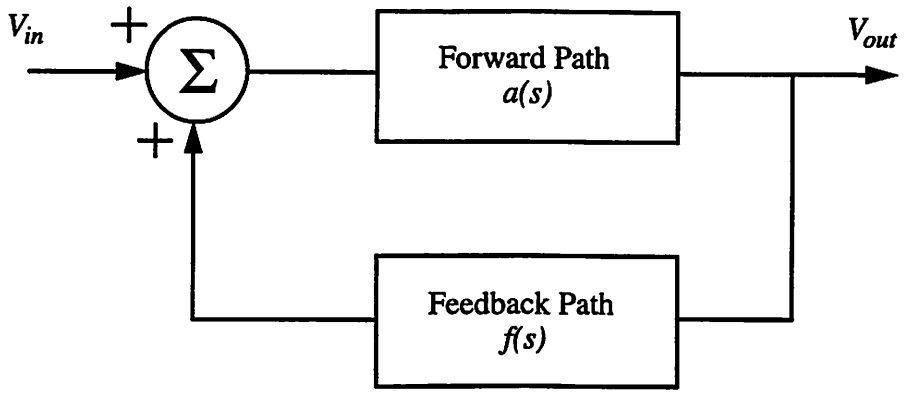


Figure 6.1: An Oscillator Feedback Model

The transfer function from V_{in} to V_{out} can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a(s)}{1 - a(s)f(s)}, \tag{6-3}$$

where the minus sign in the denominator is due to the positive feedback and v_{in} represents any excitation signal. The poles of the system thus can be determined from the roots of the characteristic equation:

$$1 - a(s)f(s), \tag{6-4}$$

where $a(s)f(s)$ is defined as the oscillator loop gain.

For a LC-tuned oscillator, the feedback model can usually be presented in Figure 6.2, where a transconductance amplifier driving a parallel LC loading network in the forward path is enclosed by a positive feedback consisting of an n:1 step-down transformer. An unity gain feedback can be modeled with $n = 1$.

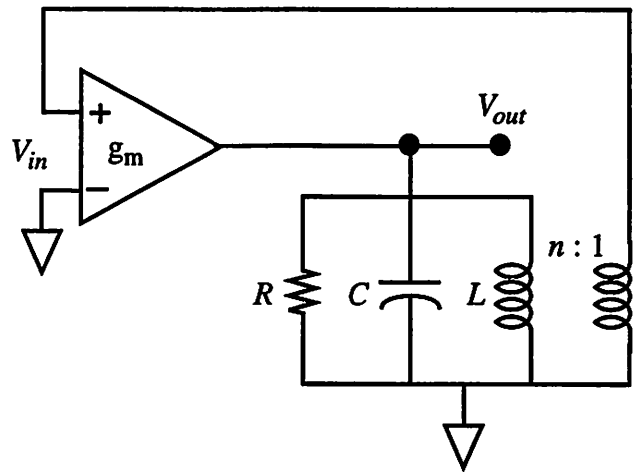


Figure 6.2: Feedback Model for Parallel LC-Tuned Oscillator

The corresponding transfer function from V_{in} to V_{out} thus can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m Z_L}{1 - g_m Z_L \frac{1}{n}}, \tag{6-5}$$

where Z_L is the impedance of the LC loading network and is found as:

$$Z_L = \frac{Ls}{1 + \frac{L}{R}s + LCs^2}. \tag{6-6}$$

Substituting (6-6) into (6-5), the transfer function can be further expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m Ls}{1 + \frac{L}{R}\left(1 - \frac{g_m R}{n}\right)s + LCs^2}. \tag{6-7}$$

It can be shown that Equation (6-7) has a pair of complex conjugate poles:

$$P_{1,2} = -\frac{a}{2} \pm j\frac{1}{2}\sqrt{4b - a^2}, \tag{6-8}$$

where

$$a = \frac{1}{RC}\left(1 - \frac{g_m R}{n}\right), \tag{6-9}$$

and

$$b = \frac{1}{LC} = \omega_o^2. \tag{6-10}$$

For theses poles to be in the right half of the s-plane, $(1 - g_m R/n)$ needs to be negative, thus requiring $g_m R/n$ to be greater than unity. This term is also the small-signal loop gain around the oscillator at the LC tank resonant frequency, ω_o^2. With the poles in the right half of the s-plane, an exponentially growing sinusoidal signal is therefore produced. In a typical oscillator design, the small-signal loop gain is usually set around 3~4 to ensure a reliable start-up.

6.2.2 Oscillator Steady-State Behavior

The initial waveform, $V(t) = V_o e^{\alpha t} cos(\beta t)$, will continue to grow until it drives the active devices into the nonlinear region. In this region, the device transconductance starts to decrease monotonically due to the increased driving signal amplitude. The oscillator ultimately reaches its steady-state when the loop gain, $g_m R/n$, becomes unity where g_m represents the large-signal transconductance of the active device. At this condition, the complex conjugate poles are onto the $j\omega$-axis of the s-plane, resulting in a steady-state waveform:

$$V(t) = V_A cos(\omega_o t). \tag{6-11}$$

The steady-state oscillation amplitude, V_A, for a given oscillator is then determined by the quiescent current consumption, initial loop gain, LC tank impedance, transformer ratio, and device inherent nonlinearities [62, 63].

In the steady-state oscillation, the circuit supplies its own input signal. Therefore, the total loop phase shift must be 0°. Assuming there is no phase shift

through the transconductance amplifier and transformer, the circuit must oscillate at the resonant frequency of the LC tank because the tank provides a 0° phase shift only at its resonance.

6.3 Oscillator Phase Noise

The oscillator phase noise is a key parameter for high-performance communication systems. In a conventional LC oscillator, the electrical thermal noise, $1/f$ noise, and noise from the supply voltage and substrate contribute to the final phase noise. However, in a micromachine-based LC-tuned oscillator, an additional phase noise due to the mechanical thermal vibration of the tunable capacitors is generated. In this section, both phase noises are manifested and compared. Methods for minimizing these noise contributions are then proposed.

6.3.1 Phase Noise from Electrical Noise Sources

In a conventional LC-tuned oscillator, the phase noise is contributed by the various noise sources in the circuit as mentioned above. Assuming the electrical thermal noise is dominant, the resulting phase noise profile decays at 20 dB per decade away from the carrier frequency [31]. This behavior can be obtained by applying a transfer function approach based on a linear time-invariant (LTI) system as follows. For the parallel LC-tuned oscillator shown in Figure 6.2, the impedance of the tank, for $\Delta\omega \ll \omega_o$, is expressed as:

$$Z(\omega_o \pm \Delta\omega) = \frac{R}{1 + j2Q\frac{\Delta\omega}{\omega_o}}, \tag{6-12}$$

where Q and ω_o are the loaded quality factor and resonant frequency of the LC tank respectively. For the steady-state oscillation, the condition of $g_m R/n = 1$ must be satisfied. Therefore, for a parallel current source, i_{in}, shown in Figure 6.3, the closed-loop transfer function of the oscillator can be expressed as:

$$H(\Delta\omega) = \frac{v_{out}(\omega_o + \Delta\omega)}{i_{in}(\omega_o + \Delta\omega)} = -jR\frac{\omega_o}{2Q\Delta\omega}. \tag{6-13}$$

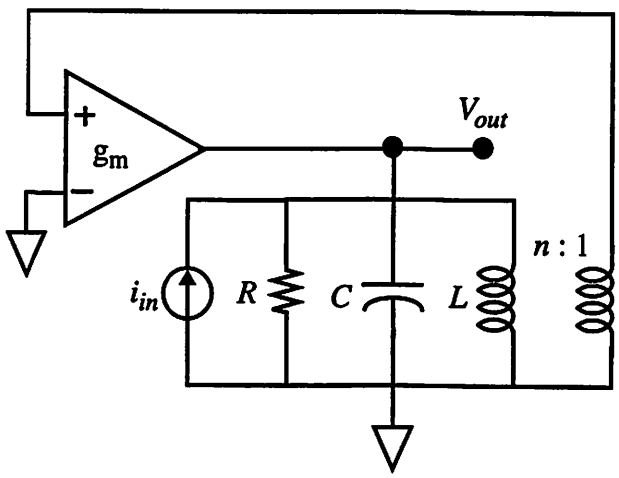


Figure 6.3: Parallel LC-Tuned Oscillator with Parallel Current Source i_{in}

The equivalent parallel resistance of the tank has an equivalent mean square noise current density of $i^2_{nR}/\Delta f = 4kT\frac{1}{R}$, positioned at the same location as i_{in} shown in Figure 6.3. In addition, the active device noise usually contributes a significant portion of the total noise in the oscillator. It is common to combine all the noise sources into one effective noise source, expressed in terms of the resistor noise with a multiplicative factor, F, known as the device excess noise factor. This factor can also be expressed as:

$$F = \frac{i^2_{nActive}/\Delta f + i^2_{nR}/\Delta f}{i^2_{nR}/\Delta f}, \tag{6-14}$$

where $i^2_{nActive}/\Delta f$ represents the noise current spectral density from the active devices. The total equivalent mean square noise current density is therefore found as:

$$i^2_n/\Delta f = 4FkT\frac{1}{R}. \tag{6-15}$$

It is generally difficult to calculate F *a priori.* One important reason is that much of the noise in a practical oscillator arises from periodically-varying processes [32]. As a result, F is usually used as *a posteriori* fitting parameter on measured data and is found typically between 1 and 10. Minimizing this factor is still an open area for research.

Using the above effective noise current density, the oscillator phase noise thus can be calculated as:

$$S_\theta(f_m)_{Electrical} = \frac{\overline{v^2_{noise}}}{v^2_{signal}} = \frac{\frac{1}{2}|H(f_m)|^2(i^2_n/\Delta f)}{\frac{1}{2}V^2_{amplitude}} = \frac{FkT}{2P_{rf}Q^2}\left(\frac{f_o}{f_m}\right)^2, \tag{6-16}$$

where P_{rf} is the oscillator RF output power, f_o, and f_m are the oscillation frequency and offset frequency respectively. The factor of 1/2 in the noise power arises from separating the contribution of amplitude noise from phase noise. The above expression excludes the contribution from the device $1/f$ noise and noise from the supply voltage and substrate. In practice, $1/f$ noise from the electronics will cause the phase noise profile to increase at 30 dB per decade as the offset frequency approaches to zero, as shown in Figure 6.4 on the logarithmic scale. The offset frequency of $\Delta f_{1/f^3}$ is the corner frequency between the $1/f^3$ and $1/f^2$ regions. This is usually determined by the device $1/f$ noise characteristics and

oscillator topology. Minimizing the $1/f$ noise contribution remains an open area for research.

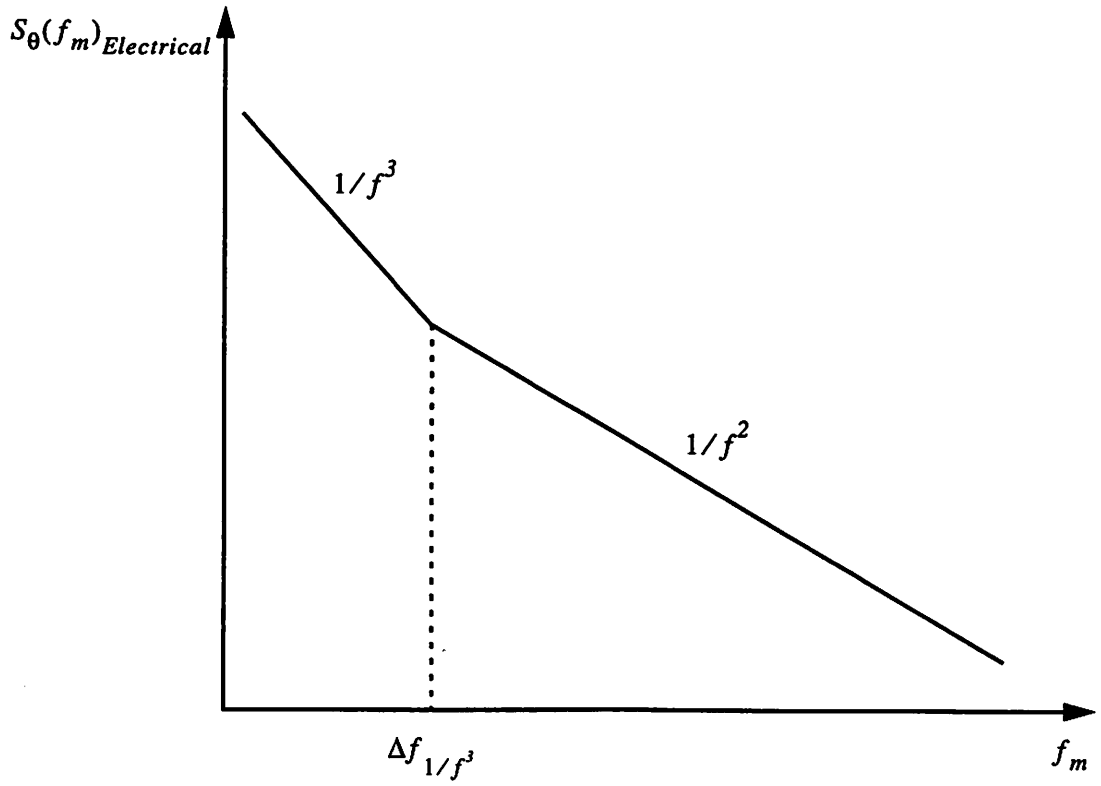


Figure 6.4: Phase Noise Profile for Conventional Oscillator

From Equation (6-16), it is apparent that a low phase noise performance can be achieved through increasing Q and P_{rf}. However, in a practical design the RF output power from an oscillator is usually limited by the available voltage swing. Therefore, maximizing the Q factor is the key step to minimize the phase noise. Based upon the phase noise expression, if a 1 GHz oscillator, with an F value of 10, develops a 2 V peak to peak swing over a 1 kΩ tank impedance, then a loaded Q value of at least 12 is required in oder to achieve a phase noise below -136 dBc/Hz at 3 MHz offset frequency, the requirement for GSM cellular telephony application.

6.3.2 Brownian-Motion-Induced Phase Noise

Besides the classical phase noise described in the previous section, a micromachine-based LC-tuned oscillator introduces an additional phase noise due to the mechanical-thermal vibration, also known as the Brownian motion, from the variable capacitors. The vibration of the suspended plates causes variation in the capacitance value; hence, jitters (or phase noise) in the output frequency. This additional phase noise can be expressed as:

$$S_{\theta}(f_m)_{Mechanical} = \frac{x_n^{\,2}(f_m)}{8\left(\frac{1+\alpha}{\alpha}\right)^2 N x_o^{\,2}}\left(\frac{f_o}{f_m}\right)^2, \tag{6-17}$$

where $x_n^{\,2}(f_m)$ is the displacement noise power spectral density of the suspended plate described by Equation (4-14), x_o is the nominal air gap of the variable capacitor, N is the number of the parallel-connected micromachined capacitors, α is the ratio between the nominal tank tunable capacitance and its parasitics, f_o, and f_m are the oscillation frequency and offset frequency of interest respectively. The derivation of this phase noise is presented in Appendix A. The significance of this noise is explained below with typical performance values.

The displacement noise power spectral density of the micromachined capacitor is constant below the mechanical resonant frequency, ω_n, and decays at 40 dB per decade above ω_n as shown in Figure 4.10. Therefore, the resulting phase noise profile decreases at 20 dB and 60 dB per decade below and above the offset frequency of $\omega_n/2\pi$, respectively, as illustrated in Figure 6.5 on a logarithmic scale. At $\omega_n/2\pi$ offset frequency the phase noise is enhanced due to the peaking in the capacitor displacement noise power spectral density at the mechanical resonance.

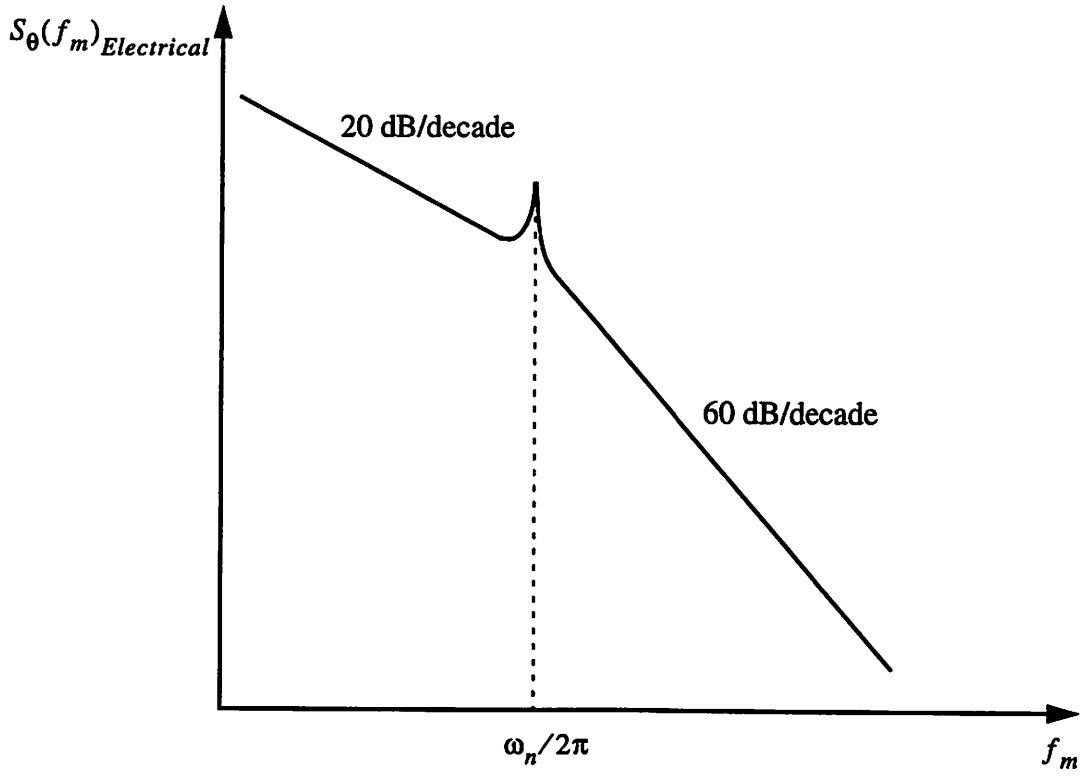


Figure 6.5: Brownian-Motion-Induced Phase Noise Profile

Based upon Equations (4-14) and (6-17), the Brownian-motion-induced phase noise can be determined at various offset frequencies. For a typical design condition of x_o = 1.5μm, m = 100ng, $Q_M \cong 1$ at 1 atm, ω_n = (2π)(30KHz), N = 4, $\alpha \cong 0.5$, and f_o = 1GHz, the phase noise at offset frequencies of 10 KHz, 100 KHz, and 3 MHz are calculated and summarized in Table 6.1, where they are also compared along with the corresponding classical phase noise from the oscillator example given in Section 6.3.1.

f_m	10 KHz	100 KHz	3 MHz
$S_\theta(f_m)_{Mechanical}$	-64 dBc/Hz	-105 dBc/Hz	-194 dBc/Hz
$S_\theta(f_m)_{Electrical}$	-85 dBc/Hz	-105 dBc/Hz	-136 dBc/Hz

Table 6.1: Comparison of Phase Noise due to Brownian Motion, $S_\theta(f_m)_{Mechanical}$ and Electrical Thermal Noise, $S_\theta(f_m)_{Electrical}$.

It is apparent that the Brownian-motion-induced phase noise is dominant for the low offset frequencies. However, it decreases much faster than the classical phase noise above the mechanical resonant frequency and is dominated by that noise above 100 KHz in this example. Both noise profiles are plotted on a logarithmic scale in Figure 6.6 for illustration. Note that the classical phase noise due to the electrical thermal noise only is shown in this plot. In practice, $1/f$ noise will result in an increased noise level for low offsets from the carrier.

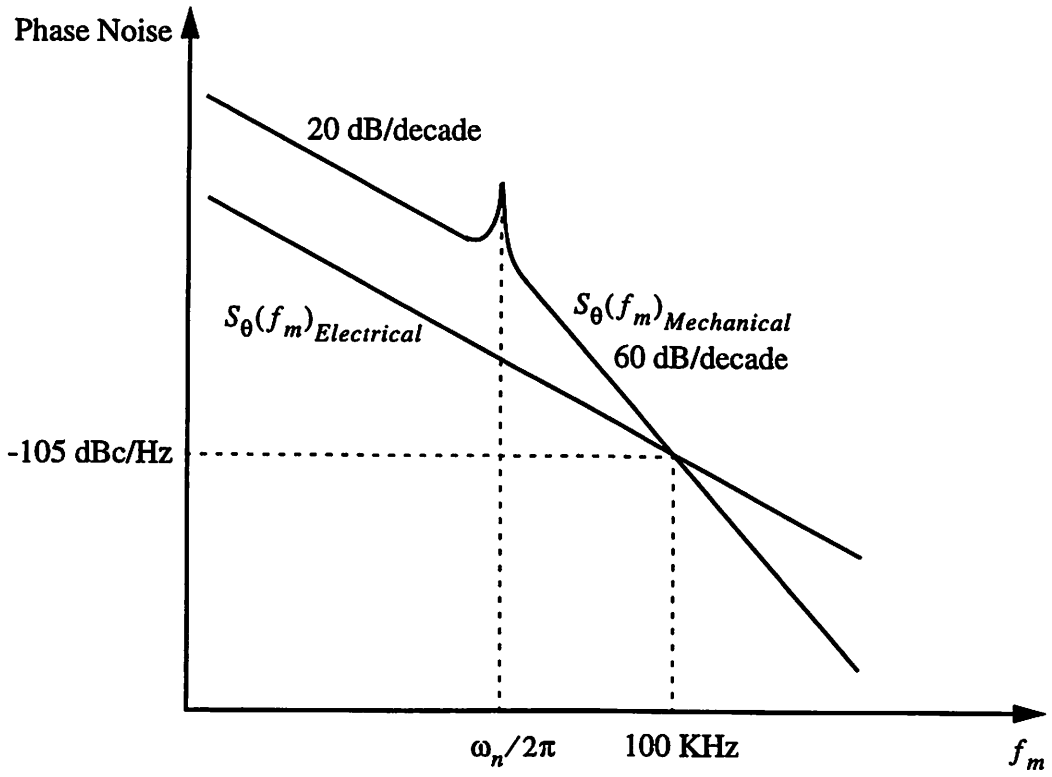


Figure 6.6: Phase Noise Profiles to Brownian Motion, $S_\theta(f_m)_{Mechanical}$ and Electrical Thermal Noise, $S_\theta(f_m)_{Electrical}$

Typical current wireless communication applications specify a low phase noise requirement at a relatively large offset frequency such as 3 MHz as shown in Table 3.1. Therefore, the Brownian motion effect does not prevent the oscillators from achieving the required performance. However, if a close-in low phase noise is demanded for certain stringent applications, then this additional noise must be reduced. The Brownian-motion-induced phase noise can be suppressed by various methods as proposed below. Each approach has its limitations and trade-offs.

Connecting N number of micromachined capacitors in parallel will result in a reduced total displacement noise power spectral density of $x_n^2(f_m)/N$ due to an averaging effect, where $x_n^2(f_m)$ represents the corresponding spectral density for each individual capacitor. Therefore, an increased number of parallel-connected capacitors will reduce the phase noise. However, the value of N is ultimately limited by the total required capacitance in an oscillator.

Using small capacitors with a reduced plate size, on the other hand, will demand an increased number of parallel-connected capacitors in order to achieve the desired total capacitance. The final resulting phase noise, however, will remain approximately the same because the displacement noise power spectral density of each capacitor will also increase due to the reduction of the suspended plate mass, provided that the mechanical resonant frequency remains constant for maintaining the same tuning voltage.

Increasing the capacitor nominal air gap, x_o, will suppress the Brownian motion effect. The associated drawback is that an increased tuning voltage is needed. Reducing the ratio between the tunable capacitance and tank parasitics will result in a phase noise suppression but at the expense of a narrowed tuning range.

Altering the capacitor displacement noise spectral density, $x_n^2(f_m)$,can minimize the phase noise in certain regions. As presented in Section 4.3.6, $x_n^2(f_m)$ can be shaped significantly through varying the mechanical quality factor, Q_M. Increasing Q_M by decreasing the ambient pressure reduces the spectral density away from the mechanical resonant frequency, thus resulting in a phase noise suppression as illustrated in Figure 6.7 on a logarithmic scale.

However, at the mechanical resonance the noise is enhanced due to the increased Q_M. Therefore, depending upon applications this phase noise shaping can potentially be attractive especially when there is no adjacent channel at ω_n away from the desired channel. Besides all the suppression methods proposed above, a close-in low phase noise can be achieved through enclosing the VCO in a wide-band phase-locked loop (PLL). By extending the PLL loop bandwidth, an improved suppression on the close-in phase noise can be accomplished [30].

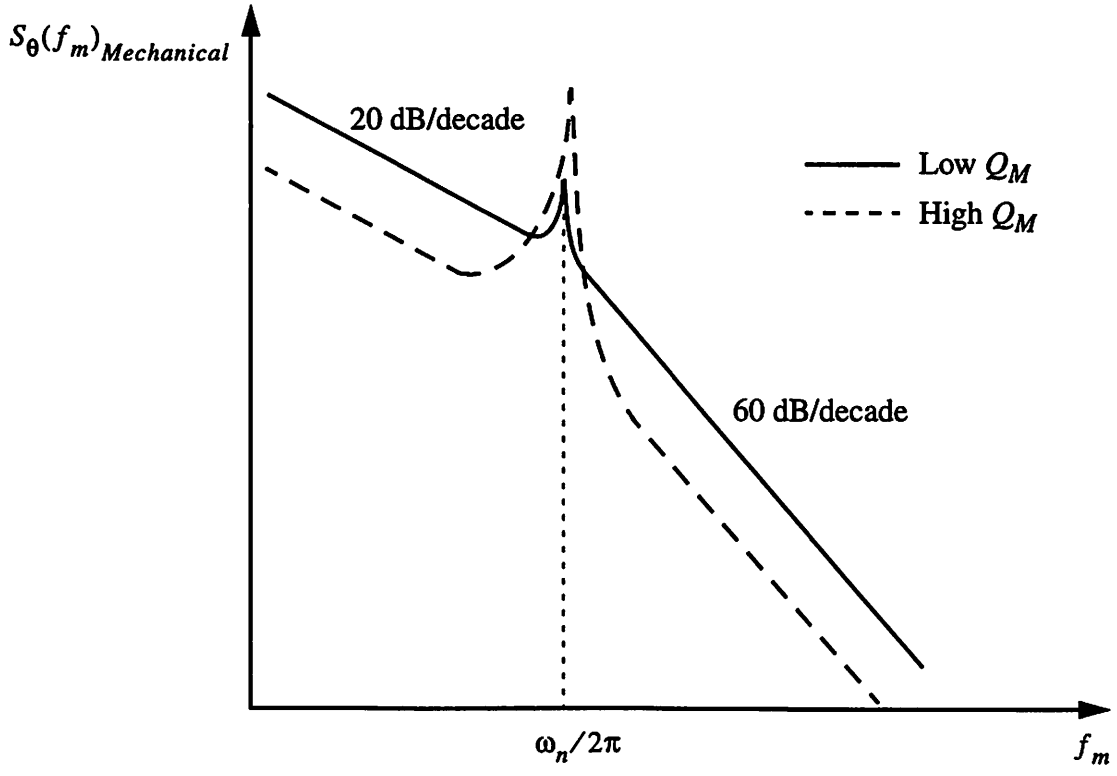


Figure 6.7: Effect of Q_M on Brownian-Motion-Induced Phase Noise

6.4 Summary

The analysis and design considerations of a LC-tuned oscillator are illustrated in this chapter. In a typical design, the small-signal oscillator loop gain is set about 3~4 to ensure a reliable start-up. The steady-state oscillation frequency is usually determined by the LC tank resonant frequency. The final oscillation amplitude is reached when the large-signal loop gain becomes unity due to the inherent nonlinearities in the active devices.

A conventional LC oscillator results in a classical phase noise caused by the electrical thermal noise, $1/f$ noise, and noise from the supply voltage and substrate. A key step to minimize this phase noise is to increase the tank Q factor. However, in a micromachine-based LC-tuned oscillator, an additional phase noise is introduced due to the mechanical thermal vibration of the tunable capacitors. This noise typically dominates the classical phase noise at the low offset frequency region and decays much faster than the classical counterpart beyond the mechanical resonant frequency. Therefore, it does not hinder the application of this type of oscillator in typical wireless communication applications. To achieve a close-in low phase noise performance for certain stringent applications, methods such as vacuum packaging or a wide-band PLL may be required.

Chapter 7

Prototype Micromachined Voltage-Controlled Oscillator

7.1 Introduction

This chapter presents the design and measurement results of two prototype micromachine-based RF voltage-controlled oscillators. In the first prototype, the micromachined variable capacitors and active electronics are realized on separate silicon substrates. They are attached to a test board and wire bonded together with a commercially available discrete inductor to form the VCO. In the second version, a fabricated 3-D coil inductor is used to replace the discrete inductor. This hybrid approach is chosen to avoid the complexity of building the prototype VCOs. Because the three key components, the variable capacitor, inductor and active electronics, are all fabricated on silicon wafers, they are amenable to integration on the same substrate.

7.2 VCO with Micromachined Capacitors and Discrete Inductor

The prototype VCO configuration is shown in Figure 7.1. The Colpitt's oscillator topology is chosen as a testing vehicle because of its simplicity.

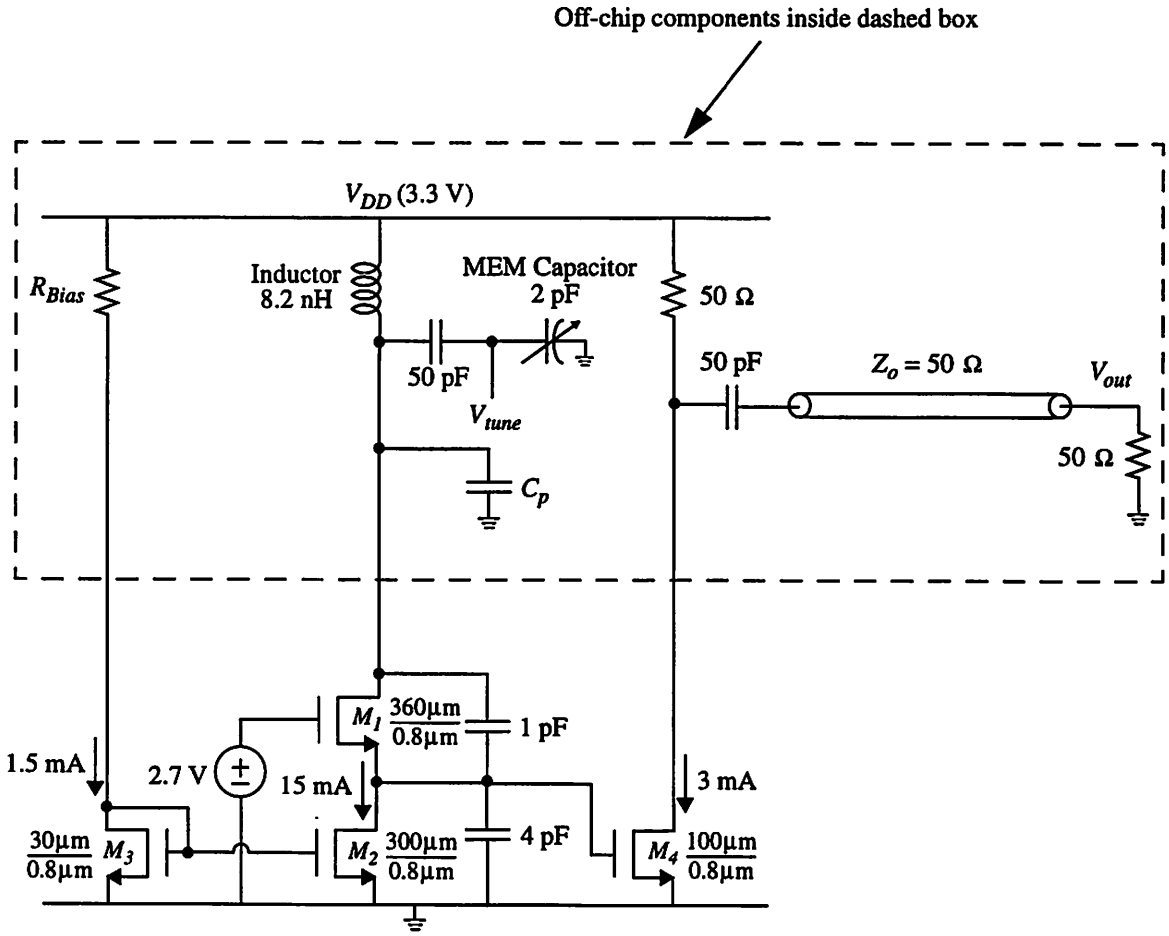


Figure 7.1: Prototype VCO Configuration

The oscillator core electronics consist of M_1 functioning as a common-gate amplifier with a small-signal transconductance of 30 mA/V, and capacitors C_1 and C_2 with 1 pF and 4 pF respectively to form a feedback path with a feedback ratio of 5:1. Both capacitors are implemented by using metal-oxide-metal sandwiched layers to ensure a high Q factor. The discrete inductor has a 8.2 nH

inductance value with a specified Q factor of 30 at 1 GHz. This inductance value is chosen to resonate with an overall capacitance, C_T, of 4.8 pF at 800 MHz, where C_T can be expressed as:

$$C_T = C_v + \frac{C_1 C_2}{C_1 + C_2} + C_P \tag{7-1}$$

The capacitor, C_p, represents the parasitic capacitance contributed by the bond pad on the electronics die and interconnects from the test board and is estimated around 2 pF in this design. The tank impedance, R, at the resonant frequency can be calculated around 850 Ω, assuming C_1, C_2 and C_p have Q values much higher than that of C_V. As a result, the small-signal loop gain around the oscillator, $\left(\frac{g_m R}{n}\right)\left(1-\frac{1}{n}\right)$, is equal to 4, which ensures a reliable oscillation start-up. The term, $\left(1-\frac{1}{n}\right)$, represents the loading effect from M_1 [64]. In the steady-state oscillation the oscillator develops a 2.5 V peak to peak swing across the LC tank. To minimize the tank loading, the oscillator output is taken between C_1 and C_2 and buffered through M_4 for an external measurement. A 50 Ω resistor load is used at the output of M_4 to achieve an impedance matching.

The VCO electronics are fabricated using HP's 0.8 μm CMOS process. The die photo is shown in Figure 7.2, where M_1 is placed adjacent to a bond pad through which the active electronics are interfaced to the external LC tank. Every high-frequency signal pad is shielded by a metal layer underneath, which is then grounded through two adjacent bond pads on each side. This approach minimizes the substrate noise coupling and high-frequency signal feed through to the nearby bondwires used for DC biasing. The shielding also ensures a high-Q parasitic capacitance for the bond pad connected to the resonator, critical to achieve a low phase noise.

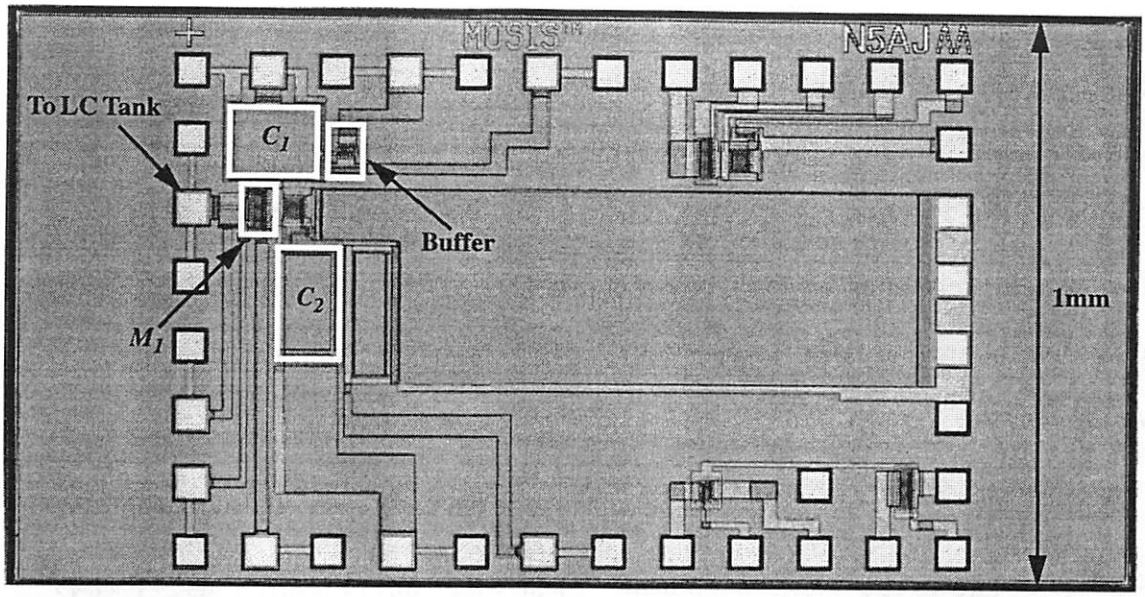


Figure 7.2: CMOS VCO Electronics Die Photo

A photograph of the prototype VCO test board is presented in Figure 7.3.

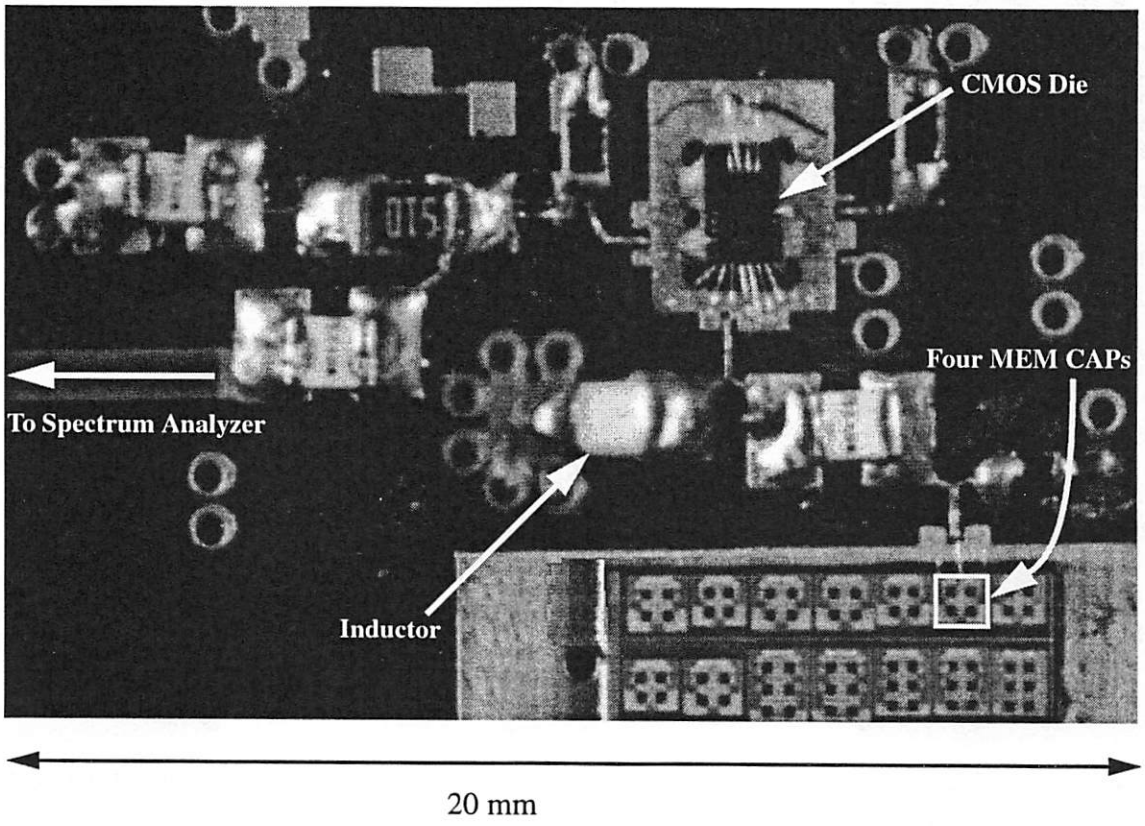
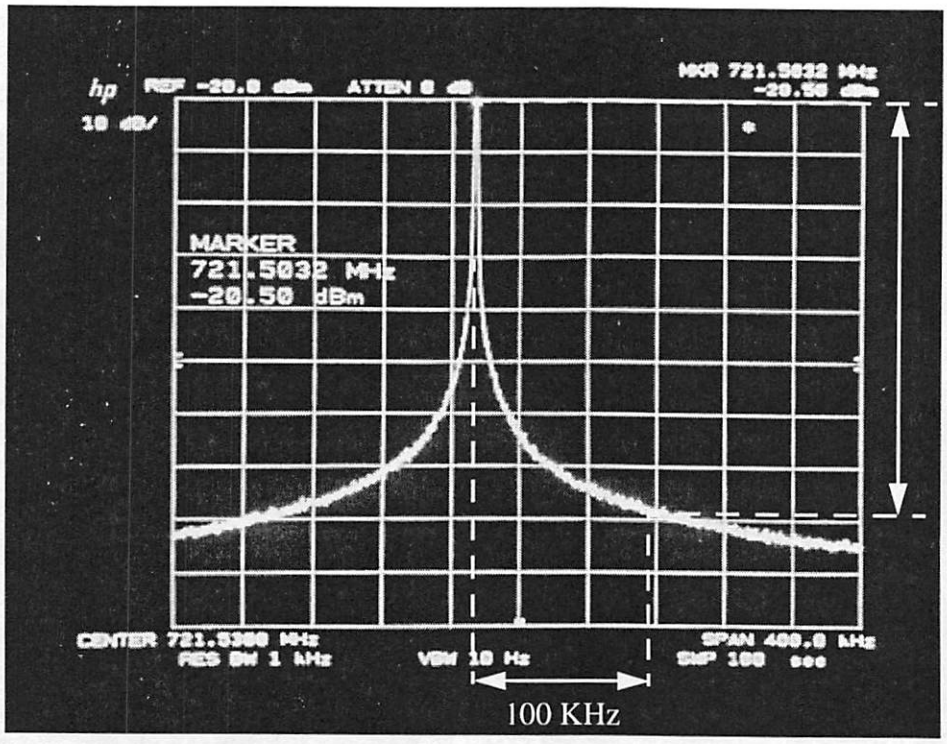


Figure 7.3: First Prototype VCO Test Board

A set of four parallel-connected micromachined variable capacitors on a silicon substrate is wire bonded to the test board with the CMOS VCO electronics die and a discrete inductor to form the oscillator. The VCO oscillates at a center frequency of 714 MHz and can be tuned from 707 MHz to 721 MHz with 3 V. The center frequency is lower than the designed value of 800 MHz due to an excessive board parasitic capacitance, which also limits the tuning range of the VCO.

The phase noise is another key performance parameter of the oscillator. Figure 7.4 shows the oscillator output power spectrum measured at 721 MHz.



Phase Noise:
-110 dBc/Hz

Figure 7.4: First Prototype VCO Output Power Spectrum

At 100 KHz offset frequency, a phase noise of -110 dBc/ Hz is achieved. To measure the VCO phase noise at 3 MHz offset frequency, a low noise-floor phase noise measurement system, HP 3048AR, is used. Figure 7.5 presents the measured phase noise plot of the prototype VCO, indicating that a phase noise of -139 dBc/Hz is achieved at 3 MHz offset frequency. The low phase noise is due to the high-Q micromachined capacitors and discrete inductor used in the design. The performance is suitable for most wireless communication applications and matches that of a typical VCO relying on external varactor diodes and inductors. The core of the oscillator dissipates 49.5 mW from a 3.3 V power supply.

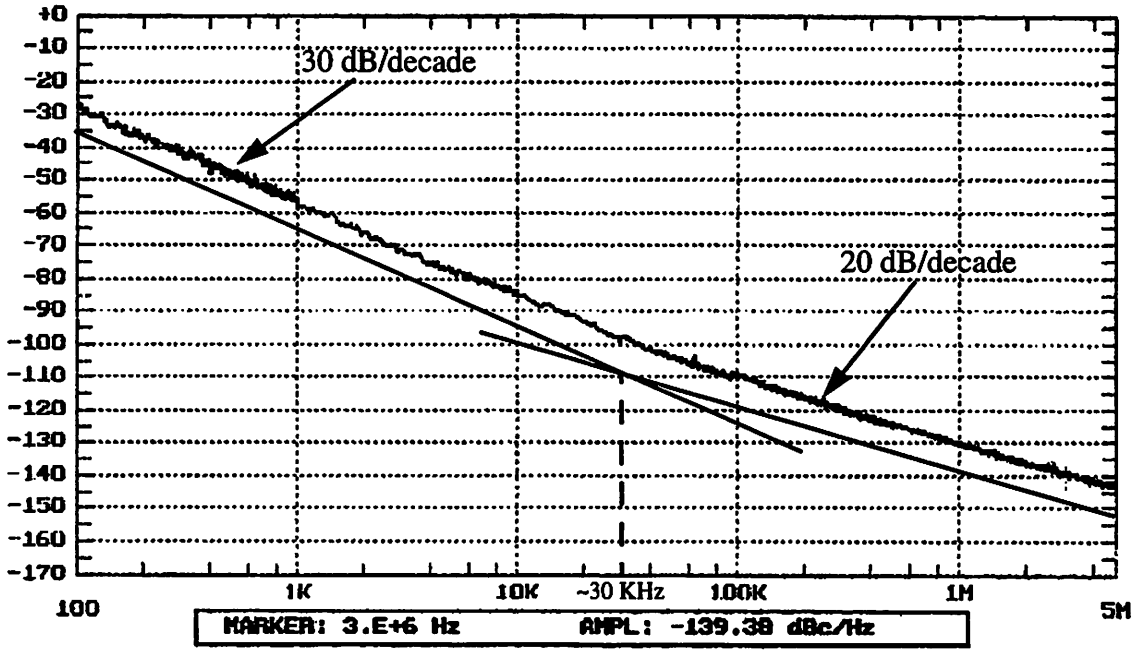


Figure 7.5: First Prototype VCO Phase Noise Plot

From the measurement results obtained in the atmospheric pressure, the VCO phase noise is limited by the $1/f$ noise from the active circuits for the close-in region with a corner frequency around 30 KHz and thermal noise from the electronics at large offsets rather than the Brownian motion. This is because the total tunable capacitance of 0.8 pF in this design is a small fraction of the tank parasitic capacitance of approximately 5 pF, 3 pF of which is due to the measurement setup. To verify the pressure-dependent noise shaping effect for the Brownian-motion-induced phase noise, as discussed in Section 6.3.2, the VCO is tested in a vacuum environment. Figure 7.6 presents the oscillator output power spectrum measured in a 20 mT vacuum chamber.

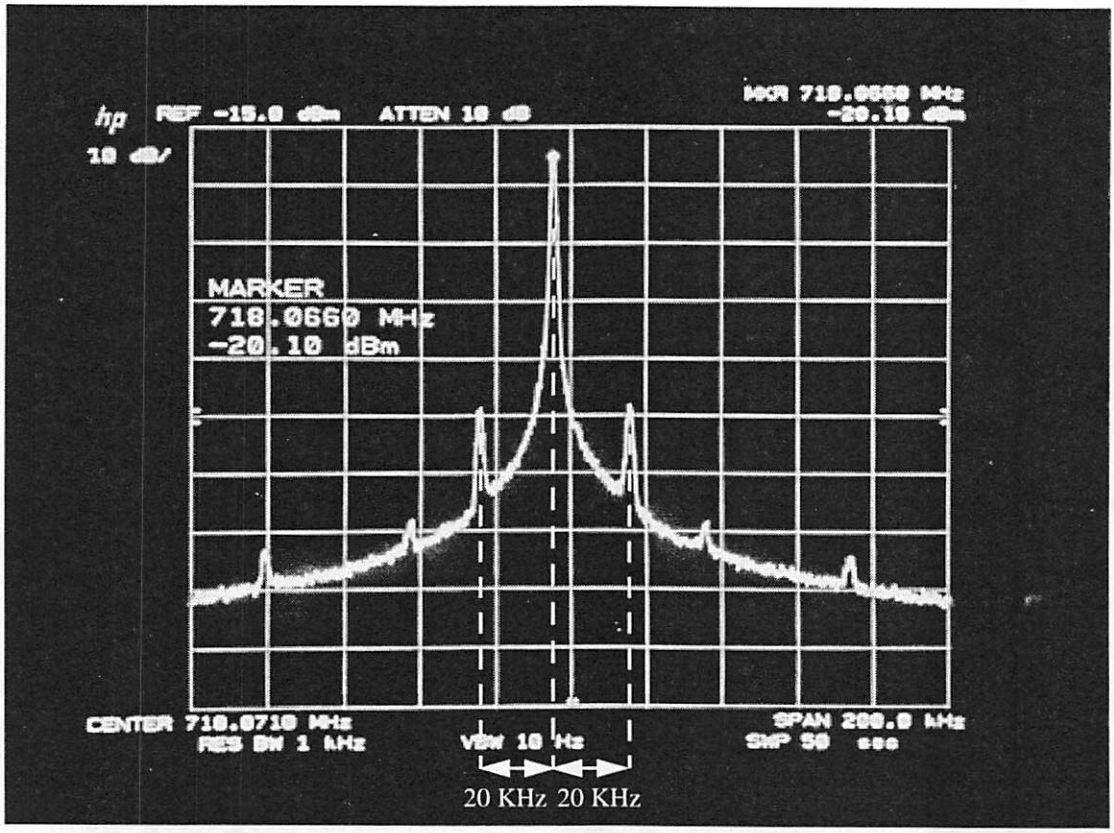


Figure 7.6: First Prototype VCO Output Power Spectrum in 20 mT Vacuum

The spectrum reveals two main side-band peaks occurring at 20 KHz away from the carrier with a 15 dB noise enhancement. This indicates that the micromachined capacitor has a fundamental mechanical resonant frequency of 20 KHz. The Brownian-motion-induced phase noise is at least 15 dB higher than the floor at that frequency. The overall phase noise remains the same away from the resonance because it is dominated by noise sources from the active electronics in this design. The measured mechanical resonant frequency is less than the designed value of 30 KHz because of the process variations in the deposited film thickness and wet etching rate on the aluminum suspensions. Also shown in Figure 7.6 are four additional side-band peaks occurring at approximately 40 KHz and 78 KHz away from the carrier each with 5 dB noise enhancement. These peaks are caused by the higher-order mechanical resonances of the micromachined capacitors.

7.3 VCO with Micromachined Capacitors and 3-D Coil Inductor

The second prototype VCO replaces the discrete inductor used in the previous design with a 3-D coil inductor fabricated on a separate silicon substrate. The 3-D inductor has two turns and an inductance of 8.2 nH with a Q factor of 16 at 1 GHz. Figure 7.7 presents the photograph of the VCO test board. A set of four parallel-connected micromachined variable capacitors, a 3-D coil inductor, and a CMOS VCO electronics die are wire bonded to form the oscillator. The long alumina bar is used in the prototype inductor fabrication for manual handling. In the future improved process only a small amount of core material is needed, shown by a white box located at the center of the alumina

bar, for building the inductor. Because all the key components are fabricated on silicon wafers, they are amenable to integration on the same substrate.

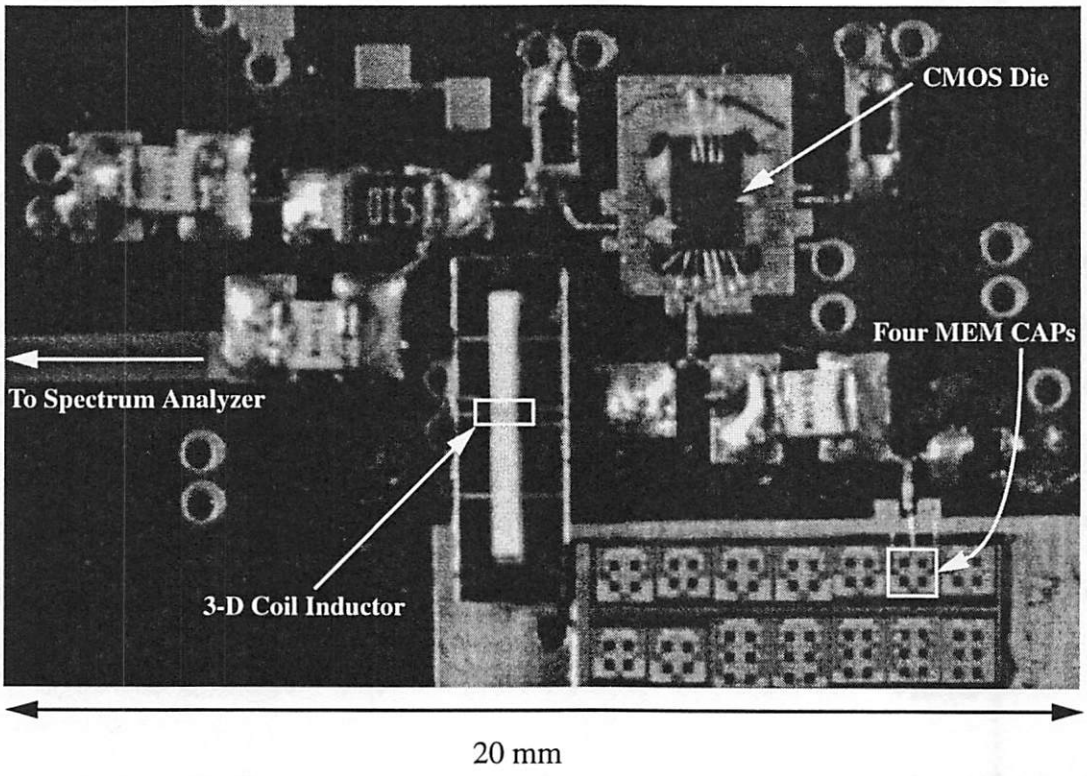


Figure 7.7: Second Prototype VCO Test Board

Figure 7.8 shows the oscillator output power spectrum at 863 MHz with a phase noise of -106 dBc/Hz achieved at 100 KHz offset frequency. The measured phase noise profile is plotted in Figure 7.9. At 3 MHz offset frequency a phase noise of -136 dBc/Hz is achieved. This phase noise is 3 dB higher than that of the first prototype VCO because of the reduced inductor Q value. However, the obtained performance is suitable for most wireless communication applications such as GSM cellular telephony and has not been achieved by VCOs relying on conventional silicon junction variable capacitors and on-chip spiral inductors. The oscillator is tunable from 851 MHz to 863 MHz with 3 V

limited by the parasitics of the test setup. In an ultimate monolithic implementation, the tank parasitic capacitance will be reduced substantially. An increased tuning range of at least 50 MHz for a 1 GHz carrier signal is expected.

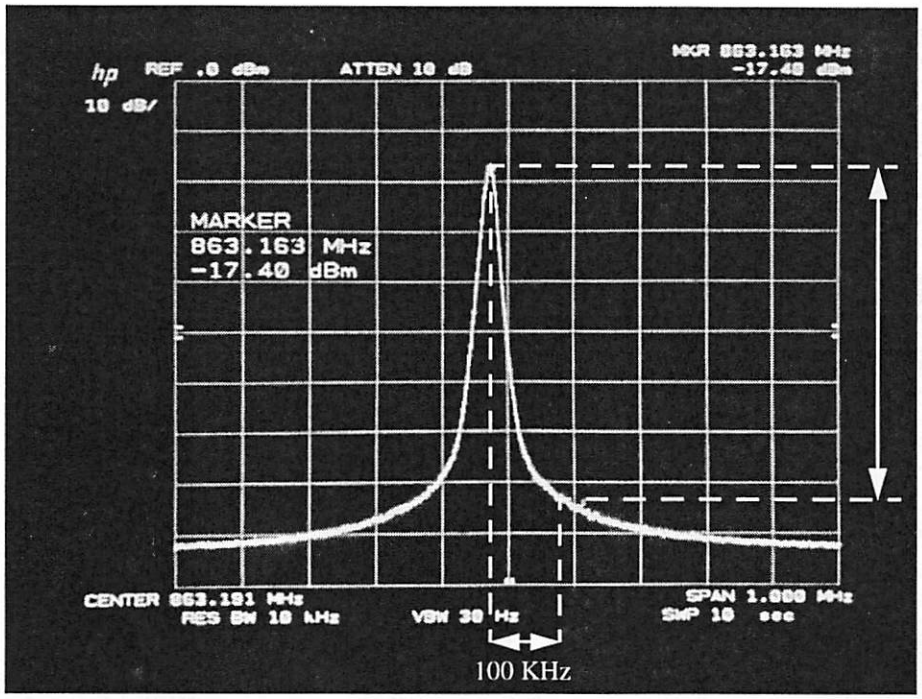


Figure 7.8: Second Prototype VCO Output Power Spectrum

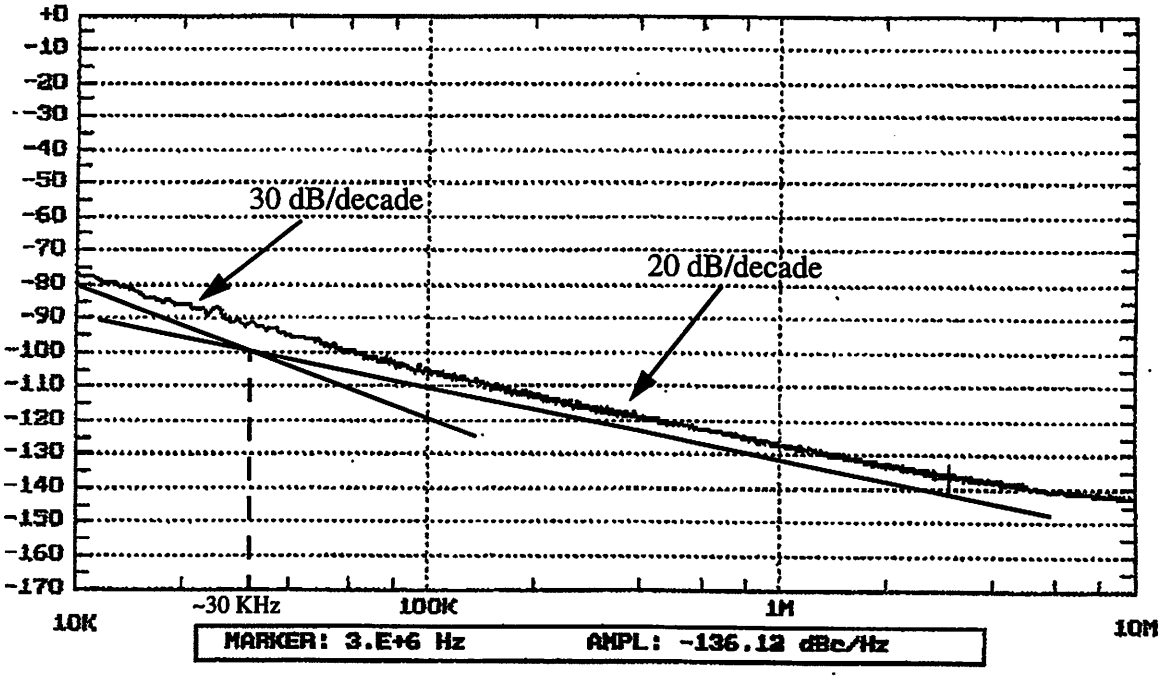


Figure 7.9: Second Prototype VCO Phase Noise Plot

7.4 Summary

Two prototype micromachine-based RF voltage-controlled oscillators have been developed. To reduce the fabrication complexity of the first prototype VCO, the variable capacitors and oscillator electronics are fabricated on separate silicon substrates and wire bonded with a discrete inductor to form the oscillator. This oscillator demonstrates a low phase noise of -139 dBc/Hz at 3 MHz offset frequency from a 721 MHz carrier signal due to the high-Q passive elements and is tunable between 707 MHz and 721 MHz with 3 V, limited by the parasitic capacitance from the test setup. The phase noise performance is dominated by the $1/f$ noise and thermal noise from the active circuits rather than the Brownian-motion. The oscillator tested in a 20 mT vacuum chamber shows a

15 dB noise enhancement at 20 KHz offset frequency, indicating that the micromachined capacitor has a fundamental mechanical resonant frequency of 20 KHz. The core of oscillator dissipates 49.5 mW from a 3.3 V power supply. The second prototype replaces the discrete inductor with a two-turn 3-D coil inductor fabricated on a separate substrate. Because all the key components are realized on silicon wafers, they are amenable to integration on the same substrate. This oscillator achieves a low phase noise of -136 dBc/Hz at 3 MHz offset frequency from a 863 MHz carrier signal and is tunable between 851 MHz and 863 MHz with 3 V, limited by the setup parasitics. The achieved phase noise performance is suitable for most wireless communication applications such as GSM cellular telephony.

Chapter 8

Conclusions

8.1 Results

Highly miniaturized wireless transceivers are critical for future multistandard wireless communication applications. In this research, MicroElectroMechanical technologies are explored as a means to achieve IC-compatible high-Q RF tunable capacitors and inductors. These passive components are the key elements for miniaturizing RF building blocks employed in current transceivers. An RF micromachine-based low phase noise voltage-controlled oscillator has been chosen as a demonstration vehicle to illustrate that complete monolithic high-performance VCOs can be realized through MicroElectroMechanical technologies. Monolithic VCOs will help the size reduction of current transceivers, which offers a potential solution to achieve a single hand-held wireless phone providing multistandard capabilities.

Several conclusions can be drawn from this research work. Micromachining technologies provide IC-compatible RF tunable capacitors and

inductors with high Q factors that cannot be achieved through current conventional IC process. These high-Q passive components are crucial for integrating high-performance RF building blocks, in particular the low phase noise RF VCOs. A prototype RF VCO has been designed and built using the micromachined high-Q tunable capacitors and 3-D coil inductor. The oscillator meets the stringent GSM phase-noise requirement and demonstrates that complete monolithic high-performance VCOs can be achieved through micromachining technologies for cellular telephony applications.

8.2 Future Work

It is the goal of this research project to ultimately realize a fully monolithic micromachine-based high-performance VCO. Each individual passive component has been explored. However, process integration issues involving the passive devices and active electronics need to be further investigated in order to obtain a monolithic implementation.

The micromachined variable capacitors and 3-D coil inductors explored in this research are not only critical for low phase noise RF VCOs, but also for implementing other RF building blocks such as the front-end tunable RF filters for multiband operation, low-loss impedance matching networks, and high-efficiency power amplifiers. It is highly desirable to further increase the quality factor and tuning range for the micromachined capacitors and Q factor for the 3-D coil inductors. An increased Q value will result in a reduced power consumption for VCOs meeting the same phase noise requirement, a critical key advantage for portable wireless communication devices. An extended tuning range will minimize the oscillator sensitivity to process variations. High Q

values are also crucial for minimizing the insertion loss for LC-based RF filters and impedance matching networks, a key requirement for high-performance radio applications. The proposed methods outlined in Sections 4.6 and 5.6 can be employed to achieve this goal.

Appendix A

Brownian-Motion-Induced Phase Noise

The change of the air gap of a micromachined variable capacitor causes a capacitance value variation expressed as:

$$C = \frac{\varepsilon_o A}{x_o + \Delta x} \cong \frac{\varepsilon_o A}{x_o}\left(1 - \frac{\Delta x}{x_o}\right) = C_o\left(1 - \frac{\Delta x}{x_o}\right), \tag{A-1}$$

where Δx is the plate displacement and assumed to be a small fraction of the nominal air gap, x_o. This will result in a shifted resonant frequency of the corresponding LC tank as shown in Equation (A-2),

$$\omega_{res} = \frac{1}{\sqrt{LC}} = \omega_o\left(1 + \frac{\Delta x}{2x_o}\right) = \omega_o + \Delta\omega \tag{A-2}$$

where $\omega_o = \frac{1}{\sqrt{LC_o}}$ and $\Delta\omega = \omega_o\left(\frac{\Delta x}{2x_o}\right)$.

Furthermore, if the capacitor suspended plate vibrates at a single frequency, $\omega_{vibrate}$, with a displacement amplitude of $x_{vibrate}$, then a LC-tank oscillator using this capacitor, assuming without any parasitic capacitance, will develop an FM-modulated output signal at the steady state, which can be expressed as:

$$v_{osc}(t) = V_{osc}cos\left(\omega_o + \omega_o\frac{x_{vibrate}cos\omega_{vibrate}t}{2x_o}\right)t, \tag{A-3}$$

where V_{osc} is the output signal amplitude. This signal can be written as:

$$v_{osc}(t) = V_{osc}cos(\omega_o + \beta sin\omega_{vibrate}t)t, \tag{A-4}$$

where β is the FM modulation index and can be found as:

$$\beta = \frac{\omega_o x_{vibrate}}{2\omega_{vibrate}x_o}. \tag{A-5}$$

For $\beta \ll 1$, Equation (A-4) can be simplified as:

$$v_{osc}(t) = V_{osc}\left(cos\omega_o t + \frac{\beta}{2}cos(\omega_o + \omega_{vibrate})t - \frac{\beta}{2}cos(\omega_o - \omega_{vibrate})t\right); \tag{A-6}$$

hence, the noise to signal ratio (phase noise) at $\omega_{vibrate}$ away from the main carrier signal, ω_o, can be determined as:

$$S_\theta(\omega_{vibrate}) = \left(\frac{\beta}{2}\right)^2 = \frac{x^2_{vibrate}}{16x_o^2}\left(\frac{\omega_o}{\omega_{vibrate}}\right)^2 = \frac{x^2_{vibrate-rms}}{8x_o^2}\left(\frac{\omega_o}{\omega_{vibrate}}\right)^2. \tag{A-7}$$

Consequently, if the mechanical-thermal vibration of the suspended plate has a displacement power spectral density of $x_n^2(f_m)$, the corresponding phase noise can be expressed as:

$$S_\theta(f_m)_{Mechanical} = \frac{x_n^2(f_m)}{8x_o^2}\left(\frac{f_o}{f_m}\right)^2. \tag{A-8}$$

In practice a LC-tuned voltage-controlled oscillator will always include some parasitic capacitances, C_p, in addition to the tunable capacitance of C_v. Thus Equation (A-1) can be modified as:

$$C = C_v + C_p = \varepsilon_o\frac{A}{x_o + \Delta x} + \frac{1}{\alpha}\varepsilon_o\frac{A}{x_o}, \tag{A-9}$$

where α is the ratio between the nominal tunable capacitance value and C_p. Equation (A-1) can be further simplified as:

$$C = \varepsilon_o \frac{A}{x_o}\left(\frac{1+\alpha}{\alpha}\right)\left(1-\left(\frac{\alpha}{1+\alpha}\right)\frac{\Delta x}{x_o}\right). \tag{A-10}$$

By following the same approach as previously shown, the Brownian-motion-induced phase noise can be found as:

$$S_\theta(f_m)_{Mechanical} = \frac{x_n^{\,2}(f_m)}{8\left(\frac{1+\alpha}{\alpha}\right)^2 x_o^{\,2}}\left(\frac{f_o}{f_m}\right)^2. \tag{A-11}$$

Connecting N micromachined variable capacitors in parallel will result in a total displacement noise spectral density of $x_n^{\,2}(f_m)/N$, where $x_n^{\,2}(f_m)$ is the corresponding spectral density for each individual capacitor. As a result, the phase noise of a VCO consisting of N parallel-connected micromachined variable capacitors can be expressed as:

$$S_\theta(f_m)_{Mechanical} = \frac{x_n^{\,2}(f_m)}{8\left(\frac{1+\alpha}{\alpha}\right)^2 N x_o^{\,2}}\left(\frac{f_o}{f_m}\right)^2. \tag{A-12}$$

Appendix B

Maxwell 3D Field Simulation

The inductance value of three-dimensional coil inductors can be simulated by using Maxwell 3D field simulator. Figure B-1 shows a graphical view of the setup for a one-turn coil inductor simulation.

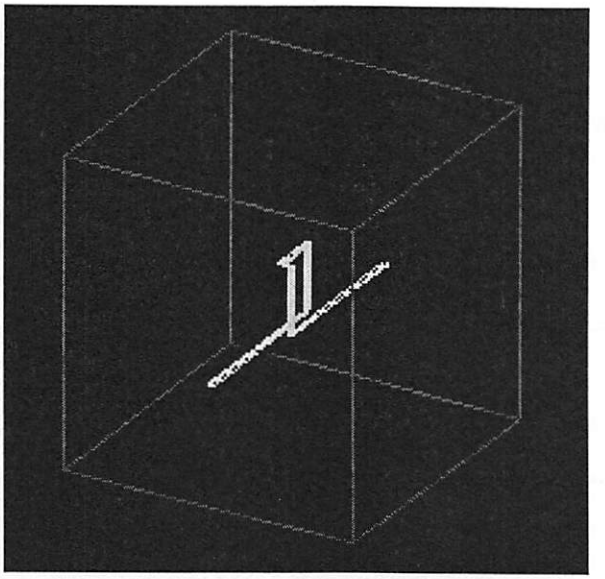


Figure B-1: 3-D Coil Inductor Simulation Setup

The 3-D device, generated by the simulator drawing program, is placed at the center of a box which defines the simulation region. In order to minimize the edge effect due to the boundary conditions imposed on the box surfaces, the box size needs to be made much larger than that of a 3-D coil inductor. In this example, the box dimension is 2980 μm by 2980 μm by 2980 μm compared to the coil inductor with a cross-section area of 500 μm by 650 μm. Two interconnect extension traces with a length of 1240 μm are required to connect the 3-D inductor to the front and back surfaces of the box as shown in the figure. This constraint is imposed by the simulation program.

After defining the trace material properties and boundary conditions, eddy-current mode is selected to simulate the inductance value of the entire structure. The inductance of the 3-D device can be determined by subtracting the contribution due to the interconnect extensions from the total simulated inductance. In the current setup, the inductances for the entire structure and interconnect extensions are found to be 5.64 nH and 1.64 nH respectively. This results in a 4 nH inductance for the one-turn 3-D coil inductor.

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