PHYSICAL MODELING OF RTD-BASED CNN CELLS

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Physical Modeling of RTD-Based CNN Cells

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Abstract

Resonant tunneling diodes (RTDs) have intriguing properties which make them a primary nanoelectronic device for both analog and digital applications. They excel in their size, switching speed, and the negative differential resistance property, and they can readily be integrated together with GaAs FETs. In this report, we investigate their use in circuits for Boolean cellular neural networks (CNNs).
First, we propose a simple RTD-based circuit capable of realizing linearly separable Boolean functions. To implement the network parameters, the transconductances of the FETs are used. Hence, the cell is not programmable or universal, but application-specific. The theoretical results are confirmed by Spice simulations, and an example is given.
In a second part, we study the universal cell circuit for Boolean CNNs which is proposed in [1]. In this circuit, the negative differential resistance of the RTD is fully exploited. Spice simulations confirm that it is capable of realizing a large class of linearly not separable Boolean functions.

1 Introduction

1.1 Nanoelectronics and the Resonant Tunneling Diode

There is a physical limit to how far conventional transistors and integrated circuits can be downscaled. At some point, revolutionary concepts such as *nanoelectronics* will be needed to meet the challenge of smaller, faster, and better devices and circuits. Nanoelectronics goes back to the mid 1980s, when work began on resonant tunneling and bandgap engineering in low-dimensional quantum wells and superlattices.

When the size of a system scales down to the size of an electron wavelength, quantum effects take over. When transistors are downscaled and their dimensions are measured in nanometers, new phenomena and devices based on quantum tunneling mechanisms are needed – devices and circuits fabricated with nanometer precision. In the last ten years, advances have been made at realizing artificial semiconductor structures using molecular-beam epitaxy, metal-organic vapor deposition, and chemical-beam epitaxy.

The structural simplicity, the relative ease of fabrication, the inherent high speed, the flexible design freedom, and the versatile circuit functionality make the *resonant tunneling diode* (RTD) an excellent candidate for nanoelectronics devices in both analog and digital applications. Furthermore, RTDs and FETs can readily be integrated *monolithically*, allowing extremely compact circuits.

The basic RTD device configuration is a double barrier quantum well structure measured in nanometers [2, 3]. The structure has two contacts (the emittor and the collector) made from a semiconductor with a small bandgap (e.g., GaAs), quantum barriers made from a semiconductor

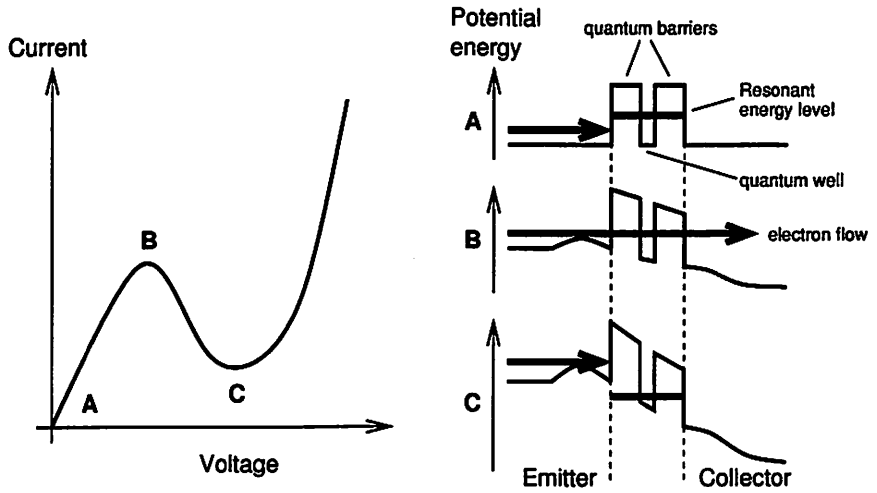


Figure 1: The resonant tunneling diode: I–V characteristics and energy band diagrams.

with a larger bandgap (e.g., InGaAs), and a quantum well made from the smaller bandgap semiconductor (Fig. 1). The wave nature of electrons in such a structure leads to quantum phenomena like interference, tunneling, and energy quantization; the quantum well is so narrow ($\approx$ 5nm) that it can only contain a single, the so-called *resonant*, energy level. Electrons wishing to travel from the emitter to the collector can only do so if they are lined up with this resonant energy level.

Initially, with a low voltage across the device (point A in Fig. 1), the electrons are below the the point of resonance, and no current can flow through the device. As the voltage increases, the emitter region is warped upwards, and the collector region is warped downwards. Eventually, the band of electrons in the emitter will line up with the resonant energy state, and allows tunneling through to the collector (peak at point B). With higher voltage, the electrons are pushed past the resonant energy level and are unable to continue tunneling, which can be observed by the drop in current to the valley at point C. If the voltage increases further, more and more electrons are able to flow over the top of the quantum barriers, and the current flow will rise.

The *negative differential resistance* (NDR) between points B and C is the key property of RTDs. In digital applications [4], the NDR property permits compact bistable circuits without feedback. In this report, however, we focus on the modeling of *analog RTD circuits*; in particular, we consider the potential of RTDs for the design of cells for the cellular neural network (CNN) [5, 6].

While conventional technology requires more than about 60 CMOS transistors to build cell for a so-called *uncoupled* CNN [7], this number may be reduced by a factor of 3 by using RTDs. Furthermore, the highly nonlinear I–V characteristics of the RTD permits the extension from the linearly separable class of Boolean functions in the standard CNN cell to *any* Boolean function.

1.2 Physics-based Model of Resonant Tunneling Diodes

In order to incorporate the RTD into a Spice-like circuit representation, its current-voltage characteristic has to be modeled with sufficient accuracy. It is desirable to dispose of a model which is based on actual physical parameters such as energy levels, dopant concentrations, and the geometry of the device. In [8], Schulman et al. solved this task satisfactorily, starting by

expressing the current density of the RTD with an effective mass approximation,

$$J = \frac{em^*kT}{2\pi^2\hbar^3}\int_0^\infty T(E,V)\cdot\ln\left[\frac{1+e^{(E_F-E)/kT}}{1+e^{(E_r-E-eV)/kT}}\right]dE \tag{1}$$

which includes nonzero temperature and Fermi-Dirac statistics. The transmission coefficient $T(E,V)$ is approximated by a Lorentzian, i.e.,

$$T(E,V) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left(E-\left(E_r-\frac{eV}{2}\right)\right)^2+\left(\frac{\Gamma}{2}\right)^2}, \tag{2}$$

where E is the energy measured up from the emitter conduction band edge. E_r is the energy of the resonant level relative to the bottom of the well at its center, and Γ is the resonance width. The formula assumes equal width barriers, which is not always valid. For better generality, $eV/2$ can be replaced by eVn, with n as a fitting parameter. Calculations show that Γ is on the order of only one meV even for quite thin barrier widths [9], which is much less than kT at room temperature. The substitution $E := E_r - eV/2$ is therefore resonable, and the integral (1) reduces to

$$J = \frac{em^*kT\Gamma}{2\pi^2\hbar^3}\ln\left[\frac{1+e^{(E_F-E_r+eV/2)/kT}}{1+e^{(E_F-E_r-eV/2)/kT}}\right]\cdot\left[\frac{\pi}{2}+\arctan\left(\frac{E_r-\frac{eV}{2}}{\frac{\Gamma}{2}}\right)\right]. \tag{3}$$

This formula provides the correct shape of the I–V characteristics, but is calculated in an oversimplified way. The physical quantities can be allowed to deviate from their actual values to compensate for approximations and omissions in the model. The result is of the form

$$J_1 = A\ln\left[\frac{1+e^{(B-C+n_1V)q/kT}}{1+e^{(B-C-n_1V)q/kT}}\right]\cdot\left[\frac{\pi}{2}+\arctan\left(\frac{C-n_1V}{D}\right)\right], \tag{4}$$

where the parameters A, B, C, and D can, on the one hand, be used to shape the curve to match a measured characteristic, and, on the other hand, have a well-defined physical interpretation. However, (4) merely produces a peak current and an NDR region, but there is no increasing valley current, which is due to tunneling through other channels and inelastic scattering. The simplest way to include a valley current contribution is to give it the form of tunneling through a higher resonance or thermal excitation over a barrier. For voltages below this higher energy channel, the additional current takes on the familiar diode form $J_2 = H(e^{n_2qV/kT}-1)$. The final form of the RTD current density is just the sum $J = J_1 + J_2$.

In this paper, we focus on the DC characteristics of the device; hence, the capacitances of the device are neglected. It can, however, be expected that the time constant of the RTD CNN cell will be in the order of tens of picoseconds [2]. For the circuits proposed in this paper, J_1 is specified by the parameters $A = 4800\text{A/cm}^2$, $B = 0.05\text{V}$, $C = 0.07\text{V}$, $D = 0.038\text{V}$, and $n_1 = 0.2$, and an area of 10^{-8}cm^2 is assumed. The parallel diode carrying J_2 is modeled by a generic Spice diode with an emission coefficient of $n = 1.75$ and a series resistance of $R_S = 1\text{k}\Omega$ (Fig. 2).

The NDR causes RTD circuits to possibly have multiple equilibrium points. Simulators such as Spice, not being explicitly designed for such systems, may encounter problems when solving (dc analysis) or integrating (transient analysis) the network equations [10]. It may therefore be necessary to tune the analysis options of the program in order to get meaningful results.

For CNN architectures with array sizes in the order of 1000 by 1000 cells, the use of nanostructures is a prerequisite, since such integration densities are far beyond what can be achieved by downscaling conventional CMOS devices. Due to its *negative differential resistance* property, the RTD is a promising candidate for such nano CNNs.

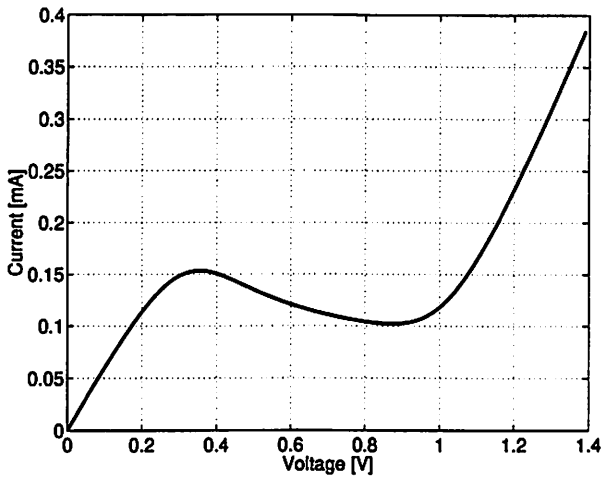


Figure 2: I–V characteristics of the RTD used in the proposed circuit.

2 A Simple RTD-Based CNN Cell for Linearly Separable Boolean Functions

As a first step into this field of RTD-CNNs, we propose and study a very simple RTD-based circuit for Boolean CNNs. The circuit is a realization of the uncoupled and static CNN cell equation

$$y_{ij} = \mathrm{sgn}\,(B * u_{ij} + I)\,, \tag{5}$$

where y_{ij} is the output of the cell at position (i, j), u_{ij} is its input, the B template comprises the weights of the usual spatial convolution $B * u_{ij}$, and I is a spatially invariant bias.

2.1 Circuit characterization

The basic idea is to exploit the bistable property of an RTD with a FET load [4]. If an additional FET is added in parallel to the RTD (Fig. 3), we may consider the two gate-source voltages as the *inputs* and the voltage across the RTD (and the lower FET) as the *output*. The lower FET is referred to as the *inhibiting* FET, while the one connected to V_{DD} is the *activating* FET – this terminology will be justified shortly. The I–V curves of the activating FET and the RTD are presented separately in Fig. 4 (a), and their combined characteristic in Fig. 4 (b), both as a function of V_{DS} and V_{GS}. The transconductance of the FET is chosen to be $k_p = 0.44\mathrm{mA/V}^2$, in accordance with [11]. The gate-source voltage ranges from 0V (logic "0") to 1V (logic "1").

If we select V_{DD}=2V and plot the I–V curves for the whole circuit, we can determine the stable (and unstable) equilibrium points. The case of equal transconductances for both FETs is depicted in Fig. 5 (a). From this plots, the logical operation of the circuit is derived:

- A logic "1" at the inhibiting gate always results in a "0" at the output, irrespective of the value of the activating gate. If u_{act} is low, the operating point is A, corresponding to an output value of less than 0.1V, if it is high, the operating point is B, i.e., $\approx$0.2V.
- A logic "0" at the activating gate also forces the output to be low, irrespective of the state of the inhibiting gate.

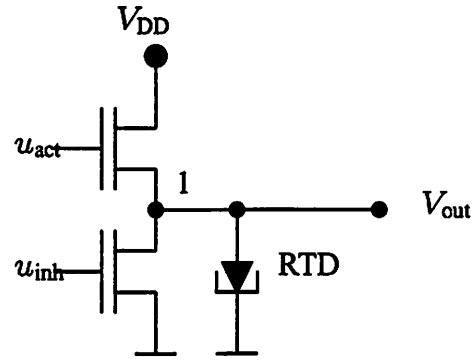
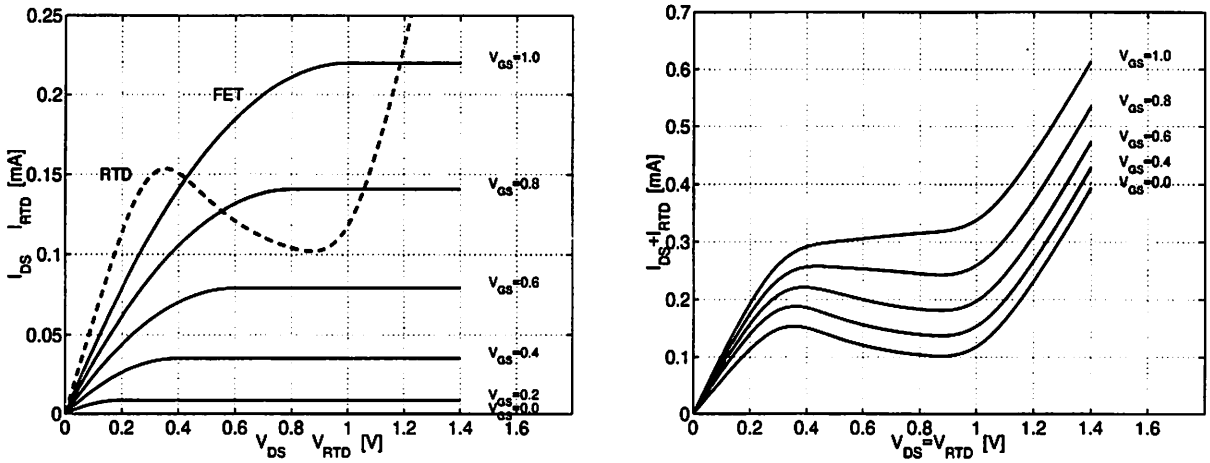


Figure 3: RTD-based CNN cell with 2 inputs.



(a) RTD and FET separately

(b) RTD and FET in parallel

Figure 4: I–V characteristic of an RTD and a FET with k_p=0.44mA/V^2.

- Only if u_{inh} is low *and* u_{act} is high, the output will be high (operating point C at a voltage of 1V or more).

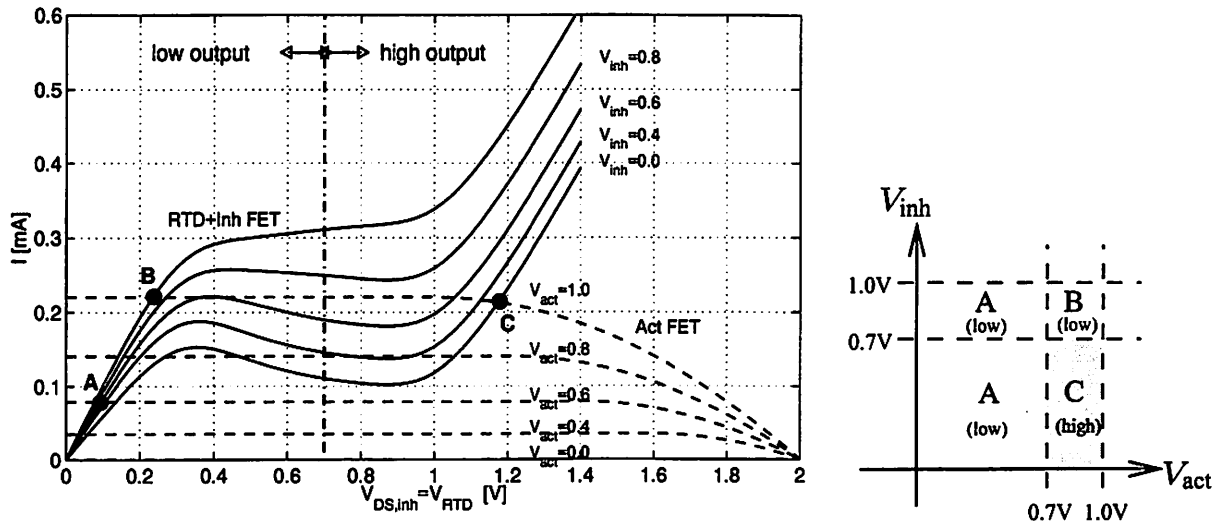
We conclude that the circuit performs the operation OUT=ACT·$\overline{\text{INH}}$, as visualized in Fig. 5 (b), where OUT, ACT, and INH are the logic states of the output, the input at the activating gate, and the input at the inhibiting gate, respectively. To determine the threshold level between logic "low" and "high", the quadratic dependence of the drain-source current on the gate voltage

$$I_{DS} = \frac{k_p}{2}(V_{GS} - V_T)^2 \tag{6}$$

has to be taken into account. Since

$$I_{\text{DS}}(V_{\text{GS}} = \sqrt{0.5}\text{V}) = \frac{1}{2} I_{\text{DS}}(V_{\text{GS}} = 1\text{V}),$$

we get, for $V_T = 0$, a threshold voltage of 0.7V, which is indeed reasonable, as the NDR region in Fig. 5 (a) extends approximately from 0.4V to 1.0V – the threshold level lies exactly in the middle of these two boundaries. The circuit is extendible to multiple inputs in a straighforward



(a) Combined I–V characteristics

(b) Circuit output

Figure 5: Characteristics and output of the circuit as a function of V_{act} and V_{inh}. V_{DD}=2V.

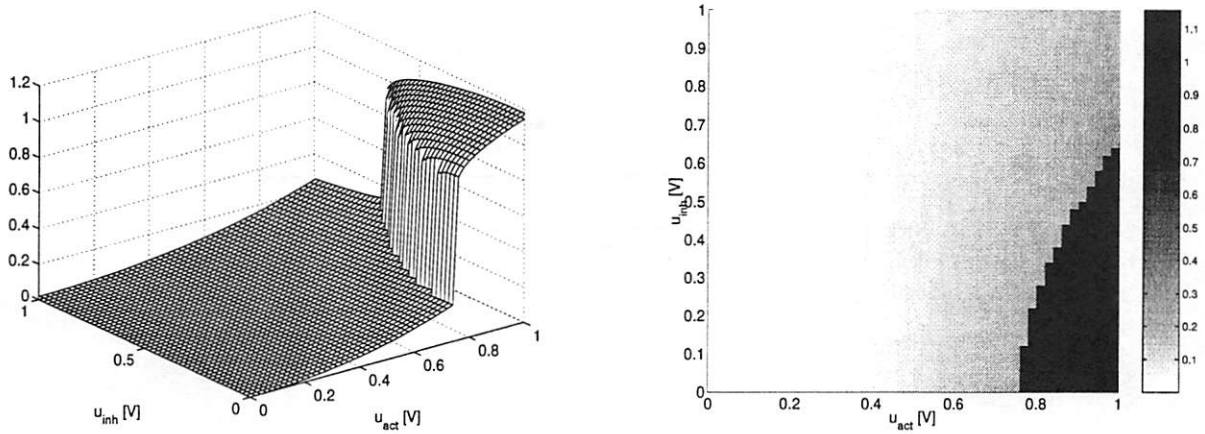
manner by including additional transistors parallel to the activating and inhibiting transistor, respectively.

2.2 Simulation results

In Fig. 6, the results of the Spice simulation are displayed. The two-dimensional plot (b) looks qualitatively similar to Fig. 5 (b). Note the abrupt ascent of the voltage between the "low" and "high" output levels, the circuit produces a perfectly binary signal.

The size of the "high" (black) area increases with increasing transconductance of the transistors.

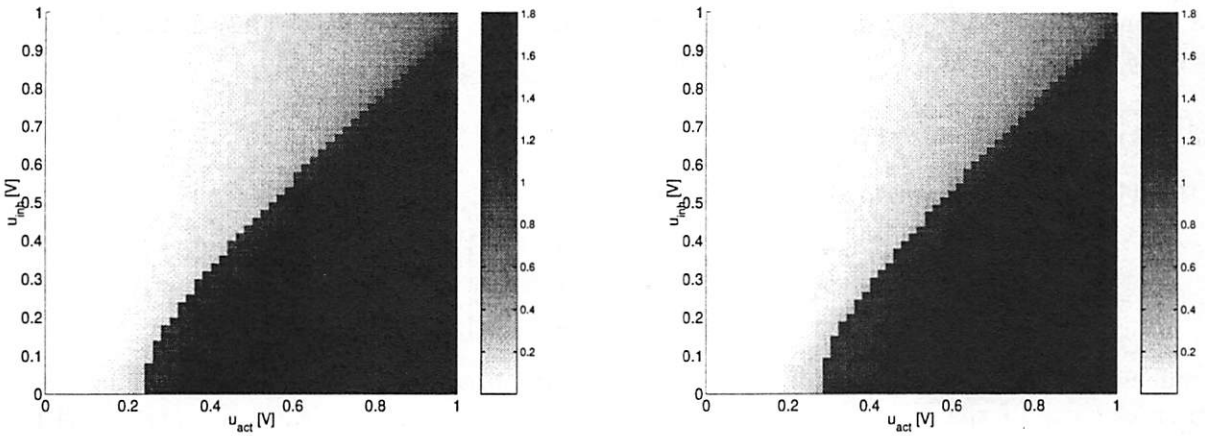
To build a CNN cell, we basically need a *comparator*, i.e., an output function whose "high" area is a triangle and ideally covers half of the input space. With 10 times larger transconductances, this can, in fact, be achieved closely, as depicted in Fig. 7. Due to the region of negative



(a) 3D plot

(b) 2D plot with uniform grayscale

Figure 6: Circuit output as a function of u_{act} and u_{inh} (Spice simulation).



(a) Decreasing u_{act}

(b) Increasing u_{act}

Figure 7: Comparator (Spice simulation). Hysteresis causes the slight difference between the two outputs.

differential resistance, the transistion from the "low" to the "high" state (Fig. 7 (a)) does not occur at precisely the same voltage as the opposite transition (Fig. 7 (b)). This *hysteresis* may be overcome by using a clocked supply voltage, which would force the circuit to always start at the "low" state, as proposed in [12].

In the proposed circuit, the three basic ingredients needed for a fixed-template uncoupled CNN cell are implemented with a minimum amount of circuitry, by exploiting the physical properties of FETs and RTDs:

Multiplication:	The input voltage is multiplied by the transconductance of the FETs.
Summation:	The currents of the individual transistors, which are connected in parallel, sum up. The difference between the activating and the inhibiting current sum flows into the RTD.
Nonlinear output function:	This is the task of the RTD. Depending on whether its current is negative or positive, it is put in one of the stable states, thus producing a binary output voltage.

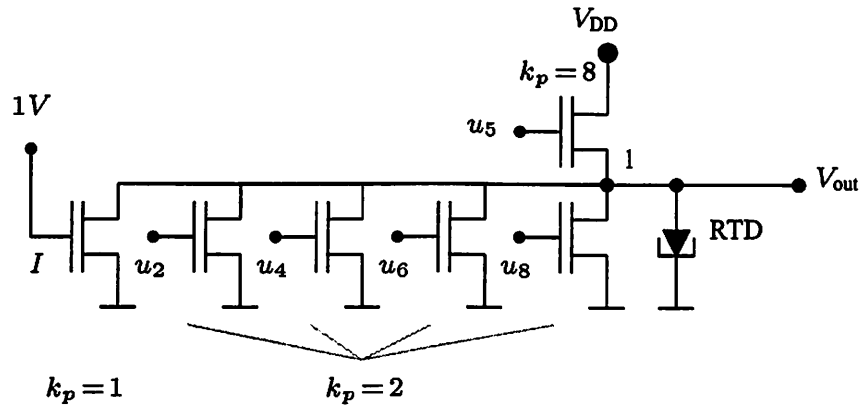


Figure 8: RTD-based CNN cell for edge extraction.

This cell is, in fact, a circuit realization of the equation (5). In this context, the fixed template B is the so-called *transconductance* template. Since the relationship between the transconductance and the drain-source current is linear, existing template values can readily be used, as demonstrated in the next Subsection.

2.3 An Example: Edge Extraction

A robust version of an edge extraction template is

$$B = \begin{bmatrix} b_1 & b_2 & b_3 \\ b_4 & b_5 & b_6 \\ b_7 & b_8 & b_9 \end{bmatrix} = \begin{bmatrix} 0 & -2 & 0 \\ -2 & 8 & -2 \\ 0 & -2 & 0 \end{bmatrix}; \qquad I = -1. \tag{7}$$

Assume the transconductances of the FETs are normalized to multiples of k_{p0}. Since the center element of the B template is positive, there is one single *activating* transistor with $k_{p,\text{act}} = 8k_{p0}$; the four off-center entries are negative, we thus have four *inhibiting* transistors with $k_{p,\text{inh1}} = 2k_{p0}$, and for the bias, there is an additional *inhibiting* FET with constant input and $k_{p,\text{inh2}} = k_{p0}$. In Fig. 8, this circuit is shown with transconductances normalized to $k_{p0} = 0.5\text{mA/V}^2$. Its logic output equation is

$$y_5 = \text{sgn}\big(8u_5 - 2(u_2 + u_4 + u_6 + u_8) - 1\big),$$

if the numbering from (7) is applied, where the center cell 5 is the cell under consideration.

2.4 Discussion

In this Section, we have proposed an extremely simple RTD-based circuit for Boolean CNN cells. The lack of programmability is a serious disadvantage, but specific applications may not require universal cells. We conclude that with RTDs, when sacrificing generality, extremely compact CNN circuitry can be designed.

In contrast to standard CNN cells, there is no macroscopic dynamic process involved; the only capacitances in the circuit are those of the FETs and the RTD. Thus it can be expected that the switching speed of the binary output will be in the order of tens of picoseconds [2].

Compared to the circuit proposed in [12], where a two-input logic circuit consisting of two Schottky diodes and three RTDs is proposed, the fan out is sufficient to drive a large number

of gates in subsequent logic stages. Hence, in principal, feedback is possible.

One major disadvantage is, however, the fact that the input voltages at the activating gate, u_{act}, have to be generated relative to the output node. If, instead, the gate-to-ground voltage of the activating transistor were used, the transistor current would change abruptly when the output toggles, which would, in turn, force the circuit into a different equilibrium. The usage of PMOS transistors may be considered to overcome this problem; however, this would complicate monolithic integration and reduce the switching speed of the circuit considerably, since the hole mobility in GaAs is more 20 times smaller than the electron mobility – it is even smaller than the electron mobility in silicon. This obstacle and the fact that the circuit lacks programmability are the main reasons why more complex (and more versatile) circuits will have to be designed and studied. A very promising candidate is the circuit presented in [1, 13], which is studied in more detail in the next Section.

3 An RTD-Based CNN Cell for Arbitrary Boolean Functions

In all current digital applications of RTDs, the *local activity* property of the NDR is not really exploited, but merely the bistability property, because the third equilibrium point in the NDR region is not stable in such circuits and therefore unwanted. However, by using the principle of nesting piecewise linear circuits, the so-called *Universal CNN Cells* [14], it is possible to take full advantage of all branches in the I–V characteristics of the RTD. The design principles and the functionality of the proposed RTD-CNN cell circuit are described in [1, 13]; here, we will concentrate on the issues related to model-based simulation in Spice.

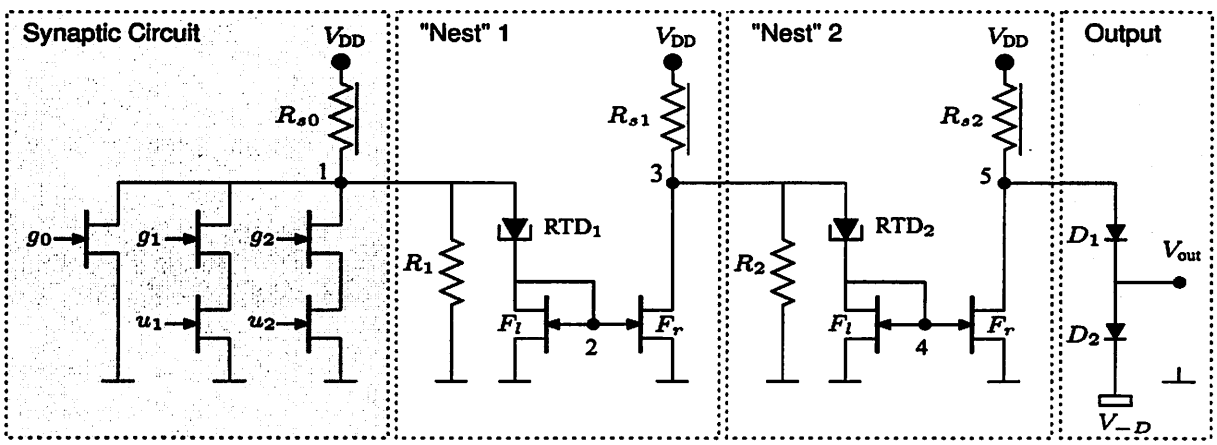


Figure 9: The RTD-CNN cell circuit with 2 inputs and 2 nests.

3.1 Description of the circuit

The circuit (Fig. 9, specifications in Table 1) contains GaAs FETs, RTDs, conventional resistors and diodes, and the so-called *saturated resistors*, which serve as a current source, but are more compact and can be more accurately built than the usual depletion-mode FET with its gate connected to the source [15]. The I–V properties of the RTD deviate noticeably from the piecewise linear model proposed in [13], which entails some necessary adjustments of the saturated resistors. In fact, the circuit reacts rather sensitively to changes of their values.

The transistors connected to the RTDs should exhibit a negligible voltage drop, i.e., they should have a large transconductance, while, at the same time, a current amplification by a factor of 10 must be guaranteed between F_l and F_r. The transconductance of F_r is therefore relatively high (see Table 1). However, it should be pointed out that this circuit is by no means optimized with respect to area and power consumption. Once correct operation of the circuits is established, the current RTDs can be easily replaced by others with smaller peak and valley voltages and currents, which, in turn, permits the usage of smaller transistors and reduces both area and power consumption.

The output circuit consists of two generic diodes to shift the voltage from node 5 to "low" and "high" values that correspond to the respective values at the inputs u_i.

g_0, g_1, g_2	synaptic inputs (template parameters)	$0 - 0.4V$
u_1, u_2	binary inputs	low: 0V, high: 0.4V
V_{DD}	voltage source for saturated resistors	3V
R_{si}	saturated resistors	$R_{s0} = 0.8\text{mA}$, $R_{s1} = 1.775\text{mA}$, $R_{s2} = 1.175\text{mA}$
g_0 transistor	synaptic transistor	$k_p = 1.5\text{mA/V}^2$
g_1, g_2 transistors	synaptic transistors	$k_p = 5\text{mA/V}^2$
u_1, u_2 transistors	synaptic transistors	$k_p = 50\text{mA/V}^2$
R_1	linear resistor	$R_1 = 2.2\text{k}\Omega$
R_2	linear resistor	$R_2 = 2\text{k}\Omega$
F_l	GaAs FET	$V_T = 0\text{V}$, $k_p = 5\text{mA/V}^2$
F_r	GaAs FET	$V_T = 0\text{V}$, $k_p = 50\text{mA/V}^2$
D_i	standard diodes	
V_{-D}	negative voltage source	$V_{-D} = -0.2\text{V}$

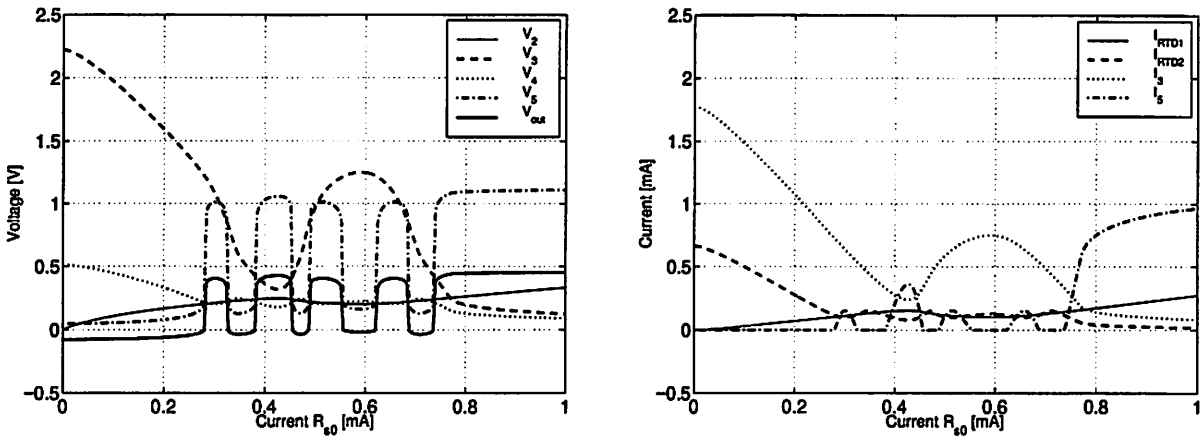
Table 1: Properties and specifications of the devices in the circuit.

3.2 Simulation results

First, we demonstrate that the "nests" with the RTDs in fact operate as desired. The synaptic transistors are disconnected, and the node voltages are plotted as a function of the current from the saturated resistor R_{s0} (Fig. 10). The output voltage is approximately rectangular, with equally spaced rising and falling flanks, and all $3^2 = 9$ flanks predicted by the theory are present between 0.2 and 0.8mA. Hence, with this small piece of circuitry, we are able to generate output voltage which depends in a highly nonlinear manner on the input current and is, at the same time, regular enough to be exploited for Boolean functions!

With an additional FET at the output, parallel to D_2, with its drain connected to the gate, it is possible to get rid of the additional voltage source V_{-D}. The FET ensures that a "low" voltage of 0.2V at node 5 results in a zero output voltage (Fig. 11).

It remains to show that the synaptic circuit can be used to *program* the cell. The g_1 and g_2 transistors (we might actually call them *template* transistors) together should sink the whole R_{s0} current if turned "on", i.e., $V_G = 0.4\text{V}$. With a maximum R_{s0} of 0.8mA, the transconductance is $k_p = 2\,(0.8\text{mA}/2)/(0.4\text{V})^2 = 5\text{mA/V}^2$. The transistor g_0 can be used to toggle between even and odd Boolean functions; in the "on" state, it will sink 0.12mA which implies $k_p = 1.5\text{mA/V}^2$. In Fig. 12, the output voltage is plotted as a function of g_1 and g_2 for $u_1 = u_2 = 0.4\text{V}$ ("high").



(a) Node voltages

(b) Currents

Figure 10: Simulations for the case of disconnected synaptic transistors.

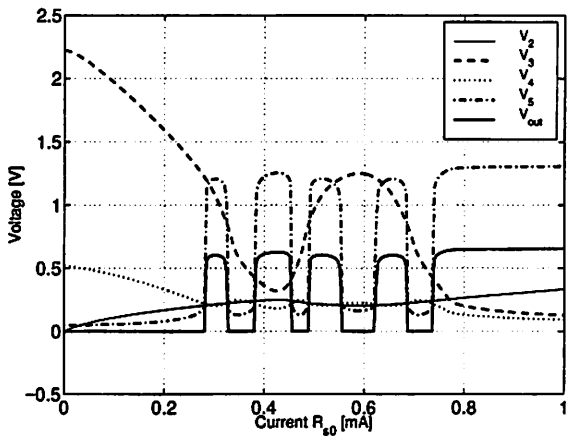


Figure 11: Node voltages with transistor output in the case of disconnected synaptic transistors.

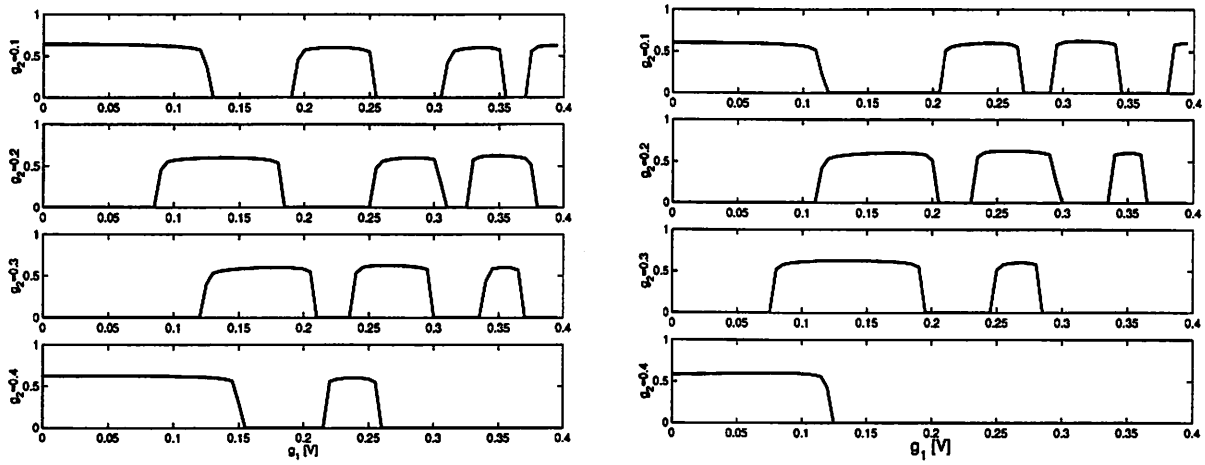
4 Conclusions and Outlook

We have demonstrated the impressive capabilities of resonant tunneling diodes for a new type of uncoupled CNN cells. The number of devices per cell is greatly reduced, while, at the same time, the functionality is enhanced, since any possible Boolean function, including the linearly non-separable ones, can be programmed on this cell.

The Spice simulations, which are based on a physial model of the RTD, show good agreement with the theoretical results in [13]. Conversely, replacing the actual I–V function of the RTD by a simple piecewise linear characteristics seems to be a viable way for the design of analog RTD-based circuitry, which substantially reduces the computational effort.

In our further work, we will try to develop a systematic method to transform standard CNN templates into genes for our new cell model. To achieve (at least) the same functionality as the standard CNN, we will also incorporate feedback loops, i.e., add circuitry to implement the A template.

One of the major concerns in such advanced cell models is the *robustness*. It may turn out that some of the Boolean functions are highly sensitive to deviations in the template parameters, thus



(a) $g_0 = 0$ (b) $g_0 = 0.4$

Figure 12: Output voltage as a function of the template parameters g_0, g_1, and g_2.

requiring an accuracy which is beyond the possibilites of the current technology. Theoretical investigations and extensive Monte Carlo simulations will be needed to get deeper insight into this problem.

Another task is the optimization of the circuit with respect to area and power consumption. Only together with minimum-size transistors, the RTD will display its excellent properties. In this context, we might also consider *multipeak RTDs*, which are very promising in the field of multi-valued logic [16].

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