ADAPTIVE CALIBRATION METHODS FOR AN IMAGE-REJECT MIXER

by

Isaac Sever

Memorandum No. UCB/ERL M01/36

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Adaptive Calibration Methods for an Image-Reject Mixer

by Isaac Sever

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II.**

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Adaptive Calibration Methods for an Image-Reject Mixer

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Chapter 1

Introduction

1.1 Motivation

The wireless communications market has grown substantially during the last decade. Recent advances in wireless technology have reduced the size and cost of mobile radios while improving performance. The increasing level of integration in wireless circuits has led to many of these improvements. However, increased integration is dependent on the development of novel transceiver architectures that allow the designer to eliminate many large discrete electronic components and to combine multiple circuit blocks on a single chip.

At the same time, numerous wireless standards have been introduced which dictate the performance specifications of the hardware in wireless devices. Hardware requirements differ substantially between wireless communications applications. The implementation of multiple cellular standards in a single architecture also requires novel transceiver design approaches. Currently, most analog receiver front-ends use multiple integrated circuits fabricated in different processes. It is difficult to meet the requirements of multiple standards using discrete components and simultaneously reduce the size of a receiver.

A novel multi-standard image-reject receiver was proposed in [1,2]. In past, image-reject designs have focused on careful circuit layout and matching in order to achieve maximum performance. This design features a different approach - in order to allow the system to support multiple standards, the mixer has the capacity for self-calibration. The self-calibration procedure can be used to optimize system performance over a wide frequency range. This improves the system performance for each standard and allows hardware reuse. The increase in wireless networking with various wireless local area network (WLAN) protocols such as IEEE 802.11b (in the 2.4Ghz band) and 802.11a (in the 5Ghz band) [22] creates new opportunities for multi-standard receives. Migration from 802.11b to 802.11a will require a dual-band solution, and would be a good application of a multi-standard receiver.

The fundamental limitations of an image-reject receiver and past attempts to minimize the effect of circuit mismatches will be explored. A digital signal processing algorithm will be proposed that can be used to calibrate image-rejection mixers. The algorithm and custom VLSI implementations, with the minimization of their power consumption and circuit area in mind, will be explored.

1.2 Problem Statement

An image-rejection mixer uses complex phase shifts to allow the signal and its image to be processed differently. In this system, the RF carrier is translated to baseband by two pairs of quadrature mixers, which exploit the relationship between the image and the desired signal. By summing the baseband channels, the image frequencies cancel

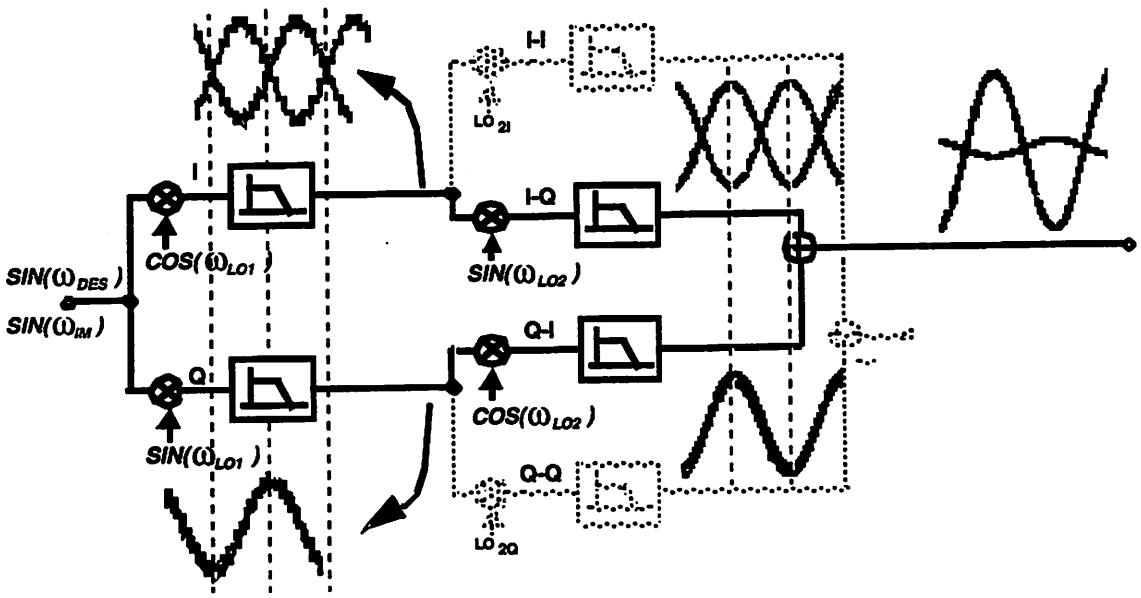


Figure 1.1 Time-Domain representation of Image-Rejection Mixer [Courtsey J. Rudell]

while the desired band adds constructively for both the I and Q channels. This is shown in the time-domain in the Figure 1.1:

The mixer's image-rejection ratio is limited by fundamental circuit mismatches. For perfect matching, the image-rejection ratio is infinite. In practice, however, there is a phase mismatch between quadrature oscillators and a gain mismatch between I and Q signal paths, which reduces the mixer's image-suppression.

At the system level, a high image-rejection ratio has numerous implications. In particular, it reduces the Q requirements of RF and Image-Reject filters. Typically, these filters have been implemented off-chip using discrete components; integration or complete elimination of these filters would substantially reduce the size, complexity and cost of a receiver.

In general, it is difficult to eliminate circuit mismatches and obtain a high image-rejection ratio. For optimal system operation, wideband image-rejection is required for a broad range of operating temperatures and signal power levels. This is not achievable

using a one-time optimization technique, such as trimming. This paper will explore calibration techniques that allow adaptive optimization of image-rejection mixers.

1.3 Organization of this Thesis

Chapter 2 gives the background of image-reject receivers and mixers. The merits of different receiver architectures and mixers for image-rejection are discussed. In Chapter 3 previously published image-reject receivers are reviewed. Chapter 4 gives a new proposed image-reject mixer calibration architecture, and Chapter 5 goes into the analysis of this algorithm. Chapter 6 gives the results of simulations of the proposed algorithm and compares it to the results of the previous solutions described in Chapter 3. Chapter 7 discusses implementation of the DSP algorithm and Chapter 8 concludes the thesis and suggests future work.

Chapter 2

Receiver and Mixer Background

2.1 Image-Rejection Receiver Architecture Background

The problem of wireless communication differs from many other communications problems because of the properties of the channel. The wireless channel is shared between all users, leading to a limited spectrum being allocated to each user. The wireless channel is also a harsh and dynamic environment with time varying interferers, multi-path and frequency selective fading.

2.2 Receiver Architectures

The super-heterodyne receiver has become the standard receiver architecture for wireless communication since its invention by Armstrong in 1917 [4]. The limited spectrum available means that the RF receiver must be able to process the desired wireless channel while simultaneously rejecting nearby interferers. The level of suppression of the image-tone often leads to very demanding filter requirements. For example in a standard heterodyne receiver the DCS-1800 standard calls for 60dB of attenuation in a pass band 200 kHz wide, 500kHz from the center of the desired channel. This requires a band-pass filter with a Quality Factor (Q) of around 10^5. High quality

discrete components, such as a Surface Acoustic Wave (SAW) filter or FBAR filter, are usually required to meet this requirement.

2.2.1 Super-Heterodyne Receiver

The super-heterodyne architecture translates the signal band to a lower frequency where the channel selection is performed. The frequency translation uses a mixer to convert the incoming frequency, ω_{RF}, to the intermediate frequency (IF) by multiplying by a local oscillator offset from the RF frequency by the amount of the IF, $\omega_{LO} = \omega_{RF} - \omega_{IF}$. This mixing produces the desired frequency component at the IF and higher frequency byproducts that are removed with low-pass filtering. Problems arise from the relationship between the LO frequency and the incoming RF frequency. Another incoming signal at a frequency offset by the same amount, the image-tone, is also mixed down to the same frequency as the desired signal. Once this mixing has occurred the image-tone can not be separated from the desired tone and corrupts the signal. The image tone at $\omega_{RF} + \omega_{LO}$ is also converted to ω_{IF}.

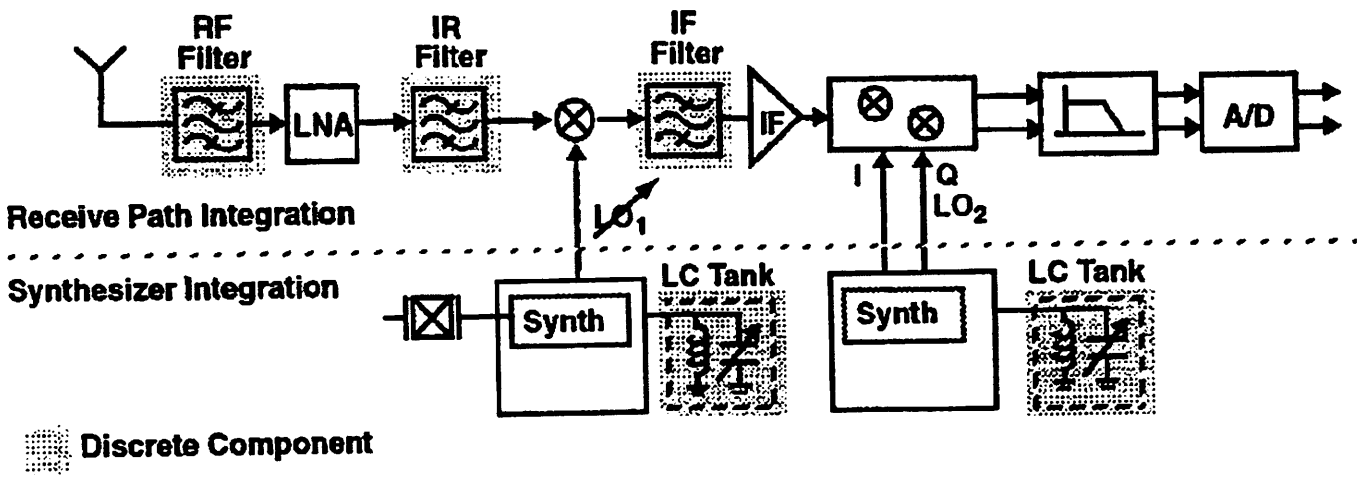


Figure 2.1 Super Heterodyne Mixer showing integrated and external components. [Courtsey J. Rudell]

The image tone can be in or out of band and has the potential to be higher power than the desired signal. Traditionally super-heterodyne architectures have been implemented with both integrated and discrete components. The common method of image-suppression in this case is to add external image-reject filters at the RF front end and immediately before the mixing stage in the receive path. These filters must have low attenuation in-band and high attenuation in the image band. If the IF is large enough the filter's Q will be low enough for a practical filter implementation, this must be traded off with channel selection which is easier at lower IFs.

2.2.2 Direct Conversion Receiver

A direct conversion receiver, or homodyne receiver, translates the incoming RF signal directly to baseband with one mixer. This architecture removes the IF and removes the image-rejection problem. Although direct conversion performs very well for image-rejection the direct conversion architecture suffers from many other performance disadvantages. The LO is the same frequency as the RF input, leakage from the LO to

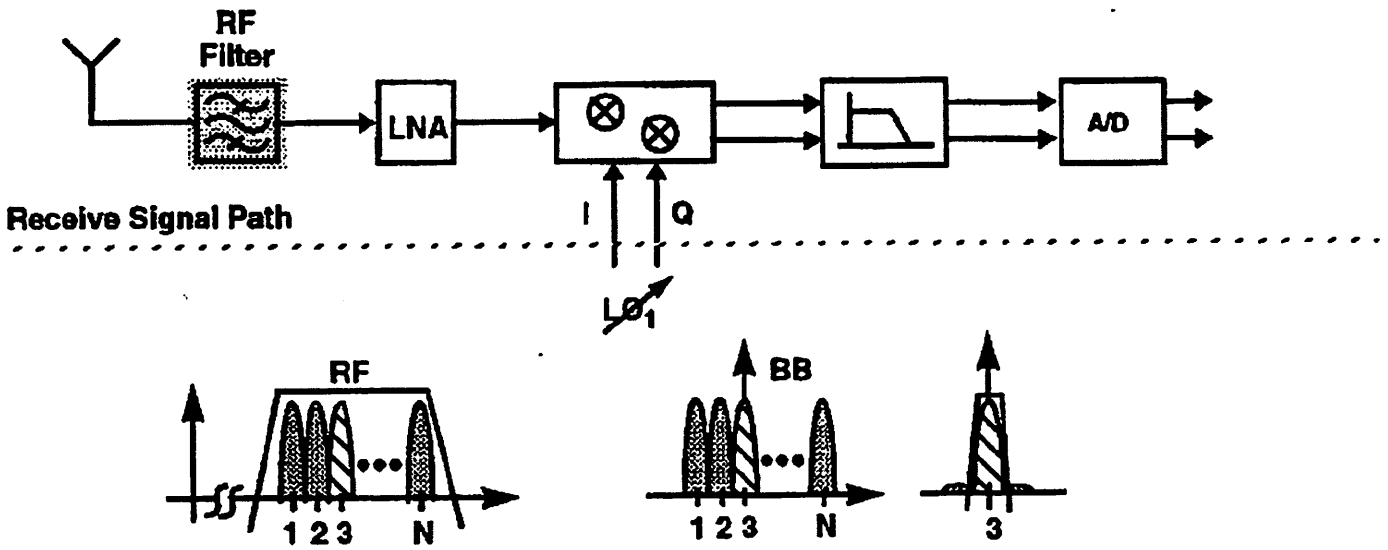


Figure 2.2 Direct Conversion Receiver. [Courtsey J. Rudell]

the mixer input and to the antenna causes DC offset at the mixer output that is time varying and difficult to remove.

2.3 Image-Reject Receivers

Image-reject receivers attempt to process the image frequency in order to suppress the image without the requirement for an external filter. If an accurate replica of the input band can be generated that contains the desired signal and the negative of the image signal, cancellation of the image can occur. The performance of these methods will depend on how accurately the negative of the image signal can be generated.

Single and dual-conversion image-rejection architectures can be designed to attempt this cancellation. Single-conversion architecture is based on the Hartley modulator [5] that creates a negative of the image with a quadrature mixer stage followed by quadrature phase shifters. The required quadrature phase shifters must be in the signal path so they are also required to be low loss, a condition that is difficult to achieve at high-frequency.

Dual-conversion architectures use the Weaver mixer [6] that replaces the phase shifters with a second quadrature mixing stage. Weaver mixers can be utilized in a wide-band double conversion receiver architecture[1,2].

2.3.1 Double Conversion Wide-Band Receiver

The dual conversion wide-band receiver proposed in [1] translates the entire channel band down to the IF with one mixer. A second mixer stage then converts a channel down to baseband with a channel select frequency synthesizer. This architecture

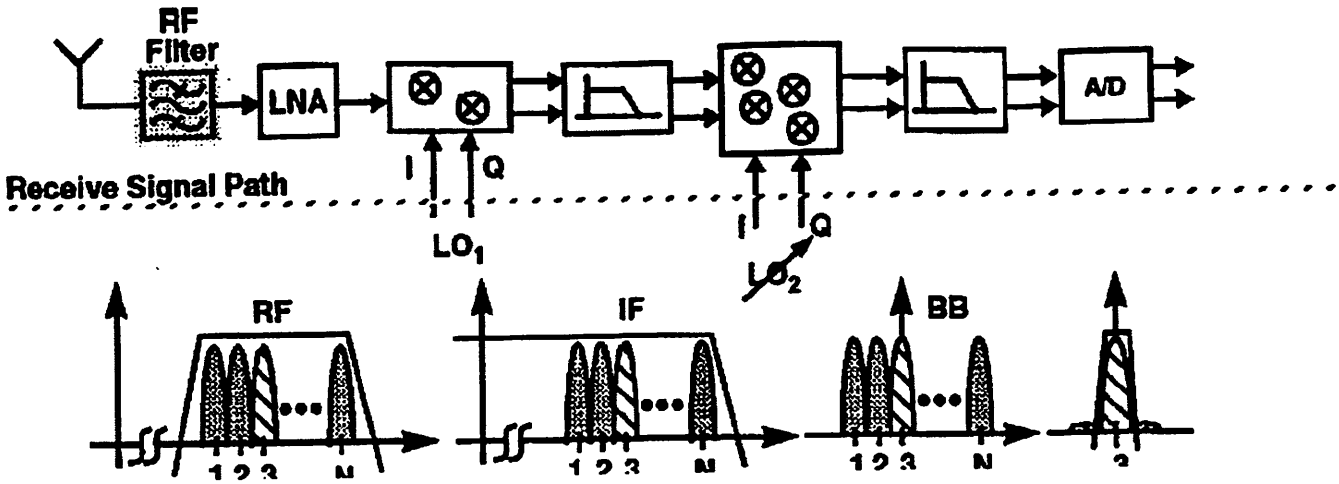


Figure 2.3 Double Conversion Wide-Band Receiver. First LO converts band to IF, where channel selection is performed by LO2. [Courtsey J. Rudell]

differs from a super-heterodyne receiver in that it translates the entire receive band to IF. Delaying the channel selection until IF is facilitates multi-standard features. The super-heterodyne architecture can provide superior performance but it relies on external components, increasing the cost and tailoring the receiver to a particular standard. Channel selection and filtering at baseband makes it possible to implement an integrated programmable filter to facilitate multi-standard operation.

The wide-band IF architecture offers advantages over direct conversion as well.

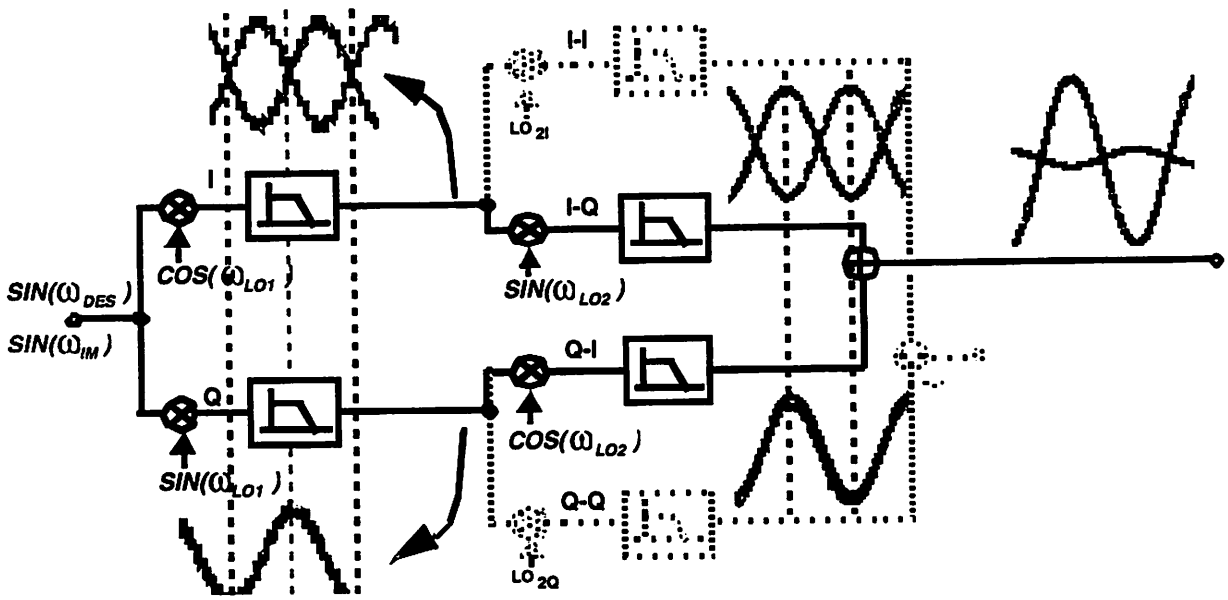


Figure 2.4 Time domain representation of Image-Reject Mixer. [Courtsey J. Rudell]

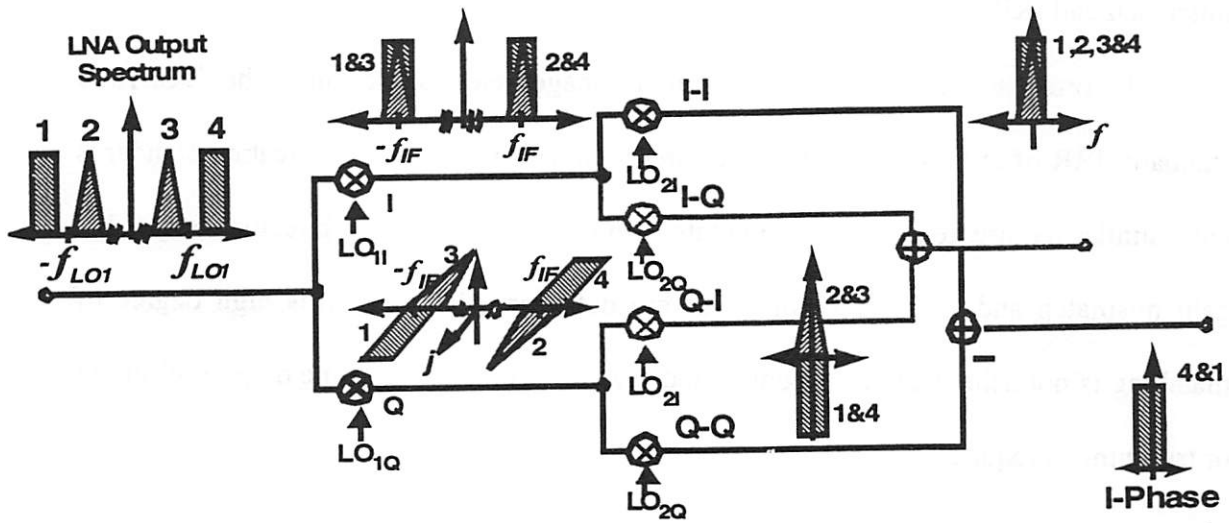
Because the second local oscillator performs channel selection the first oscillator does not have to be tunable and can be implemented with a fixed-frequency crystal oscillator and a Phase-Locked Loop (PLL). This oscillator has a much cleaner signal with lower phase noise and lower Q requirements for on-chip components.

The wide-band IF architecture's high integration and multi-standard capabilities also have disadvantages. Channel selection with the second tunable local oscillator increases the relative frequency tuning range required of the IF synthesizer. The external IF channel select filter is also removed which increased dynamic range requirements of the receiver blocks and makes adjacent channel interference more of a concern. The biggest problem comes from the non-ideality of the architecture. The dual-conversion architecture utilizes the Weaver mixer for image rejection that further helps to eliminate external filtering requirements. This image rejection is essentially limited by the inherent phase mismatch between the LOs and the conversion gain mismatch between the I and Q channels.

2.4 Image-Reject Mixers

The Weaver image-reject mixer provides high image-rejection ratios (IRR) by forming a negation of the image and summing it with the positive image at baseband to leave only the desired signal at the mixer output.

A time domain representation of the same architecture is shown in Figure 2.6. The frequency domain representation in Figure 2.5 shows how the image tone cancellation occurs. The problem comes from the non-idealities of the integrated receiver. For perfect matching the Weaver architecture provides infinite image-rejection.



In practice however the phase mismatch between quadrature signals and conversion gain

Figure 2.5 Frequency domain representation of Image-Reject Mixer. [Courtsey J. Rudell]

is a function of these mismatches. The image-rejection ratio (IRR) can be derived in terms of the mismatch as [2]:

$$IRR = \frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_1+\phi_2)}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_1-\phi_2)}$$

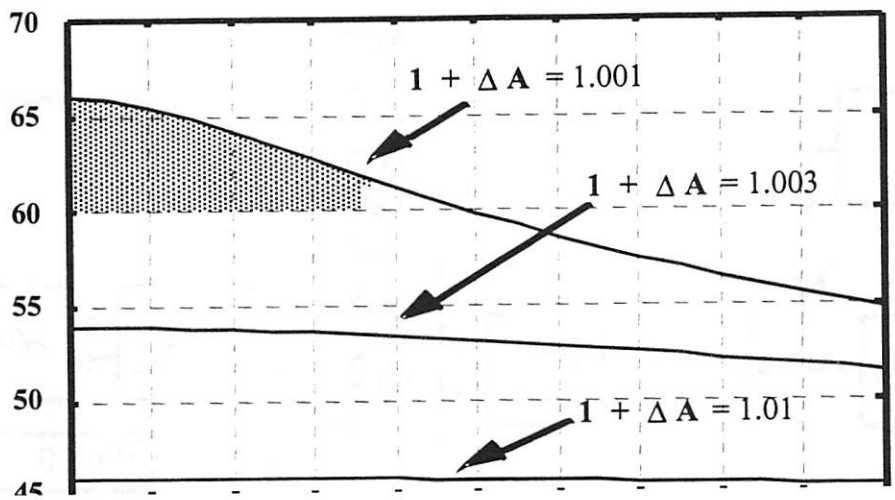


Figure 2.6 Image-Rejection Ratio (IRR) as a function of phase mismatch, for 3 gain mismatch points. [Courtsey J. Rudell]

Using this formula we can find the relationship between the phase mismatch, gain mismatch and IRR.

In order to provide sufficiently high image rejection to meet the DCS1800 standard, IRR of at least 60dB IRR is desired. Other wireless communication standards have similar requirements. To provide this with the wide-band IF architecture only 0.1% gain mismatch and 0.1 degrees of phase mismatch are allowed. This high degree of matching is not achievable using only good layout techniques, so some degree of tuning or trimming is required.

2.5 Receiver Implementation

The receiver designed by Rudell [2] uses the DCS1800 standard. In order to meet the substantial blocking requirements of this standard the weaver-mixer can be self-calibrated to improve image rejection. The phase of the second LO and the gain of the I path can be adjusted to improve the path matching. In order for calibration to occur a calibration tone is generated at the image frequency and injected at the input of the mixer.

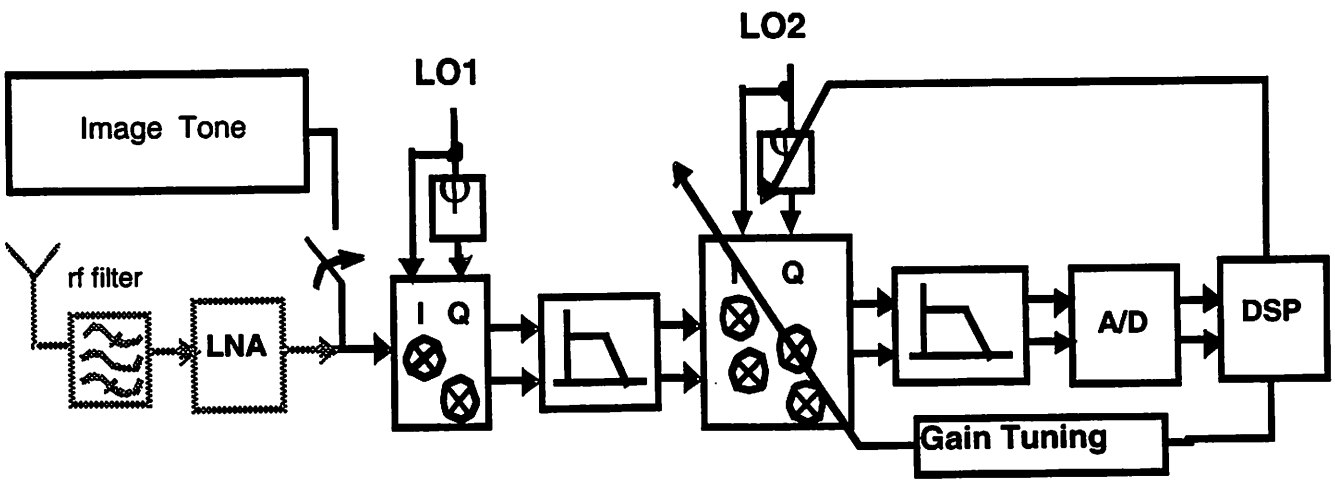


Figure 2.7 Image-Reject Receiver showing calibration method. Calibration image tone is injected at the input and a DSP uses the output of the A/D converter to tune mixer 2 gain and LO2 phase. [Courtesy J. Rudell]

The output of the A/D converter can be monitored by a digital signal processor (DSP) which adjusts the gain and phase to improve the image rejection. The calibration tone can be applied to each cannel when the receiver is powered up. During operation and over time the inherent phase and gain mismatch may very; this issue can be addressed with periodical re-calibration at convenient times (i.e. between TDMA frames).

The tuning mechanism is illustrated in Figure 2.7 of the receiver shown. The first LO has a fixed 90° phase shift between the I and Q input ports. In the second LO this shift is variable and is tuned to correct for the phase error between the oscillators. The gain of two of the four mixers in the second stage is varied to tune the gain mismatch between the signal paths. The DSP block tunes the gain and phase independently and the optimum values are stored in memory for each channel.

The receiver is designed to work with the DCS1800 standard and uses a first IF of 400 MHz. The standard calls for 60dB of image suppression at the output of the mixer. The IRR achieved by the receiver depends on the accuracy of the tuning of both the gain and phase. One-percent gain matching between paths was achievable using good layout techniques. To insure tuning would be possible, the receiver was designed to compensate for a maximum +/- 5% gain error. This gain tuning was realized by varying the tail current of two Gilbert mixers fed by LO2. A requirement for the minimum gain tuning resolution of 0.001 between signal paths was determined from simulations. From this, the total resolution required was found to be:

$$\text{Resolution} = \text{Max}\ \Delta A/\text{Min}\ \Delta A = 0.05/0.001 = 50\,\text{levels} = 6\,\text{control bits}$$

Similar simulations were performed to determine a phase resolution of 0.05° with a tuning range of 3°. This required 8 control bits for phase tuning. These digital gain and

phase tuning mechanisms were built into the receiver using current DACs. With these tuning knobs available to adjust the path matching characteristics and improve the receiver image rejection, a method was needed to determine when the maximum image-rejection was reached.

The phase shifter to produce the quadrature local oscillator signals can be performed using a poly-phase filter followed by fine-tuning adjustable buffers [1]. For this implementation a different approach was used, the phase shifter for the second local oscillator consists of a set of D-latches that perform a divide by 4 operation to generate quadrature signals, shown in Figure 2.8. This is followed by a series of buffers that drive the mixer local oscillator switches and tune the local oscillator phase for maximum image suppression [2].

Several solutions previously published for improving image-rejection are described in Chapter 3 and a new solution is proposed in Chapter 4.

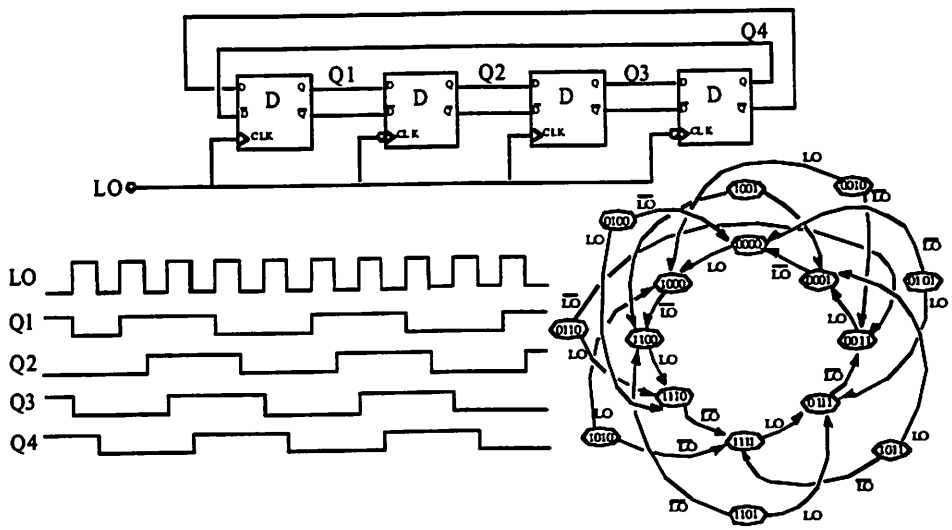


Figure 2.8 D-Latches configured to perform a divide by four and generate quadrature signals. The timing and state diagrams are also shown. [Courtesy J. Rudell, 2]

Chapter 3

Prior Work

3.1 Prior Work

Several solutions have been implemented in an attempted to improve the image-rejection of receivers on chip so that external filtering requirements are reduced or eliminated. Solutions attempt to minimize the image tone seen at the intermediate frequency by using image-reject mixer architectures as described in Chapter 2. These designs suffer from the limitations of the rejection due to the matching between the I and Q channels. If there are phase mismatches between the local oscillators on chip or between the quadrature phases of each oscillator used in the mixing, the image rejection will be degraded. Similarly a gain mismatch between the I and Q paths will lower the image-rejection. Methods to improve the image-rejection focus on various ways to reduce this mismatch. Designers have used good layout techniques alone, individual trimming and tuning and active adjustment to correct for the mismatches.

3.1.1 Hand Tuning

In 1997 Rudell et al [1] used an individual tuning approach with a monolithic receiver. The core of the wideband double IF receiver architecture was the image-reject mixer consisting of six mixers that performed the double down conversion.

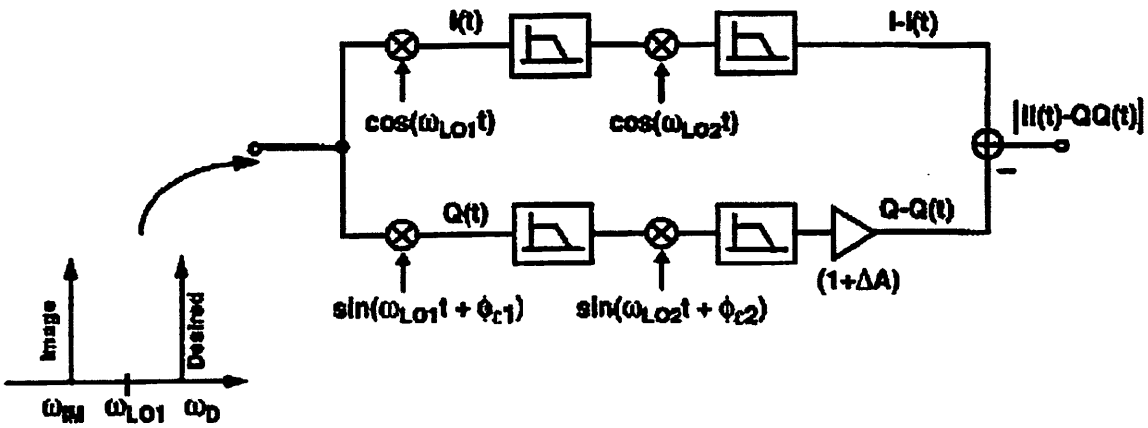


Figure 3.1 Image-Reject Mixer using Weaver architecture. [Courtesy J. Rudell]

The gain mismatch between the I and Q channels could be tuned with a variable gain amplifier and the phase mismatch could be adjusted by varying the phase of the second local oscillator. Using this design and hand tuning the receiver delivered 45 dB of image-rejection on-chip.

Good layout techniques gave Long and Maliepaard 44 dB of rejection on-chip in 1999 [7]. Their dual doubly-balanced mixer architecture used common-centroid and symmetric layout techniques to improve the matching enough replace the external

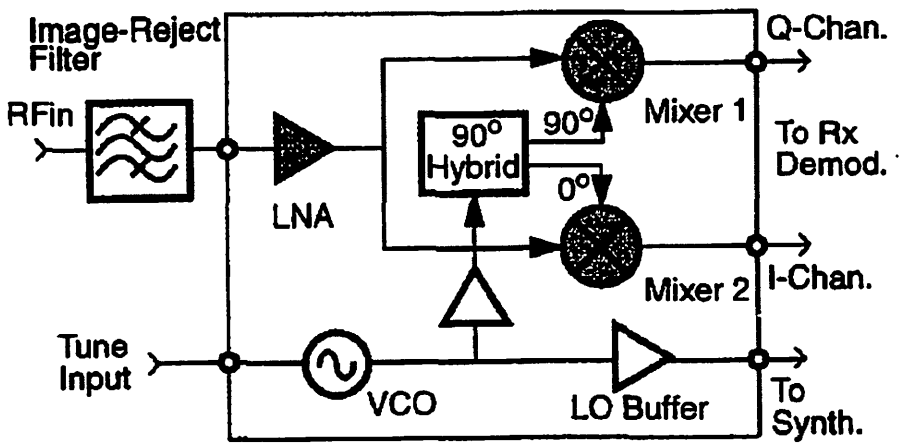


Figure 3.2 Dual doubly-balanced mixer architecture used for image-rejection with good layout matching. [7]

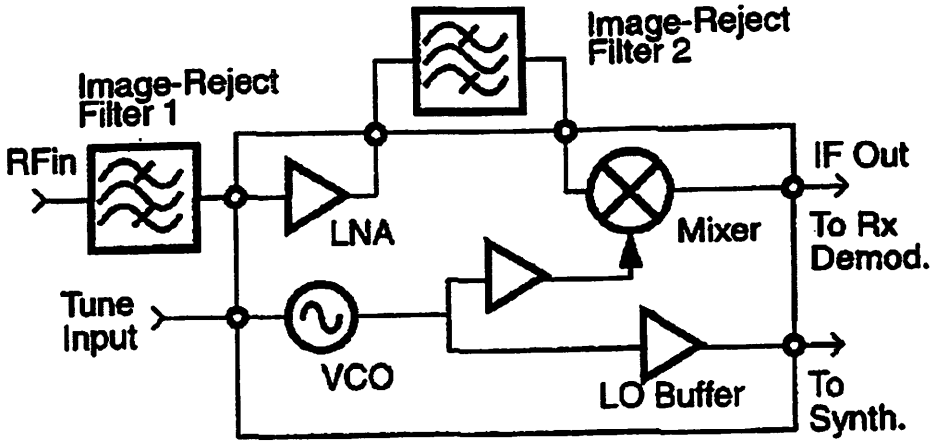


Figure 3.3 Dual doubly-balanced mixer architecture used for image-rejection. [7]

interstage image-reject filter used in typical heterodyne receivers.

A follow up presented at ISSCC 2000 demonstrated a peak IRR of 80dB [8]. This chip used trimming to adjust the amplitude and phase between the I and Q signals at IF to calibrate for the mismatch. The phase angle between the LO signals was then adjusted by setting a bias current ratio to produce a phase tuning relatively independent of frequency. The amplitude errors at the output of the receiver were compensated by varying the gain. Although hand tuning and trimming methods are clearly unworkable for mass production receivers they proved that high IRRs could be realized on-chip. Changes in operating

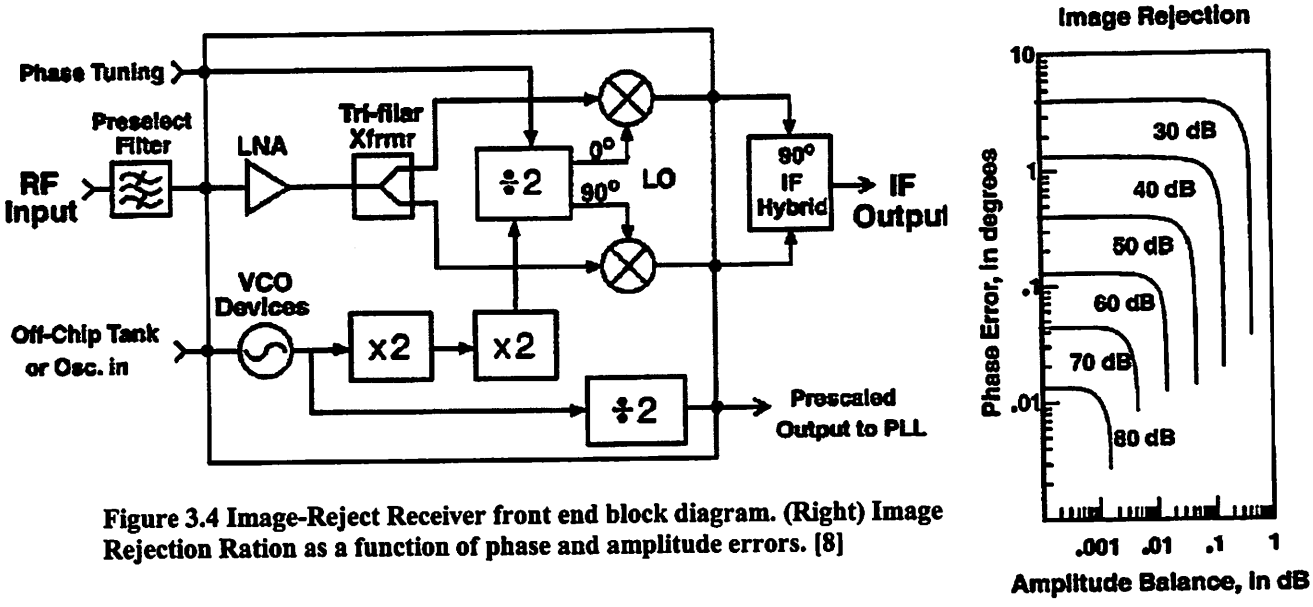


Figure 3.4 Image-Reject Receiver front end block diagram. (Right) Image Rejection Ration as a function of phase and amplitude errors. [8]

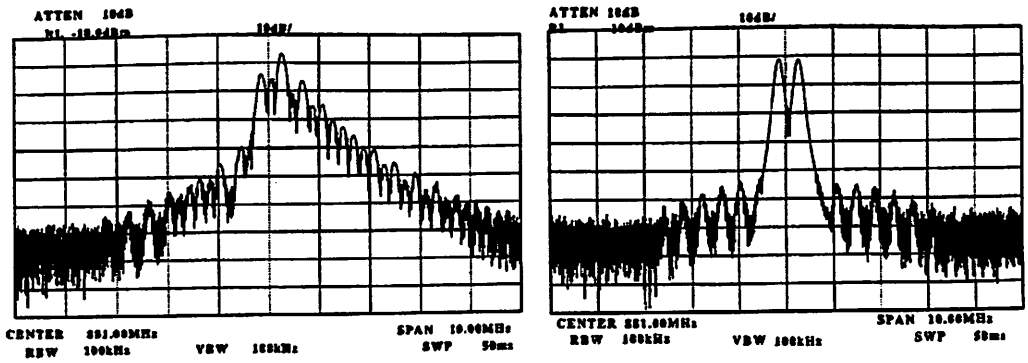


Figure 3.5 Improvement in phase characteristics of an RF amplifier after phase tuning. [9]

condition and environment such as temperate and drift are also not addressed by a one-time calibration method. For a commercial receiver an automatic method to perform the tuning on-chip is needed.

3.1.2 Analog Tuning

A phase adjustment scheme to linearize RF components by Faulkner [9] utilized calibration algorithms to quickly improve performance. By measuring the output power and using a direct search algorithm Faulkner was able to find the minimum in the output power, which correlates to the best linearity and noise performance. The algorithm converged by adjusting the phase to the optimum to improve amplifier output as shown.

An important improvement in the algorithm overcame the problem of

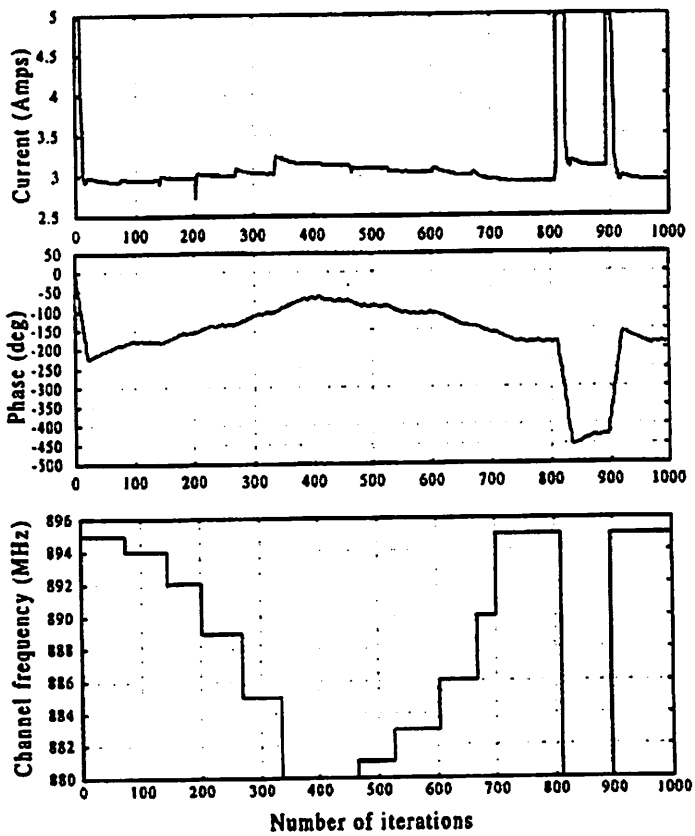


Figure 3.6 Iterative tuning of phase as frequency drifts, phase is modified by varying bias current. [9]

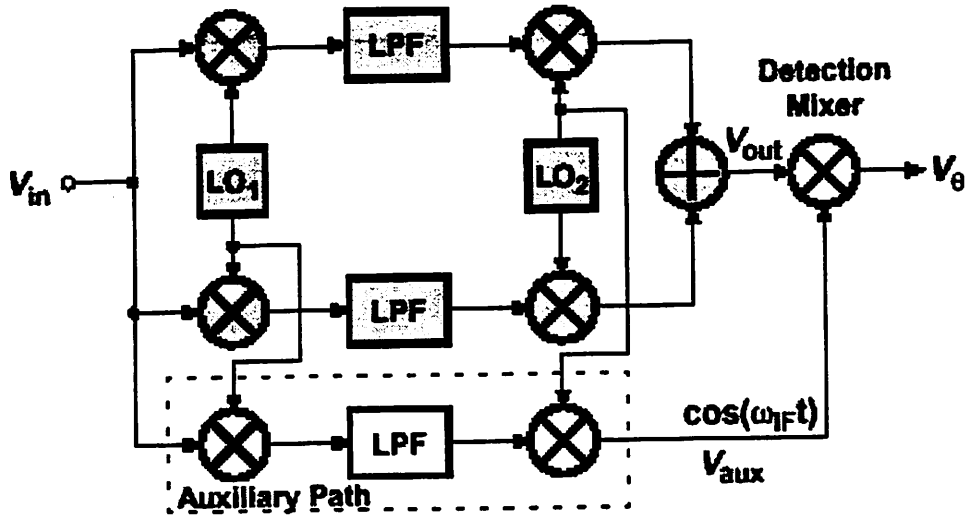


Figure 3.7 Image-RejectReceiver block diagram. Uses Weaver Mixer architecture and analog phase tuning. [10]

hysteresis by delaying reversal of iteration in the phase until three unsuccessful iterations were made. The improved calibration of phase and frequency is shown.

Another analog calibration technique for an image-rejection receiver was introduced in 2000 by Montemayor and Razavi [10]. This calibration detects phase and gain mismatches and drives them to zero with a negative-feedback loop. The phase calibration uses an error signal independent of gain derived by multiplying the output signal by $cos(\omega_{IF} \cdot t)$.

$$V_O = A \cdot V_m \cdot sin\left(\frac{\theta}{2}\right) \approx A \cdot V_m \cdot \left(\frac{\theta}{2}\right)$$

Figure 3.7 shows the realization of the error signal generation. An auxiliary path generates the $cos(\omega_{IF} \cdot t)$ in parallel with the signal path that is used for calibration. This error signal is then used in a feedback loop to tune the phase difference between the I and Q outputs of LO2. The full calibration loop for the receiver is shown in the Figure 3.8. Gain calibration can be achieved in a similar manner by multiplying the output with $sin(\omega_{IF} \cdot t)$ to obtain an error signal related to the gain mismatch.

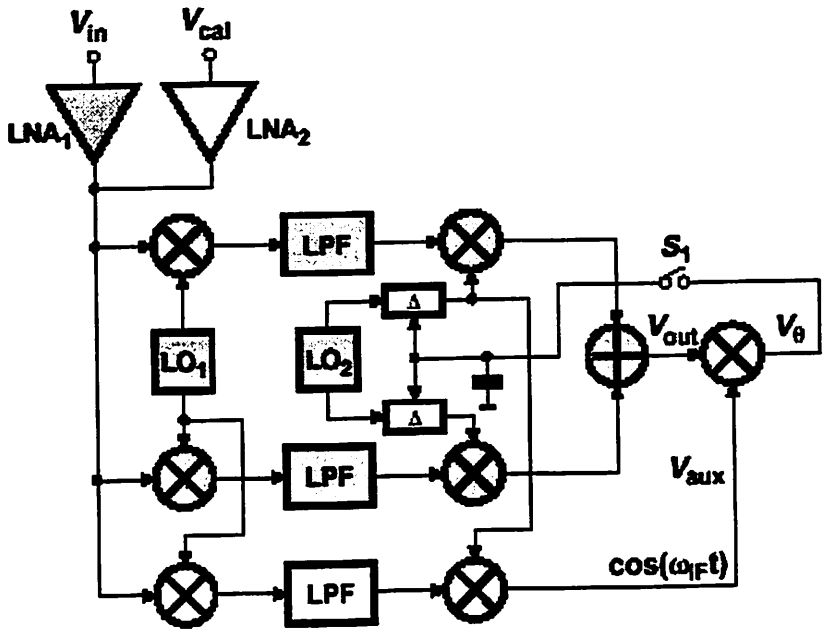


Figure 3.8 Complex receiver block diagram illustrating calibration using parallel down-conversion path and calibration of phase in LO2. [10]

The receiver designed used only phase calibration to achieve 57dB of image-rejection, improving over the un-calibrated rejection of only 17dB. Increased rejection would be expected with the addition of gain calibration.

3.1.3 Digital Tuning

A digital signal processing solution to on-chip calibration was presented at ISSCC 2001 [11]. Using a Weaver image-reject architecture with a sign-sign least-mean-squares (LMS) calibration achieved 57dB IRR.

The adaptation varied the phase of the I channel LO2 to compensate for the phase mismatch between the first and second LOs. A variable gain mixer used with the main mixer in the second stage provides the differential gain control. The sign-sign LMS block takes inputs from the I and Q channels and an error signal. The error signal is derived from the output with a simple comparator referenced to zero. Two additional

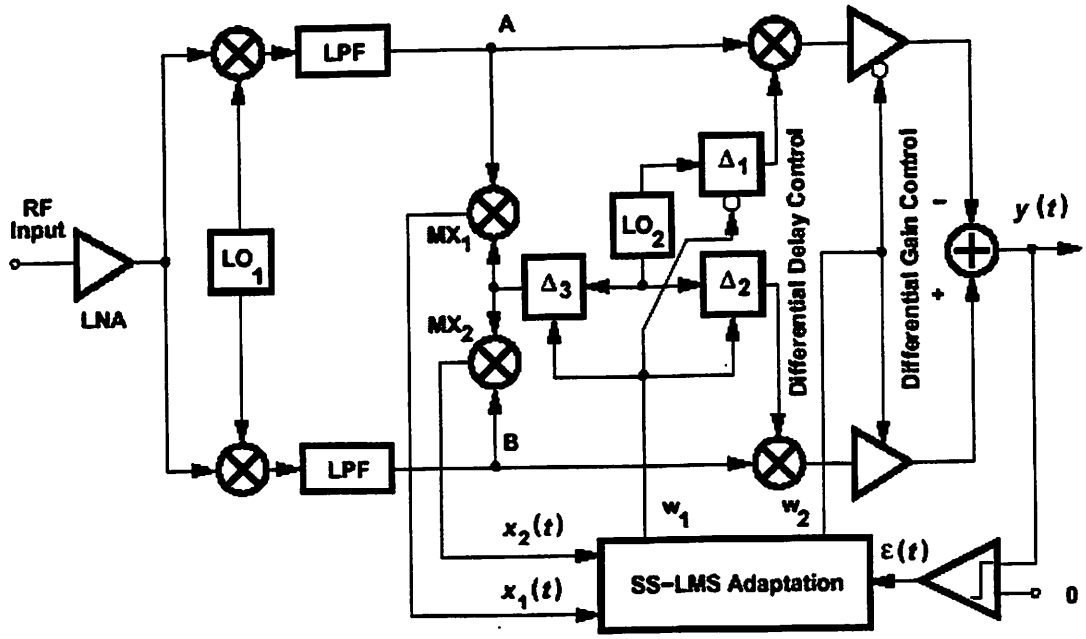


Figure 3.9 Image-Reject Receiver IC Implementation diagram. [11]

mixers are required to down-convert the inputs X1 and X2 to make them available for calibration. Because the adaptation is performed using a sign-sign LMS algorithm the adaptation block is implemented with comparators to produce the sign inputs, and then XOR gates and up/down counters that act as digital integrators.

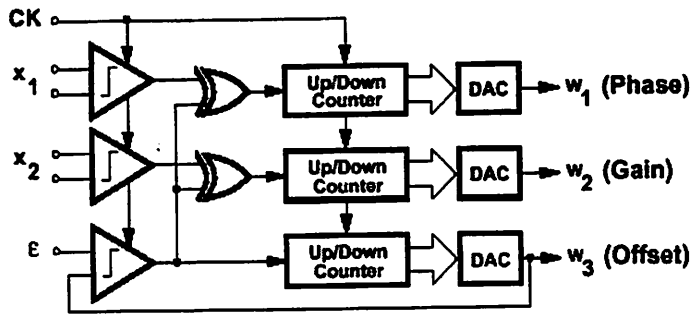


Figure 3.10 Sign -Sign LMS adaptation to tune the phase, gain and offset uses comparators, XOR gates and digital counters. [11]

3.1.4 Tuning based on Spectral Estimation

Recently, another on-chip calibration method was proposed by Desjardins for the second wideband double IF receiver architecture designed at UC Berkeley[12]. This

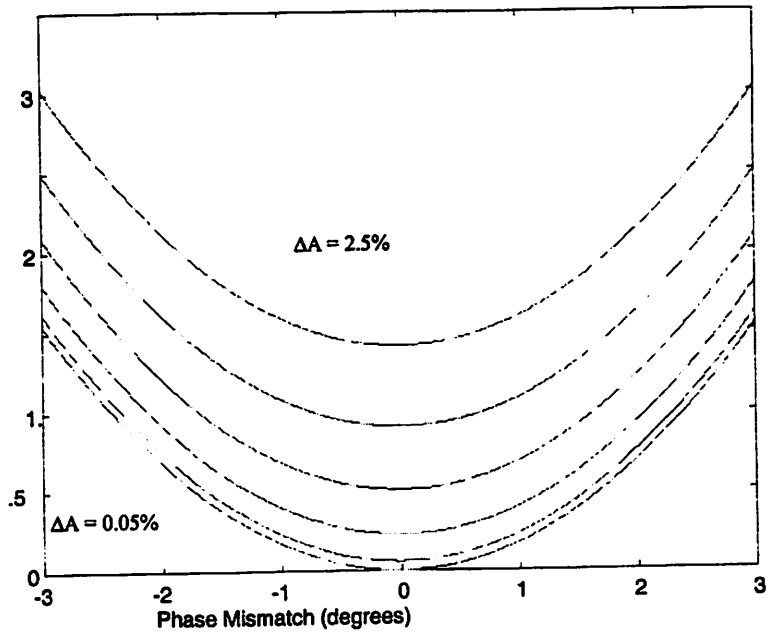


Figure 3.11 Optimization space for phase and gain tuning is well-behaved. [12]

dual-mode receiver uses a Weaver based image-reject mixer. The receiver converts the input down to a baseband centered around 100kHz where it is sampled by a 13bit ADC at 300 kHz. In calibration mode, an image tone is applied to the input, and the output can be monitored. If the value of the image tone at the output of the ADC could be determined during calibration it could be used to adapt the phase and gain to tune out the mismatch between the I and Q signal paths. The magnitude of the image-tone was found to be a parabolic performance surface. Figure 3.11 shows that for a given gain mismatch, varying the phase mismatch away from perfect monotonically increases the output magnitude. This allows the minimum in this surface to be found with a relatively simple search. Desjardins' spectral estimation technique uses a discrete-fourier-transform (DFT) to find the value of the image-tone at baseband and then uses a finite state machine (FSM) to vary the gain and phase to find a minimum in the output image value. In

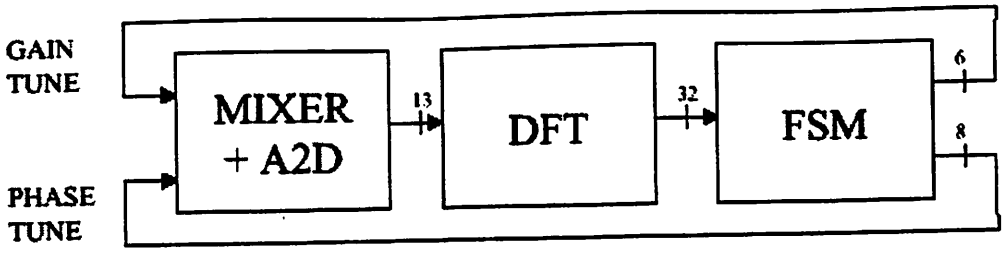


Figure 3.12 Spectral Estimation Tuning uses a discrete-fourier-transform (DFT) and a finite-state-machine (FSM) following the Mixer and A/D Converter. [12]

simulation this technique quickly converges to calibration values to give approximately 75dB IRR.

The relative performance metrics of these different solutions will be compared in the Results section of Chapter 6.

Chapter 4

Proposed Solution

4.1 Introduction to Least Mean Squares Algorithm

The least-mean-square algorithm is a technique for descending towards the minimum of a performance surface. A generalized procedure for finding a minimum requires an estimation of the gradient in each iteration [14]. When the gradient is known a step can be taken towards the minimum. General techniques such as to calculate the gradient call for calculations of the mean square error (ζ). Many algorithms such as Newton's and the steepest descent method require multiple calculations of the MSE in order to find a difference between estimated points on the performance surface.

The least-mean-square, or LMS, algorithm uses a specialized estimation of the gradient. Although the LMS algorithm can be used in a more restricted class of minimization (or maximization) problems it often requires simplified calculations. The LMS algorithm does not require off-line gradient calculations and estimations or repetitions of data. In many adaptive systems the LMS algorithm is the best choice.

4.1.1 LMS Algorithm

A general adaptive algorithm consists of an update equation to modify the values of the weights based on the error calculated. The calculation for the error simply consists of the difference between the estimated value d_k, and the product of the input vector X_k^T, and the weights to be adapted, W_k. The error equation is,

$$\varepsilon_k = d_k - X_k^T W_k$$

The gradient of the mean square error (MSE, ζ) can be estimated by taking short averages of the expected value of the square of the error term, $\zeta = E[\varepsilon_k^2]$. The essence of the LMS algorithm is to make an important approximation by taking ε_k^2 alone as an estimate of the mean square error, ζ. This greatly simplifies the calculations of the gradient. The gradient ∇_k simplifies in the following equation,

$$\nabla_k = \left[\frac{\partial \varepsilon_k^2}{\partial w_i}\right] = 2\varepsilon_k\left[\frac{\partial \varepsilon_k}{\partial w_i}\right] = 2\varepsilon_k(-X_k) = -2\varepsilon_k Xk\ .$$

Substituting this form of the gradient into the adaptive update equation leads to the LMS update equation.

$$W_{k+1} = W_k - \mu\nabla_k$$

$$W_{k+1} = W_k - \mu(-2\varepsilon_k X_k)$$

$$W_{k+1} = W_k + \mu 2\varepsilon_k X_k \quad \text{(LMS Update Equation)}$$

The LMS update equation works well for adaptive systems in which you have the input, X_k, and the error term available. This leads to the main drawback of the design implemented in the Der and Razavi paper described in Chapter 2 [11] . For an image-reject mixer the "input" term is not at the same frequency as the error term at the output

of the receiver. This means two additional mixers are required to down-convert the input for use in the tuning block.

4.2 Proposed Solution

The solution proposed in this research project used the LMS update equation for motivation in deriving tuning blocks to adapt the gain and phase weights towards their optimum value. The requirement for two additional analog mixers is eliminated in favor of all digital tuning blocks. These blocks take the digital output (13bit available in the DCS receiver implementation) from the ADC at baseband and adjust the digital control lines for the phase and gain tuning DACs. The analysis of these tuning blocks is detailed in the following chapter.

The phase and gain tuning block uses digital signal processing to derive a term that is correlated to the error of the phase and gain respectively. This error term is then

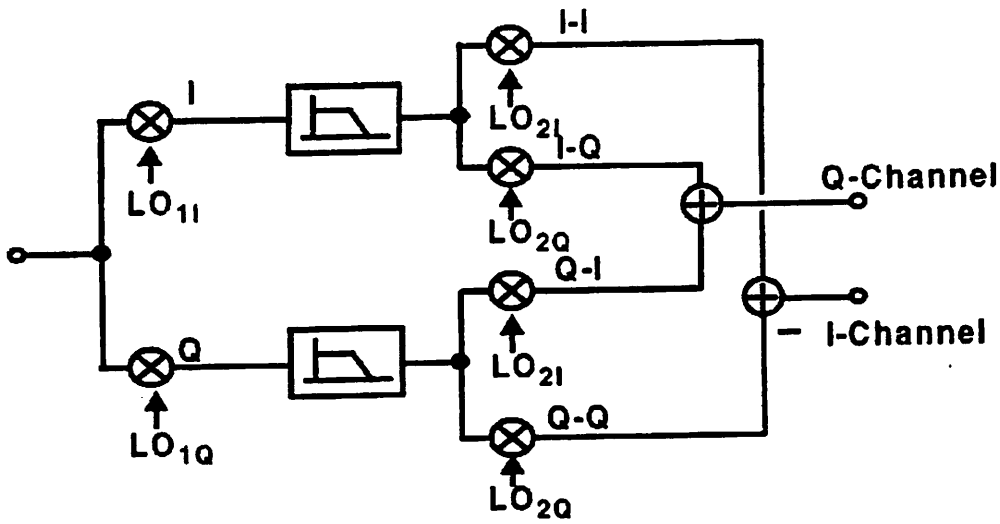


Figure 4.1 Weaver based wide-band IF receiver configuration. [2]

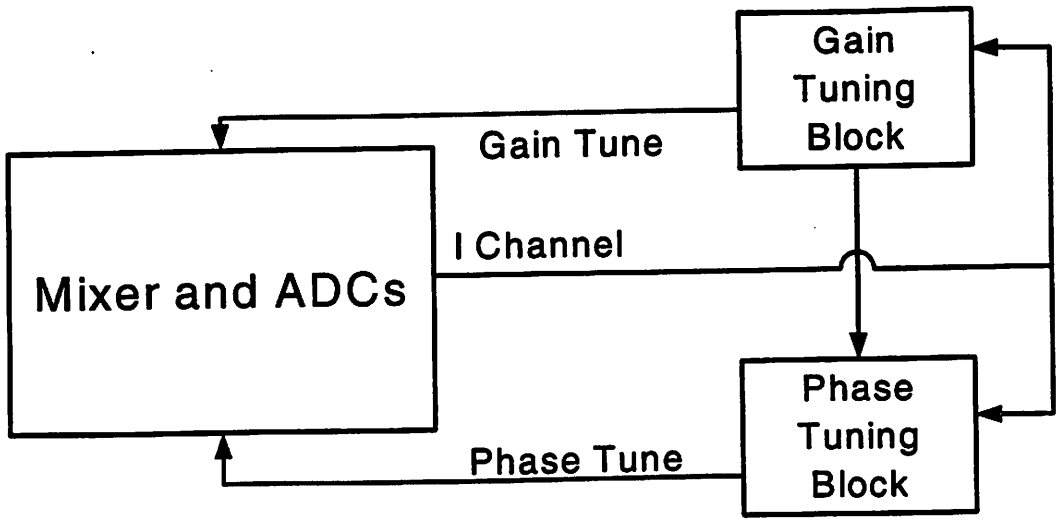


Figure 4.2 Block diagram of mixer calibration.

used to adapt the weight to minimize this error. Phase and gain tuning must occur sequentially because simultaneous tuning disturbs the convergence of each to its desired value. The gain tunes first and then signals the phase block to begin its tuning. The tuning is performed gain first for faster convergence time. The gain typically has a larger relative error to tune, and calibrates faster if it is tuned first.

4.2.1 LMS Equation Analysis and Derivation

Analysis begins with Rudell's dual-conversion Image-Reject Mixer[1,2]:

Image Rejection Ration (IRR) can be shown to be a function of gain offset (ΔA) and the mismatch in phases ($\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$) [2].

$$IRR = \frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\varphi_{\varepsilon 1}+\varphi_{\varepsilon 2})}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})}$$

Using the LMS algorithm described above we can tune the phase and gain mismatch independently. The digital output from the ADC is fed into two tuning blocks. The gain

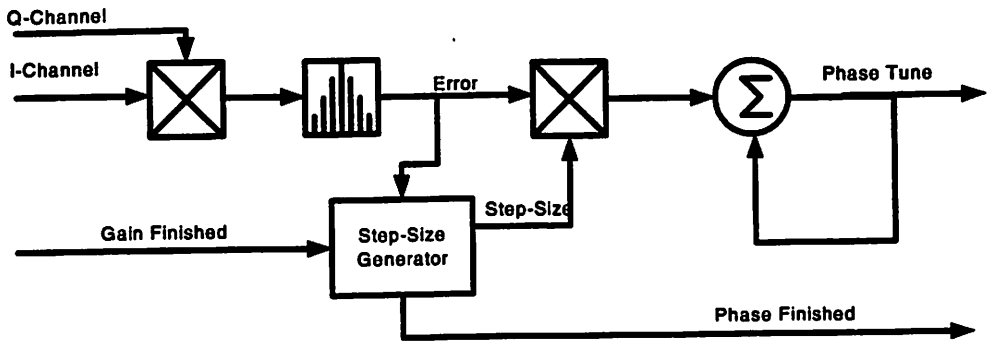


Figure 4.3 Block diagram for Phase tuning using both I and Q channels as inputs.

block will calibrate first in a feedback loop feeding back into the mixer. It will then signal the phase tuning block to begin its feedback loop to calibrate the phase.

The phase can be found by from the output I and Q channels. By multiplying the I and Q channels together, applying a low-pass-filter, and scaling with a step-size generated from the error signal, and then accumulating the result we can modify the phase towards the optimal value. Derivation of the phase and gain tuning is detailed in the Appendix. The following block diagram shows the tuning setup for the phase using both the I and Q channels.

Although using the I and Q channels for tuning works well, the output of the Q channel does not contain the desired signal, and may not be available in many cases. A

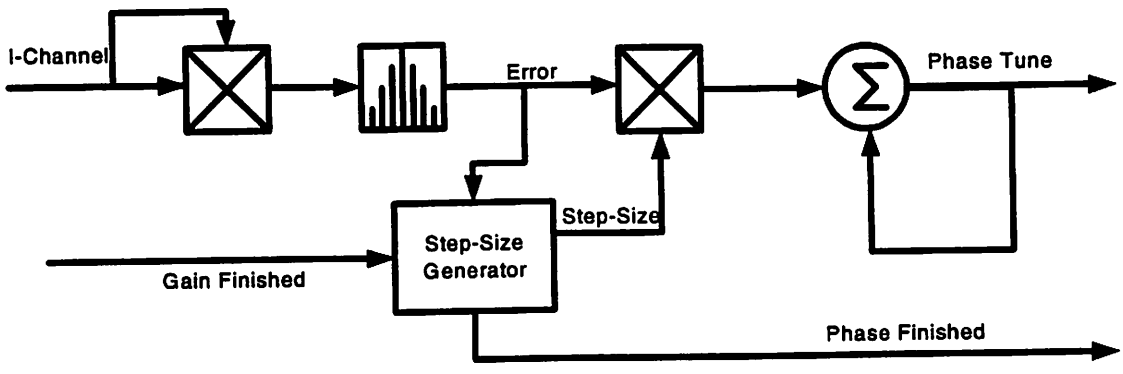


Figure 4.4 Block diagram of phase tuning using only I-channel input. Step-size generator and FIR filter must also change from I and Q channel inputs.

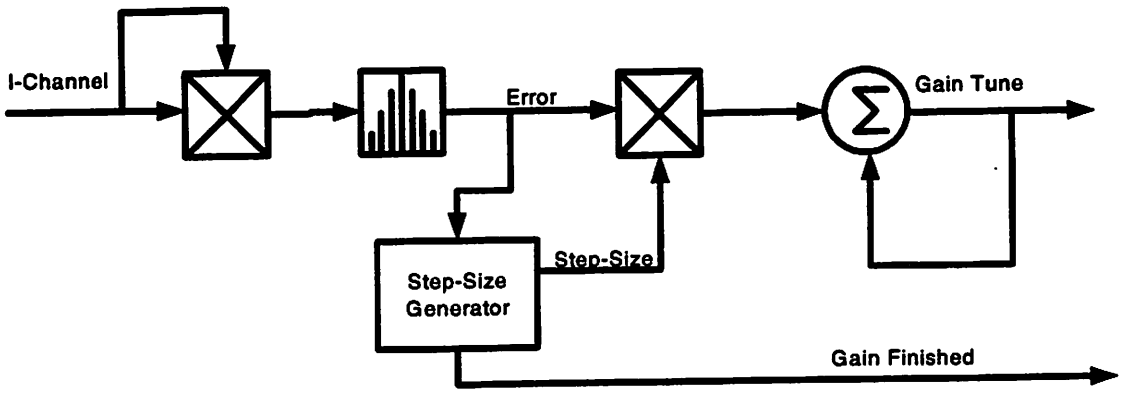


Figure 4.5 Block diagram for Gain tuning using I-channel input. Internals of blocks differ from phase tuning shown above.

more desirable method would use only the I channel for phase tuning. This can be accomplished by using the square of the I channel for a tuning input. By modifying the low-pass-filter and the step generator this method will also converge to the desired tuning value for the phase. The modified block diagram is shown in the following, Figure 4.5.

Gain tuning can similarly be accomplished with the LMS algorithm using the I channel output. The gain tunes first, and then raises the gain finished line to signal the phase tuning block to begin. The phase tuning then begins and used the gain tunned output of the I channel to optimize the phase. When the phase tuning has completed it raises the phase finished line, and both gain finished and phase finished are reset. The gain tuning is illustrated in the following block diagram.

Simulation shows that the gain and phase converge to optimal values and the tuning increases the image-rejection ratio from 35dB to approximately 75dB. The gain and phase tune to optimal values over a range of initial mismatches. These results will be described in the following chapter along with a comparison to the results presented for other proposed solutions.

Chapter 5

Results

5.1 Algorithm Simulation

The LMS tuning algorithm was tested with time domain simulations with MATLAB/Simulink to determine its ability to converge to the desired values for gain and phase. The tuning blocks were tested with a baseband equivalent model of the mixer, filters and analog-to-digital converters. This accurate representation of the high

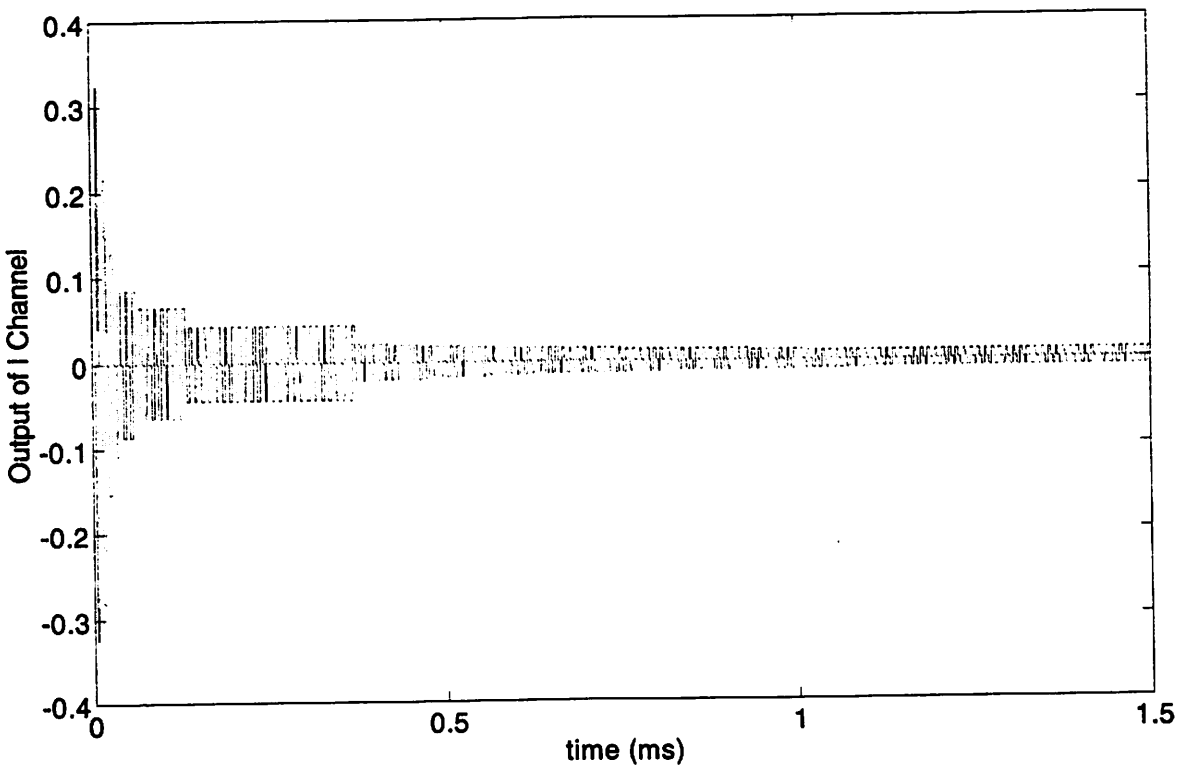


Figure 5.1 Image Tone output converges down towards zero as gain and phase tuning is performed.

frequency components allowed the simulation to be performed easily.

As described in chapter 4, the tuning algorithm attempts to minimize the error term by independently adjusting first the gain, and then the phase. Using the I channel output of the ADC as the only input to the tuning DSP allows for calibration with minimal hardware. From Simulink the LMS Tuning algorithm is able to converge to optimum phase and gain values within 1.2ms. The convergence of the tuning values increases the IRR from around 35dB to approximately 75dB. This custom DSP block achieves this tuning using minimal power and area. The area of the tuning block is approximately 77000 μm^2 in a 0.25μm CMOS, and it consumes only around 40μW during calibration. Implementation is detailed further in Chapter 7. To get an accurate power estimate the power consumed by the quadrature signal generation and phase tuning block also needs to be figured in. The additional power consumed by the tuning buffers

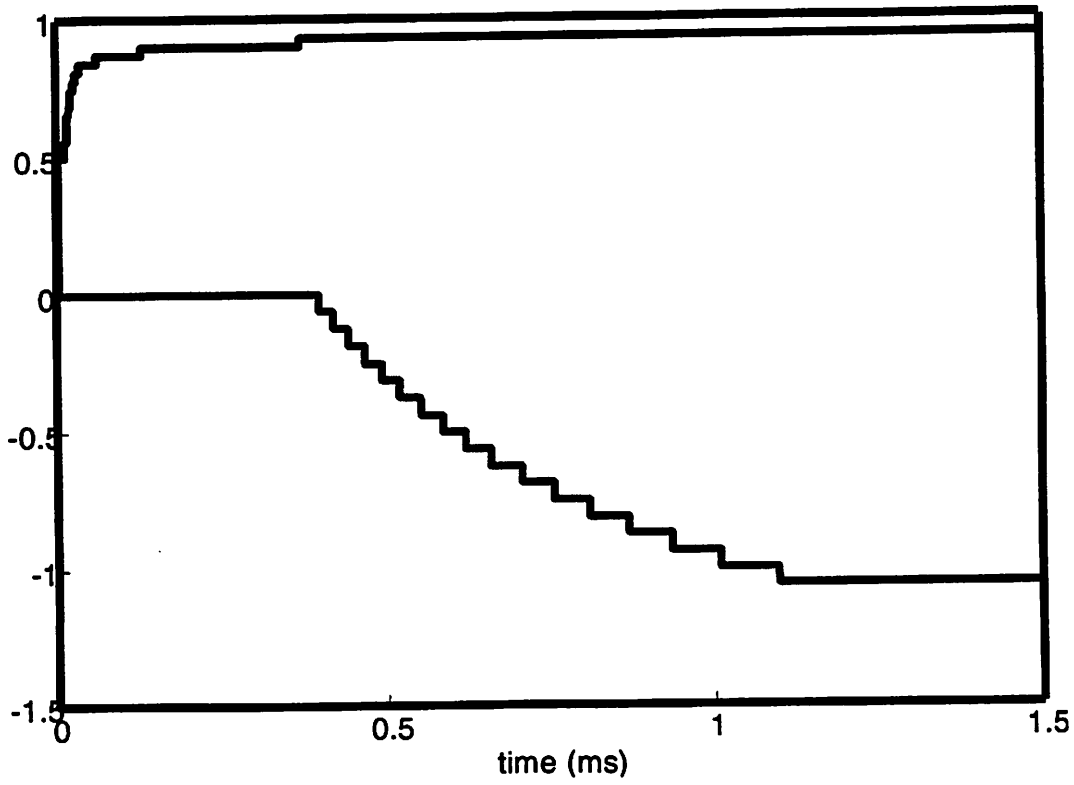


Figure 5.2 First Gain, and then Phase tune to their optimal values during calibration.

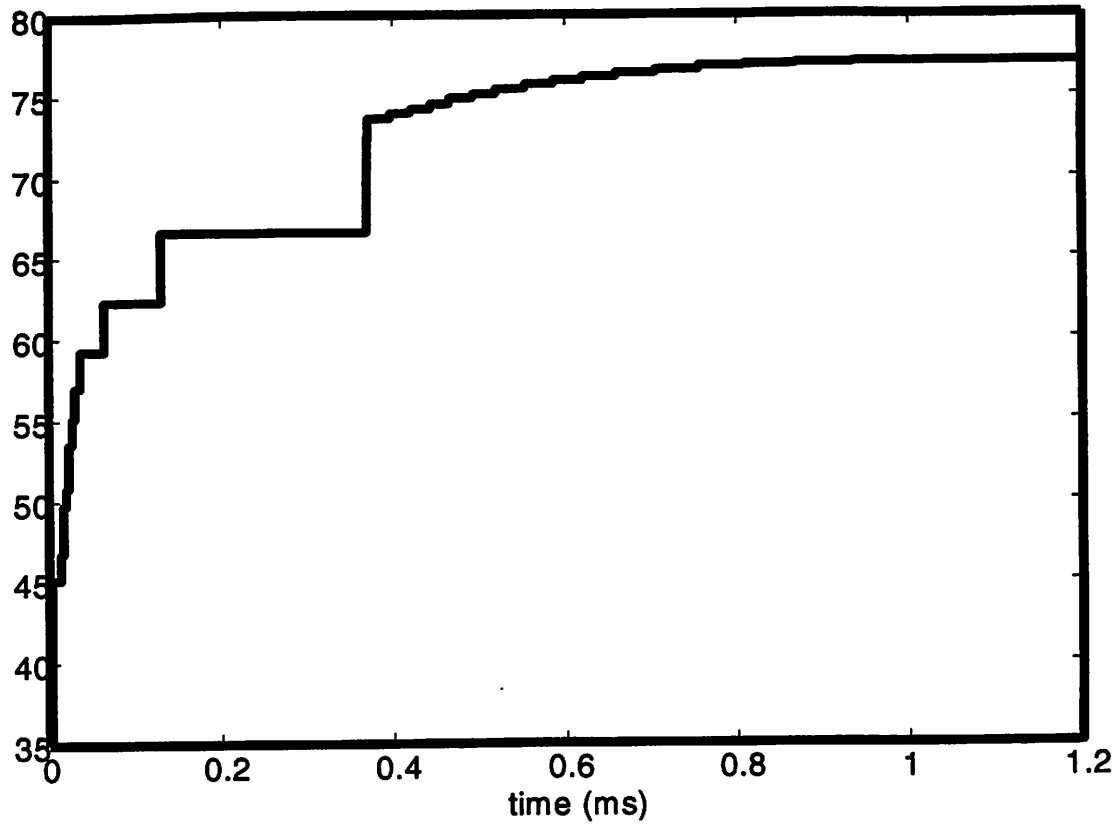


Figure 5.3 As Gain and Phase tune Image Rejection Ratio (IRR) improves from 35dB to ~75dB.

of the quadrature signals is 660 μW (0.2mA from a 3.3V supply) [2].

The calibration attempts to minimize the error term produced in the DSP block. This can be seen in Figure 5.1 the output of the I channel is driven to zero as the phase and gain converge. This is how the algorithm locates a minimum in the image-tone at the output, and thus achieves a maximum IRR. Figures 5.2 and 5.3 show the convergence of the phase and gain terms and the improvement in IRR.

Convergence was tested over a range of initial offsets ranging from ±5° phase mismatch and ±5% gain mismatch. The convergence time varied depending on the initial offset, but remained in a range between 1 ms and 1.3 ms. The small variations in convergence time over a wide range of initial offsets is due to the variable step nature of the tuning. A gear shifting technique was used to speed convergence. The step size

started large, and as the magnitude of the error signal was reduced below a threshold, the step size was reduced. This allowed the benefits of fast convergence of large step sizes and the accuracy of small step sizes to be combined. With a larger initial offset the algorithm takes larger initial steps and converges to within a small range quickly.

5.2 Performance Comparison

In order to determine the relative merit of this calibration architecture the performance of the previously published solutions detailed in chapter 3 will be explored.

5.2.1 Manual Tuning & Trimming

The results of Long and Maliepaard [7,8] demonstrate that good layout clearly improves matching and IRR. While good layout is required, the degree of matching achieved is not enough to meet the image-rejection requirements of most standards without additional external filtering or additional calibration. Calibration with hand tuning as shown by Rudell [1] and Maliepaard [7,8] and can reach the necessary IRR but has very limited applications due to the high cost, long calibration time, and one-time nature of the calibration. Hand tuning or trimming greatly increases the production costs, and cannot address problems of changing environmental and operation condition, such as changes in on-chip temperate and drift over time.

On-chip signal processing is capable of achieving similar IRR to hand tuning methods, but has many additional advantages. On-chip calibration can be mass-produced, can improve IRR to sufficient levels to replace external filtering, can calibrate the receiver quickly and can potentially re-calibrate when necessary.

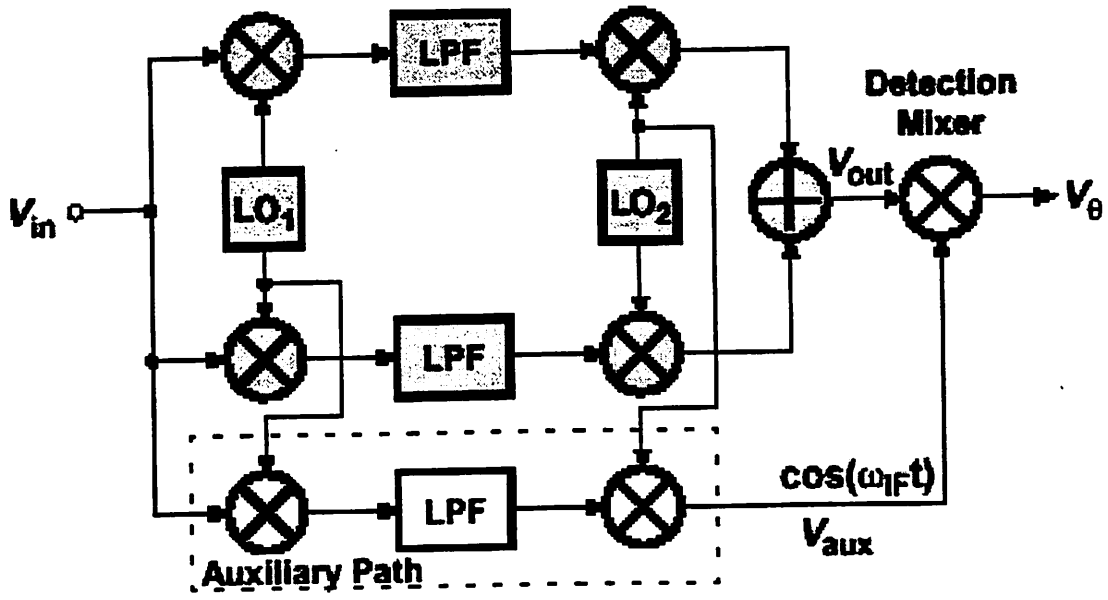


Figure 5.4 Block diagram showing Weaver mixer and auxiliary calibration path. [10]

5.2.2 Analog Solutions

The analog calibration method has problems with limited accuracy and excessive power consumption. The error signal is generated by multiplying the output of the Weaver mixer with a cosine signal from a parallel down-conversion path [10]. This error signal is then used to tune the phase mismatch by adjusting the I and Q channel phase difference. Mismatch between the auxiliary path and the signal paths can corrupt this ideal error signal and introduce error that can't be calibrated out. The calibration time for this method was not reported, so re-calibration in a timely manner may be a problem. One of the main drawbacks of this analog calibration technique is its power consumption. The power dissipation of the receiver jumps from 105mW during receive mode to 170mW during calibration [10]. This sixty percent increase in power can be attributed to the additional, LNA, mixers and filtering of the calibration path, as well as the calibration itself. The analog nature of the solution also limits the prospects of this power scaling down with digital evolution.

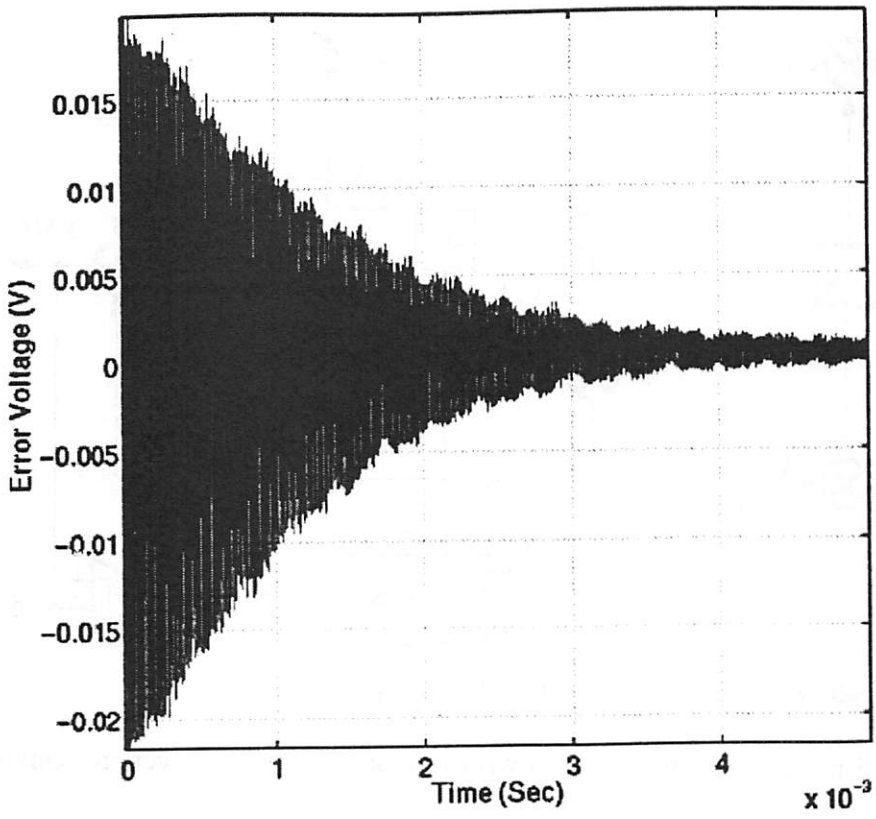


Figure 5.5 Time domain plot of the error voltage converging towards zero. [10]

5.2.3 Digital Solutions

The DSP calibration solution presented by Der and Razavi [11] at ISSCC 2001 achieved 57dB of IRR using a sign-sign LMS calibration algorithm. The system block diagram is shown in Figure 5.6. While very simple, one immediate drawback is clear from this system level picture. Two extra analog mixers are required to make the IF input values available to the calibration block. Additional problems arise from the algorithm itself. Sign-sign LMS has the disadvantages of being slow, and not having guaranteed stability. Conditions could arise where the algorithm becomes unstable and does not converge to a solution for the tuning variables. Because the sign-sign algorithm takes only one bit (sign) from the input and error terms hardware requirements are reduced to comparators and digital counters, but convergence is very slow. One case of

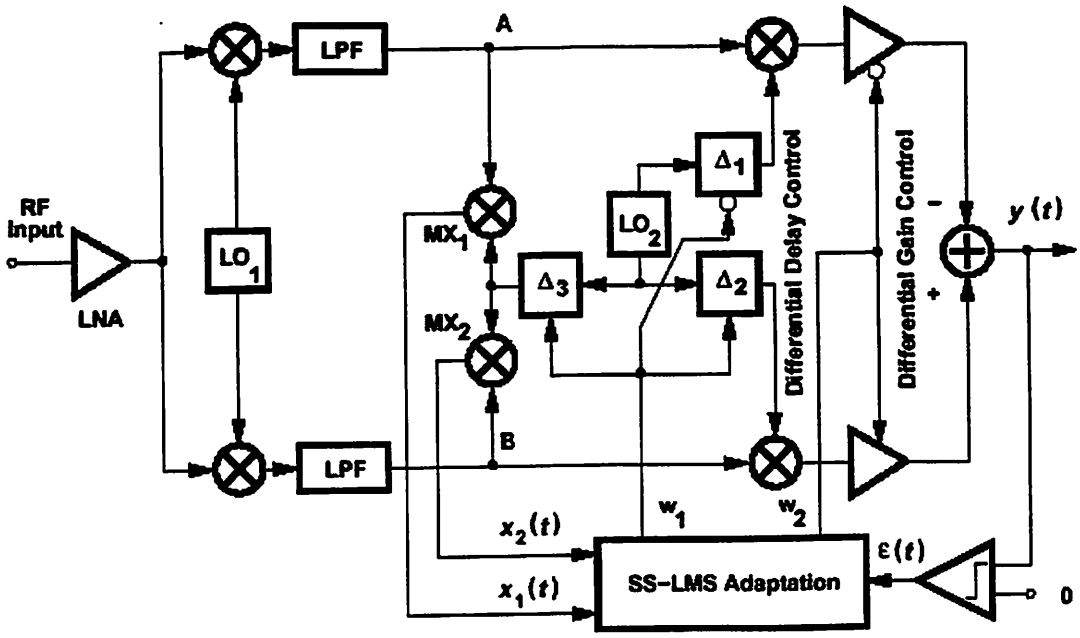


Figure 5.6 DSP calibration implementaion block diagram. [11]

approximately 5 ms convergence was shown in Figure 5.5, but no average convergence time was revealed. When used in a TDMA system this calibration procedure would be too long to allow for re-calibration during usages (between TDMA frames). The calibration also consumes an extra 5mW, increasing the circuit consumption from 50mW to 55mW during calibration. Although this calibration method improves image-rejection by tuning out path mismatches and the power is not too large, there is room for improvement in power and calibration speed.

5.2.4 Tuning based on Spectral Estimation

The spectral estimation calibration techniques presented by Desjardins in his Masters Thesis [12] was designed for the same wide-band dual-conversion receiver as this work, designed by Rudell et. al. [1,2]. Performing a Discrete-Fourier-Transform (DFT) the spectral content of the output can directly measure the image tone at the output. This measurement can then be used to vary the phase and gain to minimize the

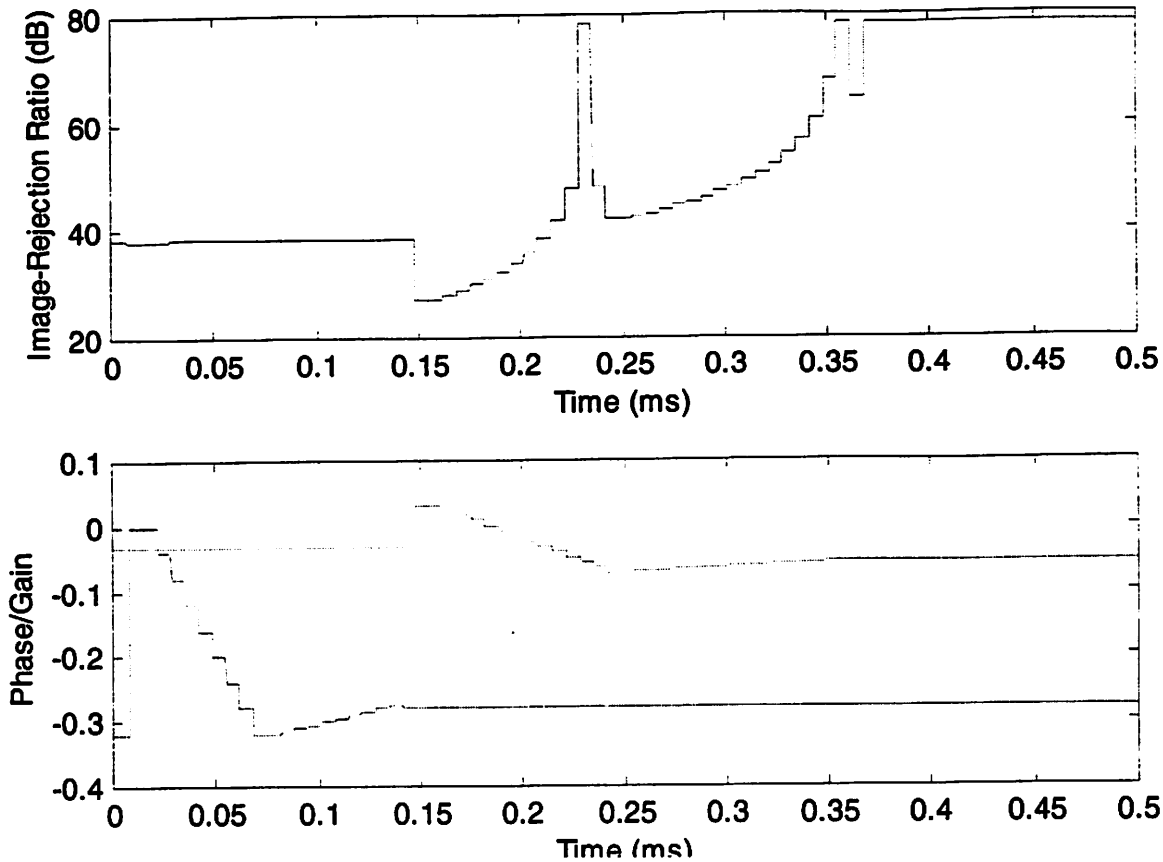


Figure 5.7 Time domain plots show tuning of gain and then phase and the improvement in IRR from 35dB to ~75dB. [12]

image-tone. With Simulink simulations this method achieved approximately 75dB of image-rejection by tuning the gain and phase in under 1ms. The custom DSP block consumes approximately 15μW during calibration. This block consumes less power than the LMS tuning approach because there is less digital computation required. The LMS tuning algorithm uses more digital multipliers in its FIR filters. The phase tuning buffer's 660 μW additional power must also be taken into account. The time-domain calibration and improvement in IRR are shown in Figure 5.7. The ability for the power to scale down with decreasing circuit dimensions is also indicated as well as the year of publication.

Comparison of Calibration Methods

Solution	IRR	Time	Power	Scale	Year
Hand Tuning [1]	45 dB	-	-	-	1997
Hand Tuning [7]	44 dB	-	-	-	1999
Hand Tuning [8]	80 dB	-	-	-	2000
Analog Calibration [10]	57 dB	??	65 mW	no	2000
Sign-Sign LMS [11]	57 dB	~5ms ?	~5 mW ?	yes	2001
Spectral Estimation [12]	~75 dB	<1ms	675 mW*	yes	2000
LMS Calibration	~75 dB	<1.2ms	700 mW*	yes	2001

* Includes 660 μW of power consumption in the quadrature signal generation and phase tuning [2].

Image-rejection can be improved with on-chip calibration to levels that eliminate the requirement for external image-filtering. Calibration solutions that are small, fast and low-power have advantages over slower and more power-consuming methods. Low power, fast calibration allows for re-calibration between active usage and a minimal impact on device battery life.

Chapter 6

Implementation

6.1 Design Flow

The LMS tuning algorithm was implemented using the Berkeley Wireless Research Center research design flow, a simplified top down flow called Simulink to

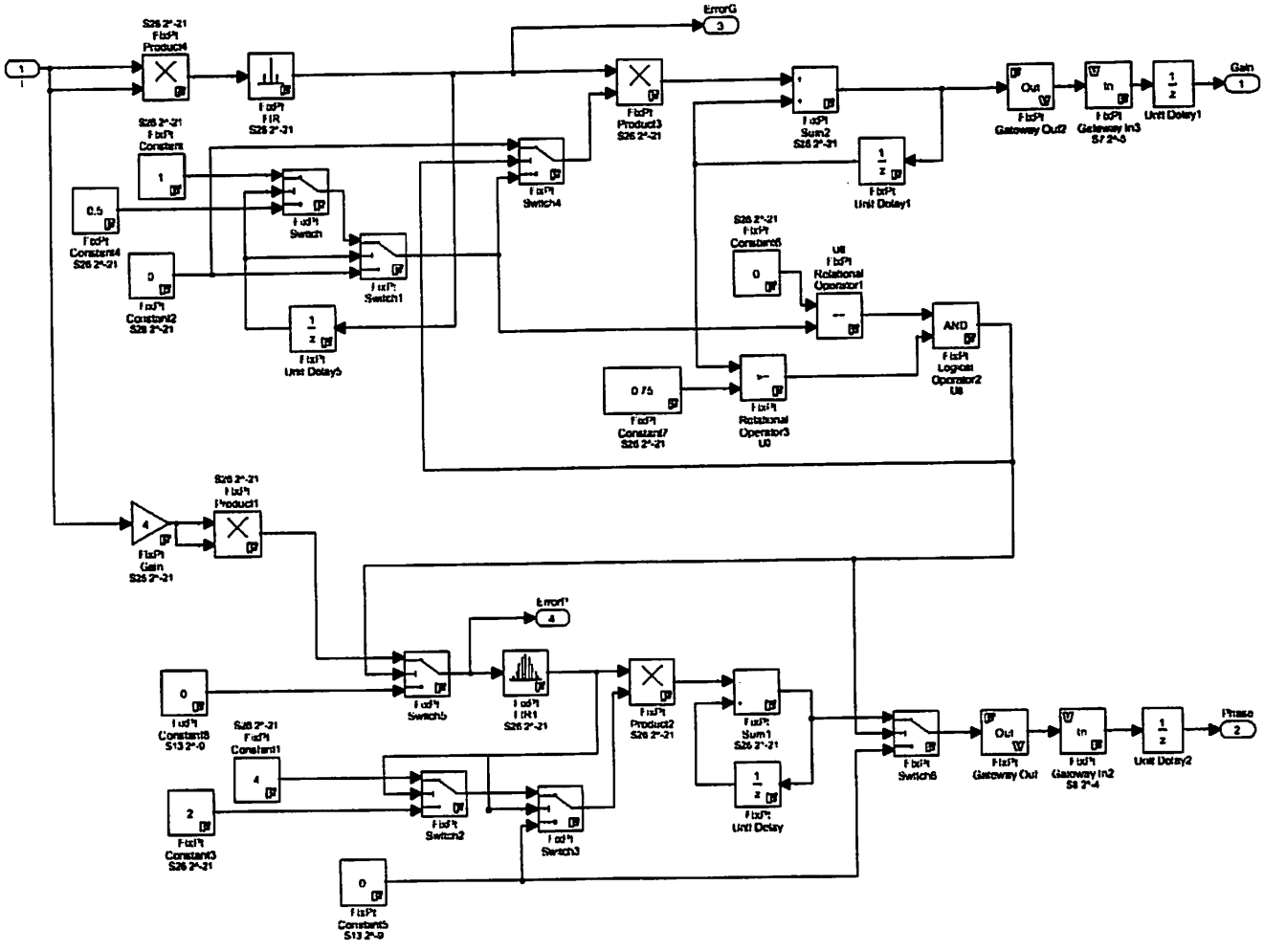


Figure 6.1 Simulink model of Gain and Phase tuning.

Silicon Hierarchical Automated Flow Tools (SSHAFT). The flow allows the creation of ICs with acceptable performance and minimal power consumption, without the need to cross abstraction boundaries. [16, 23]

Implementation of the LMS tuning algorithm began with Simulink and Module Complier. Module complier code was written to match the functionality of the block diagrams made in Simulink. The primary implementation objectives are low power and small area. It is desirable to keep the area of the calibration circuits which do the phase and gain tuning small so they will not greatly impact the overall size of the receiver. A reference size on-chip for a small component is the digital-to-analog converters.

This leads to a target size of $0.1mm^2$ ($100{,}000\mu m^2$) or less. Power of the calibration system should not affect the overall battery life or performance of the receiver. This is partially achieved by the low duty-cycle of the calibration, but is also affected by the implementation of the calibration circuits. A digital implementation will be a low-power solution and will continue to benefit from the future scaling of the digital domain.

In Module Complier different architectures for the DSP block were explored. These included using booth encoding for the multipliers, and creating the adders with ripple carry adders, carry-select adders (CSA), carry-look-ahead (CLA) and fast CLA. The best choice for area and power was found to use booth encoding and carry-select adders.

Micro-Architecture Trade-Offs

Area (μm2)	Delay (ns)	Normalized Power	Mult Type	Adder Type
77211	12.99	1.000	Booth	CSA
83916	12.99	1.086	Booth	CSA
85536	16.09	1.114	Booth	CLSA
85536	16.09	1.114	Booth	Ripple
87147	12.99	1.086	Booth	CSA
90099	11.09	1.171	Booth	CLA
96741	10.87	1.314	Booth	FastCLA
109368	15.47	1.486	No Booth	CSA
111357	18.17	1.486	No Booth	CLSA
111357	18.17	1.486	No Booth	Ripple
117504	14.78	1.600	No Booth	CLA
125622	15.48	1.771	No Booth	FastCLA

The lowest power and smallest area led to an implementation under 80,000μm^2. The Module Compiler code was then verified to match the Simulink model in the Synopysis VHDL debugger. The results are shown in the following plots.

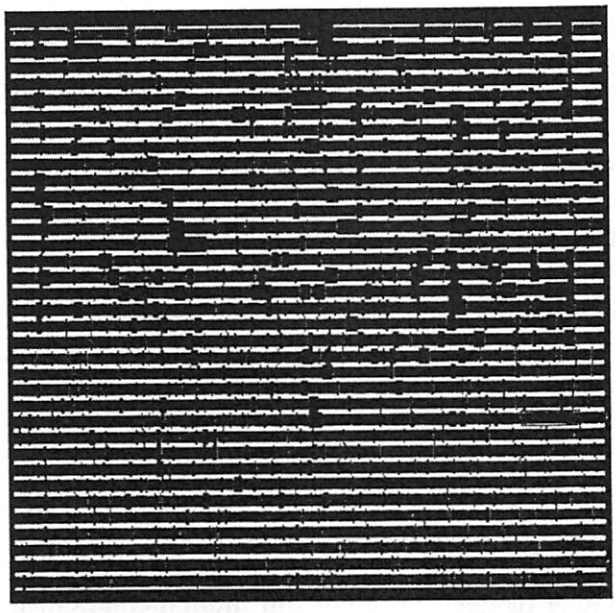


Figure 6.3 Layout of calibration circuit viewed in Cadence.

6.2 SSHAFT outputs

In order to get layout information and more realistic power numbers the design was run through the Simulink-to-Silicon Hierarchical Automated Flow Tools (SSHAFT) [16]. SSHAFT takes the Simulink block diagram and the corresponding Module Complier (MCL) code and performs the steps needed to

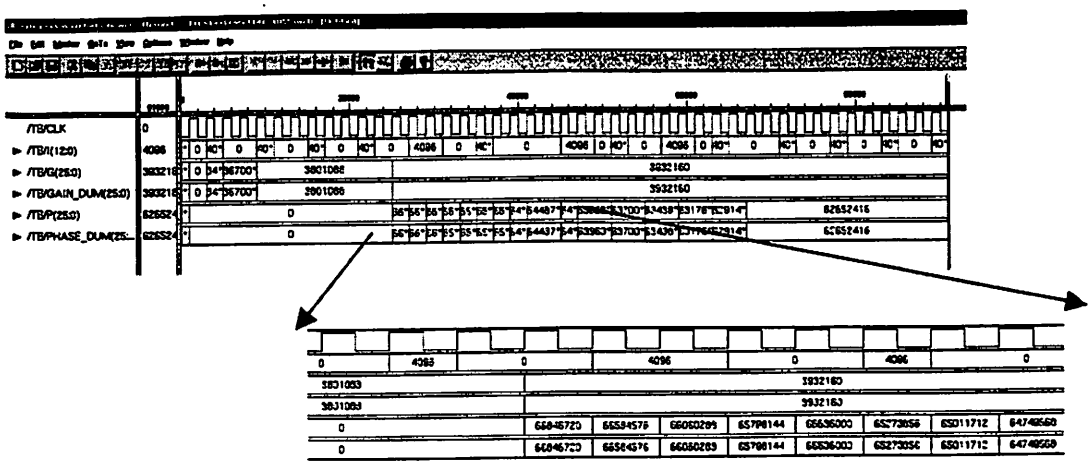


Figure 6.2 VHDL Debugger verification of Module Complier and Simulink operation.

obtain netlists, place and route and layout, as well as better power estimates.

Running this design through SSHAFT led to an Epic™ simulation power estimate of 40μW for the calibration block during calibration. To get a power estimate for the system an estimate of the power consumed by the phase tuning can be added as described in chapter 6, to give a total calibration power of approximately 700μW. This power estimate assumes an operating frequency of 300 kHz, the rate required to perform the tuning algorithm on the calibration image tone injected at the input. The calibration circuit was targeted to 0.25μm silicon, with a supply voltage of 1.2V. Under these conditions the critical path determined by the calibration feedback loop was measured to run with a maximum delay of 2.89 us, fast enough to meet the timing requirements.

6.3 Xilinx

FPGAs can be used to test algorithmic functionality on with real hardware. Although an FPGA won't reproduce the power or delay of a custom implementation, it can be used implement the algorithm and test the hardware with other pieces of the

system. Xilinx is the leading manufacturer of FPGAs and has a large product line with varying gate counts and functionality. The Virtex familyis a high performance, high density FPGA [21]. This algorithm could be tested on a wide variety of FPGAs, but a Virtex chip from Xilinx was available for use. Module Complier can write out VHDL code as one of its outputs. This code was used with the Xilinx Foundation tools to produce an implementation for a XCV-600E Xilinx FPGA. This FPGA is in the Virtex, 1.8V family. The Virtex Power Estimator [20,21] from Xilinx estimates a power consumption of 81mW to implement this calibration block. This includes the core power and the I/O power to drive signals off chip. The FPGA implementation meets the timing requirements. This algorithm could be implemented in a variety of programmable devices; this Virtex FPGA had a utilization of only 20%.

Chapter 7

Conclusion

7.1 Conclusion

This work designed and analyzed a calibration algorithm for an image-rejection mixer. Previously published solutions that used hand calibration and digital-signal-processing solutions were analyzed and their performance was compared to the least-mean-squared (LMS) tuning algorithm developed.

Background for the image-reject receiver and mixers was presented and motivation was developed for calibration to make-up for on-chip path mismatches. By calibrating the gain between the signal paths and the phase between the local oscillators the image-rejection can be improved enough to meet the standards without additional external components. This image-rejection performance takes an important step towards a comply integrated receiver.

The convergence time of the tuning algorithm is also desired to be as low as possible so calibration can be interleaved between TDMA frames during data transmission.

The DSP tuning algorithm developed uses less than 0.08mm2 of on-chip area, slightly smaller than the additional DACs that perform the tuning, and consumes around 40uW during calibration. Because of the low-power and the very low duty cycle the

calibration process will have virtually no effect on the battery life or overall energy consumption of the receiver.

7.2 Future Work

Recalibration will often be necessary due to changing environment, external conditions as well as heating of the chip, during data transmission. While interleaving calibration between frames works well for recalibrating TDMA systems, there is no such time window in CDMA systems. New calibration methods that could operate during data transmission will be necessary for recalibration of CDMA receivers. If such a calibration technique could be developed it would be essentially independent of the wireless standard in which the receiver was operating. This would require a decision driven calibration, with decisions being made during transmission and reception. Such a calibration method would need to operate without corrupting the signals being received, injecting an image tone for calibration would make this difficult.

Additional work will also need to be done to build a full receiver with image-rejection calibration built in to test these methods in hardware. Further use of digital signal processing techniques to move the calibration from the analog to the digital domains has the potential to provide for high accuracy, low power solutions that will enable greater receiver integration.

Chapter 8

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Appendix 1

Derivation of LMS Algorithm

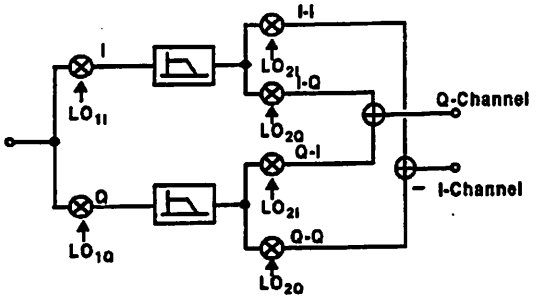

Figure 5. Weaver-based Wide-band IF mixer configuration [Courtesy J. Rudell]

Figure A.1 Weaver based wide-band IF receiver configuration. [2]

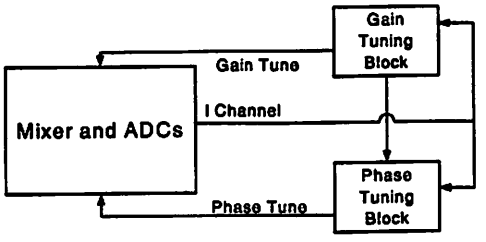

Figure A.2 Block Diagram of Mixer and Tuning interface.

Image Rejection Ration (IRR) is a function of gain offset (ΔA) and the mismatch in phases ($\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$).

$$IRR = \frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\varphi_{\varepsilon 1} + \varphi_{\varepsilon 2})}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\varphi_{\varepsilon 1} - \varphi_{\varepsilon 2})}$$

Using the LMS algorithm described here we can tune the phase and gain mismatch independently. The goal is to develop block that will take the digital outputs from the ADCs and produce gain and phase tuning signals.

Analysis to Tune the Phase Mismatch, First Assume perfect gain matching.

Input Signal contains only the image frequency

$RF_{input}(t) = sin(\omega_{image} t)$

The oscillators are defined as follows,
all of the phase error is lumped into the quadrature signals.

Local Oscillator 1	Local Oscillator 2
$LO_{1I} = cos(\omega_{LO1}t)$	$LO_{2I} = cos(\omega_{LO2}t)$
$LO_{1Q} = sin(\omega_{LO1}t + \varphi_{\varepsilon 1})$	$LO_{2Q} = sin(\omega_{LO2}t + \varphi_{\varepsilon 2})$

First we will look at the In - phase (I) Path :
After the first mixing stage

$$I(t) = \frac{1}{2}\left[sin\left(\left(\omega_{image} + \omega_{LO1}\right)t\right) + sin\left(\left(\omega_{image} - \omega_{LO1}\right)t\right)\right]$$

A Low Pass Filter is applied and upconverted term is removed
define $\omega_{IF1} = \omega_{LO1} - \omega_{image}$

$$I(t) = -\frac{1}{2}sin(\omega_{IF1}t)$$

This signal is then passed to two mixers to be multiplied
by the second local oscillator (both phases, I and Q)

$$I - I(t) = -\frac{1}{4}\left[sin\left(\left(\omega_{IF1} - \omega_{LO2}\right)t\right) + sin\left(\left(\omega_{IF1} + \omega_{LO2}\right)t\right)\right]$$

$$I - Q(t) = -\frac{1}{4}\left[cos\left(\left(\omega_{IF1} - \omega_{LO2}\right)t - \varphi_{\varepsilon 2}\right) + cos\left(\left(\omega_{IF1} + \omega_{LO2}\right)t + \varphi_{\varepsilon 2}\right)\right]$$

define $\omega_{IF2} = \omega_{IF1} - \omega_{LO2}$ and LPF to again remove the sum terms

$$II(t) = -\frac{1}{4}sin(\omega_{IF2}t)$$
$$IQ(t) = -\frac{1}{4}cos(\omega_{IF2}t - \varphi_{\varepsilon 2})$$

Similarly for the Quadrature Path :
After the first mixing stage

$$Q(t) = \frac{1}{2}\left[cos\left(\left(\omega_{image} + \omega_{LO1}\right)t + \varphi_{\varepsilon 1}\right) + cos\left(\left(\omega_{image} - \omega_{LO1}\right)t + \varphi_{\varepsilon 1}\right)\right]$$

A Low Pass Filter is applied and upconverted term is removed
define $\omega_{IF1} = \omega_{LO1} - \omega_{image}$

$$Q(t) = \frac{1}{2}cos(\omega_{IF1}t + \varphi_{\varepsilon 1})$$

This signal is then passed to two mixers to be multiplied
by the second local oscillator (both phases, I and Q)

$$Q-Q(t)=-\frac{1}{4}[sin((\omega_{IF1}-\omega_{LO2})t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})+sin((\omega_{IF1}+\omega_{LO2})t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})]$$

$$Q-I(t)=\frac{1}{4}[cos((\omega_{IF1}-\omega_{LO2})t+\varphi_{\varepsilon 1})+cos((\omega_{IF1}+\omega_{LO2})t+\varphi_{\varepsilon 1})]$$

define $\omega_{IF2}=\omega_{IF1}-\omega_{LO2}$ and LPF to again remove the sum terms

$$QQ(t)=-\frac{1}{4}sin(\omega_{IF2}t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})$$
$$QI(t)=\frac{1}{4}cos(\omega_{IF2}t+\varphi_{\varepsilon 1})$$

Combine to get the I - channel and Q - channel outputs

$$I_{output}=|II(t)-QQ(t)|=\left|-\frac{1}{4}sin(\omega_{IF2}t)-\left(-\frac{1}{4}sin(\omega_{IF2}t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})\right)\right|$$
$$=\left|\frac{1}{4}sin(\omega_{IF2}t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})-\frac{1}{4}sin(\omega_{IF2}t)\right|$$

$$Q_{output}=|IQ(t)+QI(t)|=\left|-\frac{1}{4}cos(\omega_{IF2}t-\varphi_{\varepsilon 2})+\frac{1}{4}cos(\omega_{IF2}t+\varphi_{\varepsilon 1})\right|$$
$$=\left|\frac{1}{4}cos(\omega_{IF2}t+\varphi_{\varepsilon 1})-\frac{1}{4}cos(\omega_{IF2}t-\varphi_{\varepsilon 2})\right|$$

To isolate the phase error terms multiply I_{output} and Q_{output}, then apply a LPF.

$$I_{output}*Q_{output} = \frac{1}{4}(sin(\omega_{IF2}t+\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})-sin(\omega_{IF2}t))\cdot\frac{1}{4}(cos(\omega_{IF2}t+\varphi_{\varepsilon 1})-cos(\omega_{IF2}t-\varphi_{\varepsilon 2}))$$

$$=\frac{1}{16}[sin(\omega_{IF2}t)cos(\omega_{IF2}t)cos(\varphi_{\varepsilon 2})+sin^2(\omega_{IF2}t)sin(\varphi_{\varepsilon 2})+sin(\omega_{if2}t)cos(\omega_{if2}t)cos(\varphi_{\varepsilon 1})$$
$$-sin^2(\omega_{if2}t)sin(\varphi_{\varepsilon 1})-sin(\omega_{if2}t)cos(\varphi_{\varepsilon 1})cos^2(\varphi_{\varepsilon 2})cos(\omega_{if2}t)-sin^2(\omega_{if2}t)cos(\varphi_{\varepsilon 1})cos(\varphi_{\varepsilon 2})sin(\varphi_{\varepsilon 2})$$
$$-sin(\omega_{if2}t)cos^2(\varphi_{\varepsilon 1})cos(\varphi_{\varepsilon 2})cos(\omega_{if2}t)+sin^2(\omega_{if2}t)cos(\varphi_{\varepsilon 1})cos(\varphi_{\varepsilon 2})sin(\varphi_{\varepsilon 1})$$
$$-2sin(\omega_{if2}t)sin(\varphi_{\varepsilon 1})sin(\varphi_{\varepsilon 2})cos(\omega_{if2}t)cos(\varphi_{\varepsilon 2})-sin^2(\omega_{if2}t)sin(\varphi_{\varepsilon 1})sin^2(\varphi_{\varepsilon 2})$$
$$-2sin(\omega_{if2}t)sin(\varphi_{\varepsilon 1})sin(\varphi_{\varepsilon 2})cos(\omega_{if2}t)cos(\varphi_{\varepsilon 1})+sin^2(\omega_{if2}t)sin^2(\varphi_{\varepsilon 1})sin(\varphi_{\varepsilon 2})$$
$$-cos^2(\omega_{if2}t)sin(\varphi_{\varepsilon 1})cos^2(\varphi_{\varepsilon 2})-cos^2(\omega_{if2}t)sin(\varphi_{\varepsilon 1})cos(\varphi_{\varepsilon 2})cos(\varphi_{\varepsilon 1})$$
$$+cos(\omega_{if2}t)sin^2(\varphi_{\varepsilon 1})cos(\varphi_{\varepsilon 2})sin(\omega_{if2}t)+cos^2(\omega_{if2}t)cos(\varphi_{\varepsilon 1})sin(\varphi_{\varepsilon 2})cos(\varphi_{\varepsilon 2})$$
$$+cos(\omega_{if2}t)cos(\varphi_{\varepsilon 1})sin^2(\varphi_{\varepsilon 2})sin(\omega_{if2}t)+cos^2(\omega_{if2}t)cos^2(\varphi_{\varepsilon 1})sin(\varphi_{\varepsilon 2})]$$

use symbolic toolbox in MATLAB to simplify

$I_{output}*Q_{output}=$

$$\frac{1}{32}[2sin(\varphi_{\varepsilon 2})-2sin(\varphi_{\varepsilon 1})+sin(2\omega_{IF2}t-\varphi_{\varepsilon 2})+sin(2\omega_{IF2}t+\varphi_{\varepsilon 1})-sin(2\omega_{IF2}t+\varphi_{\varepsilon 1}-2\varphi_{\varepsilon 2})-sin(2\omega_{IF2}t+2\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})]$$

$I_{output}*Q_{output}$ contains a dc term and several terms at $2\omega_{IF2}$

The DC term can be obtained with a simple LPF

$$I_{output}*Q_{output}(DC)=\frac{1}{16}[sin(\varphi_{\varepsilon 2})-sin(\varphi_{\varepsilon 1})]=\varepsilon_n$$

This error term can be used to tune the phase in the second local oscillator

to drive $\phi_{\varepsilon 2}=\phi_{\varepsilon 1}$

To Tune Phase

$$\phi_{\varepsilon 2_{n+1}}=\phi_{\varepsilon 2_n}-\mu\varepsilon_n$$

$$\varepsilon_n=\frac{1}{16}[\sin(\phi_{\varepsilon 2})-\sin(\phi_{\varepsilon 1})]$$

This error term was derived for perfect gain matching, however

If $\Delta A \neq 0$, it can be included as a constant in the phase error term.

$$\varepsilon_n=\frac{1}{16}(2+3\Delta\Delta+\Delta A^2)[sin(\varphi_{\varepsilon 2})-sin(\varphi_{\varepsilon 1})]$$

$$\varepsilon_n=K[sin(\varphi_{\varepsilon 2})-sin(\varphi_{\varepsilon 1})]$$

where the constant $K = \frac{1}{16}\left(2 + 3\Delta\Delta + \Delta A^2\right)$ K remains constant

as long as ΔA is constant. for $\varphi_{\varepsilon 2}$ and $\varphi_{\varepsilon 2} \approx$ small

we can make the approximations $sin(\varphi_{\varepsilon 2}) \approx \varphi_{\varepsilon 2}$ $sin(\varphi_{\varepsilon 1}) \approx \varphi_{\varepsilon 1}$

$\varepsilon_n = K(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$

substituting and absorbing the K into μ

$\varphi_{\varepsilon 2_{n+1}} = \varphi_{\varepsilon 2_n} - \mu(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$

$\varphi_{\varepsilon 2_{n+1}} = \varphi_{\varepsilon 2_n}(1-\mu) + \mu\varphi_{\varepsilon 1}$

take the expected value of both sides

$\overline{\varphi_{\varepsilon 2_{n+1}}} = \overline{\varphi_{\varepsilon 2_n}}(1-\mu) + \mu\varphi_{\varepsilon 1}$

if the mean of the variable phase, $\varphi_{\varepsilon 2}$ converges then

$\lim_{n\to\infty} \overline{\varphi_{\varepsilon 2_{n+1}}} = \lim_{n\to\infty} \overline{\varphi_{\varepsilon 2_n}}$

$\overline{\varphi_{\varepsilon 2_{n_\infty}}} = \overline{\varphi_{\varepsilon 2_{n_\infty}}}(1-\mu) + \mu\varphi_{\varepsilon 1}$

$\overline{\varphi_{\varepsilon 2_{n_\infty}}} = \varphi_{\varepsilon 1}$

if $\overline{\varphi_{\varepsilon 2_{n_\infty}}} = \varphi_{\varepsilon 1}$ then the error goes to zero

$\varepsilon_n \Rightarrow 0$

This can be implemented using the following block diagram.

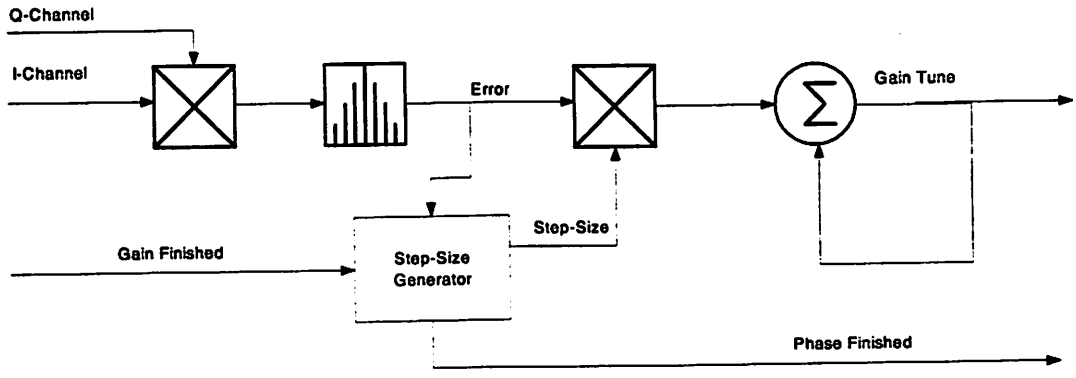

Figure A.3 Block diagram of I and Q channel input phase tuning.

An alternate approach to tuning the phase error attempts to use only the I-channel output.

Starting with the I - channel output we can generate an error value by squaring it, applying a LPF, and subtracting out a constant value.

$$I_{output} = |II(t) - QQ(t)| = \left| \frac{1}{4}(1+\Delta A)\sin(\omega_{IF2}t + \varphi_{\varepsilon 1} - \varphi_{\varepsilon 2}) - \frac{1}{4}\sin(\omega_{IF2}t) \right|$$

$$(I_{output})^2 = \left(\frac{1}{4}(1+\Delta A)\sin(\omega_{IF2}t + \varphi_{\varepsilon 1} - \varphi_{\varepsilon 2}) - \frac{1}{4}\sin(\omega_{IF2}t) \right)^2$$

$$= \frac{1}{2} + \frac{1}{2}(1+\Delta A)^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1}) - \frac{1}{2}(1+\Delta A)^2\cos(2\omega_{IF2}t + 2\varphi_{\varepsilon 1} - 2\varphi_{\varepsilon 2})$$

$$+ (1+\Delta A)\cos(2\omega_{IF2}t + \varphi_{\varepsilon 1} - \varphi_{\varepsilon 2}) - \frac{1}{2}\cos(2\omega_{IF2}t)$$

We can apply a LPF to remove to terms that are a function of $\omega_{IF2}t$

$$(I_{output})^2_{LPF} = \frac{1}{2} + \frac{1}{2}(1+\Delta A)^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$$

$$= \frac{1}{2} + \frac{1}{2}(1 + 2\Delta\Delta + \Delta A^2) - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$$

$$= \frac{1}{2} + \frac{1}{2} + \Delta A + \frac{1}{2}\Delta A^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$$

$$= 1 + \Delta A + \frac{1}{2}\Delta A^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1})$$

We can now attempt to remove the dc component that depends only on the gain mismatch and initial phase mismatch.

$$(I_{output})^2_{LPF} = 1 + \Delta A + \frac{1}{2}\Delta A^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2o} - \varphi_{\varepsilon 1o}) = constant\ K\ 1$$

$$(I_{output})^2_{LPF} - K1 =$$

$$\left[1 + \Delta A + \frac{1}{2}\Delta A^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1}) \right] - \left[1 + \Delta A + \frac{1}{2}\Delta A^2 - (1+\Delta A)\cos(\varphi_{\varepsilon 2o} - \varphi_{\varepsilon 1o}) \right]$$

$$= K2 \cdot [\cos(\varphi_{\varepsilon 2} - \varphi_{\varepsilon 1}) - \cos(\varphi_{\varepsilon 2o} - \varphi_{\varepsilon 1o})]$$

where K2 is a constant $(1+\Delta A)$

This can be implemented by modifying the block diagram above slightly to square the I channel rather than using the product of the Q and I channels.

The gain loop uses only the I-channel output. A simplified diagram of the I-channel is shown below:

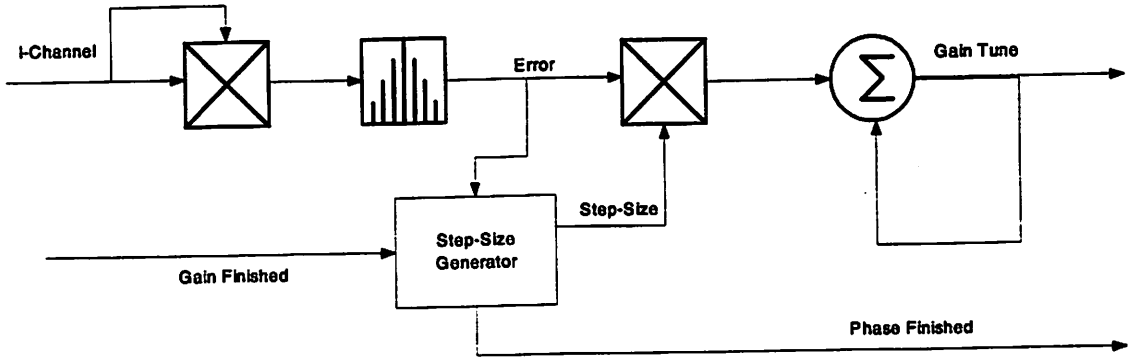

Figure A.4 Alternate Phase tuning block diagram, using only I-Channel input.

To Tune Gain

We can find similar output equations in the case of gain mismatch as when we had phase mismatch

Assuming perfect phase matching and a mismatch in gain of ΔA :

$$II(t) = -\frac{1}{4}\sin(\omega_{IF2}t)$$
$$IQ(t) = -\frac{1}{4}(1+\Delta A)\cos(\omega_{IF2}t)$$

$$QQ(t) = -\frac{1}{4}(1+\Delta A)\sin(\omega_{IF2}t)$$
$$QI(t) = \frac{1}{4}(1+\Delta A)\cos(\omega_{IF2}t)$$

$$I_{output} = |II(t) - QQ(t)| = \left|\frac{1}{4}(1+\Delta A)\sin(\omega_{IF2}t) - \frac{1}{4}\sin(\omega_{IF2}t)\right|$$

$$I_{output} = \frac{1}{4}\Delta A\sin(\omega_{IF2}t)$$

$$G_{n+1} = G_n - \mu X_n \varepsilon_n$$
$$\varepsilon_n = G_A G_D X_n - G_d G_m G_n G_A X_n$$
$$G_{n+1} = G_n - \mu X_n (G_A G_D X_n - G_d G_m G_n G_A X_n)$$
$$G_{n+1} = G_n - \mu X_n^2 G_D G_A + \mu X_n^2 G_D G_A G_m G_n$$

Taking the expected value of both sides gives

$$X_n^2 = \sin^2(\omega_{image}t) \quad \Rightarrow \quad E[X_n^2] = \frac{1}{2}$$

$$\overline{G_{n+1}} = \overline{G_n} - \frac{1}{2}\mu G_D G_A + \frac{1}{2}\mu G_D G_A G_m \overline{G_n}$$

$$\overline{G_{n+1}} = \overline{G_n}\left(1 + \frac{1}{2}\mu G_D G_A G_m\right) - \frac{1}{2}\mu G_D G_A$$

if the mean of the variable gain $\overline{G_n}$ converges then

$$\lim_{n\to\infty} \overline{G_{n+1}} = \lim_{n\to\infty} \overline{G_n}$$

$$\overline{G_{n\infty}} = \overline{G_{n\infty}}\left(1+\frac{1}{2}\mu G_D G_A G_m\right)-\frac{1}{2}\mu G_D G_A$$

$$\overline{G_{n\infty}} = \frac{1}{G_m}$$

if $\overline{G_{n\infty}} = \frac{1}{G_m}$ then the error goes to zero

$$\varepsilon_n = G_A G_D X_n - G_d G_m G_A X_n \frac{1}{G_m}$$

$$\varepsilon_n \Rightarrow 0$$

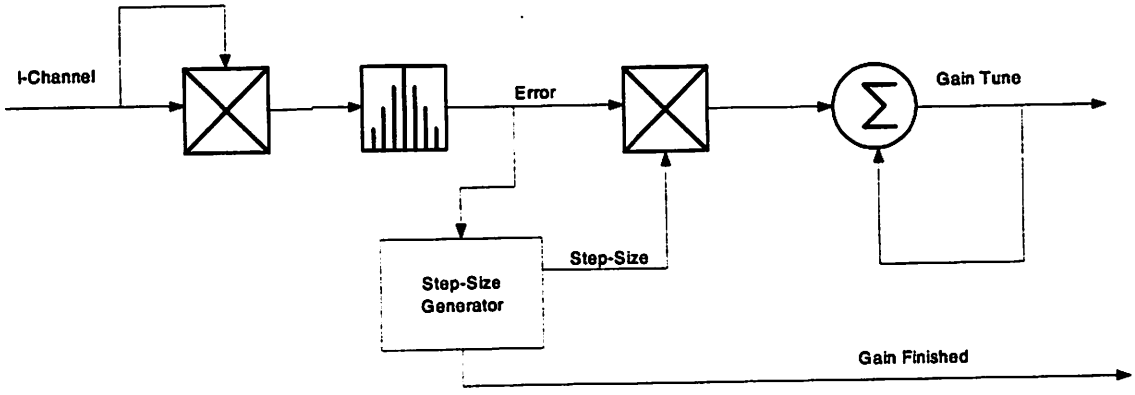

Figure A.5 Block Diagram of Gain tuning.

The gain tuning block can be implemented with a block diagram similar to the phase tuning one.

As described in Chapter 6, simulation shows that the gain and phase converge to optimal values and the tuning increases the image-rejection ratio from 35dB to approximately 75dB.