ULTRA-LOW POWER WIRELESS TECHNOLOGIES FOR SENSOR NETWORKS

by

Brian Patrick Otis

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
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Ultra-Low Power Wireless Technologies for Sensor Networks

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Brian Patrick Otis

B.S. (University of Washington, Seattle) 1999
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Dissertation Commitee:

Professor Jan Rabaey, Chair
Professor Roger Howe
Professor Paul Wright

Spring, 2005

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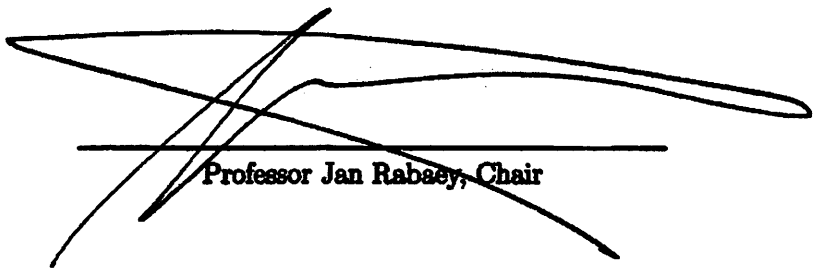

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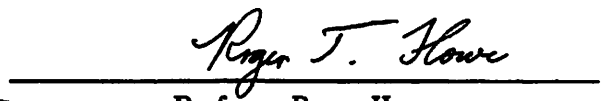

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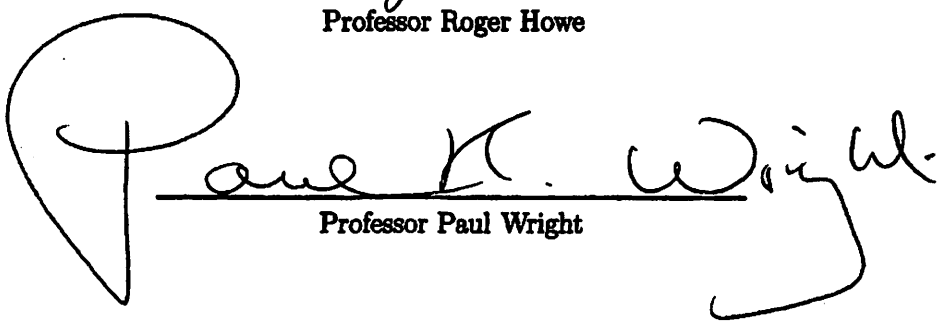

Professor Paul Wright

University of California, Berkeley

Spring, 2005

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Abstract

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The new field of wireless sensor networks presents many opportunities and just as many challenges. One particularly difficult aspect of wireless sensing is the implementation of the radio link. To enable energy scavenging, a technique that harvests ambient energy to power the sensor node indefi-

nitely, sub-mW power levels are necessary for the receiver. To allow a small node form-factor, all external surface-mount components must be eliminated. Traditional RF transceiver design techniques are not suitable for achieving complete integration since they rely on frequency synthesis, requiring a surface mount quartz crystal and a power hungry on-chip phase locked loop.

This thesis demonstrates that subthreshold RF CMOS circuit design and high quality RF MEMS passive components are useful tools for reducing the power consumption and increasing the level of integration of GHz-range transceivers. To demonstrate these concepts, two transceivers using these principles were designed, implemented, and tested. One was a multiple channel 3mW receiver. The other is a 400μW super-regenerative receiver with a 1mm^3 total implementation volume. A 20m indoor wireless link and operation with scavenged energy was demonstrated. Finally, to further address integration concerns, a CMOS/MEMS reference clock was designed to replace the quartz crystal reference and flip-chip techniques were shown to further reduce the transceiver size.

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Acknowledgements

The past six years in Berkeley has truly been a fascinating experience. To acknowledge everyone who contributed to these experiences would double the length of this thesis. Thank you all.

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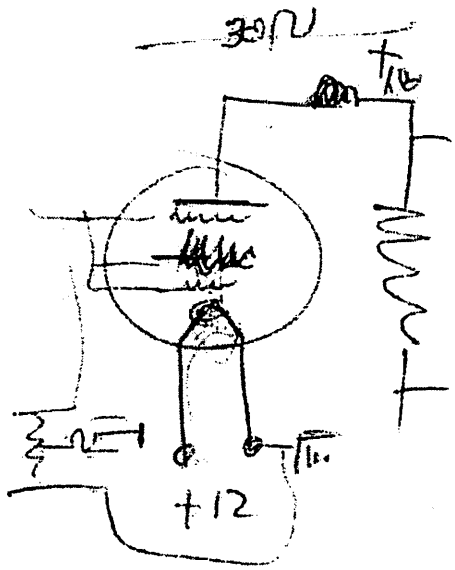
I would like to acknowledge Professor Eve Riskin from the University of Washington for her candid advice over the years. Thanks to Professors Ralph Freeman (U.C. Berkeley) and Kelly Tremblay (U. Washington) who took a chance on an Electrical Engineer wanting to learn more about the brain.

Thanks to my family for their support over the years. My Mom, Dad, and sister Sara have now spent years feigning interest while looking through a microscope at a die or a layout plot of one of my chips. I will conclude with a schematic drawn by my Grandpa Moose on a Post-It note during a brief lecture he gave me many years ago on vacuum tube amplification. Even



though I didn't fully understand the concepts at the time, it goes to show that inspiration can come from strange places...

Brian P. Otis

Berkeley, 2005

Chapter 1

Wireless Sensor Networks

The accurate quantification of environmental parameters has been an important part of human existence for centuries. In 1612, Santorio Santorio invented the graduated thermometer, and human curiosity and quest for knowledge has been growing ever since. Modern sensing parameters include humidity, seismic activity, building occupation, airflow, particulate detection, and many others. A *wireless sensor* monitors one or more environmental parameters and transmits the data to the network for automatic control or human evaluation. This process could include data compression and accumulation to reduce the amount of transmitted data. One could conceive of a huge network of these sensors that are able to communicate with each other. Decades of technological advances have made it conceivable to build and deploy dense wireless networks of autonomous nodes collecting and disseminating wide ranges of environmental data. Wireless sensor networks

have many valuable potential applications, ranging from closed-loop environmental control of office buildings and homes to wildlife monitoring. Other possible applications are robot control and guidance in automatic manufacturing environments, warehouse inventory, integrated patient monitoring, diagnostics and drug administration in hospitals, home providing security, identification and personalization, and interactive museums. Successful deployment of wireless sensor and actuator networks in sufficient numbers to provide true ambient intelligence will require the confluence of progress in several disciplines: networking, low power RF and digital IC design, MEMS techniques, energy scavenging, and packaging. Figure 1.1 shows the various specialized blocks of a sensor node.

In large-scale system designs, some of these blocks (clock generation, for example) are often considered negligible in terms of power and volume. However, in the implementation of extremely small sensor nodes, each of these components becomes crucial. The most challenging aspect of sensor node implementation is the integration of ultra-low power RF transceivers. It will be shown that the requirements of these transceivers are fundamentally different from those of existing wireless applications, such as cellular telephony, Bluetooth specification radios, and wireless local area network (WLAN) transceivers. The goal of this dissertation is to address some of the design challenges involved with integrating RF communication functionality in a self-contained sensor node.

This chapter introduces the University of California, Berkeley PicoRadio

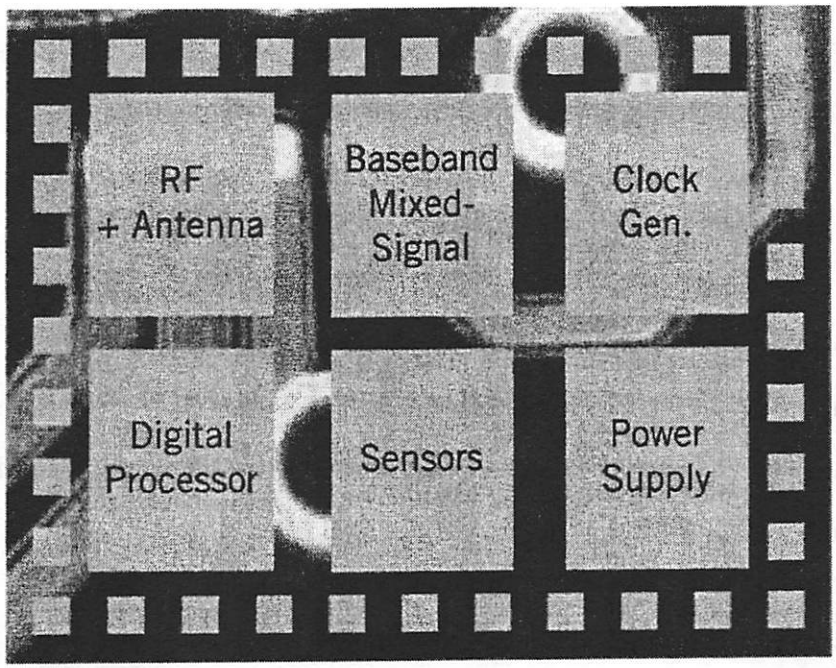


Figure 1.1: Hardware blocks for sub-mW sensor network implementations

project and describes system level requirements for ad-hoc sensor nodes. The RF transceiver challenges are discussed, including range, sensitivity, power consumption, and integration requirements.

1.1 The PicoRadio Project

The *PicoRadio* Project at the University of California, Berkeley was founded by Professor Jan Rabaey to identify and address technical barriers to the implementation and large-scale deployment of wireless ad-hoc sensor networks [3]. As will be shown in this chapter, the most challenging aspect of

the system implementation is the radio frequency communication datalink. We will begin with a description of the system requirements.

1.2 System Requirements

To make dense node deployment possible in practical scenarios, each node must be physically and economically unobtrusive. A node's "obtrusiveness" can be measured by three important metrics: energy scavenging capability, cost and size. These requirements are outlined below.

- **Energy Scavenging:** To reduce installation cost and to allow for a flexible method of deployment, most nodes must be untethered. Maintenance cost considerations render frequent replacement of the energy source of the node unrealistic. Thus, the nodes must scavenge their energy from the environment. This leads to a very aggressive node average power budget of approximately 100μW.

- **Low Cost Implementation:** Commercial viability dictates that the unit cost ($\frac{\$}{m^2}$) of the wireless sensor network mesh be very small. For network reliability and high sensing resolution, the node density ($\frac{nodes}{m^2}$) must be high. Thus, the cost of each node must be extremely low (<1$US).

- **Small Form Factor:** Embedding the components into the existing infrastructure of daily environments (walls, furniture, lighting, etc.)

requires a very small form factor of the entire sensor node. Typically, node volumes less than $1cm^3$ (much smaller than a AA battery) are necessary. A very high level of integration is mandatory if such small dimensions are to be achieved.

The ubiquitous deployment of sensor nodes is economically feasible only if the individual nodes are negligible in cost and size. Achieving such a diminutive stature requires a minimal number of components, a high level of integration, simple and cheap packaging and assembly, and avoidance of expensive components and/or technologies. In the next section, energy scavenging for wireless sensor networks will be discussed, which determines the transceiver power consumption requirements.

1.3 Energy Scavenging

The considerations discussed above dictate that each sensor node be self-sufficient from an energy perspective for the lifetime of the node. This may span up to 10 years for certain building environmental control applications. The energy storage capability of a node is limited by the storage medium (battery or capacitor) and the size constraints. While a single-time charge could work for applications with life cycles below one year, replenishment of the energy supply using energy scavenging is often a necessity. Table 1.1 illustrates the finite power density of state-of-the-art energy sources [2].

Thus, the average power dissipation of the node is severely constrained

Table 1.1: Average power density of various energy storage and scavenging devices [2]

Power Source	Power Density $\frac{\mu W}{cm^3}$	Lifetime
Lithium Battery	100	1 year
Micro Fuel Cell	110	1 year
Solar Cell	10-15000($\frac{\mu W}{cm^2}$)	∞
Vibrational Converter	375	∞
Air Flow	380	∞
Temperature Gradients	50	∞

by the energy scavenging volume of the node. These sources can be broadly grouped into two categories: *energy scavenging sources* and *energy storage sources.* From a volume of $1cm^3$, an average continuous power output of $100\mu W$ could be supplied by one or a combination of these power sources. If a one year lifetime were acceptable, either a lithium battery or fuel cell would suffice. However, micro fuel cell technology is still in the early stages of research, and is prohibitively complex and expensive. Another active area of research is in thin-film battery technology, which will yield large benefits for sensor node implementations. For desired node lifetimes greater than one year, however, $1cm^3$ does not provide ample storage for the node's 3110 $\frac{J}{year}$ energy requirements. Typical node deployment scenarios would demand a 10 year lifetime (31kJ). This is a prohibitively large amount of energy to store in a $1cm^3$ volume, necessitating the harvesting of energy from the environment.

Solar power is a proven, universal method of collecting ambient energy. For outdoor or high-light conditions, this is the obvious solution. However, in dim lighting conditions, the power output drops dramatically. In these envi-

ronments, an additional energy source is needed. Vibrational converters, air flow generators, and temperature gradient generators all produce 50-400$\frac{\mu W}{cm^3}$, as listed in Table 1.1. Of the three, vibrational converters are the simplest and have the most potential for wafer-scale fabrication. In conclusion, a 1cm^3 sensor node can support an average power draw of 100μW. A combination of solar and vibrational energy scavenging and battery energy storage is likely to yield the most robust and inexpensive solution.

In addition to limitations on average power dissipation, the available peak power levels that can be supplied to the electronics are also limited. Since most microscale energy scavenging and storage devices provide a naturally high impedance, the peak current drive capability is small (less than a few mA). Providing high drive current would require excessively large storage capacitors and complex voltage regulators. The RF datalink circuit design must address this issue by presenting a low peak active current draw.

The next section describes the implication of the energy scavenging requirements on the RF datalink.

1.4 RF Transceiver Requirements

This section describes the transceiver requirements that are unique to sensor node communication. As will be shown, the radio requirements are very different from traditional low power transceivers (pager receivers, RFID tags, Bluetooth-specification radios, keyless-entry).

1.4.1 Power Consumption

In the design of prototype sensor nodes, the wireless interface consumes the largest fraction of the power and size budget of the node. While the demands of the sensing and digital processing components cannot be ignored, their duty cycle is typically very low. A combination of advanced sleep, power-down, and leakage reduction techniques makes it possible to make their average power dissipation virtually negligible [4]. Thus, the wireless interface for sensor networks is the dominant source of power consumption. While optical communication approaches offer the potential of very low power and small size, line-of-sight and directivity considerations make them less attractive [5]. For this work, we will limit our discussion to RF interfaces.

1.4.2 Datarate

As mentioned, the requirements of a transceiver for wireless sensor networks differ dramatically from a traditional wireless link. Thus, common performance metrics such as $\frac{energy}{bit}$ and $\frac{\frac{bits}{s}}{Hz}$ should be applied with the realization that other factors prevail. For example, a modified metric such as $\frac{energy}{useful-bit}$ is relevant if all sources of power and overhead (for example: synchronization, the impact on energy storage) are included. First we will examine the typical operation mode of the sensor node. An investigation of the traffic patterns and data payloads reveal that the transceiver operation is fundamentally different than a wireless LAN or Bluetooth-specification radio. Data packets

in sensor networks tend to be relatively rare and unpredictable events. In most application scenarios, each node in the network sees only a few packets/second. In addition, the packets are relatively short (typically less than 200 bits/packet). This is expected as the payloads normally represent slowly varying and highly correlated environmental data measurements. Combined, this means that the average data rate of a single node rarely exceeds 1 $\frac{kbit}{s}$. These observations are of foremost importance when designing the wireless transceiver, as we will highlight in the following sections.

1.4.3 Range

In the rest of the discussion, we will assume that the sensor networks of interest are dense, which means that the nodes in the network are placed relatively closely (the average distance between nodes is less than or equal to 10m). For a given sensitivity, scaling the node to larger ranges would require additional transmit power or increased coding gain (longer transmit times). As the transmitted power increases in low power transmitters, the global transmitter efficiency increases. Thus, in short-distance links, increasing the transmitted power the preferred approach over increased coding gain. As the transmitted power increases, a linear increase in the link budget is obtained for a sub-linear increase in the transmitter power consumption. Improving the link budget through coding gain would involve linear or super-linear increases in the receive power consumption due to increased packet length and/or higher received bandwidths. Indeed, at transmitted power levels of

-10dBm and below, a majority of the transmit mode power is dissipated in the circuitry and not radiated from the antenna. However, at high transmit levels (over 0dBm), the active current draw of the transmitter is high. It is difficult to source high active currents with micro-scale energy scavengers and batteries. Convenient and efficient transmit power levels for sensor node applications are roughly in the range of -10 to +3 dBm.

1.4.4 Sensitivity

Figure 1.2 plots the theoretical range for a radio with a -70dBm sensitivity for various RF propagation models at 2GHz. As shown, the range varies greatly depending on the radio environment. For free space (where the path loss exponent r=2), a range of 37m is achieved with a 0dBm transmit power. However, in indoor environments, a higher exponent (r=3 or r=4) is more appropriate. In that regime, a transmit power of at least 0dBm is required for a 10m range. To add a margin for deep fading, the receiver sensitivity for a 0dBm transmit signal and a 10m range should be greater than -75dBm. Thus, for this application, a receiver sensitivity of better than -75dBm is imposed. Higher sensitivities will allow lower transmitted power levels, subject to the constraints in the previous section.

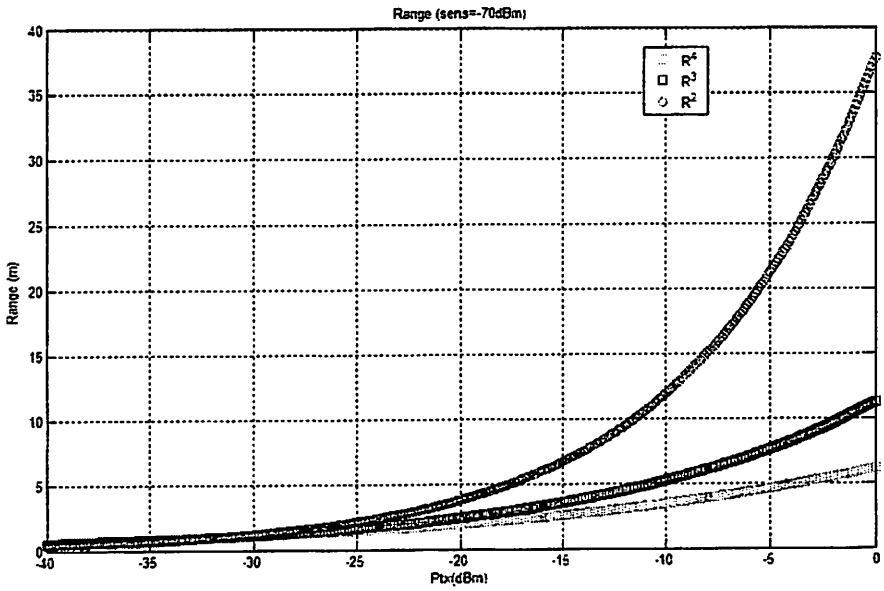


Figure 1.2: Radio range for receiver with a -70dBm sensitivity

1.4.5 Turn-On Time

In an environment in which the radio is in idle or off mode most of the time, and in which data communications are rare and packets short, it is essential that the radio start up very quickly. For instance, a typical 1Mbps Bluetooth-specification radio with a 500μs turn-on time would be poorly suited for the transmission of short packets. The on-time to send a 200 bit packet would be only 200μs. Start-up and acquisition represent an overhead that is larger than the actual payload cost, and could easily dominate the power budget (given that channel acquisition is typically the most power-

hungry operation). Thus, fast start-up and acquisition is essential to minimize this overhead. An agile radio architecture that allows for quick and efficient channel acquisition and synchronization is desirable. Complex wireless transceivers tend to use sophisticated algorithms such as interference cancellation and large constellation modulation schemes to improve bandwidth efficiency. These techniques translate into complex and lengthy synchronization procedures and may require accurate channel estimations. Packets are spaced almost seconds apart, which is beyond the coherence time of the channel. This means that these procedures have to be repeated for every packet, resulting in major overhead unsuitable in a low-power environment. Simple modulation and communication schemes are hence the desirable solution if agility is a prime requirement.

1.4.6 Integration/Power Tradeoff

Achieving the goal of a very low power/low cost RF design is complicated by a well documented power/integration (cost) tradeoff. For example, the use of high performance SiGe processes, while offering the designer high f_T operation and low bias current levels, eliminates the possibility of integration with low power digital systems. A multi-chip solution would prohibitively increase the cost and area for sensor network applications. Another common strategy for CMOS RF designers trying to reduce power consumption is to use high quality passive surface mount components [6]. This solution also prohibitively increases cost and board area, as each surface mount inductor

is larger than the entire transceiver chip.

Recently published "fully integrated" transceivers typically refer to a transceiver that has simply eliminated the need for external ceramic or surface acoustic wave (SAW) filters. They still, however, require an off-chip quartz crystal and various passive components. To meet the cost and form-factor requirements of this application, a truly fully integrated transceiver is mandatory. In addition to increasing the size, off-chip passives add to the complexity and cost of the board manufacturing and package design. In addition, these macro-fabricated components increase the manufactured performance distributions of the radio by adding completely uncorrelated component variations. One method that can be used to achieve a high level of integration is the use of a relatively high carrier frequency. Currently available simple low power radios, as used in control applications, typically operate at low carrier frequencies between 100 and 800MHz. A high carrier frequency has the distinct advantage of reducing the required values of the passive components, making integration easier. For example, a 2.53μH inductance is needed to tune out a 1pF capacitor in a narrow-band system at 100MHz, requiring a surface mount inductor. For a 2GHz carrier frequency, the inductance needed is only 6.33nH, which can easily be integrated on-chip using interconnect metallization layers. In addition, the critical antenna physical dimensions are linearly related to the carrier frequency. For a given antenna radiation pattern and efficiency, a higher carrier frequency allows for a much smaller antenna. A quarter-wavelength monopole antenna

at 100MHz would be 0.75m long. At 2GHz, the size shrinks to 37.5mm, allowing very efficient and inexpensive board-trace antennae. However, the drive to higher carrier frequencies in the interest of high integration is in direct conflict with the need for low power consumption. As the carrier frequency increases, the active devices in the RF signal path must be biased at higher cutoff frequencies, increasing the bias current and decreasing the transconductance-to-current $\frac{g_m}{I_d}$ ratio. The results is an increased power dissipation at higher carrier frequencies. Thus, there exists an inherent tradeoff between integration and power consumption that must be addressed through architectural decisions and the use of new technologies.

To reduce the die area and cost of the transceiver, the entire physical layer must be taken into account. For example, a simple, low power front-end with a large, power hungry A/D and complex digital baseband would be counterproductive. Thus, modulation schemes, datarates, and packet sizes that reduce baseband complexity must be embraced to optimize the global power consumption.

In conclusion, RF transceivers for wireless sensor networks must be simple, consume a minimum amount of on-current, and operate at high carrier frequencies to allow high levels of integration. In the next section, the current state-of-the-art in low power RF transceivers is discussed.

1.5 State-of-the-art

There has been substantial work in the field of low power transceivers for wireless sensing. Much of this work has focused on scaling down the power and datarate of traditional transceiver architectures for use in wireless sensing applications. As a case study, a two recent architectures reported in [7] and [8] will be discussed.

The first case study, reported by Peiris [7], achieves impressive sensitivity performance and low power consumption, truly representing the state-of-the-art in heterodyne transceivers for sensor networks.

The receiver, which can utilize either OOK or FSK modulation, was implemented in a 0.18μm CMOS process. Integration of a the transceiver, A/D converters, RISC microcontroller core and an SRAM block were achieved on the same chip. The receiver consumed 2.1mA from a 1V supply with a high sensitivity of -111dBm and -108dBm in the 433MHz and 868MHz band, respectively. The low current consumption is possible due to the relatively low carrier frequency used. External high Q inductors in the VCO tank reduce the power consumption and improve the phase-noise of the synthesizer block. The VCO phase noise was measured as -110 $\frac{dBc}{Hz}$ at 600kHz offset. The low carrier frequency prohibits the full integration of the VCO and LNA matching inductors, necessitating off-chip components. The antenna form-factor would also suffer from the relatively low carrier frequencies.

The second case study, reported by Molnar [8], uses an FSK modulation

scheme with a 900MHz carrier frequency. The transceiver operated from a 3V supply and dissipated 1.2mW for a sensitivity of -93dBm. A low-IF architecture was used. The transceiver made use of the relatively large supply voltage to share bias current between the LNA and the local oscillator. To reduce the power consumption, an off-chip high Q inductor was used for the VCO.

This work demonstrates that, although low power consumption and good sensitivity performances are possible using traditional architectures, complete integration remains elusive. An integration/power tradeoff is observed: as carrier frequencies are lowered to reduce the power consumption, passive components become more difficult to integrate and the antenna grows. In addition, a quartz crystal reference is still needed for the synthesizer. Thus, to achieve sub-mW receive power consumptions and full integration, new techniques must be explored.

1.6 Contributions of this Thesis

The following Chapters generally explore the following two main areas:

1. **CMOS/MEMS Co-Design:** Techniques for designing new MEMS technology with sub-micron CMOS circuitry are introduced. Many design examples are presented, including RF local oscillators, RF amplifiers, and low frequency reference clocks. Both low frequency electrostatic silicon resonators and high frequency bulk-acoustic wave res-

onators are covered. The increasing f_T of sub-micron CMOS processes is leveraged by using weak inversion biasing in all circuit blocks, from DC to 2GHz.

2. **Ultra-Low Power, Highly Integrated Radio Design:** Techniques and philosophies increasing the level of integration and decreasing the power consumption of CMOS transceivers beyond the current state-of-the-art are presented. A RF transmit beacon operating purely from scavenged energy is presented. Two fully functional receivers have been designed, implemented, and tested to validate these concepts. The first, a two-channel tuned radio frequency (TRF) architecture, demonstrates passive channel selection using MEMS resonators and is scalable to multiple channels. The second, using a super-regenerative architecture, achieves extremely low power dissipation (400μW) by using a MEMS resonator to set the RF frequency.

Chapter 2 outlines the design philosophies used in this research, such as MEMS/CMOS co-design and weak-inversion RF circuit design, and energy scavenging. To verify these philosophies, three proof-of-concept designs are presented: two RF circuit blocks and one system implementation. Advanced CMOS/RF MEMS circuit co-design research included the analysis, design, and implementation of a fully differential oscillator. Section 2.4 describes the circuit and compares the testing results to a single ended version with the same power consumption. To demonstrate the potential for energy scaven-

ing, a 2GHz transmit beacon operating indefinitely on scavenged energy is discussed.

Based on these concepts, a fully functional two-channel transceiver was designed, implemented, and tested. Chapter 3 fully documents this effort from the initial analysis phase through the testing methodology.

To further reduce power consumption, a super-regenerative radio architecture was investigated. A fully functional, prototype 400μW receiver was demonstrated. Chapter 4 presents the theory behind the receiver operation. The circuit design, implementation, and subsequent receiver testing results are revealed.

Chapter 5 describes a fully-integrated transceiver based on the super-regenerative radio. The pulse-width demodulator synthesis, analysis, and circuit design is described. In addition, a digitally programmable interface is implemented, which allows control over the receiver biasing, super-regenerative RF frequency, and the transmitter output tank frequency.

Chapter 6 describes an efficient and robust integration methodology for the transceiver. To address an important bottleneck in the implementation of wireless sensor networks, a proof-of-concept CMOS/MEMS 16MHz reference clock with amplitude control loop was designed and implemented. Section 6.1 provides a brief background into micromachined silicon resonators before describing the circuit design. Robust packaging techniques of the MEMS and CMOS components are then discussed. Performing a flip-chip of the MEMS chips directly onto the CMOS chips provides a low parasitic, low form-factor

system that saves both die and board area. Two proof-of-concept examples are provided.

Finally, Chapter 7 concludes the thesis with a summary and a discussion of directions for future work.

Chapter 2

Low Power CMOS Design for Radio Frequencies

In Chapter 1, an integration/power tradeoff was identified as one main obstacle to the implementation of small, cheap, low power transceivers for wireless sensor networks. This chapter describes the circuit design philosophies that have been developed to address these tradeoffs.

An important metric for RF blocks is the transconductance, which typically determines the total current consumption of the circuit. This chapter begins with a discussion of weak inversion circuit design, which is an increasingly relevant way of achieving efficient transconductance and is becoming more feasible with each technology node. Next, combining MEMS components with CMOS circuitry is shown to greatly reduce the reliance on external passive components. Three proof-of-concept chips are discussed to demonstrate the validity of these design strategies:

1. Circuit Proof-of-Concept I: 300μW Pierce BAW-Oscillator

2. Circuit Proof-of-Concept II: Differential $300\mu W$ BAW-Based Oscillator

3. System Proof-of-Concept: Energy Scavenging Transmit Beacon

We now turn to a discussion of weak inversion CMOS for Radio Frequencies.

2.1 Weak Inversion RF CMOS

As technology scaling relentlessly provides increasing digital clock frequencies, the effects on analog/RF circuit design continue to accumulate. Aggressive supply voltage scaling impedes the implementation of high dynamic range A/D converters and other precision analog circuitry. However, the increasing thickness and reduced resistivity of the copper metallization, coupled with the increased distance to the lossy substrate, allows the fabrication of high quality inductors and transmission lines. Subthreshold circuit design has been identified as a powerful tool in reducing the power consumption of the transceiver. Weak inversion circuit biasing has been used for years in low frequency analog circuit design [9] to achieve increased transconductance efficiency. However, increasing transistor f_Ts allows weak-inversion operation in some RF circuit blocks. The inversion coefficient (IC) describes the relative level of channel inversion, which is most easily determined by the device current density. As the current density decreases, the transconductance efficiency increases. Equation 2.1 shows the inversion coefficient as a function

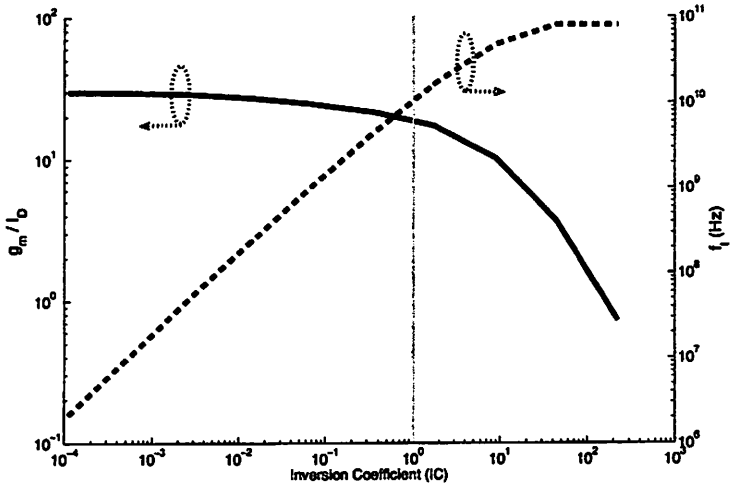


Figure 2.1: The transconductance efficiency is plotted vs. the inversion coefficient

of the transistor process parameters and operating point.

$$IC = \frac{I_d}{2nk'\frac{W}{L}V_t^2} = \frac{I_d}{I_o S} \tag{2.1}$$

Where n is the subthreshold slope factor, $k' = \mu C_{ox}$, $V_t = \frac{KT}{q}$, I_o is the specific device current, and S is the transistor aspect ratio. See Figure 2.1 for the transconductance efficiency vs. the inversion coefficent (IC) for a commonly used 0.13μm process [10].

The plot clearly shows the increase in transconductance efficiency as the inversion coefficent decreases. The line at IC=1 is considered the middle of moderate inversion. Since the performance of many RF circuit blocks is directly related to device transconductance, it is advantageous to maximize

the transconductance efficiency of all critical devices in order to reduce the necessary bias current. However, reducing the current density also results in a severely decreased device f_T. An optimization of the current density is required to provide the correct balance between transconductance efficiency and bandwidth. Plots such as Figure 2.1 are useful tools for designers when choosing appropriate transistor bias points. Technology scaling allows greatly increased f_T realization for a given IC. Thus, weak inversion biasing for RF design will become increasingly useful in future technology nodes.

Throughout this work, the IC of critical transistors will be discussed. Most of the RF devices are biased in moderate to weak inversion to achieve enhanced transconductance efficiency and reduced bias current.

2.2 MEMS Background

The relatively new field of Radio Frequency Microelectro Mechanical Systems (RF MEMS) provides unique opportunities for RF transceiver designers. This section provides background on RF MEMS and provides insight into the opportunities presented by these new technologies. The field of RF MEMS includes the design and utilization of RF filters, resonators, switches, and other passive mechanical structures constructed using bulk processed integrated circuit fabrication techniques. To date, these devices have been commercially used as discrete board-mounted components, primarily used to enhance the miniaturization of mobile phones. However, RF MEMS com-

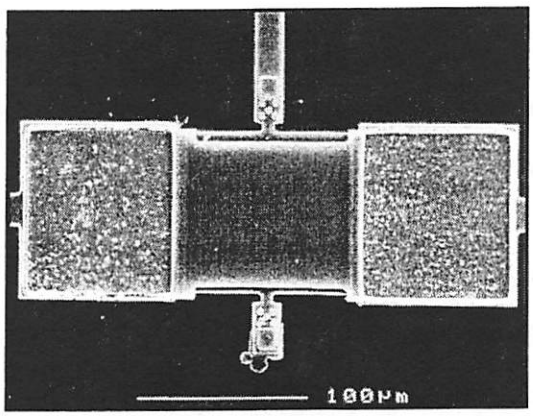


Figure 2.2: 50MHz Capacitively Driven/Sensed Resonator

ponents have the potential to be batch fabricated using existing integrated circuit fabrication techniques. Recent capacitively driven and sensed structures offer the potential of integration on the same substrate as the CMOS circuitry. In addition, because the resonant frequency of the structure is set lithographically, rather than by a deposition layer thickness, it is possible to fabricate devices with many unique resonant frequencies on the same die. See Figure 2.2 for an example of this technology. This resonator was constructed of micromachined polysilicon on a silicon wafer [11]. The continued improvement in the performance, reliability, and manufacturability of these structures will greatly change the performance and form-factor of RF transceivers by allowing the reliable fabrication of advanced mechanical structures on the same substrate as the circuitry. However, as will be shown in this chapter, these devices hold the potential to enable new circuit blocks and architectures even in their present state as off-chip components.

At the onset of this project, RF MEMS was identified as an emerging technology with the potential to benefit low power RF transceivers. These devices provide three main benefits to circuit designers:

1. **High quality factor (Q) resonant structure.** BAW resonators can achieve quality factors greater than 1000, about 100X higher than on-chip LC resonators. The resulting increased RF filtering ability both reduces oscillator phase noise and reduces frequency pulling/pushing of oscillators.

   When used in the design of bandpass filters and duplexers, high Q resonators help to realize the steep skirts necessary to meet cell phone specifications [12]. High Q resonators are further useful in a variety of other transceiver blocks. For example, high Q resonators provide the potential for radio frequency channel select filtering, as their bandwidth is much narrower than what can be obtained from integrated LC filters. This passive channel select filtering can be exploited to simplify the receiver architecture and to reduce the number of active components. In addition, when used in an RF oscillator, RF MEMS resonators provide a vastly improved phase noise compared to a standard, low Q LC resonator [13].

2. **Passive RF frequency reference.** For all narrowband communication systems, an RF carrier frequency generator is necessary. The absolute frequency reference used is typically a low frequency quartz

crystal oscillator. The low frequency sinusoid is then multiplied up to radio frequencies by a frequency synthesizer. This technique has a few disadvantages for low power radio design. First, even for a fully integrated frequency synthesizer, an off-chip quartz crystal is always necessary, rendering true full integration impossible. In addition, frequency synthesizers are a large source of power dissipation in low power radios [6]. The VCO and frequency dividers tend to dominate the power consumption of frequency synthesizers. Radio frequency MEMS components provide an inherent high-frequency reference without the need for a power hungry frequency synthesizer.

3. **CMOS/MEMS co-design.** Since MEMS structures are fabricated using the same thin-film fabrication techniques as integrated circuits, each device may be custom-designed for its intended application. This provides additional degrees-of-freedom to the circuit designer. Unlike quartz crystals or discrete 50Ω filters, this flexibility allows the circuit designer to control impedance levels for minimal power consumption. One of the most exciting aspects of RF micromachined components is the potential for co-designing the MEMS devices with the CMOS circuitry. Until now, passive components are either low quality on-chip devices (inductors, capacitors) or high quality off-chip components (inductors, SAW filters, quartz crystals, duplexers). The on-chip components allow customization to meet the requirements of the circuitry, but their performance is usually poor. Meanwhile, high quality off-chip

passives offer few designer degrees of freedom. For example, most filters and duplexers are designed for 50Ω input and output impedances. This rigid impedance level is very detrimental from a low power point of view, and has been extremely troublesome in past receiver implementations [14]. The potential of integrating RF MEMS components and circuitry on the same die or on the same substrate using, for instance, fluidic self assembly (FSA) could allow the circuit designer to size the MEMS components and the circuitry simultaneously [15]. The ability to design these devices alongside the circuitry provides increased system performance and additional designer degrees of freedom.

Currently, many industrial (Infineon, ST Microelectronics, Agilent) and academic (University of Michigan, U.C. Berkeley) organizations have begun development of RF MEMS resonators. One promising technology is the Bulk Acoustic Wave (BAW, FBAR) piezoelectric resonator [16]. The FBAR employs a metal-piezo-metal sandwich to achieve a high frequency, tightly controlled second order resonance with an unloaded Q of approximately 1200. As shown in Figure 2.3, the resonator can be modeled as a series LCR circuit, with a series resonance occurring at $f_s = \frac{1}{\sqrt{L_x C_x}}$ or approximately 1.9GHz in this design. Capacitor C_o represents a parasitic feedthrough capacitance created by the parallel plates of the resonator. R_o models the finite quality factor of the feedthrough capacitance. Z_s and Z_p represent the loading effects of the CMOS circuitry on the resonator. These external impedances have a large effect on the resonator quality factor, resonant frequency, and

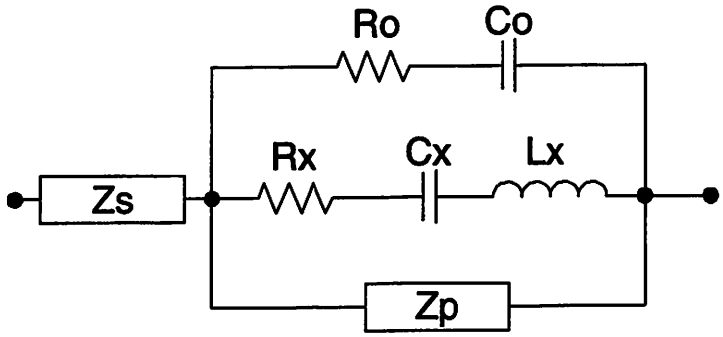


Figure 2.3: Simplified circuit equivalent model of a BAW resonator.

frequency stability. In current applications, FBARs are combined into ladder structures and used as duplexers and bandpass filters for wireless applications [16]. Used in this manner, a much smaller form factor is achieved over traditional RF duplexers and filters. For low power transceivers, it is desirable to use single resonators to achieve a high quality factor and very narrow bandwidth. Referring to Figure 2.3, it is possible to distinguish two different resonant modes. The first, occurring at the *series resonance*, allows a low impedance path through the resonator at RF frequencies. At the series resonance, the effective series impedance is approximately R_x. Above the series resonance, the structure looks inductive and will naturally tune out any parallel capacitive elements. This produces the *parallel resonance*, which occurs approximately 20MHz above the series resonance. At the parallel resonance, there is a circulation of RF current through the resonator and the feedthrough capacitor C_o. Due to this current circulation, at the parallel resonance the impedance of the structure increases dramatically to a

value approximately 3 orders of magnitude higher than the series resonance. To avoid detuning the resonator in the series resonant mode, the impedance added to the resonator by the electronics (Z_s) must be small compared to R_x, or a few ohms. This is typically not possible using low power RF design techniques, where high impedances are necessary to reduce the current consumption. To avoid detuning the parallel resonant mode, the shunting impedance presented by the electronics (Z_p) must be much higher than the resonator impedance at parallel resonance (approximately 2kΩ). Thus, for low power RF transceiver design, it is desirable to operate on the parallel resonance of the resonator [17]. It should be noted, however, that the intrinsic quality factor of the series resonance will be higher than the parallel resonance due to the additional resistive losses of the circulating RF current.

The frequency stability of high Q resonators is a key feature that provides much more reliable operation that other LC-based frequency generators. Equation 2.2 shows the sensitivity of the parallel resonance[1] to capacitive variation.

$$\frac{\delta f_p}{\delta C_T} \simeq f_{series} \frac{-C_x}{2C_T^2} \tag{2.2}$$

C_T describes the total capacitive loading on the resonator This equation corresponds to a sensitivity of approximately -10kHz/fF of frequency variation due to process, temperature, or non-linear capacitor bias point shift. Equa-

[1] And thus the subsequent oscillation frequency.

tion 2.3 shows the frequency sensitivity of an LC tank to capacitive variation.

$$\frac{\delta f}{\delta C_T} = \frac{-C^{-3/2}}{4\pi\sqrt{L}} \tag{2.3}$$

For a tank defined by a 5nH inductance at 2GHz, a typical value for a fully-integrated oscillator, the frequency sensitivity is -856kHz/fF, nearly two orders of magnitude higher than the BAW resonator. Thus, an LC resonance would always need to be frequency locked to a reference even if perfect frequency accuracy were possible. In contrast, a BAW resonator, if sufficient accuracy were available, would not need to be frequency locked. This is a fundamental benefit of using high Q MEMS resonators in low power transceivers.

2.3 Circuit Proof-of-Concept I: 300μW Pierce Oscillator

To demonstrate the concepts presented in Sections 2.2 and 2.1, a proof-of-concept circuit was designed, implemented, and measured in a 0.18μm standard CMOS process [13] [17]. The goals of this project were threefold:

- A proof-of-concept circuit would verify the resonator/CMOS models and the co-design methodology. This verification is necessary as the accuracy of the models for MEMS components and weak inversion CMOS at RF frequencies are not as heavily developed as the traditional mod-

els for strong inversion CMOS circuitry, which designers have become accustomed to.

- A prototype would allow the refinement of the unresolved resonator/CMOS packaging and interconnect problem.
- This circuit, when used as a local oscillator, would also provide a stepping-stone to the implementation of an entire low power transceiver.

This section describes the state-of-the-art in transceiver local oscillator design. Used to generate the transmitted carrier frequency and the local oscillator (LO) signal, a stable, low-noise RF sinusoid generator is crucial for the performance of an RF link. Traditionally, this signal is obtained through frequency synthesis, which entails multiplying the frequency of a stable low frequency crystal oscillator via a phase- or delay- locked loop (PLL or DLL) [18]. There are, however, serious drawbacks with a frequency synthesizer. First, due to the low Q of the voltage controlled oscillator (VCO) tank and finite loop bandwidth of the PLL, the phase noise of the crystal oscillator is severely degraded by the frequency synthesizer. Secondly, the synthesizer consumes large amounts of power in the VCO and frequency dividers.

A few examples are useful for putting the problem in perspective. In a recent ultra low power frequency synthesizer design, approximately 400μW was consumed to provide a 434MHz carrier [6]. As the carrier frequency of these systems is increased into the GHz range, the power consumption of

the frequency synthesizer increases dramatically. Outstanding phase noise performance can be achieved at the expense of high power dissipation. A recent high-performance 900MHz frequency synthesizer consumed 130mW with a phase noise of -127$\frac{dBc}{Hz}$ at a 330kHz offset [18]. The start-up time of a traditional frequency synthesizer is relatively long, and can be very inefficient if the transceiver requires agile duty-cycling and short packet transmission. Additionally, even with a "fully integrated" synthesizer, an off-chip quartz crystal is always required. Crystal oscillators typically exhibit very low phase noise due to the high quality factor of the crystal resonator. However, the resonant frequencies of quartz crystals are lower than most desired carrier frequencies, so frequency synthesis is usually required. A recent crystal oscillator implementation reports a phase noise of -113$\frac{dBc}{Hz}$ at 300Hz offset for a 78MHz oscillation frequency with a power dissipation of 340μW [19] .

Another option is to use an integrated free-running LC-oscillator without a frequency reference. This could satisfy the need for a fast start-up time and low power dissipation, but the frequency variation and phase noise of such a design would be prohibitively poor. In [13], we presented an alternate method of sinusoid generation. A frequency reference is generated directly at the RF frequency of interest, with no low frequency reference. This is accomplished by placing a BAW resonator in the feedback path of a CMOS oscillator, ultimately combining the frequency stability of a mechanical resonance with the low power capability of standard submicron CMOS. The technique of co-designing the resonator with the CMOS electronics provides an extremely

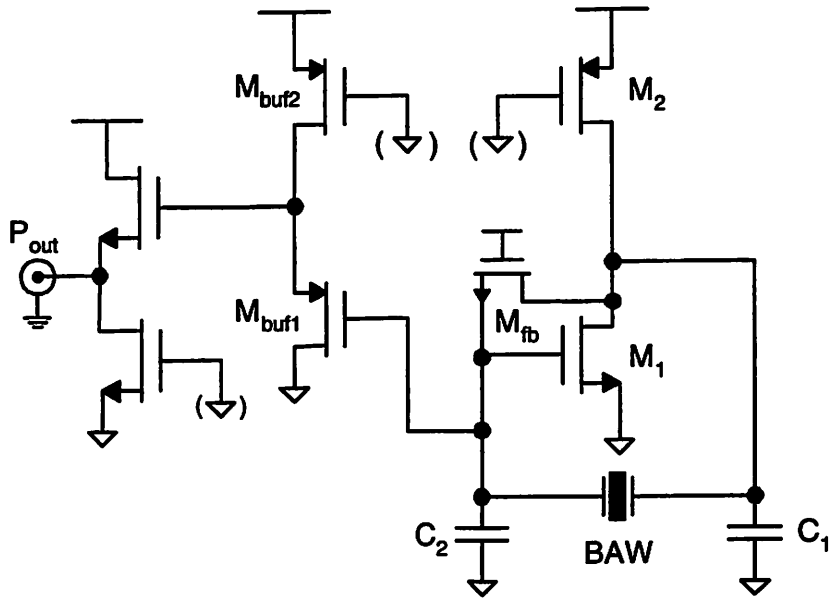


Figure 2.4: Simplified oscillator schematic

low power solution.

In this design, a single resonator is used to maximize the loaded Q of the oscillator. The impedance of the resonator is less than 5Ω at series resonance and larger than 1500 ohms at parallel resonance. Thus, to avoid severely loading the natural Q of the resonator, operation at the parallel resonance of the FBAR was chosen. The resonator occupies an area of approximately 100μm x 100μm and is wire-bonded directly to the CMOS chip containing the circuitry. The Pierce oscillator topology was chosen for its low phase noise potential and because it operates on the parallel resonance of the FBAR, allowing a higher loaded Q. A circuit schematic of the oscillator is shown in Figure 2.4. The signal is DC coupled to the first stage of the output buffer

(M_{buf1}). Capacitors C_1 and C_2 represent the device, interconnect, and pad capacitances. Accurate modeling and prediction of these values is crucial for the high frequency implementation of this topology. Transistor M_{fb} acts as a large resistor to provide bias to M_1. At the parallel resonance of the resonator, C_1, C_2, and C_o are tuned out. M_1 sees a high impedance at its drain node, allowing oscillation at this frequency. The sizing and layout of the circuit and resonator was optimized to minimize the power consumption of the oscillator.

At resonance, the initial loop gain is $A_L = g_{m1}R_L\frac{C_1}{C_2}$ where R_L is the real impedance seen at the drain of M_1 at the parallel resonance of the resonator. It can be shown that the optimal frequency stability and start-up factor are achieved with C_1=C_2 [20]. Therefore, to minimize the transconductance necessary for oscillation and to maximize the output voltage swing for a given bias current, R_L was maximized. For a given frequency, BAW resonators may be designed with various membrane areas. As the area increases, the motional resistance (R_x) decreases. However, increasing the area also increases the feedthrough capacitance C_o. Increasing R_x degrades the loaded Q of the oscillator, thus decreasing R_L. Increasing C_o has a similarly detrimental effect. Thus, it is possible to calculate an optimal resonator area that minimizes the power dissipation and phase noise of the oscillator. Figure 2.5 plots R_L vs. the normalized resonator area for various values of C_1=C_2. Using this technique, an optimal resonator area of approximately (100x100)μm^2 was chosen for fabrication. The curve marker in Figure 2.5

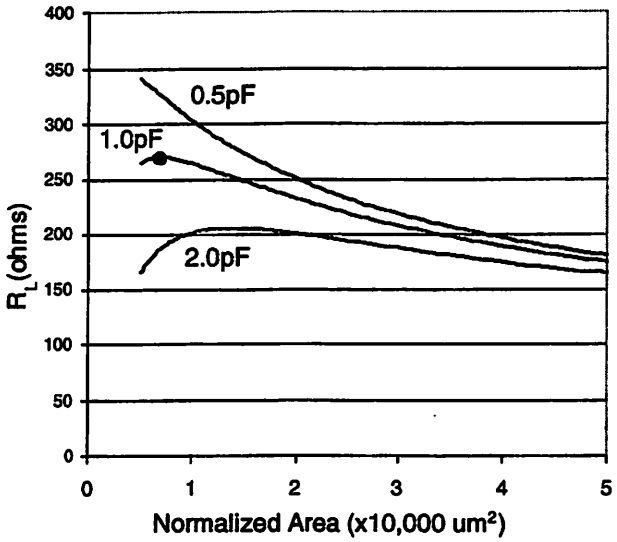


Figure 2.5: Optimization of BAW resonator area. Three curves are shown with various values of $C_1 = C_2$

indicates the design point. It is important to note that the finite Q of the CMOS device and pad capacitance must be taken into account, as they also reduce the loaded Q of the oscillator. This optimization led to a maximized value of R_L at parallel resonance. The desired voltage swing of the oscillator was 100mV zero-peak. The equation $V_0 = I_1 R_L$ relates the desired voltage swing to the first harmonic component of the drain current of M_1. Thus, since the oscillator is operated in the current-limited regime, the necessary oscillator core bias current is 300μA. As discussed in Section 2.1, weak inversion operation provides higher transconductance efficiency ($\frac{g_m}{I_d}$). The sizing of transistor M_1 (500/0.18)μm was chosen as to provide subthreshold operation, ensuring sufficient initial transconductance for reliable start-up. For transistor M_1, $IC = 0.2$, yielding $\frac{g_m}{I_d} = 23$.

A symmetric resonator layout allowed equal loading on the drive and sense electrode. The resonator was wirebonded directly to the CMOS chip to eliminate board parasitics, which would drastically degrade the resonator response. To accomplish this, the CMOS and BAW pad layouts were constructed with equal spacing so the chips could be mounted in close proximity to each other and directly wirebonded. See Figure 2.6 for a photograph of the completed prototype. The two chips were bonded with conductive epoxy to a grounded substrate, resulting in A 200μm spacing between the chips. A custom assembly with two bondwires per interconnect was used in the initial prototype to reduce the bondwire inductance, but subsequent experimentation showed that standard chip-on-board (COB) assembly using one

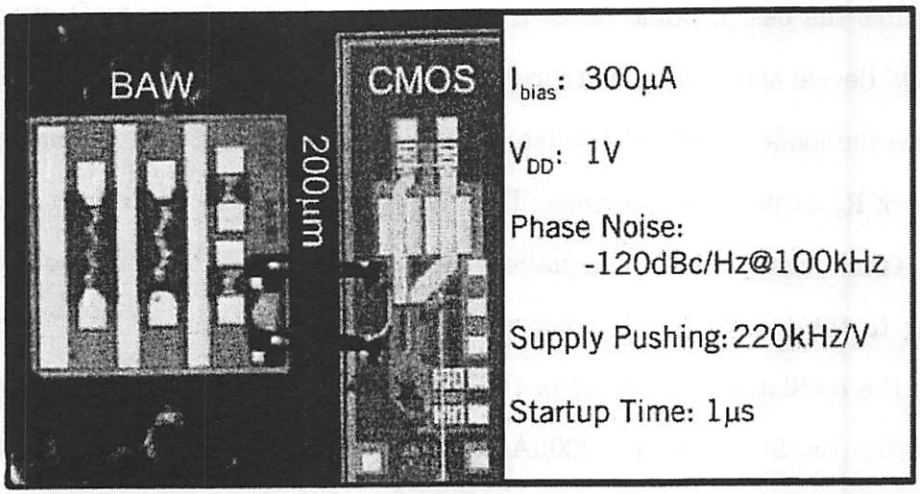


Figure 2.6: Photograph of the CMOS/BAW prototype oscillator

bondwire per pad and a 500μm chip spacing was adequate. The oscillator core was biased at 300μA with a power supply voltage of 1V. The amplitudes of the 2^{nd}, 3^{rd}, 4^{th}, and 5^{th} harmonics were measured to be 30dB, 36dB, 45dB, and 49dB below the carrier, respectively. The measured phase noise performance is shown in Figure 2.7. Phase-noise was measured with an *Agilent E4445A PSA* and verified with an *HP 3048A* phase noise measurement system. The measured phase noise of the oscillator is -100$\frac{dBc}{Hz}$at 10kHz offset, -120$\frac{dBc}{Hz}$at 100kHz offset, and -140$\frac{dBc}{Hz}$at 1MHz offset. The start-up time of the oscillator was measured to be approximately 800ns, making it suitable as a frequency reference for receivers requiring agile duty-cycling. For example, it is possible to cycle the oscillator on/off between transmitted bits for low data rate OOK transceivers. Indeed, this property forms the basis for the transmitter that will be presented in Chapter 3. In addition,

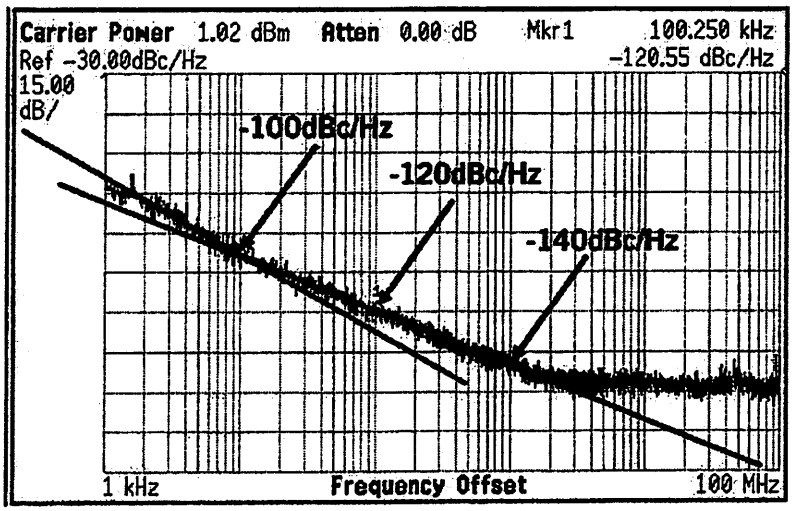


Figure 2.7: Measured phase noise performance of the oscillator

it was experimentally verified that analog pulse shaping of the OOK signal is possible by modulating the bias current of the oscillator as a function of time. Second, third, and fourth-generation oscillators have been fabricated and tested in a 0.13μm CMOS process, and similar performance results were observed. The supply pushing of the oscillator was measured to be $220\frac{kHz}{V}$, yielding only a 26.4kHz frequency shift over a 10% supply voltage variation. The temperature coefficient of oscillation was also measured. A plot and detailed discussion of the effect of temperature on the oscillator is presented in Section 2.4, Figure 2.14. A useful FOM for comparing the performance of RF oscillators is given by Equation 2.4 [21].

$$FOM = 10log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega)\cdot V_{DD}\cdot I_{DD}}\right] \tag{2.4}$$

This FOM was used to compare some recently published low power RF oscillators. Table 2.1 shows a breakdown of oscillator performance and FOM for these oscillators. This table depicts low power oscillators using a variety

Table 2.1: Comparison of recently published RF oscillators

Parameter	This work [13]	[6]	[21]	[22]
Power Consumption (μW)	300	230	1460	100
V_{dd} (V)	1	1	0.35	0.5
Oscillation Frequency (GHz)	1.9	0.4	1.4	1.9
Phase Noise ($\frac{dBc}{Hz}$ @ 1MHz)	-140	-118	-129	-114
FOM (dB)	210	177	190	190
Comment	BAW	SMT L	Integ. L	Bondwire L

of tuning elements, including surface mount inductors, on-chip integrated inductors, and bondwire inductors. As shown in the table, the co-design of BAW resonators and subthreshold-biased CMOS circuitry provides FOM performance at least two orders of magnitude above the state-of-the-art in RF oscillators.

Co-design and optimization of CMOS circuitry and RF MEMS components will become an increasingly important tool with the proliferation of this technology. The imminent integration of RF MEMS on the same silicon substrate as the CMOS will enhance the performance of the system as well as the need for co-design.

2.4 Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator

In Section 2.3, the co-design of a single-ended CMOS oscillator and BAW was presented. However, to achieve better supply rejection and higher output swings, a differential topology is often used. The goal of the work presented in this chapter was to design a differential BAW-based oscillator for direct comparison with the single-ended oscillator presented in Section 2.3. This section presents the design, implementation, and testing of a 300μW differential BAW based oscillator.

2.4.1 Analysis/Design

The goal of the differential oscillator is to drive the BAW resonator symmetrically and excite its parallel resonance while maintaining symmetry throughout the oscillator. In many traditional integrated differential oscillators, the negative resistance of the sustaining amplifier is achieved through a cross-coupled transistor pair. Looking into the cross-coupled pair, a wideband, DC-to-RF negative resistance is created. To achieve oscillation at a certain frequency, a parallel LC load is used to provide a high impedance at that frequency. At this frequency, the total tank impedance is negative and oscillation occurs. Bias current can conveniently be provided through the same inductors that tune out the tank capacitance.

A mechanical resonator-based differential oscillator, however, is more

complicated. The following issues had to be overcome for successful implementation:

- **Low frequency stability:** The resonator can be shunted across the cross-coupled pair, providing a high Q response at the parallel resonance to set the oscillation frequency. However, at low frequencies, the resonator presents a high impedance. Thus, the circuit would be DC unstable and latch-up like a comparator.

- **Loaded Q:** Bias current must be supplied to the cross-coupled pair without de-tuning the BAW resonator at RF frequencies. Thus, a high impedance circuit environment at high frequencies is necessary.

- **Common-mode control:**A high-impedance bias circuit necessitates common-mode control over the oscillator core.

Current sources could be used to supply bias current to the cross-coupled pair without de-tuning the resonator, but latch-up would occur. One way to circumvent this problem is to design a high-pass response into the cross-coupled pair negative resistance. This is realized by using separate current sources for the cross-coupled pair and coupling the sources through a capacitor [23]. At low frequencies, the cross-coupled pair experiences a large degeneration, reducing the negative resistance. At high frequencies, the sources interact, providing full transconducance from the cross-coupled pair. The simplified schematic of the oscillator is shown in Figure 2.8. It can be shown

2.4 Circuit Proof-of-Concept II: Differential $300\mu W$ BAW-Based Oscillator

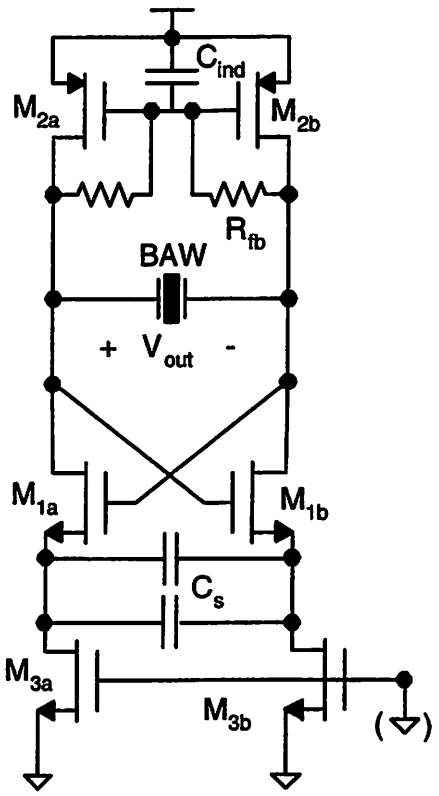
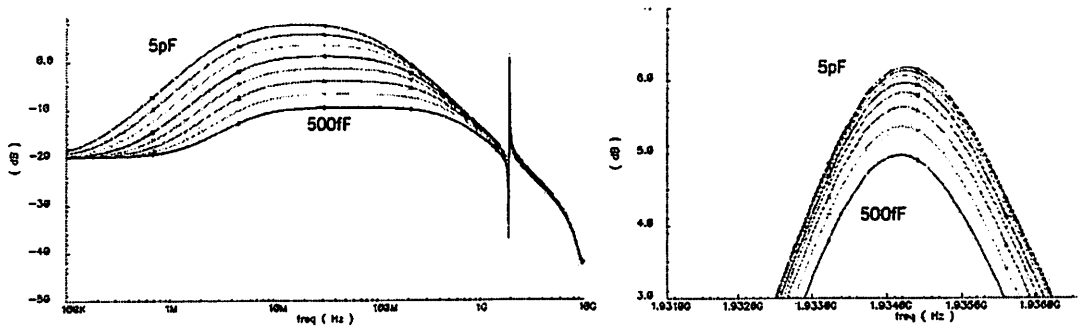


Figure 2.8: Simplified schematic of differential oscillator



(a) Oscillator loop-gain over C_s (b) Detail of parallel resonance

Figure 2.9: Simulation results of oscillator loopgain for varying values of C_s

that the differential impedance looking down into the cross-coupled pair is given by Equation 2.5.

$$Z_{cc} = \frac{-1}{g_{m1}}[1 + \frac{g_{m1}}{s2C_s}] \tag{2.5}$$

Thus, at high frequencies, the structure provides $\frac{-1}{g_{m1}}\Omega$ of negative resistance. The effect of varying values of C_s is shown by the simulation results in Figure 2.9 (a) and (b). Figure 2.9 (a) shows the AC analysis of the oscillator loopgain for various values of C_s, swept logarithmically from 500fF to 5pF. The high Q BAW resonator series and parallel resonance is clearly visible. The desired oscillation mode is at the 1.9GHz parallel resonance peak. There is also a low Q low frequency resonance visible in the response due to the inductive nature of the capacitively degenerated cross-coupled pair interacting with the BAW parallel plate capacitance. This resonance would cause a parasitic oscillation if the loopgain exceeded 0dB, and the stability would degrade as the parallel plate capacitance increased. To improve stability, C_s

should be made small. However, reducing C_s increases the negative resistance pole frequency in Equation 2.5, thus reducing the oscillator loop gain at the desired resonance. Figure 2.9 (b) shows a close-up of the oscillator loop gain at resonance for various values of C_s. The loop-gain degradation is clearly shown as C_s is decreased. Thus, proper choice of C_s is crucial for stable and efficient oscillation. For this oscillator, C_s=1pF was chosen to provide stable operation over a range of BAW resonators.

The next difficulty is achieving a stable common-mode voltage equilibrium. The common-mode feedback must not degrade the high frequency differential impedance of the current sources. To achieve a low LF common-mode impedance and a high HF differential-mode impedance, a self-biasing common mode feedback circuit was developed. This structure consists of M_{2a}, M_{2b}, R_{fb}, and C_{ind}. At low frequencies, the common-mode impedance looking into the inductor is $\frac{1}{g_{m2}}$. At RF, the differential impedance is $R_{fb}//R_{o2}$. Thus, the structure provides a stable DC common-mode operating point but does not de-tune the high Q BAW resonator. One drawback of the structure is that it consumes substantial supply headroom, limiting the low voltage operation potential of the oscillator. The common-mode voltage is easily adjustable by varying the aspect ratio of transistors M_{2a} and M_{2b}.

The sizing of the cross-coupled pair is an important consideration for achieving low power consumption. For oscillation, the transconductance of each device is dictated by the following: $g_m > \frac{2}{R_{p,res}}$. The sizing is a tradeoff between transconductance efficiency and f_T degradation in the weak inversion

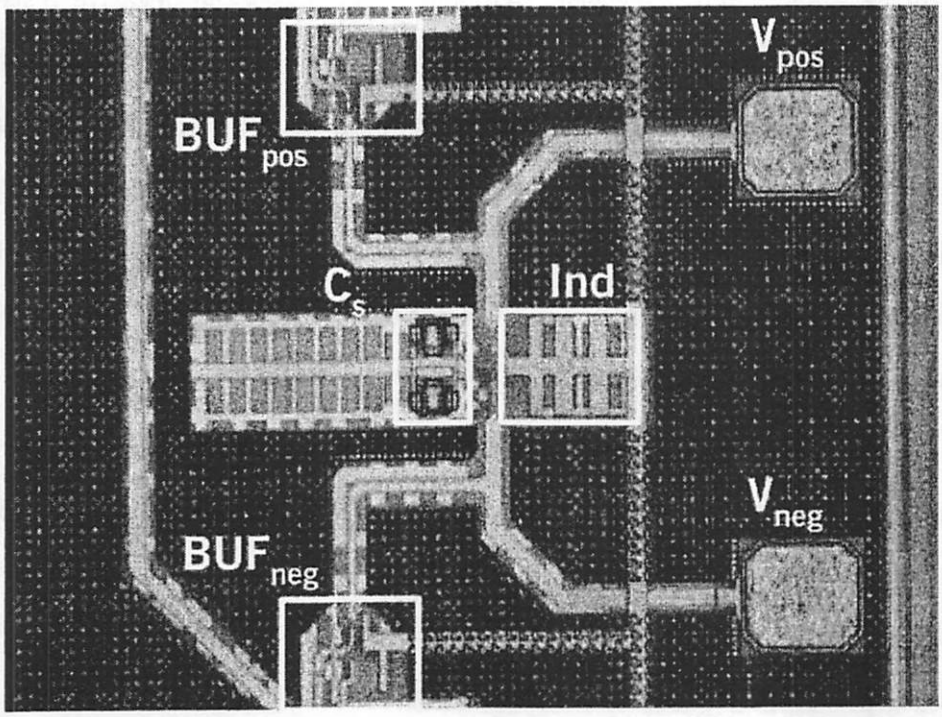


Figure 2.10: Differential oscillator layout detail

regime. The devices were sized at $\frac{100\mu m}{0.13\mu m}$, yielding an inversion coefficient of 0.33, providing a $\frac{g_m}{I_d}$ of approximately 21.

2.4.2 Experimental Results (1.9GHz)

To verify these concepts, the oscillator was implemented in a standard 0.13μm CMOS process. The layout detail is shown in Figure 2.10. The oscillator layout was symmetric with a 290μm pad-to-pad spacing of the BAW interconnect pads. Both oscillator outputs are buffered with self-biased 50Ω output drivers that present a 100fF capacitance to the oscillator core. The active

2.4 Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator

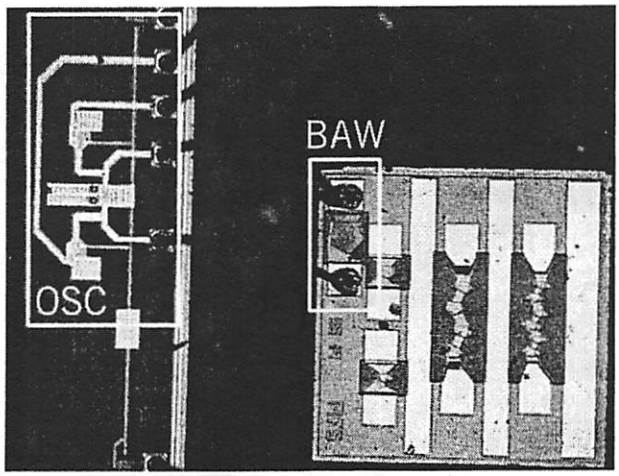


Figure 2.11: Differential oscillator COB assembly

inductor structure and output buffers are visible in the photo. Capacitor C_s, also visible, was split into two cross-coupled capacitors to eliminate the asymmetry of the back plate connection. The oscillator layout is symmetric up to the buffer outputs, where an asymmetric pad structure was used for die area efficiency. A photograph of the oscillator COB assembly is shown in Figure 2.11. The board was assembled using standard COB techniques with no special processes required. The oscillator was then tested over various bias current levels. Oscillation was sustained at a bias current as low as 155μA total, corresponding to a g_m of approximately 1.6mS for each cross-coupled device. Thus, back-calculating the resonator parallel resonant impedance reveals $R_{p,resonator} = \frac{2}{g_m} = 1.2k\Omega$, agreeing well with calculations. The differential zero-peak swing for a 155μA bias current was 50mV. The output swing increased linearly with bias current up to a total bias of 600μA, where the

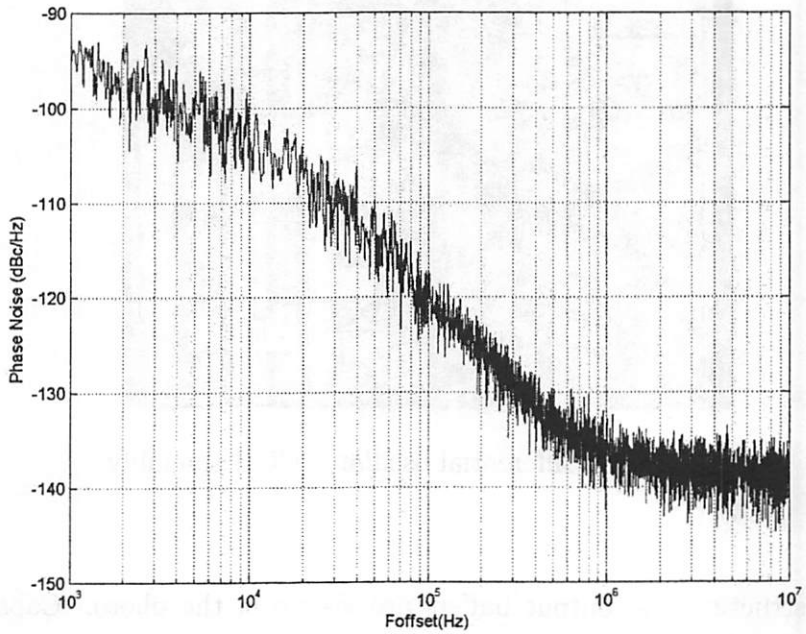


Figure 2.12: Measured differential oscillator phase noise

differential voltage swing was 318mV zero-peak. As the current was further increased, the oscillator entered the voltage-limited regime and subsequent increases in bias currents resulted in diminishing increases in voltage swing.

Next, the oscillator was biased to the design value of 300μA (150μA through each leg) for the remainder of the testing, yielding a differential output power of -13.2dBm (corresponding to an oscillator core differential swing of approximately 200mV zero-peak). The phase noise was measured with an *Agilent E4445A PSA*. The data is plotted in Figure 2.12. A comparison of this phase noise measurement to that from the Pierce oscillator presented

in Section 2.3 reveals interesting results. Since both oscillators operate with nearly equal differential voltage swings across the resonator (200mV zero-peak) and nearly equal resonator impedances, it follows that the power in the resonant tank is nearly identical. In addition, because the resonator quality factors are nearly equal, the phase noise of the both oscillators, calculated with Leeson's formula, yield similar results.

Table 2.2 shows the phase noise comparison of the differential oscillator to the Pierce oscillator presented in Section 2.3. Notice that the phase noise

Table 2.2: Measured oscillator phase noise ($\frac{dBc}{Hz}$)

f_{offset}(Hz)	Differential	Pierce
10k	-103.3	-100
100k	-120.3	-120
1M	-136.4	-140

performances of the two oscillators are very similar. An oscillator supply-pushing performance of $500\frac{kHz}{V}$ was measured over a V_{dd} range of 0.7V to 1.4V. The low supply-pushing figure is due to the low resonator frequency dependence to non-linear capacitor bias point shifts, as explained in Section 2.2. A 10% variation in the nominal 1.2V supply would result in only a 60kHz frequency shift.

The measured harmonic components of the differential and Pierce oscillators are compared in Table 2.3. As expected, the even order harmonics of the differential oscillator are suppressed by the differential architecture. The fourth harmonic was below the noise floor of the spectrum analyzer.

Table 2.3: Measured oscillator harmonic distortion (dBc)

Harmonic	Differential	Pierce
Second	-55	-30
Third	-58	-36
Fourth	–	-45
Fifth	-65	-49

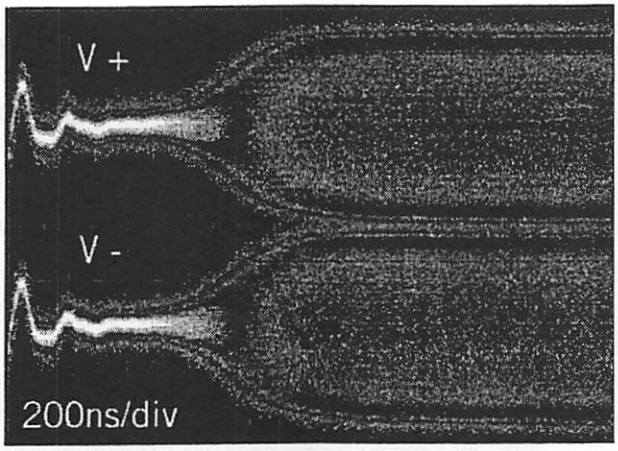


Figure 2.13: Measured differential oscillator start-up transient

The start-up time of the oscillator was measured with an *Agilent 54855A* 8bit, 6GHz oscilloscope. Figure 2.13 shows the measured oscillator start-up transient. The positive and negative output voltages of the differential oscillator are shown. The start-up time, measured from the onset of bias current to oscillator saturation, is approximately $1\mu s$. This matches, both theoretically and experimentally, the start-up time of the Pierce oscillator presented in Section 2.3. This result is expected because both oscillators have similar tank quality factors and initial loop gains.

2.4 Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator

The temperature dependence of a BAW-tuned reference oscillator is important because it is not locked to a stable temperature compensated crystal reference. As described in [24], the temperature coefficient of the parallel resonance of a Molybdenum/Aluminum Nitride/Molybdenum (Mo/AlN/Mo) BAW resonator is approximately -25$\frac{ppm}{^oC}$. For a high Q resonant structure, the resonator temperature coefficient should determine the temperature coefficient of oscillation frequency (TCF). To verify this relationship, the differential oscillator frequency was measured over a temperature range of -20°C to 100°C. This measurement was performed with a *Thermonics T-2420* temperature forcing system. In addition, the Pierce oscillator that will be used in Chapter 3 was measured over the same range for comparison. See Figure 2.14 for the measured results. The differential oscillator uses a custom-designed 70Ω resonator while the Pierce uses a 50Ω resonator test structure. The theoretical -25$\frac{ppm}{^oC}$ curve was plotted for reference. As expected, the measured TCF of both oscillators closely match the theoretical resonator coefficient. The Pierce oscillator shows a slightly higher TCF that increases with temperature. This increase is due to the temperature dependence of the CMOS power amplifier that loads the oscillator. The addition of temperature-independent bias stabilization circuitry would return the curve to its theoretical TCF value. The linear, known TCF response may be easily compensated to provide a stable frequency reference. A compensation circuit providing approximately -5$\frac{fF}{^oC}$ to the resonator would provide temperature stability. In completely uncompensated form, both oscillators exhibit a +/-

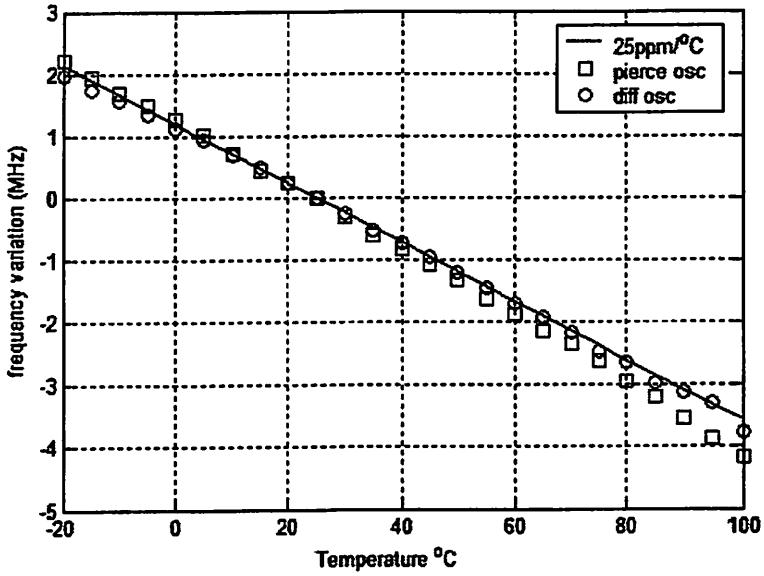


Figure 2.14: Measured temperature coefficient of oscillation for two CMOS oscillators

1MHz tolerance from 5°C to 45°C.

The motional resistance of the BAW resonator also exhibits a temperature dependence [24]. Important to low power CMOS oscillators is the temperature coefficient of the parallel resistance, which affects the oscillator loop-gain, output swing, and phase noise performance. This temperature coefficient is approximately -1500$\frac{ppm}{°C}$. Over a range of -20°C to 100°C, R_p decreases by approximately 18%. This relatively small variation is easily compensated by oscillator amplitude control circuitry.

2.4.3 Experimental Results (2.4GHz)

As designed, the differential oscillator can operate successfully over a wide frequency range with no modifications. One particularly interesting frequency band is the 2.4GHz ISM[2] band. This band is sufficiently high to allow completely integrated inductors, but low enough to allow subthreshold RF transistor biasing and low power consumption.

It should be noted that there is an optimal C_s for each oscillation frequency. As the frequency increases, the allowable cross-coupled pair pole frequency (given by Equation 2.5) can be increased, allowing a smaller C_s and thus higher stability against low frequency parasitic oscillations. A custom 2.4GHz resonator was designed and fabricated to demonstrate oscillator operation in this frequency band. Figure 2.15 shows a photograph of the completed ISM band oscillator implementation.

[2]Industrial, Scientific, and Medical

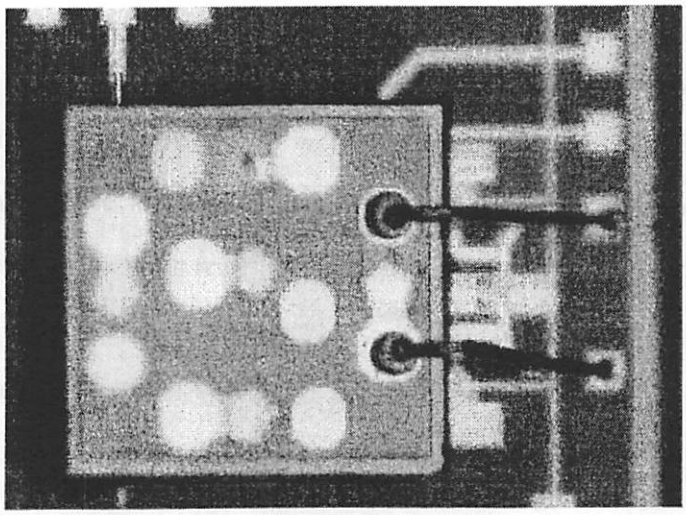


Figure 2.15: ISM implementation of differential oscillator

The CMOS chip is shown underneath the BAW chip. The resonator chip was designed with five resonators. The four perimeter resonators are spaced in frequency across the ISM band. The resonator die (1mm x 1mm) was assembled on top of the CMOS die with non-conductive epoxy. Wire-bonding provided the electrical connectivity between the two chips. This experimental assembly methodology worked well and successfully de-coupled the CMOS/FBAR assembly and the CMOS/board assembly.

The oscillator was biased to 200μW per leg for stable startup (400μW total). This relatively high bias current is due to the quadratic relationship of bias current to the operation frequency, which predicts a 1.6x increase in startup transconductance. In addition, due to the experimental nature of the ISM-band resonators, high variation in resonator motional resistances

2.4 Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator

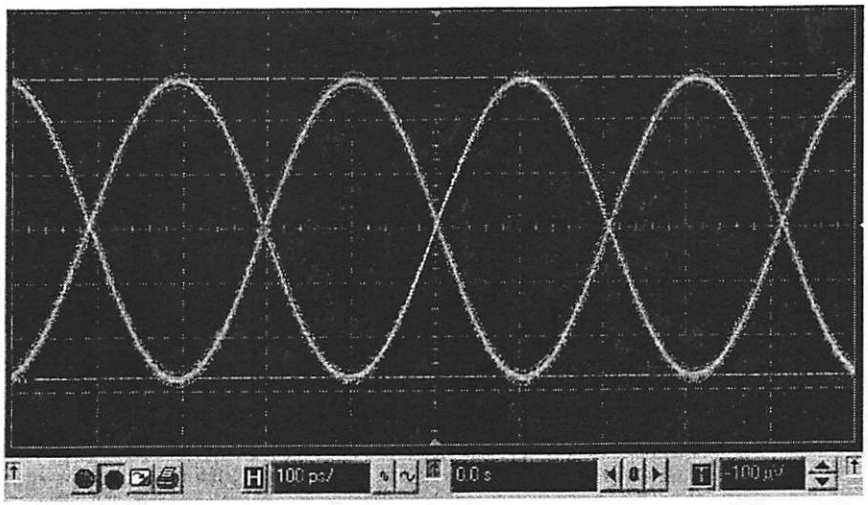


Figure 2.16: ISM differential oscillator transient output

were expected. Figure 2.16 shows the steady-state transient oscillator output. Oscillation occurred at 2.43GHz as expected. The oscillator exhibited a clean spectrum and good amplitude matching. The phase-noise of the oscillator was measured with an *Agilent E5052A* Signal Source Analyzer over four bias point settings (400μA, 500μA, 600μA, 700μA). See Figure 2.17. As expected, the close-in phase noise and noise floor decrease as the oscillator loop power increases. At a bias current of 400μA, the oscillator exhibits a phase noise of approximately $-113\frac{dBc}{Hz}$ at 100kHz offset. This is approximately 7dB higher than the previous 1.9GHz version of the oscillator, indicating a reduced resonator quality factor. The inferred quality factor of the resonator from these phase noise measurements is approximately 200.

This proof-of-concept demonstrates the practical application of MEMS/CMOS

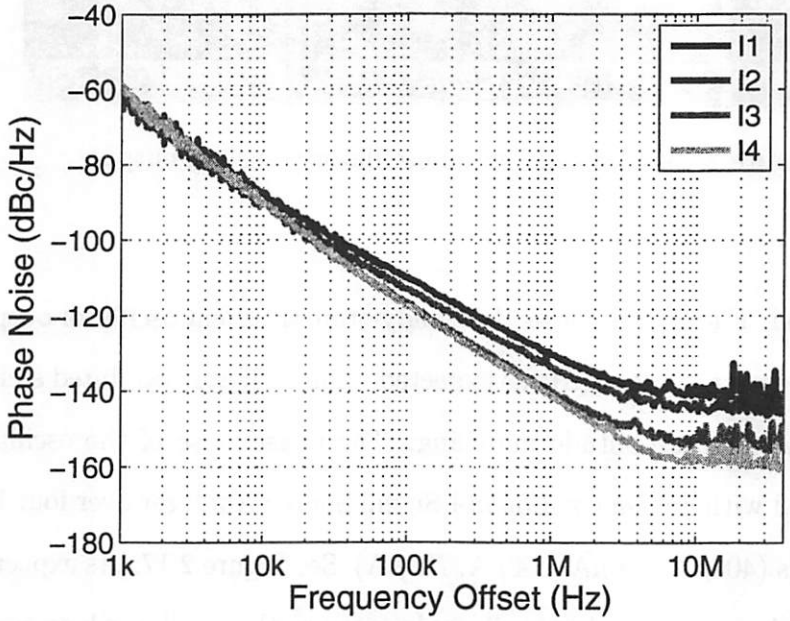


Figure 2.17: ISM differential oscillator phase noise

co-design techniques at higher frequency bands.

2.5 System Proof-of-Concept: Energy Scavenging Transmit Beacon

The previous section confirmed the design philosophies involved in co-designing BAW resonators and CMOS circuitry at RF frequencies. This section seeks similar confirmation of the system-level philosophies: *Can $1cm^3$ energy scavengers realistically and robustly power GHz-range RF circuitry?* The ultimate goal of this work, as reported in [25] was to develop a completely self-powered wireless node.[3] The two most applicable energy scavenging technologies are solar power and vibration-based power, due to the large potential application space of these technologies. Photovoltaic solar cells are a mature technology, and a solar cell based power source may be implemented using commercial off-the-shelf technology. In addition, the technique of utilizing low-level vibrations as a power source was also investigated.

This section reports a 1.9GHz transmit beacon that is successfully operational using solar and vibrational power sources. The main components of the design are the energy scavenging devices, the powertrain, the local oscillator, the power amplifier, and the antenna. One main goal was to maximize the efficiency of the conversion from solar and vibrational power to

[3]The work in this section was in collaboration with S. Roundy, Y.H. Chee, and P. Wright

transmitted RF power. The power circuitry converts the scavenged energy into a stable supply voltage for the RF circuitry. This process entails converting a high impedance, unstable supply into a stable, low impedance 1.2V supply. A 10μF storage capacitor functions as an energy reservoir. When the capacitor charges to a pre-specified energy level, the supply rails to the RF circuitry are activated and energy is consumed. Because the transmitter dissipates power faster than the rate at which the piezoelectric generator or solar cell can produce it[4], the voltage across the storage capacitor falls when the radio is on. Once the energy has been depleted to a level specified by a "Shutdown control" block, the supply rails are disabled and the capacitor is recharged.

The choice of energy storage mechanism involves a tradeoff between energy density and reliability. Batteries have far higher energy density than do capacitors. For example, rechargeable lithium ion batteries have an energy density of roughly 1000 J/cm^3. Ceramic capacitors have an energy density on the order of 1 to 10 J/cm^3. However, most lithium ion batteries are limited to 500 to 1000 recharge cycles and have a finite shelf life. Furthermore, the life of the battery would suffer in the proposed application because the batteries are kept charged with a trickle of current rather than undergoing deep discharge. Capacitors, on the other hand, have an almost infinite lifetime and are simpler to charge. Because wireless sensor nodes do not require substantial energy storage, and because lifetime of the node is a primary

[4]Except in direct sunlight

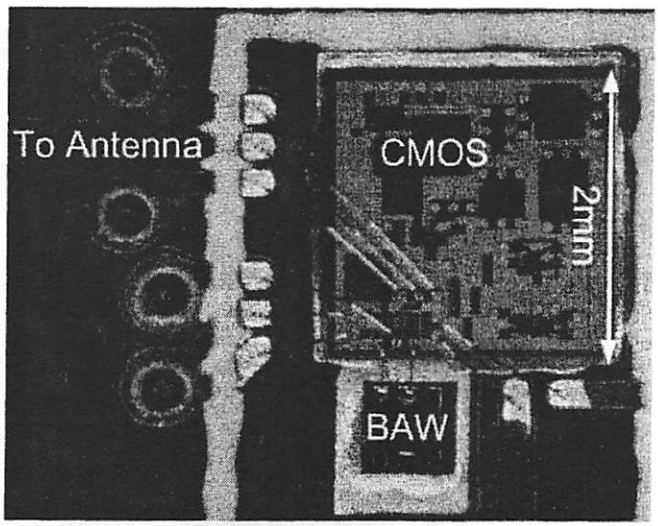


Figure 2.18: RF Transmitter COB implementation

concern, a capacitor was used.

Although a linear regulator would result in a lower total efficiency in the current design scenario, a linear regulator was chosen because of its ability for a higher level of integration and increased simplicity[5]. The transmitter was designed using the same CMOS/MEMS co-design philosophies described earlier in this chapter. A photo of the transmitter is shown in Figure 2.18. The entire transmit area consumes less than $20mm^2$ of board space. The oscillator provides a 100mV signal to the integrated power amplifier, which provides a 0dBm signal to the chip antenna. An output power of -1.5dBm was measured in close proximity to the chip antenna. The completed $(2.4x3.9)cm^2$ transmit beacon implementation is shown in Figure 2.19. The powertrain,

[5]No external filtering inductors or capacitors is needed, in contrast to switching regulators

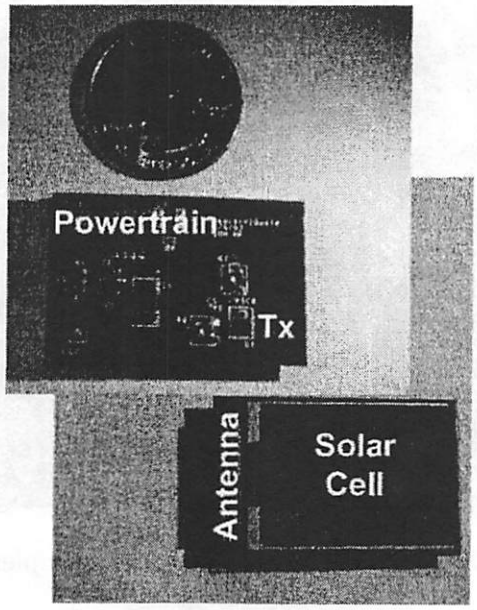


Figure 2.19: Transmit beacon implementation

photovoltaic solar cell, transmitter, and 1.9GHz chip antenna are clearly visible. All circuitry is placed on the back of the board, allowing the front to be utilized for solar collection and RF emission. Although a commercial, off-the-shelf voltage regulator was used, a custom integrated circuit could provide higher efficiency and a much smaller board footprint[6]. A custom piezoelectric bender was also designed[7] to power the beacon. The bender exhibits a resonant frequency of approximately 200Hz and a quality factor of about 20. Thus, the output power drops off rapidly as the stimulus frequency drifts from the bender resonant frequency. Although not shown, the transmit

[6]This is a subject of current research
[7]Designed by Shad Roundy, U.C. Berkeley [2]

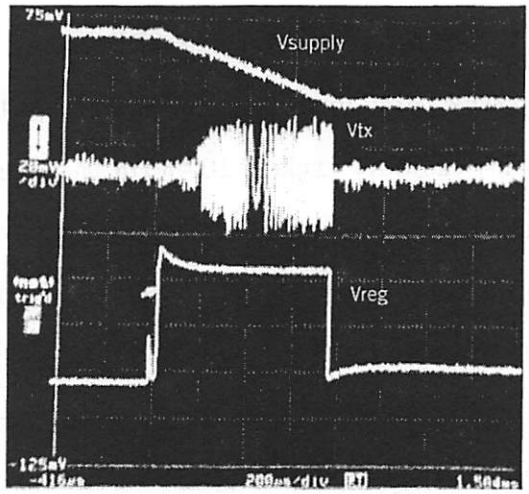


Figure 2.20: RF transmit beacon under low light conditions

beacon was successfully powered by this bender, demonstrating that hybrid energy scavenging is a viable option for wireless sensor networks.

See Figure 2.20 for the measured beacon voltage levels under low lighting conditions. V_{supply} is the voltage on the storage capacitor. Under low solar input conditions, this voltage slowly charges to a pre-defined level. At that voltage, the voltage regulator is enabled and V_{reg} rises to a stable 1.2V, powering the RF transmitter. The RF blocks are then enabled, beginning transmission. During this stage, V_{supply} decreases as energy is drawn from the storage capacitor. When a sufficiently low level of capacitor energy is sensed, the voltage regulator is disabled and the RF transmission stops. The main figure of merit of this system is the transmit duty cycle under various environmental conditions.

The achievable transmit duty cycle varies dramatically over various light-

ing conditions. In the presence of low indoor light, the duty cycle is approximately 0.4% (400bps throughput assuming a 100kbps transmitter datarate). In direct sunlight, the duty cycle is 100% (in that condition, the solar cell is supplying more power than necessary for constant transmitter operation). For a $5.7m/s^2$ vibration level (about $0.58G$), the transmitter duty cycle is about 2.6%, corresponding to a throughput of 2.6kbps. The transmit beacon operates indefinitely from ambient energy, and has been operating reliably for over two years as of March 2005.

Chapter 3

Two Channel BAW-Based Transceiver

This Chapter describes the implementation of a low power, fully integrated, two-channel transceiver that builds off the principles that were developed in Chapter 2. For example, Chapter 2 discussed how RF MEMS technology and weak inversion standard CMOS may be used to reduce the power consumption and increase the integration of low power RF components. Two proof-of-concept designs were described: a low power oscillator and an entire energy scavenging transmit beacon. Building on this knowledge, an entire transceiver based on these concepts was designed. The following goals set the landscape for the decisions made during the design of the transceiver.

- Design a transceiver that leverages the benefits of state-of-the-art RF MEMS technology *and* incorporates a vision of future technology scaling of RF MEMS.

- The transceiver should be robust against BAW process variations.

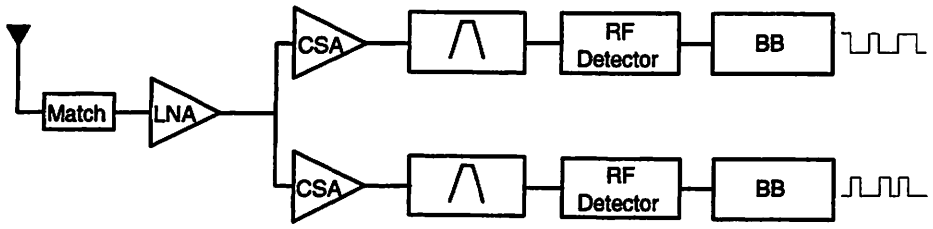


Figure 3.1: Block diagram of the two-channel transceiver

- The effort should result in a working ultra-low power transceiver that can be used in peer-to-peer wireless sensor networks and represents a reduction in power consumption over the current state-of-the-art.

This chapter describes how these goals were met, resulting in an ultra-low power two-channel transceiver [26].

3.1 Architecture

The receiver block diagram is shown in Figure 3.1. The two-channel tuned radio frequency (TRF) architecture was chosen to demonstrate the effectiveness of RF MEMS resonators in low power transceivers. The antenna feeds a 50Ω impedance presented by the LNA. The LNA drives a tuned LC load absorbing the capacitive input of two channel select amplifiers (CSAs). Each CSA incorporates an FBAR resonator, which performs receiver channel selection. Although two channels were used in this implementation, the architecture is scalable to larger numbers of channels. In the future, advanced RF MEMS technology will allow lithographically defined resonant frequen-

cies and the integration of MEMS onto CMOS wafers. At that point, this architecture could accommodate multiple channels with widely varying frequencies, limited only by the bandwidth of the LNA[1]. The CSAs drive an envelope detector, which acts as a self-mixer to perform signal downconversion. Baseband buffers are included to drive test instrumentation. Because the frequency stabilization is performed entirely by the MEMS resonators, no quartz crystals were used in this receiver architecture. The absence of a phase-locked loop (PLL) ensures a much faster receiver start-up time than that required by a traditional radio.

The two-channel embodiment displays flexibility in terms of modulation schemes: the receiver can detect two unique on-off keyed (OOK) data streams at two carrier frequencies, or it can detect a frequency shift keyed (FSK) modulation. For dense wireless sensor networks, it is anticipated that two separate OOK channels will be used, with one reserved for beaconing. Changing between these two modulation schemes can be accomplished with no receiver modifications, and can be performed dynamically in either the analog or digital baseband detection circuitry.

3.2 LNA Design

The low noise amplifier (LNA)[2] was designed to serve three main purposes:

- Present a 50Ω impedance match to the antenna.

[1] Approximately 200MHz
[2] Designed by Richard Lu, EECS Dept., U.C. Berkeley

- Absorb the capacitive load of N channel select amplifiers. For a scalable architecture, it is important that the addition of each subsequent channel results in little (or no) performance degradation of the amplifier.

- Achieve high RF gain to overcome the large noise of the self-mixing process.

A single-ended, cascoded, tuned input/output LNA was chosen to meet these requirements with a minimum amount of power consumption. See Figure 3.2 for a front-end schematic of the receiver. The LNA comprises transistors M_{LNA1} and M_{LNA2}. Unlike typical CMOS LNAs, this design eliminates the source degeneration inductor by matching to the non-quasi static (NQS) and parasitic device resistance of transistor M_{LNA1}. This design decision allows a higher RF gain and smaller implementation area at the cost of reduced linearity performance. Moderate inversion operation of M_{LNA1} allowed a reasonable inductor value of L_{gate}, providing the possibility of implementing this inductor on-chip. As the f_T of CMOS processes continues to scale, the size of this inductor will increase to prohibitively large values. Operation in weak inversion is a useful way to control this trend. Although the f_T is degraded, the performance penalty is partially mitigated by the increase in transconductance efficiency. The output tank consists of L_{load}, the channel select amplifier capacitance, and a small explicit capacitor to achieve the correct resonant frequency.

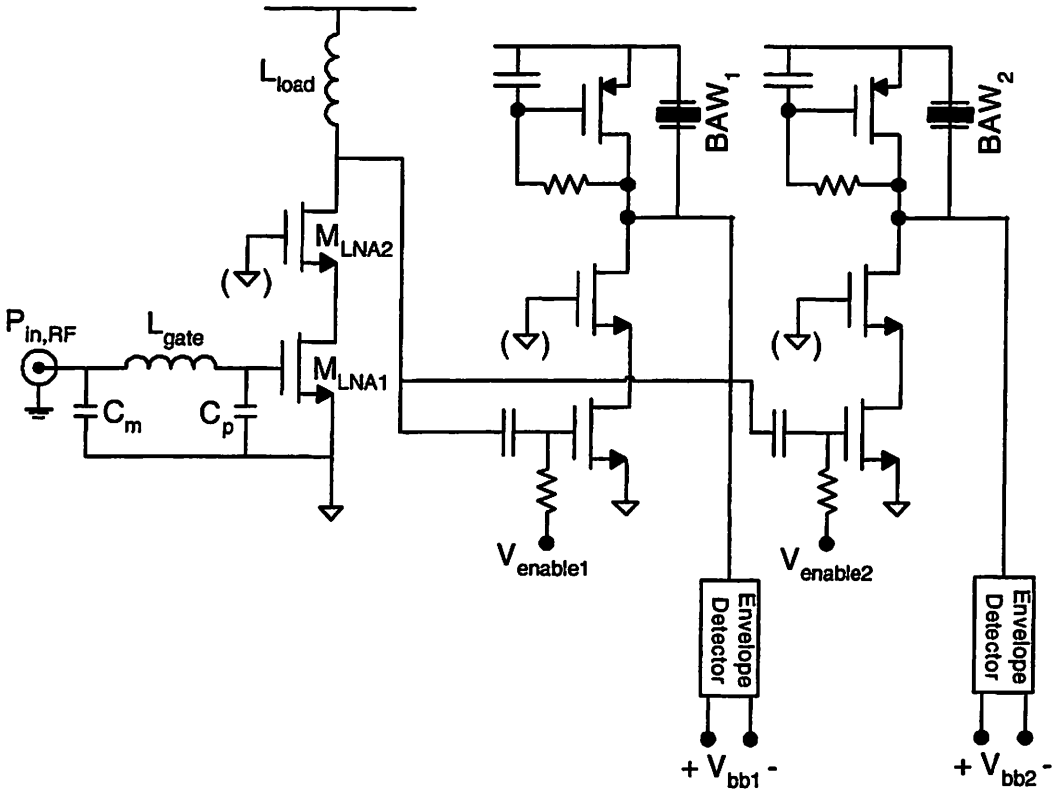


Figure 3.2: Simplified receiver front-end schematic

A standalone LNA test structure was implemented for performance verification. The output was matched through a passive capacitance transformer for testing purposes. Figure 3.3 shows the measured input matching and forward gain of the amplifier when biased at 1.4mA. The measurement shows good input matching and correct output tank frequency. The S_{21} of the standalone LNA at resonance is approximately 13dB, corresponding to an in-situ[3] voltage gain of 22dB. The amplifier noise figure, measured with an

[3]Meaning in the receiver, loaded with a high impedance LC tank

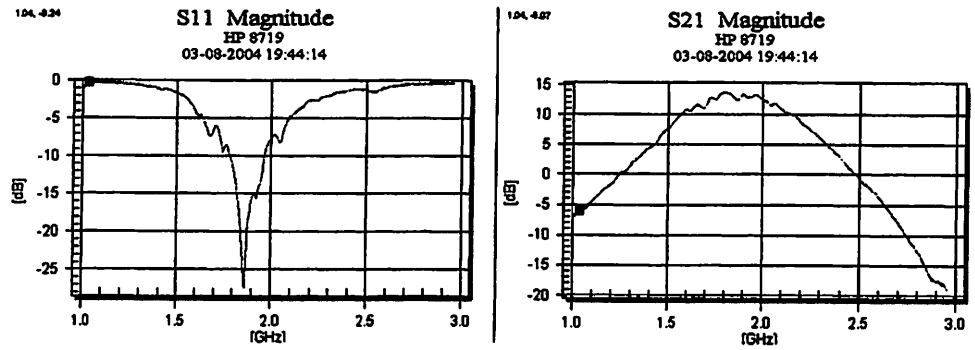


Figure 3.3: Measured S-parameters of the LNA test structure

HP 8970B Noise Figure Meter, is 2.5dB at 1.9GHz. See [27] for a thorough discussion of the design methodology and performance of the LNA.

3.3 CSA Analysis and Design

The channel select amplifier performs two main functions: it provides high RF gain in order to overcome the high noise figure of the detector. In addition, it interfaces the electrical signal with the acoustic resonator to perform high Q filtering of the signal. The amplifier must exhibit high RF gain with low power consumption while limiting the extent to which the resonator is de-tuned. Three separate RF amplifiers were implemented on each chip: one standalone test structure (50Ω input/output) and two integrated amplifiers; one for each of the two radio channels. This section discusses the design of the active choke inductor, the standalone amplifier, and the integrated amplifier.

3.3.1 Active Inductor

The BAW resonator, used in the parallel resonance mode, performs high Q filtering by presenting a high impedance for a very narrow bandwidth about its parallel resonant frequency. However, for off-resonance frequencies, the resonator presents a $\frac{1}{j\omega C}$ impedance[4]. Thus, at low frequencies (LF), the resonator presents a high impedance to the active circuitry. To provide bias current (a low DC impedance) to the active devices and reduce LF gain, a low load impedance at LF is desirable. However, at the signal frequency, the impedance must be high to avoid de-tuning the BAW resonator. Thus, an inductive structure is a natural candidate. To avoid substantial de-tuning of the BAW resonator at 1.9GHz, the bias device must present an impedance greater than 1500Ω. This specification corresponds to an inductance of 125nH, which is marginally reasonable to fabricate on-chip. Even if possible, it would resonate with the parallel plates of the BAW at (2pF) at 318MHz, adding an out-of-band response to the receiver input. It would also consume more than 10,000μm^2 of silicon area. The use of an active inductor, however, allows the realization of very high inductance values and easy control over the inductor Q. For this application, a large, low Q inductance is needed to provide high RF impedance with a low frequency, low Q parasitic resonance.

An active inductor topology is proposed for this application. See the

[4]Mechanically, off-resonance, the resonator is simply two parallel plates filled with an AlN insulator with relative permittivity $k = 9$

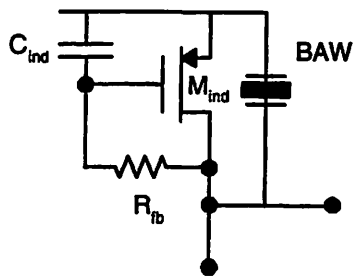


Figure 3.4: Schematic of active choke inductor structure

inductor schematic in Figure 3.4. At low frequencies, the inductor impedance is $\frac{1}{g_{m,ind}}$. At high frequencies, the impedance is $R_{o,Mind}//R_{fb}$. It can be shown that the effective inductance and Q of the structure are given by Equations 3.1 and 3.2, respectively.

$$L = \frac{R_{fb}C_{ind}}{g_m} \tag{3.1}$$

$$Q = \omega R_{fb}C_{ind} \tag{3.2}$$

Table 3.1 shows the design values for the active inductor that will be used in subsequent calculations. As shown in the table, the active inductor achieves LF and HF impedances of approximately 360Ω and 6kΩ, respectively. The parasitic resonance of the active inductor and the resonator plate capacitance occurs at 34MHz with a Q of 6.4. Cascaded with the LNA presented in Section 3.2, the antenna-to-detector response in the 34MHz band will be negligible. This would not be the case with a 100nH on-chip choke inductor. Active inductors are routinely believed to have a prohibitively high

Table 3.1: Active inductor design values

Component	Design Value
$R_{p,resonator}$	1.4kΩ
$I_{bias,CSA}$	500μA
$g_{m,ind}$	2.8mS
$\frac{g_m}{I_d}$	5.6
C_{ind}	5pF
R_{fb}	6kΩ
L	8.5μH
C_{res}	2pF
$f_{res,calc}$	38MHz
$f_{res,sim}$	34MHz
Q_{34MHz}	6.4

noise figure. However, in this application, when used as a choke inductor, it will be shown that the excess noise that accompanies the structure is sufficiently low. The noise performance of this structure will now be analyzed. As shown in Equation 3.3, the noise is first calculated considering only the resonator[5].

$$\overline{v_0^2} = 4KTR_{p,resonator} = 22.4\frac{(nV)^2}{\sqrt{Hz}} \tag{3.3}$$

$$Simulation: 24\frac{(nV)^2}{\sqrt{Hz}}$$

As shown in Equation 3.4, the resonator is de-tuned by the accompanying circuitry. Additional components also modify the noise characteristics. Finally,

[5]Corresponding to a fictitious circuit providing ideal, noiseless current sourcing and common-mode feedback

equation 3.6 includes the transistor noise sources.

$$R_{p,effective} = R_{p,resonator}//R_o//R_{fb} = 1k\Omega \tag{3.4}$$

$$\overline{v_0^2} = 4KTR_{p,effective} = 16\frac{(nV)^2}{\sqrt{Hz}} \tag{3.5}$$

$$\overline{v_0^2} = \left[4KT\frac{1}{R_{p,effective}} + 4KT\gamma g_m\right]R_{p,effective}^2 = 45\frac{(nV)^2}{\sqrt{Hz}} \tag{3.6}$$

$$Simulation: 39.3\frac{(nV)^2}{\sqrt{Hz}}$$

The load noise factor, (β), is given by Equation 3.7.

$$\beta = \frac{\left[4KT\frac{1}{R_{p,effective}} + 4KT\gamma g_m\right]R_{p,effective}^2}{4KTR_{p,effective}} = 1 + \gamma g_m R_{p,effective} \tag{3.7}$$

$$\beta = 2.86$$

Because the load contributes little noise to the total noise figure, the excess noise factor is acceptable for this application.

3.3.2 Standalone RF Amplifier

The RF amplifier consists of an NMOS cascode transconductance stage and a tuned load. A cascode transconductor structure is used to increase reverse isolation, ensuring amplifier stability. The tuned load consists of an FBAR resonator to perform channel selection and the inductive PMOS-R-C structure described in Section 3.3.1, which stabilizes the low-frequency bias point

of the amplifier. The loaded quality factor of the tuned load is approximately 600, yielding an RF bandwidth of 3MHz.

A standalone RF amplifier was designed and implemented to verify the performance of this structure. Due to RF testing considerations, the structure had to be modified slightly from the in-situ receiver implementation. Figure 3.5 for the schematic of the standalone RF amplifier. Transistor M_1 is operated in weak inversion for two main reasons: first, the degradation in f_T is not crucial because the gate capacitance of the integrated version is tuned out by the LNA. Secondly, the voltage gain of the stage is proportional to the transconductance of M_1, and $\frac{g_m}{I_d}$ is maximized in lower levels of inversion. In this implementation, a $\frac{g_m}{I_d}$ of approximately 20 is achieved. The gate of cascode device M_2 is self-biased, and the layout of M_1 and M_2 is optimized for low drain and interconnect parasitic capacitance.

The input is terminated with an on-chip 50Ω resistor. This allows accurate RF characterization by minimizing the reflections coming from the 50Ω instrumentation transmission lines. An on-chip buffer is used to present a 50Ω output impedance, which is accomplished by maintaining the g_m of M_{2buf} at 20mS. The noise figure of the standalone amplifier can be calculated as follows:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}}{S_{out}}\frac{N_{out}}{N_{in}} = \frac{1}{A_v^2}\frac{\overline{v_o^2}}{4KTR_s} \tag{3.8}$$

Equations 3.9 and 3.10 show the voltage gain and total output noise, respec-

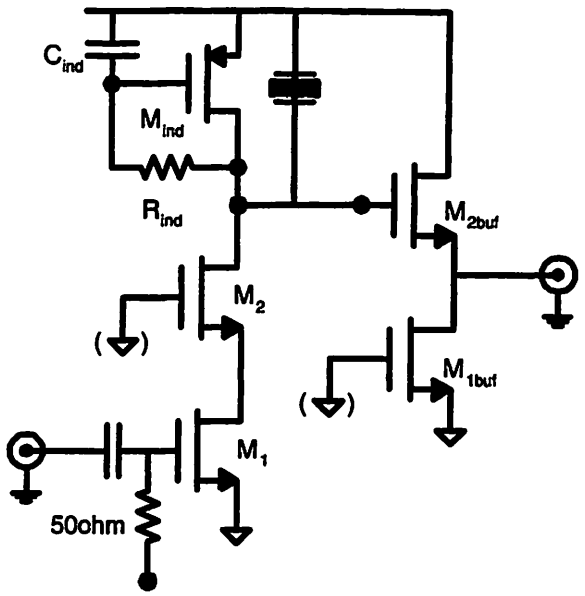


Figure 3.5: Standalone RF amplifier schematic

tively.

$$A_v = \frac{R_{in}}{R_s + R_{in}} g_{m1} R_{p,effective} \tag{3.9}$$

$$\overline{v_o^2} = 4\left(\frac{4KTR_s}{2}\right)A_v^2 + (4KT\gamma g_m)R_{p,effective}^2 + \beta 4KTR_{p,effective} \tag{3.10}$$

Thus, the noise figure is given as Equation 3.11

$$F = \frac{1}{\left(\frac{R_{in}}{R_s+R_{in}} g_{m1} R_{p,effective}\right)^2} \frac{4\left(\frac{4KTR_s}{2}\right)A_v^2 + (4KT\gamma g_m)R_{p,effective}^2 + \beta 4KTR_{p,effective}}{4KTR_s} \tag{3.11}$$

which simplifies to Equation 3.12.

$$F = 2 + \frac{4\gamma}{g_m R_s} + \frac{R_{p,effective}\beta}{R_s A_v^2}\Big|_{R_s=R_{in}} \tag{3.12}$$

$$F = 11.7dB$$

Table 3.2 shows the breakdown of the noise in the various amplifier components. A majority of the noise is due to the main transconductor. This is

Table 3.2: Breakdown of RF amplifier noise sources

Noise Source	Noise Contribution
Transistor M_1	60.8%
Source Resistance	21.0%
Active Resonator Load	18.2%

due to the relatively high noise figure of the standalone, 50Ω referenced test structure. Less than 20% of the noise contribution is due to the active choke inductor. The simulated S_{21} and NF are shown in Figure 3.6.

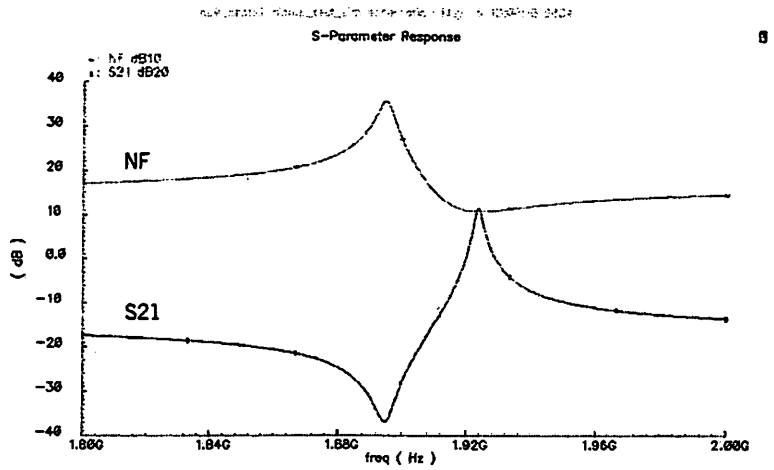


Figure 3.6: Simulated S_{21} and NF of the RF Amplifier

The series and parallel resonances of the BAW resonator are clearly visible in Figure 3.6. At the parallel resonance the simulated noise figure[6] is 10.8dB and the simulated S_{21} is 11.5dB. The implemented standalone amplifier is shown in Figure 3.7. Clearly visible are the three wirebonds connecting the CMOS chip to the resonant structure in a ground-signal-ground (GSG) configuration. The amplifier core was biased at the design value of 500μA. The measured S-parameters of the standalone amplifier are shown in Figure 3.8. Because the standalone test structure is terminated by an on-chip resistor at the input and a on-chip buffer at the output, the S_{11} and S_{22} shows matching $<$ -10dB. The S_{21} measurement shows good bandwidth agreement with the simulated and calculated values. The measured gain at parallel resonance is

[6]Including the loss from the output buffer. This corresponds to an in-situ voltage gain of 17.5dB.

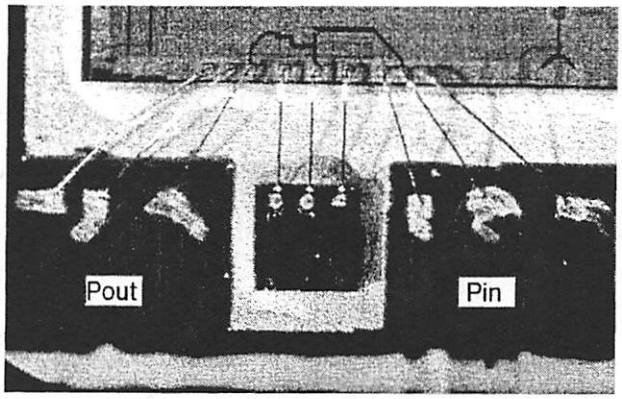


Figure 3.7: Photograph of standalone RF amplifier

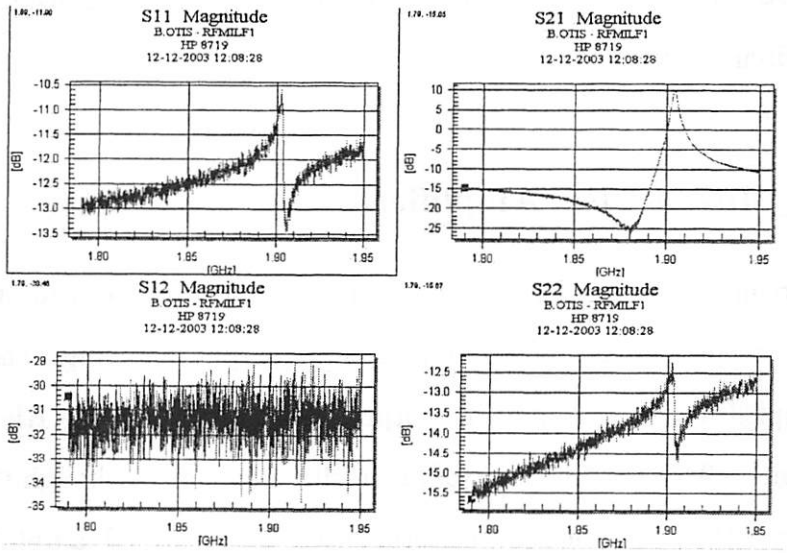


Figure 3.8: Measured S-Parameters of the RF Amplifier

10dB. The 2dB discrepancy can be attributed to variations in resonator R_p and board trace losses. The noise figure measurement was performed with an *HP 8970B* Noise Figure Meter and was duplicated using the "Spectrum Analyzer Method" with an *Agilent E4445A PSA*. A summary of the calculated, simulated, and measured parameters is shown in Table 3.3.

Table 3.3: Table of RF amplifier parameters

	NF	S_{21}
Calculated	11.7dB	17.7dB
Simulated	10.8dB	17.6dB
Measured	11.4dB	16.0dB

Close matching was observed between all calculated, simulated, and measured circuit parameters.

3.3.3 In-Situ RF Amplifier

The circuit design of the in-situ amplifier is the same as the standalone version except there is no need for 50Ω input/output matching. The input is AC coupled to the LNA, and the output is DC coupled to the RF detector. See Figure 3.9 for the schematic of the in-situ amplifier. Although the circuit topology is the same, the noise performance of the in-situ RF amplifier differs greatly from the standalone RF amplifier, due to the significantly higher source resistance of approximately 500Ω. This manifests itself as a much lower effective noise figure. See Equation 3.13 for the output noise power of

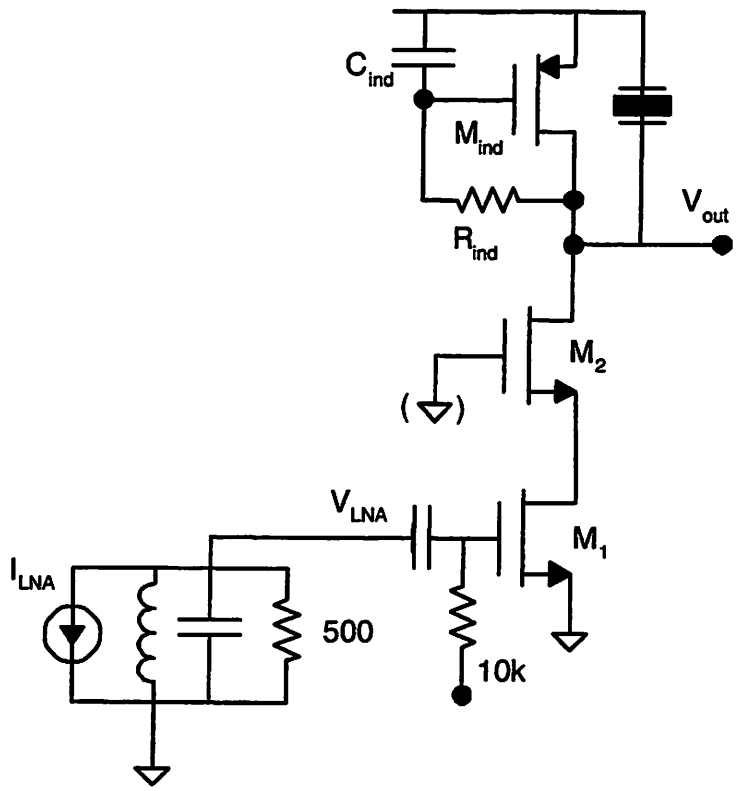


Figure 3.9: Schematic of in-situ RF amplifier

the amplifier.

$$\overline{v_o^2} = 4KTR_sA_v^2 + (4KT\gamma g_m)R_{p,effective}^2 + 4KTR_{p,effective}\beta \tag{3.13}$$

The noise figure is thus:

$$F = \frac{1}{(g_{m1}R_{p,effective})^2}\frac{4KTR_sA_v^2 + (4KT\gamma g_m)R_{p,effective}^2 + 4KTR_{p,effective}\beta}{4KTR_s} \tag{3.14}$$

Which reduces to:

$$F = 1 + \frac{4\gamma}{g_mR_s} + \frac{R_{p,effective}\beta}{R_sA_v^2} \tag{3.15}$$

Notice that the first term in Equation 3.14 is unity, not two as in Equation 3.12. This 6dB noise penalty is not present in the in-situ amplifier because the input is not resistively terminated. Additionally, because R_s is 10x higher than before, the effective noise figure of the amplifier is much lower.

$$F = 1.15dB$$

Table 3.4 shows the noise breakdown for the two amplifier topologies.

Table 3.4: Breakdown of the standalone and in-situ amplifier noise sources

Noise Source	Standalone	In-Situ
Transistor M_1	60.8%	17.8%
Source Resistance	21.0%	76.7%
Active Resonator Load	18.2%	5.5%

The in-situ amplifier's main transconductor contributes less than 20% of

the total output noise, compared to over 60% from the standalone amplifier. The active resonator load of the in-situ amplifier contributes negligible noise to the output. Thus, integrated into the receive chain, the RF amplifier contributes negligible noise to the receiver noise figure.

3.4 RF Detector Analysis and Design

The RF detector performs a signal level detection on each channel of the receiver. Rectification, or self-mixing, is achieved through the non-linear low-pass filtering of the RF input signal. The self-mixing is achieved through MOSFETs biased in the deep-subthreshold region to increase their non-linearity. The simplified schematic of the detector is shown in Figure 3.11. This circuit, which was previously used in bipolar applications [28], is well suited to subthreshold CMOS implementations as well. Transistors M_1 and M_2 are sized at $\frac{10\mu m}{1\mu m}$ and biased at $\frac{10nA}{\mu m}$ (IC=0.015), yielding a $\frac{g_m}{I_d}$ of approximately 30. The detector exhibits an intrinsic low-pass filter with a cutoff frequency set to 300kHz, which attenuates all fundamental tones passing through the receive chain. Although the receiver front-end is single-ended to reduce power consumption, it is desirable to have a fully-differential baseband for increased supply rejection and dynamic range. To perform a single-ended to pseudo-differential conversion, a replica envelope detector with feedforward offset cancellation was implemented. The bandwidth of the offset cancellation filter is 1.5MHz. The current consumption of each detector, includ-

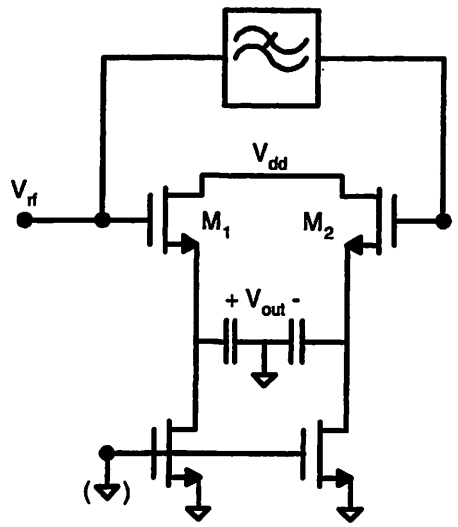


Figure 3.10: Schematic of the RF Detector

ing replica circuitry, is 200nA. Additionally, the efficiency of the circuit can be increased if transistor M_1 and its replica are designed in a DTMOS configuration (gate connected to body contact) [29]. This configuration decreases the subthreshold slope to a value approaching 60mV/decade, increasing the conversion gain of the detector.

A standalone envelope detector was designed and fabricated to verify its performance and conversion gain. Figure ?? shows the measured transfer function of multiple envelope detectors. These results show the decrease in conversion gain that occurs at low input signal levels. This creates a thresholding effect, where decreasing RF input levels cause a dramatic decrease in the noise figure of the detector. This threshold sets the noise floor of the tuned RF receiver.

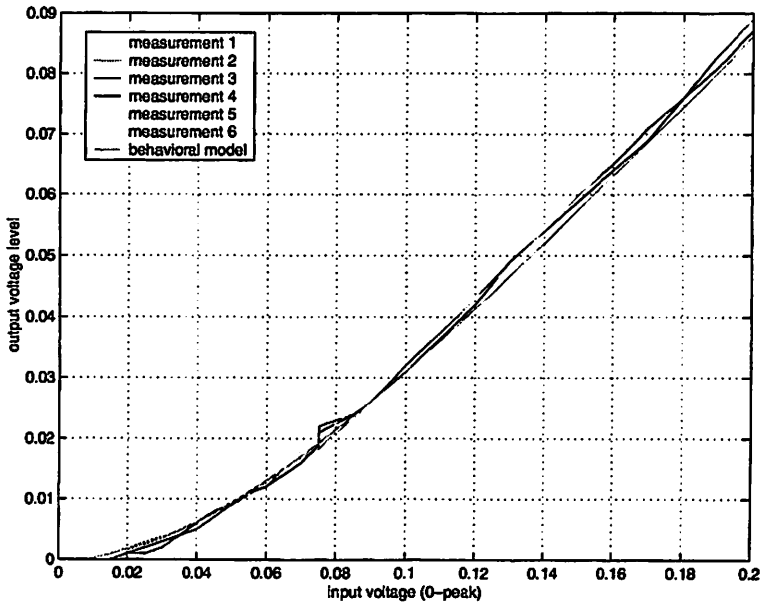


Figure 3.11: Measured conversion gain of the envelope detector

Each channel in the receive chain also contains a low-power buffer to drive off-chip instrumentation[7]. The buffers are capable of driving a 20pF/2kΩ off-chip load while consuming 50μA. On-chip threshold-referenced bias circuits provide a moderate level of power-supply independence.

3.5 Transmitter Architecture and Design

In a typical sensor network, the transmitter sends out sporadic bursts of short data packets to neighboring sensor nodes (<10m). As shown in Figure 1.2, for a receiver sensitivity of -70dBm and a healthy margin for indoor

[7]Designed by Nathan M. Pletcher, EECS Dept., U.C. Berkeley

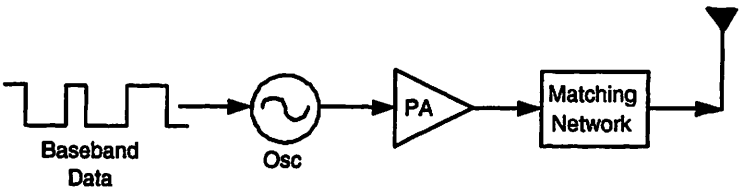


Figure 3.12: Block diagram of the transmitter

multi-path fading conditions, a transmit power of approximately 0dBm is required. The transmitter must exhibit fast turn-on time and high efficiency. The transmitter architecture shown in Figure 3.12 is well-suited for these requirements.

The architecture utilized direct modulation of the BAW-based oscillator. The oscillator is similar to the one presented in Section 2.3. Migration from the 0.18μm to the 0.13μm technology node, however, required a re-optimization of the transistor sizing. The start-up time of the oscillator is approximately 1.5μs, allowing direct modulation of the transmitter to datarates over 150kbps. Direct modulation eliminates power hungry mixers and PLLs. Multiple channels can be implemented by tuning the oscillation frequency or by adding oscillators/transmit chains in parallel. For this implementation, two separate BAW resonators were used, so two discrete Tx chains were implemented. The power amplifier (PA) is a standard class-AB cascoded topology[8]. The high PA drain impedance is matched to the 50Ω antenna through a fully integrated, high Q capacitive transformer. See

[8]Designed by Yuen-Hui Chee, EECS Dept., U.C. Berkeley

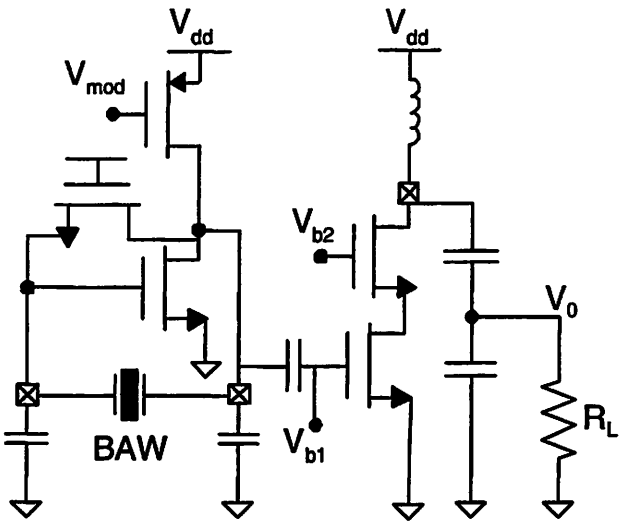


Figure 3.13: OOK Transmitter Schematic

Figure 3.13 for a simplified transmitter schematic.

3.6 Experimental Results

3.6.1 Implementation

The transceiver was implemented in a standard 0.13μm CMOS process. The complete transceiver system is shown in Figure 3.14. The chip area is (4x4)mm^2, which is mostly consumed by passive test structures. The actual area consumed by the transceiver is approximately 8mm^2. Chip-on-board (COB) wirebonding was used to interface to the chip. As shown in the system photograph, the four FBAR resonators are bonded directly to the chip using standard COB wirebonding. This technique eliminates board

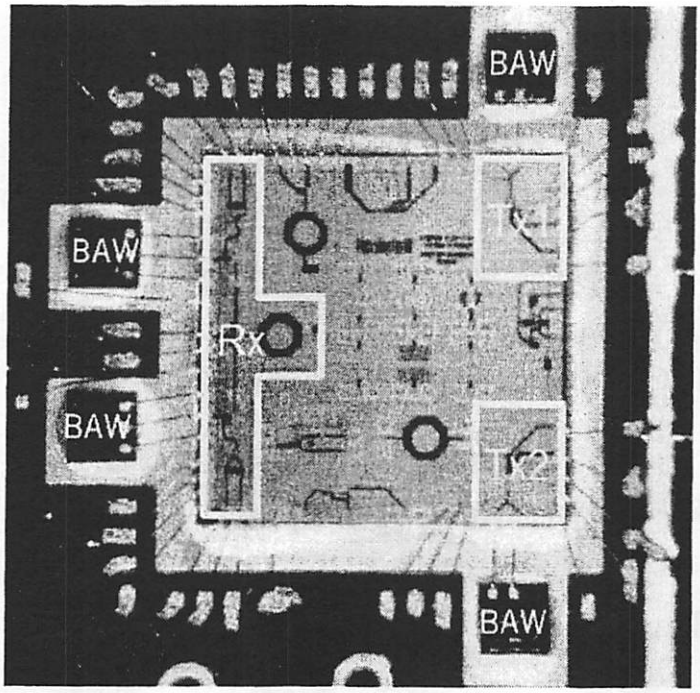


Figure 3.14: Photograph of the transceiver implementation

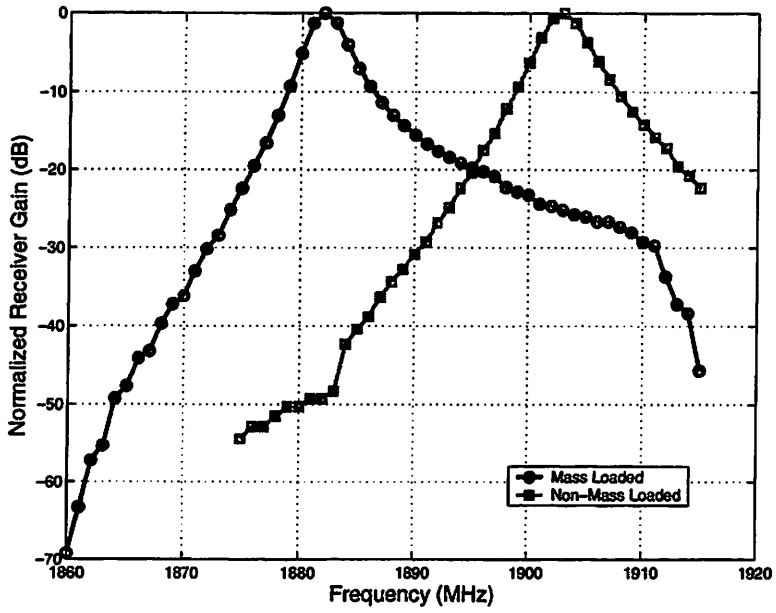


Figure 3.15: Normalized receiver gain of both channels

parasitics on these sensitive nodes and reduces the required board area. The testboard was connected to a single 1.2V supply for testing.

3.6.2 Receiver

The normalized receiver gain of both channels is shown in Figure 3.15. Both receive channels exhibit a 3MHz bandwidth and close gain matching. This implies that, when integrated into the receive chain, the BAW resonators in the channel select amplifiers are not being de-tuned. Receiver sensitivity for a 12dB SNR was measured at -78dBm[9]. The start-up time of the receiver is

[9]Receiver sensitivity was measured with external baseband amplification to overcome the noise of the test equipment

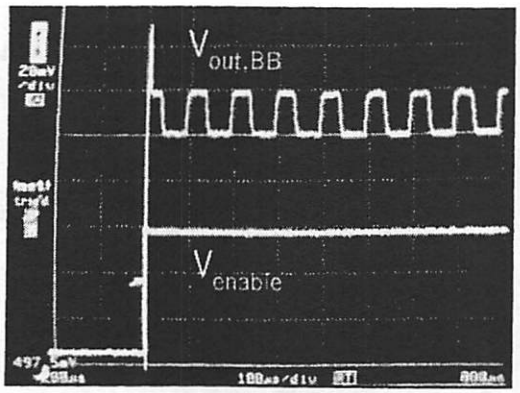


Figure 3.16: Receiver enable-to-data start-up time

crucial in a wireless sensor network application due to the very short packet lenghts. Figure 3.16 shows the receiver start-up transient. The bottom trace is the 0 to V_{dd} enable signal transient, while the top trace is the baseband output in the presence of a 20kbps OOK input signal. The measured start-up time is $10\mu s$, minimizing the overhead associated with heavy duty-cycling. The total receiver current consumption is 3mA from a 1V supply with both channels active. See Figure 3.17 for a component current breakdown of the receiver. Clearly, a majority of the current is consumed by the LNA and channel select amplifiers. With only one receive channel active, the current consumption reduces to 2.3mA.

3.6.3 Transmitter

The peak global transmitter efficiency for the low frequency (LF) and high frequency (HF) channels was measured as 16.5% and 14.7% respectively,

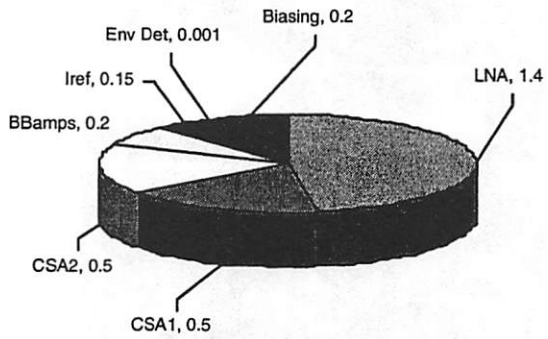


Figure 3.17: Breakdown of the receiver current consumption (mA)

and occurs at an output power of 1.45mW. Higher efficiency is observed for the LF channel due to better alignment between the oscillator resonant tank and the power amplifier output filter. At an output power of 0dBm, the measured second- and third-harmonic distortion ratios (HD2 and HD3) for the LF channel are -38.4dB and -45.3dB below the carrier, respectively. For the HF channel, the measured HD2 and HD3 are -35.0dB and -45.7dB respectively. The start-up time of the transmitter determines the maximum achievable transmitter datarate. Figure 3.18 shows the measured start-up time of the transmitter to be approximately 1.5μs. The transmitter achieved a maximum measured datarate of 160kbps.

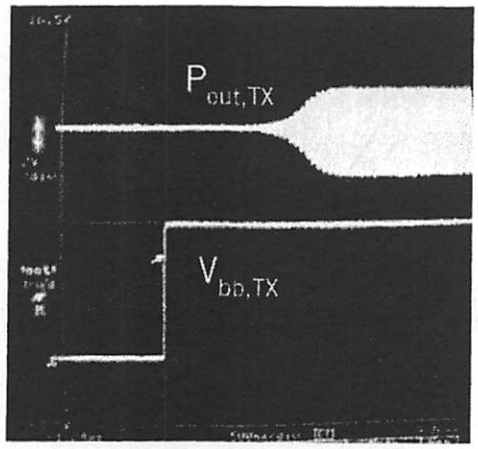


Figure 3.18: Transmitter modulation start-up time

3.7 Conclusions

The goal of this chapter was to explore the feasibility of placing the burden of filtering on a passive RF MEMS component instead of the traditional downconvert-and-filter method. This section described the design, implementation, and testing a low power transceiver using BAW resonators as the tuning elements. The benefits of this architecture are the avoidance of a crystal and PLL on the transmit side and the avoidance of any local oscillator on the receive side. The elimination of the quartz crystal allows the entire transceiver to be fabricated using thin-film techniques. The transceiver was fully functional and a robust 20m indoor wireless link was demonstrated. The architecture described in this chapter provides a modest sensitivity and is tolerant to frequency variations of the BAW resonators.

From Figure 3.17, we learned that a large majority of the power dissipa-

tion occurred in the amplification stages. Recall that a high RF gain was necessary to reduce the noise contribution of the self-mixing RF detectors. This is a problem common to all architectures that avoid traditional downconversion, and represents room for improvement in subsequent implementations. In the next chapter, this issue is addressed by exploring a super-regenerative receiver architecture.

Chapter 4

Super-Regenerative Receiver Design

So far, we have shown that RF MEMS technology can enable new circuit blocks and transceiver architectures. The next step is to push the boundaries and further decrease the size and power consumption of the transceiver. To continue this architecture exploration, a super-regenerative receiver architecture was evaluated. This chapter describes the design, implementation, and testing of a sub-mW BAW-based super-regenerative receiver. First, a brief history of this architecture is given.

4.1 History of the Super-regenerative Receiver

The super-regenerative concept was first introduced by Armstrong in the 1920s [30]. Reasons for its success during the first half of the 20th century included a minimal number of required active devices (vacuum electron tubes), a high RF gain, and the ability to operate at high RF frequencies [1].

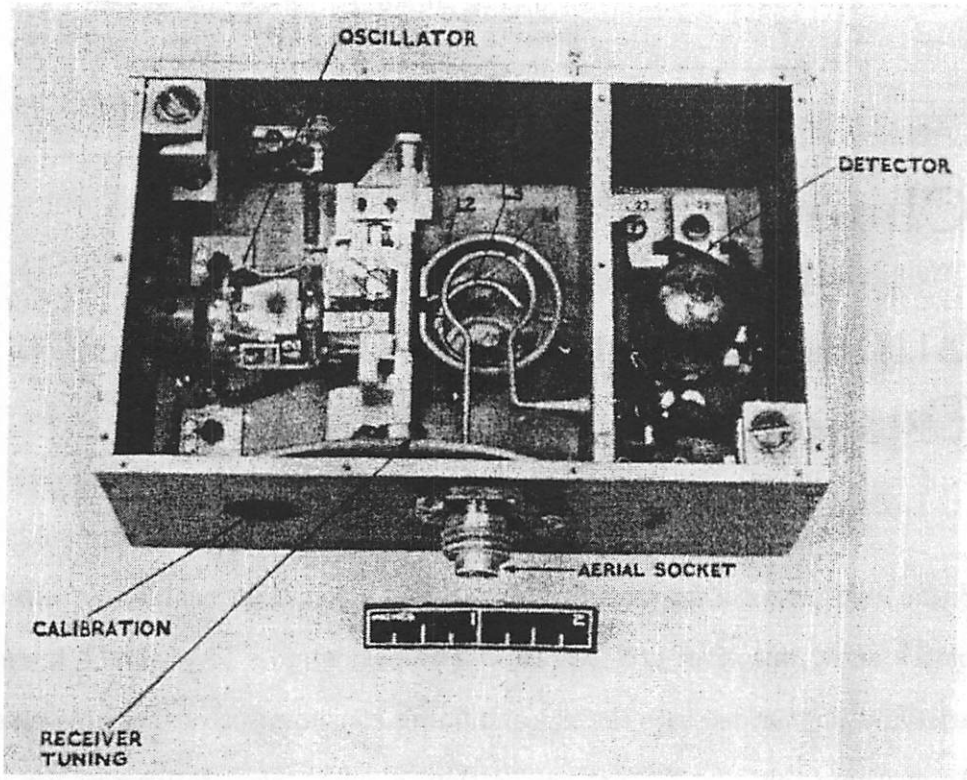


Figure 4.1: Vintage 1940s two-tube super-regenerative detector [1]

Typical RF circuit blocks use transistors biased at f_T values multiple times greater than the carrier frequency. The super-regenerative architecture is attractive because it allows receiver operation above the f_T of the RF devices. See Figure 4.1 for an example of a 1940s super-regenerative receiver [1]. This 500MHz receiver consists of a super-regenerative oscillator, an input coupling transformer, a tunable capacitor, and a detector tube. Manual adjustments are required to fine-tune the oscillator frequency and loop gain. Although the receiver is bulky and requires calibration, the few number of active de-

vices and operation above device f_T is an impressive accomplishment. Antenna re-radiation, low spectral efficiency, distortion of analog modulation, and the advent of inexpensive transistors allowing super-heterodyne architectures rendered the super-regenerative receiver obsolete by the late 1950s. However, in this chapter it is shown that modern RF MEMS, CMOS technology, circuit design techniques, and digital communications solve many of the inherent problems with this architecture, providing very low power and high integration for sensor node applications.

4.2 Motivation

As shown in Chapter 3, the tuned radio frequency architecture utilizes RF MEMS technologies to perform channel selection without the need for mixers or frequency synthesizers. However, a high RF gain is necessary due to the high noise injected by the self-mixing RF detection circuitry. A super-regenerative front-end provides extremely high RF amplification and narrow-band filtering at low bias current levels. As shown in Figure 4.2, the heart of a super-regenerative detector is an RF oscillator with a time-varying loop gain. This block diagram consists of a passive matching network, an isolation amplifier, an amplifier with time-varying gain, and a bandpass positive feedback network forming an oscillator. The isolation amplifier between the antenna and the oscillator performs the following functions: it reduces RF leakage of the oscillation signal to the antenna, it provides an input match

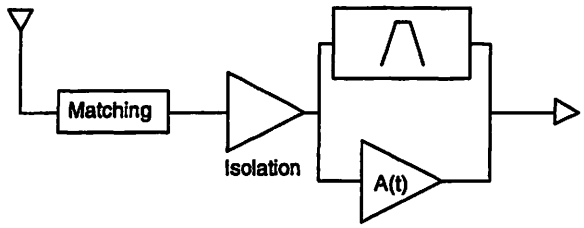


Figure 4.2: Conceptual diagram of super-regenerative detection

to the antenna via the passive matching network, and it injects the RF input signal current into the oscillator tank without adding significant loading to the oscillator. The time-varying nature of the loop gain is designed such that the oscillator transconductance periodically exceeds the critical g_m necessary to induce instability. Consequently, the oscillator periodically starts up and shuts off. The periodic shut-down of the oscillator is called "quenching". The start-up time of an oscillator can be shown by Equation 4.1.

$$t_{rise} = \tau_{rise} \cdot ln\left[\frac{V_{osc}}{V_{initial}}\right] \tag{4.1}$$

where τ_{rise} is the time constant of the exponentially increasing oscillation envelope, V_{osc} is the zero-peak RF voltage of the saturated oscillator, and $V_{initial}$ is the zero-peak RF signal when the oscillator loop gain is unity (at the onset of oscillation). As this equation shows, the start-up time of the oscillator is exponentially dependent upon the initial voltage of the oscillator tank. This dependency provides the large gain attainable by the super-regenerative receiver. There are two basic modes of operation: the logarithmic mode and

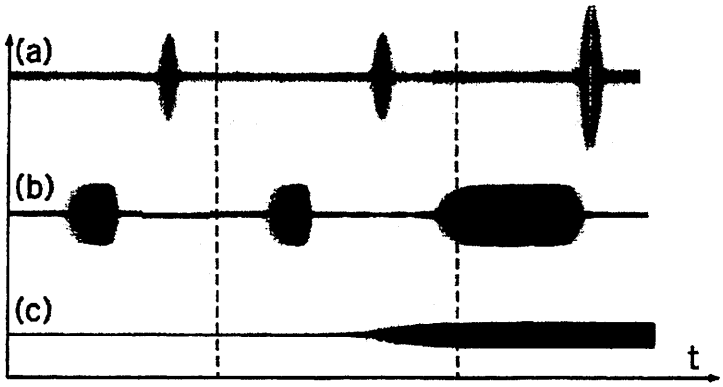


Figure 4.3: Modes of super-regenerative operation. a) Linear b) Logarithmic c) RF Input

the linear mode [1]. Waveforms (a), (b), and (c) in Figure 4.3 show the detector output in the linear mode, the output in the logarithmic mode, and the RF input signal, respectively. In the linear mode, the amplitude of oscillation is measured before the oscillator reaches saturation, providing a high signal-independent gain. If the oscillator peak level is sampled before it reaches saturation, a signal-independent gain is realized. As shown in waveform (a), the sampled envelope is much larger in the presence of an RF input signal. Notice that, in this mode, the oscillator is disabled after the amplitude is measured. Thus, in the linear mode, the oscillator never reaches saturation. In the logarithmic mode, however, the oscillator is allowed to saturate during each cycle. Detection circuitry senses the area under the oscillation envelope, providing signal-dependent gain. Waveform (b) shows the increased area under the saturated oscillation envelope in the presence of an RF input, resulting from the decreased oscillator start-up time in this condi-

tion. Due to the severe fading anticipated in dense indoor sensor networks, a very wide dynamic range is required from the receiver. The logarithmic mode provides an inherent automatic gain control, making its use preferable for this application.

It should be noted that there are two very different methods to achieve a logarithmic-mode response. The first, as mentioned above, is the full on/off quenching of an oscillator by an external signal. This signal modulates, as a function of time, either the active device gain or the tank impedance. A second method of logarithmic mode excitation involves the use of a squegging oscillator. The term "squegging" refers to a parasitic mode that completely extinguishes the oscillation envelope before commencing oscillation again. Typically, this is caused by a DC bias point shift that occurs during the onset of oscillation, which gradually degrades the device transconductance and causes oscillation to cease periodically.

A super-regenerative oscillator may be operated in the squegging mode, which eliminates the need for an external quench signal. Detection is achieved by measuring the frequency of the squegging occurrences. In the presence of an RF signal, the oscillator starts up faster. Thus, the squegging frequency increases with the RF input level. It can be shown that detecting this frequency provides a logarithmic detection of the RF input, providing the same limitations and benefits as an externally quenched logarithmic mode detector. It should be noted that, in the squegging mode, no external quench signal is needed. The elimination of the quench signal is one main benefit of

a squegging-mode receiver. However, for flexibility in the prototyping phase, an external quench signal is preferred for complete receiver characterization. Thus, for this implementation, an external quench logarithmic mode detector was designed. Ultimately, however, a squegging-mode receiver would be an efficient way to eliminate the need for an explicitly generated quench signal.

The potential of the super-regenerative receiver to generate large signal gain at very low bias currents makes it an attractive architecture for integrated ultra-low power wireless receivers.

4.3 Architecture

In contrast to traditional vacuum-tube implementations, the proposed architecture makes use of additional active devices to provide increased receiver performance. A block diagram for the proposed transceiver is shown in Figure 4.4. The on-off keyed (OOK) transmitter consists of a BAW-referenced oscillator to provide a stable RF carrier and an antenna driver to provide efficient power gain. Digital bits are directly modulated onto the carrier by on/off cycling the transmitter. High transmitter efficiency is achieved through direct modulation and careful oscillator/driver co-design. At the receiving end, the RF input is matched to the 50Ω load presented by the isolation amplifier. The isolation amplifier converts the RF power to a current, injecting it into the detector oscillator while providing isolation between the oscillator and the antenna. The detector oscillator, whose time-varying

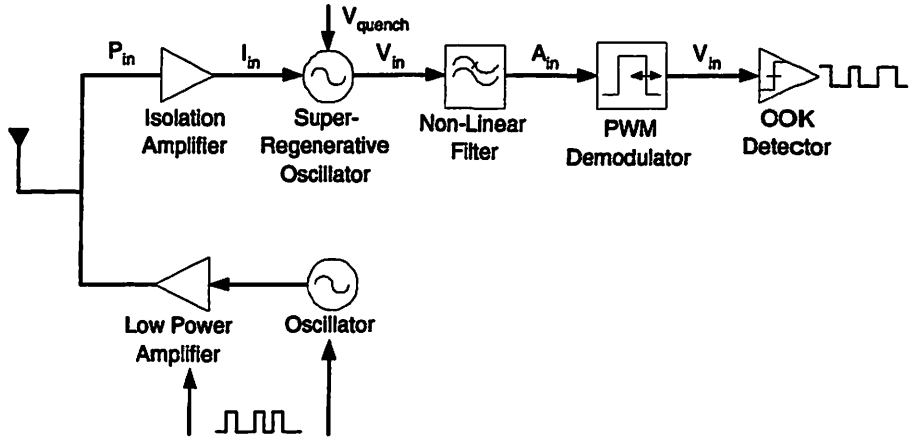


Figure 4.4: Block diagram of proposed super-regenerative transceiver

tank impedance is cycled at 100kHz, samples the RF input signal as an initial condition for its growing exponential, modifying the start-up envelope. The receiver operates in the quenched logarithmic mode. Thus, the signal is sampled directly at RF by the detector oscillator, providing a large RF gain (>55dB) for low signal levels. A BAW resonator sets the free-running frequency of the detector oscillator. The envelope of this oscillation is detected by the non-linear filter, and its 100kHz sampling tone is removed by a pulse width demodulator, leaving a raw OOK analog signal. The baseband signal can be readily detected with an analog matched filter, an A/D with digital baseband, or a one bit slicer with an appropriately placed threshold.

4.4 Analysis

This section will analytically describe the operation of super-regeneration in the logarithmic mode. We will begin with a qualitative explanation of the receiver operation. An analysis of the super-regenerative gain and bandwidth follows. Finally, limitations of the quench frequency are derived.

4.4.1 Operation

The RF signal is coupled into the oscillator tank. It is then discretely sampled by the time-varying detector oscillator. Since this is a discrete-time sampled process, the quench rate must be at least twice the highest frequency component of the baseband signal. This quench tone must be filtered from the data signal to avoid corrupting the baseband signal. Thus, the oversampling ratio is determined by the complexity of this filter. The datarate is ultimately limited by the bandwidth of this filter. However, the quench frequency cannot be arbitrarily increased to achieve a higher datarate. The frequency of the quench signal is limited by the time varying growing exponential time constant of the oscillator, τ_{det}. For a high Q resonant structure, such as a BAW resonator, τ_{det} is relatively long (greater than 100ns). To allow a higher quench frequency, a short duty-cycled quench signal (e.g. 10%) can be utilized. In this implementation such a short duty cycle is possible due to the very rapid quenching of the oscillator tank by the shunting transistor. A majority of the quench cycle can be dedicated to oscillator start-up and

detection instead of quenching.

4.4.2 Super-regenerative gain

The following is a derivation of the gain of a super-regenerative receiver in the logarithmic mode. First, let us consider the startup time of an oscillator (the time from enabling the oscillator until it reaches its saturation voltage V_{osc}) as shown in Equation 4.2.

$$t_{rise,noise} = \tau_{rise} \cdot log\left[\frac{V_{osc}}{\sqrt{\overline{v_n^2}}}\right] \tag{4.2}$$

Notice that this is the same as Equation 4.1 except that the initial oscillator signal is the thermal noise of the oscillator tank and active devices. Thus, we predict that the oscillator will actually reach saturation in a different amount of time each time it starts up. This is indeed the case, as shown by the measured histogram of oscillator startup transients in Figure 4.5.

This histogram was created by superimposing many startup traces, allowing a visualization of the uniformity of the startup time. The histogram shows that the startup time of the oscillator is poorly defined (fuzzy light colored leading edge) since it is directly related to the instantaneous noise in the tank at as the oscillator loop gain exceeds unity. Observing that the startup time is very sensitive to low-level signals in the oscillator tank, it becomes clear that this mechanism can be used to amplify desired signals as well. As the input signal current is injected into the oscillator tank, it

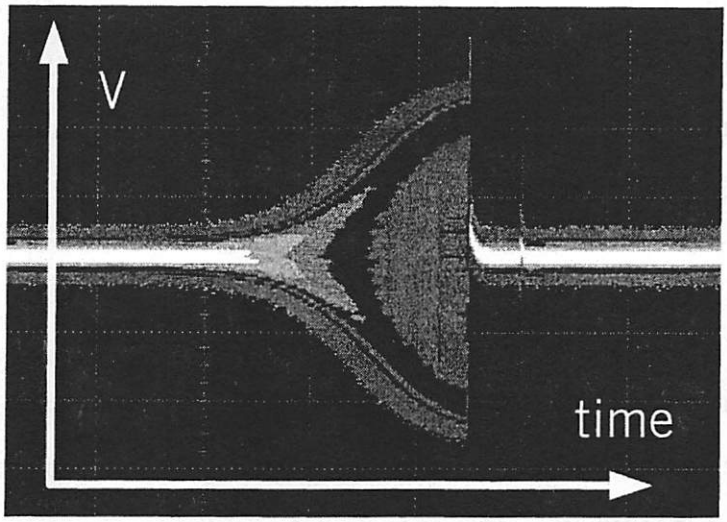


Figure 4.5: Startup of RF oscillator in the presence of noise

is converted to a voltage V_{rf}. For large RF signals, the startup time of the oscillator is given by Equation 4.3.

$$t_{rise,signal} = \tau_{rise} \cdot log\left[\frac{V_{osc}}{V_{rf}}\right] \tag{4.3}$$

One can quantify the signal to noise ratio as the area between the two exponential Equations 4.2 and 4.3. This is given by Equation 4.4.

$$\Delta_{area} = V_{rf}\int_0^{t_{rise,sig}} e^{\frac{t}{\tau}}dt + V_{osc}(t_{rise,noise} - t_{rise,signal}) - \sqrt{v_n^2}\int_0^{t_{rise,noise}} e^{\frac{t}{\tau}}dt \tag{4.4}$$

To extract the modulated data from this signal, a running average of

the oscillator envelope is taken, yielding V_{bb}. V_{bb} represents the demodulated output voltage in response to an RF input. In this analysis, DC is the quench waveform duty cycle and f_q is the quench frequency. Equation 4.5 gives the demodulated output assuming a high receiver SNR.

$$V_{bb} = V_{osc}\left[DC - \frac{\tau}{T_q} ln\left(\frac{V_{osc}}{2V_{rf}}\right)\right] \tag{4.5}$$

V_{osc} is the RF oscillator zero-peak swing, $T_q = \frac{1}{f_q}$, V_{rf} is the RF resulting from the input RF power, and τ is the oscillator start-up time constant. The receiver gain, therefore, is given by Equation 4.6.

$$Gain = \frac{V_{bb}}{V_{rf}} = \frac{V_{osc}}{V_{rf}}\left[DC - \frac{\tau}{T_q} ln\left(\frac{V_{osc}}{2V_{rf}}\right)\right] \tag{4.6}$$

Notice that the receiver gain is approximately a linear function of the input signal amplitude. Thus, from a system perspective, the receiver can be modeled quite accurately as a linear amplifier followed by a logarithmic detector. This property will be revisited in the measurements section of this Chapter.

4.4.3 Super-regenerative bandwidth

As shown in the block diagram in Figure 4.2, the receiver is tuned by a bandpass filter with bandwidth f_{FB}, which sets the free-running oscillator frequency. For this analysis, we will assume that this bandpass filter block has a second-order, high Q resonance.

4.4 Analysis

By applying positive feedback to the system with a gain $A(t)$, the poles move closer to the $j\omega$ axis, increasing the Q of the system. This mode is called the *regenerative mode.* In this mode, a gain enhancement is achieved since the tank impedance increases. In addition, the receiver bandwidth decreases, resulting from the Q enhancement of the positive feedback. As one may expect, such a system is prone to oscillation and requires frequent calibration. However, as observed by Armstrong, periodically allowing oscillation can provide the same benefits as the regenerative mode with increased robustness. This section derives the frequency response of this mode, called the *super – regenerative* mode. For the bandwidth analysis, we will limit our discussion to the logarithmic mode of super-regeneration.

Let us define g_{tank} as the effective conductance of the tank. The bandwidth of the tank is then:

$$BW_{-3dB} = \frac{f_o}{Q_{tank}} = \frac{g_{tank}}{k} \tag{4.7}$$

Where k is a constant that will be subsequently canceled. Let $g_{active}(t)$ represent the time-varying negative conductance presented to the tank by the active devices. The total conductance is given by $g_t(t) = g_{tank} - g_{active}(t)$. When $g_t(t)$ becomes negative, the exponential oscillator start-up ensues. The RF input signal plus noise is sampled as an initial condition for this growing exponential. The magnitude of g_t thus effects the bandwidth of the receiver, as will now be shown.

During super-regeneration, the bandwidth is modified by the new pole locations to yield Equation 4.8.

$$BW_{-3dB} = \frac{f_o}{Q_{tank}} \frac{(g_{tank} - g_{active})}{g_{tank}} = \frac{f_o}{Q_{tank}} \frac{(g_t(t))}{g_{tank}} \tag{4.8}$$

During operation, this appears as two coupled tanks, giving the following -6dB receiver bandwidth [1].

$$BW = \frac{g_{tank} g_t}{(g_{tank} + g_t)k} \tag{4.9}$$

Where k is the same constant given in Equation 4.7. Thus, we can normalize the super-regenerative bandwidth to that of the tank resonator only. This would provide the amount of bandwidth narrowing that occurs during the super-regeneration process.

$$\frac{BW_{SR}}{BW_{tank}} = \frac{g_t}{g_{tank} + g_t} = R \tag{4.10}$$

Where we will define R as our bandwidth narrowing factor. Equation 4.10 indicates that, if a great deal of bandwidth narrowing is needed, the transconductance g_t must be very tightly controlled. For a high bandwidth narrowing factor R, the tank conductance must be greatly reduced in the super-regenerative mode, causing the high precision requirements on the transconductance. To quantify the sensitivity, we must relate the bandwidth to the oscillator transconductance. Here we will consider the tank conductance only during super-regeneration, removing the time-varying nature of the tank and

using the magnitude of the oscillator transconductance g_m for simplicity.

$$g_t = |g_m| - g_{tank} \tag{4.11}$$

The initial loop gain of the oscillator is given by Equation 4.12.

$$A_{initial} = \frac{g_m}{g_{tank}} \tag{4.12}$$

We can now write the initial loop gain of the super-regenerative oscillator in terms of the desired bandwidth narrowing.

$$A_{initial} = 1 + \frac{R}{1-R} \tag{4.13}$$

For example, assuming an on-chip LC tank at 2GHz with $L = 10nH$, $C = 633.2fF$, and $Q = 10$ would yield a bandwidth of 200MHz and $g_{tank} = 795.8\mu S$. A reasonable desired receiver bandwidth is 500kHz. To provide a 500kHz super-regenerative bandwidth, the tank Q must be narrowed by almost three orders of magnitude ($R = 400$). To achieve this, Equation 4.10 dictates that the total transconductance during super-regeneration must be $g_t = (-2.5x10^{-3})g_{tank}$. Conceptually, to create a high Q system out of a low Q tank, the poles must be placed very near the $j\omega$ axis, necessitating very tight control on the oscillator transconductance. Equation 4.13 indicates that the initial loop gain of the oscillator must be controlled to $A_{initial} = 1.0025$. In a super-regenerative implementation, this requirement manifests itself as the need to have a precisely set quench amplitude. This is traditionally

accomplished through hand-tuning or complex amplitude control loops [31].

In contrast, if one starts with a high Q tank, the transconductance precision requirements are greatly reduced. Now assume a tank consisting of a 2GHz BAW resonator with Q=1000. This yields a tank bandwidth of 2MHz. To achieve a 500kHz receiver bandwidth, the tank must be narrowed by only 4x ($R = 4$). Equation 4.10 now indicates that the total transconductance during super-regeneration must be $g_t = (-0.333)g_{tank}$. This corresponds to an initial loop gain of approximately $A_{initial} = 1.3$, which is much easier to achieve in practice.

The sensitivity of the receiver bandwidth to transconductance variations is also extremely important. For a tank with $Q = 10$, a 5% increase in oscillator transconductance causes a 1895.2% increase in the receiver bandwidth. A 5% decrease in transconductance would eliminate oscillation altogether, disabling the receiver operation. For a high tank ($Q = 1000$), a 5% transconductance variation causes a 14% receiver bandwidth variation, allowing drastically improved robustness in practice. In addition, incremental reductions in transconductance would not eliminate receiver operation. As another specific example, it is interesting to calculate the necessary transconductance accuracy for a 20% receiver bandwidth accuracy. For a $Q = 1000$ tank, the transconductance accuracy must be greater than 7%. For a $Q = 10$ tank, the transconductance accuracy must be better than $5x10^{-5}$%. This highlights the very high sensitivity to bias current and transconductance variations that occur when trying to narrow the bandwidth of a low Q tank through

super-regeneration.

In this work, a high Q tank is used with a low R factor. Thus, a digital square wave quench signal is used and modest oscillator bias current variations have minimal impact on the receiver bandwidth. This will be shown experimentally in Section 4.7.

4.4.4 Quench frequency limitations

The receiver quench frequency is important because it determines the maximum receiver datarate. Because the receiver performs a discrete sampling process, $f_{bb} < \frac{f_q}{2}$. In addition to the sampling rate, the oscillator must decay to below the receiver noise level before the next quench cycle starts. If this condition is not met, the initial condition of the oscillator start-up will be the previous cycle's oscillation and not the desired input RF signal. Equation 4.14 shows the oscillation voltage as a function of time during the decay phase.

$$V_{decay}(t) = V_{osc} \cdot e^{\frac{-t}{\tau_{decay}}} \tag{4.14}$$

To reduce the oscillation to below the oscillator noise floor, the following condition must be met:

$$V_{osc} \cdot e^{\frac{-t}{\tau_{decay}}} < \sqrt{\overline{v_n^2}} \tag{4.15}$$

were $\sqrt{\overline{v_n^2}}$ is the oscillator noise voltage. Thus, the damping time of the

quench phase is given by Equation 4.16.

$$t_{damp} > \tau_{decay} \cdot ln \frac{V_{osc}}{\sqrt{v_n^2}} \tag{4.16}$$

Additionally, because the receiver input signal is discretely sampled by the RF oscillator, noise aliasing occurs. The excess noise factor due to noise folding is given by Equation 4.17.

$$N_{excess} = 10 \cdot log\left[\frac{BW_{noise}}{f_{quench}}\right] \tag{4.17}$$

Where BW_{noise} is the effective brick-wall RF input bandwidth. To reduce noise folding, f_{quench} should be maximized. By substituting for the maximum allowable quench frequency as defined above, and the noise bandwidth, Equation 4.18 is obtained.

$$N_{excess} = 10 \cdot log\left[\left(\frac{f_0}{Q}\right)\frac{2Qln(\frac{V_{osc}}{\sqrt{v_n^2}})}{f_0\pi}\right] \tag{4.18}$$

This relationship can be simplified to Equation 4.19.

$$N_{excess} = 10 \cdot log\left[\left(\frac{2}{\pi}\right) \cdot ln\left[\frac{V_{osc}}{\sqrt{v_n^2}}\right]\right] \tag{4.19}$$

In summary, the discrete-time nature of the RF sampling process causes aliasing to take place, which increases the noise figure of the receiver. For typical values, the excess noise may exceed 5dB. Notice that this noise factor

is independent of the resonator Q. The folding factor may be reduced by modifying the quench waveform to provide higher resonator damping factors, allowing a higher quench frequency and less noise folding. Modern circuit technologies allow the use of an additional active device that acts as a switch to dissipate the RF energy quickly after each quench period. This allows a near-instantaneous oscillator quench, reducing the effects of aliased noise on the receiver noise figure.

4.5 LNA/Oscillator Design

The main considerations in the isolation amplifier design were the following: fully-integrated input matching network achieving an S_{11} of <10dB at 1.9GHz, very low current operation, and sufficient reverse isolation of the detector oscillator signal. Because the current consumption of this stage is set by the detector oscillator, a PMOS amplifier topology was chosen for the isolation amplifier due to the higher transconductances of the NMOS devices. For an inductor degenerated amplifier, the input match occurs at the resonance of the gate and source inductors and the gate-to-source device capacitance (C_{gs}) of the input transistor. This input device was sized for weak inversion operation. While this reduces the f_T of the device, it allows a reasonable gate inductor size (10nH), facilitating full integration of the input matching network. The cascode device sizing is a tradeoff between reverse isolation, headroom, and total amplifier transconductance.

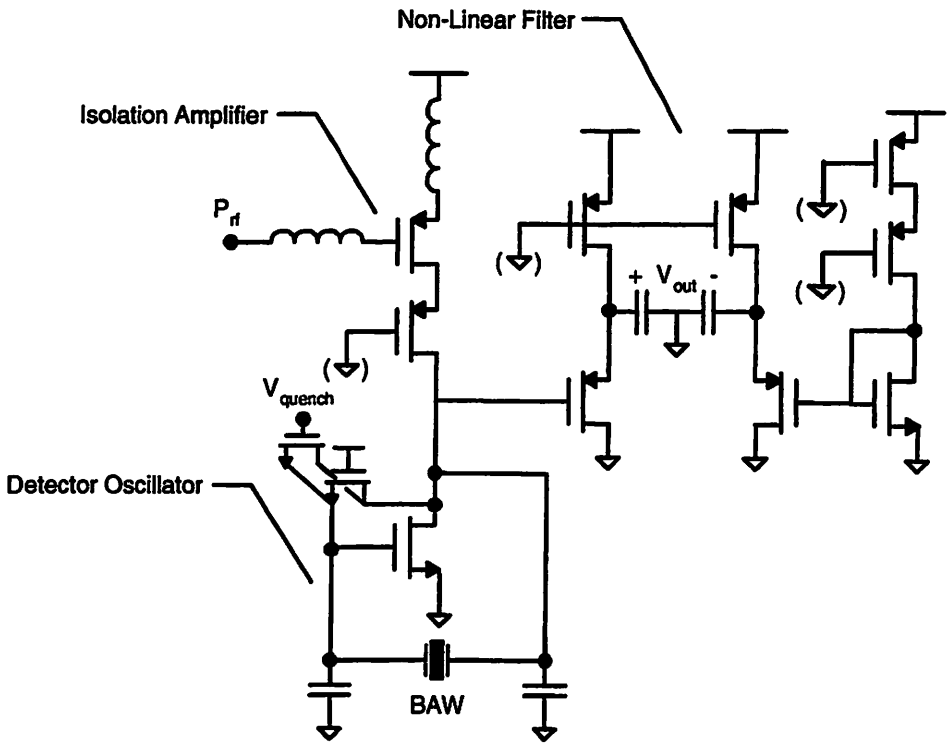


Figure 4.6: Schematic of super-regenerative front-end

The 1V, 400μA receiver front-end schematic is shown in Figure 4.6. The isolation amplifier comprises an inductively degenerated PMOS LNA with two on-chip inductors, yielding a fully integrated matching network. The most power-hungry components in the receiver - the isolation amplifier and detector oscillator - share their bias current, thereby effectively halving the current consumption of the receiver. The detector oscillator is cycled by the quench signal (V_{quench}), which creates a time varying tank impedance, periodically dissipating the RF energy stored in the BAW resonator through

a shunting transistor. The shunting transistor must be sized wide enough to quickly quench oscillation, but small enough to avoid loading the tank with unnecessary capacitance. A 50Ω on-resistance is sufficient, yielding the addition of very low parasitic capacitance. The power consumed in driving the quench transistor must be absorbed into the receiver power budget. For a 300fF capacitance (including pad and wiring capacitance), this power dissipation is approximately 30nW. The shape of this impedance waveform allows for the tuning of the receiver gain and bandwidth properties [32]. A square wave (10% duty cycle) impedance waveform allows simple and adaptable quench generation. Because the data symbols are oversampled, the exact quench frequency and phase is not crucial, and may be readily supplied from a digital control block. The high Q nature of the resonant BAW structure, providing a relatively long oscillator time constant and narrow intrinsic bandwidth, relaxes the need for precise control over the oscillator transconductance. Fine Tx/Rx frequency alignment can be achieved with relatively large, binary-weighted capacitor arrays due to the high Q resonator.

A weak-inversion PMOS non-linear filtering stage is DC-coupled to the oscillator. This stage consists of a PMOS source follower with a relatively low pole frequency (1MHz). The 2GHz carrier is attenuated, but the non-linearity of the PMOS transistor creates a DC component proportional to the envelope of oscillation. By using a DC coupled topology, the non-linear bias point shift of the oscillator NMOS transistor adds to the PMOS non-linear filter, thereby increasing the signal level to the pulse-width demodulator.

A replica stage (with 20x current division relative to the super-regenerative core) was used to provide a pseudo-differential output of the non-linear filter.

4.6 Additional Circuitry

In addition to the RF front-end, the prototype integrated a two-stage RF buffer, a non-linear filter, and a baseband buffer. The RF buffer allows access to the core of the super-regenerative oscillator. Although not needed for normal receiver operation, access to this node is useful for diagnostic purposes. The buffer is self-biased, two-stage, DC coupled, and common-mode insensitive. It presents a 50fF capacitive load to the super-regenerative oscillator and drives a 50Ω, 1pF test equipment load. The RF buffer was included for diagnostic purposes, and allows full characterization of the super-regenerative oscillator operating points.

4.7 Experimental Results

This section documents the experimental verification process for the super-regenerative prototype.

4.7.1 Board Design

A custom printed circuit board was designed, fabricated, and populated. The chip and accompanying resonators were assembled with COB technology; no

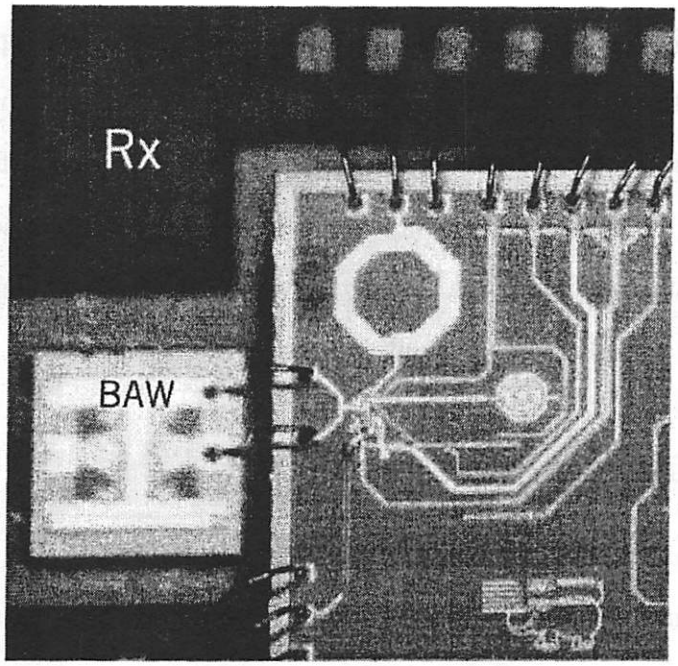


Figure 4.7: Die photograph of the super-regenerative receiver

special assembly techniques were used for the resonator mounting. The prototype receiver implementation is shown in Figure 4.7. Board trace lengths were minimized in order to reduce interconnect parasitics. Finally, bypass capacitors were used on supply lines to reduce noise.

4.7.2 Testing Methodology

For receiver testing, a modulated RF signal generator was used to provide a test signal. An *HP3764A* Bit Error Rate Tester (BERT) was used to provide real-time BER measurements. A pseudorandom sequence of length 2^{23}-1

(8,388,607) was used as the data pattern, providing a non-repeating pattern for 27.9 minutes at 5kbps. Assuming 10 error hits are needed for an accurate BER measurement, 20 seconds of measuring time is needed for a 10^{-4} BER at 5kbps. For a BER measurement of 10^{-5} and 10^{-6}, 200 and 2000 seconds (33.3 minutes) are needed, respectively. Thus, measurement resolution is limited to a BER of approximately 10e-6.

4.7.3 Results

The combined active circuit and inductor area is less than $1mm^2$. The accompanying 1.9GHz BAW resonator is wirebonded directly to the CMOS die to eliminate board parasitics. The measured S_{11} of the fully-integrated matching network is shown in Figure 4.8. The plot shows two distinct input matching curves. Direct chip-level probing of the circuit yields an input match of -27.5dB at 1.894GHz. This is an extremely good match, considering this was a first revision circuit using a fully-integrated matching network. Placement of the chip on a COB test board provides a -25dB input match at 1.7GHz. The reduction in input match frequency is due to the bondwire inductance and the parasitic board capacitance. Because COB board placement is a likely permanent solution, this mismatch in input frequency was corrected in a revised design. The measured eye diagram of the detector oscillator RF signal in the presence of a -80dBm OOK input is shown in Figure 4.9, illustrating the variation in oscillator startup time for "1" and "0" symbols. The measured sensitivity for a bit error rate (BER) of 10^{-3} is

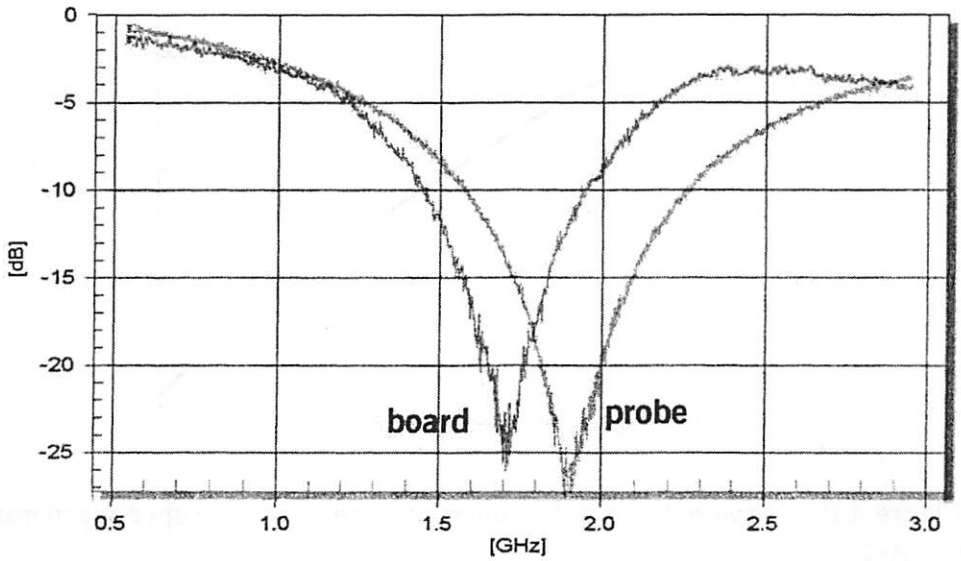


Figure 4.8: Measured S_{11} magnitude of super-regenerative receiver

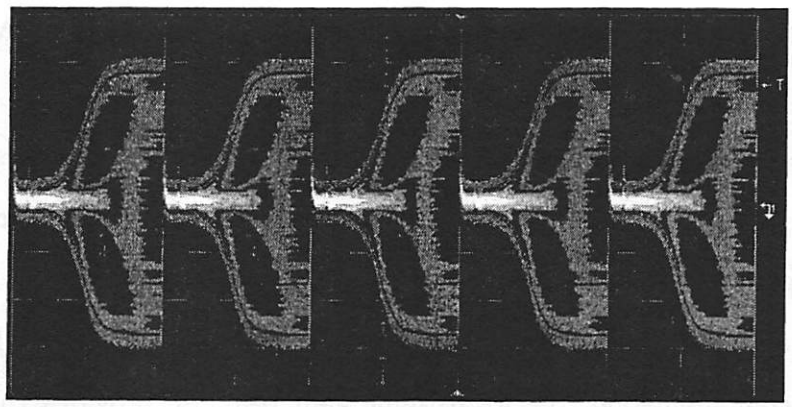


Figure 4.9: Super-regenerative eye diagram in the presence of a -80dBm signal

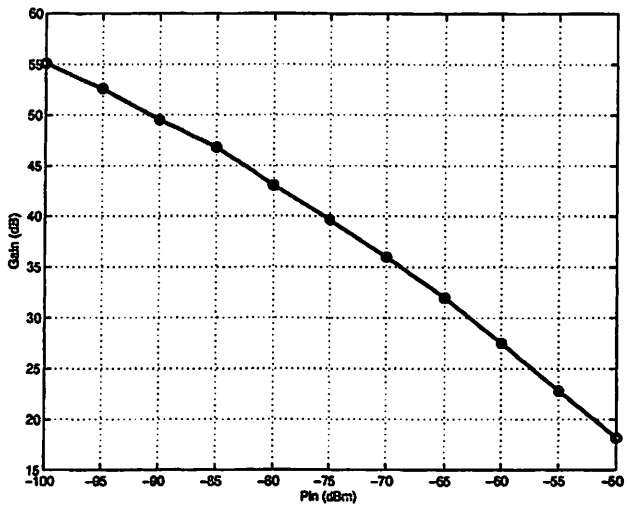


Figure 4.10: Measured signal-dependent gain response of super-regenerative receiver

-100.5dBm at 5kbps, displaying negligible degradation over a supply voltage range from 0.9-1.3V. For a quench frequency of 100kHz and a 10% quench duty cycle, the RF small signal bandwidth of the receiver is 0.5MHz. The measured gain response of the receiver, displayed in Figure 4.10, shows the signal-dependent gain characteristic of super-regenerative detectors operated in the saturated oscillator mode. In a vintage super-regenerative transceiver, the logarithmic mode was avoided since unacceptable distortion to analog modulation was introduced by this transfer function. However, for digital OOK communication, the logarithmic gain response provides the receiver with an inherent automatic gain control (AGC), easing the dynamic range requirements of the baseband circuits. AGC is a desirable trait in transceivers for indoor wireless sensor networks which must accommodate large

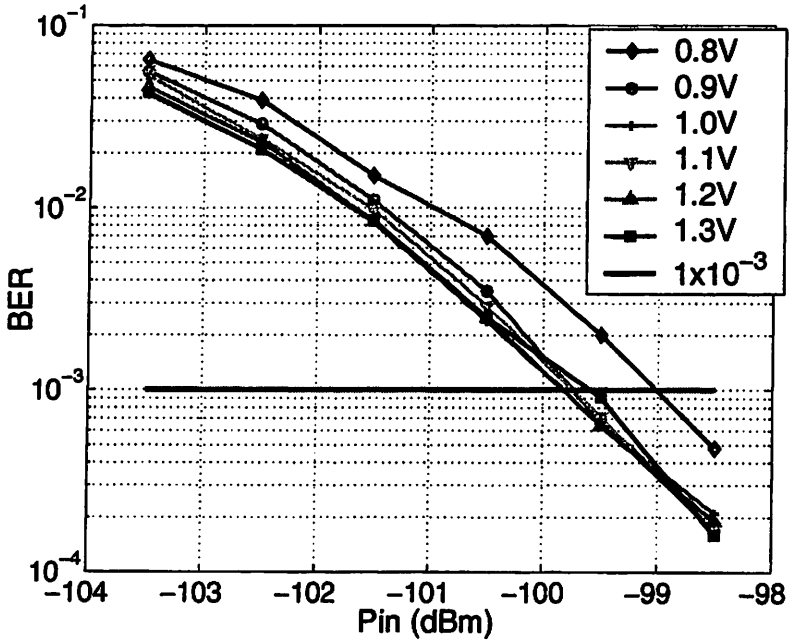


Figure 4.11: Supply voltage dependence of super-regenerative receiver

input power variations due to deep fading and interferers.

To ascertain the performance of the receiver over a range of supply voltages, V_{dd} was swept while monitoring the BER at the output of the demodulator. The experimental data is shown in Figure 4.11. Negligible degradation in BER occurs from 0.9V-1.3V. For a V_{dd} of 0.8V, there is a reduction in sensitivity of approximately 0.5dB, a result of the input PMOS in the isolation amplifier being forced out of saturation by the self-biased cascode device. This sensitivity data was taken with a 20kHz demodulator bandwidth, reducing the sensitivity slightly. The receiver is thus expected to operate over the entire battery life of a typical cell.

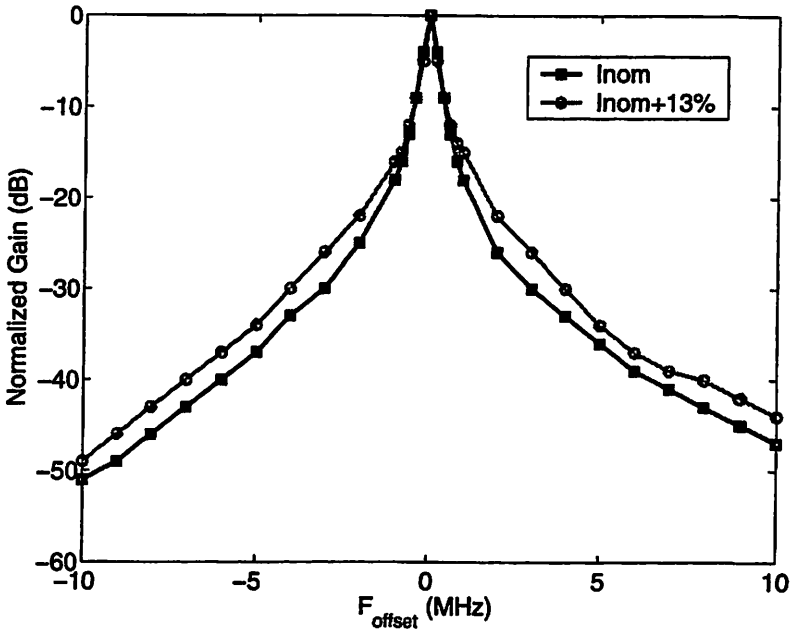


Figure 4.12: Receiver selectivity profile for two bias current levels

The selectivity of the receiver was measured at a quench frequency of 100kHz. The selectivity measurement is important because it determines the interferer frequency offset and power levels that can be tolerated before the desired signal is corrupted. The measurement was performed by adjusting the input signal power for a demodulated BER of 1e-3 at various frequency offsets. See 4.12 for the corresponding receiver attenuation. The small signal receiver bandwidth is approximately 0.5MHz, and the upper and lower rejection is -47dB and -51dB, respectively. Super-regenerative receivers are typically very sensitive to exact bias levels. However, operation in the logarithmic mode relaxes the requirements on the absolute bias current accu-

racy. Figure 4.12 plots the selectivity for the nominal bias current of 400μA. A higher current level of 455μA was also plotted for comparison. A 13% variation in the detector oscillator bias current results in minor variation in the receiver attenuation. Thus, the receiver bandwidth is relatively insensitive to the absolute transistor biasing.

The radiation leakage of oscillator power back to the antenna is an important metric in super-regenerative receivers. Historically, this phenomenon has been a problematic cause of interference when the input signal is transformer-coupled into the oscillator [1]. The use of a cascoded isolation amplifier limits the measured re-radiation at the antenna port to -69dBm[1].

4.8 Discussion

This chapter described the design and implementation of a super-regenerative receiver using BAW resonators. The main benefits of a super-regenerative architecture are:

- Operation at carrier frequencies above the f_T of the active devices, allowing subthreshold device operation and/or high carrier frequencies.

- Fabrication using entirely thin-film processes. This is made possible by using thin-film RF MEMS resonant structures and integrated passive elements.

[1]Modulated with a 100kHz quench tone

- Very high receiver sensitivity due to the high RF gain generated in the super-regeneration process and the relatively small signal bandwidth, allowing reduced transmitted power.

Table 4.1 shows the measured performance characteristics of the prototype super-regenerative receiver.

Table 4.1: Super-Regenerative Receiver Performance Summary

Parameter	Performance
Power Consumption	400μW
V_{dd}	1V
Datarate	5-10kbps
Sensitivity	-100.5dBm
Quench Frequency	100kHz
S_{11} (probe)	-27.5dB
S_{11} (COB)	-11dB

The next step was a standalone transceiver that would integrate the pulse width demodulator, the transmitter, and eliminate all external biasing. This effort is described in detail in the next chapter.

Chapter 5

Fully Integrated Super-Regenerative Transceiver

Chapter 4 described the analysis, design, and testing of a super-regenerative prototype receiver. That work was the basis for the fully integrated super-regenerative transceiver that will be described in this chapter, combining the design strategies developed during the first few chapters. The goals of this design were as follows:

- Minimize the die area of a fully integrated, sub-mW transceiver;
- Achieve full integration: no crystals, inductors, or biasing resistors;
- Integrate programmable transmit and receive RF frequencies;
- Integrate programmable baseband gain and frequency; and
- Utilize a serial interface to minimize digital control pads.

The rest of this chapter will describe the design and implementation of a 1.9mm^2, 400μW super-regenerative receiver and integrated transmitter [33].

5.1 Architecture

Referring back to Figure 4.2 shows the basic architecture used here, which is the same as in the prototype version. The pulse width demodulator and the transmitter are now integrated on the chip. In addition, a digital serial interface was added to allow control over all receiver operation. The front end bias current, front end RF frequency, and baseband filter cutoff frequency and gain are all programmable through this interface.

5.2 RF Front-End Circuit Design

Recall Figure 4.6, showing the front-end circuit schematic. In the fully integrated chip, the layout of the isolation amplifier was modified to reduce the substrate coupling from the super-regenerative oscillator back to the antenna. A guard ring separates the oscillator from the isolation amplifier in order to suppress leakage. A tradeoff exists between the substrate coupling suppression between the oscillator and amplifier and the parasitics added by the critical coupling node between the two blocks. Additionally, the on-chip input matching network was modified slightly to accommodate the anticipated COB assembly parasitic impedances (refer to Figure 4.8).

To eliminate all off-chip biasing circuitry, a digitally programmable on-chip bias circuit was implemented. Current source digital-to-analog converters (DACs), controlled by the SPI interface, were used to provide a variable bias current to the RF front-end. See Figure 5.1 for the DAC schematic.

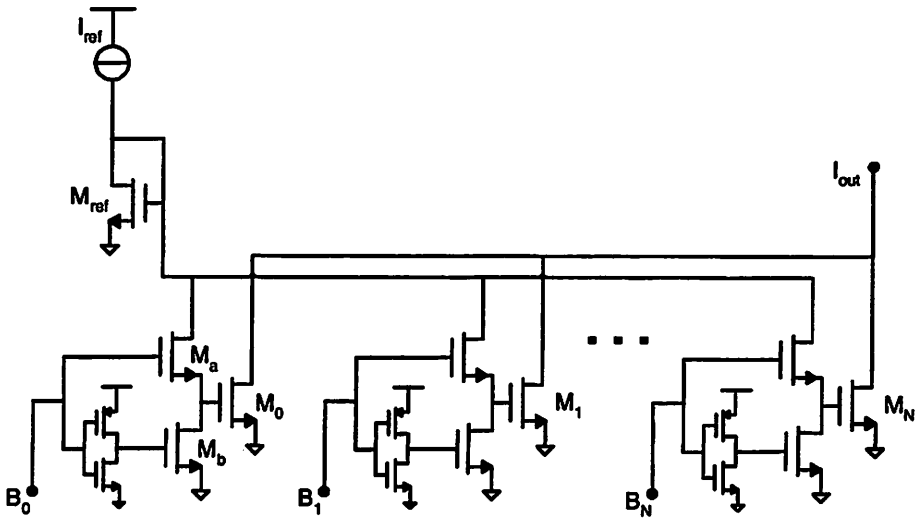


Figure 5.1: Simplified schematic of the current source DAC

The reference current I_{ref} is generated on-chip. Transistors M_0 through M_N are matched binary weighted aspect ratio devices. The gate voltage of transistor M_{ref} is switched to the array via transistor M_a. M_b is driven with an inverted binary code to ensure positive pull-down of all current source gates. For the super-regenerative oscillator biasing, a 6-bit DAC was designed, providing bias currents from 0 to 630μA with a resolution of 10μA.

The DAC layout consumed (80x40)μm^2, including 4pF of decoupling capacitance and a biasing resistor. Dummy cells and randomized unit cell placement was utilized in the layout of the binary weighted array to ensure good DAC linearity. The layout is shown in Figure 5.2.

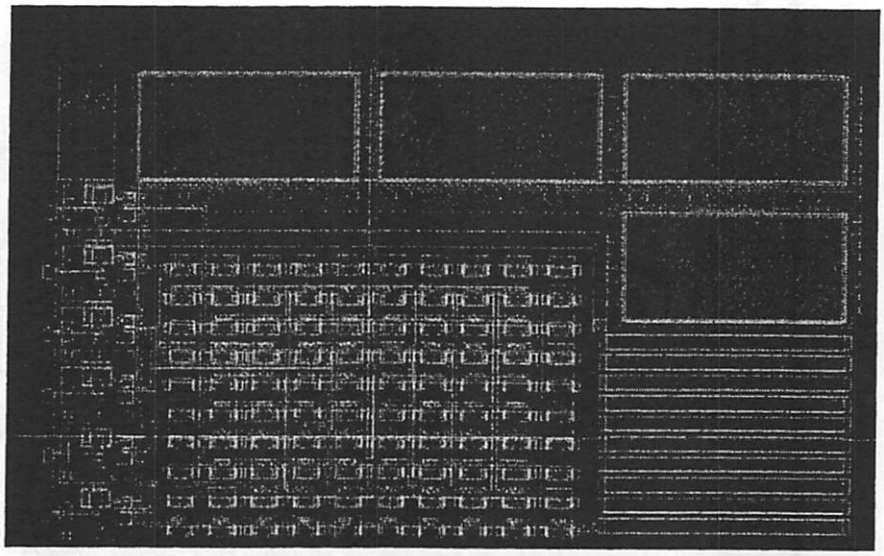


Figure 5.2: CAD layout of current source DAC

5.3 Pulse Width Demodulator

One crucial block of the super-regenerative receiver is the pulse width demodulator. This circuit is responsible for separating the quench tone from the desired signal. To accommodate variable quench frequencies and datarates, a programmable filter is necessary. In addition, in order to accommodate various baseband detection methods, a programmable gain is desirable. The following section describes the filter specification and realization.

5.3.1 Filter Specifications

The signal entering the filter is an envelope of the super-regenerative oscillator output. It consists of a pulse train modulated at the quench frequency

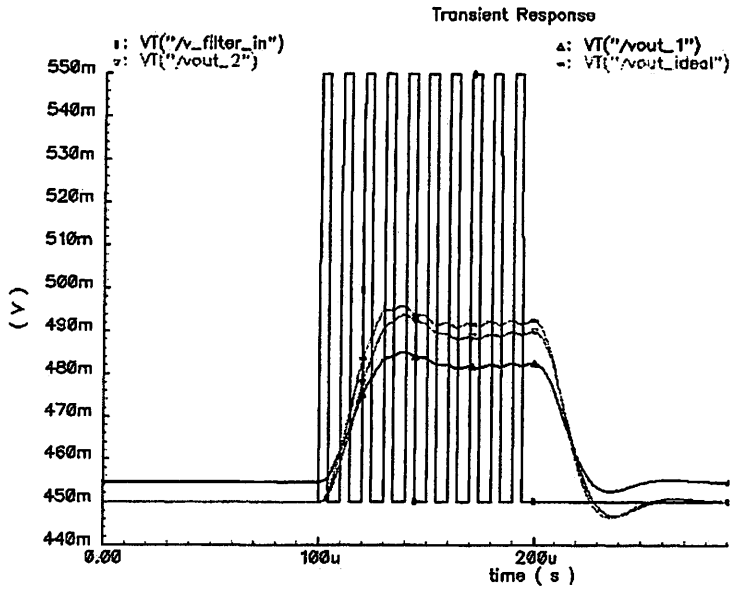


Figure 5.3: Simulated input/output waveforms of the demodulator

(approximately 100kHz). The duty cycle of this pulse train is dependent upon the RF signal strength at the antenna. Mathematically, the demodulated signal is extracted by taking the average of this pulse train. In practice, this can be achieved by a multi-order low pass filter. This filter must separate the baseband signal from the strong quench frequency tone. The quench tone appears as ripple at the filter output. Figure 5.3 shows the simulated input and output waveforms of the pulse width demodulator. A 100mV pulse train at 100kHz simulates the output pulse train of the detector oscillator. The two overlaid curves are the ideal 3rd order butterworth filtering and the simulated output of the full active filter implementation, which closely match. The non-ideal output waveform is the result of using non-linearized

transconductor elements. The filter circuit design will be described in detail in the next section. To ensure that the receiver sensitivity is not compromised by the filter, this ripple must be reduced below the noise floor of the receiver, corresponding to an attenuation of approximately 40dB at 100kHz. It should be noted that the filter also performs anti-aliasing of a subsequent A/D converter.

The design of the filter must trade off filter complexity and datarate. As the filter order increases, the filter cutoff frequency can be placed closer to the quench frequency, allowing higher datarates. System-level Matlab simulations were used to identify the optimal filter order. Figure 5.4 shows the simulation results for a 100kHz quench frequency at a 20kHz filter cutoff frequency. The simulation shows demodulation of 10kbps OOK data and the resulting quench ripple. The duty cycle of the pulse train is varied from 15% to 30%, simulating the receiver operation under low SNR conditions.

A 3^{rd} order Butterworth filter allows sufficient quench signal rejection for this cutoff frequency to allow reception at the receiver RF minimum detectable signal level. For higher signal levels, additional ripple can be tolerated. Thus, the filter bandwidth should be dynamically adjustable to accommodate variable datarates over varying levels of SNR. Additionally, to ease the implementation requirements on the baseband detector, digitally programmable gain should be included in the filter path. These requirements will now be used to synthesize and design the baseband pulse-width demodulator filter.

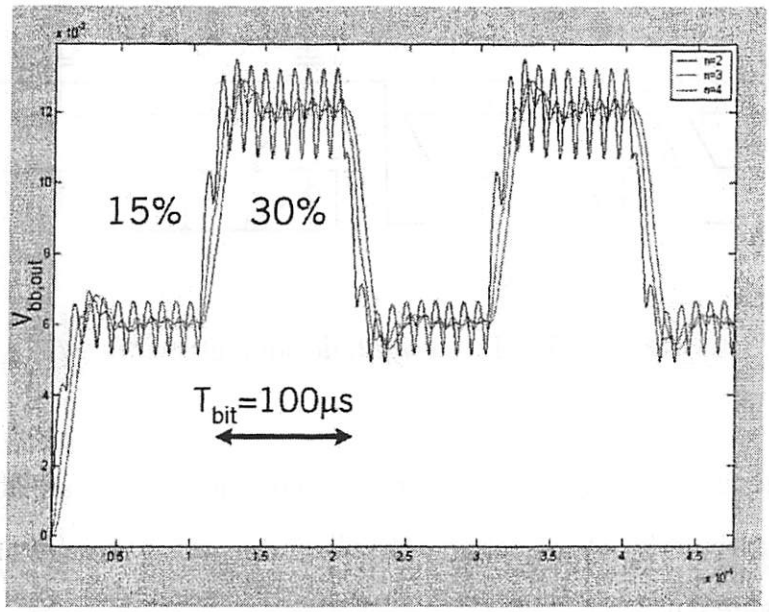


Figure 5.4: System-level simulation of pulse-width demodulator

5.3.2 Filter Synthesis and Design

The 3^{rd} order Butterworth filter was synthesized for a nominal cutoff frequency of 20kHz. A terminated, lumped C-L-C filter ladder was chosen, yielding C_1=795.7pF, L=0.159H, and C_2=795.7pF [34]. Conservative noise scaling was used to render the filter noise contribution negligible in relation to the quench ripple and receiver noise. Scaling yielded C_1=39.78pF, L=3.18H, and C_2=39.78pF. The large-value inductor was synthesized with a 3-OTA, one capacitor gyrator. The result of the synthesis is the filter ladder shown in Figure 5.5.

A folded-cascode structure was chosen for good low voltage performance.

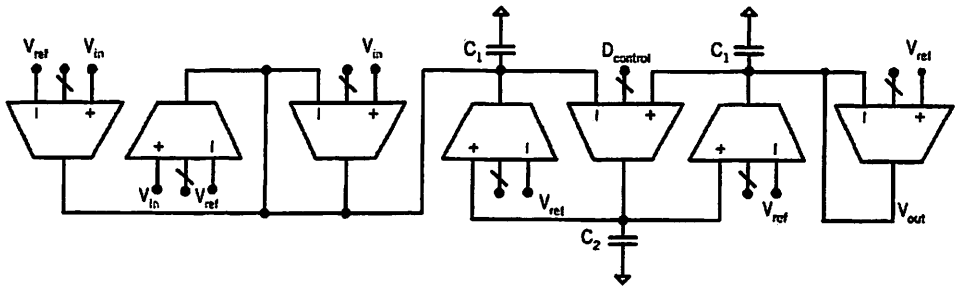


Figure 5.5: Pulse width demodulator filter ladder

The input common mode range and output voltage range are large, allowing the potential for 1V operation. The filter transconductor schematic is shown in Figure 5.6.

Although modern processes necessitate low supply voltages which reduces the circuit headroom, multiple threshold voltages are provided. These transistors can be utilized to facilitate low voltage analog design without sacrificing performance. A combination of high V_t and low V_t transistors was used to achieve optimal V_{ds} values in the output cascode stacks in order to maximize the output swing. The input transconductors are biased in deep subthreshold at 800nA with a $\frac{40\mu m}{0.5\mu m}$ aspect ratio (IC=0.01). Linearization is accomplished through a degenerated split-source input differential pair. The sources of M_1 and M_2 are coupled with the trioded transistors $M_{5,6,7}$. Frequency tuning is achieved by digital control of the gates of these transistors, for which three bits of control are used. The same OTA is used as a termination resistor, yielding digitally adjustable gain control. Each OTA consumes 3.2μW at 1V. The OTA achieves an open-loop DC gain of 60dB

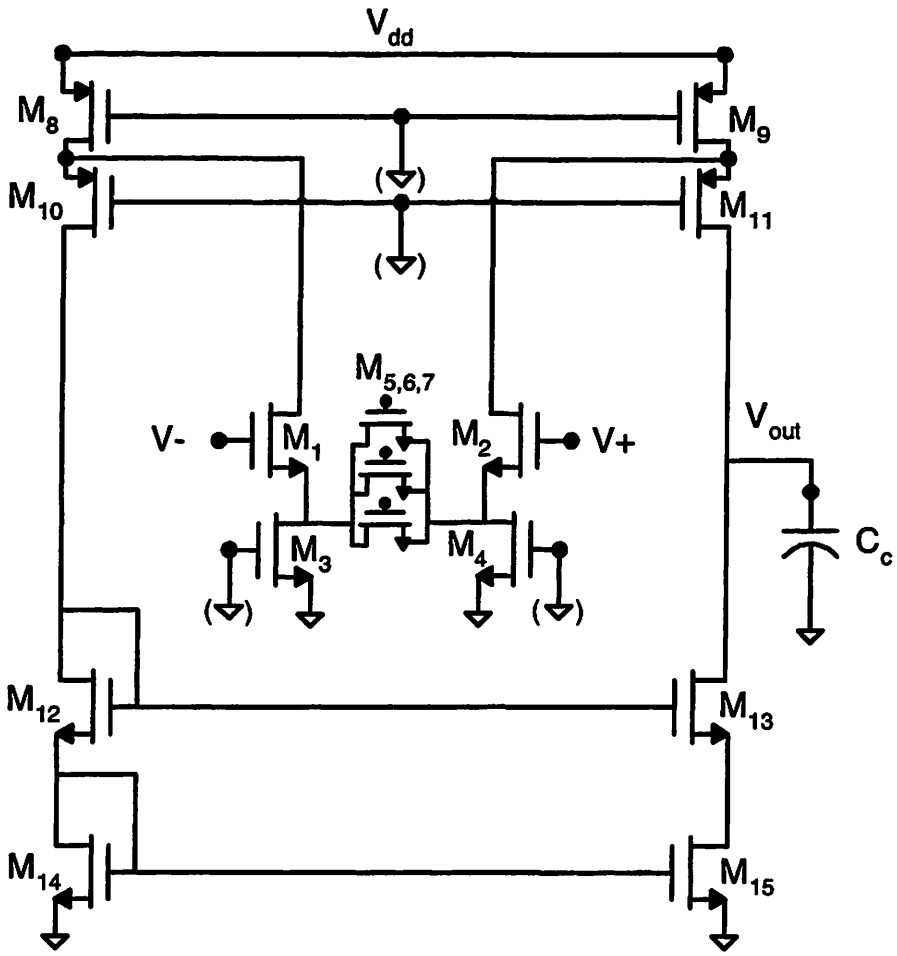


Figure 5.6: Schematic of the filter transconductor

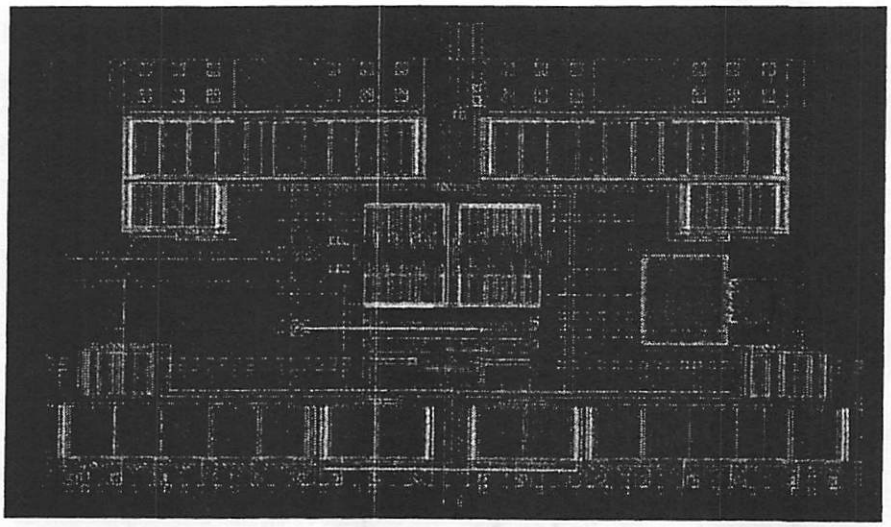


Figure 5.7: Layout of the filter OTA

over a 250-700mV output swing. The minimum phase margin at the maximum transconductance setting is 65°. To reduce the OTA offset voltage, a common centroid structure was used on the input pair. See Figure 5.7 for the OTA layout. Furthermore, large area transistors (greater than $100\mu m^2$) were used for $M_{8,9,14,15}$ to reduce the flicker noise contribution. The filter utilizes a total of 10 OTAs, yielding a total power consumption of 32μW. The filter bandwidth is digitally programmable from 9kHz to 30kHz. Programmable gain from from 6dB to 22dB is achieved. The acceptable filter common mode input range is 300mV to 600mV, and can tolerate a +/-50mV input offset without saturating. The layout of the filter is crucial to obtain good matching between OTAs and filter capacitors. The filter layout is shown in Figure 5.8.

The ten OTAs, filter capacitors, and a bias generator are clearly shown

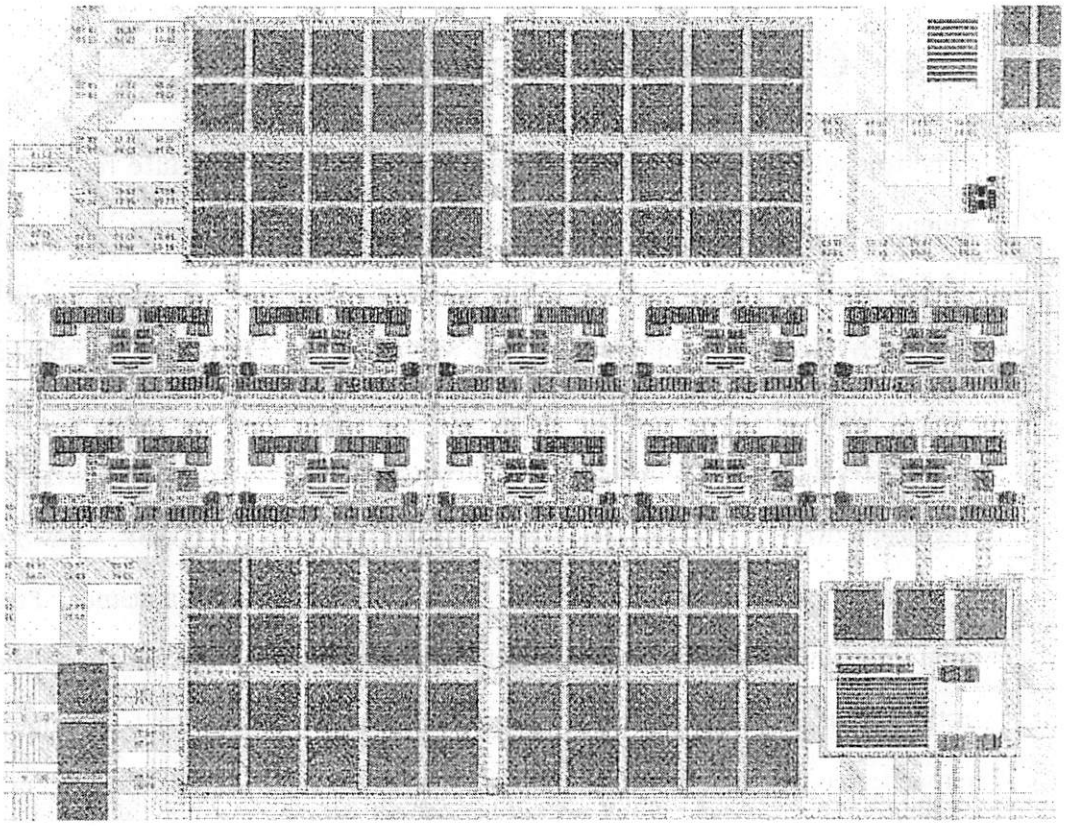


Figure 5.8: Layout of the pulse width demodulator

in the plot. A compact layout is essential, because the area of the filter occupies a sizeable percentage of the total receiver die area. The completed filter consumes (350x450)μm^2.

5.4 Capacitance Tuning

The frequency of the detector oscillator (and, thus, the absolute receiver frequency) is programmable by a binary weighted capacitor array. Due to the high Q resonant structure used, fine frequency steps may be achieved using relatively large unit capacitors. This was shown in Equations 2.2 and 2.3. The bandwidth of the receiver is 500kHz, setting the limit for the frequency tuning resolution. A 3-bit capacitive array was used to provide 500kHz tuning steps over a total frequency range of approximately 3.5MHz, allowing a Tx/Rx alignment that is insensitive to small changes in capacitance. Equation 2.2 provides the frequency sensitivity to capacitive variation. The theoretical frequency shift of the BAW parallel resonant frequency to changes in capacitance is given by Equation 5.1.

$$\frac{\delta f_p}{\delta C_T} \simeq f_{series} \frac{-C_x}{2C_T^2} \tag{5.1}$$

For 500kHz steps, a 60fF least-significant bit (LSB) capacitance is needed. The switch transistor design entails an optimization of the tradeoff between series resistance and un-switched capacitance, both of which reduce the oscillator performance. The result of the optimization was a $\frac{20\mu m}{0.13\mu m}$ NMOS

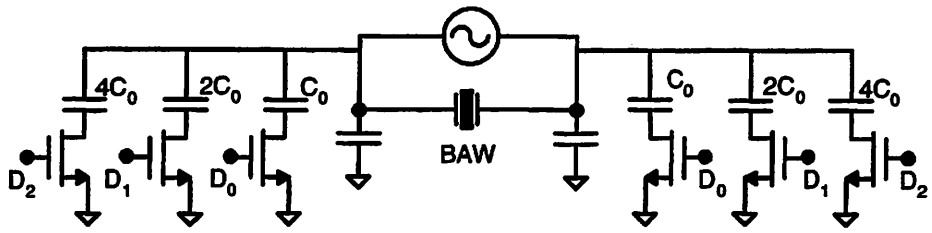


Figure 5.9: Schematic of binary weighted switched capacitor tuning array

switch aspect ratio and a 80fF unit cell LSB capacitance was used, providing a switched capacitance of 60fF and a series switch resistance of approximately 25Ω at a 1V switch voltage, yielding a switched capacitor quality factor of approximately 50.

Two matched capacitor arrays were used, one on each side of the BAW resonator. Figure 5.9 shows the implementation of the capacitor array.

It should be noted that, due to Miller multiplication, a factor of two reduction in the necessary capacitance could be achieved by using one array shunting the BAW resonator. However, it is advantageous to use two non-Miller multiplied arrays because the capacitance on either side of the resonator forms the feedback network. To optimize loop stability, any additional capacitance should be added to these feedback capacitors, not the BAW shunting capacitance. Capacitive tuning allows compensation for resonator fabrication uncertainty, a means of temperature compensation, and the opportunity for both frequency hopping and interferer avoidance.

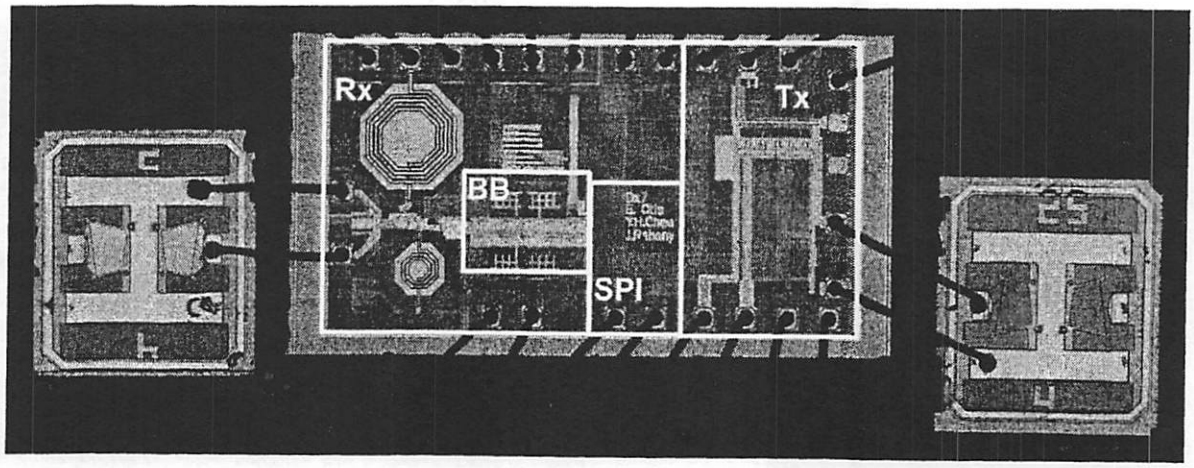


Figure 5.10: Chip photograph of the assembled integrated transceiver

5.5 Chip Implementation

The goal of the chip floorplanning was to reduce the die area, ensure RF signal integrity, and integrate as much functionality as possible on-chip. To reduce the die size, a three pin serially programmable interface (SPI) was implemented, allowing control over the transceiver control bits. All biasing was generated internally and controlled digitally, eliminating external references and trimming. The RF receive path consumes an area of $0.5mm^2$, and was isolated from the transmitter and SPI interface to minimize coupling. See Figure 5.10 for a photograph of the assembled chip.

The left side of the chip (RF front-end) is the "quiet" side, and the right hand side (transmitter) is the "noisy" side. As the signal passes from left-to-right, from the super-regenerative oscillator to the non-linear filter and through the pulse-width demodulator, the signal frequency decreases,

making the signal less susceptible to coupling. An output buffer located in close proximity to the demodulator drives the signal to the output pads. The buffer provides drive capability for a 2kΩ, 20pF off-chip load.

The transmit and receive resonators are clearly visible on either side of the chip. Standard commercial assembly techniques (chip placement with conductive epoxy and gold wirebonding) were used, providing a very economical and repeatable assembly.

5.6 Measured Results

This section describes the measured results of the fully integrated super-regenerative receiver.

5.6.1 Serial Interface

A three-wire SPI interface was used to facilitate on-chip biasing and frequency tuning while allowing a low pad count. This interface was fully functional, and allowed the the programming of eight 8-bit registers on the chip (2^{64} total states). These registers control on-chip biasing DACs, baseband transconductantances, and switched capacitor arrays. The SPI interface was fully functional, and all receiver tuning and biasing was controlled via a laptop computer USB interface. The SPI interface utilizes a commonly-used, standard chip-to-chip protocol, allowing easy integration of this chip with other custom digital chips.

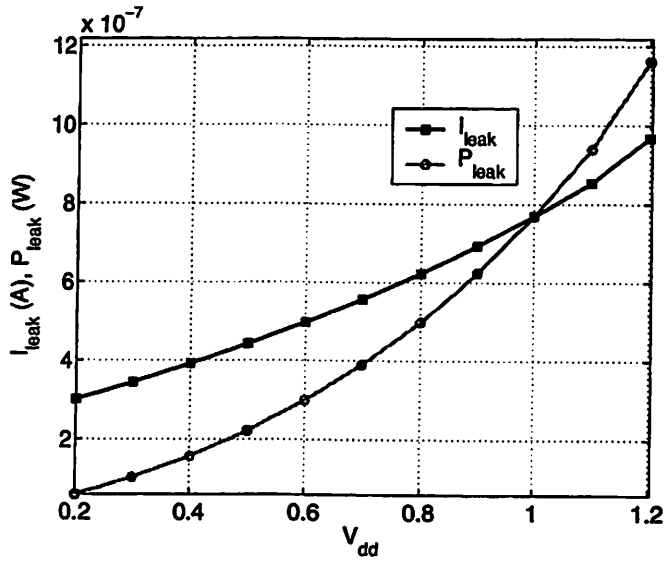
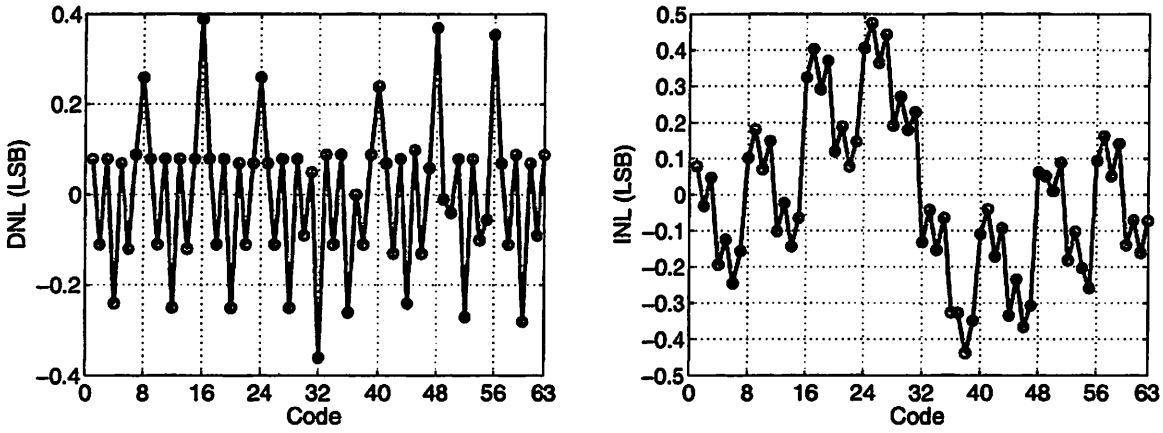


Figure 5.11: Measured leakage current and power of digital control block

The SPI interface block integrates over 4000 high-V_T transistors and is composed of standard cell static $0.13\mu m$ CMOS logic. It is important to ensure that the leakage currents of such blocks are small relative to the rest of the receiver circuitry. Figure 5.11 shows the measured leakage current and power of this digital block over a range of supply voltages.

At the nominal supply voltage of 1V, the total leakage power of the SPI interface block is 770nW, which is negligible in relation to the other transceiver blocks. The total power consumption of the receiver when active is 380μW.

The linearity of the current source DAC was measured. Two important metrics for the accuracy of ADCs and DACs are the Integral Non-Linearity



(a) DAC DNL Measurement

(b) DAC INL Measurement

Figure 5.12: Measured linearity of the current source DAC

(INL) and the Differential Non-Linearity (DNL). The DNL is the incremental difference of each code width compared to the ideal code width (one LSB). A DNL less than +/- one LSB ensured there will be no missing codes. The INL is the integral of the DNL over the entire code range. See Figure 5.12 for the measured linearity performance of the current source DAC.

The DNL and INL errors are below +/- 0.5 LSB, indicating linearity accuracy that is sufficient up to 7 bits with no missing codes.

5.6.2 RF Front-End

This section documents the measured performance results of the radio frequency portion of the receiver. The BAW resonator capacitive tuning array operates as expected, and its performance matches theoretical calculations well. The measured frequency step size indicates a great deal about the

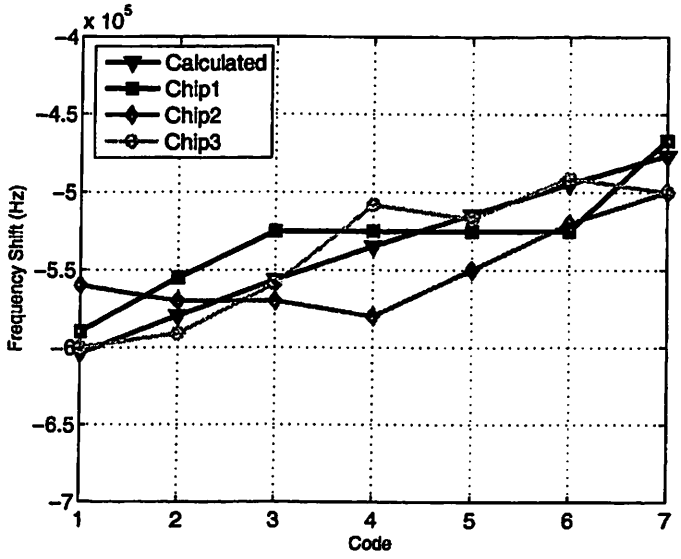


Figure 5.13: Incremental frequency shift over all codes

health of the receiver; it reveals the accuracy of the switched capacitance, the loaded resonator Q, and the parasitic shunting capacitance of the resonator. The frequency shift at each code was measured for three different chips and compared to the theoretical values as calculated by Equation 5.1. These results are plotted in Figure 5.13.

The measured values agree reasonably well with calculations. As Equation 5.1 predicts, the incremental frequency decrease is a function of the frequency code. As more capacitance is loaded on the tank, the frequency sensitivity to capacitance variation decreases. To achieve a linear frequency-code characteristic, the capacitors could be implemented as a thermometer-coded capacitor bank with increasing capacitance as a function of code. A

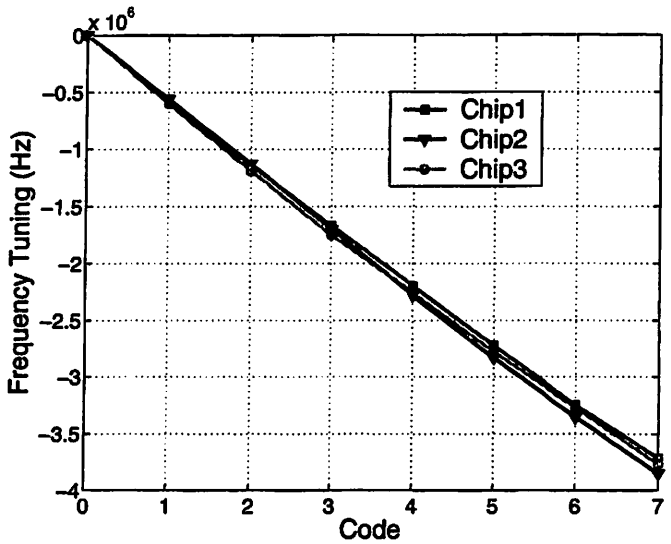


Figure 5.14: Switched capacitor frequency tuning of receiver

non binary-weighted scheme would result in a large increase in the required capacitance area.

The effects of random mismatch in the absolute and relative capacitive values are clearly visible. In addition, variation in the intrinsic resonator qualify factor will alter the total tuning range. Figure 5.14 shows the total measured frequency offsets for the three different chips. The matching of frequency tuning between the three CMOS/BAW systems is very close, allowing predictable frequency tuning. The maximum frequency variation that accumulated across the entire frequency range of the three chips was 72.6ppm, which is likely due to Q variation of the BAW resonators.

The super-regenerative oscillator amplitude will naturally vary across the oscillator tuning range. Figure 5.15 shows the measured variation in ampli-

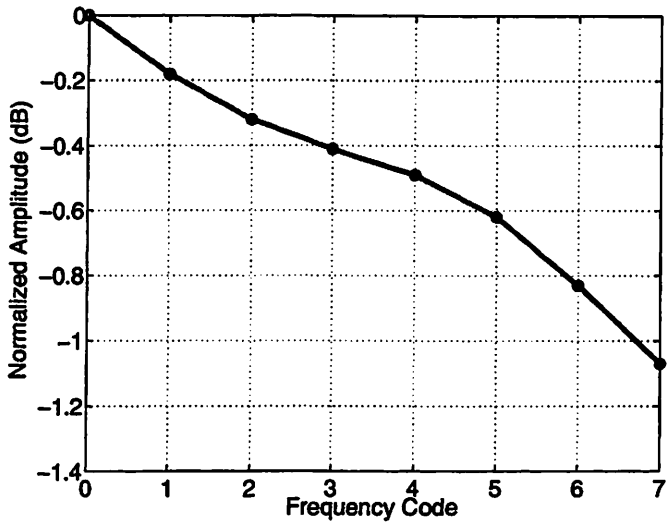


Figure 5.15: Measured super-regenerative oscillator amplitude vs. frequency code

tude over the entire range.

Due to the relatively small tuning range and the high Q of the switched capacitance, the output amplitude variation across frequency code is small.

The phase noise of the detector oscillator was characterized over the frequency code range. See Figure 5.16 for the measured phase noise data.

The close-in phase noise is nearly identical to the other oscillators discussed in this thesis (for example: Figure 2.7 and Figure 2.12). Notice that the noise floor at large frequency offsets is higher than the other measurements presented here. Because there is no explicit RF output port, the phase noise was measured as a leakage signal at the receiver input port. This measurement technique results in a very low sinusoid amplitude, yielding a high

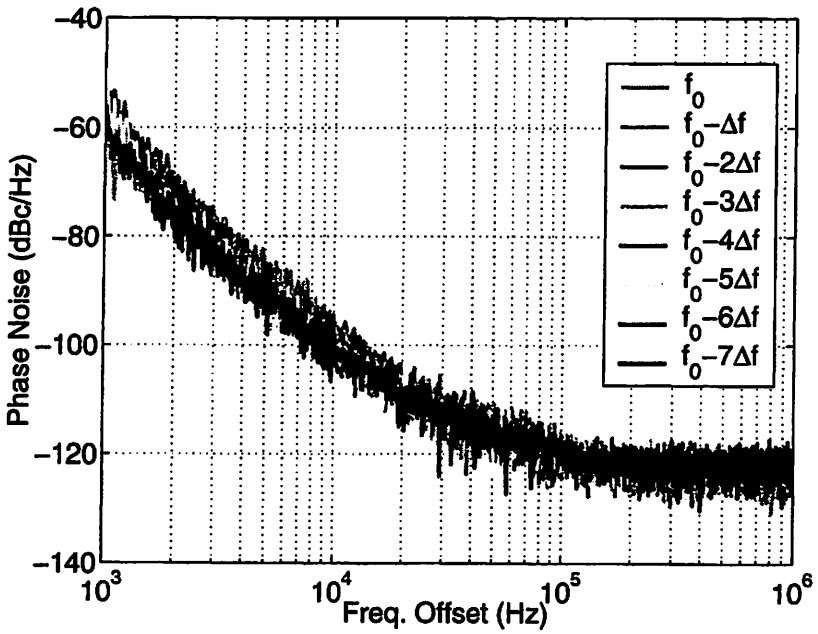


Figure 5.16: Measured phase noise of detector oscillator over tuning range

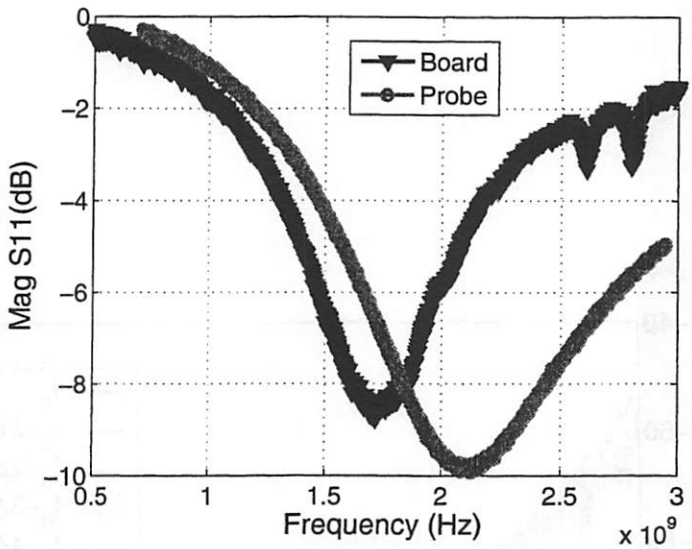


Figure 5.17: Magnitude of receiver S_{11}:

measurement noise floor. Notice that the close-in phase noise actually improves slightly at the lower frequency range. This phenomenon is due to the increased RF signal power that results from the decreased oscillator tank impedance under the higher capacitive loading conditions.

The impedance match of the receiver was measured at nominal operating conditions and is shown in Figure 5.17. A comparison of input match on a test board and though direct die probing was made and plotted in Figure 5.17. As expected, the input match resonance decreases by approximately 200MHz when mounted on a test board. However, the quality of, as measured through die probing (approximately -10dB) is worse than expected. The most likely explanation is a lower-than expected source inductance.

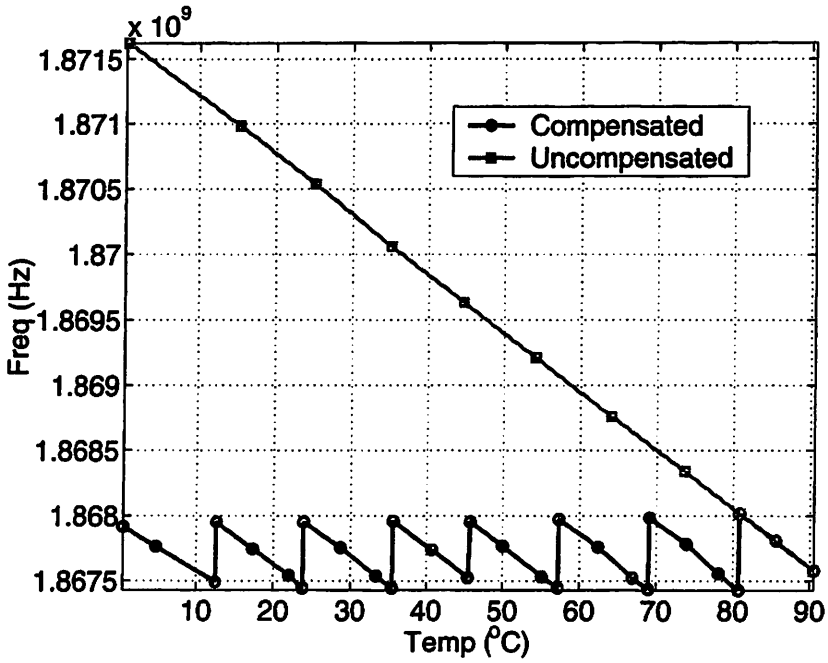


Figure 5.18: Temperature compensation of BAW-based receiver

5.6.3 Temperature Compensation

As was shown in Figure 2.14, BAW resonators exhibit a temperature coefficient of approximately -25$\frac{ppm}{^oC}$. This temperature coefficient, though large, is well-behaved and easily compensated through switched capacitors. The integrated 3-bit capacitive array size was chosen to place the detector oscillator frequency within the -3dB bandwidth of the receiver (approximately 0.5MHz). This technique was experimentally verified with the super-regenerative receiver. See Figure 5.18 for the measured temperature data.

A temperature variation from 0 to 90°C would theoretically predict a fre-

quency shift of 4.2MHz. However, by switching the capacitor array, this temperature drift can be compensated. The frequency deviation due to temperature was limited to the approximate RF bandwidth of the receiver. Temperature variation testing was performed with a *Temptronic LM01980* thermal forcer. All temperature readings were verified with a *Fluke 52* thermometer with k-type thermal probe.

5.6.4 Baseband

A standalone pulse-width demodulator circuit was tested. The filter is programmable through the SPI interface. The measured performance of the filter across tuning range is shown in Table 5.1.

Table 5.1: Measured demodulator performance over tuning range

Parameter	Low Limit	High Limit
Cutoff Frequency (kHz)	14.5	45.0
Gain (dB)	6	16
Power (μW)	36	36

The filter worked as expected and exhibits good pole matching. Figure 5.19 shows the measured filter frequency response at the low and high frequency settings.

Next, the filter was tested in-situ in its receiver environment. The replica biasing and non-linear filter worked as expected. This filter must provide baseband gain and reduce the quench tone ripple to below the receiver noise floor. The receiver quench signal was varied from 10kHz to the design value

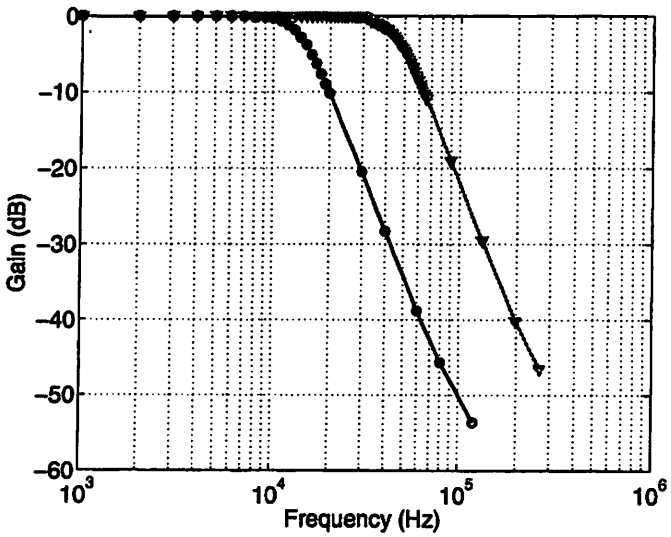


Figure 5.19: Measured frequency response of baseband filter at the high and low bandwidth settings

of 100kHz. Figure 5.20 shows the analog receiver output for three different quench frequencies.

As expected for the 10kHz quench tone pulse train, only a relatively large fundamental tone is visible. For a 100kHz quench tone, the ripple is reduced below the receiver noise floor, as desired.

5.6.5 Link Demonstration

To verify the link budget calculations and ascertain the robustness of the system, an end-to-end wireless link was implemented with two transceiver chips. A 10kbps, 27m indoor wireless link was demonstrated with a 400μW transmit power and a 380μW receiver power dissipation.

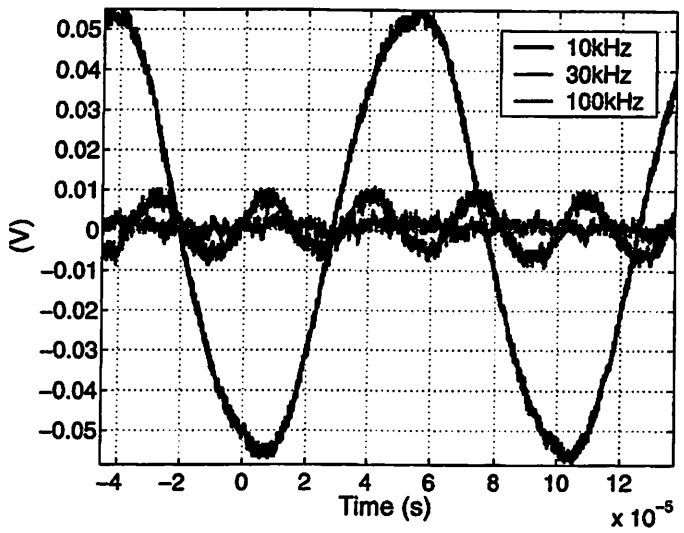


Figure 5.20: Measured ripple of the pulse-width demodulator at quench frequencies of 10kHz, 30kHz, and 100kHz

5.7 Discussion

This chapter has documented the design, implementation, and experimental results of a fully integrated 380μW super-regenerative receiver. The power breakdown of the receiver is given in Figure 5.21.

A majority of the power dissipation occurs in the RF front-end, where the required f_T of the transistors is approximately 2GHz. The required front-end current is approximately 250μW. The I/O consumes 15% of the receiver power budget. This is due to a conservatively-designed analog output buffer designed to drive a wide variety of test equipment loads. Likewise, conservative bias circuitry led to 9% of the chip power dissipation. Future modification of these components could lead to a near-negligible power dissipation

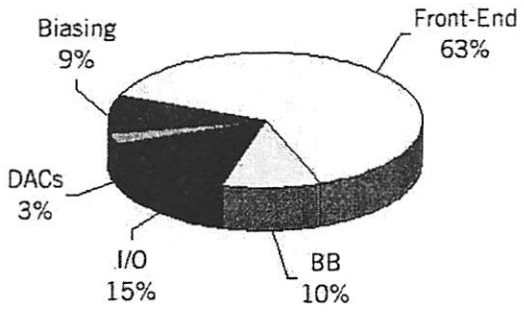


Figure 5.21: Power breakdown of the fully integrated super-regenerative receiver

contribution of these blocks.

Another option to reduce the interference levels and allow channelization is to use a CDMA approach. A CDMA scheme has been proposed for super-regenerative receivers that takes advantage of the excess receiver bandwidth [35]. This is yet another example of re-inventing the super-regenerative architecture by re-examining it with new tools.

The re-radiation of RF energy has been a traditional concern with super-regenerative receivers. This concern is especially valid relating to very dense wireless sensor networks. The measured re-radiation of RF power of the receiver presented here is -69dBm, comparable to that of modern direct conversion receivers. At 2GHz, RF power drops off by approximately 35dB in the first meter. Thus, for node-to-node distances of greater than 1m, the incoming radiated receiver power from another node is below the noise floor.

Chapter 6

Integration Techniques

One of the most aggressive goals of the wireless sensor research vision is the node volume specification. Achieving a $1cm^3$ node volume (approximately the same volume as a 8-pin DIP op-amp package) is very challenging, and new integration techniques must be developed. This chapter describes two innovations that dramatically decrease the required implementation area.

First, a CMOS/MEMS silicon reference clock is described. Ultimately, this component will obviate the need for a bulky, surface-mount quartz crystal resonator. It also enables system level degrees-of-freedom that are not currently available. For example, since customized frequencies can be defined lithographically, arrays of resonators at varying frequencies can be fabricated in a very small area on one substrate. Similar to the transition from discrete to integrated transistor circuit design, new design methodologies and architectures will accompany this new method of clock generation.

Secondly, flip-chip techniques are investigated, and two proof-of-concept prototypes are presented. Advanced CMOS/MEMS packaging and assembly

techniques can improve the robustness, reduce interconnect parasitics, and decrease the form factor of these systems.

6.1 Silicon Reference Clocks

In wireless sensor network applications, a low frequency reference clock is needed for timing synchronization, digital circuit clocking, and A/D clocking. This clock is typically implemented by a CMOS oscillator tuned by a surface mount (SMT) quartz crystal. There are, however, serious drawbacks to this strategy. First, the SMT crystal (and accompanying SMT capacitors) often consumes a board area larger than the entire transceiver CMOS chip. See Figure 6.1 for an implementation photograph of a recent sensor network transceiver using an off-the-shelf quartz crystal [36]. The photograph shows that the SMT crystal and capacitors define a board area as large as the transceiver chip. This is unacceptable if the entire sensor node must be implemented in a $1cm^3$ volume. Additionally, the SMT parts add to the bill-of-materials, increasing the cost of components and assembly. Furthermore, there is a finite selection of off-the-shelf quartz crystals, limiting the choice of operation frequency and motional resistance to that provided by commercially available crystals. Finally, the cost and size of quartz crystals greatly limits the number of frequency references available for use in the system. It would be desirable that the digital processor, the analog baseband, and the RF transceiver have the ability to use their own unique and optimized

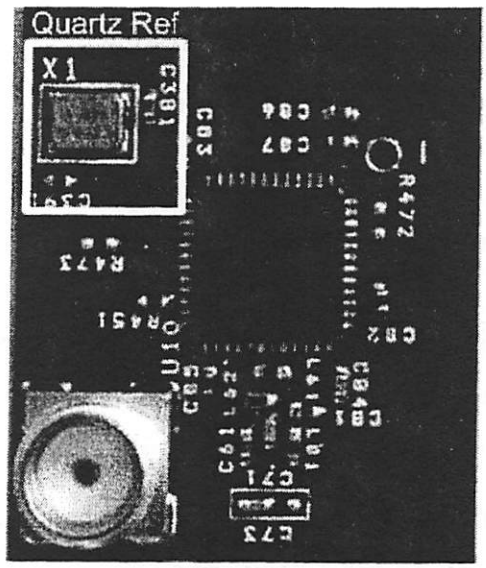


Figure 6.1: A recent wireless sensor network transceiver implementation

frequency reference. This chapter describes an effort to co-design a 16MHz MEMS resonator[1] with custom designed 0.13μm CMOS oscillators. This technology merge would allow the fabrication of very small (approximately 10000μm^2), fully integrated MEMS resonators on top of standard CMOS circuitry.

Two oscillators were designed: one optimized for low phase noise and the other optimized for low power consumption. Both include an amplitude control loop to provide a stable output amplitude at a user specified value. The low power oscillator[2] will not be discussed here. This chapter will de-

[1]Designed by Emmanuel Quévy of the Berkeley Sensor and Actuator Center (BSAC), U.C. Berkeley

[2]Designed by Nathan M. Pletcher, EECS Dept., U.C. Berkeley

scribe the design, implementation, and testing of a 100μW, low phase noise reference clock for wireless sensor networks.

6.1.1 Silicon Resonator Background

Post-processing of MEMS structures on top of CMOS using low temperature processing is possible using SiGe structural layers and Ge sacrifical layers [37]. This process has been further modified to fabricate very small electrostatic gaps. Two custom 16MHz resonators were designed and fabricated in the Berkeley Microlab Blade process [38]. This is an experimental MEMS process developed at U.C. Berkeley to allow the fabrication of narrow, high aspect-ratio gaps for efficient capacitive transduction. The process uses germanium "blades" that are defined and etched as thin as 50nm. The silicon-germanium (SiGe) structural layer is then deposited over the blades. When the sacrificial Ge blades are removed, a 50nm gap remains. A brief process outline is shown below:

- **Mask 1 - Substrate Contact:** The contact substrate to the n+ wafer is patterned and etched through a SiO_2 and Si_3N_4 barrier layer.

- **Mask 2 - Interconnect:** The 1μm Al/TiN interconnect layer is deposited, patterned, and etched. The contact substrate to the n+ wafer is patterned and etched through the SiO_2 and Si_3N_4. A 1μm resolution is possible.

- **Encapsulation:** The interconnect is encapsulated and planarized by a SiO_2 deposition / CMP step.

- **Ge Deposition:** A 2.5μm thick Ge layer is deposited (350°) along with a 0.5μm SiO_2 hardmask.

- **Mask 3 - Blade Definition:** The SiO_2 hardmask is patterned and etched, allowing etching of the Ge blade layer. This results in 50nm thick, 2μm tall Ge blades.

- **Mask 4 - Interconnect Contact:** Contacts are patterned and etched through the Ge sacrificial layer down to the Al/TiN interconnect layer.

- **SiGe Structural Definition:** The SiGe structural layer is deposited (425°) and planarized with CMP.

- **Mask 5 - Pad Formation:** Aluminum pads are deposited, patterned, and etched on the SiGe structural layer.

- **Ge Release:** The Ge is etched away, releasing the SiGe structural layer with 50nm gaps.

The use of a Ge sacrificial layer and a SiGe structural layer allows a high selectivity in the release process. To limit the SiGe gap increase to 10nm, a 40 minute release step is possible, which allows a 20μm lateral etch of the Ge sacrificial layer. A simplified process sequence is shown in Figure 6.2 [38].

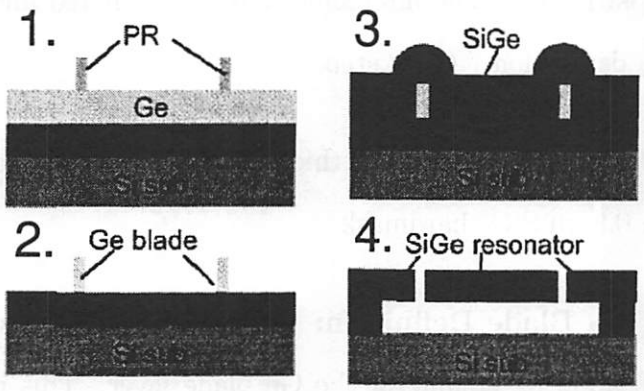


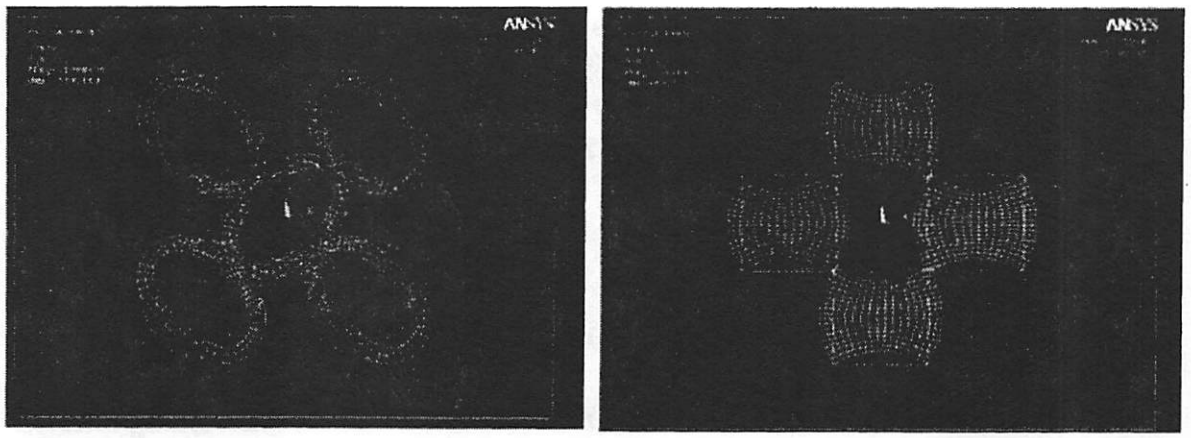
Figure 6.2: Cross-sectional process sequence

This process was used to fabricate two different 16MHz resonators. One is composed of wineglass mode rings. The other consists of Lamé mode plates. See Figure 6.3 (a) and (b) for the Ansys simulation of the two resonators.

From an electrical point of view, the series motional resistance (R_x) of the resonator is one of the most important parameters. A low R_x is desirable as this allows a low series impedance and a high parallel impedance, facilitating the design of oscillators and tuned amplifiers. For an electrostatic resonator, the motional resistance is given by Equation 6.1.

$$R_x = \frac{kg^4}{\epsilon^2 A^2 \omega^2 Q V_{bias}^2} \tag{6.1}$$

Where g is the physical electrostatic gap, A is the electrode area, ω is the natural frequency, and V_{bias} is the applied DC bias voltage. It is apparent that reducing the physical gap and increasing the DC bias voltage are the



(a) Coupled wineglass mode resonator (b) Coupled lame mode resonator

Figure 6.3: Simulation of the coupled wineglass and lamé mode resonators

most effective ways of decreasing the resonator motional resistance. Capacitively driven and sensed resonators require a DC bias voltage to increase their transduction efficiency. Varying the bias voltage allows tuning of the series resonant frequency. For a nominal bias voltage of 3.3V, the targeted resonator parameters for the wineglass mode resonator are given in Table 6.1. Due to the experimental nature of the Blade process, precise control over the

Table 6.1: Predicted resonator parameters for different achieved gaps

Parameter	50nm	100nm
C_o	1fF	1fF
L_x	0.20	3.22
C_x	482aF	30.1aF
R_x	2.04kΩ	3.27kΩ

sub-lithographic gaps is not possible in the first revision. The expected fabricated gap sizes are between 50 and 100nm. Table 6.1 provides the expected

resonator parameters for both ends of the anticipated tolerance range. The most important implication for the oscillator design is that the circuit must tolerate a motional resistance from 2kΩ to 3.5kΩ with an expected resonator Q of approximately 10,000.

6.1.2 Circuit Analysis and Design

To minimize the phase noise of the reference oscillator, the sinusoidal power exciting the resonator should be maximized. Ultimately, this power is limited by the power dissipation budget of the electronics, the acheivable voltage swing of the process used, and the linearity of the MEMS resonator transducer. To this end, the series resonant mode of the resonator was used for the low phase noise version. The series resonance presents a lower impedance to the oscillator, allowing a higher oscillator loop power for a given supply voltage. Additionally, capacitively driven and sensed resonators typically exhibit high motional resistances (>1kΩ) and extremely high (>1MΩ) parallel resistances. To avoid detuning the resonator excessively, it is easier to drive the resonator in its series mode [39]. However, driving a resonator at its series resonance requires an entirely different sustaining amplifier compared to that used for a parallel resonant oscillator. See Figure 6.4 for a conceptual oscillator diagram. In order to avoid degrading the quality factor of the mechanical resonator when driven in its series resonant mode, the resonator should be driven and sensed with a low impedance. Thus, the sustaining amplifier must present a transimpedance to the resonator. This amplifier

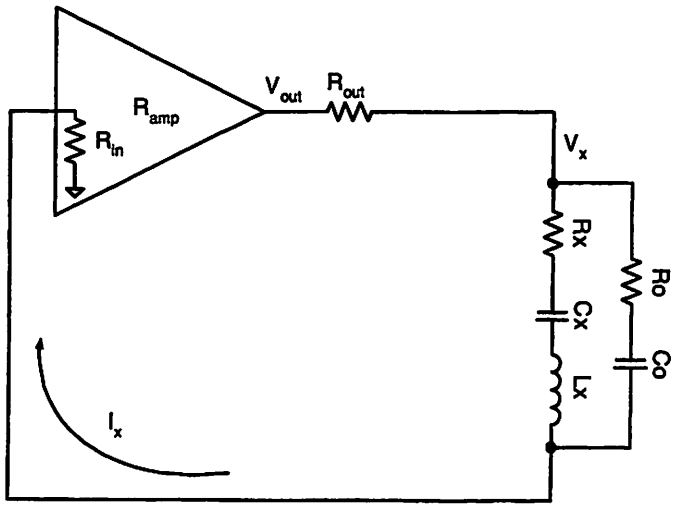


Figure 6.4: Conceptual schematic of 16MHz clock oscillator

drives the resonator with a voltage and senses the current passing through it, providing positive feedback at one precise frequency. In Figure 6.4, the amplifier sustains oscillation with a transimpedance gain R_{amp}, and exhibits a finite input and output resistance. Equation 6.2 shows the Q degradation that occurs with a finite transimpedance amplifier input/output resistance.

$$Q_{loaded} = Q_{unloaded} \frac{R_x}{R_x + R_{in} + R_{out}} \tag{6.2}$$

It can be shown that the oscillator loop gain at the series resonance of the mechanical resonator is given by Equation 6.3

$$A_L = \frac{R_{amp}}{R_x + R_{in} + R_{out}} \tag{6.3}$$

Thus, if the acceptable Q degradation is 50%, a transimpedance gain of $2R_x$ is needed. To accommodate resonator variation in Q and R_x, adjustable gain, R_{in}, and R_{out} is desirable. In addition, for stable and efficient oscillation, an amplitude control loop (ACL) is necessary.

A new oscillator circuit topology was designed to meet these requirements. See Figure 6.5 for the oscillator schematic. The oscillator consists of a transimpedance amplifier with adjustable gain, level detection circuitry, and a compensated OTA to close the amplitude control loop. The transimpedance amplifier comprises transistors M_1-M_5. The current from the mechanical resonator is sensed by the low impedance of the source of transistor M_1. The signal then undergoes amplification by a factor of $g_{m1}R_{gain}$, where R_{gain} is the effective resistance of M_{gain} in the linear operating regime. The structure formed by M_{gain}, C_{gain}, and M_3 provides an effective inductance given by Equation 6.4.

$$L_{eff} = \frac{R_{gain}C_{gain}}{g_{m3}} \tag{6.4}$$

It can also be shown that a flat load impedance (amplifier gain) of R_{gain} is achieved at frequencies over

$$f_{passband} = \frac{g_{m3}}{2\pi C_{gain}} Hz \tag{6.5}$$

Thus, for frequencies higher than $f_{passband}$, the gain of the amplifier can be controlled by adjusting the gate voltage of M_{gain}. At very large values of R_{gain}, the gain is limited by a shunting resistor (not shown). Through this

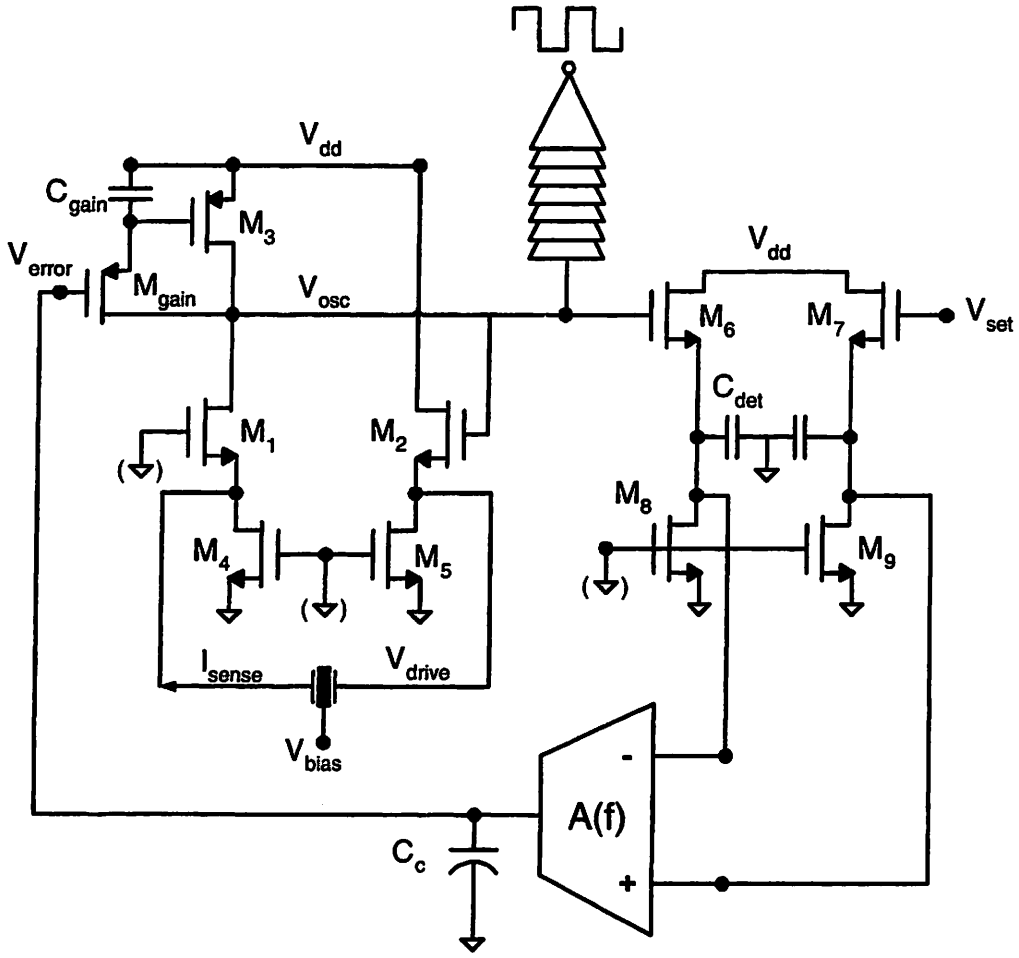


Figure 6.5: Schematic of 16MHz clock oscillator

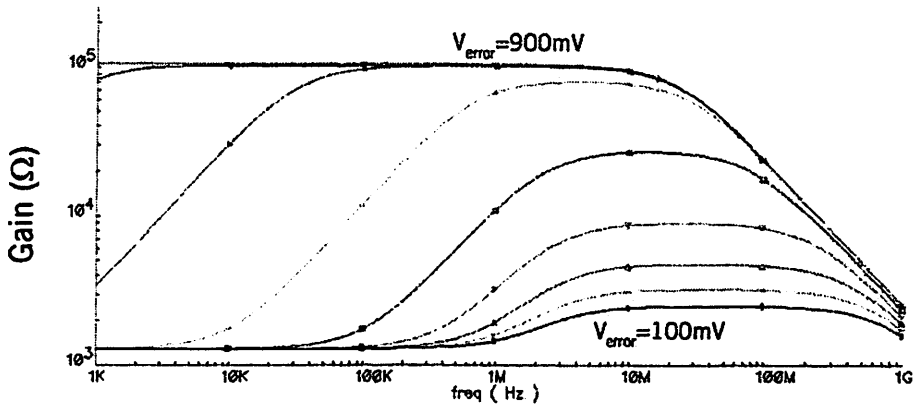


Figure 6.6: Gain (Ω) of the transimpedance amplifier

method, the maximum amplifier gain is limited to approximately 100kΩ. In this regime, maximum gain is reached at even lower frequencies. This amplified signal is buffered by the M_2, M_5 follower. Thus, the input and output impedances of the transimpedance amplifier are $\frac{1}{g_{m1}}$ and $\frac{1}{g_{m2}}$, respectively.

The proposed oscillator topology allows independent control over the input impedance, output impedance, and amplifier gain. The minimum anticipated resonator R_x was 2kΩ and the allowable Q degradation factor was set at 2. Thus, $R_{in} + R_{out} < 2k\Omega$. For moderate inversion operation of M_1 and M_2, yielding $\frac{g_m}{I_d} = 20$, the required bias current in each leg is 50μA. The gain of the transimpedance amplifier is shown in Figure 6.6. For $\frac{g_{m3}}{I_d} = 10$, and $C_{gain} = 20pF$, Equation 6.5 predicts the amplifier passband beginning at 4MHz for low gain values. This is evident in Figure 6.6. In addition, the passband clearly expands as the gain is limited by shunting conductance. The valid error voltage range, 100mV to 900mV, is determined by the out-

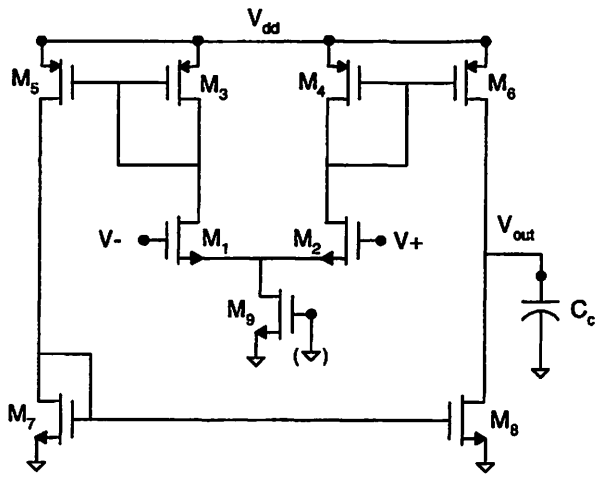


Figure 6.7: Schematic of amplitude control OTA

put swing capability of the amplitude control loop OTA. Over this voltage range, the linear resistance of the PMOS transistor M_{gain} increases. Thus, the amplifier gain varies from 2kΩ to 100kΩ, covering all possible ranges of resonator motional resistances. For the nominal value of R_{amp}=4kΩ, the required V_{error} is 300mV.

The amplitude control loop consists of a signal level detector (M_{6-9}), an OTA, an external signal V_{set}, and the resulting error signal V_{error}. See Figure 6.7 for the OTA schematic. A current mirrored OTA with a common source, non-cascoded output was the chosen OTA topology. This choice is appropriate because the loop accuracy requirements are not stringent; high OTA gain is not necessary. The non-cascoded output stage allows a large output voltage range, which is necessary to allow a large variation in the variable gain of the transimpedance amplifier. The input transconductors,

M_{1-2}, are large ($\frac{50\mu m}{0.5\mu m}$) and laid out in a common centroid configuration to minimize the offset voltage of the OTA. The open-loop DC gain of the OTA is approximately 50dB, and the circuit consumes 2μA from a 1V supply.

Although not shown in Figure 6.5, the oscillator loop is AC-coupled to the amplitude detector. The coupling circuitry has a high pass characteristic with a 1.6MHz cutoff frequency. AC-coupling allows the removal of the oscillator DC offset and pulls both detector inputs to the same default voltage. Thus, the loop defaults to a zero oscillation amplitude. To begin oscillation, V_{set} is increased above its equilibrium voltage by the desired oscillation amplitude. This increases the positive OTA input, reducing the V_{gs} of transistor M_{gain}, increasing the transimpedance amplifier gain. Thus, the loop gain of the oscillator increases. As oscillation ensues, the negative OTA terminal is driven to the same value as the positive terminal. See Figure 6.8 for the transient simulation of the oscillator amplitude control loop convergence process. Due to the initial set voltage on V+, the error signal V_{error} is driven high by the OTA. The transimpedance amplifier gain is set to its maximum value, allowing a high initial loop gain. At the onset of oscillation, V- increases to meet V+. Meanwhile, V_{error} settles to its equilibrium value with no visible ringing. Notice the relative amplitudes of the three oscillator signals V_{osc}, V_{drive}, and V_{sense}. The simulated amplitudes correspond well to calculated levels using the model in Figure 6.4. The dominant pole of the amplitude control loop is set by the resonator time constant $\frac{2Q}{\omega}$. Thus, as the quality factor of the resonator decreases, the loop stability degrades.

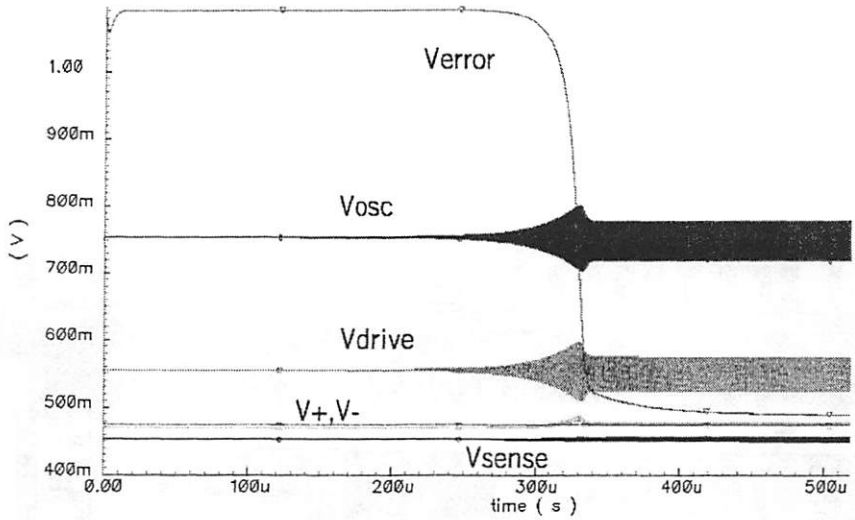


Figure 6.8: Simulation of amplitude control loop convergence

The amplitude control loop is stable down to a resonator Q of 1000. Below this value, the response time of the oscillator is fast enough to compromise the stability of the loop. The oscillator drives a seven-stage inverter chain, which was optimally sized to drive a 10pF test equipment load.

See Figure 6.9 for the CAD layout of the complete oscillator. Shown in the layout plot is a 500μm x 500μm section of the die that contains the active circuitry and the resonator flip-chip pads. The completed resonator will be flipped and bonded directly to this inner padring to avoid board parasitics. There are two drive pads, two sense pads, and two sets of ground pads to accommodate multiple mechanical resonant structures. The resonator bias pads are also shown. Although only one bias contact is necessary, two pads allow current flow through the resonator, enabling temperature compensation

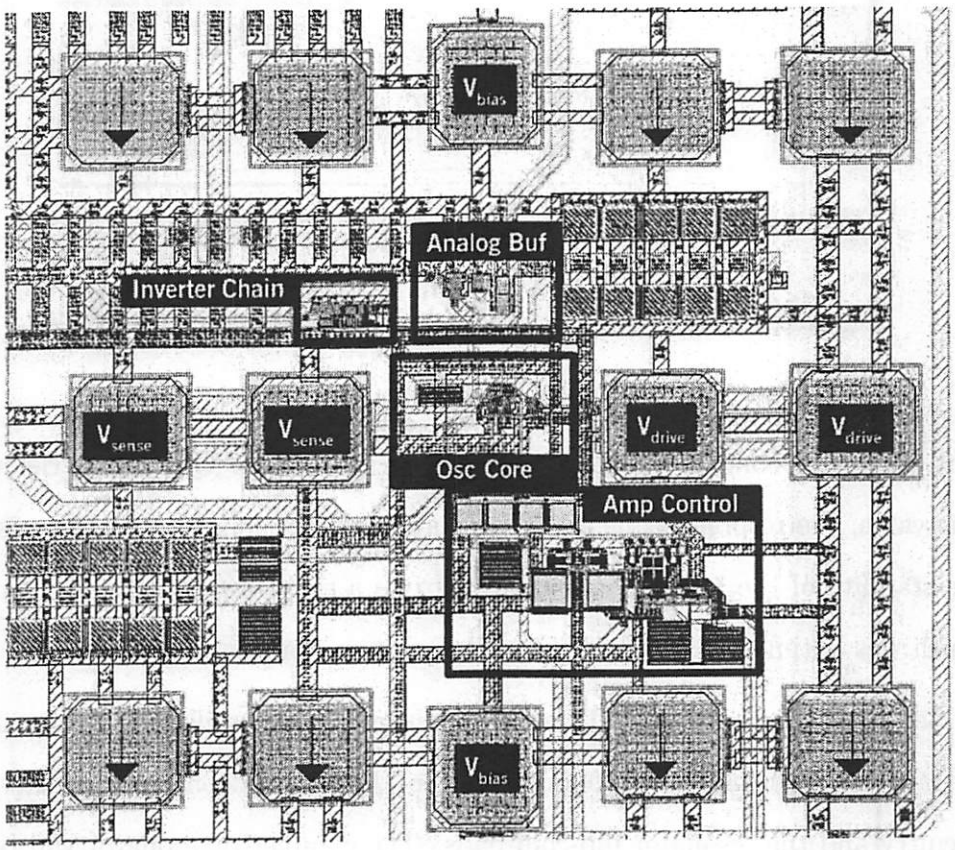


Figure 6.9: Layout of 16MHz reference clock

at the expense of dissipated power. The oscillator core is situated directly between the drive and sense pads. Visible in the amplitude control loop are the coupling capacitors, the amplitude detector, and the OTA. An analog buffer with 50Ω drive capability is included for diagnostic purposes. The oscillator consumes approximately 100μW, and the amplitude control circuitry consumes approximately 3μW.

The CMOS chips are been fabricated and initial tests performed. Basic functionality and amplitude control loop stability have been verified. Processing of the MEMS resonators is still in progress, and full oscillator characterization will proceed presently.

6.2 Flip-Chip Packaging

Packaging and assembly of the transceivers presented in Chapters 3, 4, and 5 has consisted of COB bonding on a test board. The connection of the BAW resonator to the CMOS circuitry has been accomplished through direct wirebonding of one chip to the other, as shown in Figure 4.7. Although this assembly method provides an inexpensive, sufficiently low parasitic interconnect of the resonator to the COB, more advanced packaging techniques are desirable. For example, to minimize bondwire length, the two chips must be placed in close proximity. Thus, a very sparse pad structure must be present on the perimeter of the CMOS chip. For pad-limited implementations, this requirement translates into an increased CMOS die area, which

is prohibitively expensive. In addition, as resonator technology progresses and multiple frequencies become available, even more die perimeter would be needed to realize the CMOS/resonator interconnect. Thus, it would be preferable that the resonators be flipped directly on top of the CMOS chip, allowing arbitrary placement on the chip. This methodology eliminates the need for pre-allocating space on the chip perimeter to accommodate resonator connections. In addition, the interconnect inductance would be smaller, reducing the risk of parasitic modes in oscillator or amplifier operation. To test this strategy, two prototypes were implemented. Both prototypes utilized a μ-capped (microcapped) PCM test structure from Agilent [40]. This technology allows wafer-scale hermetic packaging of BAW resonators. Thus, epoxy can be flowed under the inverted resonator without risk of damaging the delicate AlN membrane. This method uses one conductive and one non-conductive epoxy for the interconnect and mechanical support, respectively. See Table 6.2 for the relevant epoxy characteristics.

Table 6.2: Flip-chip epoxy characteristics

	Conductive	Insulating
Epoxy	H20E-PFC	U300
Resistivity ($\Omega - cm$)	$4x10^{-4}$	$1x10^{14}$
Relative permittivity	-	4.1
Dielectric breakdown	-	$17.71\frac{V}{\mu m}$

The electrical characteristics of the epoxy determine the parasitic losses and coupling that occur when the resonator is flipped onto the CMOS chip.

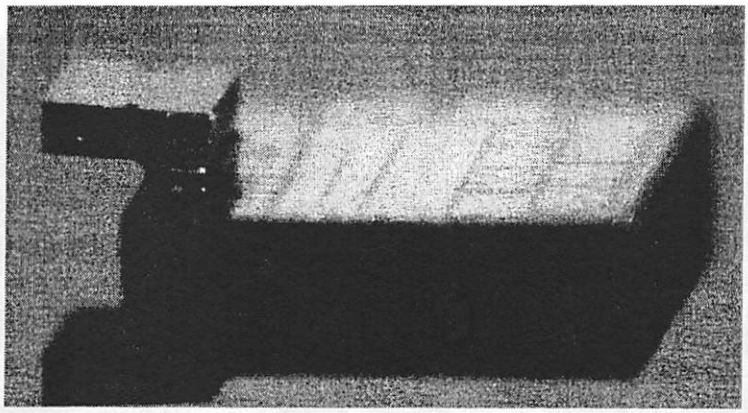
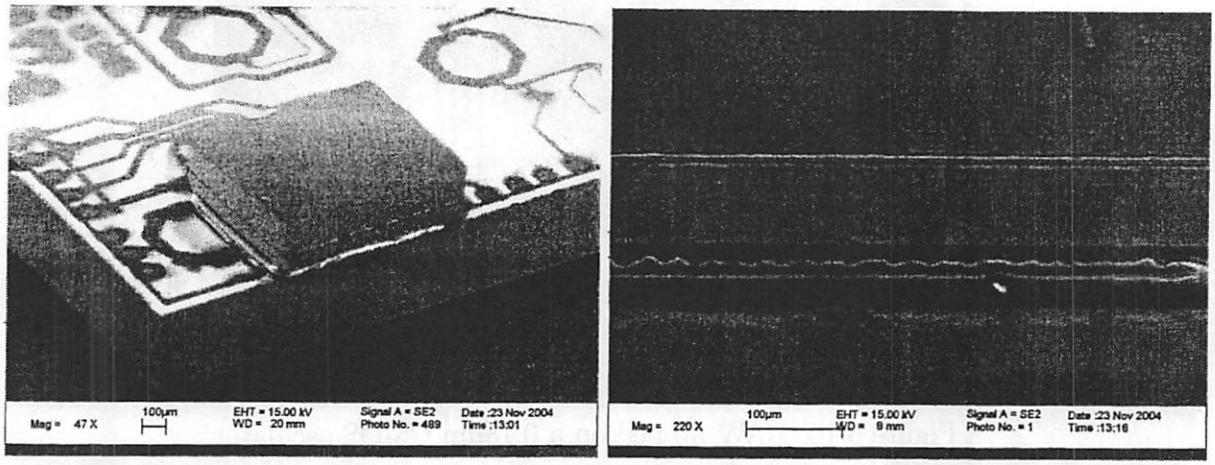


Figure 6.10: BAW flipped on a 0.18μm CMOS oscillator

6.2.1 Oscillator Flip-Chip

As a proof-of-concept, an encapsulated FBAR was flipped onto a well characterized 0.18μm CMOS oscillator presented in Section 2.3. Due to pad limitations, it was necessary to cantilever the resonator off the edge of the CMOS chip. Although this presented obvious complications for the flip-chip procedure, success with this effort would bode well for the reliable assembly of more conservative mounting orientations. The assembly process consisted of the die-level bumping of the CMOS chip with gold bondwire. Next, the FBAR chip was mechanically bonded to the bumps and non-conductive epoxy was underfilled between the chips. See the photograph of the completed flip-chip in Figure 6.10. The technique was successful, and the oscillator was functional. Direct comparison the wirebonded version was not possible since different resonator technologies were used.



(a) BAW flip-chip (b) Detail of BAW/CMOS interface

Figure 6.11: SEM image of super-regenerative flip-chip

6.2.2 Super-Regenerative Flip-Chip

To demonstrate a fully integrated, 1mm^2 receiver, a BAW resonator was flipped onto the super-regenerative receiver discussed in Chapter 4. Figure 6.11 (a) shows an SEM image of the flip-chipped system. A detailed view of the interface is shown in Figure 6.11 (b). The die-to-die distance is approximately 60μm, which is filled with *Epo-tek U-300* non-conductive epoxy.

The total thickness of the receiver is increased by a factor of less than two. The entire CMOS/BAW assembly could easily be packaged in a single, standalone unit. Aggressive use of this technique would allow placement of BAW resonators over the entire surface of the CMOS transceiver, including over the on-chip planar inductors that typically occupy much the transceiver

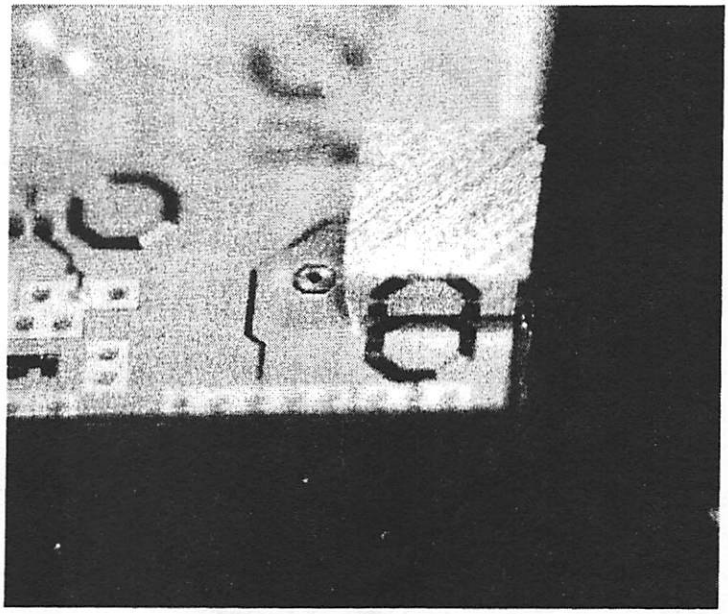


Figure 6.12: Coverage of planar inductor by BAW resonator

area. One concern is that the flip-chipped BAW die would couple to the planar inductors, decreasing the self-resonant frequencies and reducing the quality factor. To quantify the effect of this phenomenon, the input matching (S_{11}) of the super-regenerative receiver was probed with and without a BAW resonator flip-chipped over the input matching inductor. See Figure 6.12 for the coverage of the planar inductor by the BAW resonator. Approximately 40% of the 10nH inductor is directly covered by the resonator. With a typical die-to-die distance of 60μm and a *U-300* epoxy dielectric constant of 4.1, the expected coupling between the inductor and resonator is weak. Figure 6.13 quantifies the effects of the flip-chip assembly on the input match. The receiver front-end was biased to its nominal conditions. The input match

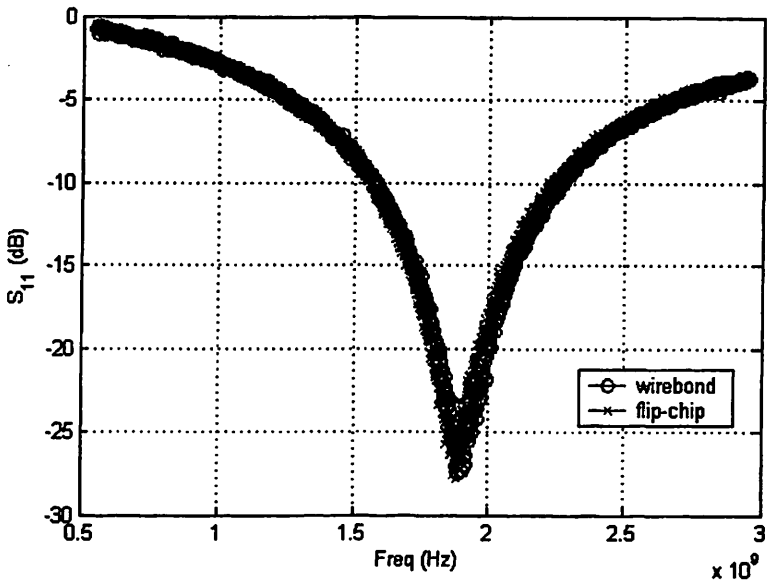


Figure 6.13: Super-regenerative S_{11}: Effect of flip-chip proximity on planar inductors

was measured with a *Cascade ACP* GSG probe and an *HP 8719* Network Analyzer. In the implementation where the BAW resonator is wirebonded to the CMOS die, the S_{11} peak is -27.5dB at 1.894GHz. For the receiver with the flip-chipped resonator, the S_{11} peak is -27.8dB at 1.891GHz. The input match frequency shift of 0.16% is negligible, indicating little loss in performance if planar inductors are covered by a flip-chipped resonator. These results are summarized in Table 6.3.

Table 6.3: Input matching performance of flip-chip vs. wirebonded die

Assembly	Measured S_{11} peak	Frequency
wirebonded	-27.5dB	1.894GHz
flip-chip	-27.8dB	1.891GHz

The direct flip-chipping of BAW resonators onto CMOS die provides a high performance, robust, easy to package option for the implementation of fully integrated transceivers.

6.3 Conclusions

New applications like peer-to-peer wireless sensor nodes and implantable electronics demand extremely small and inexpensive electronics. These systems demand a paradigm shift in packaging techniques. Multi-layer printed circuit boards with surface-mount components are too bulky for these applications. Components like quartz crystal resonators are much larger than the actual CMOS chips. This chapter described the design of a reference clock using

SiGe MEMS resonator to replace quartz crystals. In addition, advanced packaging techniques to directly bond BAW resonators to the CMOS chips were investigated.

Chapter 7

Conclusions

The field of wireless sensing holds the potential to greatly change the way we live. Pushing these devices to smaller, cheaper, and more functional implementations greatly increases the scope of their application. However, there are huge technological challenges in making this visions a reality. This thesis has discussed technologies and methodologies for overcoming these obstacles.

Implementation of the RF transceiver is the biggest challenge in the realization of energy scavenging sensor networks. The transceiver must consume very little power (less than 1mW), be fully integrated, and exhibit a very rapid start-up time. These requirements are in direct conflict with each other. To overcome these tradeoffs, emerging RF MEMS technologies were investigated. These devices are shown to greatly reduce the complexity and power consumption of low datarate transceivers.

An RF MEMS/CMOS co-design methodology was developed that allows the simultaneous optimization of the CMOS active devices and the MEMS

components. Multiple proof-of-concept circuit blocks were developed and tested to verify these concepts. These include a single-ended Pierce oscillator and a new differential oscillator topology. With these devices, it was possible to demonstrate a self-contained energy scavenging transmit beacon. This device continues to operate on scavenged energy after over two years of operation.

The proposed methodologies were successful, and built the foundation for the next step: designing a wireless link based on these principles. An architecture exploration was performed, and two prototype transceivers were implemented and tested. The first was a tuned RF architecture. This architecture takes advantage of the array capability of RF MEMS devices, and is scalable to multiple discrete channels. The second was a super-regenerative receiver. This receiver achieves well below state-of-the-art power consumption by employing MEMS resonators and subthreshold CMOS design techniques. A fully integrated, (1 x 2)mm^2 transceiver was developed. For both transceivers, an indoor 20m wireless link was demonstrated to verify robust operation. These transceivers can be directly applied to various wireless sensing scenarios. The methodologies presented in this thesis can be applied to the design of other communications systems. As an example, the design of a communication link for an ultra-dense sensor network ($> 10\frac{nodes}{m^2}$) would greatly benefit from these techniques.

The benefits of MEMS/CMOS co-design techniques are not only limited to the transceiver. For example, these devices can be used to replace

quartz crystals as the system time base. This is advantageous because quartz crystals are bulky and available only with discrete frequency and impedance values. To tackle this challenge, an interdisciplinary project was completed to co-design a 16MHz electrostatic resonator with custom CMOS oscillators. This greatly reduces the form factor of the system reference clocks.

Although the techniques in this thesis were designed with an eye towards wireless sensor networks, they can certainly be extended to other circuits and systems in many application spaces. As RF MEMS technologies mature, they will be more reliable, more fully integrated, and handle more power. The maturity of these technologies will open up a new dimension of circuit design.

Bibliography

[1] J. Whitehead, *Super-Regenerative Receivers.* Cambridge Press, 1950.

[2] S. Roundy, *Energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion.* PhD thesis, University of California, Berkeley, May 2003.

[3] J. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, and T. Tuan, "Picoradios for wireless sensor networks: The next challenge in ultra-low power design," *IEEE ISSCC Digest of Technical Papers*, pp. 200–01, Feb 2002.

[4] J. Kao, S. Narendra, and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques," *Proceedings of IEEE/ACM International Conference on Computer Aided Design*, pp. 141–148, 2002.

[5] L. Zhou, J. Kahn, and K. Pister, "Corner-cube retroreflectors based on structure-assisted assembly for free-space optical communcation," *IEEE J. Microelectromechanical Systems*, vol. 12, pp. 233–242, June 2003.

[6] A.-S. Porret, T. Melly, D. Python, C. Enz, and E. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: architecture and receiver," *IEEE J. Solid-State Circuits*, vol. 36, pp. 452–66, Mar 2001.

[7] V. Peiris *et al.*, "A 1V 433/868MHz 25kb/s-FSK 2kb/s-OOK RF Transceiver SoC in standard digital 0.18μm CMOS," *IEEE ISSCC Digest of Technical Papers*, p. 258, Feb 2005.

[8] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," *IEEE Custom Integrated Circuits Conference*, 2004.

[9] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak-inversion operation," *IEEE J. Solid State Circuits*, vol. 12, pp. 224–231, June 1977.

[10] N. Pletcher, "Micro Power Radio Frequency Oscillator Design," Master's thesis, University of California, Berkeley, Dec 2004.

[11] B. Bircumshaw *et al.*, "The radial bulk annular resonator: Towards a 50ohm RF MEMS filter," *12th Int. Conf. on Solid State Sensors, Actuators and Microsystems*, vol. 35, pp. 875–878, June 2003.

[12] K. Lakin, "Thin film resonators and high frequency filters," *http://www.tfrtech.com*, June 2001.

[13] B. Otis and J. Rabaey, "A 300μw 1.9GHz CMOS oscillator utilizing micromachined resonators," *IEEE J. Solid State Circuits*, July 2002.

[14] S. Sheng and R. Brodersen, *Low-Power CMOS Wireless Communications.* Kluwer, 1998.

[15] J. Smith, "High density, low parasitic direct integration by fluidic self-assembly (FSA)," *Dig. IEEE International Electron Devices Meeting*, pp. 201–204, 2001.

[16] R. Ruby, P. Bradley, J. L. III, Y. Oshmyansky, and D. Figueredo, "Ultra-miniature high-Q filters and duplexers using FBAR technology," *IEEE ISSCC Digest of Technical Papers*, pp. 120–21, Feb 2001.

[17] B. Otis, "The Design and Implementation of an Ultra Low Power RF Oscillator using Micromachined Resonators," Master's thesis, University of California, Berkeley, Dec 2002.

[18] G. Chien and P. Gray, "A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1996–99, Dec 2000.

[19] Q. Huang and P. Basedau, "Design considerations for high-frequency crystal oscillators digitally trimmable to sub-ppm accuracy," *IEEE Trans. on VLSI Systems*, vol. 5, pp. 408–16, Dec 1997.

[20] E. Vittoz, M. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: theory and application," *IEEE J. Solid State Circuits*, vol. 23, pp. 774–83, June 1988.

[21] K. Kwok and H. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 652–660, 3 2005.

[22] N. Pletcher and J. Rabaey, "A 100μW, 1.9GHz oscillator with fully-digital frequency tuning," *Submitted: Proceedings of the IEEE ESSCIRC*, 2005.

[23] D. Ruffieux, "A high-stability, ultra-low-power differential oscillator circuit for demanding radio applications," *Proceedings of the IEEE ESSCIRC*, pp. 85–88, Oct 2002.

[24] J. Larson and Y. Oshmyansky, "Measurement of effective k_t^2, Q, Rp, Rs vs. temperature for Mo/AlN FBAR resonators," *IEEE Ultrasonics Symposium*, 2002.

[25] S. Roundy, B. Otis, Y. Chee, J. Rabaey, and P. Wright, "A 1.9GHz RF transmit beacon using environmentally scavenged energy," *Proceedings of the ISLPED*, Sept 2003.

[26] B. Otis, Y. Chee, R. Lu, N. Pletcher, and J. Rabaey, "An ultra-low power MEMS-based two-channel transceiver for wireless sensor networks," *Proceedings of the IEEE VLSI Symposium*, June 2004.

[27] R. Lu, "CMOS low noise amplifier design for wireless sensor networks," Master's thesis, University of California, Berkeley, Dec 2003.

[28] R. Meyer, "Low-power monolithic RF peak detector analysis," *IEEE J. Solid State Circuits*, vol. 31, Jan 1995.

[29] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. Elec. Devices*, vol. 44, Mar 1997.

[30] E. Armstrong, "Some recent developments of regenerative circuits," *Proc. IRE*, vol. 10, pp. 244–260, Aug 1922.

[31] N. Joehl, C. Dehollain, P. Favre, P. Deval, and M. Declercq, "A low-power 1-GHz super-regenerative transceiver with time-shared PLL control," *IEEE J. Solid State Circuits*, vol. 36, pp. 1025–1031, July 2001.

[32] A. Vouilloz *et al.*, "A low-power CMOS super-regenerative receiver at 1GHz," *IEEE J. Solid-State Circuits*, vol. 36, pp. 440–451, Mar 2001.

[33] B. Otis, Y. Chee, and J. Rabaey, "A 400μW Rx, 1.6mW Tx super-regenerative transceiver for wireless sensor networks," *IEEE ISSCC Digest of Technical Papers*, p. 396, Feb 2005.

[34] A. Zverev, *Handbook of filter synthesis.* Wiley, 1967.

[35] F. Moncunill, O. Mas, and P. Pala, "A direct-sequence spread-spectrum super-regenerative receiver," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. I–68–I–71, May 2000.

[36] Motiv, "Moteiv website," *http://www.motiv.com*, 2004.

[37] A. Franke, T.-J. King, and R. Howe, "Post-CMOS modular integration of poly-SiGe microstructures using poly-Ge sacrificial layers," *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 18–21, June 2000.

[38] H. Takeuchi, E. Quevy, S. Bhave, T.-J. King, and R. Howe, "Ge-blade damascene process for post-CMOS integration of nano-mechanical resonators," *IEEE Electron Device Letters*, 2004.

[39] C. Nguyen and R. Howe, "An integrated CMOS micromechanical resonator high-Q oscillator," *IEEE J. Solid State Circuits*, vol. 34, pp. 440–455, Apr 1999.

[40] R. Ruby, P. Bradley, and J. L. III, "FBAR microcap technology," *IEEE ISSCC Digest of Technical Papers*, Feb 2002.