Enabling Technologies for Organic Memories

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ORGANIC MEMORIES

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ABSTRACT

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A series of advances in organic memory technology is demonstrated that enable an entirely new low-cost memory technology. We investigate the optimization and structural design of organic transistors that are to be used in addressing circuitry. We overcome previous limitations in organic circuit density through the use of electron-beam lithography and special water-soluble resists. Finally, we incorporate these advances with the first-ever organic antifuse. We present this novel memory technology to be utilized in a three-dimensional one-time-programmable (3D-OTP) nonvolatile storage array. Without the prohibitive costs of silicon processing, this memory is capable of setting cost points several orders of magnitude lower than their inorganic counterparts. We have also successfully integrated this technology onto flexible plastic substrates, enabled by our low processing temperature (<100C). Combined with stacking, these vertical memory elements can create ROM densities denser than many inorganic memories, at a fraction of the cost.

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GLOSSARY AND ABBREVIATIONS

Antifuse. A two terminal memory device that is composed of a diode and capacitor in series. The device is programmed by the breakdown of the dielectric within the capacitor.

FPGA (field programmable gate array) An array of devices that can be interconnected in custom ways via the application of voltages.

MIM (metal-insulator-metal) A capacitive structure often used in field-programmable gate arrays

ONO (oxide-nitride-oxide). An antifuse dielectric stack common in commercial antifuses in field-programmable gate arrays.

OTFT (organic thin film transistor). A three-terminal electronic device in which a gate terminal controls conduction of current between the source and drain terminals through a thin layer of organic semiconducting material.

RFID (radio frequency identification). A system of wireless communication between a reader and a tag, where data is transmitted through inductively coupled signals.

Chapter 1: INTRODUCTION

The idea of ubiquitous computing is extremely attractive. The idea of electronics integrated into everyday items is extremely attractive, but currently well beyond the cost structure inherent to silicon chips. From integrated displays to radio-frequency identification, silicon solutions remain economically out of reach due to high material costs, processing costs, and the need for clean-room fabrication. In essence, a significant paradigm shift is necessary to enable electronics to be cheaply built in to everyday items.

Through reel-to-reel processing, where devices are fabricated through the solution deposition of materials, ultra-low cost points can be achieved. Without the need for vacuum processing, lithography, or clean rooms, reel-to-reel processing can facilitate reducing the costs of low-performance electronics by several orders of magnitude. Organic semiconductors are generally associated with the reel-to-reel process due to their ability to be deposited from solution, and their ability to produce acceptable transistor active layers. The combination of these technologies has created excitement, as their joining has enabled prototyping of low-cost devices. Both of these topics are directly explored in Chapter 2. This chapter also explores the background of the largest target application for low cost electronics, radio-frequency identification tags (RFID).

Within the scope of low-cost RFID, a key component is the memory circuit responsible for the unique identity of each individual tag. This work focuses on the two key components of the memory needs of low-cost RFID: the nonvolatile memory element and the memory

addressing array. Through stacking, vertical memory density is explored, which may enable this technology to break into other low-cost memory applications.

For the addressing technology, Chapter 3 investigates the optimization and stability of the organic transistors used. By examining the effects of environmental contamination and recovery, as well as the effect of surface treatments, this chapter identifies ways to improve transistor performance and develops understanding into the degradation mechanisms.

Another important need for organic memory addressing arrays – electrical isolation – is addressed in Chapter 4. Through two separate techniques, the beneficial effects of transistor isolation are demonstrated. By establishing isolation technology, the individual organic transistors can be placed in much closer proximity while limiting cross-talk between devices. This effort enables tighter pitching of the addressing arrays, saving lateral area and material costs.

Individually gating the organic transistors is also necessary for addressing arrays, and is demonstrated in Chapter 5. Combining this need with a process that is vertically stackable and below the thermal budget of low-cost plastic substrates is crucial. The development of the process, as well as the electrical characteristics of the resultant devices is examined.

In the second thrust of the thesis, a novel nonvolatile memory element is created that is fully compatible with a low-cost reel-to-reel fabrication system. The background for this device, the organic antifuse, is given in Chapter 6. The physical operation of this device is explored, as well as the factors limiting the scaling of the memory array sizes. Performance metrics for antifuses are also identified.

The background work for the construction of organic antifuses is the focus of Chapter 7. The construction of discrete capacitors and diodes is used to explore materials and processes compatible with the complete antifuse fabrication procedure. These processes are combined in the latter parts of the chapter in the creation of the first-ever organic antifuse.

With the process targeted for integration into reel-to-reel processing, demonstration of the nonvolatile memory technology using plastic substrates is illustrated in Chapter 8. Issues involving surface roughness, device yield, and array structure are explored. The technology is also progressed, as complete 100 bit memory arrays are demonstrated, rather than the discrete disconnected devices of Chapter 7. Complementary antifuse structures are also developed to investigate the plausibility of memory stacking.

Finally, Chapter 9 demonstrates the two-layer vertical stacking of organic antifuse arrays on plastic substrates. The high-speed programming of these organic antifuses is also explored to determine the relative performance of these devices to other memory systems. The future goals for this research thrust are identified, as well as a brief view into the variety of potential applications for a low-cost vertically stacked nonvolatile memory system built on flexible plastic substrates using reel-to-reel fabrication technology.

Chapter 2: BACKGROUND ON ORGANIC ELECTRONICS

In recent years, there has been great interest in organic semiconductor devices, driven by their potential use in low-cost flexible displays and disposable electronics applications [1][2]. As a whole, organic materials allow electronics to be economically feasible for niches out of reach for their silicon-based counterparts. In particular, there exists great potential in soluble organic semiconductors, since these may potentially be used to form low-cost all-printed circuits [3] by eliminating the need for many of the major semiconductor-manufacturing cost points, including lithography, physical and chemical vapor deposition, plasma etching, and the waste management costs associated with subtractive processing. In addition, the electrical performance of organic devices rivals that of α-Si thin film transistors [4], making them suitable for a broad range of applications. The major focus points of organic-based electronics to date include chemical sensors (wherein device performance varies when exposed to certain liquids or gases) [5][6], displays and the pixel addressing circuits [7][8], and in the creation of RFID tags [9], which aim to replace conventional barcodes.

2.1 Conduction in Organic Semiconductors

Organic semiconductors operate under conduction mechanisms that are vastly different from inorganic semiconductors such as silicon. In silicon, the atoms are bonded through strong covalent bonds, and band-transport dominates. On the other hand, organic molecules are weakly bonded to one-another through van der waal bonds. Within each semiconducting organic molecule are chains of alternating single and double bonds. By definition, these are conjugated molecules, which results in electrons residing within pi-orbitals orthogonal to the plane of the molecule. When multiple molecules are placed in close proximity, overlapping of

the pi-orbitals occur, enabling the transport of electrons between molecules. As a result, the degree of molecular packing and alignment can play a large role in the ease of electron transport. The result is that organic films can operate in many different modes, depending on order and defect density, which has resulted in the development of many competing charge-carrier transport models [10]. The common thread within these theories is that the overlapping pi-orbitals form delocalized states, resulting in the formation of a highest occupied molecular orbital (HOMO) energy band and a lowest unoccupied molecular orbital (LUMO) energy band. In devices, these bands act similarly to the valance and conduction bands of inorganic crystals.

In highly purified organic crystals band transport is observed, rendering room temperature mobilities in the range of 1 to 10 cm^2/Vs. In the other extreme, electron-hopping transport is observed in amorphous organic films. Since hopping is thermally activated process, the mobility of these devices is generally dependent on temperature and electric field [11]. Within these molecular conduction mechanisms, trap-limited transport models can be used to explain carrier generation under applied bias [12]. In this process, the mobility is gate-bias dependent. At low biases, nearly all generated charge is relegated to reside in localized trap states, and does not aid in conduction. As larger biases move the Fermi level closer to the delocalized band, the vast majority of the traps become filled, and newly generated carriers are injected directly into the delocalized levels [12]. As the carriers in delocalized levels assist in conduction, mobility drastically increases with applied bias. With this knowledge of transport in organic semiconductors, films can be designed to create optimized electrical characteristics for use in field-effect transistors (FETs), diodes, and other devices.

2.2 Radio Frequency Identification (RFID)

A specific target application for low-cost organic devices is the radio frequency identification tag (RFID). These passive devices could be used on commercial products to assist in tracking, inventory control, and theft prevention. RFID chips require less human manipulation to read, and contain far more data than bar codes. Since RFID systems allow tags to be read at a distance, they can expedite in-store check-out, and control warehouse inventory with little human supervision. Each RFID tag transmits a specific signal to the outside world when activated, which can contain precise information about the tag, and the product on which it resides.

2.2.1 RFID Technology

RFID can excel as a technology only when all of the individual system components operate seamlessly. While the development of RFID tags receives significant attention, it is also important to understand the role of the RFID support structure illustrated in Figure 2.1. In a local environment, the reader produces a signal that interrogates all RFID tags in range. When each tag responds with its unique 128 bit identification, the reader is responsible for collecting the returned signal through its antenna. Then, on a local front-end computer, the discrete tag signals are separated through anti-collision software, and the 128-bit code is checked for integrity through check-sums and headers. The application bits generated from each tag are then queried in the back-end computer database to identify information about the product on which the tag is attached. In the case of inventory control, this database is developed by the product manufacturer, so that queried tags can give location information for each tagged product. Because of the complexity of the system, reader costs, front-end computing, and back-end database management present significant costs the implementation of RFID

technology. However, this distribution of cost is largely intentional in order to reduce the cost and complexity of the most numerous system component – the RFID tag.

As a single reader is expected to read hundreds or thousands of tags, and back-end databases are suspected to support hundreds or thousands of readers, a low-cost tag design is vital. With this in mind, the simple RFID tag implementation shown in Figure 2.2 illustrates the basic tag components. First, the tag is responsible for inductively coupling to the reader with its antenna to collect the signal. The collected signal is passed through a high-frequency diode, and then through a low-pass filter to generate a DC power supply for the digital logic, eliminating the need for on-chip power generation. The original collected signal also provides the clock for the digital logic, where the operational frequency can be stepped down to be compatible with organic TFTs. The digital logic itself is comprised of two main components – the nonvolatile memory array and the output shift register. At the proposed digital clock frequency of 110kHz, organic TFTs can be fairly readily produced. On the other hand, the memory array is a far larger challenge for low-cost RFID. Finally, the digital logic is responsible for serially outputting the contents of its nonvolatile memory to the antenna, transmitting a signal to the reader.

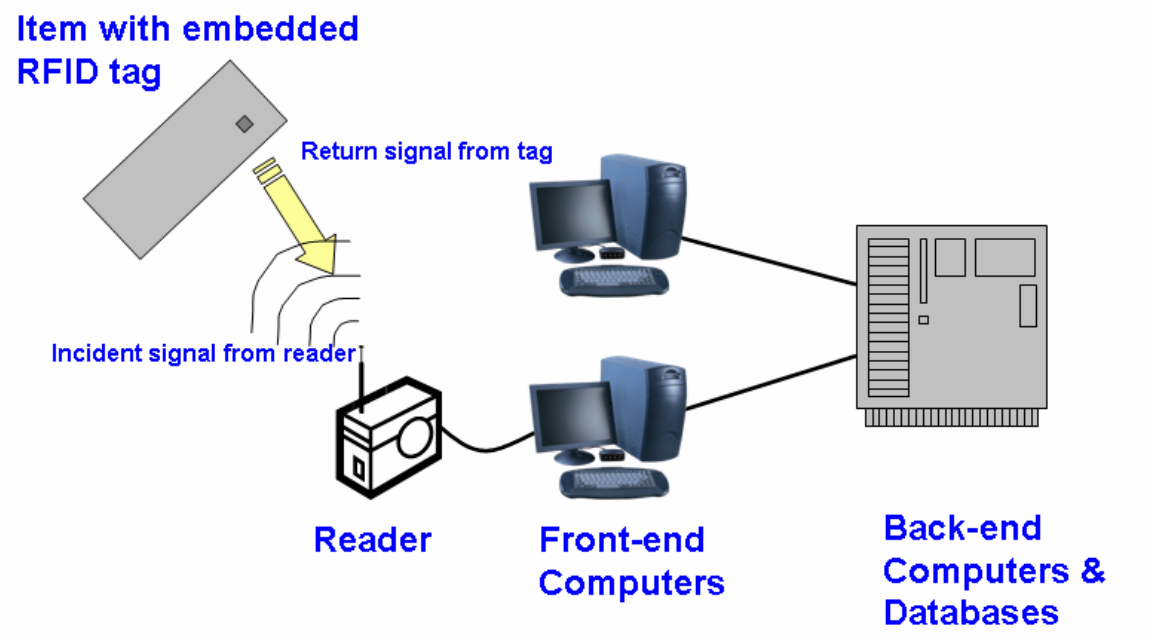

Figure 2.1: The complete RFID system environment.

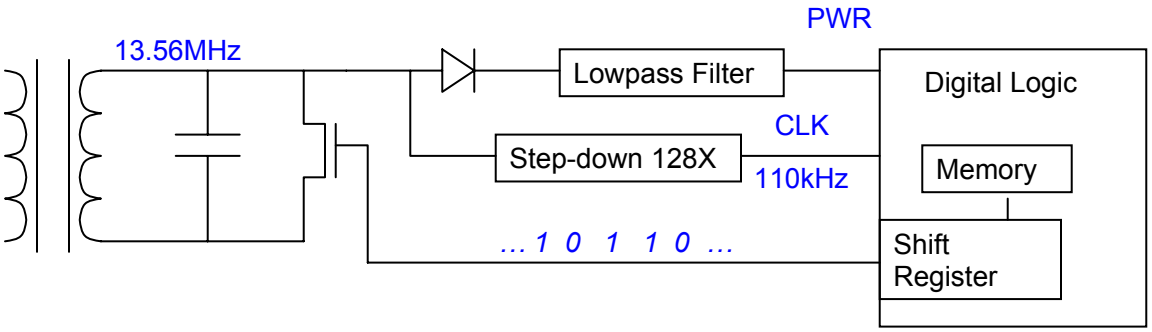

Figure 2.2: Internal circuit structure of an RFID tag.

2.2.2 The Mu Chip

To facilitate an understanding of RFID system issues, it is worthwhile to consider an archetypal silicon-based RFID tag, the Mu chip, first introduced by Hitachi in 1998. The device was originally designed to be inserted into currency to prevent counterfeiting, but the

capability of the chip to assist in inventory control became immediately evident. The 2.45Ghz Mu Chip was first introduced as a die about 0.4mm × 0.4mm in area and 0.1mm thick, and contained an identification string of 128 bits. The extremely small form factor, as seen in Figure 2.3 enables the RFID tag to be integrated into paper products. However, the real motivation for the small dimensions is the reduction in material costs. In fact, the initial Mu Chip dies were produced at $0.05 each. At this price point, it was perceived that Hitachi's invention had ushered in the era of "disposable silicon." However, the small size of the Mu Chip has direct drawbacks. On this scale, the effective range of the device is on the order of millimeters, which questions its value over traditional barcodes, whose read range is on the scale of inches. To compensate, the Mu Chip was integrated with an external antenna to increase its range to several meters. The antenna assembly is on the order of 3 inches, and is pictured in Figure 2.4.

On a cost analysis, the need for an external antenna dramatically decreases the possible applications for the Mu Chip. With a total silicon area of 0.16mm^2, the cost of producing the Mu Chip die is on the order of one cent. Likewise, producing the external antenna is on the order of one cent. However, providing electrical connections between the two, as well as providing packaging for the system, has proven to cost approximately 17 cents [13].

As a result of Hitachi's success, inorganic RFID chips have already been implemented in the palette-level tracking of goods for over 100 independent Wal-Mart suppliers. They have also been widely accepted in the tracking of cattle, providing crucial information in the tracking of livestock diseases. However, the cost associated with silicon-based RFID tags limits their ability to penetrate the item-level tracking market. Also, while the use of high frequencies (900MHz or 2.4GHz) decreases the chip area consumed by inductors and capacitors, the

signal is more readily absorbed by liquids and metals. This means that the range can be significantly decreased and line of sight may be necessary, which reduces the advantages of RFID over the UPC barcode. Thus, large-area, low-frequency devices would be preferred for item-level tracking. To reach this market, the cost of large-area integrated RFID chips must be greatly reduced.

As mentioned above, the cost of producing the silicon RFID component is minimal, and the primary costs are associated with packaging and assembly. While the assembly cost can be reduced through the use of techniques such as fluidic self-assembly [16], improvements are limited and slow in developing, and all silicon chips in the market currently utilize conventional pick-and-place technologies [17]. Thus, unlike many other silicon technologies, further improvements in device scaling will not significantly reduce cost points, and the price scaling of silicon RFID tags is expected to be slow.

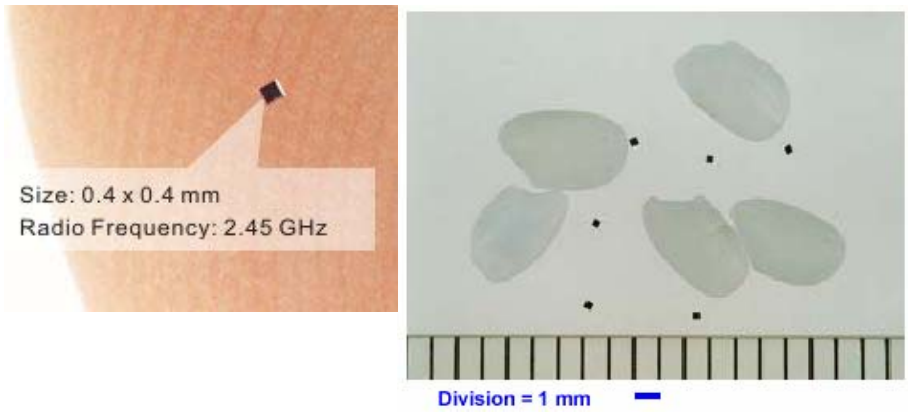

Figure 2.3: Hitachi's Mu Chip on a human finger (left) and next tograins of rice (right) [13].

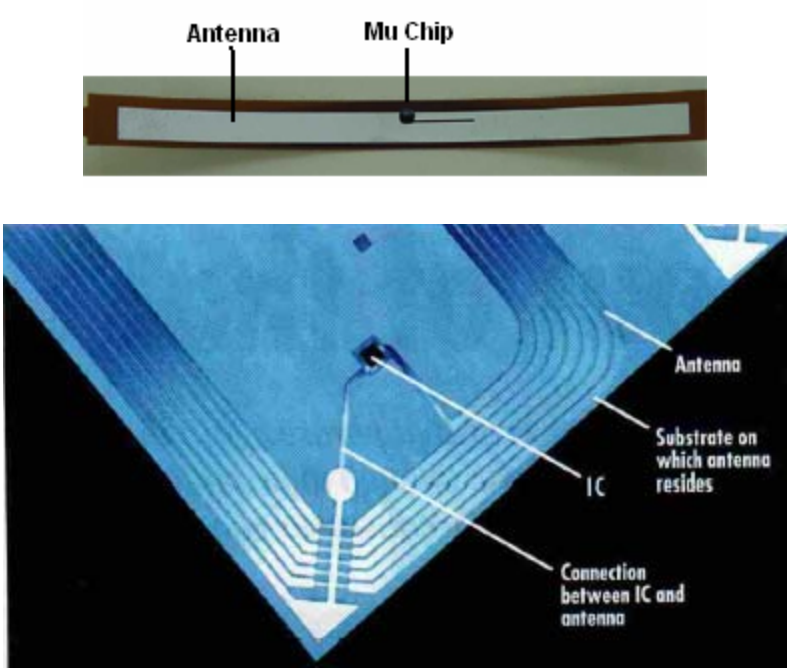

Figure 2.4: External antennas used to increase the range of the Mu Chip [16].

2.3 Reel-to-reel Fabrication

An innovative alternative pathway to reduce RFID costs is to eliminate the silicon substrate completely, and produce RFID on the same flexible plastic substrate as the antenna. If the antenna and chip are built on the same low-cost substrate, attachment costs are removed. Cheap substrates also allow large antennas to be employed, enabling lower frequencies and increasing RFID penetration through metals and liquids.

The most ambitious approach for producing low-cost item-level RFID is fully-printed organic electronics. As opposed to silicon processing, the process for making all-printed organic circuits is fully additive. That is, lithographic patterning steps and film etching costs are directly removed from production costs. Also, if all layers of the circuit are printed, vacuum deposition processes can also be eliminated, further reducing costs. By combining the

technology of fully-printed organic circuits with flexible substrate technology, ultra-low costs are achieved on what is dubbed a "reel-to-reel" system.

2.3.1 System Basics

In the reel-to-reel system, illustrated in Figure 2.5, the complete fabrication of the organic circuits is accomplished on a track-like system. During the procedure, the source plastic substrate resides on a large spindle, pictured to the left in Figure 2.6. This roll is unwound during the process, and the plastic surface passes underneath several deposition stages. Each stage is responsible for the deposition of a device layer through a solution printing process such as inkjet, screen-printing, or gravure. In this process, the deposition source is responsible for lateral pattern control, while the reel motion is responsible for advancing the substrate in-line. This is similar to the operation of a commercial inkjet printer, where the print head moves across the sheet, and the paper feed controls the rate at which the sheet passes underneath the head. Finally, the substrate can be rolled at the destination spindle. Once the process is complete, the spindle can be removed, and the individual dies can be cut, separated, and packaged for use. An example of a commercial reel-to-reel system is shown in Figure 2.6.

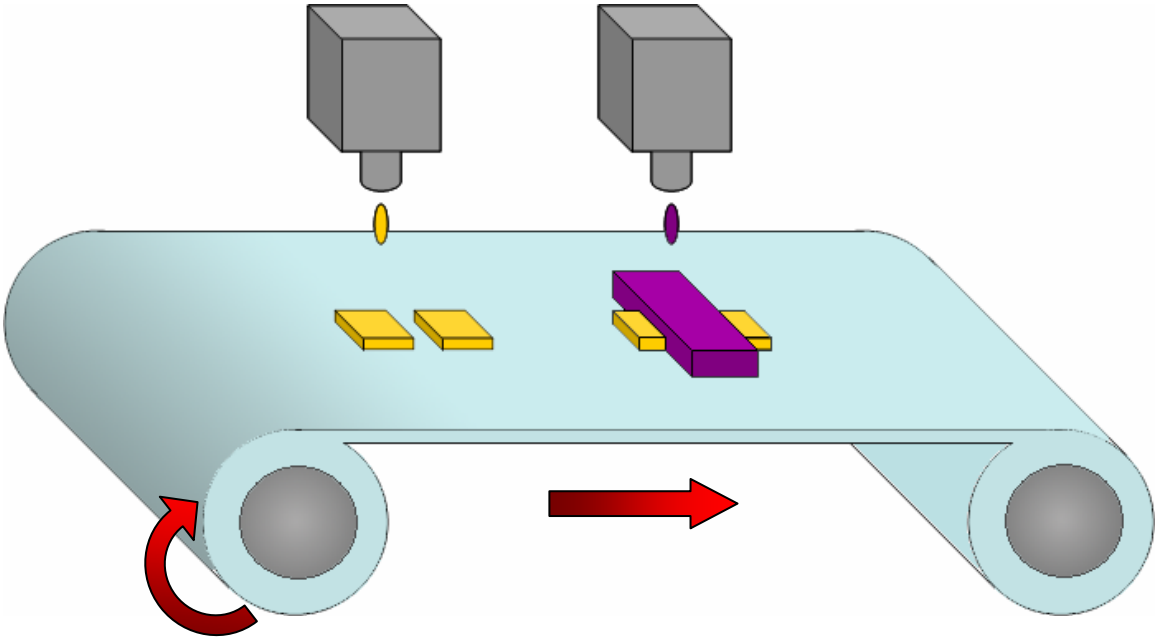

Figure 2.5: Reel-to-reel system for printing organic circuits.

Figure 2.6: Commercial reel-to-reel printer by PolyIC.

In a reel-to-reel system the number of deposition stations employed has no fundamental limit, enabling the creation of complex devices with many discrete layers. Moreover, a reel-to-reel system is capable of producing endless stacks of organic devices, enabling vertical circuit density. Previously, vertical stacking was only possible in structures utilizing amorphous silicon [18], which still required expensive vacuum processing. Despite the highlighted printing methods having resolutions in the range of 5µm to 20µm, it is possible to obtain the same lateral device density as high-end silicon processing through vertical stacking.

2.3.2 Material Developments

Although the performance of the organic active layer receives the majority of attention in literature, the reel-to-reel process is strongly supported by the development of printed metal lines. Early work focused on printing conductive polymers to serve as device electrodes [19][20]. This work generally focused on polyaniline (PANI) and poly(3,4)ethylenedioxythiophene doped with polystyrenesulfonate (PEDOT/PSS). Under ideal printing conditions, PANI was able to demonstrate conductivites of 8.5S/cm [20]. In that work, vast conductivity gains were realized with the use of lower PANI viscosities, also resulting in smoother films. Meanwhile, PEDOT has demonstrated conductivities up to 51S/cm [21]. As seen in Figure 2.7, the capabilities of the PEDOT material depend widely on the solvent ratios and deposition method. While these results are favorable for a polymer film, much higher conductivities are required for RFID. To collect large amounts of power the antenna inductor and capacitor are generally quite large, and the quality factor (Q) of the tag is limited by series resistance. At these conductivities the range of the RFID range would be limited to single millimeters.

Sample description	Thickness (nm)	Roughness (nm)	Conductivity (S/cm)
Inkjet Printed PEDOT	350	8-10	4.3
Spincoated PEDOT	160	3	3.1
Inkjet - 1:1 PEDOT/water	150	10-12	4.7
Spincoat – 1:1 PEDOT/water	60	3	3.7
Inkjet – 1:1 PEDOT/water +5% DMSO	300	Very rough and non-uniform	33
Inkjet – 1:1 PEDOT/water + 5% DMSO +1% Surfynol	300	31	51
Inkjet – 1:1 PEDOT/water + 1% DMSO +1% Surfynol	180	25-28	31

Figure 2.7: Physical and electrical properties of inkjetted and spincoated PEDOT films, with solvents including water and

dimethyl sulfoxide (DMSO), and including Surfynol surfactants [21].

To combat the limited range resulting from low-conductivity polymers, a novel nanoparticle was developed in-house by Huang *et. al.* [22]. In this process, gold nanoparticles are produced with particle diameters as low as 1.5nm. To prevent conglomeration, the nanoparticles are encapsulated with various alkanethiol molecules. An interesting consequence is that the gold nanoparticles show melting temperatures less than 150ºC, while bulk gold is known to melt above 1000ºC. By printing encapsulated gold nanoparticles in solution with toluene, and then heating the substrate to 150ºC, conductive gold lines can be created on plastic substrates. After further experimentation this process was able to produce conductivities as high as 312,000 S/cm (70% bulk gold) [23]. Other nanoparticle materials have been developed, including silver and copper, to complement the gold nanoparticle work, and to provide metals of varying workfunction to the realm of printed electronics [24]. As a whole, the nanoparticle technique is capable of producing printed conductors with conductivities greater than three orders of magnitude better than printed polymers, which enables the creation of effective passive components for RFID.

Soluble dielectrics for printed devices have also been investigated. Early work on printed OTFTs used polyimide dielectrics underneath the organic semiconductor [25]. Polyimides enabled some degree of ordering for the printed poly(3-hexylthiophene) semiconductor, giving mobilities of 0.045 cm^2/Vs. This mobility is similar to the performance seen for this organic on standard SiO_2 dielectric [25]. In searching for printable dielectrics compatible with other organic semiconductors, Benzocyclobutene (BCB) was investigated by Gray *at al.* [26], and showed excellent compatibility with pentacene as a gate dielectric on a plastic substrate. Mobilities of $0.1cm^2/Vs$ were achieved, indicating that the vapor deposited pentacene

molecules aligned well on the BCB material. Unfortunately, large threshold voltage shifts occurred (V_T=-20V), and the material required anneal temperatures of 250ºC, which is above the melting point of many plastics. Much more success has been seen with the work by Infineon Technologies in developing polyvinylphenol (PVP) dielectrics [27]. In this work, which will be examined in more depth in Chapter 7, PVP was spin-cast and used as a gate dielectric in a non-printed OTFT process. The high mobilities achieved (1cm^2/Vs) and high breakdown strength caused this dielectric to become the standard polymer dielectric for printed OTFTs [26][29][30][31][32].

Materials for the organic semiconductors have also improved with time, as shown in Figure 2.8 [28]. However, when employing a new deposition process, such as printing, methods for device optimization must be rediscovered. Printing can introduce problems with semiconductor ordering, including poor molecular alignment and decreased grain size, and results in material performance lower than with methods such as spin-casting. In a sense, when moving to the printing platform, the material performance reverts back to the discovery phase, leaving potential for significant performance improvements through processing optimization. For printing technology, much work has been done with poly(3-hexylthiophene) (P3HT), generally deposited from a chloroform solution [20]. All-printed P3HT devices have shown relatively poor performance to date due to environmental contaminants [20], which are investigated in the next chapter. Another organic semiconductor, Poly(9,9-dioctylflourene-co-bithiophene) (F8T2), has shown improved resilience to environmental contaminants and residual impurities, at the cost of mobility [29]. Spin-case P3HT has demonstrated mobilities of 0.1 cm^2/Vs, while F8T2 is limited to 0.02 cm^2/Vs [29].

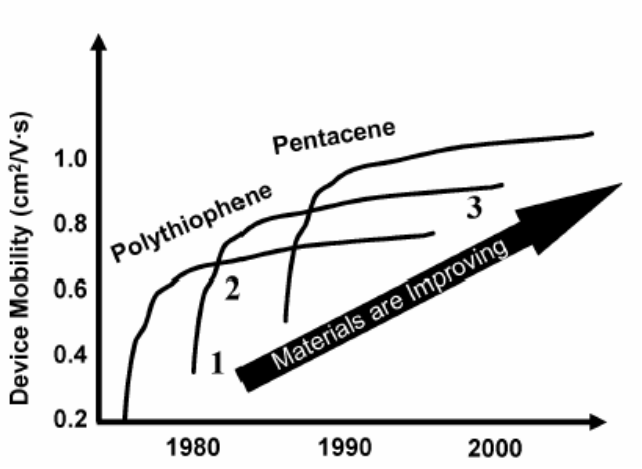

Figure 2.8: The performance of each organic semiconductor material goes through the phases of (1) discovery, (2) process management, and (3) saturation [28].

Typically, most small-molecule organic semiconductors, such as pentacene and oligothiophenes, are not inherently soluble. Instead, solubilizing groups must be attached to the molecule to enable them to be solution-cast via printing. Unfortunately, the bulky solubilizing groups also prohibit the proper stacking of the molecules, inhibiting intermolecular transport through the overlap of pi-bonds, as they do in regioregular P3HT [33]. Thus, to obtain high-performance OTFTs through printing, it is of critical importance that the side-groups can somehow be removed post-deposition. In work by IBM [34], a soluble pentacene precursor was developed. In this process, the bulky side group was effectively removed through a post-deposition anneal processes at temperatures less than 200ºC. This process initially demonstrated saturation mobilities of 0.13 cm^2/Vs and on/off ratios of 2×10^7 for a spin-cast deposition. When this precursor material was integrated into a printed OTFT by Volkman *et al.* [32], mobilities of 0.02 cm^2/Vs and on/off ratios of 10^5 were achieved. Further optimization of the inkjet deposition process produced mobilities as high as 0.3 cm^2/Vs [31]. Similar work has been demonstrated for solubilizing oligothiophenes [33]. After printing, the

solubilizing side groups are removed with heating, and the oligothiophene molecules demonstrate high surface mobility and the ability to realign into highly crystalline structures. Inkjetting the material in an anisole solvent and annealing at 190ºC for 30 min produced devices with mobilities of 0.06 cm2/Vs and on/off ratios of 10^8. By producing these custom molecules with removable solubilizing side chains, highly ordered organic semiconductors can be deposited through printing technologies. As a result, printed OTFTs have begun to demonstrate performance only slightly less than OTFTs with organic layers deposited through vacuum deposition processes. As this new method for solution-based deposition of organic molecules matures, it is not inconceivable that printed organic semiconductors may have mobilities on par with their vacuum processed counterparts. Combined with common polymer dielectrics and nanocrystal contacts, high-performance fully-printed OTFTs for RFID are a realistic endeavor, and may enable a fully printed RFID tag in the near future.

2.3.3 Printing Mechanisms

Of the many printing techniques available, the largest portion of work in literature has been devoted to inkjet technology. While inkjet does not offer throughputs as high as other methods, the versatility of design is unparalleled. As a research tool, inkjet printing enables the user to print custom patterns on the fly, which greatly expedites the process of developing recipes to print uniform structures. This is accomplished by mounting the inkjet head on movable tracks, and moving the head as necessary to construct specific device patterns on the plastic substrate underneath. Inkjet systems also generally have many more adjustable parameters which can be used to optimize film deposition besides film viscosity and substrate temperature. The working distance from the head to the substrate, the speed of the ejected drop, the volume of the drop, and the drop-to-drop overlap on printed lines can all be tuned

to create high resolution features. Unfortunately, inkjet deposition is far too serial of a process to offer the lowest production costs.

Work has also been done on the study of screen-printing [25][26] and gravure [20] technologies. Screen-printing is a simple process where the printing surface is overlaid with a stainless steel screen. Patterns are etched through the stainless steel mask surface, much like a stencil. Once mounted and aligned to the substrate, the target material is pushed through the screen by an ink-rolling process. Screen printing has a high throughput, and is more cost effective than inkjet printing. Unfortunately, most published works cite line pitch limits at 250μm [25]. Gravure, on the other hand, is expected to enable higher pitches. Gravure is similar to stamping processes except that the solution-based deposition material resides in the recessed regions. As the roll is coated with material, a blade is used to remove material residing on raised roll features. As a result, when the roll is placed in contact with the substrate, the material stored in the recessed wells is transferred to the substrate surface. By mounting the gravure roll on the reel-to-reel system, the patterns can be deposited as the substrate is moved beneath the roll. Thus high throughput is easily achieved on a commercial gravure system. Unfortunately, the transfer of patterns to the steel roll is not trivial. By using a laser etching process, the design is imbedded into the roll. Thus, quick changes to the pattern are not available, and the cost of producing a custom roll is expensive. Gravure is a challenging technology to optimize in the scope of research and optimization, but the high throughput will likely lead to its adoption as the main deposition method in future commercial reel-to-reel systems.

2.4 Printed RFID Using Organic Semiconductors

The three main topics in this chapter will be integrated in this work to create low-cost RFID components using printable materials. By using solution-processed organic films and low temperature methods, the goal is to create an addressable non-volatile memory array for RFID tag identity. Using reel-to-reel compatible organics transistors, OTFTs for addressing memory arrays will be created. These devices will be tailored to operate in close proximity and to enable the vertical stacking. To complete the memory needs, a novel memory element is created utilizing organic diodes and polymer dielectrics that are compatible with printing processes. The end result is a fully addressed stackable memory array technology that reaches cost-points several orders of magnitude lower than their silicon RFID counterparts.

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Chapter 3: OPTIMIZING OTFT BEHAVIOR

While Chapter 2 introduced the many application thrusts for organic electronics, entrance into the commercial landscape required devices to work day-in and day-out. One of the primary detractors from the integration of organic electronics into the industrial manufacturing space lies in problems encountered in device degradation. Understanding the sources of the device degradation, and experimenting with the means to prevent them is of paramount importance in pushing the organic electronics technology into mainstream.

3.1 Performance Enhancements via Annealing

The effect of thermal annealing on the electrical and physical modifications to Poly(3-hexylthiophene) was investigated to better understand degradation mechanisms. Thermally-induced performance enhancements and thermal stability of polythiophene thin film transistors (TFTs) were explored. Substantial mobility improvements were observed in devices annealed at low temperatures (<80°C), and increases in on/off ratios by more than two orders of magnitude were observed at moderate anneal temperatures (~120°C). Changes were seen in conductivity, mobility, on current, and on/off ratio with anneal temperature and total thermal budget. This investigation is able to show the expulsion of environmental contaminants and increases in film density as means to performance recovery and enhancement. This study provides a comprehensive analysis of the effect of thermal cycling of polythiophene TFTs on various device performance metrics, and identifies relevant thermal limits and failure mechanisms.

3.1.1 P3HT Thermal Stability

While many application targets of organic semiconductor-based electronics exist, all depend directly on the quality and predictability of the organic semiconductors. Of the various soluble organic semiconductors currently in use in such applications, poly(3-hexylthiophene) (P3HT) has been the most extensively studied, due to its easy synthesis and relatively high mobility ($\sim 10^{-2}$ $cm^2/V \cdot s$) [10]. It is also closely related to other high-performance semiconductors such as Poly(9,9-dictylfluorene-cobithiophene) (F8T2) and Poly(3,3'''-didodecyl-quaterthiophene) (PQT-12), and may provide insights to these materials as well. While organic semiconductors of high mobility have been created by many different groups, issues of environmental stability and device lifetime remain the largest barriers to broad commercialization.

While there have been several demonstrations of polythiophene-based TFTs, there have been few studies on the thermal stability of the same. This is an important topic for various reasons. First, given the sensitivity of polythiophene to oxygen and moisture absorbed during the fabrication process and operation, it is expected that thermal treatments may be used to recover some of the lost performance through thermally-induced expulsion of absorbed contaminants. This is especially relevant as organic semiconductors are integrated onto plastic substrates, as environmental elements can contaminate surface passivated devices due to the high permeability of flexible substrate materials. Second, polythiophene-based devices will likely be exposed to elevated temperatures during the fabrication process, due to the thermal budget requirements of subsequent layers. Finally, thermal cycling studies provide crucial insights into device lifetime and stability. In a previous publication this investigator reported upon the effects of thermal cycling on the performance of P3HT devices [11]. Here, those results are reestablished, and physical and electrical testing is used to determine the resulting

changes occurring in the semiconductor thin-film. The goal is to experimentally link the measured performance variation to associated physical phenomena, including oxygen and moisture de-doping and decreasing intermolecular spacing within the semiconductor material.

3.1.2 Experimental Details

All experiments were performed on silicon substrate-gated polythiophene TFTs with thermal SiO_2 dielectrics. This ensured good repeatability and elimination of experimental artifacts originating from other, less well-behaved, structures. Gold contacts were evaporated onto a 100 nm thermal SiO_2 layer on an n-doped Si wafer. Poly(3-hexylthiophene) (P3HT) with greater than 98.5% regioregularity was obtained from Aldrich and mixed at 0.8 wt% in chloroform. Given that the thrust of our experiment was to reclaim TFT performance lost to environmental contaminants, purification of the air-exposed source material was not necessary. The solution was spin-cast in a nitrogen environment at 6000 RPM to achieve a film thickness of approximately 180 nm. While previous works [10] showed performance enhancement via an HMDS surface treatment, we observed no significant improvement in the electrical performance of P3HT devices, and thus this process step was not used. This result is most likely due to our device structure wherein source/drain pads are defined prior to polymer deposition, causing the large polymer disorder at the pad boundary to dominate. Six inert-ambient curing temperatures were explored over the temperature range from 40°C to 140°C due to their relevancy to plastic-compatible processing and organic semiconductor material limits. This range was chosen to reside below the limits of plastic substrates currently pursued in inkjet and gravure printing technologies. For each of these temperatures, four different anneal times between 1 minute and 1000 minutes were explored. Samples were rapidly cooled to limit additional heat exposure. All experiments were performed on multiple samples, each

containing multiple pre-measured and mapped devices, to minimize statistical variations, and to enable pre- vs. post- exposure analysis. Including control samples kept at room temperature, the data set consisted of measurements from more than 200 samples.

Electrical measurements were performed in a nitrogen environment at room temperature, with each device electrically isolated via probe scratching. All reported data was gathered from devices with channel widths and lengths of 250 μm and 10 μm respectively. It was found that precise scratching around the perimeter of devices caused the electrical performance to scale well with device size, due to the elimination of lateral leakage paths. Gate and drain voltages were swept between 5 V and -35 V, and both I_D-V_G, and I_D-V_D measurements were made. Significant device-to-device variation occurred, likely due to P3HT ordering variation induced during spin deposition. Thus, for all data presented, the post-annealing data was normalized to the pre-annealing data to enable proper comparisons. To correlate the measured electrical variations in device performance to physical effects, various materials analysis tests were performed, including RBS (for background oxygen level measurement), X-Ray Diffraction (for crystallite size and orientation), UV spectra (for detecting changes in polymer chain structure), and AFM (for surface roughness measurement).

3.1.3 Results

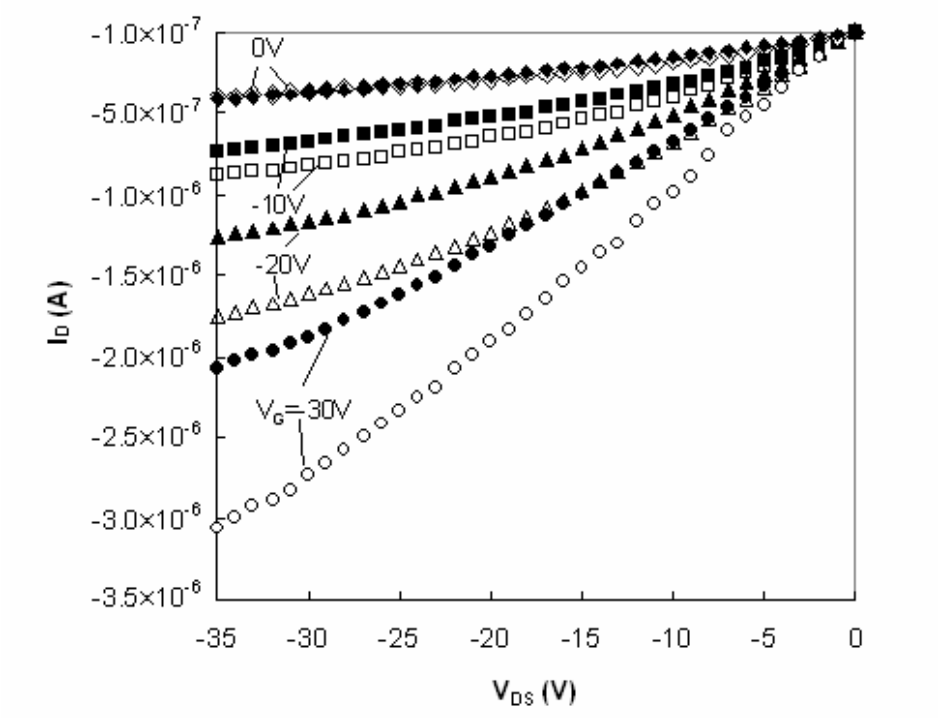

Figure 3.1: Output characteristics of an unannealed P3HT device (filled) and a device annealed an 80ºC (open).

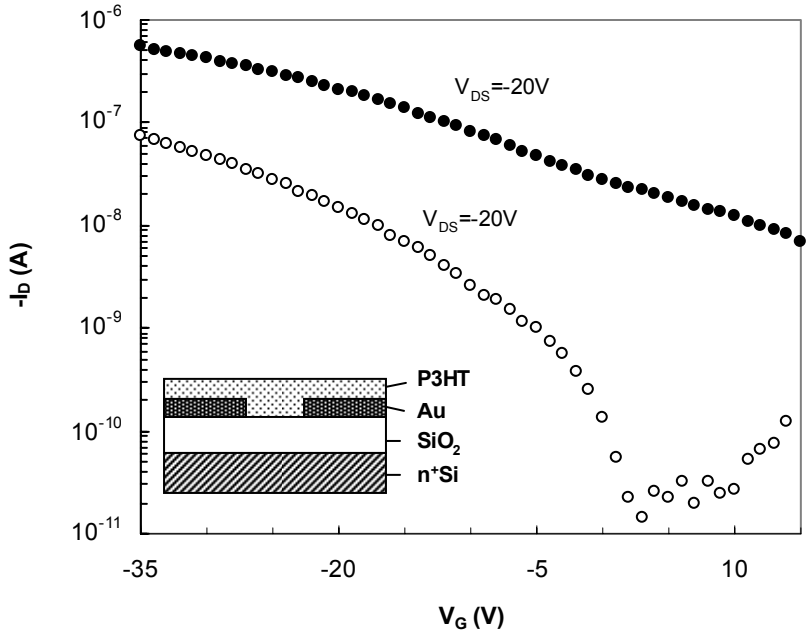

Figure 3.2: Transfer characteristics for an unannealed P3HT device (filled circles) and a device annealed at 120ºC (open circles). Backgated P3HT device (inset).

Figure 3.1 and Figure 3.2 illustrate output and transfer characteristics of baseline P3HT devices as well as a sampling of electrical performance modifications obtained through precise thermal cycling exposures. The mobilities of unannealed samples averaged ~0.06 $cm^2/V \cdot s$ and on/off ratios were ~10^2 when using V_{DS} = –20 V. This performance is on par with other published works for P3HT, including those using self-assembling monolayers (SAMs) [10], once our relatively low sweep and low V_{DS} voltages are taken into account. To eliminate the human error introduced from estimating V_T from the square-root of the I_D-V_G curve, the saturation field-effect mobility was calculated using:

$$\mu_{SAT} = \frac{g_m^2}{2I_{DS}C_{OX}\left(\frac{W}{L}\right)}$$

Conductivity measurements were also taken and correlated to mobility. With current measurements of the devices taken at $V_G = 0$ V and $V_D = -1$ V, and film thickness determined via profilometry, conductivity was calculated using:

$$\sigma = \left(\frac{L}{Wt}\right)\frac{I_{DS}}{V_D}$$

Summaries of device performance modifications as functions of anneal temperature and time are shown in Figure 3.3 and Figure 3.4. Once again, the post-annealing data was normalized to the pre-annealing data to give a percentage change in performance. It is also important to note that μ_{sat} is not linear with I_D in this case, due to parasitic current pathways through the bulk. As is evident from the assorted regions of increasing and decreasing performance, multiple effects occur, with different effects dominating in the various temperature regimes. Figure 3.3 indicates that saturation mobility can increase by as much as 60% via long duration low-temperature anneals (60°C). Additionally, on/off ratios for P3HT can be increased by almost three orders of magnitude by using long duration anneals at 120°C (Figure 3.4). Above this temperature damage to the film occurs, resulting in a decrease in both on/off ratio and mobility. From Figure 3.3 and Figure 3.4, it is apparent that there are three regions of operation:

- Up to ~60°C, the mobility increases, while the on-off ratio is mainly unchanged.
- At moderate temperatures, 60°C-120°C, there is a dramatic increase in on-off ratio, while mobility is degraded continually with increasing temperature.
- At high temperatures, >120°C, both mobility and on-off ratio are degraded.

To explain the variations of device performance in the three regimes, we introduce different physical phenomena, and correlate the electrical results to materials analyses. The concepts used to explain the phenomena seen are the oxygen dedoping of the P3HT film, lattice densification, and the energetically activated molecular reorientation at low temperature.

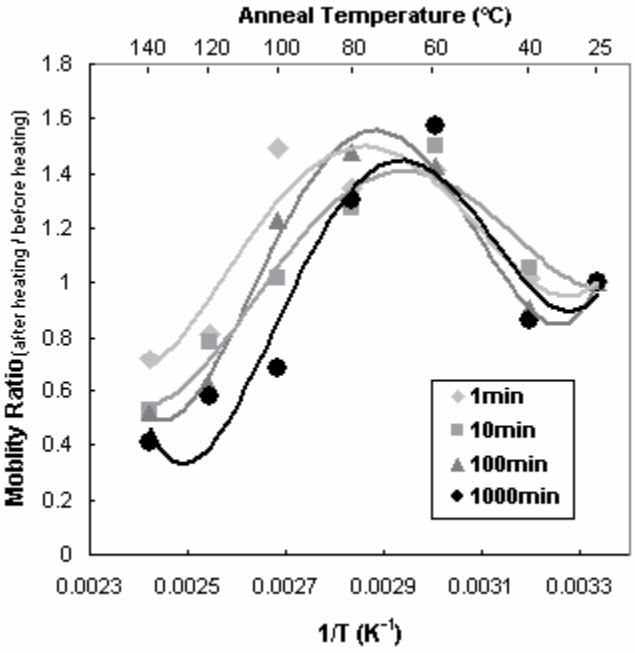

Figure 3.3: Variation in saturation mobility with thermal cycling.

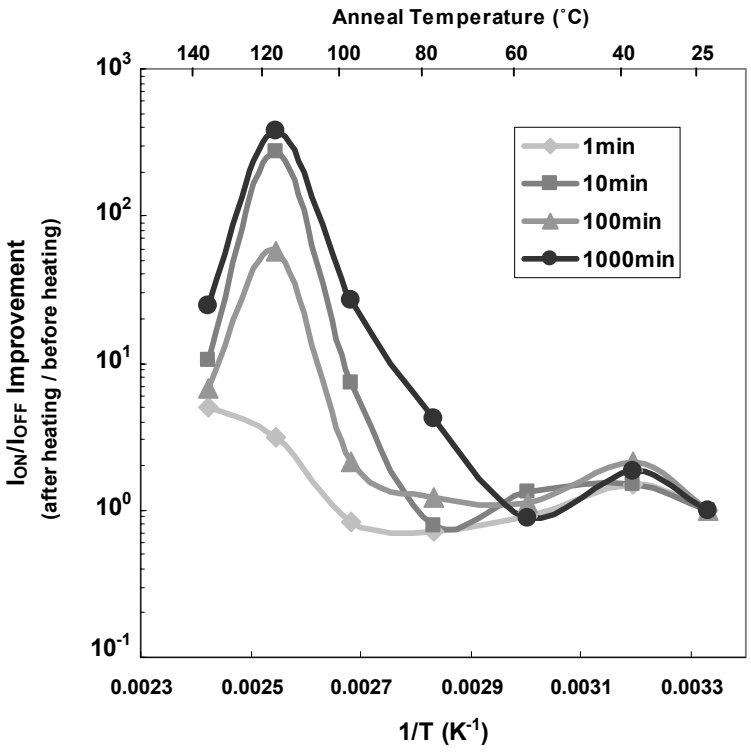

Figure 3.4: Variation in on-off ratio with thermal cycling. ION is measured at VG = -35V, VDS = -20V. IOFF is measured at positive gate voltages where the current is mostly independent of gate voltage.

3.1.4 Discussion

3.1.4.1 Oxygen Dedoping

During the production and solution preparation of the P3HT material, the solution absorbs oxygen from the environment. Therefore, despite using inert ambient environments during device fabrication and electrical characterization, significant concentrations of oxygen are expected to be embedded in the films. From a production standpoint, even if the solution is prepared in an inert environment, oxygen would quickly penetrate into the active layer due to current challenges in achieving sufficient passivation of organics on plastic substrates. In conjunction with ambient light exposure creating excited P3HT anions [12], this oxygen dopant serves to increase the conductivity of the films through the production of localized

states within the π-π* gap [13][14]. This is in-part due to the lower ionization potential of thiophene-derived conjugated molecular backbones. This increases the off-current of the transistors, reducing the on/off ratios. Experimentally, P3HT is often dedoped by soaking in ammonia-ethanol solutions [15], but this has proven insufficient for removing necessary amounts of oxygen, and certainly cannot be used to recover performance post-production. Here, we establish that use of long-duration, low-temperature anneals in an inert environment is effective in oxygen removal. Unlike previous works where doping levels are determined solely through the analysis of device current-voltage curves [16][17][18], we verified oxygen concentrations by elemental analysis via Rutherford Backscattering Spectrometry as shown in Table 1 and Figure 3.5.

Sample	Composition
control	7.7at% S; 15at% O
40°C	7.5 at% S; 12 at% O
60°C	7.5 at% S; 12 at% O (O-rich on the top $2x10^{17}/cm^2$ layer)
80°C	7.0 at% S; 6 at% O
100°C	7.0 at% S; 5 at% O (slightly more O-rich on the surface)
120°C	6.5 at% S; <1 at% O
140°C	7.2 at% S; <1 at% O

Table 1: Sulfur and Oxygen concentrations as determined by RBS. Sulfur was used as a marker for the polythiophene layer.

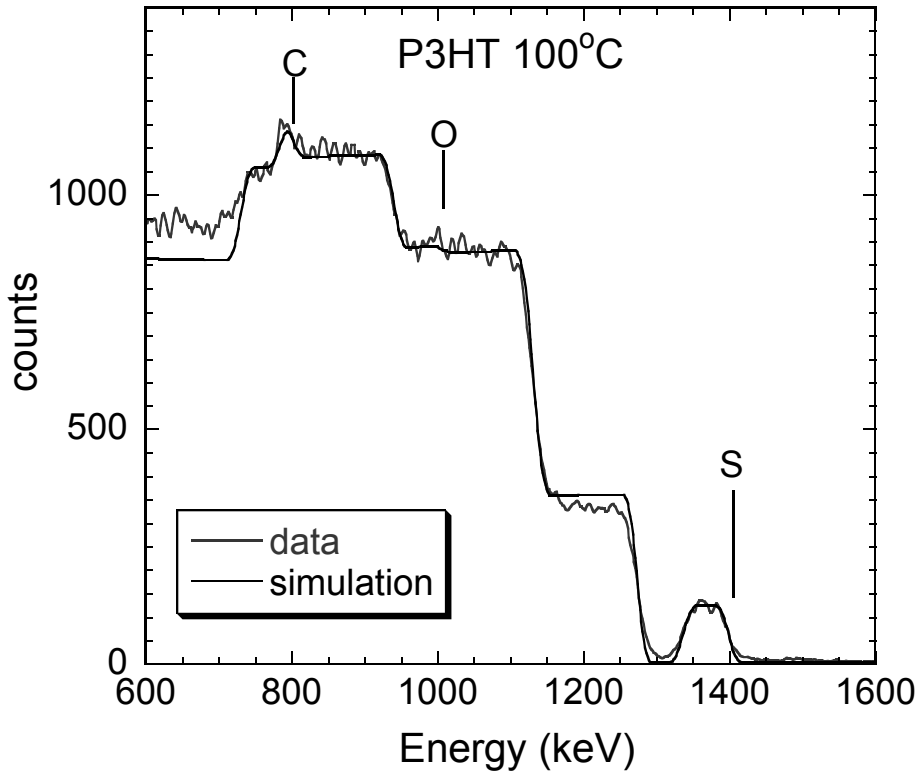

Figure 3.5: RBS Spectra for a typical sample, showing excellent fitting between the data and the parameter extraction signal.

Over all temperature regimes, the oxygen concentrations of Table 1 correlate well to the on/off ratios of Figure 3.4. Above 100°C, oxygen concentrations were reduced to below detectable limits and on/off ratios were maximized. At mid-range temperatures, intermediate values of oxygen concentration (6 at%) correspond to intermediate levels of improvement in on/off ratio, and annealing at 40-60°C had little effect on oxygen concentration or the on/off ratio.

Note that the atomic concentrations were calibrated by fitting the RBS-spectra to the film thickness of unannealed films as measured by profilometry (which has an error of ~15%; this explains the sulfur concentration being slightly lower than the theoretically expected value sans

hydrogen, which is not detected by RBS). The substantial decrease in oxygen content relative to sulfur content clearly attests to the oxygen dedoping. It must also be noted that during the RBS loading process, samples were briefly exposed to air, which posed a contamination threat to the samples. However, the RBS results demonstrate samples with oxygen levels below the detectable limit, indicating that the exposure time was not significant enough for oxygen to significantly penetrate into the P3HT film.

Within this experiment, oxygen concentrations varied by P3HT batch, but similar de-doping behavior was found consistently. In some batches, oxygen concentrations were below 3% for the control sample, and were below detectable limits for anneals greater than 60°C. Lower baseline concentrations were partially due to slow outgassing, as samples stored under vacuum for months had lower concentrations than those stored under nitrogen. However, since oxygen concentrations were generally much higher than expected, a set of samples was exposed to air for two weeks, and were then tested. Oxygen concentrations were found to be three times higher than their nitrogen-storage counterparts. As both samples were exposed briefly during RBS loading, this result qualitatively indicates significant air exposure time is needed to alter oxygen concentrations, as supported in [16].

It should be noted that V_T shifts were minor (+/-1V) and that device-to-device variation greatly outweighed any variation due to thermal cycling. No numerically significant correlation between V_T and thermal cycling could be ascertained, despite known reductions in oxygen concentrations. While this contradicts popular opinion [16][17], it directly agrees with the findings of Meijer *et al.* [17]. They found that for P3HT FETs no direct correlation between V_T and oxygen dopant density could be found. Instead, they determined that oxygen dopants played a larger and more direct role though increases in bulk mobility via $\mu_{bulk} \sim N_A^{2.3}$, which

increased leakage currents. This work tends to agree, and despite exact doping densities not being calculated here, we see similar changes in our transfer curves upon an expulsion of the oxygen concentration, as determined via RBS.

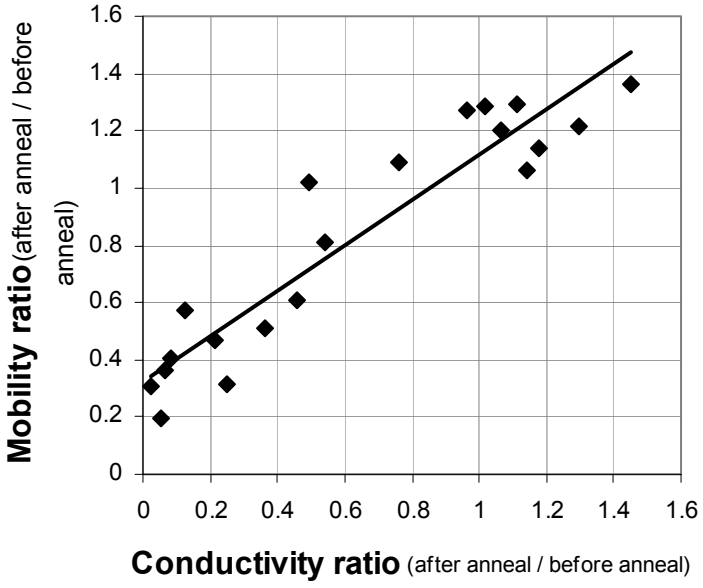

Figure 3.6: Correlation between saturation mobility and conductivity for all temperatures.

To further analyze the dedoping effect, it is illustrative to examine the correlation between saturation mobility and conductivity, shown in Figure 3.6. The linear nature of the mobility vs. conductivity plot reaffirms that the semiconductor has a relatively high doping, and that the density of states within the bandgap is high. Thus, charge transport is controlled by the variable-range hopping of carriers at the fermi level [13], as opposed to thermally activated transport, and is therefore highly influenced by oxygen doping levels. The linear nature also leads to the conclusion that oxygen concentrations below that detectable by RBS still play a significant role in charge transport. Figure 3.7 illustrates the increase in the mobility to

conductivity ratio that occurs for high-temperature anneals, which indicates a drastic reduction in the density of states within the bandgap. The reduction of states decreases both saturation mobility and low-bias conductivity, although it has a much more drastic on the later, as expected. As a result, we obtain decreased drain leakage and better channel control, with relatively small losses in device mobility. The decrease in the mobility-conductivity ratio also directly affects the on/off ratio, as related in the derived equation by Brown et al.:

$$\frac{I_{ON}}{I_{OFF}} = \left(\frac{\mu}{\sigma}\right)\frac{C_i^2}{qN_A t^2}V_D^2 \quad [13]$$

This relation directly links the device data from Figure 3.4 and Figure 3.7, illustrating that this conductivity decrease is responsible for the increase in on/off ratio. The mobility-conductivity ratio change illustrates how the decrease in acceptor density with annealing plays key roles in the maximization of the on/off ratio of the P3HT transistors. The simultaneous increase in on/off ratio and decrease in mobility evident at intermediate temperatures (60°C-120°C) is well explained using the oxygen de-doping mechanism. As a result, dopants responsible for increased bulk conductivity can be readily removed from doped films post-production to increase device performance.

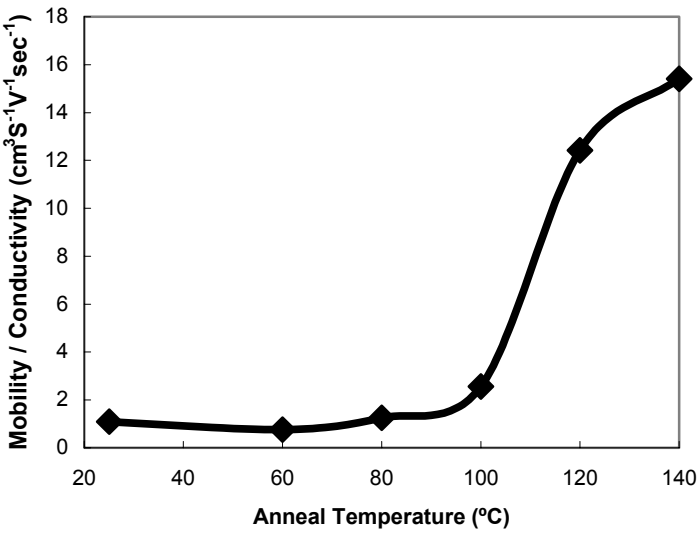

Figure 3.7: Mobility divided by Conductivity for 100 min anneal cycles and varying anneal temperature.

Upon the application of low temperature anneals, drastic increases in saturation mobility (and on-current) were discovered for both short-duration and long-duration cycles. No detectable change in oxygen concentration occurs, yet even for a one-minute anneal at 60°C the mobility increases by ~40%. For longer anneals the effect is more pronounced; saturation mobilities increase by more than 60%. It is probable that one of two mechanisms can provide an explanation for these results: the detrapping of remnant solvent molecules beneath the film surface of the as-spun film, or molecular reorganization occurring within the film itself. For the former, it has been proposed that low temperature anneals could impart enough energy to release the buried solvent molecules, resulting in the densification of the P3HT film. However, upon further analysis of RBS data taken over all anneal temperatures, it was determined that no detectable amount of Cl_2 (from the chloroform solvent) was trapped within the film. The Cl dedoping mechanism is also disproven by X-ray analysis. However,

X-ray data does give insight to permanent changes in intermolecular spacing due to thermal cycling.

3.1.4.2 Lattice Densification

Besides increases in organization of the film as a whole, changes in the intermolecular spacing within crystallites also impact electrical performance. X-ray analysis of the different P3HT samples offers significant insight to the irreversible structural changes occurring as a result of thermal cycling. The 010 direction in P3HT is of particular interest, as it relates to the direction carrier transport via π-stacking between neighboring molecules governed by van der Waals bonds. Through the observation of the (020) peak at $2\theta = 23.22^{o}$, it can be determined that the interplanar spacing of an unannealed sample is 3.785 Å, which is on par with recognized values [15]. An important effect of the thermal cycling of P3HT is the reduction of intermolecular distance in this plane with increasing anneal temperatures. Low temperature anneals appear to slightly increase intermolecular distance, while elevated temperature anneal cycles significantly decrease spacing on this axis, as shown in Figure 3.8. Similarly, we also examined the (100) diffraction peak residing at $2\theta = 5.44^{o}$. Like the (020) peak, the spacing on this axis also decreased at higher temperatures. This peak also shows a permanent increase in molecular spacing for low temperature anneals. When compared to the mobility results of Figure 3.3 we see a correlation. While it is generally believed that tighter packing of P3HT molecules aids in conduction by increasing the overlap of pi-orbitals, our data indicates otherwise. Instead, perhaps the densification of the film increases carrier scattering events, thus decreasing mobility. Reordering of the semiconductor is also a valid possibility, though not one we can readily measure. Whatever the reason, we see that intermolecular spacing is directly affected by the anneal cycles, and it likely plays a considerable role in the surface mobility alterations seen in Figure 3.3.

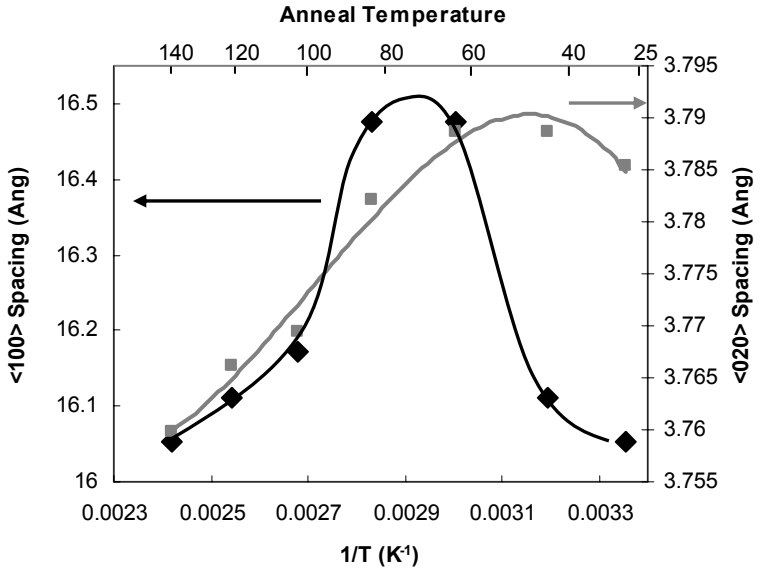

Figure 3.8: Intermolecular spacing along <100> and <020> axes, as determined by X-ray.

A remaining challenge is the explanation of the large decrease in drive current, and thus on/off ratios, after high-temperature anneals. For such large performance changes, a drastic modification in either conjugation length or film ordering appears logical. Previous studies [19-22] have extensively examined an effect called thermochromism, in which the molecule undergoes a rotation about the chain axis at the inter-thiophene C-C linkage when heated to temperatures nearing the melting point. The modification of alkyl chains from trans conformation to gauche through this chain twisting leads to the disruption of the π-π conjugation system. This disruption inhibits charge transport through the reduction of the delocalized carrier space along the molecule, reducing the electrical mobility. This effect would correspond well to the drastic change in electrical performance observed after high-temperature anneals in this experiment. However, thermochromism is understood to be a reversible effect, meaning any chain torsion induced by elevated temperatures is eliminated

upon cooling. Analysis of the UV spectra (Figure 3.9) indicates that the rapid cooling process used here did not quench the molecules into a permanent twisted conformation. The lack of a significant blue-shift in absorption peak indicates that no significant shift in the HOMO or LUMO levels occurred (indicating a lack of change in conjugation length), and therefore chain torsion is not responsible for the drastic mobility decrease seen for samples cycled at temperatures above 80ºC.

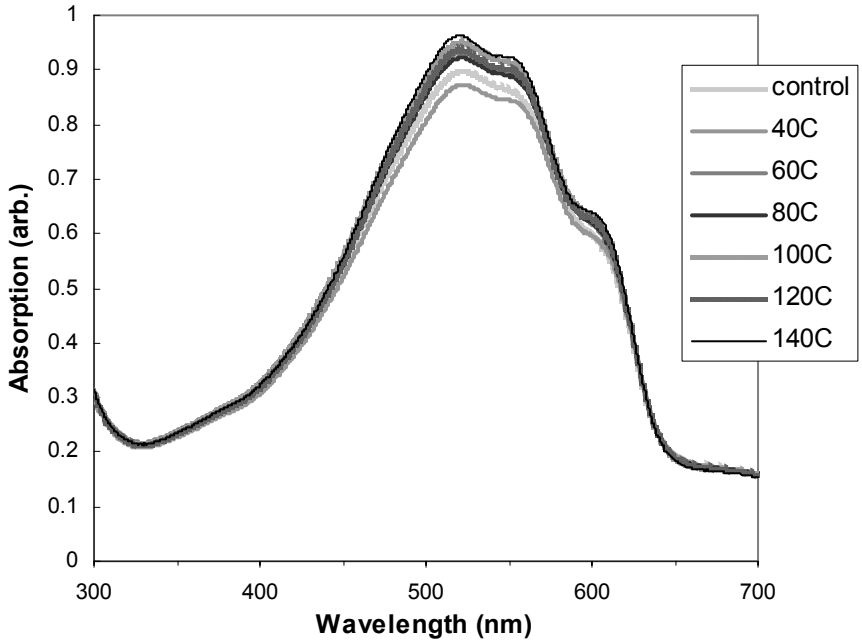

Figure 3.9: UV spectra of P3HT films following thermal cycling at various temperatures. Slight differences in absorption peak intensity most likely originate from film thickness variations on the spin-cast wafer.

Conversely, infrared spectroscopy performed in other studies [15] indicates the heating of P3HT does lead to the irreversible growth of the C-C stretching mode at 1261 cm^{-1}. The mode grows rapidly for temperatures of 80ºC and above. The stretching of this bond could result in less overlap between delocalized carrier regions, resulting in small conduction barriers

along the length of the molecule. The increase in the intensity of the C-C stretching mode does not correlate to a change in the UV spectrum. Thus, chain stretching could play a role in the mobility decrease observed for higher temperature anneals, but the magnitude of the electrical change it could induce is challenging to quantify.

3.1.5 Implications

From the experiments above, it is apparent that the performance of poly(3-hexylthiophene) transistors can be altered dramatically as a consequence of exposure to elevated temperatures. In particular, thermal annealing may represent an attractive means of improving the initial quality of organic TFTs, as a post-deposition purification technique. It has also shown to be ideal for the performance recovery of devices that have become environmentally tainted over time. Thermal annealing has proven highly effective in removing oxygen contamination from polythiophene active layers, resulting in a dramatic improvement in on-off ratio. Given the potential applications of such devices in low-cost displays and low-power RFID circuits, high on-off ratio is a critical requirement.

It is also possible to analyze the stability and reliability of polythiophene TFTs based on the results above. As described previously, temperatures above 120°C result in degradation in both mobility and on-off ratio due to structural changes in the polythiophene films. The irreversible change represents an upper limit on the thermal excursion allowed in polythiophene-based devices. This has consequences for various integration strategies – for example, the use of post-thiophene polyimide processes for dielectrics and passivation is not possible, since these typically require imidization temperatures above 150°C. Additionally, the thermal analyses performed will aid further experiments in the calculation of activation

energies associated with the thermal film disruption processes, which should also allow the development of a metric for accelerated lifetime testing of these devices.

3.1.6 Thermal Cycling Conclusions

The electrical and physical effects of thermal cycling on Poly(3-hexylthiophene) transistors have been studied. It has been shown that device performance can be enhanced through low-temperature annealing. Observations of the thermally-induced variations in device parameters have also led to insights into the physical effects occurring inside the semiconducting film. Among them, the oxygen dedoping of P3HT films has been indicated as a dominant force in driving changes in device performance, playing an important role in the minimization of leakage current. The induced changes in intermolecular spacing have also proven to play a significant role. The electrical characterization and physical testing techniques have combined to help establish the thermal limits of the material. This analysis provides a basis for integration of P3HT with other low-cost processes, and establishes a baseline set of phenomena determining the thermal reliability of the same.

3.2 Moisture Exposure Effects

While the previous study and Meijer *et al.* [18] focused identified ambient oxygen as a source of p-type doping due to a charge-transfer reaction, the true source of the oxygen was not realized. In fact, there exist two sources of oxygen in the environment – O_2 and water vapor. The previous section used RBS to accurately quantify the oxygen concentration in the films, but does not lead to a conclusion as to the source. Unfortunately, RBS operates by bombarding the film surface with helium atoms and measuring the recoil, and cannot detect atoms with smaller weights than helium, such as hydrogen. Therefore, to fully understand what is necessary to fully passivate organic devices, this differentiation must be analyzed.

3.2.1 Moisture Influence on P3HT

Hoshino *et al.* [23] successfully identified the difference through a series of experiments that test devices in vacuum, N_2, O_2, and N_2 with humidified with water. Much like the previous experiment, backgated P3HT wafers were utilized, and baseline current levels correlated well when the different geometries were accounted for. As expected, testing in vacuum and dry N_2 yielded similar results, as seen in Figure 3.10. Slight differences occurred for V_g values near 0V, but were insignificant when hole concentrations increased at higher gate bias. Such differences were attributed to the effect of pressure on the active layer.

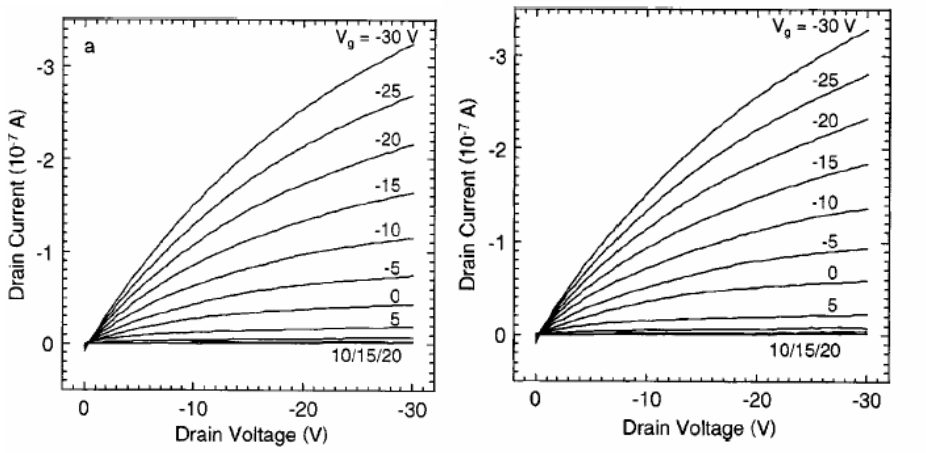

Figure 3.10: P3HT OTFTS with W=0.5cm, L=20μm, and Tox=300nm, tested in vacuum (left) and dry N_2 (right) [23].

In contrast, when N_2 was humidified by bubbling hot water, drastic changes were seen in the device behavior immediately after exposure. As can been seen in Figure 3.11 (left), the device exhibits poor saturation behavior and increased conduction in the depletion mode, much like the in-house devices of Figure 3.1 and Figure 3.2. While the electrical effect of moisture was immediate, the effect of increasing O_2 concentration in the testing chamber was gradual. As seen in the right of Figure 3.11, drive current increased in a matter of hours, with leakage

current also increasing. This is indicative of oxygen acting as an acceptor-type dopant, and it is apparent that oxygen diffusion through the polymer matrix is slow. Since the water molecule is larger molecular size than O_2, the authors conclude that vapor diffusion would be limited. Thus, to see such an immediate effect with the addition of water vapor, they hypothesize that the large dipole moment of water could generate holes in the vicinity of the active layer. While possible, whatever conclusion is reached as to the specific degradation mechanism is moderately inconsequential. More importantly, by identifying moisture in the air as the primary degradation source, steps can be taken in this route during sample preparation and in passivation engineering.

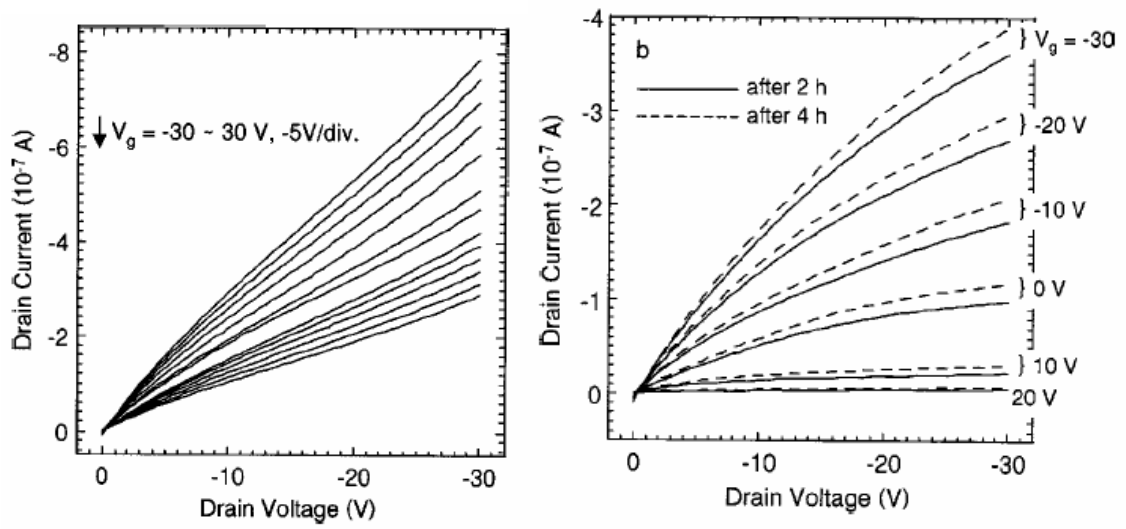

Figure 3.11: P3HT I_D-V_D curves after exposure to wet N_2 (left) and O_2 (right). [23]

3.2.2 Moisture Effects in other Organic Semiconductors

Other groups [24][27] have investigated whether moisture contaminated different organic semiconductors in a similar fashion. Pentacene, C12FTTF, and C6TFT were all investigated by Li *et al* [24], and showed several similarities to the work presented in Section 3.1, [18], and

[23]. For example, off current was shown to increase rapidly with high humidity after being exposed for only five minutes. From the inset of Figure 3.12, it is also apparent that the on/off ratio decreased with increased humidity levels, which is comparable to increased exposure time in the work by Hoshino *et al* [23]. However, a dramatic difference is the substantial decrease seen in saturation current with high humidity. It was theorized that the drop in drive current could be due to the diffusion of water molecules into the grain boundaries, changing intermolecular interactions and increasing the energy barrier for intergrain charge transport. Another possibility is that the ions associated with water screen the electric field within the channel, and thus lower the concentration of mobile carriers [24]. In either case, since diffusion is generally greater along grain boundaries, a higher density of grain boundaries would increase the sensitivity of the material to moisture.

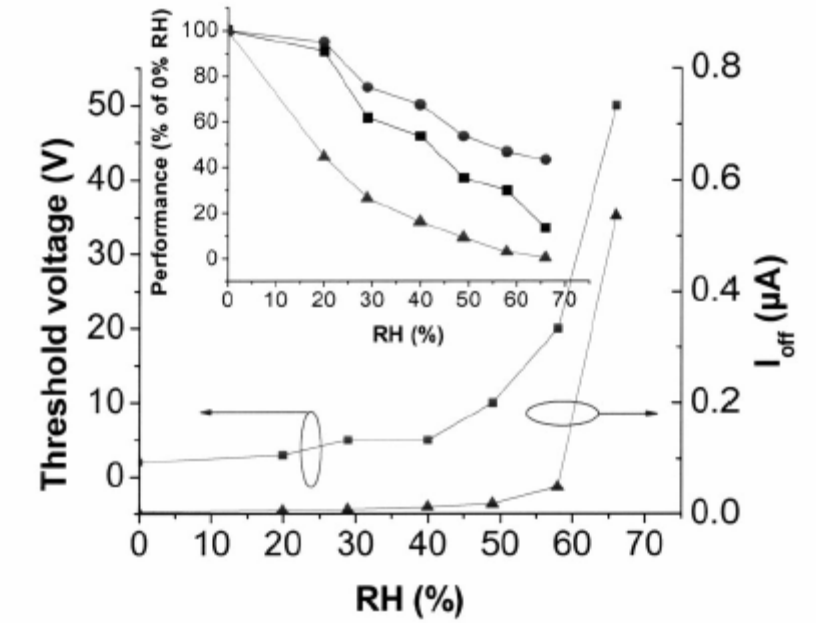

Figure 3.12: Changes in pentacene TFT electrical properties with respect to relative humidity (RH). Threshold Voltage (squares) and off current (triangles) explored. Inset: Field-effect mobility (squares), saturation current (circles), and on/off ratio (triangles) explored. [24]

Figure 3.13 illustrates the different responses in on-current for the materials investigated in [24]. While pentacene showed decreased drive current with low levels of relative humidity, C12FTTF showed stable behavior to greater than 40% relative humidity. It should be pointed out that C12FTTF is centered with a thiophene-based backbone, and therefore it is not unexpected that it should behave like the P3HT devices of Figure 3.11. It is possible that the lack of response for the hybrid molecule of Figure 3.13 (center) to humidity is due to competing processes of doping and ion charge shielding.

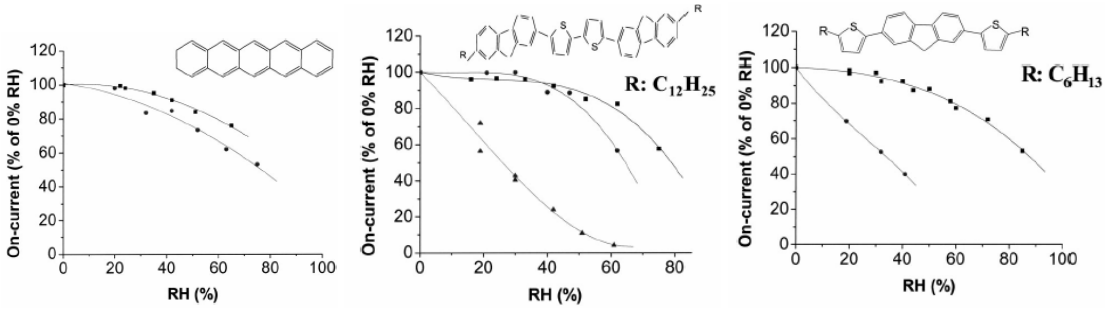

Figure 3.13: Decreases in on-current with relative humidity for pentacene (left), C12FTTF (center), and C6TFT (right). In all cases, bottom-contacted devices showed decreased on-current versus top-contacted devices. [24]

Qui et al [25] performed similar work on pentacene under standard atmospheric conditions. Comparable discoveries were found regarding decreases in on/off ratio and decreases in drive current. Through infrared spectroscopy, hydroxyl radical absorption peaks were identified in films stored in atmosphere. It was thus concluded that the primary contamination source was H_2O vapor. With so many broad contributions to the analysis of organic TFT degradation in ambient conditions, passivation of these devices for commercial uses has become far more directed. In fact, UV curable resins [25] have shown the ability to reduce decreases in on/off ratio to 5% over 500 hours in ambient atmosphere.

3.3 Surface Treatments

While passivating films developed to decrease the moisture effects of Section 3.2 have made progress, the introduction of plastic transparent substrates has created additional challenges. Besides the challenges of elasticity to prevent fracture during flexion, the increased permeability of plastic films place greater challenges on the film to prevent contaminant diffusion [26]. To combat this, other means to limit the effect of oxygen-based contaminants have been investigated.

With performance degradation showing strong correlation to H_2O vapor concentrations, elimination of any initial vapor prior to organic deposition becomes paramount. It has be theorized by Goldmann *et al* [27] that the hydrophilic nature of the thermally-grown SiO_2 gate dielectric can allow for molecular layers of water to be attracted to and absorb on the dielectric surface. To prevent such an occurrence, the dielectric was treated with octadecyltrichlorosilane (OTS), which make the surface highly hydrophobic, repelling water.

When placed in direct comparison with an untreated sample, as in Figure 3.14, a threshold voltage shift can be seen between the 'unstressed' devices. The direction of the shift is indicative of charge trapping in the untreated film. When the devices are stressed (-60V for 100min), large differences in current are seen between the two samples, as discrete trapping levels have formed in the untreated device. Goldmann *et al* [27] attribute this difference to the reduction of charge-trapping due to decreased water molecule concentration in the OTS-treated device.

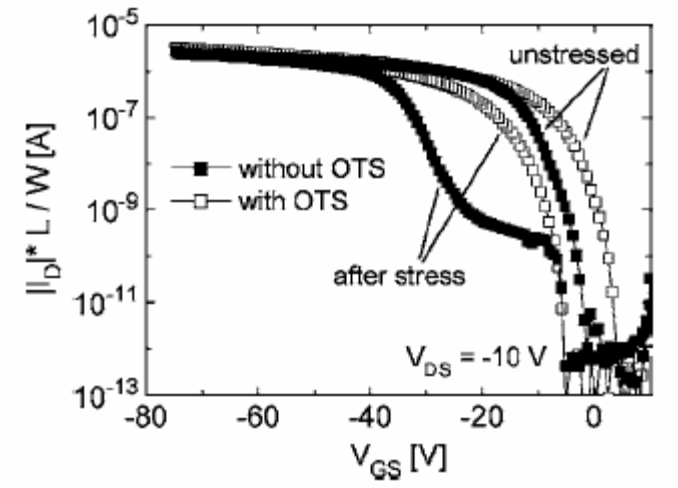

Figure 3.14: Electrical characteristics of pentacene TFTs with OTS treatment (open) and without OTS treatment (filled).[27]

A more commonly accepted possibility is that by changing the surface energy of the dielectric interface with surface treatments, the ordering of the organic semiconductor could be improved. Besides increased mobility through OTS, HMDS, or O_2-plasma treatments as seen in [28], larger grain sizes could be achieved through increased order. As trap formation is thought to originate at the molecular disorder present at the dielectric interface and grain boundaries, such treatments could reduce initial trap densities and decrease trap formation under applied stresses.

It is unlikely that water molecules could find stable absorption locations within crystalline organic grains, and more likely that they reside along grain boundaries. By simply decreasing disorder, the sheer number of locations for water molecules to reside may become limited. This concept is supported by the work in [24], where it can be seen in Figure 3.13 that bottom-contact devices incur more drastic on-current decreases with humidity. Since bottom-contacted devices generally have smaller grain sizes (and hence, more grain boundaries) due to

organic disorder at the electrode-insulator interface, it is not surprising that bottom-contacted devices show increased moisture sensitivity. Therefore, whether water vapor causes current changes through increasing the energy barrier for intergrain transport, through the screening of electric fields via ion charge, or through the generation carriers by dipole moments, increasing the molecular order should decrease the degree to which each could occur. Also, since grain boundaries aid in diffusion, more disordered films would more quickly incur electrical changes due to absorbing air-based contaminants. This is also partially demonstrated in Figure 3.13, as the bottom-contacted devices show a dramatic change after only 5 minutes of exposure at a given humidity. It is with this in mind that it is believed that surface treatments serve to increase molecular ordering of the film, and in turn reduce the electrical effect and rate of absorption of airborne contaminants such as O_2 and H_2O.

3.4 Conclusions

With the conducted experiments and literature review in this chapter, a significant understanding of the mechanisms for device degradation in ambient conditions has been developed. It is from this knowledge base that future devices can be specifically designed and passivated to enable organic devices to compete in the commercial landscape. However, while individual devices can exhibit acceptable performance and controlled degradation characteristics, few high-performance organic circuits have been demonstrated to date. As will be discussed in the next chapter, isolation in organic devices is another challenging endeavor and is another substantial hurdle to organic electronics entering the commercial space in RFID addressing technologies.

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Chapter 4: ACHIEVING ISOLATION IN OTFTS

Various cross-point arrays and other memory structures[30],[31] have been demonstrated to date, but providing integrated addressing for organic memories remains as a significant challenge due to needs for the close proximity of devices and an extremely low thermal budget. Organic semiconductors, which may be deposited at low temperatures and exhibit adequate performance[32], are a viable option. However, a method for patterning organic materials at high densities is needed to reduce cross-talk and resistive and capacitive parasitics from interconnects. Current isolation techniques cannot achieve the nanoscale pitches necessary for addressing organic memories.

4.1 Isolation Challenges

While off-state drain leakage can be reduced via thermal cycling, as in the previous chapter, much more progress must be made to enable devices to operate in close proximity without significant levels of cross-talk. This problem is much more significant in organic TFTs versus inorganic TFTs due to differences in operation mode. As mentioned in Chapter 2, OTFTs are accumulation mode devices. In other words, unlike inorganic FETs, the channel is in accumulation rather than inversion when the device is on. The result is that no depletion layer exists between the channel and the bulk, and current can flow readily between the two. To make matters worse, the conductivity of the bulk can be quite high for common organic semiconductors – between 4.7×10^{-6} S/cm and 2.4×10^{-8} S/cm for pentacene, depending on the substrate temperature during deposition [30]. Therefore, in order to have OTFTs within any relative proximity of one-another to create organic circuits, the current flow through the bulk organic material must be constrained.

There are several ways to extract the amount of current leakage this causes in actual devices. First, the drain leakage in off-state devices is, by definition, an excellent method to analyze this effect. This type of analysis was performed in the previous chapter, when the film conductivity was compared with the device mobility. However, when extracting the drain leakage, the result is somewhat convoluted due to a large gate leakage component. As shown in Figure 4.1, the leakage currents from the source and gate are additive in our test setup. While it is simple to individually extract the leakage emanating from the source, it became readily apparent that gate leakage played a much larger role.

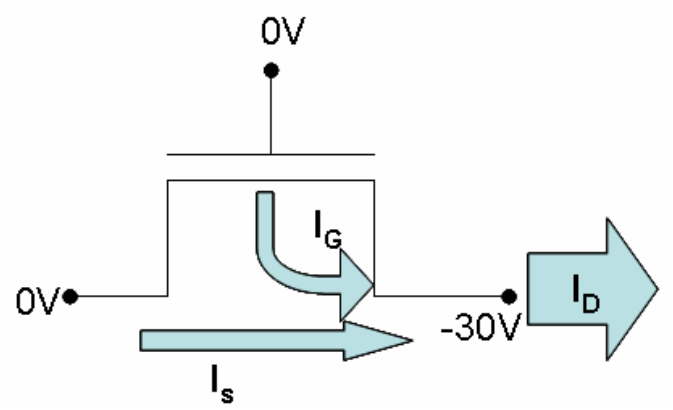

Figure 4.1: Leakage diagram of an off-state OTFT.

The source leakage component, I_S, originates from the ohmic connection between the contacts and the bulk. In fact, even when the device is on, drain leakage is a significant current component, as illustrated in Figure 4.2. While the leakage through the bulk is directly controlled by the film conductivity, limiting the film thickness can reduce this leakage component. In practice, the organic film thickness is kept to a minimum, with achieving complete surface coverage being a limiting requirement.

While initially surprising that such large gate leakage currents were observed, it made logical sense when the structure of the devices was taken into account. In the test devices generally employed for organic TFTs, the test wafer is used as a common gate for all devices, as in Section 3.1. Although the gate dielectric is both thick (>1000Å) and robust (thermally grown SiO_2), the conductivity of the off-state organic assists in gate leakage. In effect, the conductive organic film acts to increase the effective size of the drain pad, allowing current to fan out before penetrating the dielectric. As shown in Figure 4.3, the larger the conductivity of the film, the larger the effective drain size, and the larger the gate leakage through the fan-out effect.

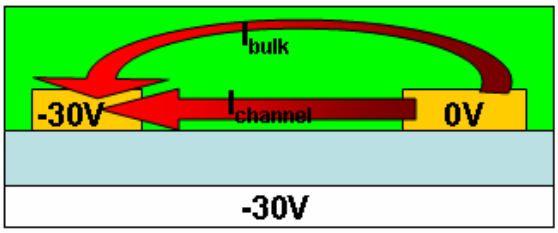

Figure 4.2: Bulk and channel currents through an OTFT in the on-state.

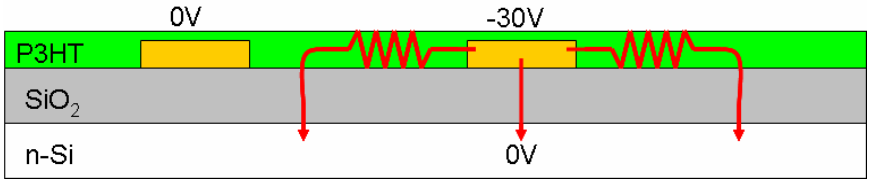

Figure 4.3: Increased gate leakage due to high bulk conductivity.

In actual organic circuits the OTFTs will be individually gated, and the OTFT described in Figure 4.2 and Figure 4.3 is generally only used as a testbed for other experiments, such as the integration of new materials or the inclusion of surface treatments, as in Chapter 3. However,

this gate leakage serves as an accurate metric to the extent of current spreading through the bulk organic material. By employing various isolation methods, measuring the gate leakage can actually give a better approximation of the spreading effect, and the amount of isolation achieved. In contrast, the leakage to the source electrode (0V) is generally much lower, and is more subject to system noise. Also, it can only establish leakage in a single lateral direction, whereas gate leakage captures the effect of the film being highly conductive in all lateral directions. As a result, both can be used in conjunction to give an accurate description of the cross-talk behavior of individually gated devices in an organic circuit.

4.2 Electron-beam Isolation

To date, the isolation of the organic thin-films has been obtained via shadow-masking[33], plasma etching with water-soluble resists[34], and UV laser ablation[35]. Here, we investigate the use of electron-beam irradiation to achieve electrical isolation on the nanoscale. While electron-beam processes are not viable for low-cost electronic thrusts, it is investigated to demonstrate electrical isolation in molecular memory addressing arrays, enabling high memory densities. Under this focus, organic TFTs are preferable because of their low-temperature fabrication process, as standard silicon MOSFET processing utilizes temperatures far above the thermal budget of molecular memory materials [36][37]. In the scope of the low-cost work presented in other chapters, it is believed that electron-beam isolation techniques could serve as a testbed and starting point toward low-cost isolation processes. By investigating the precise effects of energetic bombardment of the organic surface, methods such as intense UV exposure may be enabled as a viable low-cost alternative.

Of the various high-performance organic semiconductors currently in use, poly(3-hexylthiophene) (P3HT) and pentacene have been the most extensively studied, due to their

relatively high mobility[38]. The primary goal of this exercise is to demonstrate the ability of energetic electrons to physically break the molecular bonds along the organic chains, disrupting their conjugation. By locally altering the molecular backbones, it is theorized that bulk conductivity will rapidly decrease, and leakage currents can be drastically minimized. Using P3HT and pentacene, the sub-micron pattering and electrical device isolation of devices by electron-beam irradiation is investigated.

4.2.1 Experimental

Experiments were performed on silicon substrate-gated organic thin-film transistors (TFTs) with thermal SiO_2 dielectrics, as in Chapter 3, to ensure good repeatability. Gold contacts were evaporated onto a 100 nm thermally grown SiO_2 layer on an n-doped Si wafer. Purified poly(3-hexylthiophene) (P3HT) with greater than 98.5% regioregularity was obtained from Aldrich, mixed at 0.8 wt% in chloroform, and spin-cast in a nitrogen environment to achieve a film thickness of approximately 100 nm. While previous work[38] showed performance enhancement via an HMDS surface treatment, we observed no significant improvement in the electrical performance of P3HT devices, and thus this process step was not used. Pentacene was zone-purified and evaporated at 10 Å/min, with the substrate held at 80°C, to produce 30 nm films.

Electrical measurements were performed in a nitrogen environment at room temperature with most reported data gathered from devices with channel widths and lengths of 10 μm and 80 μm by 80 μm contact pads as shown in the inset of Figure 4.4. Channel widths of 1 μm and lengths of 0.5 μm were used to examine proximity scattering effects and precision patterning abilities. Devices were tested before and after irradiation so that comparative analyses could be made. Control devices were used on every sample. Baseline mobilities of the pentacene and

P3HT TFTs were 0.08 and 0.001 $cm^2V^{-1}s^{-1}$ respectively. Electron-beam patterning was achieved with a JEOL 6400 nanopattern generation system capable of resolutions down to 80 nm. A 20 KeV accelerating voltage was used with exposure doses varying from 5 to 1,000,000 μCcm^{-2}.

4.2.2 Results

To establish the minimum patterning dose, the channel region of both pentacene and P3HT devices was exposed to a wide range of electron doses. Figure 4.4 demonstrates that relatively low doses can have a significant impact upon the on-current and saturation mobility in both organic active layers. Compared to P3HT, pentacene films required a higher dose threshold to disrupt conjugation due to the larger bond strength within the pentacene molecule. The sharp negative slope both materials exhibit in Figure 4.4 is beneficial for reducing the effect of proximity scattering. Both materials show a curtailing of current reduction at higher doses, as parasitic FETs originating from the contact pads become the dominant current source. Thus, at high doses, the actual isolation is expected to be significantly better than predicted from Figure 4.4; this will be demonstrated below. For P3HT, the performance ratios both fall below unity for the control devices due to the degradation of the film with time. For the pentacene transistors, however, the on-current consistently increases in the control samples following the exposure procedure. This is likely due to outgassing while the sample is under vacuum in the e-beam irradiation system. Despite this, the doses necessary to alter the physical structure of each of the two organic active layers have been established, and the methodology for device isolation is therefore in place.

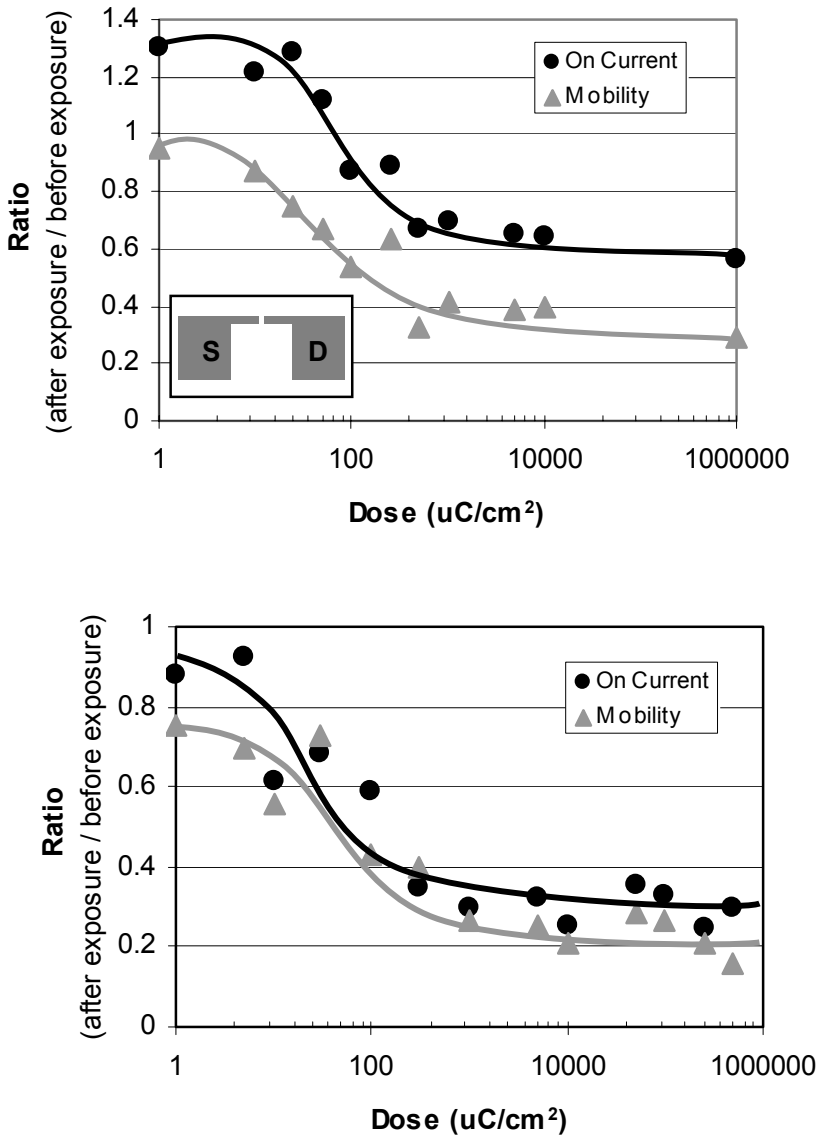

Figure 4.4: Effect of irradiation on saturation mobility and drive current of pentacene (top) and P3HT (bottom) films. Performance following exposure is compared to performance before exposure to give a performance ratio for all devices. Inset (top) shows the device test structure.

At doses above 10,000 μCcm^{-2}, the pentacene film was found to partially vaporize. It is important to note that significant changes occur in the electrical characteristics of the film at far lower doses. Unlike UV Laser ablation techniques, electrical properties can be altered without changes in topology, indicating that structural changes are occurring within the

pentacene molecule itself to disrupt delocalized carrier transport. Similarly, P3HT films do not begin to vaporize until doses exceed 300 μCcm^{-2}, well beyond doses that alter the mobility and on-current. Therefore, as opposed to wet and dry etching techniques to isolate neighboring devices, electron-beam irradiation physically changes the active layer into an insulator. This also indicates that appropriate tuning and sensitization of the materials and beam energies should enable the realization of a patterning technology providing both high resolution and reasonable sensitivity and speed.

Proximity scattering effects of the beam were also explored to determine the minimum pitch possible with this technology. As has been well established in electron beam resists, backscatter of electrons is expected to impose an ultimate limit on the resolution of this patterning technique. To test the degree of scattering in these films, lines 0.5 μm wide were drawn parallel to the current flow between source and drain electrodes 10 μm wide. While the area of the intentionally exposed area is only 5% of the total channel area, beam scattering could cause structural damage to a much larger portion of the channel. Our studies showed that for the cases of pentacene and P3HT beam scattering is minimal, and the currents accurately reflect the unexposed channel area. This indicates that the backscatter component is generally not significant, suggesting that nanoscale patterning should be possible.

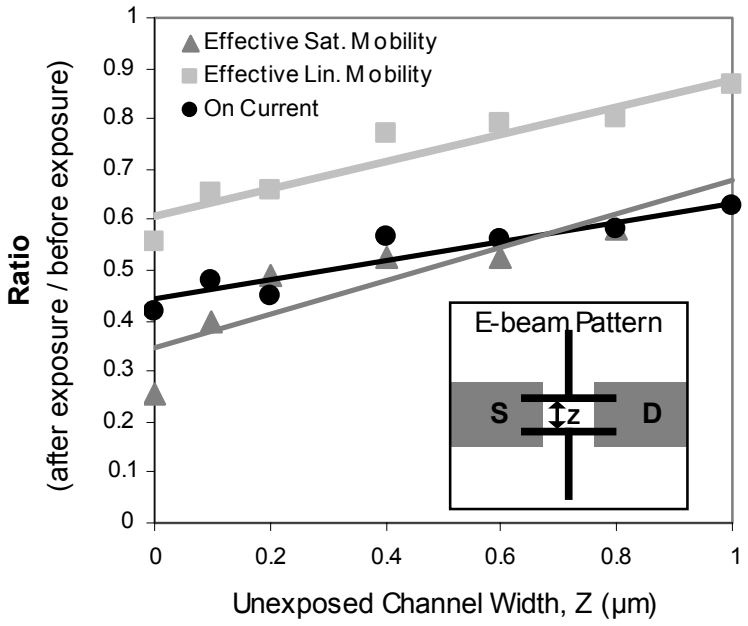

Figure 4.5: Changes in on-current and effective mobilities as the width of the unexposed region (Z) is varied. The inset shows the exposure pattern (black) relative to the source (S) and drain (D) electrodes. Electron dose = 10,000 μCcm^{-2}.

To further study the sub-micron patterning limitations, the exposure pattern illustrated in the inset of Figure 4.5 was used on pentacene devices. By gradually reducing the unexposed channel width of the exposure pattern, we are able to examine how the drive current scales. With an original device width of 1 μm, the width of the unexposed region is altered by 0.1 μm increments. The linear change in current shows that the effective unexposed channel width scales directly with the patterned line dimensions. The fact that current remains non-zero after the entire channel becomes exposed (Z=0) stems from the finite current that flows through exposed regions at moderate doses, as well as the parasitic FETs due to the large contact pads. This experiment shows that proximity scattering is far less than 0.05 μm, as the on current and effective mobility scale linearly with only a 0.1 μm exposure gap. This exposure pattern also used linewidths of 0.1 μm, demonstrating that thin exposure lines are capable of efficiently

eliminating current flow. By this result, devices could be theoretically placed with a pitch of 0.2 μm using e-beam isolation. Further scaling is likely possible with higher-resolution e-beam systems.

After establishing the doses and exposure linewidths necessary to inhibit current flow, as well as the proximity limitations, we implemented an optimized device isolation scheme for nanoscale organic devices. Figure 4.6 illustrates the dramatic device improvement that can be achieved through e-beam device isolation. For backgated devices, gate leakage currents can often be on the same order of magnitude as drive currents. In unpatterned organic semiconductors, the entire film enters a state of accumulation. This allows charge to fan out from the source and drain electrodes and increases the surface area over which charge tunnels through the SiO_2 dielectric. By tracing the perimeter of an entire pentacene TFT with a line 0.25 μm wide at a dose of 10,000 μCcm^{-2}, leaving a 1 μm border for alignment tolerance, gate leakage was reduced by three orders of magnitude, while drive current went unchanged. For comparison, e-beam isolation results in three times less gate leakage than devices isolated via mechanical scratching of the film. Off-state drain current (V_G=0V) was also drastically reduced following the e-beam isolation, resulting in a 5000X increase in the on/off ratio. Of equal importance, subthreshold swing significantly improves from 5 V/dec to 500 mV/dec, providing better turn-off characteristics, necessary for proper operation of large cross-point arrays.

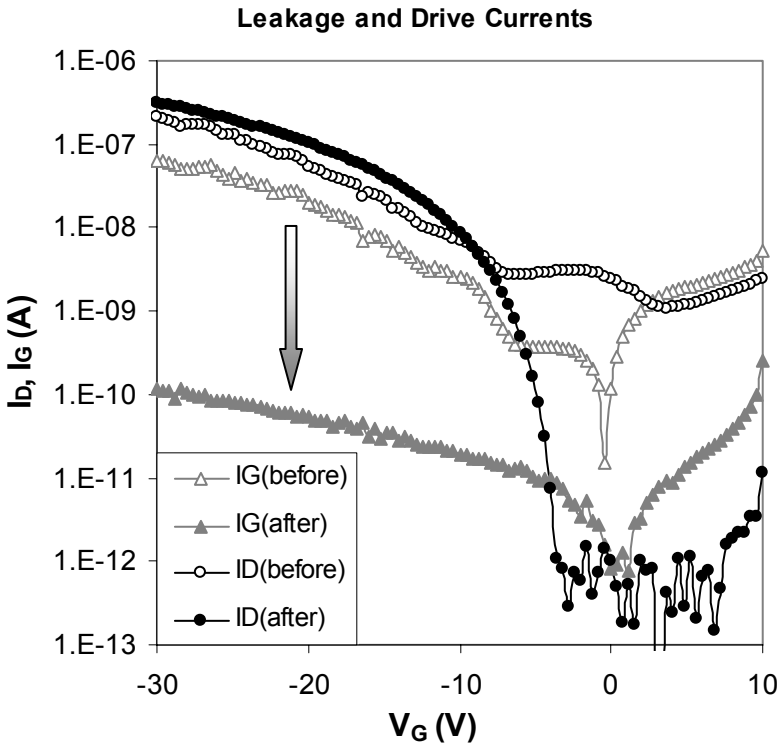

Figure 4.6: ID-VG characteristics measured before (open) and after (filled) electron-beam irradiation. W = 1 μm, L = 1 μm.

In conclusion, we have demonstrated an electron-beam electrical isolation technique for nanoscale organic devices. After exploring dosage effects and proximity scattering, we achieved isolation on both pentacene and P3HT TFTs. Significant improvements were attained in gate leakage, drain leakage, on/off ratio, and subthreshold swing at no cost to the on-current or mobility of the channel. The high precision of electron-beam lithography and the insignificant role of proximity scattering enable this technology to create tightly packed organic device arrays for addressing of molecular electronic circuitry.

4.3 PVA Isolation

While electron-beam isolation of organic devices has proven extremely effective and capable of great precision, electron-beam lithography is inherently expensive. Also, electron-beam lithography takes place in a vacuum chamber, and is serial in nature, severely limiting throughput. It has provided a proof-of-concept for the energetic disruption of conjugation along individual molecules, and perhaps provided insight to the development of cheaper alternatives with similar goals.

Perhaps the most obvious solution to achieving isolation in organic devices would be to selectively remove the semiconductor, directly preventing undesirable conductive paths. In standard inorganic processing, this would be a simple task; after blanket deposition, certain regions of the film could be masked with photoresist, and unwanted regions could be etched away. However, directly patterning organic films in this matter is nontrivial. In a standard resist processes the organic film is readily attacked by resist solvents, developer acids, and resist stripping agents. This result is not particularly surprising, considering the weak bonding nature of organic molecules to the substrate and each other. To combat this problem, a compatible resist process developed by Infineon was integrated in-house.

One of the few solvents that doesn't attack organic films is water, likely due to its highly polar nature. With this in mind, a water-based resist was developed using a combination of polyvinyl alcohol (PVA) and ammonium dichromate (ADC). PVA is a water-soluble resin produced by the hydrolysis of polyvinylacetate which is made by the polymerization of vinyl acetate monomer [39]. ADC is a photosensitizer added to improve pattern development. During the development of the resist process the relative concentrations of PVA and ADC were varied, along with the spin, exposure, and develop conditions. Before such optimization

could occur, challenges with dissolving PVA in H_2O had to be overcome. Initial work targeted 99% Hydrolyzed PVA, as the work by Infineon used PVA as a protective layer on top of the organic semiconductor. While a high degree of hydrolysis increases tensile strength and resistance to solvents, it dramatically decreases solubility in water [39]. As seen in Figure 4.7, at room temperature only extremely small concentrations of 99% hydrolyzed PVA are dissolved in water. Thus, depositing PVA films thick enough to withstand the organic etching process (to be described later) became challenging through spin-casting, as minimum spin speeds are needed to maintain uniformity across the sample. Given the information of Figure 4.7, 87% hydrolyzed PVA was used to increase PVA concentrations in solution. Although this film demonstrated poorer solvent resistance, it was determined to be not relevant in this electrical isolation process because other layers could be deposited post-isolation to passivate and protect the film.

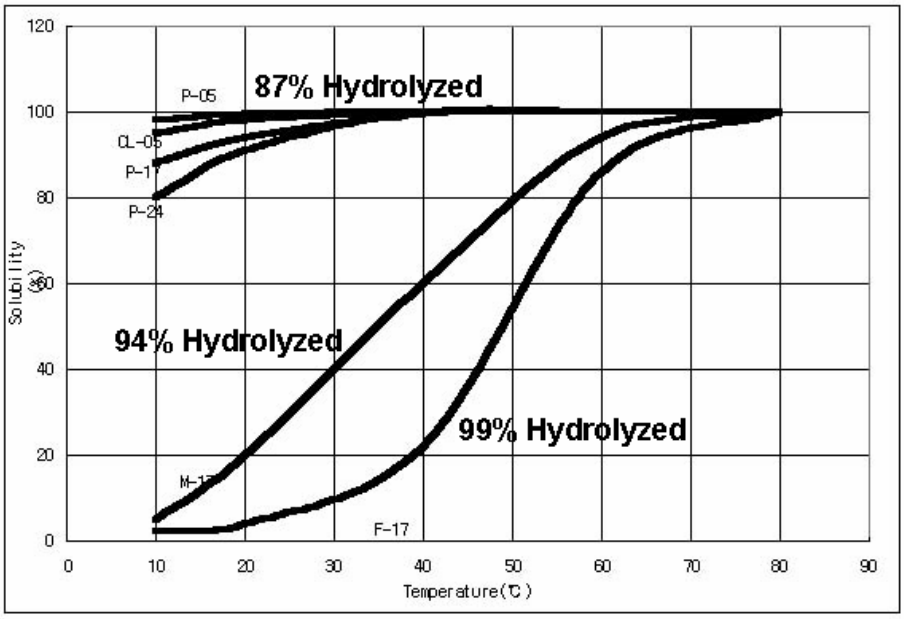

Figure 4.7: Solubility of 4% by wt. PVA in water by degree of hydrolysis [39].

4.3.1 Experimental Setup

As in Section 4.2, backgated wafers were used to test the isolation capabilities. As before, wafers were composed of gold source/drain pads placed on the surface of the thermally grown SiO_2 dielectric. For the PVA isolation technique, only pentacene was investigated, though the simple nature of the experiment lends itself to other organic semiconductors. Pentacene was thermally evaporated at 10Å/min with the substrate held at 80ºC to achieve 30nm films.

After much experimentation, optimum solution composition and spin conditions were established. For best results, PVA was mixed with water at 4% by wt., and ADC was added at 0.05% by wt. A vortex mixer was needed for up to two hours to completely dissolve the PVA in the solution. The solution was then filtered with a 0.25μm Teflon filter to remove any particulates that could create inconsistencies during the spin. The solution was poured onto the wafer at 0RPM, which was then spun at 4000RPM for 25 seconds. No pre-exposure bake was used, as PVA demonstrated rapid hardening and reduced photosensitivity with the application of low-level heating. The PVA was then exposed using a standard photomask in a stepper. The exposure time varied widely, depending on the underlying surface. Effective patterning of PVA on top of aluminum or SiO2 took a 0.8 second exposure, while patterning PVA on top of pentacene took 3.0 seconds. This is partially due to the lack of reflectivity of the pentacene surface, eliminating the double-exposure of PVA through reflection off of the underlying layer. Another possibility is that the PVA spin may have produced a thicker film on the pentacene due to adhesion issues, roughness, or the change in surface energy. Nonetheless, proper exposure conditions were verified to obtain the best possible feature definitions. Following exposure, the film was developed in a water bath for two minutes, resulting in the structure of Figure 4.8 (top). A significant amount of PVA mass loss was

identified, although accurate measurements could not be made with profilometry, since the roughness of the pentacene film made the accurate determination of step height impossible. To harden the PVA film, it was post-baked at 120ºC for 20 minutes. Finally, the sample was exposed to low-power O_2 plasma to etch the organic and achieve isolation. For these 30nm pentacene films, the optimum etch conditions were 40W for 45 seconds. As can be seen in Figure 4.8 (bottom), the channel is protected while the pentacene material outside the channel is etched.

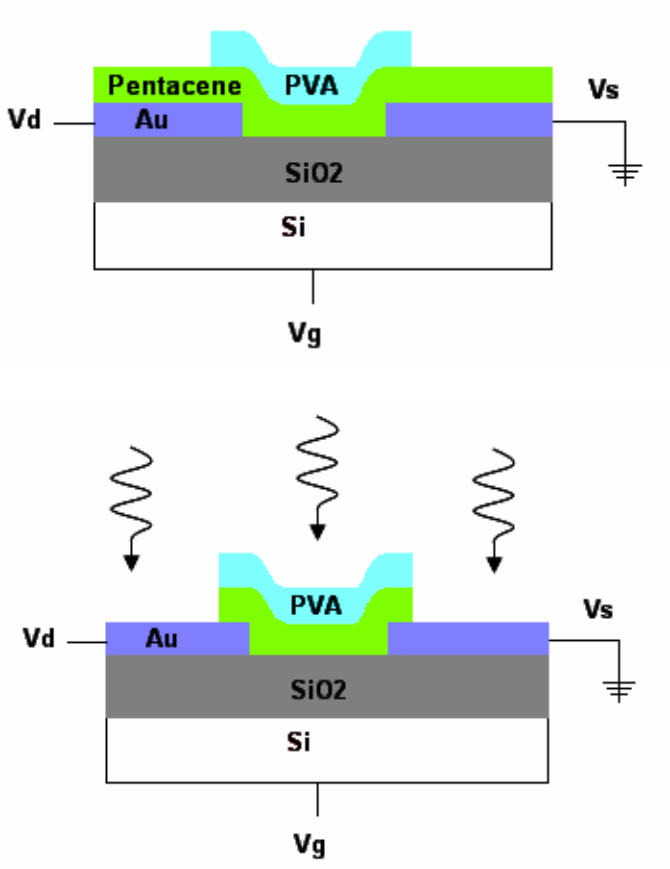

Figure 4.8: PVA isolation after development (top) and after O_2 plasma etch (bottom).

4.3.2 Results

Unlike the e-beam process, where the conjugation of the molecular backbone was broken, this process physically eliminates the organic material. As a result, absolute isolation can be achieved, enabling devices on pitch with standard lithography equipment. Figure 4.9 shows how the O_2 plasma etching process significantly reduced off-state drain leakage and gate leakage, without harming the transistor performance. In fact, the slight decrease in drive current seen in Figure 4.9 is due only to the decrease in gate leakage, which had acted additively on the current levels of the device, due to the testing setup of Figure 4.1. The PVA isolation process successfully decreased gate leakage by four orders of magnitude, and as a result, drastically improved the on/off ratio of the transistor. The subthreshold swing was not as steep as in e-beam isolation, and the entire batch showed positive threshold voltages, indicative of high trap densities. However, device testing prior to PVA isolation showed positive threshold voltages as well. It was concluded that the slow turn-on was merely a result of the poor pentacene quality at the time of deposition, and not a result of the PVA process. The gate leakages that remained after isolation were similar in magnitude to the leakages of the e-beam isolated devices of Section 4.2. For reference, the leakage through the gate dielectric before the organic deposition was measured. As shown in Figure 4.9, the gate leakage due solely to the metal electrodes (Pad Leakage) is similar to the gate leakage through the PVA isolated device. Because of this, it can be ascertained that the isolation achieved in the PVA process is extremely effective.

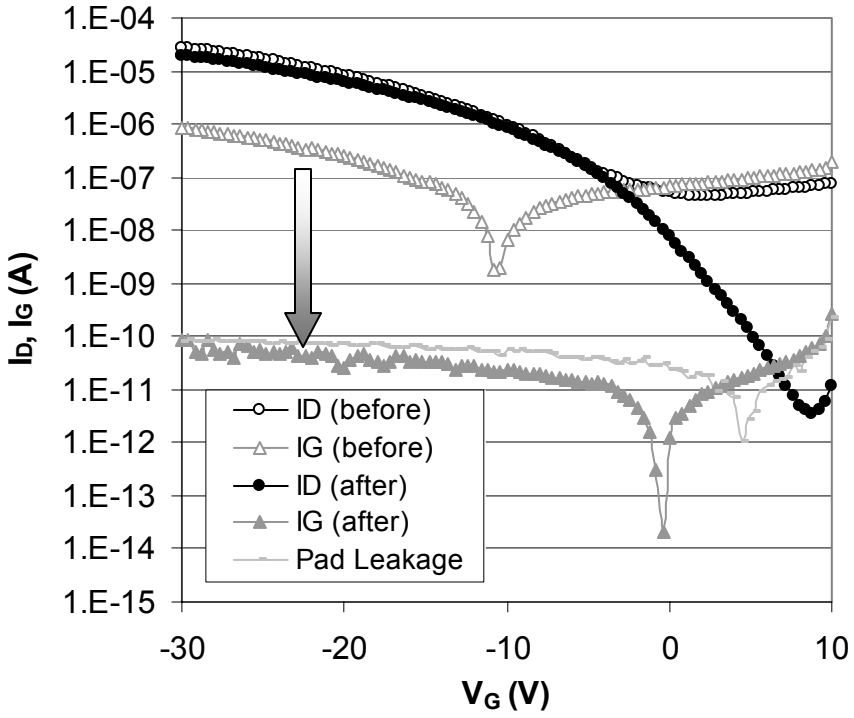

Figure 4.9: Electrical isolation achieved with a PVA etch-mask, showing I_D and I_G before and after the isolation process, with the electrode-only leakage shown for reference. W=L=10μm, Tox=100nm, and V_{DS}=-30V.

Although the precision is not to the nanoscale like the e-beam process, PVA isolation can be achieved in the range of single microns. In this experiment, the overlap of the PVA layer to the gold source/drain pads was 2μm, which proved more than sufficient. This is not surprising, considering the anisotropic nature of the O_2 plasma etch. The actual limits were not explored, since the manual alignment of our stepper system is extremely unreliable at this scale. Nonetheless, this process can allow independently gated OTFTs to reside within 2μm of one another, which is acceptable for the creation of low-cost memory addressing arrays. While a fully-printed reel-to-reel process would directly control the organic placement through an additive process such as inkjet printing, the printing accuracy is not currently capable of creating isolated devices within 20μm of one another. As a result, PVA isolation provides an

intermediate process for the creation of dense organic circuits, which in turn reduces the material costs of printing gold electrodes over wide areas.

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Chapter 5: TOP-GATE

In creating an addressing array for RFID, each organic FET will need its own discrete gate electrode. Up to this point, all of the OTFTs demonstrated have used a highly-doped silicon wafer as a common gate. While this is excellent for creating a testbed for experimentation with novel techniques such as electron-beam isolation, it is an unrealistic solution to the addressing problem. To create the addressing circuitry for a dense memory array, organic transistors with individual gates and electrical isolation from one another will be needed. As visualized in Figure 5.1, the organic FETs can be used to interrogate memory bits of a cross-array system at high pitch.

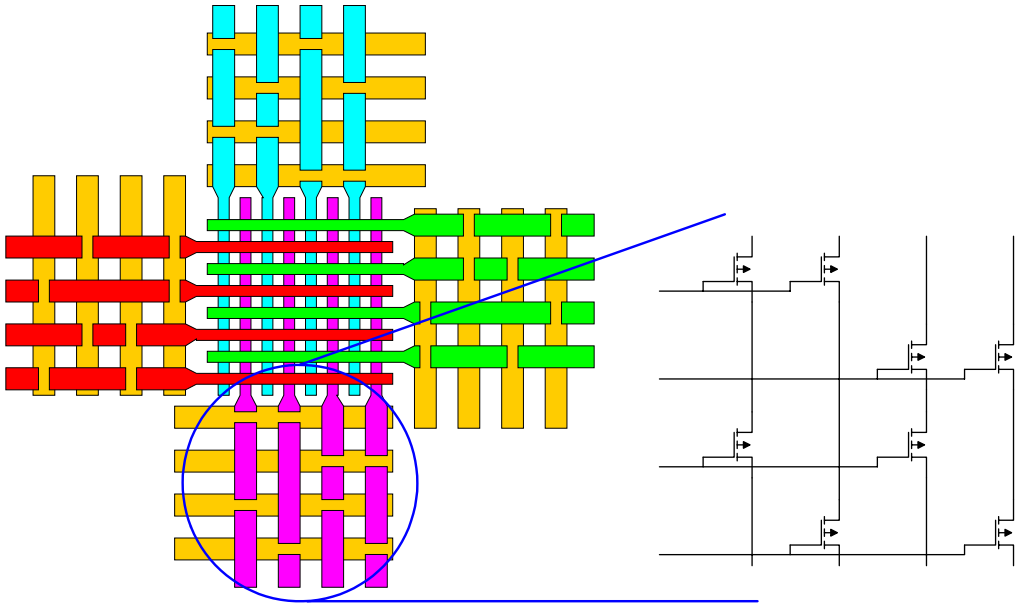

Figure 5.1: Demultiplexer addressing scheme using organic FETs. Linewidth of center lines would be pushed to the limit of the lithography tool to create high memory density, while addressing line widths would be doubled, enabling higher drive currents through the OTFTs.

5.1 Design Needs

Besides the need to be individually gated, the process for these addressing FETs will need to be compatible with the reel-to-reel fabrication technology to enable low-cost. This means that all materials must be printing-compatible, and that vacuum-deposition methods be avoided at all costs. Finally, being reel-to-reel compatible means that the thermal budget of fabrication must be below the limits of the PEN plastic substrate.

Most individually-gated devices to date are bottom-gated devices on silicon wafers with vacuum-deposited dielectrics on the metal gates [41][42]. An example of this bottom-gated structure is shown in Figure 5.2. While these processes have demonstrated devices on glass substrates, the use of vacuum processing is not inline with the goals of reel-to-reel fabrication. Although some recent work has demonstrated the use of PVP dielectrics with the bottom-gated structure in a printable process [43] (Figure 5.3), extra passivation steps would need to be taken to prevent environmental contamination of the organic layer. In the process developed here, built-in passivation of the organic layer is preferred, as it enables the construction of reliable and robust organic circuits.

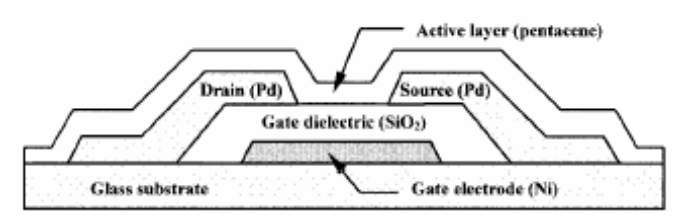

Figure 5.2: Bottom-gated OTFTs using reactive ion-beam sputtering of the SiO2 gate dielectric [41].

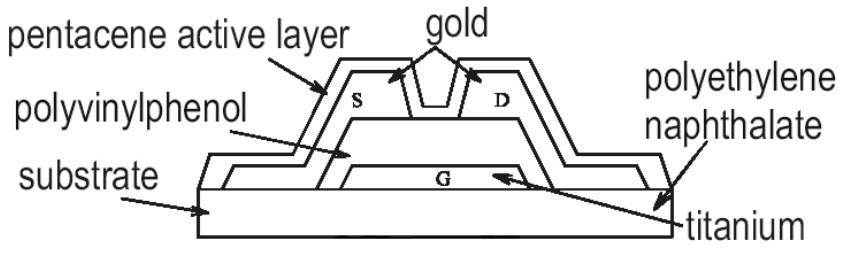

Figure 5.3: Bottom-gated organic TFT on a PEN substrate [43].

5.2 Top-gate Structure

To build the device, the process flow of Figure 5.4 was followed. First, a highly doped, thermally oxidized wafer was taken as a base substrate. This substrate was chosen so that a single device actually enables a back-gated device to be built in parallel to the top-gated device. Thus, the mobility and on/off ratio of the top-gated device can be directly compared with a baseline device. Since liftoff will be used to pattern the source/drain electrodes, G-line resist is spin-cast and patterned. 25Å Chrome is evaporated for adhesion purposes, followed by 500Å of gold. By immersing in a sonicator, the liftoff patterning proceeds. Next, 300Å of pentacene is evaporated at a rate of 6-10Å/min. The substrate is held at 80ºC to promote higher pentacene ordering. Next, a 5% by wt. PVP solution in 2-propanol was spin-cast onto the pentacene, as in [44]. The solution was poured at 400RPM, and ramped to 6000RPM for 45 seconds. The PVP film was cured at 100ºC for 10 minutes. A blanket aluminum film 850Å thick was evaporated to form the gate electrode. Through experimentation it was found that although pentacene and PVP were sensitive to most solvents, they were resilient to phosphoric acid- the primary etchant of aluminum. It was also found that the PVP-Al stack successfully protected pentacene from the weak acids of common developers, which had been shown to attack pentacene. Thus, G-line resist was spin-cast, exposed, and developed on top of the Aluminum. After hardening at 120ºC, a wet etch of the aluminum was performed with a

heated bath of concentrated H_3PO_4. This process also weakened the exposed PVP, but since the critical PVP gate dielectric is underneath the aluminum, it is inconsequential. One challenge with this structure is that after the aluminum patterning, there is virtually no way to remove the hardened resist from the top surface. Thus, all electrical measurements were made by scratching through this resist to contact the gate electrode. It would be possible to alleviate this situation by performing a two-step aluminum etch, where half the aluminum is initially etched, followed by the ashing of resist, and finally the second half of aluminum is etched. However, since obtaining electrical contacts to the top surface was achieved, it was decided that the added process complexity was not worth the gains.

It is important to note that the entire fabrication process proceeds below 120ºC, which is well within the acceptable range for a plastic substrate. Also, the entire process enables the vertical stacking of these OTFTs. This means that this technology could be used to address vertically stacked memory arrays so that each memory level is provided with its own set of in-plane addressing circuitry. Thus, the number of vertical layers of memory would not be limited by the needs for each layer to connect to address circuitry through vertical vias. Indeed, this is the case in vertically stacked memory systems that use a single planar level of MOSFETs for addressing [45].

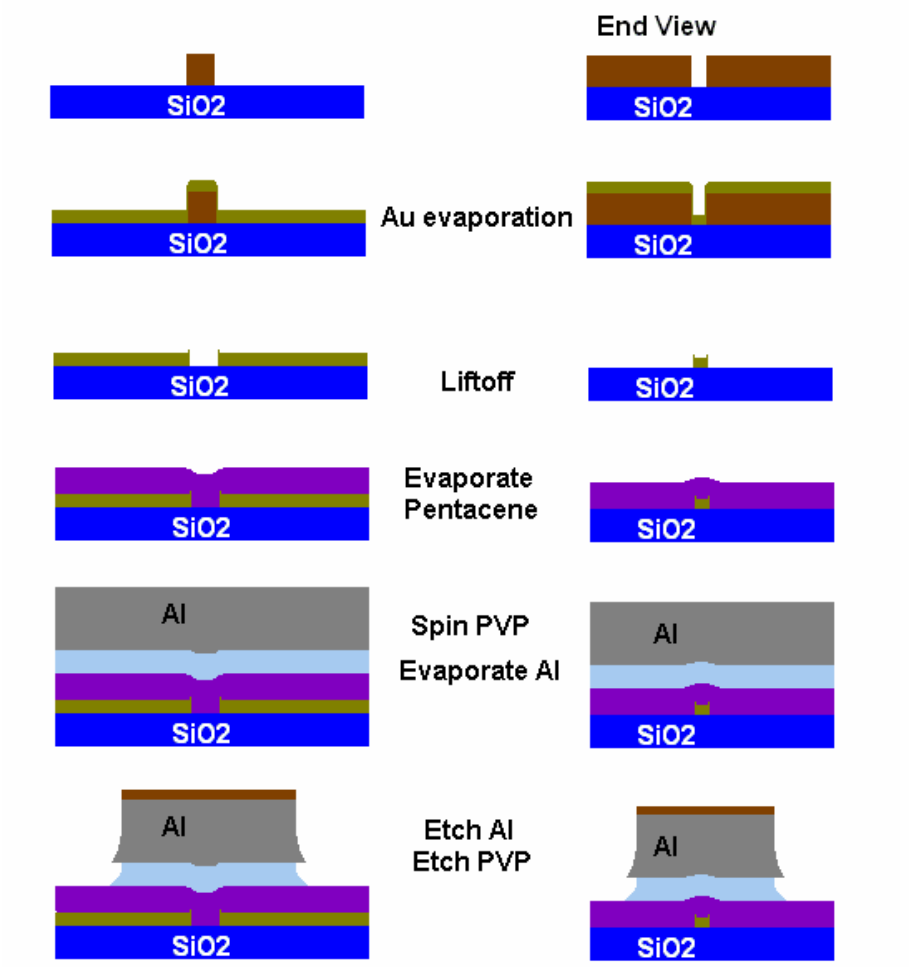

Figure 5.4: Process sequence for fabricating a top-gate device.

5.3 Electrical Characterization

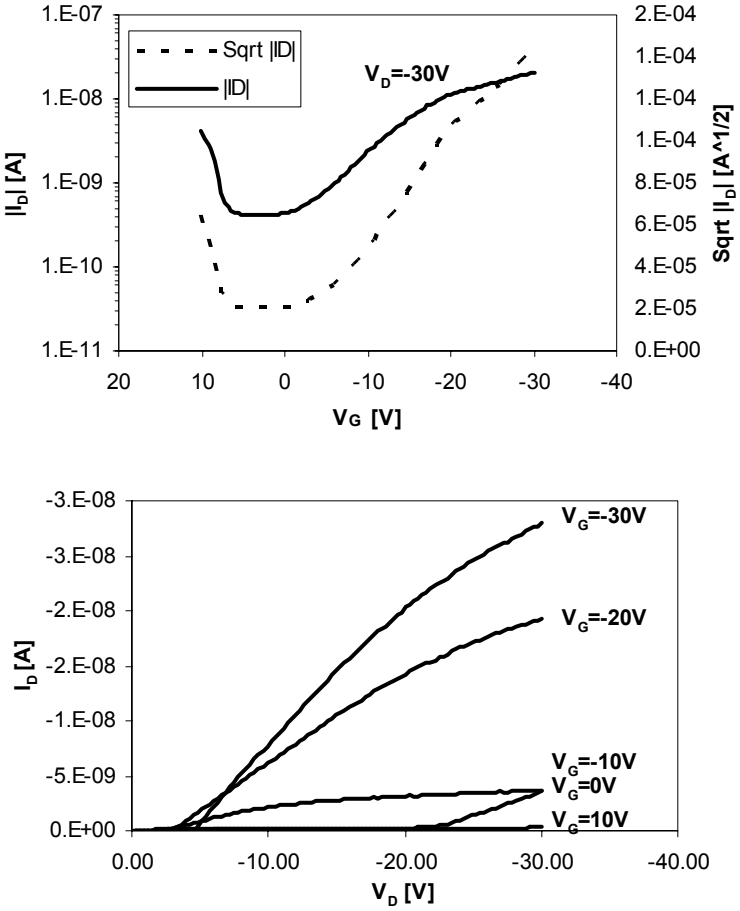

Figure 5.5: I_D-V_G and I_D-V_D curves for a top-gated device.

The electrical characteristics of an average-performance top-gate device are illustrated in Figure 5.5. Although not outstanding, the performance demonstrated is respectable for an organic device without isolation. The devices demonstrate an on/off ratio of approximately 50, and a mobility of 0.0006 cm^2/Vs. Although these values are low, in-house back-gated devices using the same pentacene layers did not fare much better. As was mentioned previously, the top-gate was fabricated on an oxidized wafer so that the back-gated device could be tested for reference. The I-V curves for the back-gated device that utilizes the exact same pentacene

channel as the device of Figure 5.5 is shown in Figure 5.6. The mobility of the reference device was roughly 0.0007 cm^2/Vs, and the on/off ratio was approximately 200. The better off-state current was achieved because the thermally grown SiO_2 dielectric is far more robust than the PVP dielectric of top-gate. However, the biggest problem lies in the gate leakage component due to the current fan-out effect of Chapter 4. This gate leakage is plotted in Figure 5.7 for the top-gated device, and its effect on on/off ratio is apparent. This is to be expected, as no isolation procedures were included in the device construction. In fact, the role of the gate leakage can be seen in the I_D-V_D curve of Figure 5.5. The gate leakage has caused the curves to show negative current at V_D=0V. As a result, larger gate voltages cause the zero-current points of the curves to shift right.

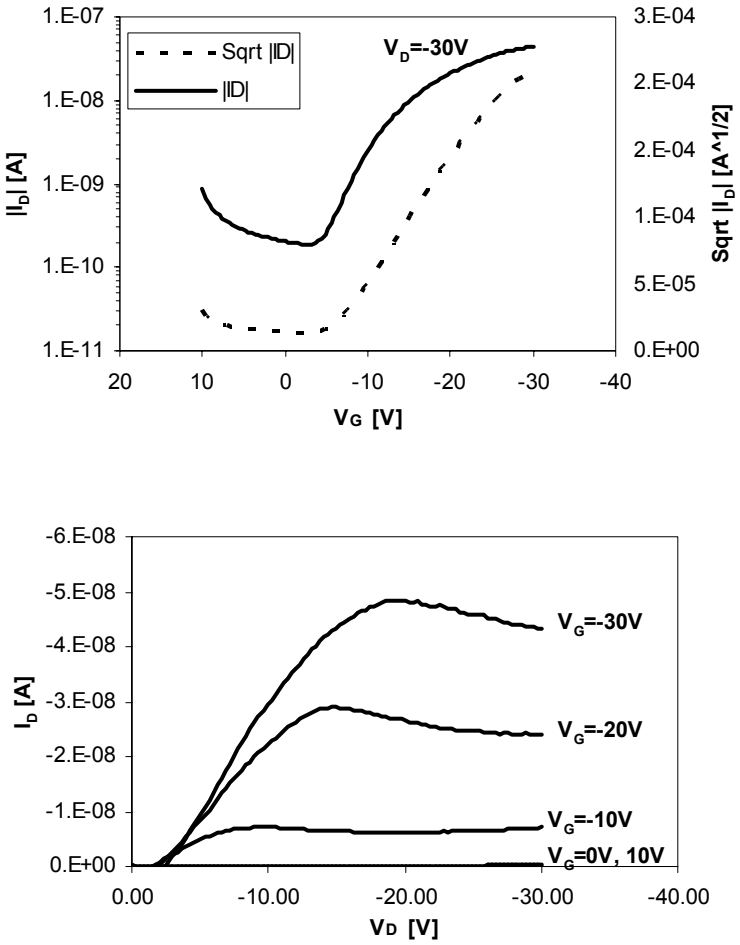

Figure 5.6: I_D-V_G and I_D-V_D curves for a bottom-gated device.

From the plots of the square-root of the drive current vs. gate voltage, it can be seen that the threshold voltages for both back-gated and top-gated devices resides between 0V and 3V. The fact that no significant shift is observed for the top-gate device indicates that minimal trap densities occur at the PVP-pentacene interface. Finally, unlike the back-gated I_D-V_D curves, the top-gated I_D-V_D curves do not demonstrate the negative differential resistance at high voltage associated with bias stress and self heating.

The top-gate structures showed performance on-par with their back-gated counterparts, which is extremely impressive. The fact that no significant performance loss occurred means that with better pentacene films, these devices could perform on-par with the best organic FETs. The built-in channel passivation also means that top-gate devices may result in more environmentally stable circuits for memory addressing.

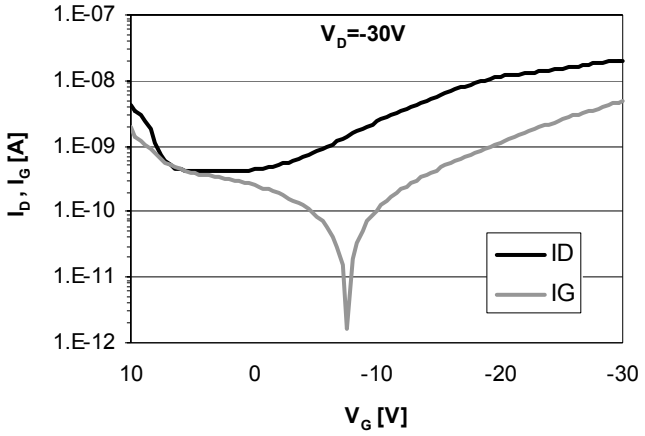

Figure 5.7: Gate leakage vs. drive current in a top-gated OTFT.

5.4 Printed OTFT developments

When the top-gate work was pursued, printing was only used to deposit the organic semiconductor onto backgated silicon wafers using thermally grown SiO_2 as the gate dielectric. Since then, much progress has been made, as other members of this research group have demonstrated fully-printed organic TFTs on plastic using many of the same materials investigated here [46]. Top-gate served as a testbed for material interactions, and investigated the feasibility of in-house pentacene-PVP based FETs. Top-gate also served as a new means to establish environmental passivation of the organic layer via the gate dielectric, which had not been previously investigated in literature. Finally, top-gate proved the functionality of a

vertically-stackable process flow. This technology, combined with isolation and annealing optimization from the previous two chapters, enables the creation of robust high-performance organic TFTs for the addressing of vertically stacked memory arrays on plastic.

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Chapter 6: ANTIFUSE MEMORIES

With organic electronics associated with the concept of low-cost electronics, a novel memory device utilizing organic semiconductors would be of considerable value. Besides obvious applications in organic RFID circuits, a low-cost organic memory element could create new applications in disposable memory. By utilizing organic materials, the use of flexible substrates for memory elements also becomes a marketable advantage. Having an organic memory technology that can be integrated with reel-to-reel printing technology is also of paramount importance in achieving low costs.

With no suitable memory technology present in literature, we focus upon the creation of a novel organic memory system based upon the work done in amorphous silicon antifuse devices. This chapter starts by exploring the history of metal-insulator-metal inorganic antifuse devices and establishing their operation mechanics and limitations. Diode-integrated inorganic antifuses are then analyzed, and operational aspects are critiqued.

6.1 Basic Principles

In the most basic configuration, antifuse memories are simply the opposite (anti-)of a fuse - initially minimal electrical conduction occurs, and once pushed to its limits with an electrical load, it conducts well. This describes the process of the physical breakdown of an insulating material. In this breakdown process, a conducting filament forms through the dielectric after a given electric field is placed across the dielectric [48]. This filament formation process is described in Figure 6.1. Although this example uses HfO_2, the process is considered universal for the breakdown of oxide-based dielectrics. In Phase I of this process, an electron

percolation path is established, generally along the grain boundaries of the dielectric. As more current flows through this path, Joule heating occurs. This leads to Phase II, where the percolation path dilates due the increasing Joule heating. In Phase III, the Joule heating becomes so intense that the contact material melts (be it silicon or a metal), and atoms from the contact can be "sucked" into the percolation path. In some cases, the atoms diffuse in through substitutional defects present in the dielectric, with the diffusion rates drastically increased by the localized heating. Other times, atoms are introduced through the intense electron wind, as filament growth can appear asymmetric [49]. In the case of silicon (and some metal) contacts, a self-healing insulating cap (SHIC) can form, generally forming an oxide with the electrode material, as shown in Phase IV. This results in devices with filament growth to revert to a non-conductive behavior. Finally, in Phase V, the SHIC can be ruptured via the extrusion force placed upon it from the filament underneath.

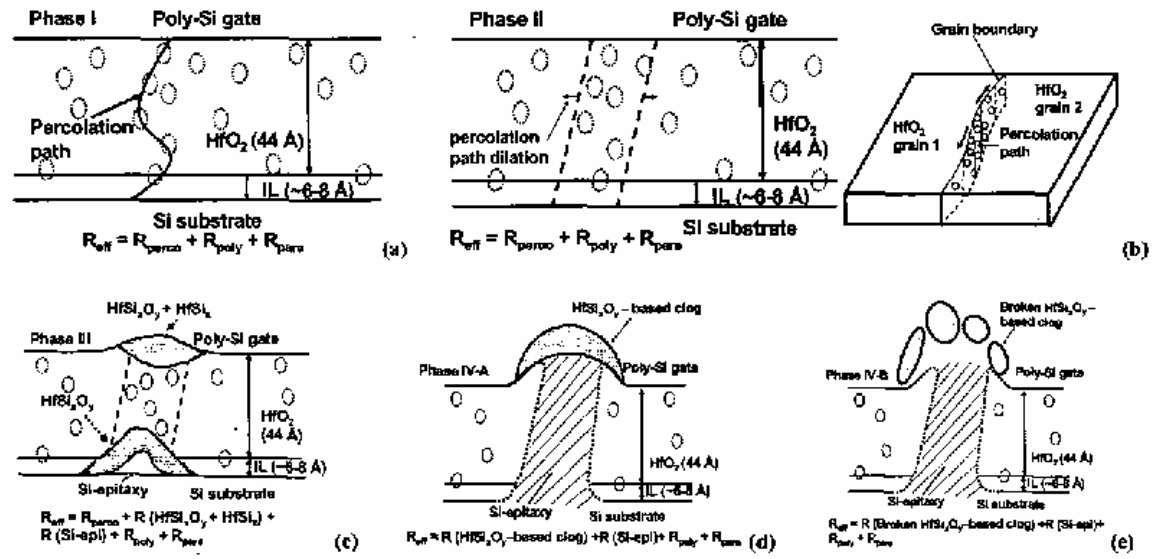

Figure 6.1: Filament formation in a HfO2 dielectric. (a) Phase I - path formation, (b) Phase II - path dialation, (c) Phase III - dielectric breakdown induced epitaxy (DBIE), (d) Phase IV - self healing, (e) Phase V - ruptured insulating cap [48].

While the breakdown event is controlled by the applied electric field, the power flowing through the device ultimately defines the diameter of the filament. With higher power, more Joule heating occurs during Phase II, and more contact material becomes pulled into the dielectric in Phase III. As a result, the filament exhibits lowered resistance.

Organic films have also shown the ability to be programmed via high electric fields. In the work by Ma *et al.* [50], metal nanoparticles were suspended between two organic films, and bistable behavior was achieved. However, unlike filament formation, these devices were able to return to the non-conductive state with an applied reverse bias. This was attributed to the encapsulated nanoparticles serving as charge transfer sites, enabled by Fowler-Nordheim tunneling under high electric field [51]. Under this theory, the HOMO of the organic becomes partially filled, and carrier generation results in high conductivity. This theory would works well for these switchable devices, as the encapsulated nanoparticles are expected to be immobile, due to their large size. It also enables the bits to return to the off-state with the application of a reverse bias, as the charge is removed from the nanoparticle sites [51].

However, for the organic devices studied here, filament formation has been achieved as an irreversible programming effect. In work by Tondelier et al. [52], pentacene films of certain thicknesses showed the ability to be programmed under high bias. In this process, it was proven that small nanoparticles from the evaporated electrodes reside near the polymer surface. Upon the application of high bias, the electric field induced the percolation of nanoparticles through the dielectric [52]. This flow of nanoparticles could be through charge trapping within the nanoparticle, causing an electronic force upon it, or just through random-walk processes. As grain boundaries have increased defect sites promoting diffusion, random-walk is not out of the question. Either way, nanofilaments have been demonstrated, similar to

the situation of Phase II of Figure 6.1. Even if a physical filament is never formed from the melting of the contact materials, the high density of nanoparticles serve as high probability tunneling sites, enabling step-wise conduction. This nanoparticle filament theory is far more compatible with the devices demonstrated later, as devices retain their programmed state even if a reverse bias is applied. Although it is unlikely that an SHIC is formed, due to the lack of compatible materials in the system, healing can still occur with this theory. It is likely that the nanoparticles relax upon the removal of bias and migrate back towards the contacts under a diffusion time constant. Thus, the idea of filament formation for organic films, although different from inorganic systems, effectively describes the same electrical breakdown behavior. This filament formation is the enabling mechanism for all inorganic antifuses, as well as the organic antifuses developed Chapter 7.

6.2 Metal-Insulator-Metal Antifuse Background

Although the metal-insulator-metal (MIM) antifuse was first developed by IBM in 1954, it was not employed in a commercial application until 1988 by Actel. The antifuses were first used in the Quicklogic family of FPGAs, and similar forms are used in today's Axcelerator chips. One of the primary benefits of antifuses in FPGAs is their small area consumption, as they are vertically constructed devices, and consume the area of a contact or via [53]. By programming antifuse bits, the FPGA elements are connected in custom ways, enabling a unique user-defined circuit.

The first MIM antifuses developed used a simple CVD oxide or amorphous silicon layer sandwiched between two metal electrodes [53]. While functional, these devices showed high leakage through unprogrammed bits, poor reliability, and wide resistance distributions of programmed bits [54][55]. As an alternative, a stacked silicon dioxide-silicon nitride-silicon

dioxide (ONO) dielectric was developed that demonstrated improved electrical characteristics [54]. In Figure 6.2 (left), the ONO antifuses showed a much tighter resistance distribution, aiding in fault tolerance. The reduction in leakage current for the ONO dielectric versus other dielectrics can be seen in Figure 6.2 (right). The decrease in leakage current between the metal/NON/metal antifuses versus the N+/ONO/poly-Si antifuses is largely attributed to the higher processing temperatures enabled by the use of doped silicon contacts. Nonetheless, it is apparent that both nitride-infused structures fared far better in terms of leakage than oxide –only antifuses. This is fairly simple to understand, as oxide is a robust dielectric that requires high breakdown fields to fail. As a result, to tailor this material to break down at a low voltage, an extremely thin film would be needed. The result is that direct tunneling current through the thin silicon dioxide results in increased leakage. For comparison, a much thicker nitride layer can be constructed that breaks at a similar voltage, due to the lower breakdown fields needed for nitride. Therefore, quality antifuses require low-leakage dielectrics that demonstrate breakdown at relatively low electric fields.

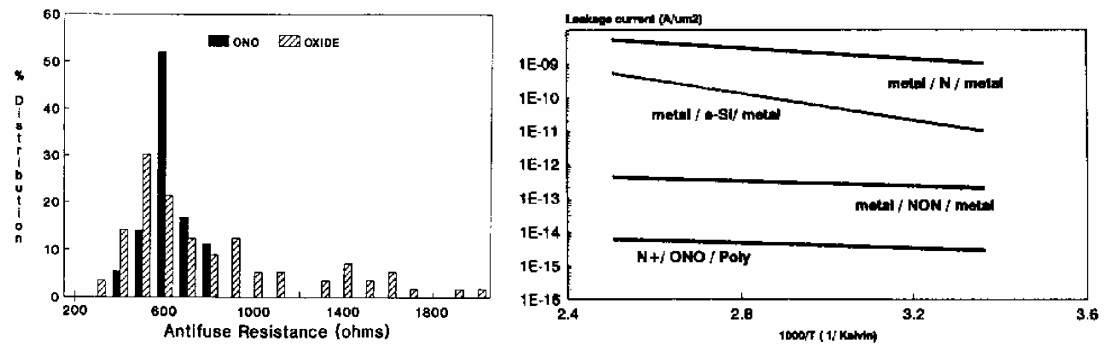

Figure 6.2: MIM antifuse resistance of programmed bits [54] (left) and leakage current through unprogrammed anftifuse bits of different technologies [55] (right).

ONO antifuses also show better reliability, as seen in Figure 6.3. In this plot, the unprogrammed antifuses are placed under varying low-level bias stresses, and the time dependent dielectric breakdown (TDDB) (the time until accidental programming occurs) is graphed on the y-axis. At a given bias, ONO antifuses showed lifetime increases of several orders of magnitude. As a result, ONO antifuses are the primary MIM antifuses in production today, and will remain so into the foreseeable future.

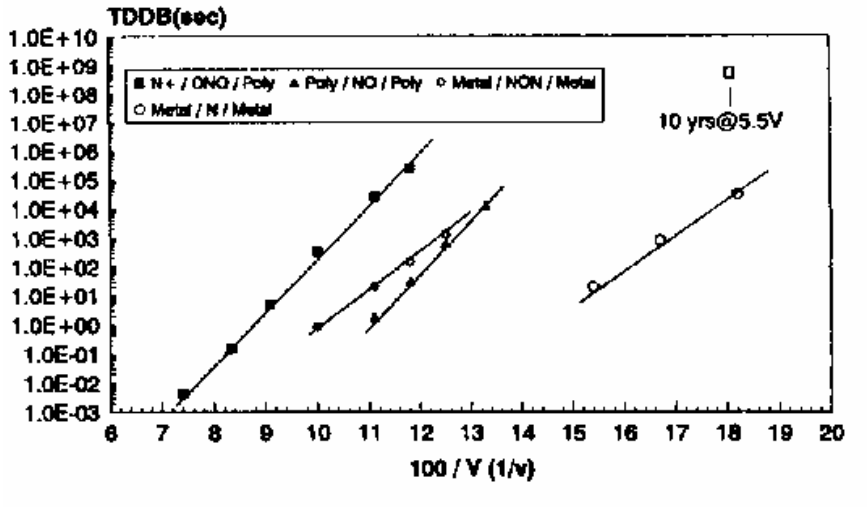

Figure 6.3: Extrapolation of lifetime of unprogrammed antifuses under constant voltage stresses [55].

Despite the advancements of Flash technology, MIM antifuses have found a niche in space-based applications. Whereas flash stores the bit as suspended charge on a floating electrode between the gate and channel of a transistor, antifuses are programmed through a physical damaging of the dielectric. In space, where large amounts of cosmic radiation penetrate the chip, charge stored on a floating electrode would be compromised. MIM antifuses have proven far more robust to radiation, and Antifuse-based FPGAs are common among satellites and spacecraft.

Antifuses have also been used by the likes of Intel Corp. [56] and others to create multiple versions of a single processor. In this method, certain regions of SRAM caches can be connected via antifuse, so that a single fabrication process can host a family of chips with different capabilities. This allows the manufacturer to cheaply define the chip identity during the electrical testing process.

6.3 Metal-Insulator-Metal Limitations

The integration of diodes into the antifuse structure is critical for the programming and error-prevention processes. While metal-insulator-metal (MIM) antifuses serve as discrete elements with a nonvolatile memory, they are not a viable option for high density memory cross-arrays. This is due in large part to the pull-up and pull-down effects of programmed bits, and the relatively low resistance of programmed bits.

In a common situation, large numbers of cells in a MIM cross-array could be programmed if special care is not taken. Figure 6.4 shows how such a situation could occur in a MIM array where the non-active lines are floated. If we take MIM antifuse "A" as the bit to be programmed, we would raise wordline 1 to a high write voltage (+W) and set bitline 1 to ground. However, if any bit along wordline 1 had been previously programmed, then there would be a short to the respective bitline (bitline 2 in this case). This would cause a bitline that was previously floating to be pulled up to the +W. Similarly, any bit along bitline 1 that had been previously programmed would allow the respective floating wordline to be pulled to ground. The result is that at the intersection of any pulled-up bitlines and pulled-down wordlines would result in the accidental programming of an MIM antifuse (the case of antifuse "C" in the figure). In fact, from a programming perspective, it would be indistinguishable to the outside user whether antifuse A or antifuse C had actually been programmed. This, of

course, is not acceptable for any type of memory array. Thus, to use MIM antifuses in a cross-array, a third voltage must be applied to all bitlines and wordlines not being programmed. By keeping the other lines directly at (+W/2) some portion of the pull-down, pull-up effect can be eliminated. This drastically increases the complexity of the addressing circuitry, as three distinct voltages must be applied to a line during the array writing cycle. Evenso, in the case of programmed MIM antifuses, we still have direct conduction paths between wordlines and bitlines of different voltages. Thus, large amounts of current can flow though the inactive devices. Finally, even if the correct bits could be accurately programmed, conduction loops could be made that would compromise any read process. For example, if in Figure 6.4 elements B, C, and D were programmed, any attempted read on element A (by applying a voltage potential across wordline 1 and bitline 1) would show high current flows, inaccurately indicating that element A had been programmed. The end result is that MIM antifuses simply cannot be used effectively in a cross-array. These devices require that they be individually addressed, and thus their density is directly limited by the transistors driving them. Because of this, MIM antifuses offer no significant benefits over other solid-state memory elements, such as flash. To enable cross-array memories without the elementary read/write errors of MIM antifuses, diode-based antifuses must be used.

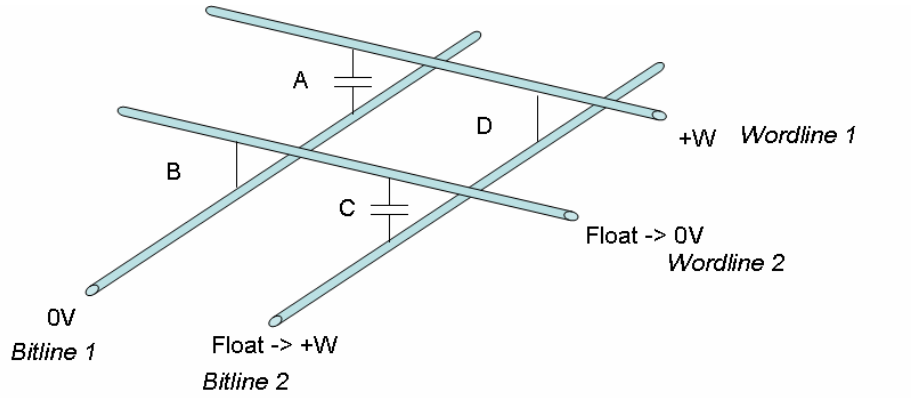

Figure 6.4: MIM memory cross-array

6.4 Diode-Driven Antifuses

To create dense memory arrays, the use of shared wordlines and bitlines is ideal, so that each memory element doesn't need individual access lines drawn to it. It has been established in the previous section that MIM antifuses do not function well in shared-line arrays for elementary reasons. However, if a diode is added in series with a MIM antifuse, many of the fundamental issues can be overcome. The basic operation of a diode-based antifuse is shown in Figure 6.5. In the 'read' event, a small voltage is applied across the device, and the state of the device is read, as in MIM antifuses. Similarly, when a large 'write' voltage (+8V in this case) is applied across the device in one direction, as in the second device in Figure 6.5, the diode is under forward bias, and the vast majority of the voltage drops across the capacitor (MIM). This enables the capacitor to undergo breakdown, programming the bit. The difference versus MIM devices is demonstrated in the third device of Figure 6.5. Here, the same 'write' voltage is applied to the other diode-antifuse terminal. Since the diode is now under reverse bias, little current passes, and a large voltage drop occurs across the diode. This event in turn reduces the voltage drop across the capacitor, thus preventing programming.

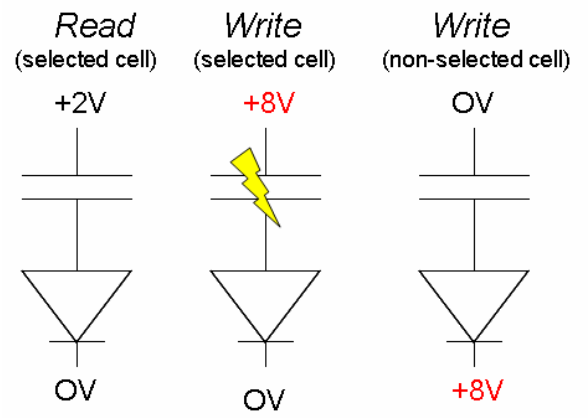

Figure 6.5: Diode in series enables dielectric breakdown for one polarity, and prevents breakdown in the other.

The reason this is vital to creating a stacked antifuse arrays with shared access lines is more easily understood when a mock system is investigated, as in Figure 6.6. In this single-level array, a target bit is selected to undergo a programming event. To achieve this, the write voltage (+W) is applied to Wordline 1, so that the target bit's diode is under forward bias, and the capacitor can undergo breakdown. However, to prevent the programming of the bit directly left of the target bit in Figure 6.6, +W must also be applied to Bitline 1. Likewise, Wordline 2 is kept at 0V so that no potential is placed across the device right of the target device. As a result of this procedure a potential of +W is formed across antifuse "A". If antifuse "A" were a simple MIM device, accidental programming would occur. However, by using the principles of Figure 6.5, bit "A" does not become accidentally programmed.

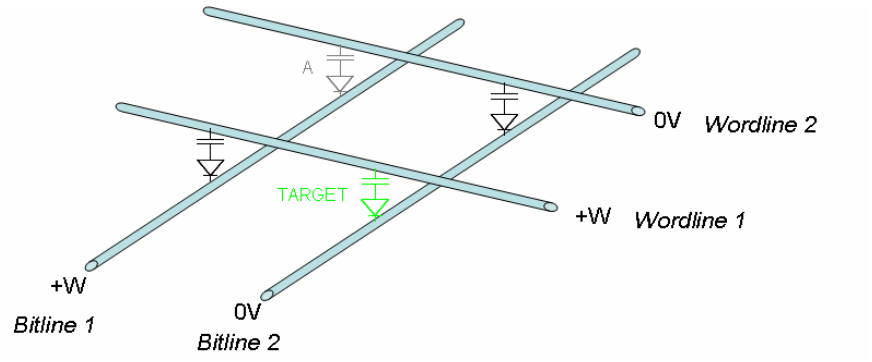

Figure 6.6: 2 x 2 single level antifuse array

The diode placed in series with the capacitor also aids in the creation of stacked antifuse arrays. If the system from Figure 6.6 has another interconnected antifuse layer directly on top, as in Figure 6.7, the diodes continue to prevent accidental programming. To prevent the accidental programming of the antifuse directly above the target bit, bitline 4 is held at +W. Similarly, bitline 3 is also held at +W to prevent the programming of a second-level bit. Once again, the voltage drop across the reverse-bias diode prevents the accidental programming of bits B1 and B2.

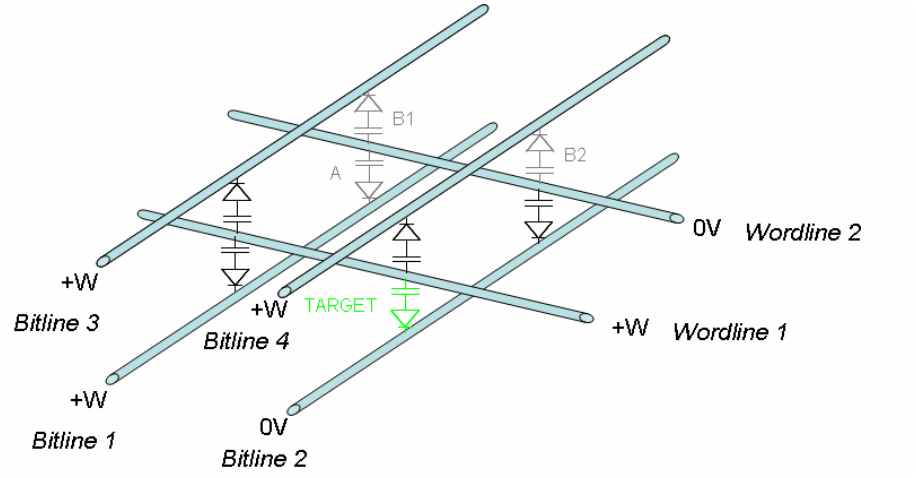

Figure 6.7: Two-level diode-based antifuse array

This process continues as the stack reaches three levels. In Figure 6.8, all of the third-level devices utilize the diode to prevent programming. However, wordlines 3 and 4 can be held at 0V, meaning that a similar programming process can occur on the fourth antifuse level at the same time as a programming event on the first antifuse level. This programming parallelism enables rapid multi-level programming, aiding in overall memory write speed. At this point it is apparent that the diode is critical to creating functional vertically stacked antifuse arrays.

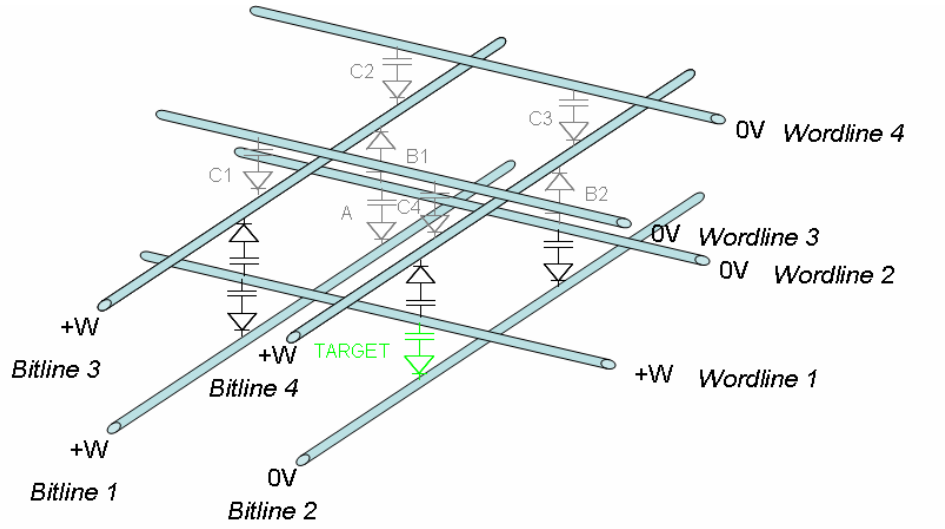

Figure 6.8: Three-level diode-based antifuse array.

Stacked diode-antifuse memories have been under investigation by various groups for some time. A schematic of these devices is shown in Figure 6.9, with an SEM of a stacked antifuse array on the right. In these devices, made primarily by Sandisk Corp., the SiO2 dielectric layer is generally between 2-3nm, so that breakdown can occur below 5V [58]. In this work, tungsten interconnects were used, with TiN diffusion-barrier layers [57], to create memory cross-arrays. Also, amorphous-silicon p-i-n diodes are created. An intrinsic layer is incorporated so that the voltage drop across the diode is distributed over a longer physical distance when the device is under reverse bias. This prevents electrical breakdown effects such

as avalanching and band-to-band tunneling to increase leakage through the reverse-biased diode. A similar effect is achieved in antifuses utilizing n^- Si – $CoSi_2$ schottky diodes [59]. Standard processing techniques include high-density plasma enhanced chemical vapor deposition (HDPCVD), low-pressure chemical vapor deposition (LPCVD), chemical mechanical polishing (CMP), and lithography [57][58].

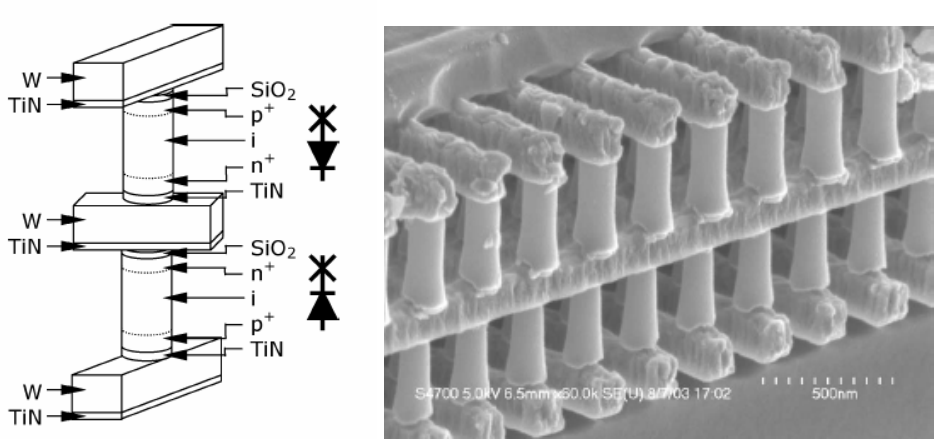

Figure 6.9: Silicon-based antifuse design (left) and SEM image of an antifuse memory array (right) [57].

These devices have been used to create commercially viable stacked antifuse arrays at densities higher than other memory technologies [60][61]. As seen in Figure 6.10, antifuses demonstrate significant area advantages once all of the circuit area is taken into account, despite using aged lithography equipment with large minimum feature sizes. Presently, this technology is limited to 8 antifuse layers in the creation of 512MB memory arrays [60][61]. This limitation is due to the controlling circuitry being resigned to the original silicon substrate, built using standard CMOS processing. These row and column decoders, sense amplifiers, and bias circuits are built directly below the antifuse array, and their space requirements only enable them to support 8 levels of antifuse devices. In theory, if the addressing circuitry could be constructed in-plane with each antifuse level, the stacking could be endless. Unfortunately, inorganics are

not well suited to this design methodology due to thermal budget requirements. This issue, combined with the need for vacuum-intensive processing techniques, will be eliminated in this work to enable antifuse memories on a reel-to-reel system with unlimited stackability.

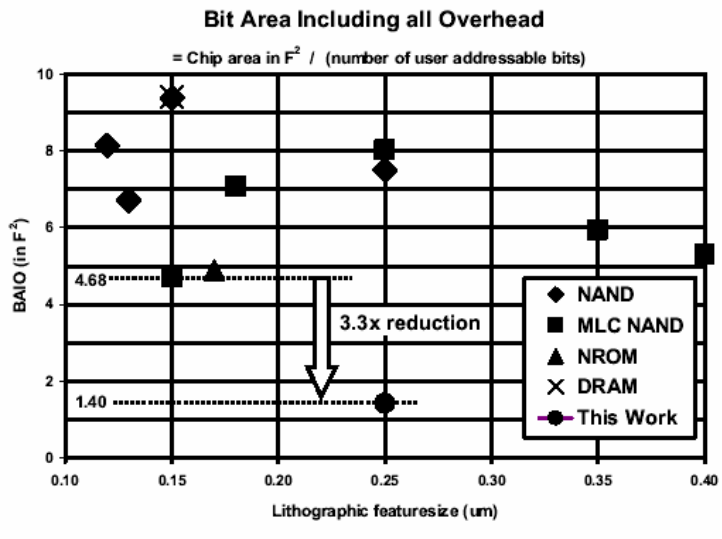

Figure 6.10: Stacked antifuse density versus other leading memory technologies [61].

6.5 Performance Challenges

6.5.1 Disturb Phenomenon

In an antifuse cross-array, programmed bits have the capability to induce programming errors with certain word or bit lines if reverse-bias diode leakage currents are high. Generally referred to as a 'Disturb Error', this effect can prevent the proper writing of a given bit, as described below and in Figure 6.11. In this situation, our goal is to program antifuse A, located at the crossing of bitline 1 and wordline 1. A write voltage (+W) is applied to wordline 1, and bitline 1 is grounded to create a potential of +W across the device, most of which is dropped across the uncorrupted capacitor. However, the presence of previously written antifuse bits can cause the latching of neighboring lines. If some bit along wordline 1 has been previously

programmed, such as antifuse B (represented here by a diode, since the capacitor has been shorted), we can cause bitline 2 to be raised to near the write voltage applied to wordline 1. This can happen because lines not directly related to the write process are generally floating. This in itself is not a particularly worrisome proposition, because it can't result in accidental write events along bitline 2 due to the reverse biased diodes protecting the capacitors. However, a problem can occur if antifuse C is already programmed, and the reverse-biased diode is leaky. If significant current it allowed to flow, the potential of wordline 2 begins to be pulled up toward the write voltage applied to wordline 1, since wordline 2 is generally allowed to float. Finally, if antifuse D is already programmed, the forward biased diode will allow bitline 1 to be pulled toward the write voltage, as has occurred for bitline 1 and wordline 2. Although bitline 1 is grounded through a series of control transistors, the leakage path described here can cause bitline 1 to have a more intermediate voltage between ground and the write voltage. The net effect of this is that the potential across antifuse A, the device we originally wanted to program, is no longer the entire write voltage (+W). Thus, antifuse A is less likely to incur a programming event, and yield becomes compromised.

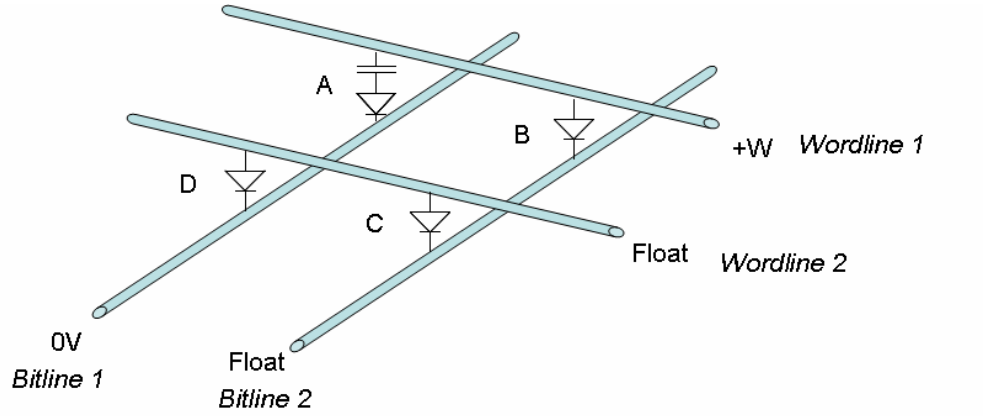

Figure 6.11: Antifuse disturb event

Although it seems improbable that a single reverse-biased diode could leak enough current to pull up a bitline biased to ground, this event works in parallel in large antifuse arrays. If hundreds of devices are programmed in an array we potentially could have thousands of reverse-biased diodes pulling up on bitline 1. Thus, the reverse leakage of the diodes used is of critical importance in the creation of large arrays. To give an idea of just how many leakage paths exist in a common array, let us consider a system with *x* wordlines and *y* bitlines. We'll say that the bit to be programmed resides at the crossing of bitline 1 and wordline 1, as in the disturb sequence described above. For a leakage path to occur, we must have three programmed bits working to create a path from wordline 1 to bitline 1. First, let us assume that the remainder of the array points have already been addressed, with exactly 50% programmed such that the capacitor has fused (which is generally called the "0" state). We can then say that half of the remaining devices along wordline 1 have been programmed $(x-1)/2$. Then, for each one of these programmed devices along wordline 1, there are $(y-1)/2$ programmed devices, representing node C in the disturb event of Figure 1. Finally for each of these potentially leaky nodes, the respective device in bitline 1 must be programmed to complete the leakage current path. For each of the relevant nodes, there exists a 50% probability of being programmed, and thus capable of completing the leakage circuit. Thus, for an antifuse array of x wordlines and y bitlines, the number of leakage paths (and thus, the number of reverse-biased diodes contributing to the latch-up event) is:

$$(x-1)/2 \times (y-1)/2 \times 1/2$$

This results in a surprisingly large number of leakage paths. For example, for a 1Mbit antifuse memory array with all bits having a 50% chance of being in the "0" state (programmed), we

have approximately 130,816 distinct leakage paths. This means that the leakage currents from 130,816 reverse-biased diodes are combined to pull down the voltage level of bitline 1. As seen in Figure 6.12, the total number of leakage paths increases linearly with the size of the memory array. The result is that the percentage of leakage paths saturates at 12.5%, meaning that for every 100 bits in the memory array, we have approximately 12.5 distinct leakage paths. This increase in leakage paths is unavoidable, and presents challenges to designers of the addressing circuitry. As arrays increase in size, the antifuse array requires that each bitline (and wordline) have larger addressing transistors, enabling larger current throughputs to combat leakage currents. For device design, it becomes of paramount importance that the diodes have extremely low reverse-bias leakage currents, as this ultimately limits the size of our antifuse array.

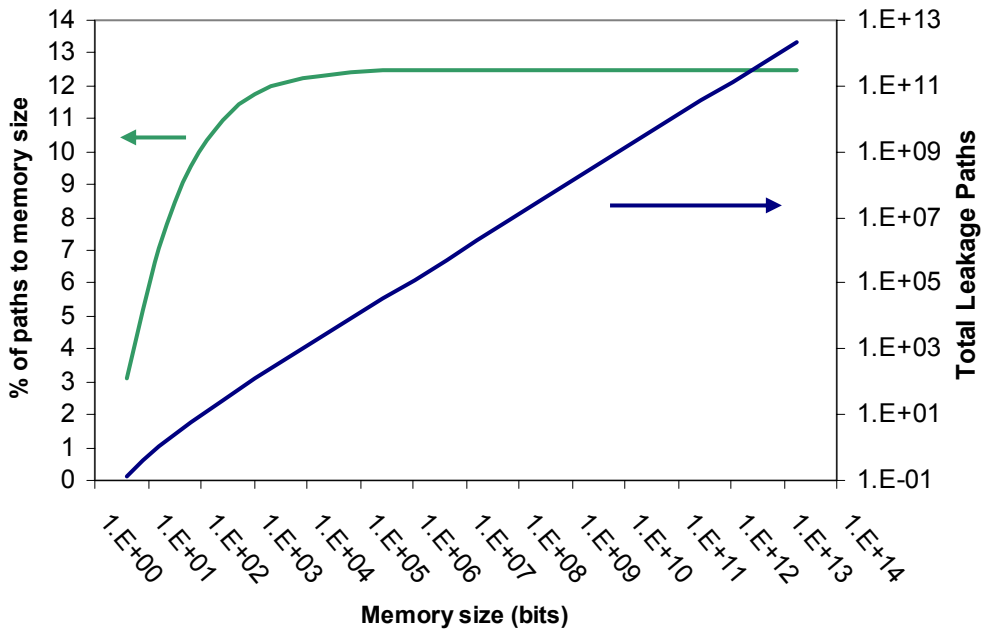

Figure 6.12: Leakage pathway scaling with memory size

While we can identify the diodes responsible for the leakage that is critical to our current programming event, other programming events will find completely different reverse-biased diodes critical, so the 'important' devices to prevent disturb errors cannot be singled out in an array. Thus, we cannot design certain diodes differently to help avoid the disturb error. As a secondary effect, the wordline held at a write voltage can be pulled down by this parasitic leakage path, further inhibiting the write process. However, this effect is much smaller, as current must pass through two reverse-biased diodes to effectively latch. As a result, wordline addressing transistors need not be as large as the bitline addressing transistors.

6.5.2 Testing Methods

To accurately test an antifuse, a series of voltage sweeps must be performed. In the test setup, two probes are used, with one of the probes including a resistor in series. This resistor is used to limit the capacitive dump from the lines of the probe station during programming. If the resistor is not used, the charge dump upon programming can cause larger filaments to form, decreasing the resistance of the broken-down insulative layer. This charge dump can also cause the dielectric to breakdown at slightly lower voltages. Finally, the massive instantaneous current flow can also induce the breakdown of the diode, which would not occur in an actual memory array programming event. The series resistor effectively removes the inaccurate effects of the testing equipment and allows a more precise measurement of the antifuse itself.

A four-stage test setup is employed to characterize each antifuse device. First, a "read" sweep of an unprogrammed device is executed at low voltages. The voltage is swept upward from 0V to the read voltage (+R), and then swept back down to zero to identify any hysteresis due to charging. Next, a "programming" sweep is executed. The device is swept from 0V to the write voltage (+W), and along the way, the dielectric is expected to break down, causing a

sudden increase in current. As the device is swept back down from (+W) to 0V, the device traces diode behavior, now that the dielectric is a short. A second "read" sweep is then performed, which illustrates the current characteristics of the programmed device. As before, the voltage is swept both forward and back, to demonstrate any remaining hysteresis due to the charging of trap states. Finally, a full diode sweep is performed to gather information about the leakage current through the reverse-biased diode.

6.5.3 Performance Metrics

Like all solid-state devices, a set of performance metrics exist to determine the overall quality of antifuses. Compared to devices that operate at a single voltage, antifuse characterization is more involved since the devices must be analyzed in the off-state, during programming, and during read operations. Also, in a cross-array configuration, the interactions between devices must be taken into consideration, as was demonstrated in Section 6.5.1. These metrics are used to analyze power considerations, in both programming and read operations, as well as device reliability and to analyze the differentiation between programmed and unprogrammed bits. Figure 6.13 illustrates several of these important metrics, with more in-depth descriptions below.

The simplest, and perhaps most telling performance metric is the margin of an antifuse. The margin is the ratio of the current that passes through a programmed device versus the current that passes through an unprogrammed device at the read voltage. The margin indicates the ease at which a programmed device can be differentiated from an unprogrammed device. The larger the margin for a given device, the simpler the memory access circuitry can be, which reduces complexity and area concerns. High margins are generally easy to achieve in antifuses, due to their simple nature. In an unprogrammed device, the current is limited by the leakage

current through the dielectric at the read voltage. Conversely, in a programmed device the current is limited by the forward-biased characteristics of the diode. As a result, the current in a programmed device generally increases much more quickly with a voltage increase than an unprogrammed device. Consequently, higher read voltages generally result in higher margins, since the forward-biased diode is allowed to turn-on more fully. However, increasing the read voltage to achieve higher margins also results in increased power draw. This is a fundamental trade-off in device design, and is a decision based upon the power and performance needs of a given application.

The programming voltage is also an important metric with which to describe antifuse operation. The programming voltage, which is the voltage at which the breakdown of the dielectric is ensured, depends largely on the dielectric thickness and robustness. A low programming voltage directly limits the size of the read voltage, which in turn can limit margin, as described earlier. On the other hand, a large programming voltage results in larger power levels to write an antifuse bit. This can directly affect the current driving needs for the addressing circuitry, resulting in larger transistors. Even worse, if the programming voltage is higher than 45V, it is a common occurrence for the filament formation event to short the organic diode.

The distribution of the programming voltages across the array is also of critical importance. Ideally, the antifuses would all break down at the same voltage. Unfortunately, inhomogeneities in the dielectric film, along with thickness variation cause the array to produce a range of breakdown voltages. In this situation, the programming voltage is designed to be at the bias necessary to induce filament formation for the vast majority of the devices, ensuring high yield. Unfortunately, a wide distribution causes the programming power levels to be high,

while directly limiting the read voltage. A wide distribution forces read voltages, and thus margins, to decrease in order to prevent the accidental programming of bits.

Besides reducing margins, the current though an unprogrammed bit at the read voltage results in power consumption. In the stacked antifuse array structure, multiple bits can be read simultaneously, and unprogrammed bits with high leakage increase the power draw of the system, and could eventually lead to device heating. Self-heating could alter the properties of the dielectric, ultimately changing the breakdown voltage of the device. Thus, it is important to limit the leakage through unprogrammed bits through the optimization of the dielectric.

Finally, because of the concerns of the disturb event of Section 6.5.1, the current of a programmed bit at the negative write voltage (-W) is significant. This metric tells the amount of current that flows through the reverse-biased organic diode, and indicates the degree to which the disturb event will occur. As described earlier, by limiting this current, smaller addressing transistors can be used, and larger arrays can be made in-plane.

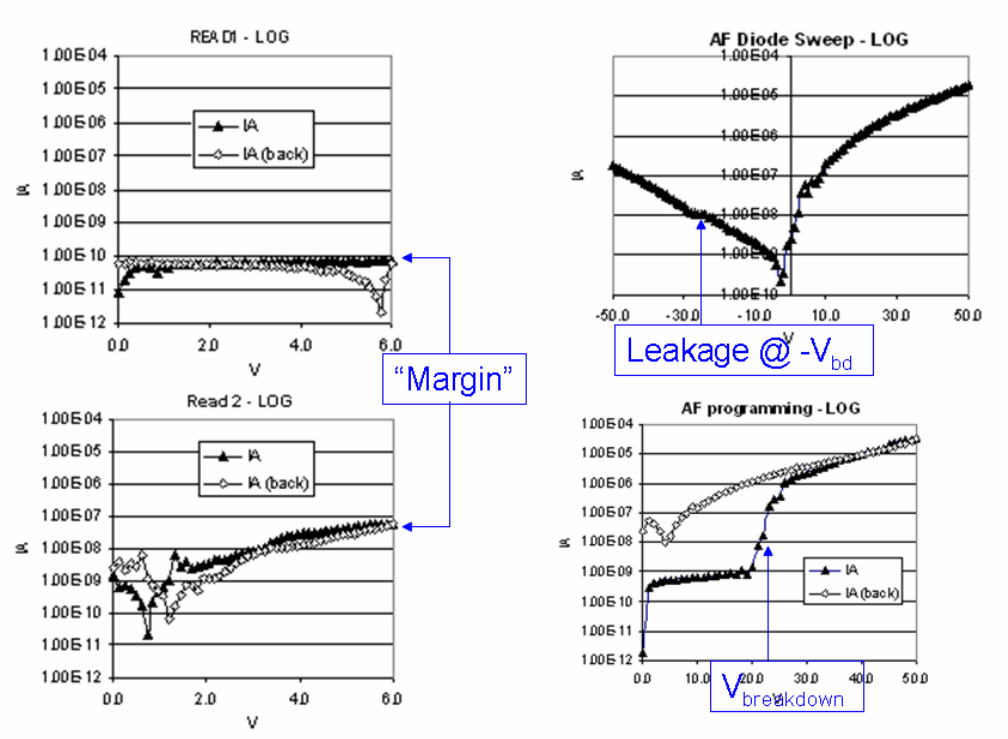

Figure 6.13: Electrical sweeps of an antifuse device, highlighting the performance metrics. Left: Read sweeps of an unprogrammed (Read 1) and programmed device (Read 2). Top Right: Diode sweep of a programmed bit (AF diode sweep). Bottom Right: Programming voltage sweep (AF Programming). Filled triangles indicate the sweep was from left to right, while unfilled represent sweeping from right to left.

6.6 Conclusions

This broad understanding of antifuse technology assists in the creation and evaluation of new devices. By exploring the history, error mechanisms, and metrics for antifuse devices, the foundation for transferring this technology into the organic electronics space has been facilitated. In the next chapter, the groundwork for organic antifuses is laid, and the first organic antifuses are demonstrated. Then in following chapters, the organic antifuses will be optimized and tailored to excel in the performance metrics outlined here to create ideal devices for low-cost printed memories.

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Chapter 7: ORGANIC ANTIFUSES

With the inorganic antifuse background established in the previous chapter, the development of an organic antifuse is investigated. This chapter begins by inspecting the individual elements of organic antifuses – the organic dielectric capacitors and the organic schottky diodes. The operational theory and experimental characteristics of each are explored. These devices are optimized and tested in-house, and provide a fundamental foundation for all future antifuse work. As a result, the first-ever operational antifuse based upon high-performance organic diodes is demonstrated. To conclude this chapter, a preview of the progression to plastic-substrate memory arrays is given.

7.1 Organic Capacitors

The basis for an antifuse memory lies on the reliability and consistency of the capacitive element. While the MIM antifuses explored in the previous chapter generally utilize silicon dioxide and nitride insulators deposited by chemical vapor deposition (CVD) or thermally grown silicon dioxide at 600-800C, these routes are incompatible with the idea of low-cost electronics and reel-to-reel processing. Besides the need for vacuum-based systems, which add significantly to cost, both processes run at temperatures above the thermal limits of even the highest-rated plastic films. Instead, a low-temperature insulator must be investigated if antifuses are to be produced in a low-cost process.

While there have been many demonstrations of low-temperature insulators to date, including poly(ethylene oxide) (PEO)[69], various polyimides, and others, only one group has shown the use of a low-temperature dielectric that has been integrated into an antifuse[70]. As mentioned

in the previous chapter, Hu *et al* [70] use a spin-cast sol-gel silica film to create the capacitive element of their antifuse structure. This film was spin-cast and partially cured at 100ºC, which is compatible with the use of plastic substrates. With the reliability and predictability of the capacitive structure being of paramount importance, this material provided an established starting point in the thrust toward making an organic antifuse.

7.1.1 Sol-gel Silica Capacitors

To test the electrical behavior of the insulator, a simple capacitive structure was made. 1500Å of aluminum was blanket evaporated onto dummy mechanical-grade silicon wafers. After acquiring the commercial "spin-on-glass" used by Hu *et al* [70] from Emulsitone Co. (Silicafilm™), we used the available documentation to develop appropriate spin conditions to replicate the film thicknesses used (30 to 200nm). As in [70], the films were cured for 40 minutes at 100ºC at standard atmospheric pressure. Before the deposition of the top contact, we verified the thickness of the silica film. The films were spun at 4000 RPM for 30 seconds, and those of pure Silicafilm™ resulted in films ~200nm thick, while those of a 1:2 volume dilution of Silicafilm™ and ethanol produced films ~70nm thick. Finally, 1500Å of aluminum was evaporated through a shadow-mask to create the second capacitive plate with an area of 100μm by 200μm.

The electrical characteristics of a typical spin-on-glass (SOG) capacitor are shown in Figure 7.1. In devices where pure Silicafilm is spincast, breakdown voltages between 5V and 15V are most common, with variation likely due to thickness inconsistencies occurring during the spinning process. As breakdown occurs, we see the current rapidly increase by many orders of magnitude, as it becomes ultimately limited by the power compliance values of the test equipment. With this device we see relatively low current before breakdown, which appears

independent of applied voltage. In can be concluded that Fowler-Nordheim tunneling is low these devices, largely due to the 200nm thick insulator.

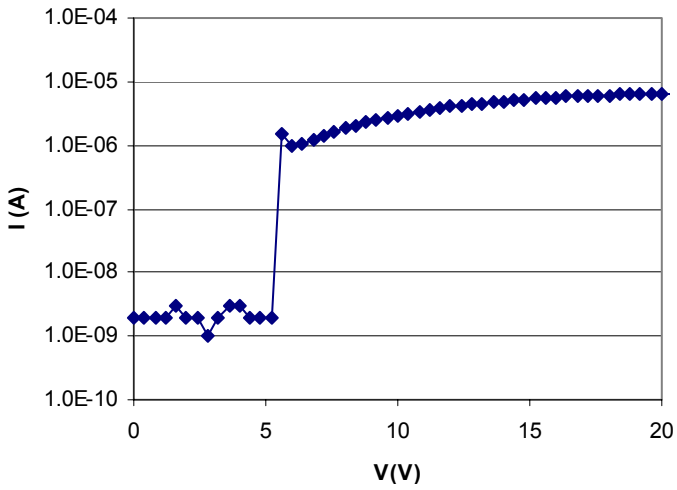

Figure 7.1: Destructive breakdown of a pure Silicafilm™ capacitor cured at 100ºC

As we scale the insulator thickness, however, the electrical characteristics change as seen in Figure 7.2. First, as we scale, the breakdown voltage decreases, as expected, since the breakdown event is controlled by the electric field across the dielectric. The breakdown for these devices generally ranges from 2V to 4V. The leakage current prior to breakdown also becomes significant in these devices. The somewhat linear increase in leakage current (on the log plot) with voltage leads to the conclusion that Fowler-Nordheim tunneling plays a significant role. For an antifuse design, low leakage is ideal, as it is this current which is compared to the diode-limited on-current of a programmed device. As will be shown in the next section, the leakages in this 1:2 Silicafilm™ layer are close to the on-currents of good organic diodes. Thus, films with such high leakages strain the operational specifications of our

proposed memory. To better control the problem, thicker films are necessary. Unfortunately, thicker films also require larger programming voltages, which are inconvenient.

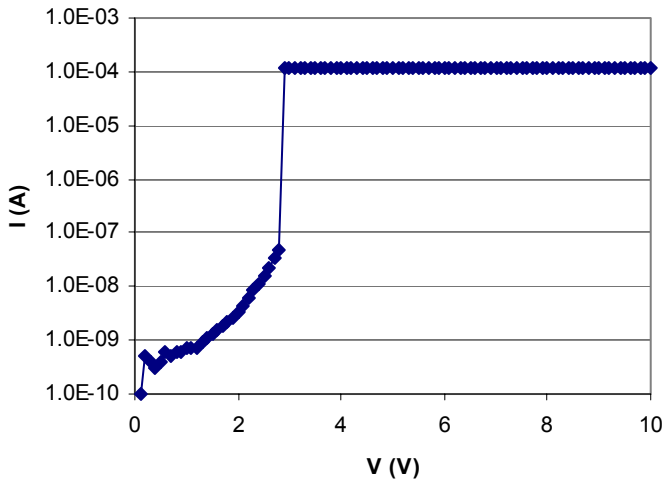

Figure 7.2: Silicafilm™ mixed in a 1:2 ratio with ethanol

These Silicafilm™ dielectrics also show stability problems. The capacitive element can undergo a "healing" effect in which the dielectric returns from a broken state to a low-leakage state. In Figure 7.3 the element undergoes breakdown at 8V, but as the electrical sweep continues to higher voltages (with current limited at the compliance value of 1×10^{-5} A), a recovery point can be seen. At 23V, the capacitor returns to a low conductivity state, and continues to vary as the voltage sweep continues. As the voltage sweep takes less than 4 seconds, the lack of a stable current level in the blown capacitor is of serious concern. As the programmed element in an antifuse, the blown capacitor needs to maintain a stable state for the operational life of the device, which should range from months to years. Unfortunately, this rapid healing effect limits the usefulness of this material. The reference solves this and other problems through the use of an HMDS soak of the film prior to anneal. While this

action may have solved the problems seen here, adhesion issues, which will be discussed in section 7.3, ultimately limited the usefulness of this material.

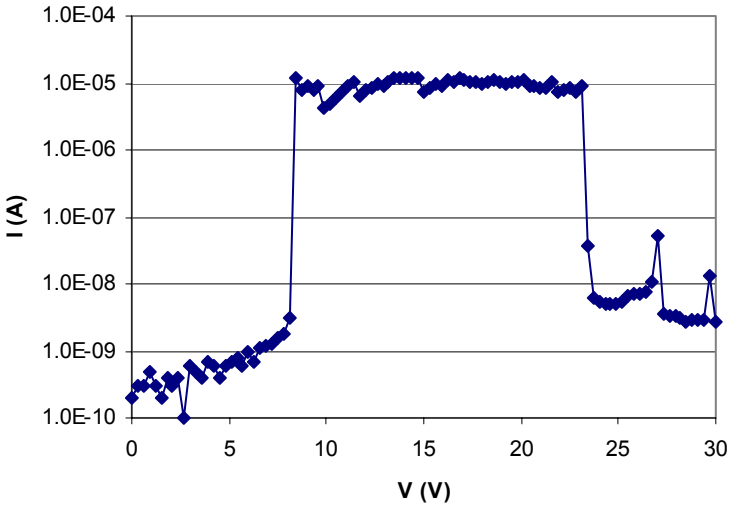

Figure 7.3: 1:1 Silicafilm™ capacitor healing during electrical characterization

7.1.2 PVA Capacitors

Poly(vinyl-alcohol) (PVA) was another material that was investigated as a dielectric for the antifuse structure. It is a natural choice as it has proven compatible with pentacene thin films, as was demonstrated in Chapter 5. PVA thickness control and spin conditions were also established in the OTFT isolation work, giving this material a head start in the insulator verification process. Unfortunately, this material was never previously characterized as a dielectric, but due to the simple nature of making capacitors, this material was analyzed.

A blanket aluminum layer of 2500Å was deposited via evaporation onto a dummy wafer to serve as the bottom electrode of the capacitor. 89% hydrolyzed PVA was mixed in solution at 4% by wt. with deinonized water, as in Chapter 4. The material was then spun onto the aluminum surface at 4000RPM for 30 seconds. The film was then baked at 125ºC for 25

minutes to aid in solvent evaporation. Profilometry was performed, and thicknesses ranged from 120nm to 157nm among 7 data points. Color variation was seen across the wafer, originating from the center, but such thickness variations were insufficient to produce thickness trends as detectable by profilometry. Aluminum contacts were then evaporated through a grid shaddowmask to form the top electrode.

Upon testing the capacitors with a whisker tip on the top electrode (so as not to put excess pressure on the dielectric), fairly uniform breakdown behavior was seen. For the set of devices tested, physical breakdown occurred between 44V and 61.6V. Devices also seemed to hold their programming for more than 10 minutes, although only rudimentary testing was performed. Although the target voltage for programming is 15V, the dielectric spin and dilution conditions can be tailored to reach this point. However, a far larger problem presented itself during testing. For these PVA films, which are already thicker than the final desired film (thinned breakdown voltage tailoring), current leakage is a serious problem. As shown in Figure 7.4, current reaches 5×10^{-7}A at 40V prior to breakdown. As will be seen in section 7.2, this high leakage is comparable in magnitude to that of a forward biased organic diode. As the quality of an antifuse is largely measured by the difference of current between a programmed and unprogrammed device, having a leaky dielectric is extremely undesirable. The device illustrated in Figure 7.1 is one of the best-case devices tested, and many PVA capacitors had leakages greater than 1μA prior to breaking down. This leakage is a likely reason why PVA has not been utilized as a dielectric in literature. Finally, when the PVA film is spin-cast onto an evaporated pentacene layer, the resulting surface roughness is visibly apparent, which raises concerns about the PVA uniformity and the resulting variation in

breakdown voltage. As a result of these two problems, PVA was abandoned as a dielectric for use in an organic antifuse.

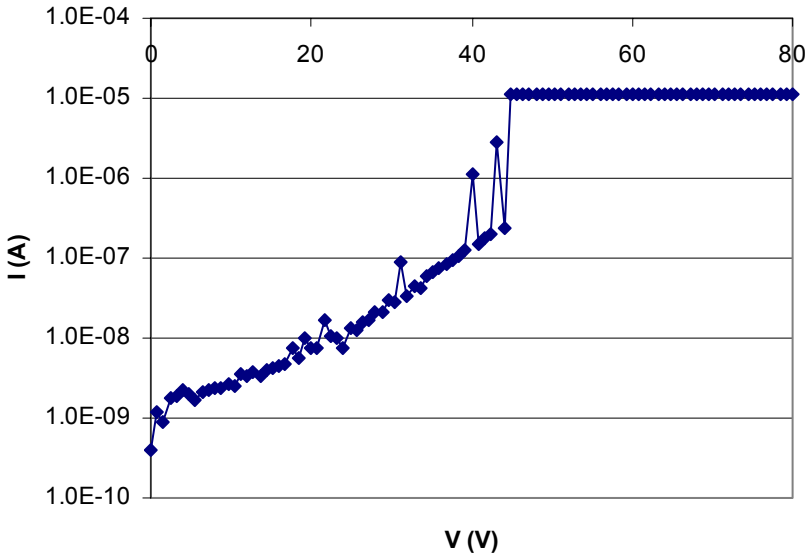

Figure 7.4: PVA capacitor showing high leakage prior to breakdown

7.1.3 PVP Capacitors

The third material directly investigated as a dielectric for the organic antifuse was poly-4-vinylphenol (PVP). As used in Chapter 5 as a gate dielectric deposited on the active organic layer, it presents a prime candidate for the integrated diode/capacitor antifuse. Unlike PVA, this material is widely used in literature as a dielectric. In the work originally performed by Infineon Technologies [27], PVP films were spun on highly-doped silicon wafers, which served as the gate electrode. As minimizing gate leakage was paramount in their search for a polymer dielectric, a cross-linked PVP process was also developed to further reduce leakage through the dielectric. In this process, PVP was combined with poly(melamine-co-formaldehyde) to form a robust dielectric with plastic-compatible curing temperatures of

200ºC. As seen in Figure 7.5, the cross-linked PVP showed reduced leakage to its PVP copolymer counterpart.

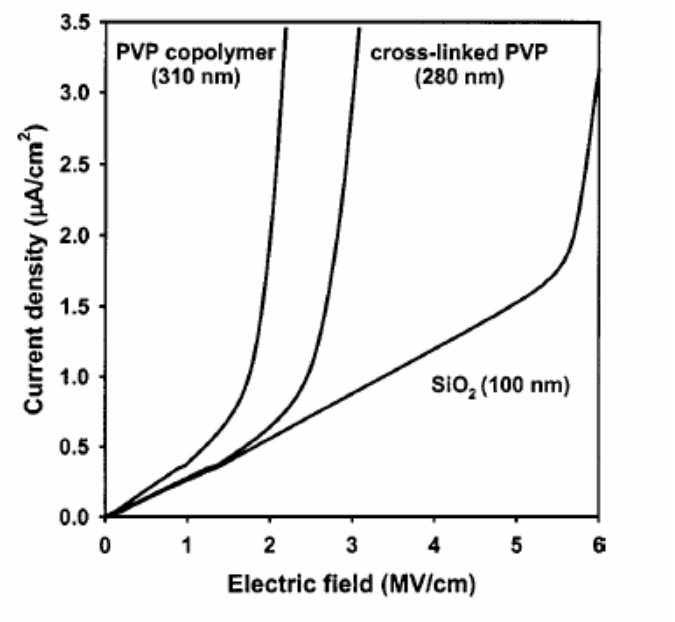

Figure 7.5: Leakage current through the various dielectrics investigated by Kluck et al. [27]

However, while crosslinked PVP was proven to reduce leakage, it also resulted in an increase in breakdown voltage. While these characteristics are ideal for OTFT gate dielectrics, this work depends on the dielectric breaking down at a relatively low field. Initial studies verified the high breakdown of the cross-linked PVP film.

A cross-linked PVP solution was created by adding 1g of PVP to 15ml of ethanol, and adding 0.2mL of poly(melamine-co-formaldehyde) (cross-linking agent). The solution was spin-cast onto a gold-coated dummy wafer at an initial pour rate of 500RPM. The spinner was ramped to 4000RPM and remained at this speed for 30 seconds. The film was cured at 100ºC for one minute and 200ºC for 5 minutes to promote cross-linking within the film. This film

concentration and anneal process is identical to the processes performed for works in the Organic Electronics Printer Group, lead by Steve Molesa[72]. Finally, 1600Å of gold was evaporated through a shadow-mask to form the top plate of the capacitor. Initially the cross-linked PVP thickness target was to match the thickness of [27], which was 280nm. Profilometry confirmed that the thickness of the as-prepared film was between 306nm and 313nm. As can be seen in Figure 7.6, current increases linearly when the y-axis is plotted in logarithmic form, which is indicative of Fowler-Nordheim tunneling current. The leakage current is as low as predicted in Figure 7.5. However, it is also readily apparent that the cross-linked PVP film in Figure 7.6 does not break down even after stressing to 100V. In fact, during testing, stressing as high as 200V (6.45 MV/cm) did not induce breakdown in the film.

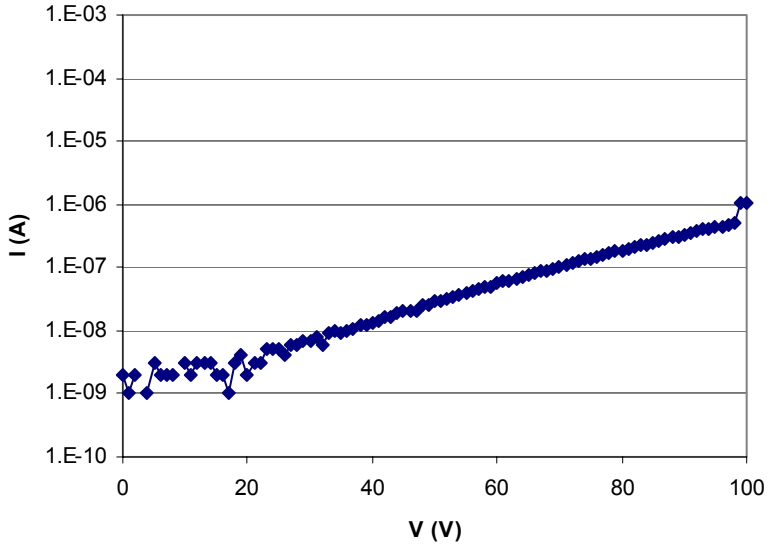

Figure 7.6: Current characteristics of a cross-linked PVP capacitor.

A PVP solution without the cross-linking agent was also investigated as a dielectric for the antifuse structure. With previous success utilizing this material with the Top-Gate

architecture, compatibility with pentacene has been confirmed. As in Chapter 5.2, 5% by wt. PVP was added to 2-Propanol. The solution was mixed via sonication, and was filtered through a 0.25μm filter prior to deposition. As with the cross-linked PVP solution, the film was poured onto a dummy gold-coated wafer at 100RPM and ramped to 4000RPM. The film was cured at 100ºC for 5 minutes. No 200ºC anneal was performed since no cross-linking agent exists, and to avoid anneal temperatures that would limit substrate selection in future processes. As before, 1600Å of gold was evaporated to form the top contact. Profilometry indicated a film thickness ranging from 251nm to 282nm. As seen in Figure 7.7, leakage through the capacitor is slightly larger than the leakage through the cross-linked devices of Figure 7.6, as predicted by Figure 7.5. However, a marked difference is that the PVP film undergoes destructive permanent breakdown at 78 Volts. At this point, a filament is established, and current becomes solely limited by the set current compliance of the HP4156 parameter analyzer. This sudden and complete breakdown from a low-leakage state is ideal for an antifuse dielectric. Although not tested extensively, these capacitors had breakdowns ranging from 65V to 85V, with a large count toward the upper one-third of that range.

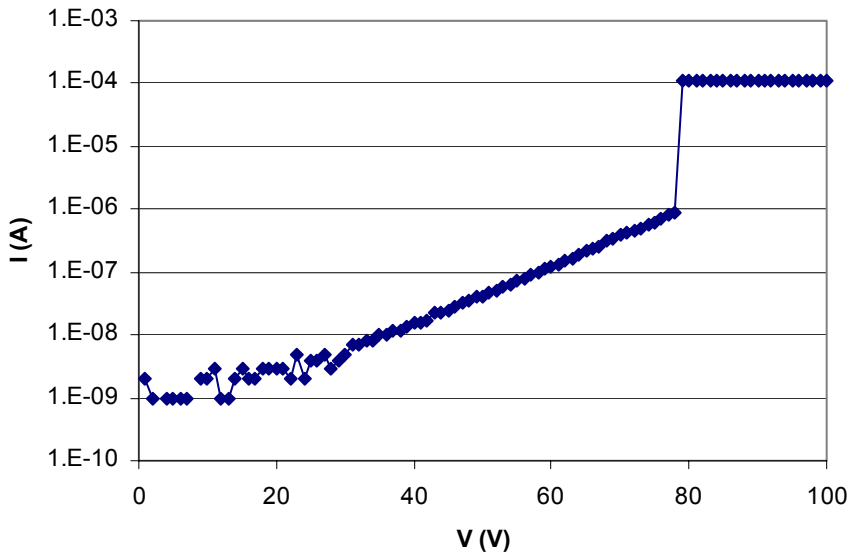

Figure 7.7: Current characteristics for a PVP capacitor.

The next step in making PVP layers for antifuses was to scale the film thickness so that breakdown occurred at more manageable voltages, preferably between 10V and 25V. Solution concentration, spin conditions, annealing temperature, and annealing duration could all have impacts on film thickness. For simplicity, and to avoid secondary effects that include surface energy effects of primary spin layers (which add a nonlinear component to the thickness variation with spin speed), the spin conditions were held constant at a pour speed of 500RPM with a ramp to 4000RPM (30 seconds). Also, to limit the scope of the investigation, anneal time was also held constant at 5 minutes. Cure temperatures for these PVP dielectrics were either 100ºC or 200ºC, and multiple spins of thin layers were used to control thickness. These capacitors used PVP mixed 1% by wt. with 2-Propanol. As before, both upper and lower contacts consisted of evaporated gold.

Figure 7.8 shows the cumulative distributions of breakdown voltages. At first glance, it is apparent that when multiple layers are spun, the breakdown voltage increases due to a thicker

film. This is consistent for both the case where the films are cured at 100ºC and 200ºC, and it is expected. The distribution of breakdown voltages for each sample is narrow, attesting to the uniformity of the spin, which was verified on previous samples earlier. This constricted distribution is promising for the integration of PVP films of this concentration into antifuse device arrays. Figure 7.8 also illustrates that higher anneal temperatures have a significant impact on the breakdown voltage, as annealing hardens the film and causes the film to require higher electric fields to induce filament formation. This effect impacts the films so much that it has resulted in a single layer of PVP cured at 200ºC to have a higher average breakdown voltage than two layers of PVP cured at 100ºC sequentially. As the goal was to optimize the PVP film to break down in the 10V to 25V range, both the single layer of PVP cured at 200ºC and the two-layer PVP film cured at 100ºC appear to reside in the optimal range. From this initial study, the two-layer film appears to have less variance, as 70% of the tested devices have breakdown voltages within a few volts. A tighter distribution is likely due to the averaging effect of spinning multiple layers of the material and having an overall higher thickness. Thus, any surface roughness from the metal electrodes becomes minimal in comparison with the film thickness, reducing the role of local minima due to spikes in electrode topography. Also, by spinning multiple layers of any film, pinhole defects can be drastically reduced, helping yield. In this dielectric tuning process, it is also important to track leakage currents though the dielectric prior to breakdown, as in Figure 7.9. The devices illustrated in Figure 7.9 are typical devices pulled from each of the four sample conditions.

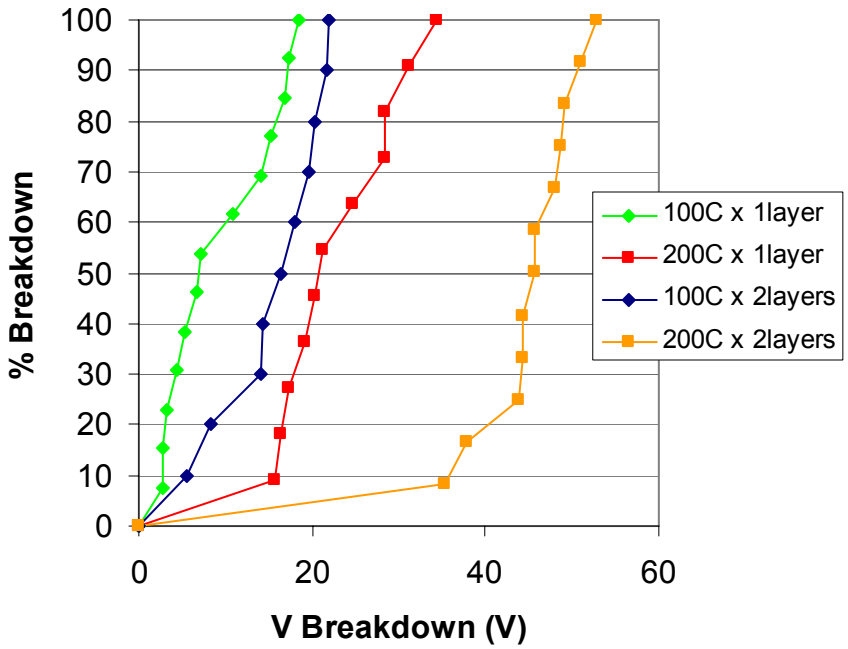

Figure 7.8: PVP capacitors created with different anneal temperatures and single or double layers of PVP. Exact thicknesses were not determined via profilometry, as spin conditions would vary when the technology is transferred to plastic substrates. Rather than measured thickness, electrical behavior was used to adjust spin conditions in future work.

In theory, thicker and hardened films should reduce leakage through a dielectric. However, Figure 7.9 clearly shows that device leakage prior to breakdown has little to do with the number of layers or the anneal conditions. In fact, it can be seen that a single layer of PVP cured at 200ºC can prohibit more leakage than a device with two layers of PVP cured at 200ºC. It can also be seen that the films annealed at 100ºC have leakages that are very similar, with noise being the largest differentiator. While these results are contrary to intuition, they clearly illustrate that curing at high temperature increases breakdown voltage, but has little effect on leakage currents. It also demonstrates that spinning multiple layers does not necessarily decrease leakage current. It is possible, though far from the only explanation, that discrete electrical traps exist at the surface between two PVP layers. These traps could enable Poole-

Frenkel leakage currents through the dielectric, increasing leakage significantly. It would be expected, however, for a given concentration, that increasing the spin speed would reduce the film thickness, and cause an increase in leakage and a decrease in breakdown voltage. Thus, if the two-layer 200ºC PVP film thickness was scaled so that breakdown occurred in the 10V-20V range, higher leakage currents would be expected.

As an added detractor, heating plastic substrates at 200ºC can cause surface warpage, which is not ideal. In fact, the lower the process temperature is kept for the final antifuse product, the better, as warpage can result in a host of problems in both the organic semiconductor and the polymer insulator. As a result, when designing the PVP dielectric for the antifuse devices, it became readily apparent that curing at 200ºC provided no electrical or physical advantages to curing at 100ºC.

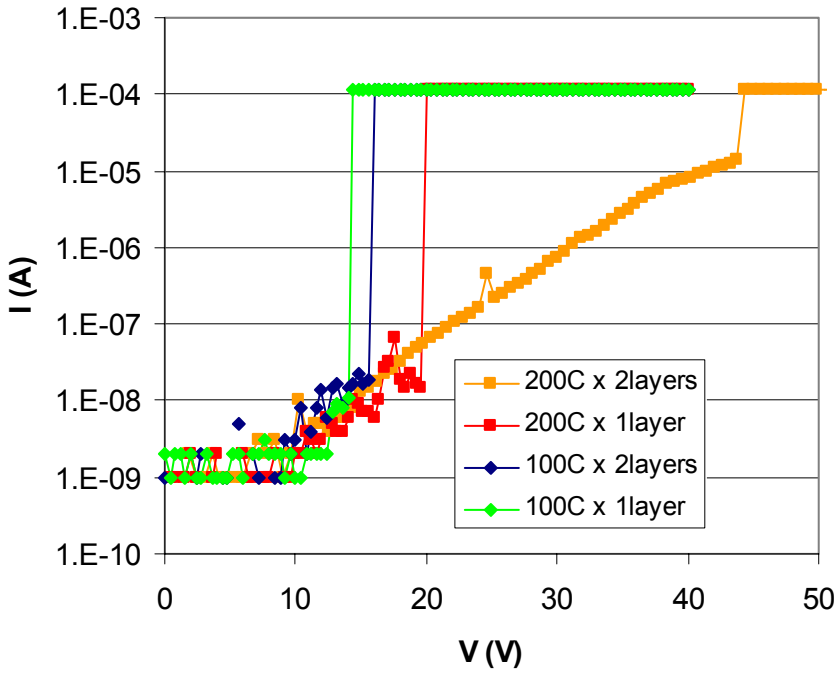

Figure 7.9: Leakage currents through PVP films with single and double layers and with different anneal conditions

7.2 Organic Diodes

The second main component for organic antifuses is the diode. Pentacene-based Schottky diodes have received the most coverage in literature due to their ease of fabrication and high performance. A large differentiation between the devices made by different groups is the use of different rectifying contact materials. These devices have been created in-house.

7.2.1 General Operation

The diodes under investigation are created in a vertical stack structure, which fits well with the vertically-stacked antifuse array target. As seen in Figure 7.10, the device is created through three distinct layer depositions, avoiding any of the highly complex doping methods used in inorganic diodes. This simple stacking process lends itself to low-cost fabrication, as production costs plummet if each layer can be deposited from solution on a reel-to-reel system, as mentioned in Chapter 2.

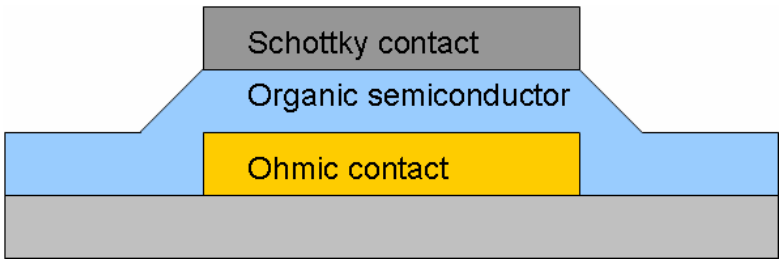

Figure 7.10: Vertically stacked organic diode structure.

The energy band diagram for these pentacene-based diodes is shown in Figure 7.11. Since pentacene is a p-type material, the Schottky junction is created with a low-workfunction conductor, such as aluminum or silver. This is the primary point of differentiation between published organic diodes, and will be discussed in section 7.2.3. On the left of Figure 7.11 is the ohmic contact to the pentacene material. To obtain this type of contact, high

workfunction materials are utilized, such as gold, platinum, and indium tin oxide (ITO). Although gold has a high workfunction (5.1eV), and should be sufficient in establishing an ohmic contact to the organic material, it often results in a minor schottky barrier due to interface pinning effects, likely promoted by high trap densities. In situations where this is critical, such as in high-performance OTFTs, platinum is utilized since its extremely high workfunction (6.35eV) overcomes these effects.

Most are familiar with Schottky contacts to n-type material, and the operation of this device is quite similar. If a negative bias is applied to the ohmic contact, the potential of the contact is decreased, pushing the semiconductor energy up on the band diagram. By doing this, the energetic barrier limiting hole injection into the Schottky contact ($q\Phi_i$) is increased, as in Figure 7.12 (left). Conversely, if a positive bias is applied to the ohmic contact, the potential of the contact is increases, pushing it down on the band diagram. As shown in Figure 7.12 (right), the energetic barrier limiting hole injection into the Schottky contact ($q\Phi_i$) is decreased. Thus, by diffusion, holes are increasingly injected into the Schottky electrode as the bias of the ohmic contact is increased. This current increase represents the drive current of the Schottky diode in the "on" state. Meanwhile, the barrier height for carrier injection into the organic semiconductor from the Schottky contact, $q\Phi_B$, remains unchanged regardless of what biases are applied to the system. This reverse current is therefore directly limited. However, like inorganic Schottky junctions, extreme reverse bias can increase leakage current through Fowler-Nordheim tunneling though the sharp potential gradient at the interface. When the high trap densities are taken into account, Poole-Frenkel tunneling can also lead to current leakage from the Schottky electrode to the bulk material during reverse bias. As discussed in Chapter 6, limiting this reverse-bias leakage is critical to the operation of an antifuse.

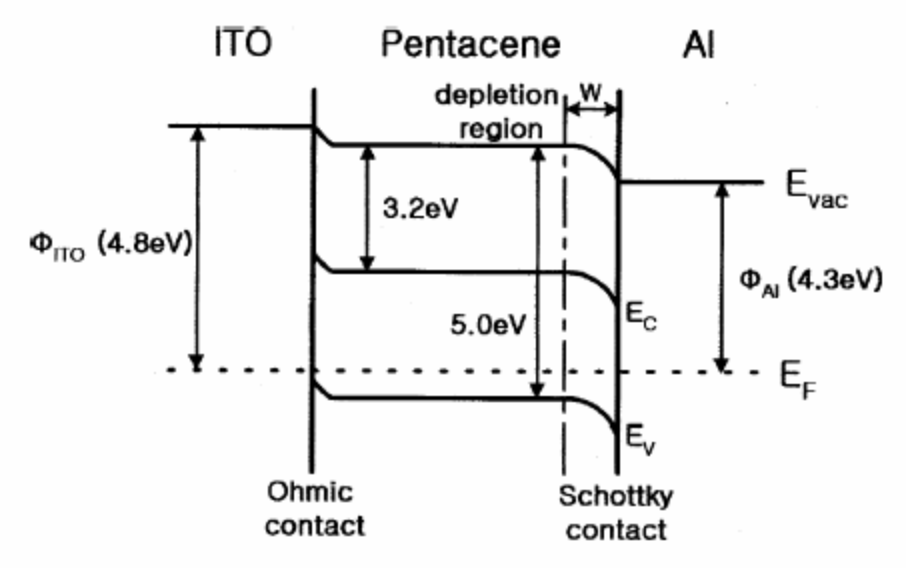

Figure 7.11: Band diagram for a pentacene Schottky diode [76].

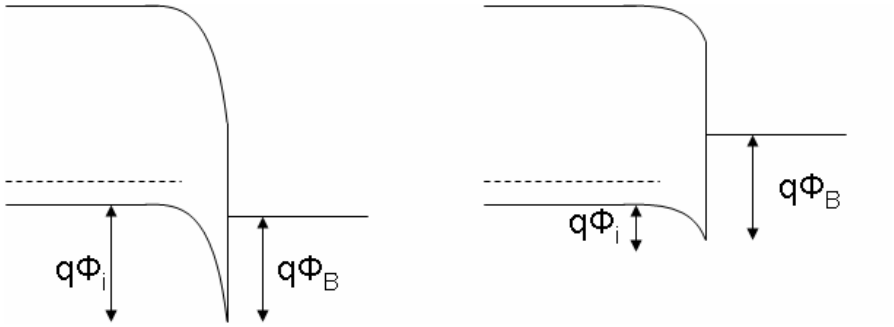

Figure 7.12: Schottky junction with a p-type semiconductor under reverse bias (left) and forward bias (right)

7.2.2 Current Regimes

Organic diodes operate in far more complex ways than simple p-n inorganic diodes. Whereas the operation of inorganic diodes is limited merely by carriers overcoming the potential barrier at the p-n junction, organic diodes undergo a variety of operational regimes.

When an insulative or semiconductive material is placed between two electrodes, the current-limiting mechanisms vary by applied electric field. Initially, when low fields are present, conduction through the device is ohmic in nature, assuming the field is large enough to overcome diffusion current. In this stage, the charge injected from the electrodes is insignificant in comparison with the intrinsic carrier concentration. Because of this, injected carriers can maintain charge neutrality, and no internal electric field is formed. However, once more carriers are injected into the bulk from the electrodes due to a higher applied electric field, the carriers are no longer able to maintain charge neutrality in the material, as carrier redistribution is governed by a time constant that is dependent on the mobility and intrinsic carrier concentration of the material. As a result, internal fields form, which prevent the injection of future carriers, therefore enabling the bulk to directly constrain conduction. This limiting effect, known as space-charge limited current (SCLC), is a prevalent effect in two-terminal devices utilizing organic polymers due to their low mobility and low carrier density (thus causing high relaxation times).

Operation becomes even more complex for the case of organic materials with high trap densities, as shown in Figure 7.13. When low bias is applied, nearly all of the injected charge goes to the localized energy levels, resulting in a low mobility[73]. As the bias is increased, additional carriers are injected, though at a slowed rate, due to SCLC, and the mobility is still low. However, with increased bias, the Fermi level of the semiconductor begins to rise above discrete trap levels, causing the traps to fill. As bias is increased further and the Fermi level approaches the delocalized band, even more traps fill, and carriers are directly injected into the delocalized levels. Because of this, a drastic increase in effective mobility is realized, which results in a rapid current increase. At this trap filling limit (TFL), charge injection is no longer

limited by SCLC. The transition from SCLC and TFL can also give rough insight to the total trap density via:

$$V_{TFL} = \frac{2qd^2 N_t}{3\varepsilon_s} \text{ [74]}$$

With V_{TFL} being the transition point between conduction mechanisms as seen in Figure 7.13, the trap density, N_t, can be extracted with knowledge of the film permittivity and thickness, d. Thus, a simple electrical sweep of the organic diode can quickly give a rough estimate of trap density, giving an approximate valuation of the quality of the organic deposition. At higher biases, the large carrier flow once again limits the material's ability to maintain charge neutrality, and the current flow becomes moderated by the internal fields generated within the bulk. This trap-free SCLC is the limiting effect in current flow until physical breakdown is reached at high electric fields.

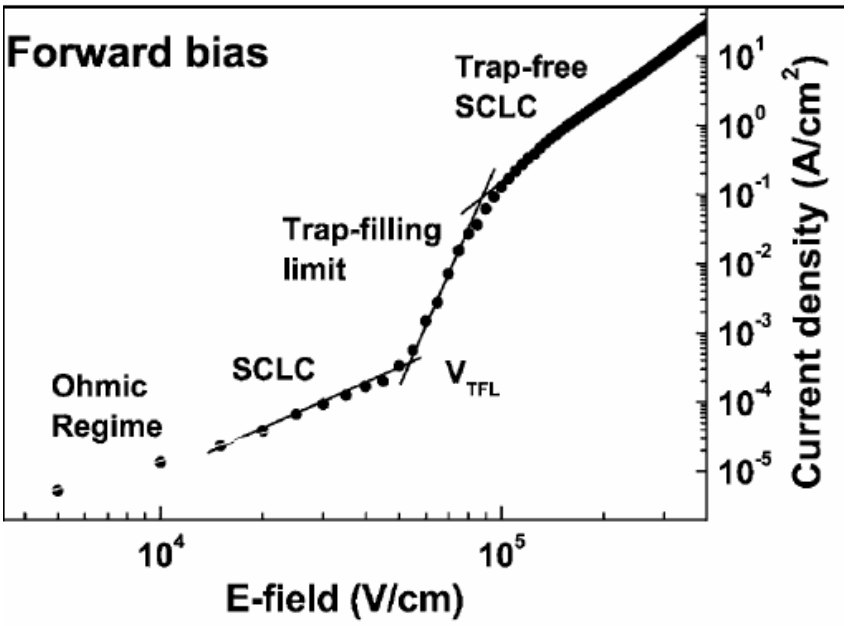

Figure 7.13: Current regimes for a Al/Pentacene diode [75].

This theoretical interpretation of current regimes is well-supported by literature [76]. In Figure 7.14, the space-charge limited current can be seen at low voltages. To follow with the above theory, the current then rapidly increases during the trap-filling limit, and eventually saturates at higher voltages via trap-free SCLC. The slope of the current increase at the trap-filling limit indicates that the traps within the device do not reside at a single energy, but are instead spread over a range of energies. Simply, as higher voltages are applied, the Fermi level moves within the pentacene bandgap, filling more of the traps. Also, the lack of any constant-current steps within the trap-filling limit indicates that the trap energies are fairly continuous within the semiconductor.

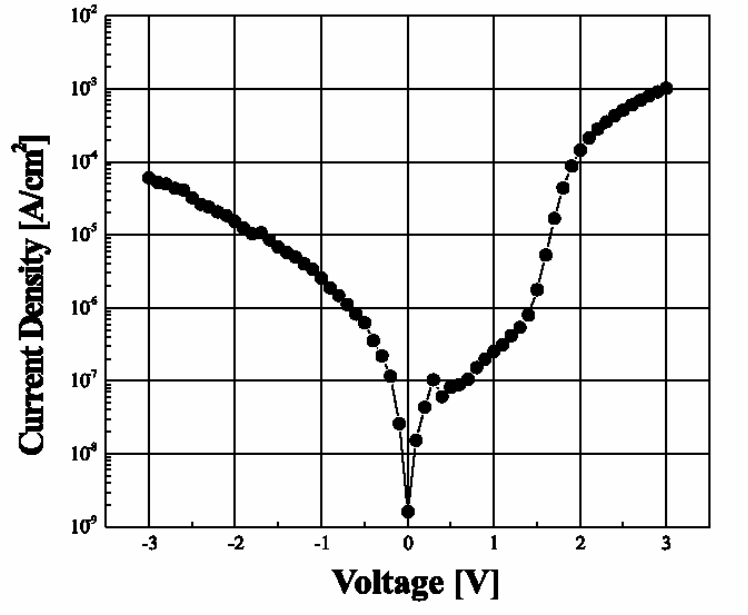

Figure 7.14: I-V characteristics of an ITO/pentacene/Al organic diode [76].

7.2.3 Schottky Contact Workfunctions

The engineering of the Schottky interface in organic diodes is also of critical importance to their behavior. In the most simplistic sense, the individual material workfunctions can be combined to determine the Schottky barrier height, as in [76]. In this work, the pentacene band edges are approximated at 5.0 and 3.2eV, with aluminum at 4.3eV [76]. As a result, a barrier height of 0.7eV is obtained. However, these classical calculations overlook interface interactions and band-level pinning, which can be induced by interface traps. Subsequently, Schottky barrier height can show variation between samples, and is best determined experimentally.

7.2.4 Initial Experimental Work

With the background of organic-metal schottky junctions and current regimes understood, a strong understanding has been developed for creating high-performance diodes. A literature

review reveals a vast variety of organic diode structures have been implemented, including Au/pentacene/ZnO:Al, SnO/pentacene/Al [77], Au/PEDOT:PSS/pentacene/Al [78], ITO/pentacene/Al [76], and many others. However, the vast majority of works on the subject have focused upon the simple Au/pentacene/Al system. Therefore, as a starting point, this device structure was developed in-house.

A 1000Å blanket layer of gold was deposited on a dummy silicon wafer. Pentacene that had been purified through the sublimation chamber was then thermally evaporated onto the wafer thickness at a rate of 6-8 Å/min. This evaporation was conducted with the wafer heated to 70ºC to increase molecular surface mobility, in the hopes of obtaining a well-ordered film. A final film thickness of 304nm was obtained. Finally, aluminum top contacts were evaporated through a shadow-mask, giving pad sizes of 200μm×100μm. Contact to the bottom layer was achieved by using a platinum probe to mechanically scratch through the evaporated pentacene layer. In contacting the top layer, care was taken to gently land the probe on the aluminum surface, to avoid puncturing through this layer and the pentacene underneath. In early devices, this was a commonly encountered challenge, as the pentacene layer was mechanically soft, causing the aluminum pads to break or flake off with little applied pressure. Eventually, by changing the pentacene evaporation conditions to increase performance in later experiments, the pad contacting problem also became eliminated, as will be discussed below.

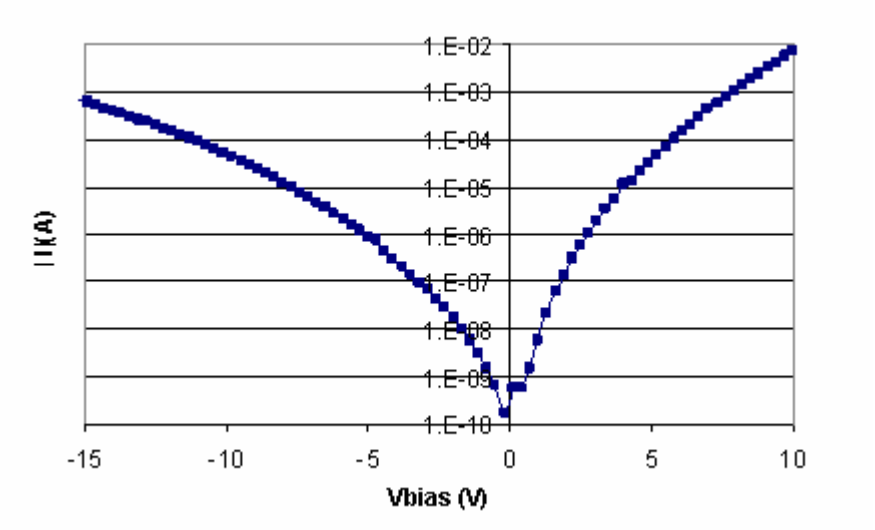

Figure 7.15: I-V characteristics of the first in-house organic diode.

An electrical sweep for a common device on this first in-house organic diode wafer is seen in Figure 7.15. While the drive current is on-par with the devices by Lee *et. al.* [76] in Figure 7.14, the reverse-bias leakage current is much higher. The result of this high leakage is the reduction in the effective rectification of the device. At 10V, the rectification is maximized at a factor of 140 for most devices. For the reasons mentioned in Chapter 6 concerning latch-up and accidental programming, the organic diode needs to more effectively limit current flow when under reverse bias. However, unlike the data from Figure 7.14, the trap-filling limit is reached immediately, enabling better turn-on of the device. Since V_{TFL} occurs near 0V, it can be said that the trap density is extremely low. This is expected, however, since the organic film was deposited at an extremely low deposition rate and with a heated substrate - both of which improve molecular ordering and limit defect density.

Another important characteristic of these organic diodes is their relatively low breakdown voltage. A cumulative distribution plot of the breakdown of the devices under forward bias is

shown in Figure 7.16. The exceptionally confined distribution of the breakdown voltages illustrates the excellent uniformity achieved during the deposition of the semiconducting film. However, the low breakdown of the devices would limit the yield of completed antifuse devices. If these diodes were to be directly integrated into an antifuse process, the fuse capacitor would need to achieve physical breakdown before 14V, but 'read' operations would still need to be performed at voltages near 10V to realize sufficient rectification. In other words, the 'read' bias would need to be large to ensure a diode could be identified as operating in either forward or reverse bias. The result is that the margin for device variation becomes narrow, and insulator thickness design must have exceptionally high tolerances to guarantee that the insulator breaks down in the appropriate range. As was shown in Section 7.1, such tolerances are difficult to achieve.

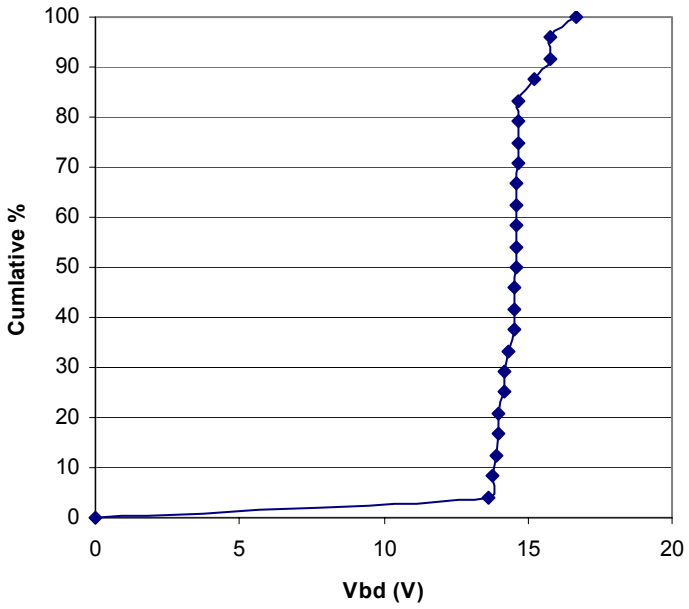

Figure 7.16: Cumulative distribution of breakdown voltages for the first in-house diodes.

7.2.5 Organic Diode Optimization

The organic diodes of Section 7.2.4 provided a framework for tailoring the performance of the organic diodes to suit the needs of an integrated antifuse. While the drive currents were large, reverse-bias leakage needed to be reduced, and diode breakdown strength improved to improve the operational window for antifuse programming.

It was proposed that the high reverse-bias leakage could be partially attributed to the high ordering of the first devices. With a lack of traps at the Schottky junction, it was deemed possible that interface pinning effects were possibly minimized, reducing the effective Schottky barrier height. The high ordering would also lead to increased conductivity through the bulk of the material, enabling large leakage currents. In fact, it was proposed that the high level of ordering was not ideal for organic diodes, and that trap-infested devices like those in Figure 7.14 could provide better overall performance.

Therefore, in developing the second round of diode experiments, it was decided that the wafer chuck inside the evaporation chamber would be held at room temperature during the pentacene deposition, as in [76]. Also, evaporation rate would be dramatically increased from 6-8 Å/min to 0.5 Å/sec. Finally, pentacene thickness would be increased so that higher biases would be necessary to induce a critical breakdown-inducing electric field.

As before, the diodes were created on dummy silicon wafers coated with blanket gold films. The pentacene was evaporated to a final thickness of 430nm, and an aluminum film of 2000Å was subsequently deposited through a shadow mask. For the testing of these devices, it was determined that a symmetric forward and reverse sweep could help identify any trapped charge located in the film through the generation of hysteresis effects.

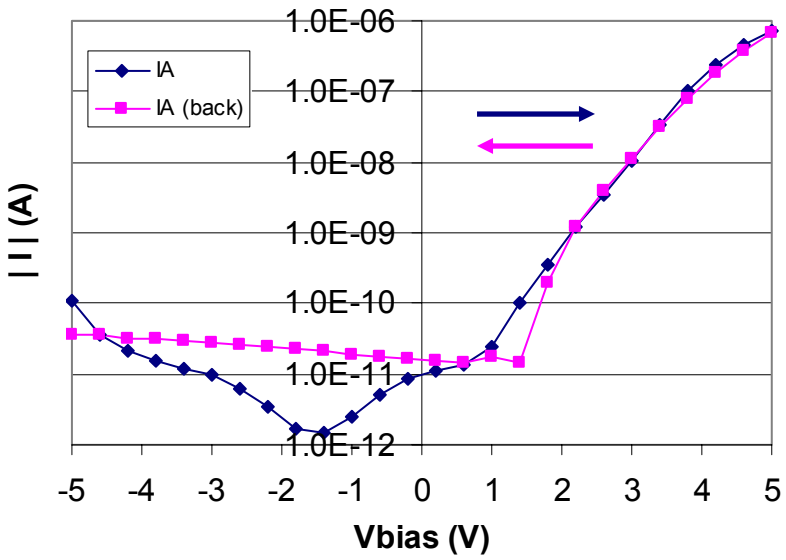

Figure 7.17: I-V characteristics of a second generation organic Schottky diode.

Vast improvements were found in electrical behavior, as shown in Figure 7.17. The deposition of a more disorganized film drastically reduced reverse-bias leakage, and as a result, significantly improved the device rectification factor. As expected, a consequence of this induced molecular disorder is also reflected in a decrease in forward-biased current. Compared to Figure 7.15, forward-biasing the device results in more than an order of magnitude decrease in current. This can be attributed to the decreased conductivity and the increased thickness of the bulk organic, adding a significant series resistance. Despite this, the device is far more appropriate for organic antifuse systems, and drive current though forward-biased devices is not a limiting performance factor. Current becomes positive at -1.4V during the forward sweep of Figure 7.17, indicating significant charging occurs within the film. However, it is perhaps more important to recognize the shape of the current increase as the device transitions into forward bias. In fact, if -1.4V is taken as a reference point for the beginning of forward bias, the forward sweep curve of Figure 7.17 demonstrates many of the

current regimes of Figure 7.13. Also, as expected, V_{TFL} is no longer zero like it was in the first generation. This confirms that the changes instituted in the pentacene deposition methods have significantly increased trap density, resulting in an increase in V_{TFL}.

The retesting of the second generation devices yielded far more data. In fact, the device characteristics represented in Figure 7.17 were far less common than those of Figure 7.18. This indicates that although some devices have significant trap densities as in Figure 7.17, Figure 7.18 demonstrates that excellent rectification can be achieved without having a detectable V_{TFL}. This diode has rapid turn-on characteristics, which will be beneficial in creating organic antifuses, as relatively low voltages can be used to reveal significant current differences between forward-biased and reverse-biased diodes. This enables low read voltages, which is beneficial for antifuse arrays by allowing a simpler power supply framework. Also, due to the suspected reduction in trap densities in comparison with Figure 7.17, Figure 7.18 shows a reduced sweep hysteresis.

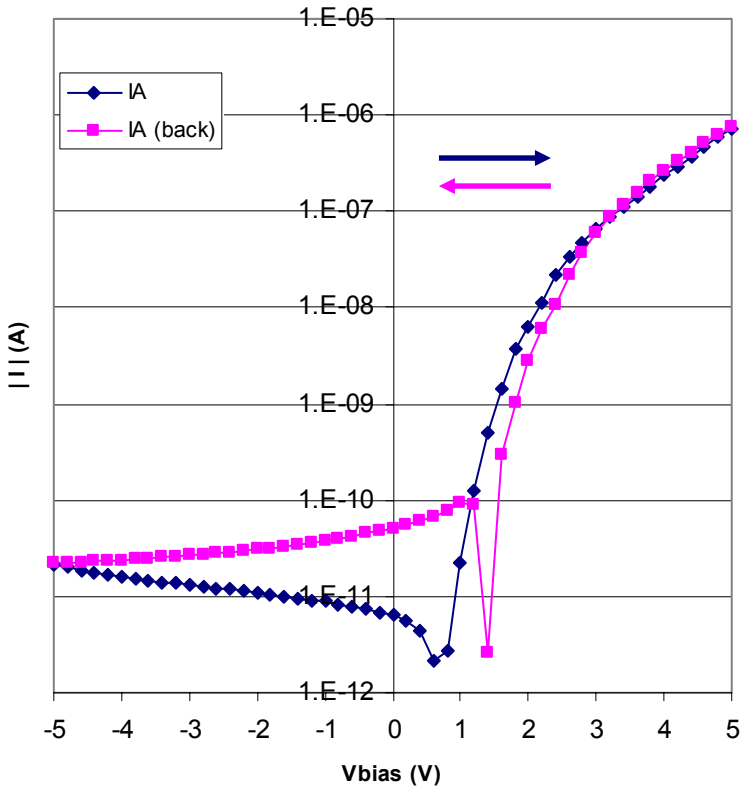

Figure 7.18: I-V characteristics of a second generation organic diode after two weeks of atmospheric hardening.

These devices were also tested at higher voltages to establish performance near breakdown fields. As in Figure 7.19, the current still continued to increase rapidly at higher biases, as the effect of trap-free SCLC was demonstrated to be minor. The devices also were far more resistant to breakdown, as the changes in deposition technique enable these devices to operate at voltages exceeding 40V. This vast improvement broadly opens the operational window for the dielectric breakdown behavior when this technology is integrated into organic antifuses. Also, as higher voltages are measured, the difference between forward-bias and reverse-bias current increases, as a rectification factor of 10^4 is easily realized at 30V. The leveling of

current on the right of Figure 7.19 is due to the power compliance of the testing equipment, and is not representative of the current limitations of the actual device.

The increase in leakage current with reverse bias is roughly linear when plotted on a logarithmic scale, as in Figure 7.19. This behavior is consistent with leakage methods through reverse-biased Schottky junctions, such as direct tunneling and Fowler-Nordheim tunneling. This leakage pattern reaffirms the fixed nature of the Schottky barrier height. Unlike the first generation, where the Schottky barrier height likely shifted with bias, integrating traps at the organic-metal interface has successfully locked the Schottky barrier height through Fermi pinning. Thus, this recipe is already well optimized to introduce a minimum of trap densities, while still enabling effective control of the pentacene-aluminum interface.

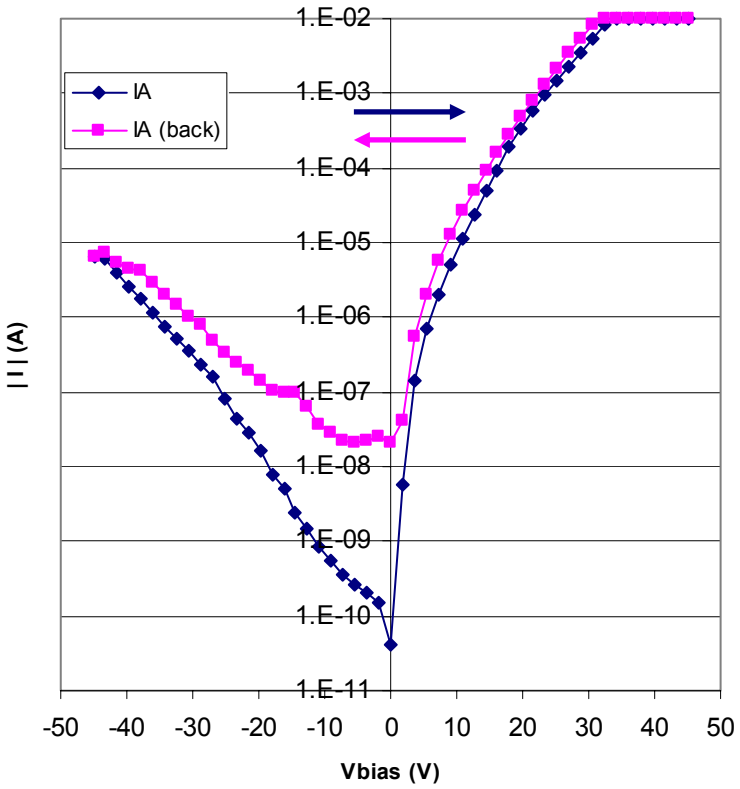

Figure 7.19: Second generation organic diodes tested at higher voltages.

The organic diodes developed here, are arguably the best in all reported literature. While other groups have demonstrated larger drive currents at smaller voltages, as in Figure 7.14 [76], none have effectively demonstrated devices with low reverse-bias leakages and such high rectification margins. Also, most devices in literature have not demonstrated the ability to function at voltages above 10V [75][76][77][78][79], and none have demonstrated operational voltages as high as 45V. For integration into organic antifuses, these pentacene-aluminum organic diodes are unmatched in performance, and well tailored to this specific application.

7.3 Organic Antifuses on Silicon

With the success achieved in building high-performance organic diodes, and the expertise developed in tuning the breakdown of the various dielectric fuse materials, the creation of an integrated organic antifuse appeared to be within the boundaries of the technological limits of organic electronics. The following sections explore the integration of the Au/pentacene/Al diode with the various dielectric materials characterized in Section 7.1, in the hope of creating reliable organic antifuse devices.

7.3.1 Silicafilm™ Antifuses

With the success seen by other groups with inorganic silica antifuses [70] and by the data taken for silica capacitors, pentacene-SOG antifuses were investigated. A thermally oxidized wafer was used as a platform, and blanket chrome and gold layers were deposited (25Å and 1250Å, respectively). 5000Å of purified pentacene was evaporated onto the surface at a rate of 2.5Å/sec to reduce film roughness. Such a thick film was deposited to ensure that no pinholes existed through the semiconductor material that would cause shorts in the device, which would result in MIM electrical characteristics. The evaporation rate was increased over the values used in Section 7.2.5 in an effort to reduce the film roughness of the pentacene layer. The reduction in roughness is necessary to minimize the breakdown variation in the dielectric layer, through the elimination of drastic localized thickness minima between the pentacene and the aluminum contact. SOG was spin-cast onto the wafer with a pour speed of 0RPM, which ramped to 4000RPM immediately. This film was then cured at 100ºC for 40 minutes, as in [70]. Finally, 2150Å of aluminum was evaporated though a shadow-mask to form the top-contact of the antifuse structure. The completed device structure is illustrated in Figure 7.20.

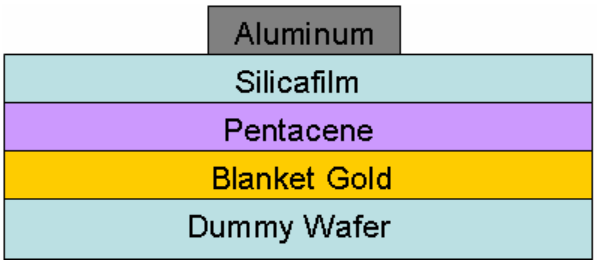

Figure 7.20: Cross-section of the Silicafilm-based organic antifuse.

These antifuses were then tested by gently landing a probe tip on the top contact while using a second tip to scratch through the SOG and pentacene layers to make a contact to the gold layer. The shadow-masked aluminum pads were roughly 100µm by 200µm, and were dispersed enough to allow plentiful space to scratch through to the bottom layer in nearby regions.

Unfortunately, these antifuses appeared to all have their SOG dielectric already broken down. As seen in Figure 7.21, the result is that the two-terminal device presents the characteristics of a simple diode. From this it is apparent that the schottky junction between pentacene and aluminum remains in tact, despite being physically separated by a conductive interlayer. While the goal was to have an insulative interlayer, it is still encouraging to see the diode survived the SOG deposition and subsequent anneal without a noticeable cost to diode performance. While previous capacitor tests predicted that the SOG insulator would produce a high-breakdown dielectric, many possible reasons exist that could explain this discrepancy. First, the roughness of the pentacene layer likely caused non-uniform Silicafilm™ coverage, resulting in localized thin spots or pinholes. Therefore, compared to the simple capacitor structures described earlier, the actual thickness of the Silicafilm™ spun onto the pentacene surface was vastly decreased. As the filament forms at the thinnest point in the dielectric film, since the

electric field is largest there, we would expect small thickness variations to have a significant impact on the fusing characteristics. As a result, thicker depositions of Silicafilm™ would be needed to overcome the pentacene surface roughness. Also, increasing the pentacene deposition rate should decrease the surface roughness of the film, better preparing it for a solution-based dielectric to be spun on top. The other source for electrical shorts has to do with the adhesion between films, which is discussed next.

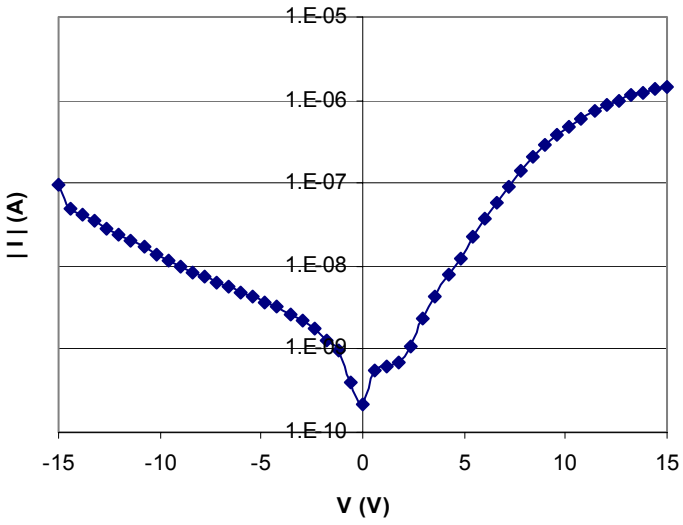

Figure 7.21: Electrical characteristics of a pentacene-SOG-based antifuse. Diode-like behavior is observed.

While the material background work that was done on Silicafilm™ capacitors and the simplistic antifuse looked acceptable for integration into the complete antifuse process, problems arose during development. Although the material spins well and evenly on a dummy silicon wafer coated with aluminum or gold, problems arose when more advanced structures were integrated. Due to solvents present in the Silicafilm™ solution, the pentacene layer was rapidly attacked, and adhesion became a serious issue. Initally, the problem was not obvious, as first-round mock-ups had blanket layers of gold (~50nm). In this case, the evaporated

pentacene bonded well to the gold, and macroscopically, the SOG spin appeared successful. However, after performing scanning electron microscopy (SEM), it was apparent that the SOG delaminated from the pentacene surface, as seen in Figure 7.22. The markers are included to verify material thicknesses and identity. From the top, Pa1 shows the gold contact thickness of 47nm, which is on target with our desired thickness of 50nm. Below this (the scan image from the SEM comes inverted), we see the multi-grain pentacene thin film. Along the gold interface we see slight gap formation and stacking faults, but as a whole, delamination of the pentacene film from the gold surface is minimal. The SOG, shown by Pa3, no longer rests on the pentacene film in this image. It is believed that the low-temperature anneal process of 100ºC performed following the SOG spin caused significant film contraction. In this case, the SOG delaminated from the pentacene surface, with a distance of ~150nm. Upon close inspection, the reflection of the pentacene topography can be seen in the delaminated SOG film, indicating that partial hardening and shape formation occurred before delamination.

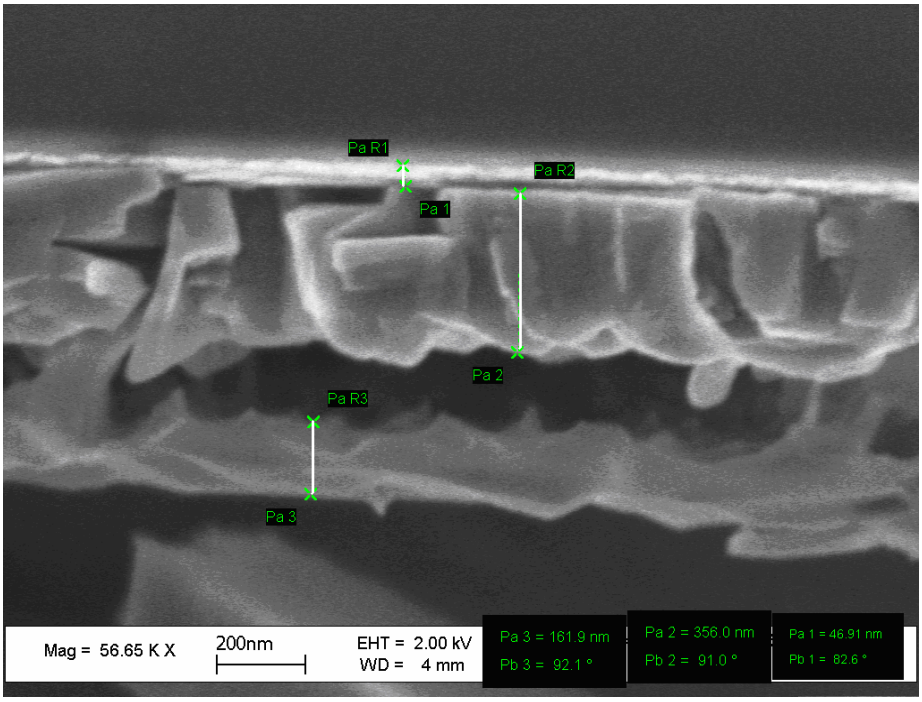

Figure 7.22: Delamination of SOG from the surface of the pentacene

The situation worsened when more accurate mock-ups were pursued. The first antifuse mock-ups used blanket gold films, which was not accurate of a full antifuse cross-array. In the second round of fabrication, the blanket gold film was replaced with gold pads defined through lithography and liftoff on top of thermally-grown silicon dioxide, as in chapters 3 and 4. In our process, evaporated pentacene tends to adhere to gold far better than to silicon dioxide. As a result, during the spin of SOG on the pentacene, large amounts of pentacene delamination occurred on the regions without gold pads. As before, pentacene on the gold pads remained with minimal damage. However, the delamination on the silicon dioxide regions was so great, that the pentacene-SOG films buckled, and folded onto one-another. Figure 7.23 shows an SEM image of the buckling phenomenon. In this cross-section, the first granular pentacene layer (top) is fractured and largely out-of-contact with the silicon dioxide wafer. Next, a gap is generated between the first pentacene layer and the SOG layer to a much

greater degree than seen in Figure 7.22. In some regions (right) the SOG delaminated from the pentacene, while in other regions (left), the pentacene remained bonded to the SOG, and both materials lifted from the substrate. Finally, a second pentacene layer is seen that is due to buckling from another region of the substrate. The large amount of physical damage caused by the SOG solvents and the subsequent film contraction during heating is unacceptable. Thus, this material was abandoned for the organic antifuse process, and more compatible materials were identified.

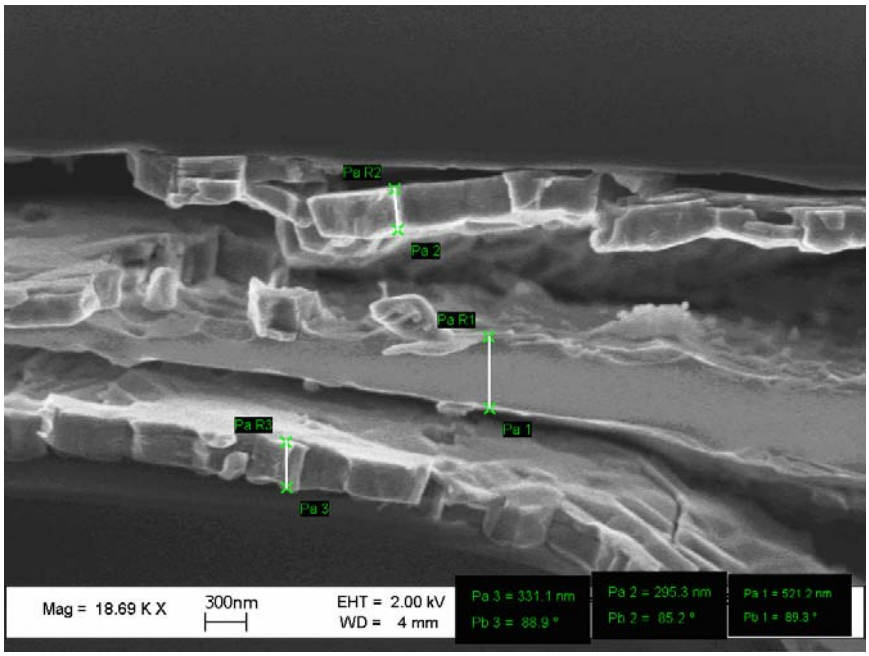

Figure 7.23: SEM image shoeing buckled layers of pentacene and SOG

7.3.2 PVP Antifuses

Since PVP had shown to operate well when deposited directly onto a pentacene surface in literature [27][29][30][31], it was expected to avoid the adhesion issues associated with Silicafilm™. To build basic PVP-based antifuses, a thermally oxidized silicon wafer was blanket coated with 25Å of chrome and 800Å of gold to form the bottom contact with strong

substrate adhesion. 3400Å of pentacene was thermally evaporated at a rate of 2.5 to 3.5 Å/sec. Since a breakdown less than 15V was the initial target, a 1% solution of PVP in 2-Propanol was prepared and spun onto the pentacene surface at 4000RPM, as in Section 7.1.3. Finally, using a shadow-mask, 1400Å of aluminum was evaporated to serve as a top contact and create the antifuse structure seen in Figure 7.24.

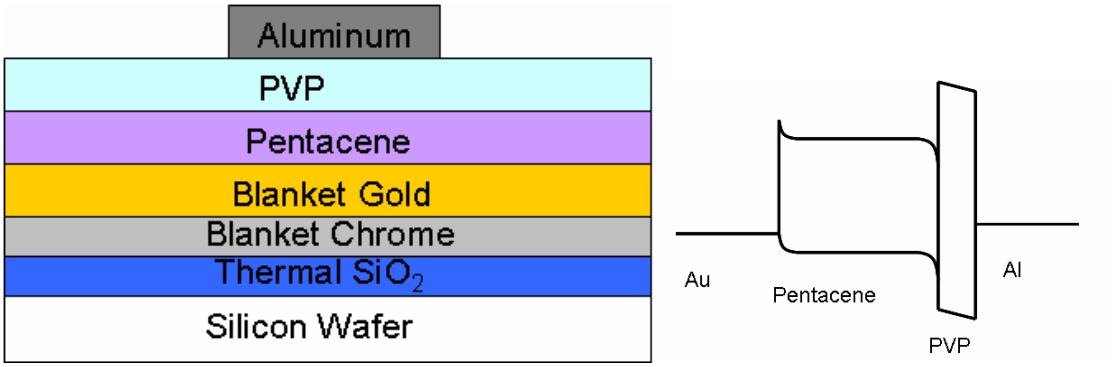

Figure 7.24: Cross-section of a PVP antifuse built on an oxidized silicon wafer (left) and band diagram (right).

These devices were first read by sweeping the voltage to a level below the estimated programming voltage, which, due to PVP capacitor characterization, was expected to be between 5V and 15V. As a result, the "read" voltage was 3V for this device. As can be seen in Figure 7.25 (left), the current is near the detectable limit for the equipment, resulting in significant noise. The device was then swept forward to a write voltage of 10V. As expected, the device broke down at 5.2V, resulting in a rapid increase in current. When the programmed antifuse was swept from the write voltage back to 0V, excellent diode characteristics were exhibited, as seen in Figure 7.25 (lower). Finally, the devices underwent the same read sweep as before to determine the margin of the device, as well as any hysteresis. From the difference in current at 3V for the unprogrammed and programmed device, we can see that the margin of this device is relatively low at 24. While this is low, it is already superior to the margin of the

Silicafilm™ work using silicon p-n diodes [70]. However, with the rapid increase in diode current as seen in the backsweep of the programming event, it is apparent that the margin could be dramatically increased by performing the read at a higher voltage. Unfortunately, these devices are limited in that respect, due to the low voltage needed to cause filament formation in the dielectric. Some hysteresis is also seen in the second read sweep of the device, indicating that trap levels are high. As is apparent, this read-write-read testing process quickly identifies some of the most important antifuse characteristics for this device.

While the margin of this device is low, and the dielectric breakdown was lower than intended, the first-ever organic antifuse has been demonstrated. This opens an entire new opportunity in low-cost memory devices. Once transferred to a process that enables printing these devices on flexible substrates, the price point for this technology can be identified, and is expected to be significantly lower than any existing memory.

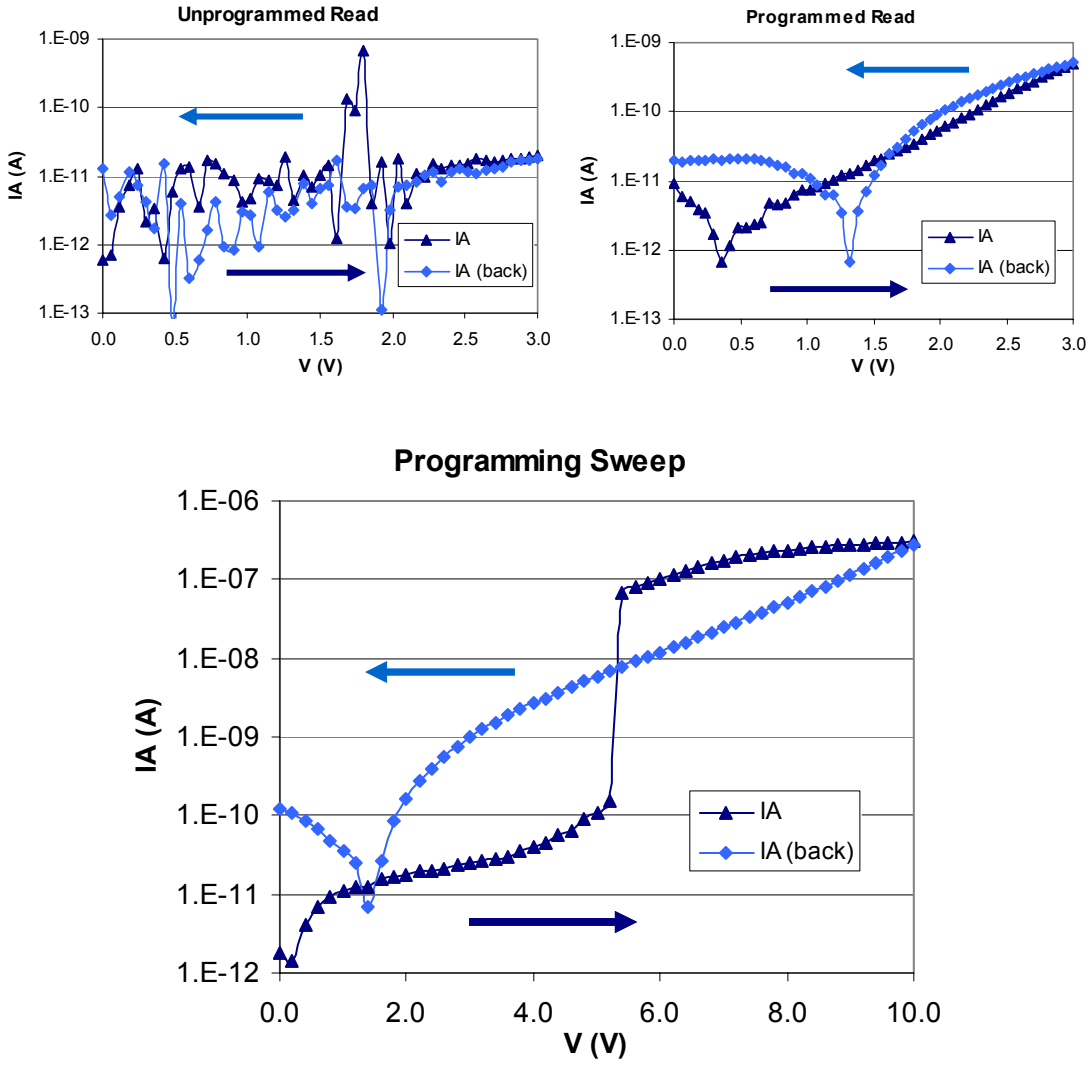

Figure 7.25: Read-Write-Read sequence for a PVP-Pentacene antifuse on a silicon substrate. The device cross-section was 100μm by 200μm.

While extensive testing was not performed on the first successful wafer, the five recorded devices demonstrated breakdowns between 4.4V and 5.4V, which is a relatively tight grouping. It also indicates that the breakdown of the PVP is lower than the target (10-15V). This is possibly due to the roughness of the pentacene surface on which it is spun, which can result in local thickness minima. To compensate for this effect, subsequent attempts were made to thicken the PVP film to a more desirable level.

The PVP thickness in next set of fabricated devices was modified by changing the spin speed, PVP concentration, and shear number of layers. Unfortunately, the film thicknesses created under different deposition conditions could not be readily measured. In general, profilometry would be used by creating a step via swabbing the material of interest with its primary solvent. In this case, however, this is not feasible since every solvent which removes PVP also removes the pentacene underneath. It is possible to spin the PVP material onto a dummy wafer and measure the thickness, as in Section 7.1.3, but as demonstrated in the first antifuse, the connection between this thickness and the PVP thickness on top of pentacene is only loosely tied. Therefore, different spin conditions were evaluated only upon their effect upon the antifuse electrical characteristics.

In one set, a baseline 1% PVP solution spun at 4000 RPM was used as the constant. From this, one wafer used a 2000 RPM spin speed, another used a 2% PVP solution, and a third used a 3% PVP solution. For the 2000 RPM spin, the voltage-induced programming event occurred from 5.7V to 11V, indicating that the deposited film was indeed thicker. The 2% PVP antifuses broke down between 6.8 and 23V. Finally, the 3% PVP sample indicated breakdown between 15V and 20V. Unfortunately, these samples all had extremely poor diodes due to inadequate purification of the pentacene material. The low ideality factors and low total current made distinguishing programmed and unprogrammed bits challenging, and resulted in margins of 10 at 3V. It was also concluded that optimizing the antifuse structure dielectric for surface roughness at this juncture was somewhat irrelevant, due to the fact that this device was to be created on a much rougher surface – plastic. At that stage, the optimization of the dielectric to perfect the device margin and programming voltage would be of more specific importance.

7.4 Conclusions

Through the investigation of dielectrics, metals, and semiconductors, the discrete components of an antifuse were demonstrated. In the course of material selection and optimizing the individual structures, a strong foundation was established for the integration of such devices into an antifuse. Utilizing a PVP dielectric and a pentacene organic semiconductor, the first-ever functional organic antifuse memory was created. This is just the first step. While impressive in its own right, this technology is advanced further in the next chapter by transferring the system to use plastic substrates, and through the creation of complete antifuse arrays instead of individual devices.

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Chapter 8: ORGANIC ANTIFUSE ARRAYS ON PLASTIC

To realize the potential of a low-cost reel-to-reel system for the fabrication of organic antifuses, the process must prove compatible with flexible plastic substrates. This issue is pursued in this chapter, as well as the creation of antifuse memory arrays to more accurately simulate the final antifuse architecture. Although the lateral density of the devices would be eventually limited by printing accuracy, density in the third dimension is investigated. By vertically stacking devices, high device density can be achieved, similar to what has been achieved in inorganic antifuses.

8.1 Organic Antifuses on Plastic

As was mentioned in the description of reel-to-reel processing in Chapter 2, a dramatic benefit of using organic materials is their ability to be deposited via solution. Another crucial characteristic is that they can be activated (through bulky side-group dissociation) by heating to temperatures below the melting point of common plastics. This allows them to be fully integrated into a low-cost reel-to-reel fabrication system. The first step in proving the acceptability of organic antifuses to such a system is to prototype them on plastic substrates, so that the directly introduced challenges can be overcome.

To limit variables and to make the change in substrate materials as straightforward as possible, the vast majority of the processing steps were kept the same as the first working antifuse from Chapter 7. However, specific challenges existed in the transfer. The smoothness of the oxidized silicon wafer that was used before was exceptional. Flexible substrates, on the other hand, were due to have much more roughness. As was experienced with the roughness of

pentacene in the previous chapter, local thickness minima could form in the dielectric, reducing the breakdown voltage required to program. Thus it became readily apparent that steps would need to be taken to reduce the roughness of the plastic surface prior to device fabrication.

8.1.1 Substrate Preparation

In this process, a polyethylene napthalate (PEN) plastic was selected as a substrate material due to its high melting point (>250ºC), and its proven compatibility with organic devices [86]. This material undergoes some degree of shrinkage during heating, but pre-cycling prior to device fabrication can limit the effect upon devices, as subsequent shrinkage is reduced. As in [86], the material was smoothed by coating the surface with multiple layers of cross-linked PVP [87]. PVP was mixed in propylene glycol monomethyl ether acetate (PGMEA) at 13% by wt. The liquid cross-linking agent poly(melamine-co-formaldehyde) methylated (PMFA) was added at 1% by volume. After sonication, the solution was filtered using a 0.25μm Teflon filter to remove any particles that could induce streaking upon spinning. In substrate preparation, a square of PEN is cleaned with acetone and 2-propanol, and dried with a jet of particle-filtered nitrogen. The PEN is then mounted to a mechanical-grade silicon wafer using Kapton tape as an adhesive. The cross-linked PVP is poured onto the wafer at 0 RPM, and the wafer is ramped to 800RPM, and held at that speed for 40 seconds.

Due to the poor uniformity and accuracy of in-house hotplates, the PEN was removed from the dummy wafer, and mounted to a stainless steel vacuum heating plate with Kapton tape. Using the precision heating chuck on the in-house inkjet printing system, the PEN was heated at 100ºC for 1 minute and 200ºC for 5 minutes to induce cross-linking in the film. Due to the vacuum system pulling the PEN to the stainless steel plate, PEN contact with the surface was

achieved, enabling improved heating uniformity. Due to the strength of the Kapton tape mounting adhesive, film contraction was also retarded upon heating, which is beneficial in the reduction of warping.

This entire process was then repeated. The PEN square was remounted to a mechanical grade wafer using Kapton tape, and cross-linked PVP was spin-cast at 800RPM. After transfer to the stainless steel plate, the sample was reheated. Finally, the PEN was remounted to a mechanical grade wafer for the remainder of processing steps. Although involved, any gains in device yield due to this complex processing cycle make the substrate preparation worthwhile.

8.1.2 Single-bit Antifuses on Plastic

Besides the substrate preparation, the antifuse process was similar to the initial working process on oxidized silicon wafers, as shown in Figure 8.1. 3600Å of pentacene was evaporated onto the 1300Å blanket gold layer. To compensate for the expected roughness, two layers of 1% PVP in 2-propanol were spin-cast, with a 5 minute anneal at 100ºC anneal after each layer. Finally, 1900Å of aluminum was evaporated through a shadow-mask to create 100μm by 200μm electrodes.

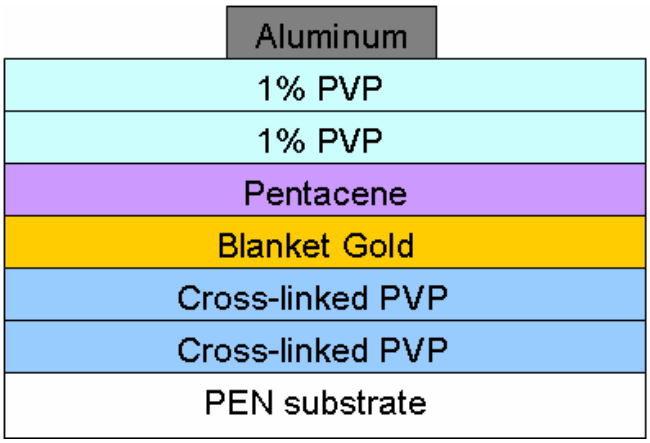

Figure 8.1: Cross-section of an organic antifuse on a PEN substrate

8.1.3 Electrical Characteristics

Surprisingly, these devices demonstrated electrical behavior superior to the antifuses using silicon substrates. This result was largely due to the excellent turn-on characteristics of the organic diodes, which is likely due to better pentacene purification and gained expertise in pentacene evaporation. In a typical antifuse bit, as in Figure 8.2, significant changes in forward-biased current could be seen between a programmed and unprogrammed bit. At 3V, margins greater than 100 were common. As expected, the roughness of the plastic caused the breakdown for the two-layer dielectric to be low. Most bits demonstrated breakdown below 8V and above 4V, despite the experimental breakdown target being 10V. Two devices achieved breakdown at voltages greater than 12V, which would be expected for stacked 1% PVP layers as per the PVP capacitor work of Chapter 7. This indicates that on devices where roughness does not play a large role, the expected breakdown voltage can be obtained. While statistically substantial amounts of testing were not performed, this device gave insight into process modifications to perfect the structure and compensate for surface roughness. This rudimentary device is the first demonstration of antifuses on flexible plastic substrates.

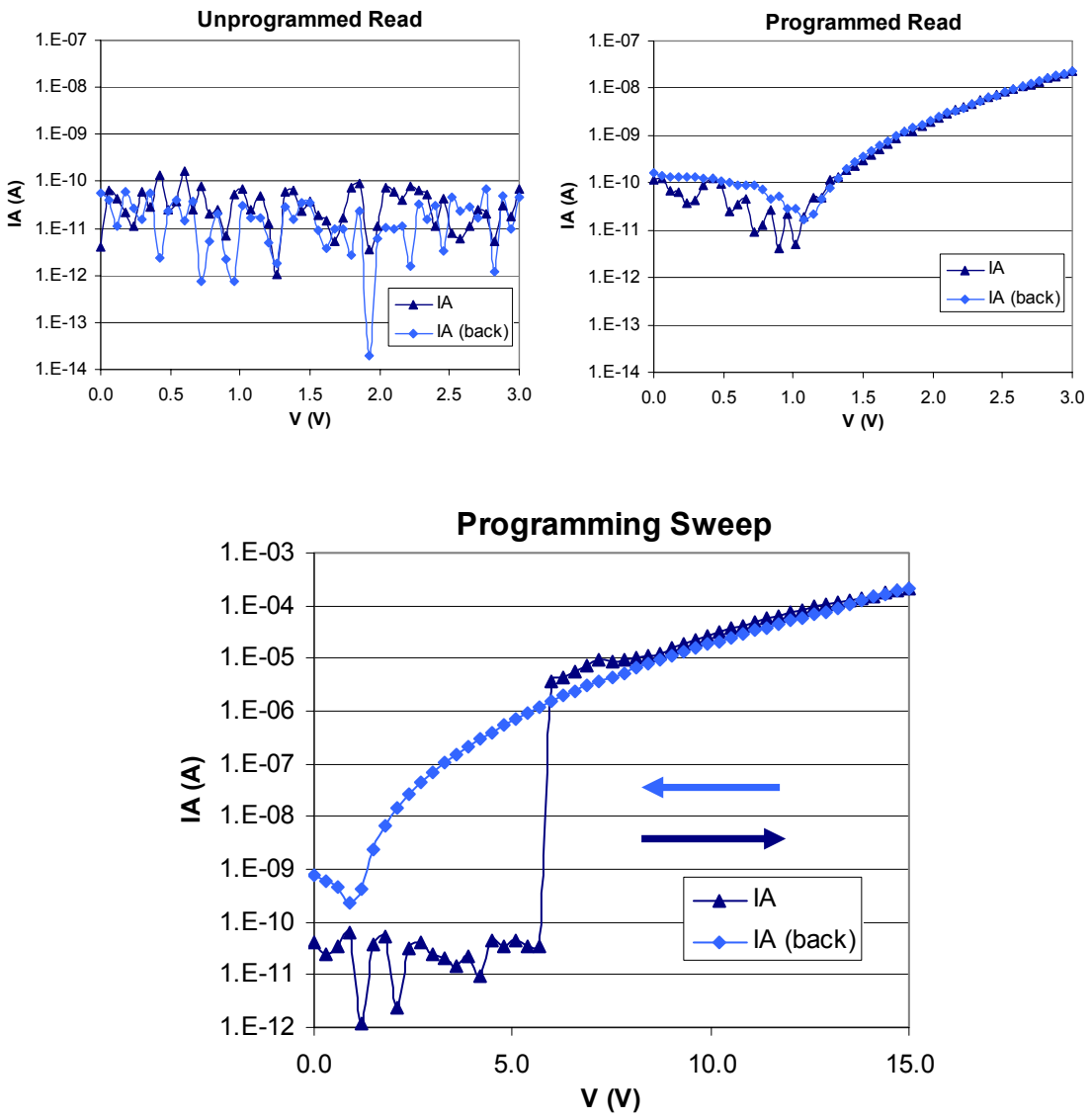

Figure 8.2: Electrical characterisics of the first antifuse on plastic. Read of an unprogrammed devie (top left), programming sweep (center bottom), and post-programming read sweep (top right).

Besides problems with breakdown voltage control, these devices demonstrated issues regarding dielectric healing. A severe example of this problem is shown in Figure 8.3. In this case, the programming sweep proceeded normally, with the dielectric breakdown occurring at 5V. However, during the voltage backsweep to the left, which is used to show the diode

characteristics, the dielectric healed, and current instantaneously dropped to pre-programmed levels. The subsequent read sweep verified that the bit indeed appeared unprogrammed. With the programming sweep lasting approximately 20 seconds, the data retention time for programmed bits was demonstrated to be as low as 15 seconds. However, in the more common case, the dielectric healing event takes minutes to occur. As shown in Figure 8.4, over the course of healing the forward-biased diode current incrementally drops until a discrete healing event occurs. For the sample of Figure 8.2, the bit remained programmed for 5 minutes, but after 10 minutes the current dropped to levels identical to those of an unprogrammed device.

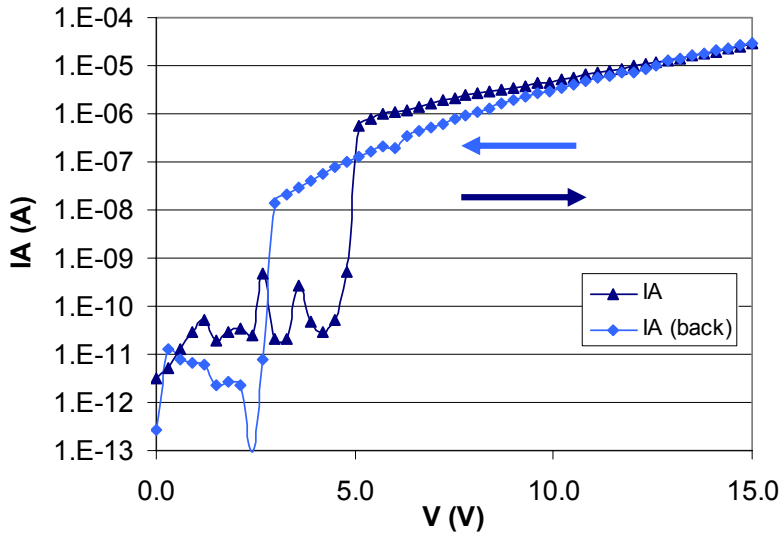

Figure 8.3: Healing event during the programming backsweep.

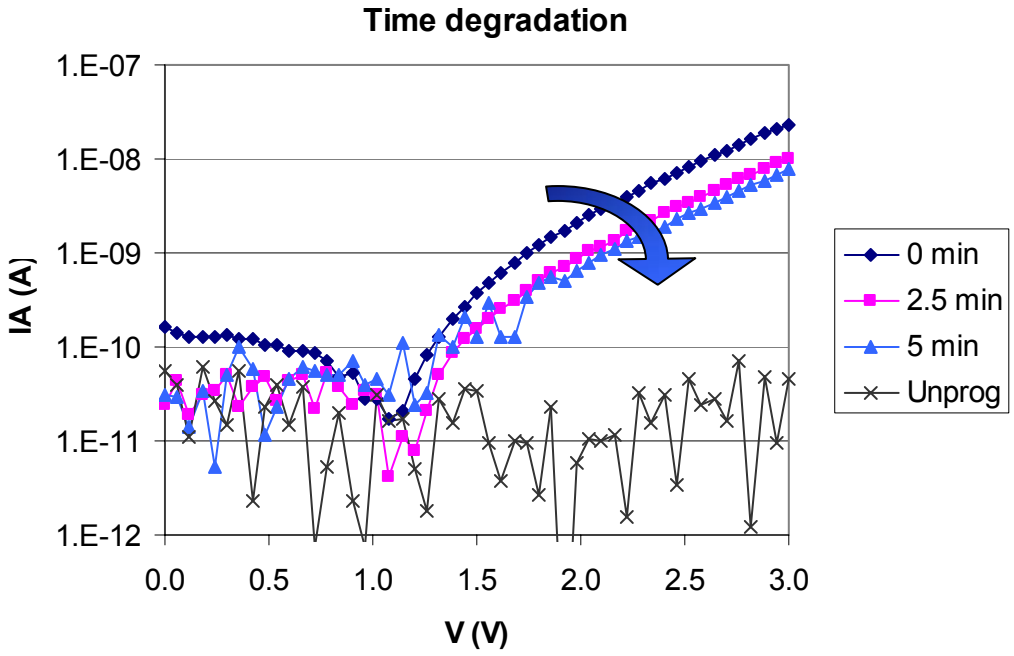

Figure 8.4: Forward biased current after 0, 2.5, and 5 minutes showing the reduction in margin. Current of the bit before programming is shown for reference (Unprog).

A final challenge faced with these devices was the inherent difficulties in obtaining reliable electrical probing. By having a blanket gold layer, all regions below the top electrode serve as an active device. In order to have an electrode large enough to land a probe onto, the top electrodes were required to be larger than 100μm × 100μm. Thus, device scaling was directly limited. Since the breakdown voltage of a bit was governed by the thinnest point in the dielectric, large areas were due to incorporate more defects, lowering the average breakdown voltage of the array.

A more important side effect of the structure involved the mechanical forces placed upon each device. Since the probe was placed directly on top of the device in the original structure, the force applied to the probe to obtain a good electrical contact placed unnecessary force on the dielectric and semiconductive interlayers. As high-temperature anneals were not used to

harden the PVP layers, the introduced force could result in a decrease in effective thickness. As illustrated in Figure 8.5 (top), this pinching effect could result in decreased breakdown voltages. A direct solution to this problem is to not deposit the bottom electrode as a blanket film. By having features defined on the bottom layer, the top electrode can have regions not directly over the active device, as in Figure 8.5 (bottom), thus avoiding a pressure pinching of the dielectric.

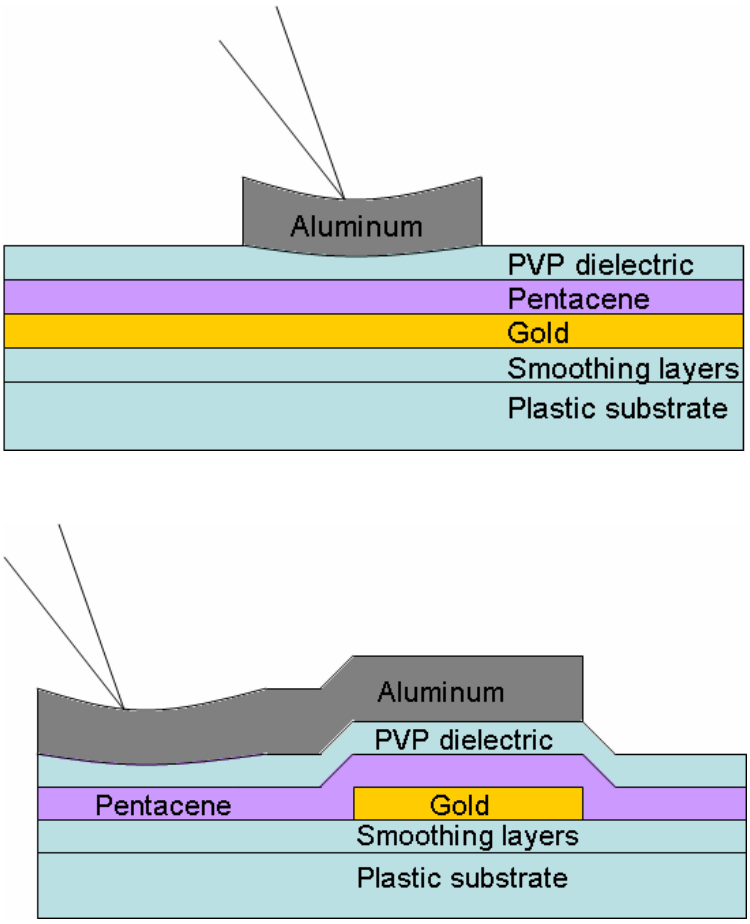

Figure 8.5: Pinching effect of probing a stacked antifuse (top) and the effect of probing a cross-array structure (bottom).

The patterning of the first electrode layer can be performed in a more useful manner to create more complex circuits. Up to this point, all devices tested were discrete antifuses with a

common bottom electrode, as in Figure 8.6. This is an unrealistic design for functional memory arrays, but was pursued due to its simplicity. Through the design of a shadow-mask with parallel lines, cross-array structures could be fabricated by placing the first electrode layer perpendicular to the second electrode layer. In this work, 10×10 arrays were constructed in this manner. As seen in Figure 8.7, this array structure enables the memory to have independent word and bit lines, and creates a memory array whose bits are easy to access. However, by increasing the topography of the first layer, uniform deposition of the PVP dielectric becomes even more challenging. Having a cross-array structure is useful in demonstrating the nonidealities of the array structure, such as the effect of leakage paths on device programming.

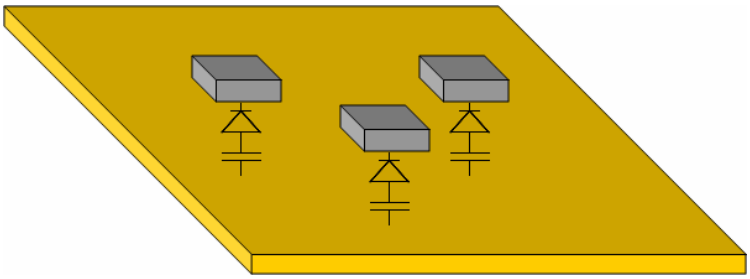

Figure 8.6: Blanket deposition of the first layer lead to discrete devices located underneath the aluminum electrodes.

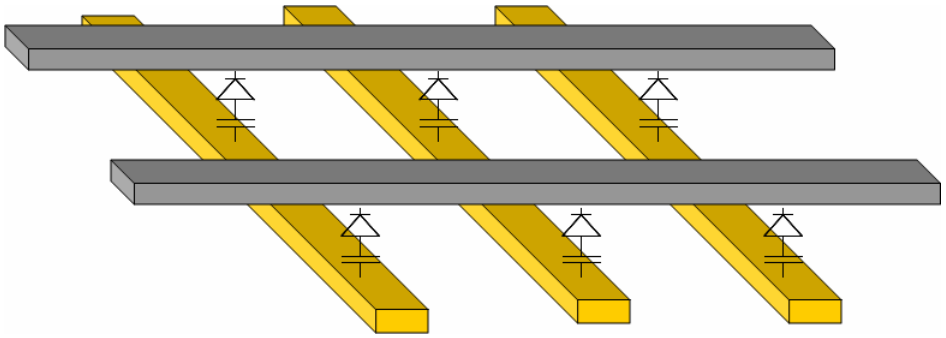

Figure 8.7: Memory array structure enabled by the creation of crossing electrode layers.

8.2 Primary Antifuse Memory Arrays

At this stage in development, the antifuse cross-arrays were built on plastic substrates, resulting in flexible samples as in Figure 8.8. These devices were optimized to improve yield, margin, and dielectric breakdown. This structure, to be called the "primary" antifuse structure for reasons explained later, proved to be very successful.

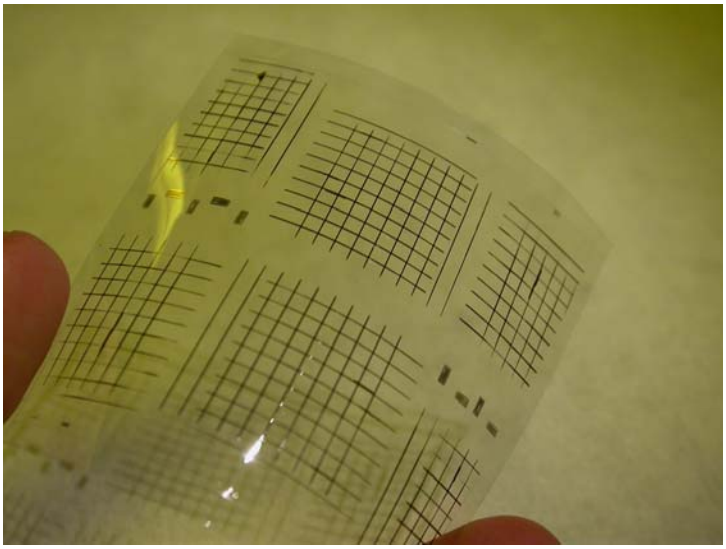

Figure 8.8: Antifuse arrays on a PEN flexible substrate.

8.2.1 Primary Antifuse Characterization

The cross section for these cross-array based devices is shown in Figure 8.9. In this structure, 1300Å of gold was evaporated through the cross-array shadow mask onto the PVP-smoothed plastic substrate to create the horizontal lines seen in Figure 8.8. Through insight gained by undergoing parallel diode experiments, the pentacene evaporation rate was increased to 4Å/sec for this work. This increase in rate results in decreased pentacene roughness, which enables the PVP dielectric to be deposited more uniformly. This uniformity is important for

the reduction of breakdown distribution of devices across the memory array. The pentacene thickness varied by run, but was between 3200Å and 3600Å. For the dielectric, a 2% PVP film in 2-propanol was poured at 0RPM, and quickly ramped to 4000RPM. After a 5 minute anneal at 100ºC, a 1%PVP layer was spin-cast at 4000RPM and annealed at 100ºC. Finally, 1500Å of aluminum was evaporated through another cross-array shadow mask to create the top electrodes of the memory array. As a result, the device area was roughly 100μm by 100μm.

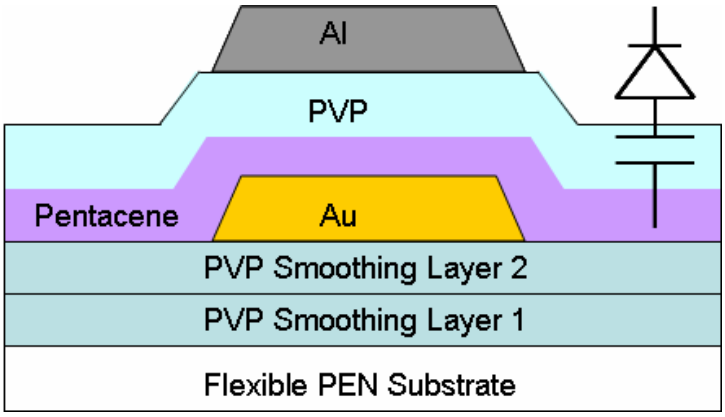

Figure 8.9: Cross-section of an organic antifuse element from an antifuse cross-array memory.

By increasing the thickness of the dielectric layer versus that of the single-bit antifuses, leakage current was drastically reduced, and the increased topology was compensated for. As seen in the first read sweep of Figure 8.10 (top left), the leakage values have been reduced from those of the single-bit devices of Figure 8.2. It is also readily apparent from the programming sweep that much higher margins are possible due to the reduction. In fact, if a read voltage of 10V is used in Figure 8.10, margins of 10^6 can be obtained. The largest possible margin occurs at 16V, where a margin of 5×10^6 is demonstrated. While the use of such high voltages is impractical, it does show how reduced leakage directly affects margin.

With the decreased pentacene roughness through increased evaporation rate, and the increased dielectric thickness, these devices could be read confidently at 5V. Due to the dielectric uniformity, accidental bit programming at 5V was rare, and yields above 90% were achieved. A second consequence of the increased pentacene evaporation rate was an increase in the rectification of these devices. The low reverse-bias leakage aids in the reduction of disturb events in arrays and enables larger lateral arrays.

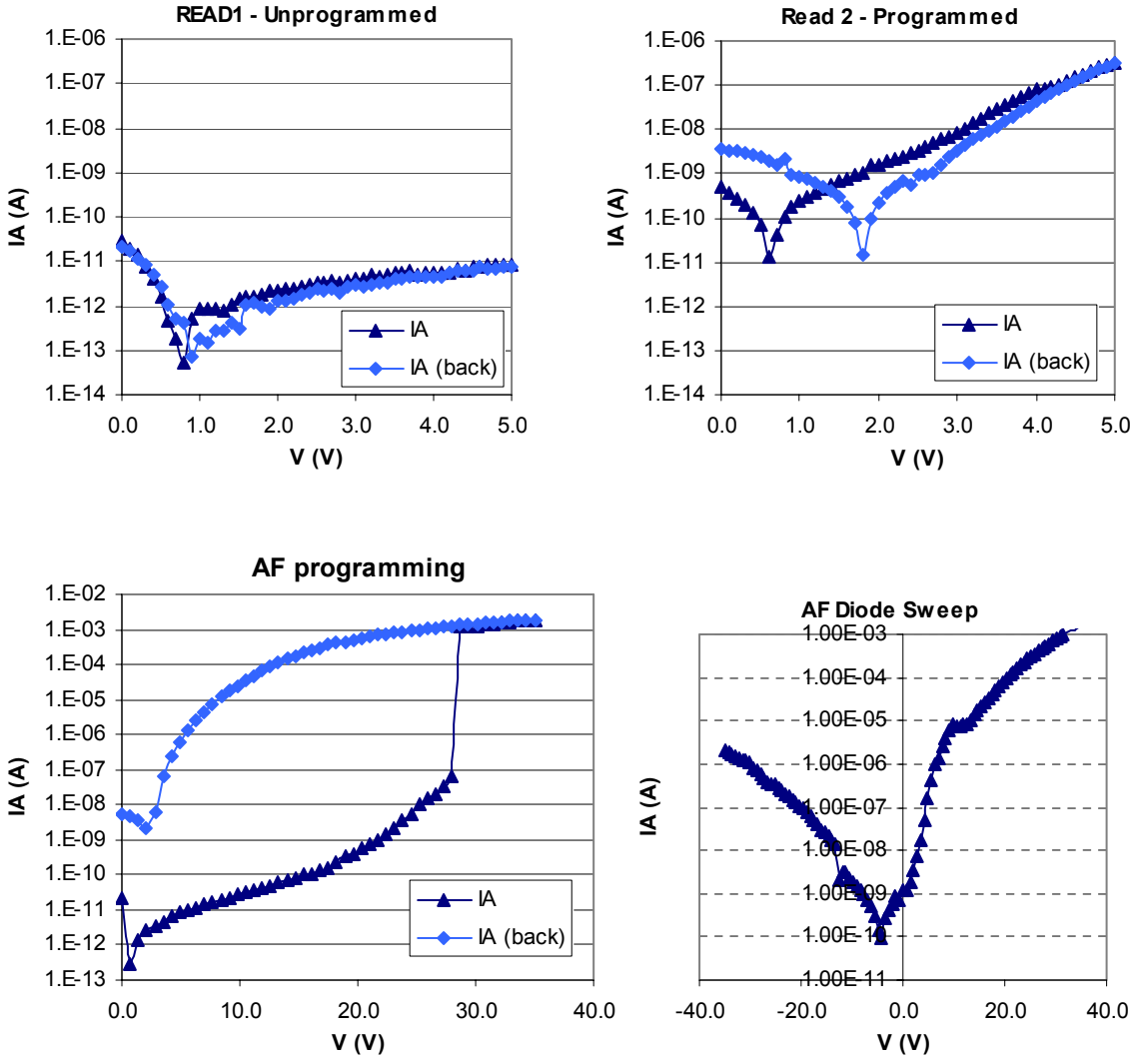

Figure 8.10: Electrical characteristics of the third generation "primary" optimized antifuse. Initial read sweep (top left),

Programming sweep (bottom left), Second read sweep (top right), and diode sweep of programmed bit (bottom right).

8.2.2 Advanced Analysis of Primary Structured Organic Antifuses

8.2.2.1 Breakdown Distribution

While an individual device is demonstrated in Figure 8.10, analysis of the entire array of samples can give further insight to the robustness of the process and insight into the physical phenomena associated with programming. First, the distribution of breakdown (programming) voltages within the memory array is shown in Figure 8.11. While not particularly tight, it is reasonable considering the challenges in topography, gold roughness, and pentacene roughness. It is encouraging to see, however, that if the write voltage was kept to 10V and the read voltage remained 5V, half of the devices would function perfectly. Although this is nowhere near an industrial yield, it is encouraging for this experimental-stage work.

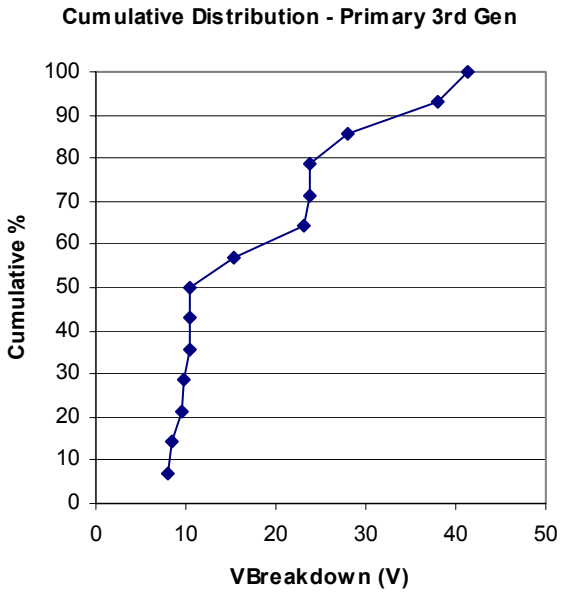

Figure 8.11: Cumulative distribution of the breakdown voltage for the third generation primary devices.

8.2.2.2 Distributions of Read Currents

Although the breakdown variation was large, the resulting currents from the programmed devices were uniform. Figure 8.12 illustrates the distribution of currents produced from the antifuse devices before and after programming at the read voltage. It is possible that the observed breakdown variation of Figure 8.11 was likely due to dielectric thickness variation. It then follows suit that this thickness variation could also produce significant variation in the current passing through unprogrammed devices, as the dielectric is the current-limiting element. Thus, with better control of the dielectric, it is conceived that the current distribution of unprogrammed devices could be tightened with better process control.

On the other hand, the current through programmed bits in Figure 8.12 is extremely uniform, attesting to the uniformity of the pentacene schottky diodes. This kind of repeatability is extremely attractive, as the sensing of bits would be simple in this case. Namely, bits demonstrating current $< 10^{-8}$A are unprogrammed, while those with current $> 10^{-7}$A are programmed. This means that even though individual device margins are much higher, an order of magnitude difference in current can still be seen across the entire memory array for programmed and unprogrammed devices. This margin is more than necessary to identify programmed versus unprogrammed bits.

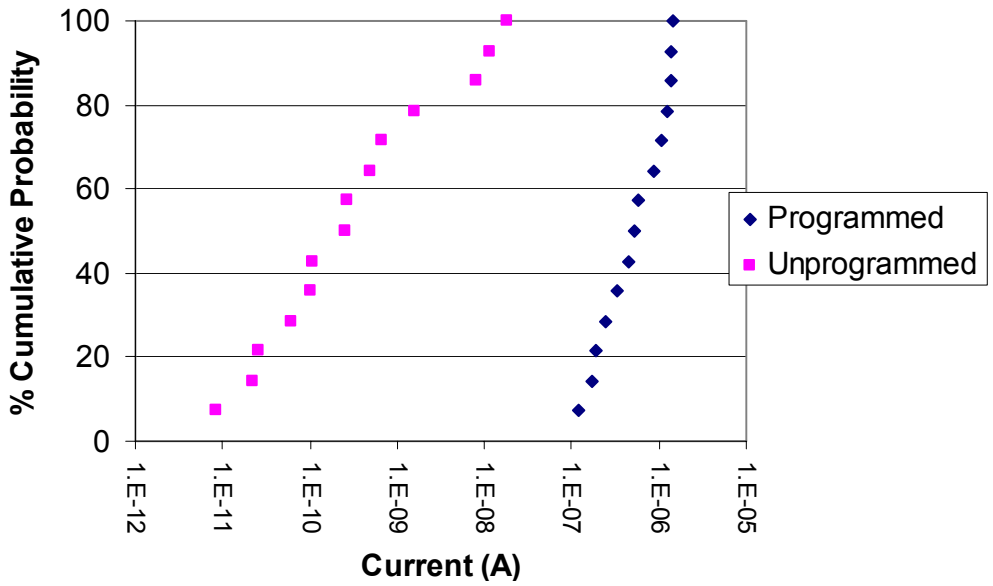

Figure 8.12: Probability plots of the programmed and unprogrammed currents at the read voltage (5V).

8.2.2.3 Diode Rectification

To further investigate the diode uniformity and performance, the distribution of forward and reverse biased currents propagating through programmed bits is plotted in Figure 8.13. With biasing set at the read voltage (+/- R), effective and reliable diode rectification is demonstrated. The roughly 3 orders of magnitude current difference in forward versus reverse biased diodes is illustrative of the effectiveness of the diode incorporation in enabling one-way programming. In other words, having low current flow through the reverse-biased diode shows that a significant voltage drop occurs across the diode. This prevents the accidental programming of the antifuse dielectric in a stacked structure, as introduced in Chapter 6. Individual devices consistently demonstrated rectifications greater than 10X, as seen in Figure 8.14.

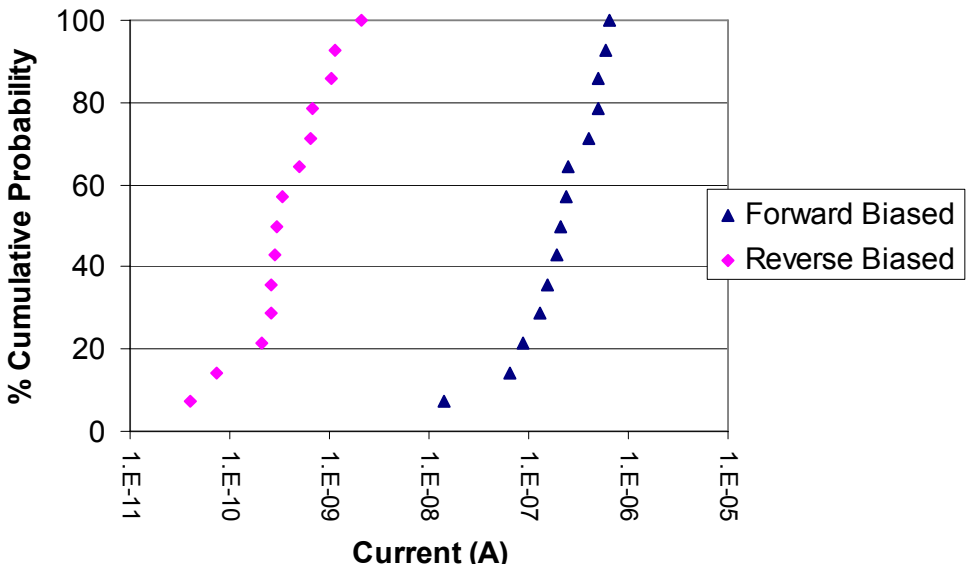

Figure 8.13: Distribution of forward and reverse biased diode currents in programmed antifuse bits, acquired at the read voltage (5V).

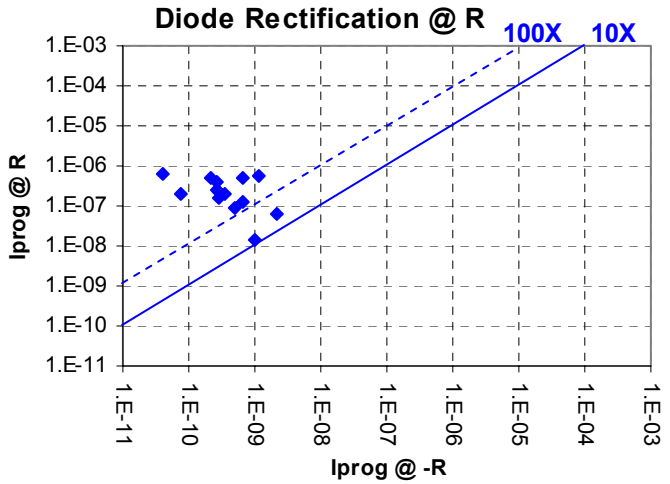

Figure 8.14: Diode rectification of devices at the read voltage.

Diode rectification is also crucial in the avoiding the disturb event of Chapter 6. As in that example, it is the reverse leakage at the highest voltage of the programming sweep that is of interest. Named the "preset W", it is generally much higher than the actual dielectric

breakdown programming event, to ensure that the majority of the devices undergo programming. For these primary antifuse arrays, this voltage is 35V. Figure 8.15 shows the excellent rectification achieved at this voltage. With differences in current averaging greater than four orders of magnitude, the diode serves to prevent accidental programming in a stacked structure, as intended. The low current passing through the reverse-biased bit enables larger arrays to be built before disturb events become a realistic problem. Assuming the organic transistor driving the wordline is capable of driving 10^{-2}A, which is practical for a large device, maximum functional array size can be calculated. Using the formula derived in Chapter 6, this technology enables memory arrays of 80,000 bits. Namely, an array with 282 bitlines and 282 wordlines can be constructed without the threat of disturb errors. This assumes a 10X necessary minimum difference in current between the driving OTFT and the combination of currents from leakage paths, which is reasonable since the "preset W" is more than 10% greater than the voltages needed to achieve dielectric breakdown.

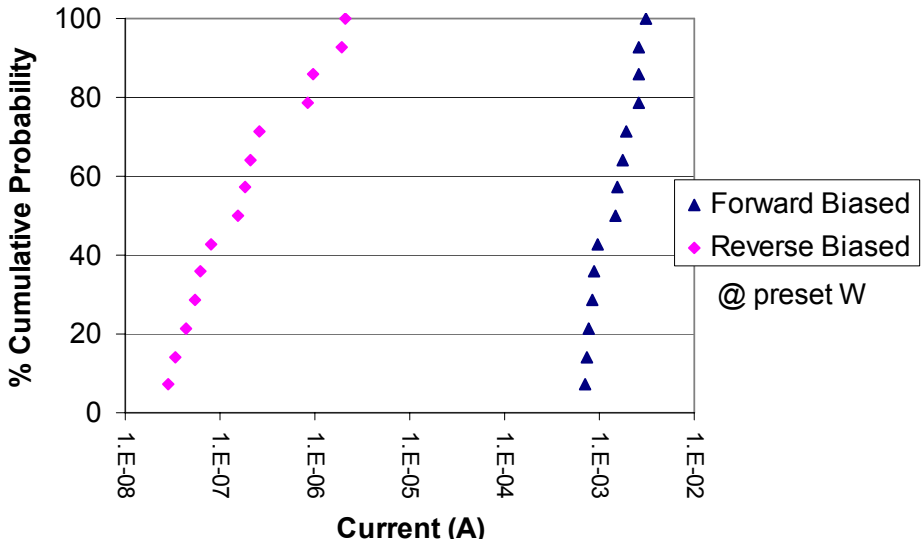

Figure 8.15: Forward and reverse biased currents of a programmed bit at +/- preset W (35V).

8.2.2.4 Filament Formation

Learning can also be achieved by analyzing how the margin varies with the programming (breakdown) voltage. As seen in Figure 8.16, devices that required larger voltages to program produced larger margins at the common read voltage (5V). Initial intuition leads to the idea that larger programming voltages could lead to larger filaments being formed during the breakdown event due to larger currents passing through the device. This would tend to increase the current measured at the read voltage of a programmed device, thus increasing the margin. However, this is not the case in these devices. Instead, by examining the relationship between programming voltage and the current through the unprogrammed bit at the read voltage in Figure 8.17, a distinct trend is observed. It is likely that the bits with thicker dielectrics would produce lower currents at a given voltage *and* require larger voltages to be programmed. It is through this mechanism that devices that called for higher programming voltages also produced higher margins. As the technology is perfected and programming voltage distributions tighten, Figure 8.16 gives an incredible amount of insight into the tradeoff between low programming voltages and high margins.

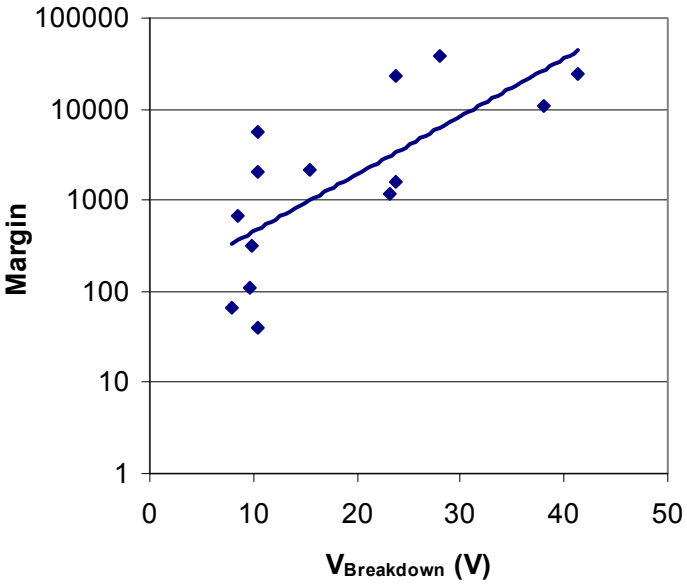

Figure 8.16: Device margin versus bit breakdown voltage.

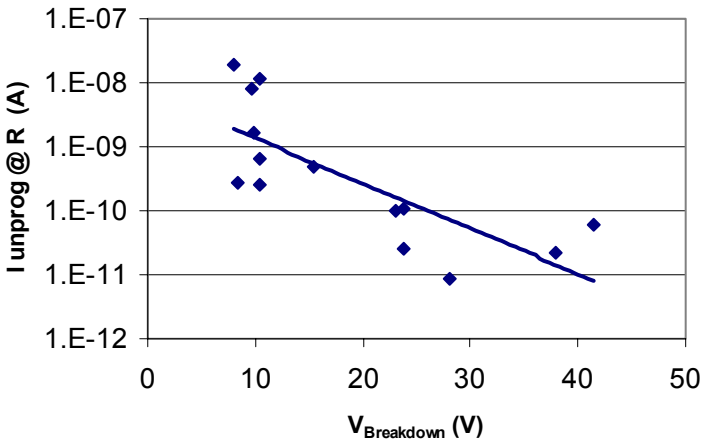

Figure 8.17: Current flowing through the unprogrammed bits at the read voltage vs. the respective breakdown voltage of the bits.

8.2.3 Fabrication Challenges and Non-idealities

Through the development of these antifuse arrays, leakage control emerged as the largest challenge. As was mentioned before, it was expected that the increased topography could

induce less-uniform insulating layers, due to corner rounding. However, when this structure was first investigated, the primary cause for this leakage was from pentacene particles becoming embedded in the PVP film.

In general, pentacene physically bonds much better to gold than to PVP-covered plastic. Without a blanket gold layer, pentacene directly resides on the PVP smoothing layers for the majority of the substrate area. During the spinning of the PVP dielectric, regions of pentacene would lose adhesion to the smoothing-PVP surface, and become embedded in the PVP dielectric. By having grains of conductive polymer embedded into the film, the leakage current likely increased through a Poole-Frenkel hopping mechanism. Also, it follows that embedded particles would not have a significant effect on the dielectric breakdown voltage, since the thickness and electric field applied to the film were essentially unchanged. The biggest problem with having this leakage is that it can directly lower device margins by increasing the unprogrammed current, and can also increase the power consumption of the memory array.

To prevent the delamination of pentacene from the substrate smoothing film, it was found that the pentacene adhesion issue could be eliminated by spinning the PVP dielectric immediately following the pentacene evaporation. It was seen that if more than two days passed between pentacene evaporation and the spinning of the PVP dielectric, pentacene would macroscopically delaminate from the smoothing layer, causing grains to become embedded in the PVP dielectric. This turned out to be a simple solution to a complex problem. While the root causes are expected to be related to the wafer storage in ambient atmospheric conditions, the exact reasons are unknown. However, with the known effects of light, moisture, and oxygen, as demonstrated in Chapter 3, it is not surprising that physical effects can go hand-in-hand with the proven electrical consequences.

With this knowledge, the leakage through unprogrammed devices was drastically reduced, as seen in Figure 8.18. By examining the current passing through the unprogrammed bit during the voltage upsweep, it is apparent that the elimination of pentacene delamination resulted in decreases of current by more than three orders of magnitude at 10V across three antifuse generations. This produces vastly increased margins in the primary device structure.

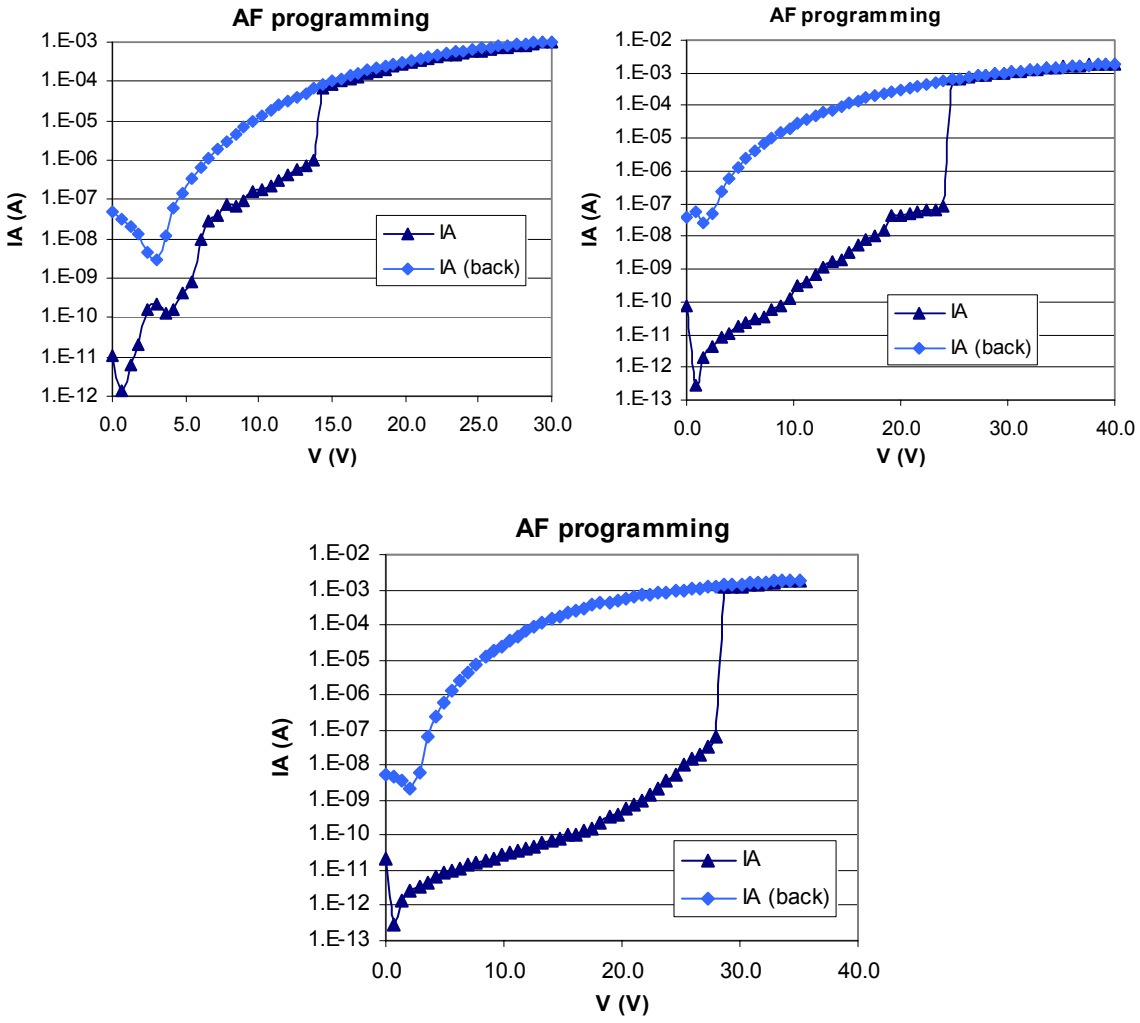

Figure 8.18: Programming sweeps for the three generations of primary antifuse devices, demonstrating off-state leakage issues. First generation (top left), second generation (top right), third generation (bottom).

The presence of these pentacene particles in the PVP layer of early generations may also be somewhat responsible for the large hysteresis effects (1V-2V) seen in the read sweeps of unprogrammed devices. The embedded particles could either be inducing increased trap densities, or collecting charge themselves. As seen in Figure 8.19, the hysteresis seen in unprogrammed devices (left) is completely eliminated in third generation devices (right), due to the reduction of pentacene delamination during fabrication.

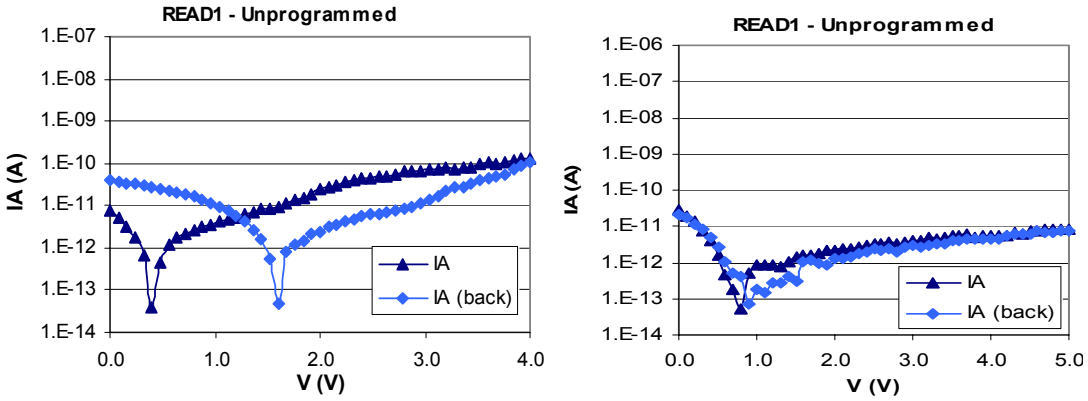

Figure 8.19: Read hysterisis through unprogrammed antifuses from the first generation (left) and third generation (right).

Conquering the delamination issues in the primary antifuse structure greatly enhanced performance levels across the 100-bit antifuse arrays. By decreasing leakage, margins were improved, and by decreasing hysteresis, smaller read voltages were enabled. Both of these consequences are crucial for creating low-power organic RFID tags.

8.3 The Complementary Structure (Invert)

At this point, a reinforcing of the memory goals is useful. A single layer of interconnected organic antifuses has been demonstrated on plastic, and operates exceedingly well. The process used to construct the device is also compatible with the low-cost reel-to-reel printing

processes of Chapter 2 (assuming aluminum contacts are replaced by silver nanoparticles). However, due to the limitations in the precision of printing technologies, creating dense memories requires a three-dimensional approach. This was one of the reasons for basing the memory on silicon antifuses, and why so much effort was placed into making stackable addressing circuitry.

While discrete and individually passivated layers of organic antifuses could be created using the technology developed thus far in this chapter, it is not the most elegant solution. To construct the stacked antifuses like those of Chapter 6 and Figure 8.20 that incorporate shared wordlines and bitlines, a secondary organic antifuse structure is needed. Currently, the primary organic antifuse device serves the function of the bottom device in Figure 8.20. To achieve high memory devices with these organic devices in an elegant and functional fashion, a device with a downward pointing diode is needed.

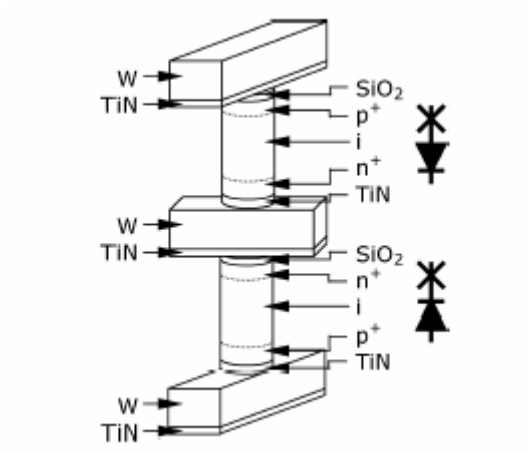

Figure 8.20: Two-layer silicon antifuse with intersecting wordlines and bitlines [88].

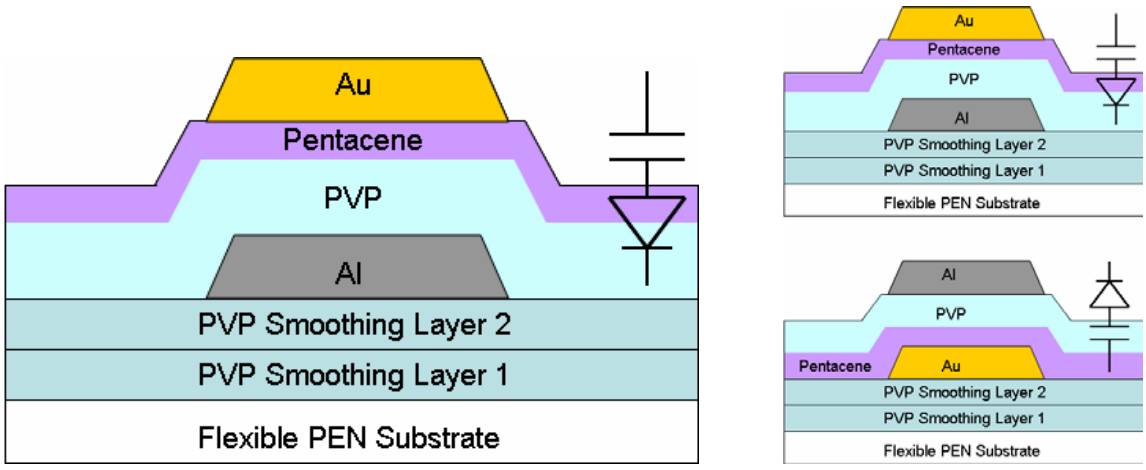

Figure 8.21: Inverted antifuse structure (left) and the combined 'primary' and 'invert' structures capable of producing memory arrays with shared wordlines and bitlines (right).

This 'inverted' structure is shown in the left of Figure 8.21, and has all of the same processing steps of the primary organic antifuse structure. Like the primary structure, multiple generations of devices were produced to optimize the performance, yield, and reliability. However, adhesion problems were not encountered, since the pentacene layer was deposited after the PVP dielectric layer.

The smoothing layers were first applied to the PEN substrate using the same multi-step spin, tape, and anneal methods described earlier. 1400Å of aluminum was then evaporated through the first shaddowmask to form the bottom electrode. PVP was then deposited through spin-casting from solution. A 1% by wt. spin and 100ºC cure was followed by a subsequent 2% by wt. spin and cure. Next, pentacene was thermally evaporated at 4Å/sec to a thickness between 3000Å and 3300Å. Finally, gold was evaporated through the shaddowmask to a thickness of 1500Å to form the top contact.

A distinct benefit of the inverted structure is that the PVP layer is deposited prior to the pentacene layer. By avoiding the known roughness of pentacene, the dielectric is expected to form a more uniform film across the wafer, and local thickness minima variations can be reduced. As a result, high device yields (>80%) were obtained on the first device demonstrations of this architecture. Because of this, large numbers of devices were tested, so that trends could be more easily identified.

A typical 'invert' antifuse device is characterized in Figure 8.22. The device shows high margins ($>10^5$) and excellent diode rectification at the read and preset write voltages. Another important characteristic is that these devices demonstrate a sharp and distinct breakdown event in the programming sweep cycle. The use of a 6V read sweep increased the read margin achieved. Also, compared to the primary structure antifuses, the diodes provided significantly better rectification at the read and write voltages, which enables larger memory array sizes.

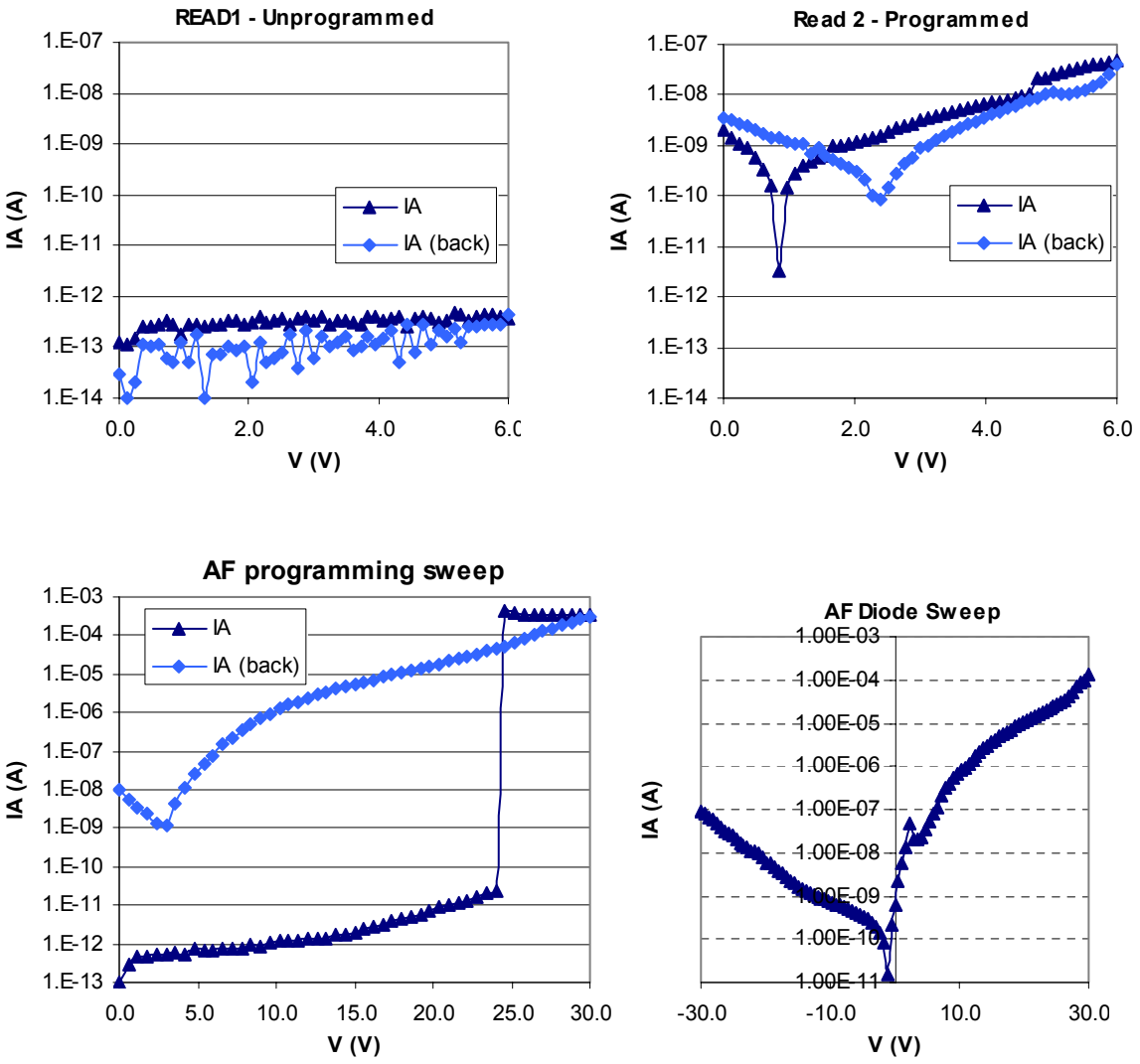

Figure 8.22: Electrical characterization of invert device. Initial read sweep (top left), Programming sweep (bottom left), Second read sweep (top right), and diode sweep of programmed bit (bottom right).

8.3.1.1 Advanced Electrical Characterization of the Invert Device Structure

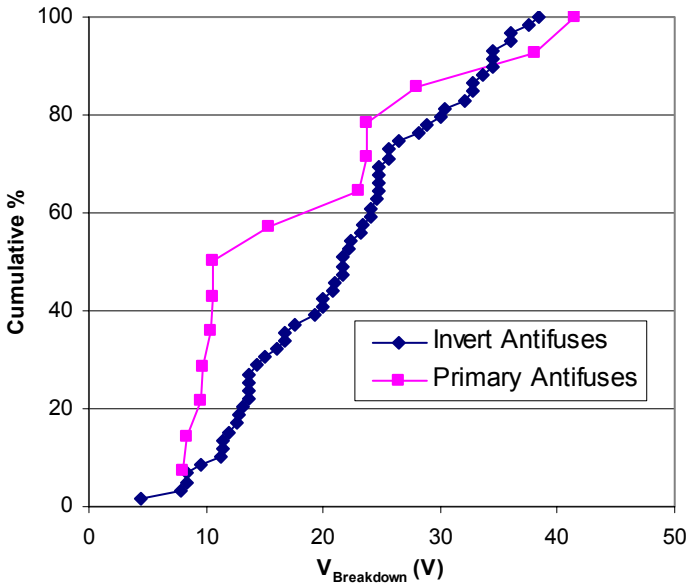

Figure 8.23: Cumulative distribution of breakdown in invert and primary structures.

The cumulative distribution of the breakdown of invert structure devices is shown in Figure 8.23. The invert structure produced a similar variation to breakdown voltage as the primary antifuse devices. However, the spread in breakdown voltage observed cannot be attributed to broad thickness variation, as it could for the primary devices. As seen in Figure 8.24, current through the unprogrammed bits is not directly related to the breakdown voltage, as it was in Figure 8.17. This uniform current indicates that film thickness is likely to be homogeneous, as tunneling current is suspected to be the primary leakage method, which has an exponential dependence on thickness. Instead, weaknesses in the dielectric due to polymer defects are likely to be the largest determining factor for breakdown voltage. It is suspected that these defects do not play a major role in Poole-Frenkel tunneling current, or that these defects are sparse enough to not contribute significantly to leakage current. However, for an antifuse

device, it only takes a single weak point in the dielectric to facilitate breakdown at low biases. Thus, since the leakage through the dielectric is uniform with breakdown voltage, it is concluded that these defect centers are few in number, but play a significant role in breakdown variation.

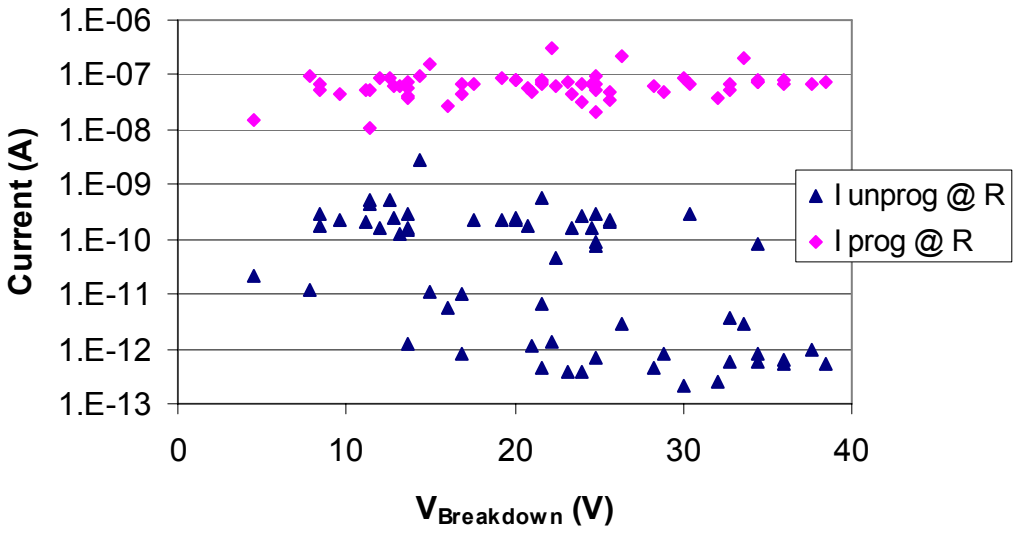

Figure 8.24: Current through programmed and unprogrammed bits as a function of bit breakdown voltage.

Another important conclusion can be drawn from Figure 8.24. The current of programmed devices also does not vary significantly with breakdown voltage. If the power consumed by the device just prior to the programming event is tracked, as in Figure 8.25, it can be seen that bits with higher breakdown voltages also require more power to program. While increased power loads generally produce lower resistance filaments, the lack of a result in the programmed bit current of Figure 8.24 means that even low-power filament formation is sufficient to prevent the filament from being the current-limiting element. This is a beneficial result, as the uniformity of current through programmed bits impacts the complexity of

addressing design. Combined with the uniformity of unprogrammed bits, identification of a bits programming state becomes simple.

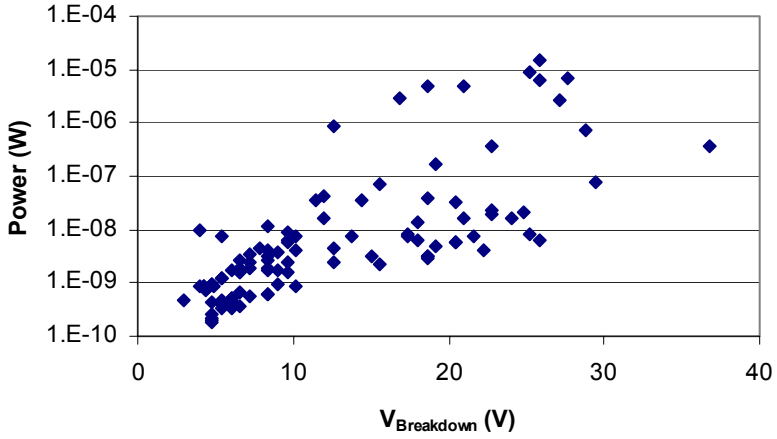

Figure 8.25: Programming power versus breakdown voltage for inverted antifuses.

The tight distribution of programmed bits and the broad distribution of unprogrammed bits can be better visualized in Figure 8.26. A distinct window of current exists between the antifuse states at the read voltage. This enables the rapid sensing of bit state within the memory array. The low leakage currents also produce extremely high margins, as seen in Figure 8.27. While 98% of the devices demonstrated margins greater than 100, roughly half of the devices have margins greater than 70,000. This is especially important, as production-level silicon-based antifuses only demonstrate margins of 10,000 [89]. In fact, others only demonstrate margins of 1000 [90]. With a record margin of 10,500,000 demonstrated in-house, it is apparent that organic antifuses drastically surpass the performance of its inorganic counterparts in this metric.

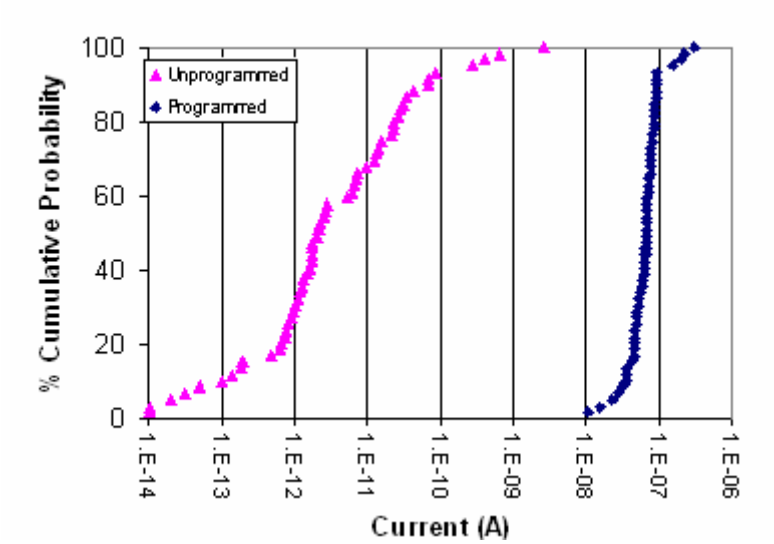

Figure 8.26: Cumulative distribution of currents through programmed and unprogrammed bits in invert antifuses.

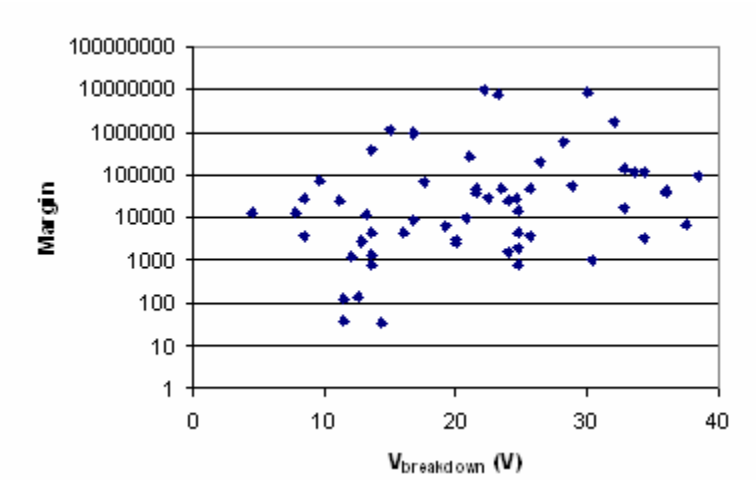

Figure 8.27: Margin vs. breakdown voltage for invert antifuse devices, illustrating margins greater than 10,000,000

Rectification at the read voltage is also important because significant reverse leakage could result in false-positive readings of unprogrammed bits. In a current path exactly the same as the disturb issue presented in Chapter 6, a series of programmed bits could cause significant flow between the specific wordline and bitline of the interrogated bit. As in the disturb issue,

the auxillary current path would consist of two forward-biased diodes and one reverse-biased diode. It is the duty of the reverse-biased diode to prevent current flow through this parasitic path so that the true nature of the target bit can be identified.

The consistency of the diodes in the invert devices, illustrated by the programmed current in Figure 8.26, is a major accomplishment. Combined with low reverse-bias currents, excellent diode rectification is achieved. Distributions of forward and reverse biased currents are shown at the read voltage (Figure 8.28) and the preset write voltage (Figure 8.29). Although the diodes do not show the performance of the primary devices, the achieved 10X rectification at the read voltage is acceptable. It is likely diodes behave better in the primary devices since the pentacene is allowed to order directly on the gold surface, of which it has an affinity. Also, Figure 8.30 shows that a rectification of at least 8 is maintained throughout for individual devices. Moreover, many devices of this generation demonstrate rectification well over 100X at the preset write voltage. These diodes also exhibit ideality factors between 15 and 25, which is reasonable for lowly doped organic diodes.

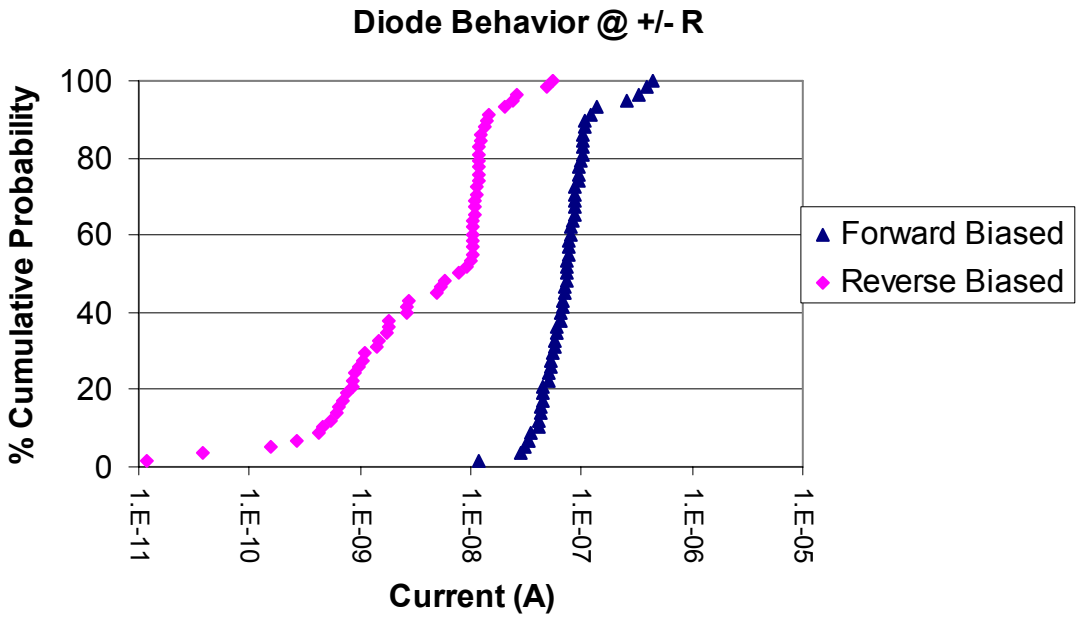

Figure 8.28: Current through programmed bits under forward and reverse bias at the read voltage (6V).

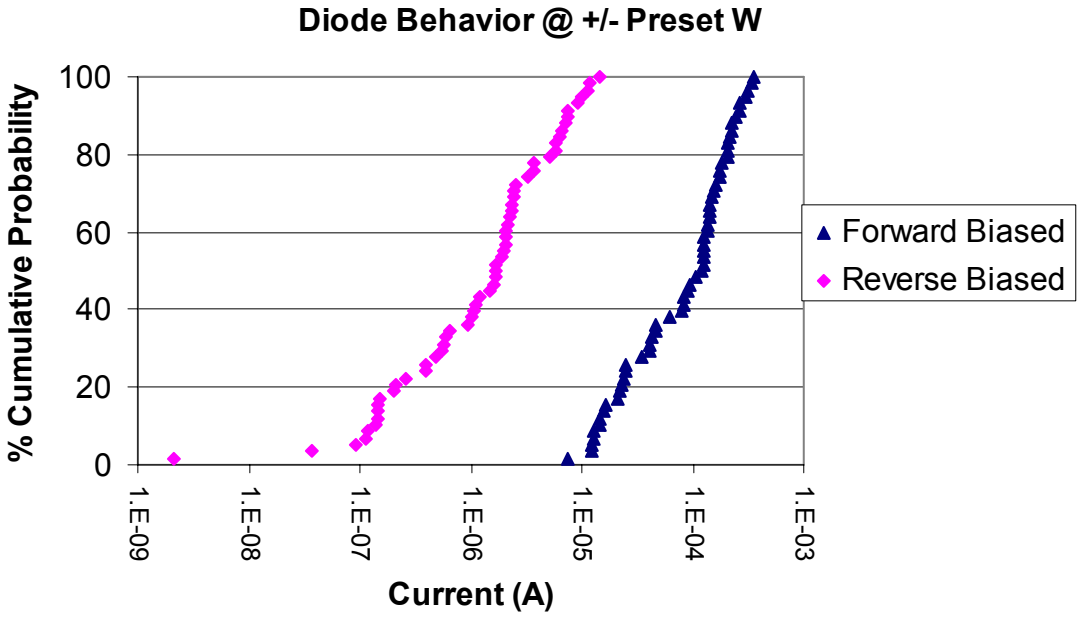

Figure 8.29: Diode rectification of invert antifuses at the 'preset write' voltage (30V).

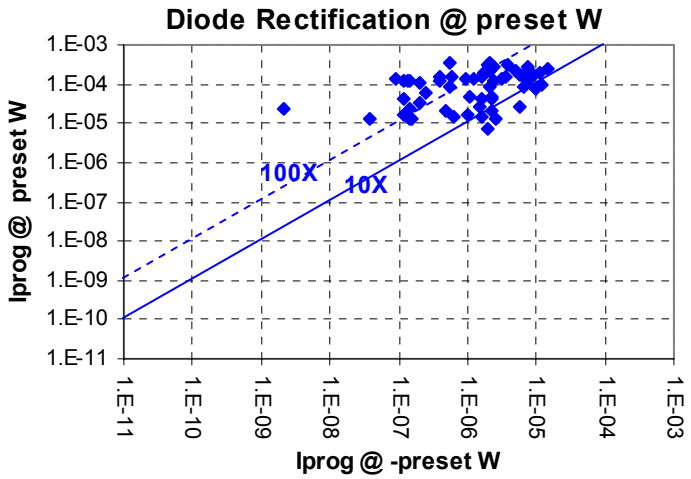

Figure 8.30: Diode rectification of invert devices at the read voltage.

8.3.2 Invert Development

The performance of the invert devices increased with each generation. For this work, tuning of the dielectric layer and the pentacene evaporation were the largest factors for change. The second PVP dielectric layer used during fabrication did effectively boost the lowest breakdown voltage to 7V, enabling a read voltage of 6V.

Initially a single 3% by wt. PVP spin provided the antifuse dielectric, and approximately 25% of the bits demonstrated breakdown at or below 6V. To prevent programming during the bit read, a thickness adjustment to the dielectric was needed to achieve yields > 90%. It was predicted that a two-layer spin could reduce breakdown variation by reducing the effect of pinholes or defect-ridden areas. This is a reasonable prediction, as the second spinning layer can help to fill-in gaps in surface coverage of the first layer. A 1% by wt. solution was spin-cast and annealed at 100ºC as before a second PVP layer was added (2% by wt.) to thicken the dielectric.

The cumulative distribution achieved improved significantly from generation to generation. As seen in Figure 8.31, the second and third generations that utilized the two-step spin showed higher breakdown voltages. 99% of the devices of the third generation also undergo breakdown after 6V, enabling higher read voltages and high yield. Also, the two-step spin enabled 100% of the devices to be programmed below 50V. Even though the distribution is not as steep as the first generation, the higher read voltage enables far higher margins, and is an acceptable trade-off.

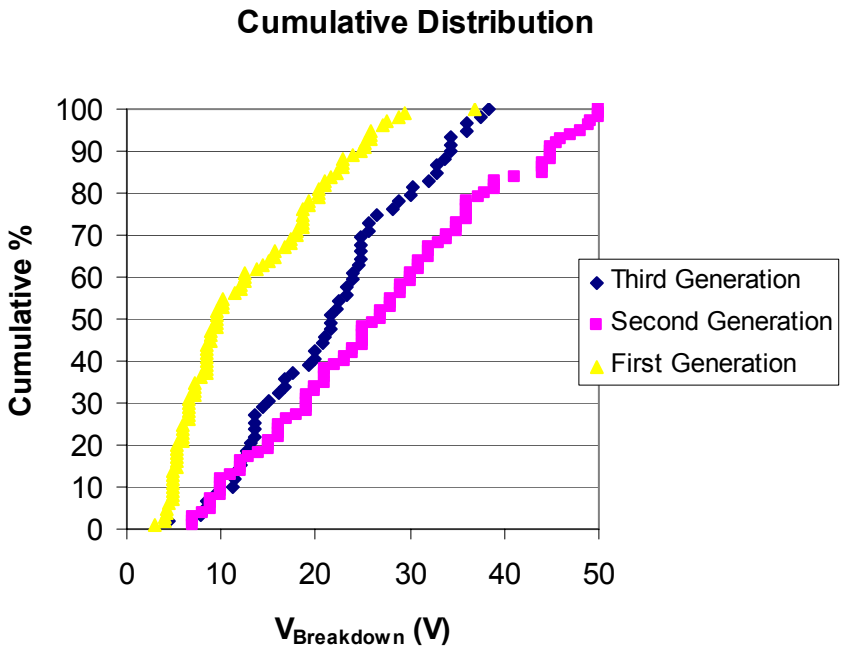

Figure 8.31: Cumulative distributions of the three invert structure generations.

Despite the great lengths taken to firmly tape and re-tape each sample to vacuum hotplates during the two-layer smoothing process, some warping of the PEN occurs. It was hypothesized that this warping caused the local pooling of the PVP used as the dielectric, causing breakdown variation. Also, since the antifuse device is built directly on top of an

evaporated aluminum electrode, it is questionable how much of a role the PEN roughness actually plays on the device. Instead, aluminum roughness may be the leading cause to variation, and would support the idea that breakdown is dominated by small discrete thickness minima (since leakage current is independent of breakdown voltage).

The distributions for the programmed and unprogrammed devices of the invert structure are shown in Figure 8.32. The reduced off-current due to the change to a two-step spin in the second and third generation devices is demonstrated. Between the first and second generation antifuses, the evaporation rate for pentacene was modified from 2.5Å/sec to 4Å/sec, while the thickness was kept constant. Surprisingly, the faster evaporation showed an increase in on-current. Generally, the slower the evaporation, the more time the molecules are given to align, decreasing diode series resistance. However, the trend of reduced resistance with increased evaporation rate is confirmed in the third generation. This trend is consistent across the entire voltage sweep of the devices, as seen at the read voltage in Figure 8.33 and at the preset write voltage in Figure 8.34.

The increased rate also decreased the leakage through the reverse-biased diodes at the read current. This is particularly important, so that an unprogrammed bit does not read as a programmed bit due to leakage currents through groups of programmed bits in the array. The results were far more mixed at the preset write voltage, but this is largely due to the first generation using a lower preset write voltage due to the breakdown distribution mentioned earlier. This can be seen more clearly with the diode examples from each of the generations in Figure 8.35. The reverse leakage is dramatically decreased at low voltages, but eventually reaches a similar level at high reverse biases.

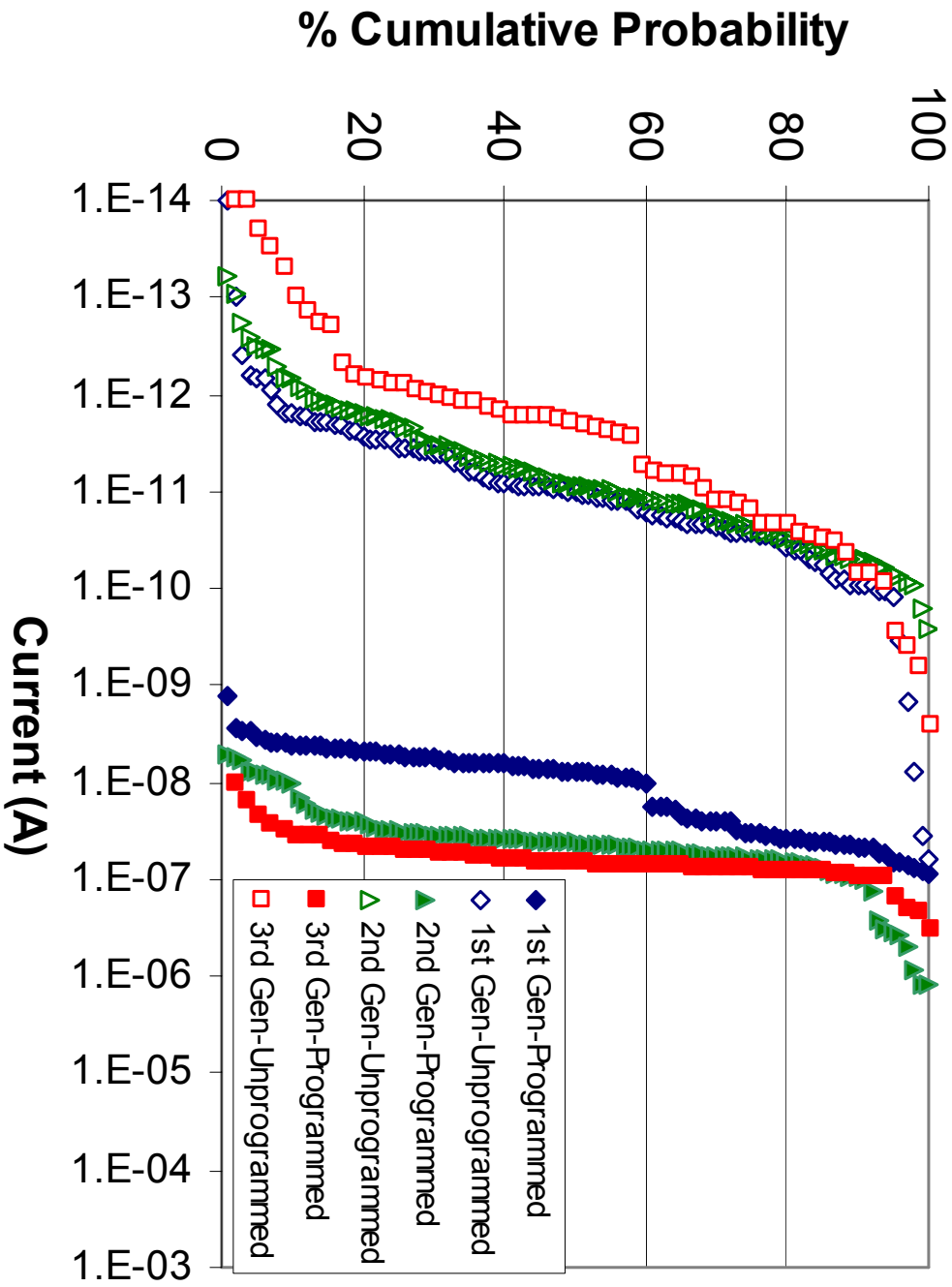

Figure 8.32: Programmed and Unprogrammed bit current distributions across three generations.

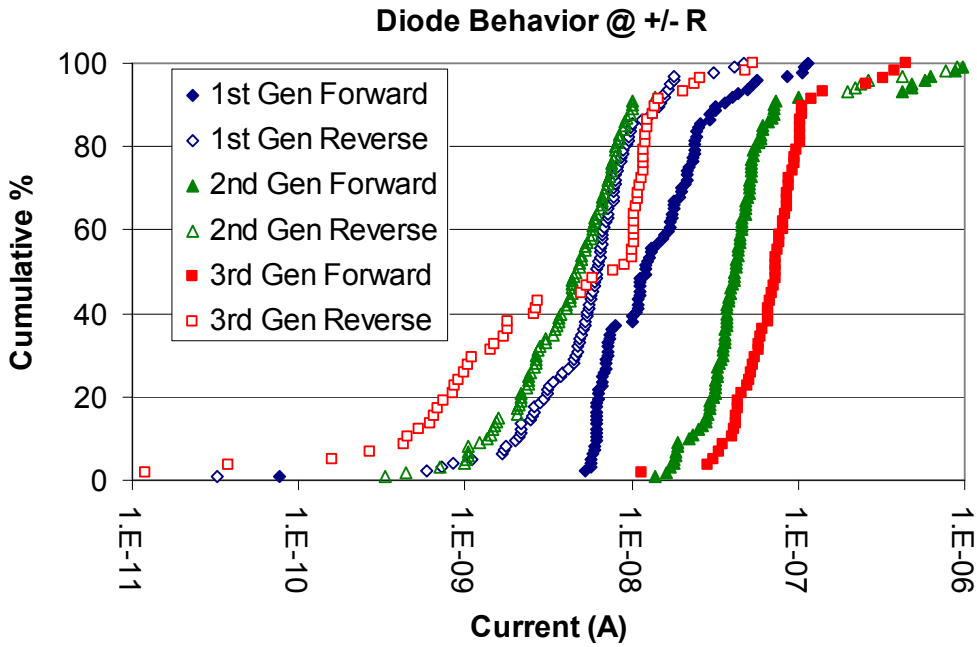

Figure 8.33: Diode rectification of programmed bits at the read voltage for several device generations.

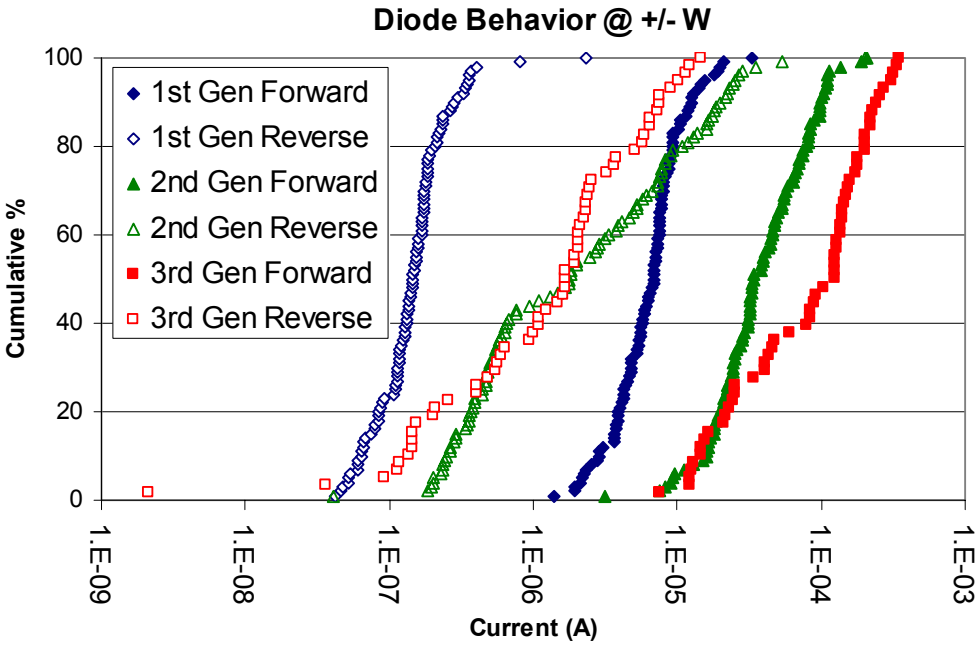

Figure 8.34: Diode rectification of programmed bits at the preset write voltage for several device generations.

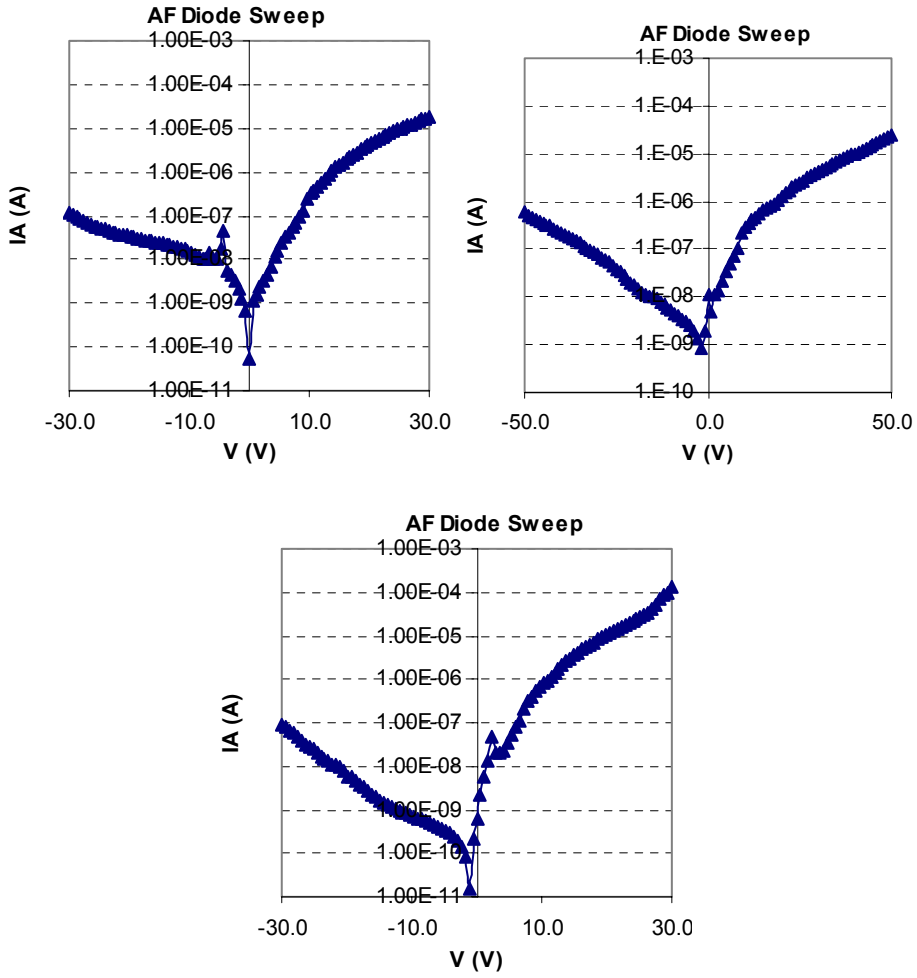

Figure 8.35: Example diodes for the first (top left) second (top right) and third (bottom) generation invert antifuse devices.

For the invert structure, over 300 devices were tested, which gave statistically significant information on various trends. The performance modifications between generations can be seen in Table 2. Both average margin and median significantly improved as the generations progressed. More importantly, diodes showed vastly improved rectification at the read and preset write voltage, enabling error-free operation in larger arrays without worries of disturb errors or false reads. The extremely high yield (>90%) demonstrated for second and third generation devices is also crucial for making functional memory arrays.

Invert Antifuses	1st Generation	2nd Generation	3rd Generation
Average Margin	8184	66,458	569,300
Median Margin	904	5367	24,000
Diode Rectification @ R	2.53	14.0	45.3
Diode Rect @ preset W	61.2	34.6	362
Average I unprog @ R	6.6×10^{-10}	2×10^{-11}	7.7×10^{-11}
Average I prog @ R	2.0×10^{-8}	9.1×10^{-8}	7.3×10^{-8}

Table 2: Performance summary for the invert antifuse structure.

8.4 Complementary Structure Conclusions

100-bit Organic Antifuse Arrays on Plastic	Bottom antifuse 	Top antifuse 
Average Margin	569,300	8100
Median Margin	24,000	1760
Diode Rectification @ R	45.3	1963
Diode Rectification @ W	362	12846
Average I_{unprog} @ R	7.7×10^{-11} A	3.0×10^{-9} A
Average I_{prog} @ R	7.3×10^{-8} A	7.1×10^{-7} A
Yield	>90%	>80%
Devices Tested	>350	>120

Table 3: Electrical characteristics of the complementary antifuse structures.

Complementary antifuse structures have been created and analyzed, with the performance metrics listed in Table 3. By implementing these antifuse arrays on flexible substrates, this work realizes single layer memory arrays suitable for low-cost RFID applications. At this point, both structures have independently demonstrated acceptable performance levels, and help verify the feasibility of this technology as a memory solution. In the next phase of

development, we demonstrate vertically stacked memory arrays on plastic substrates for low-cost RFID.

8.5 Stacked Organic Antifuse Memory Arrays on Plastic

Antifuse memory arrays have been designed and fabricated on plastic substrates to create a viable memory technology for low-cost electronics. However, with the large minimum linewidths produced by current printing methods, memory density would generally be limited in reel-to-reel processing. However, this thought is based upon conventional silicon-based ideas. In most silicon and organic devices, device density in the third dimension isn't pursued. Organic antifuses, like their inorganic counterparts, work to challenge this idea, as the vertical stacking of devices can offer extreme increases in memory devices without the need to improve patterning technologies.

8.5.1 Stacked Antifuse Structure

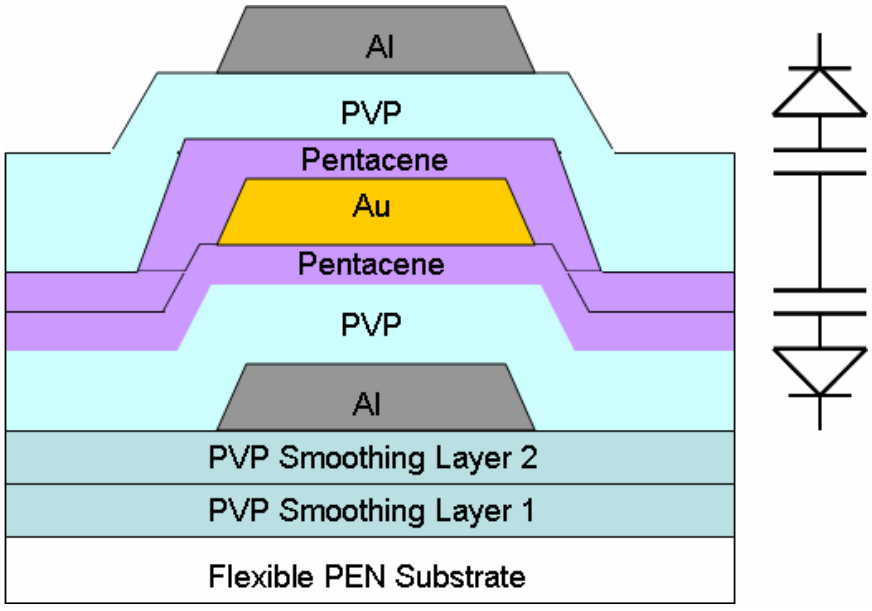

Figure 8.36: Stracked antifuse cross-section.

In this demonstration process, the 'invert' structure is fabricated first. Since contacting the first electrode layer requires mechanical scratching through two PVP layers and two pentacene layers, the shadow-masked bottom aluminum electrode was deposited much thicker (2900Å). Following this, a single 2% by wt. PVP dielectric was deposited, as in the first generation 'invert' devices. A thinner dielectric film was chosen since the cure of the second PVP layer would impart more heat upon the original PVP layer, increasing hardness and breakdown voltage. In a separate experiment, it was verified that the breakdown (programming) voltage of antifuses depended largely upon the amount of time in which the PVP film was cured. As shown in Figure 8.37, a 20 minute cure dramatically changes the breakdown characteristics versus a 5 minute cure. Since the bottom layer undergoes 15 minutes of curing at 100ºC during the fabrication, a single 2% PVP solution was chosen.

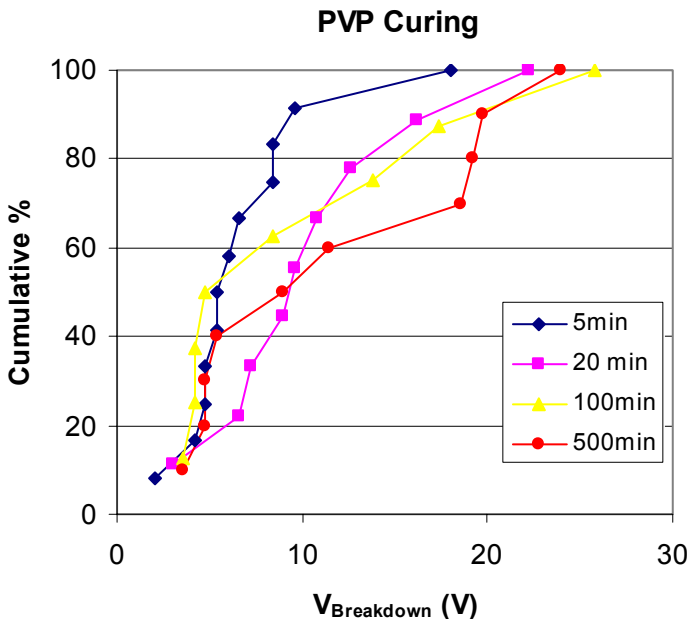

Figure 8.37: Length of PVP curing at 100ºC versus dielectric breakdown voltage in invert antifuses. Films were 1% PVP + 1% PVP, with the cure preformed after each layer.

Next, a 3300Å pentacene layer was deposited using the same rates as in Chapter 8. A 1500Å gold film was evaporated through a shadow-mask to form the intermediate contact. With the combined roughness of two pentacene layers and the gold layer, it was determined that a thicker PVP film should be deposited to form the upper dielectric. Two 2% by wt. PVP solutions were spun, with a 5 minute anneal after each layer. Finally, a 1600Å aluminum layer was shadow-masked to form the top schottky electrode.

8.5.2 Electrical Characteristics

The electrical characteristics of a typical top-level device are shown in Figure 8.38. As a whole, these devices demonstrated extremely high performance. The margin for this particular device is 85,000, and the lowest margin seen for the top-layer devices was 25,000. This is due to the rapid turn-on of the diodes, as well as the extremely low leakage through the dielectric. By examining the read sweeps, it can be seen that high margins for this device could be achieved at extremely low voltages (<2V), thus lessening the bias requirements of the system and providing a larger window to prevent accidental write events. Although the ideality factor of the diodes in these antifuses remains near 15, the rectification is vastly more important for these devices. In these diodes, rectifications of 1000 at the preset write voltages are common, which is a testament to the quality of the pentacene material and its deposition process. Also, the thicker two-layer PVP dielectric used for this layer seem to be appropriate, as the device breakdowns are within the range of the cumulative distribution of third-generation primary devices from Chapter 8.

Unlike all previous devices, no significant hysteresis can be seen in the read sweeps, which is likely due to low trap densities. This is important for device reliability, as the reading of other bits in a memory array cause voltages to be applied to common lines. This could cause traps

to be filled, introducing some read history effects into the output current of a specific bit. This low trap density could also be responsible for the excellent diode characteristics achieved.

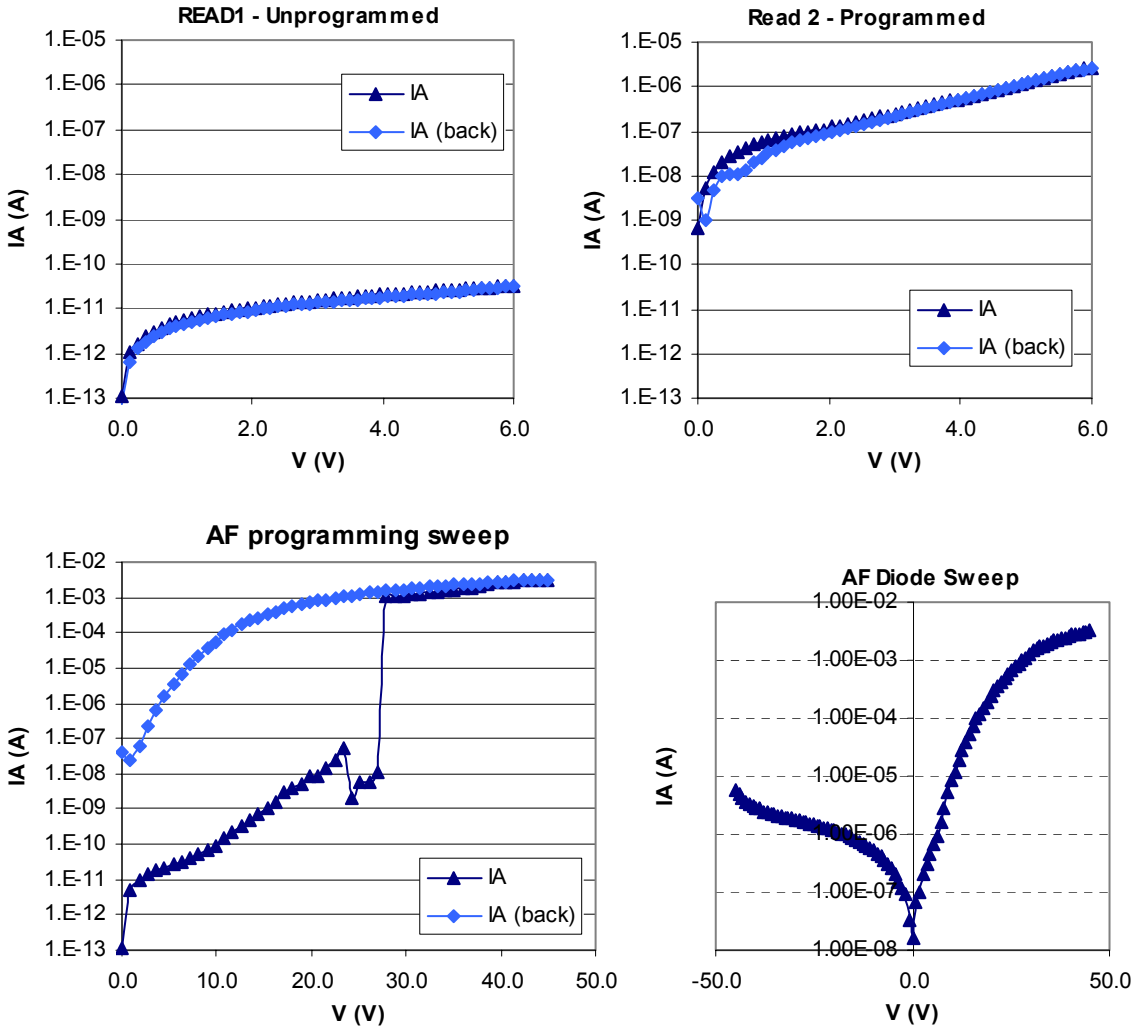

Figure 8.38: Top-layer electrical characteristics of a stacked antifuse.

The bottom-layer devices also showed high-quality electrical characteristics, with a typical device demonstrated in Figure 8.39. The devices used for this bottom layer were initially fabricated during the production of first generation invert arrays. Initially, the single 2% PVP dielectric would only demonstrate breakdown below 5V, and were not useful. However,

following the fabrication of the top layer, including the curing of the two-layer PVP dielectric, the bottom layer demonstrated much-increased resilience to breakdown. In these devices, breakdowns greater than 50V were common. Future versions will need to better take into account the impact of additional cures on dielectric breakdown, and thinner bottom-layer dielectrics will be needed. The mediocre diode rectification can be attributed to the poor quality of the pentacene, as these curves are similar to those of other first generation invert devices. However, all margins demonstrated where greater than 700, which is above the first generation invert average. Needless to say, these bottom-layer devices produce more than acceptable electrical behavior, and clearly demonstrate the functionality of stacked devices.

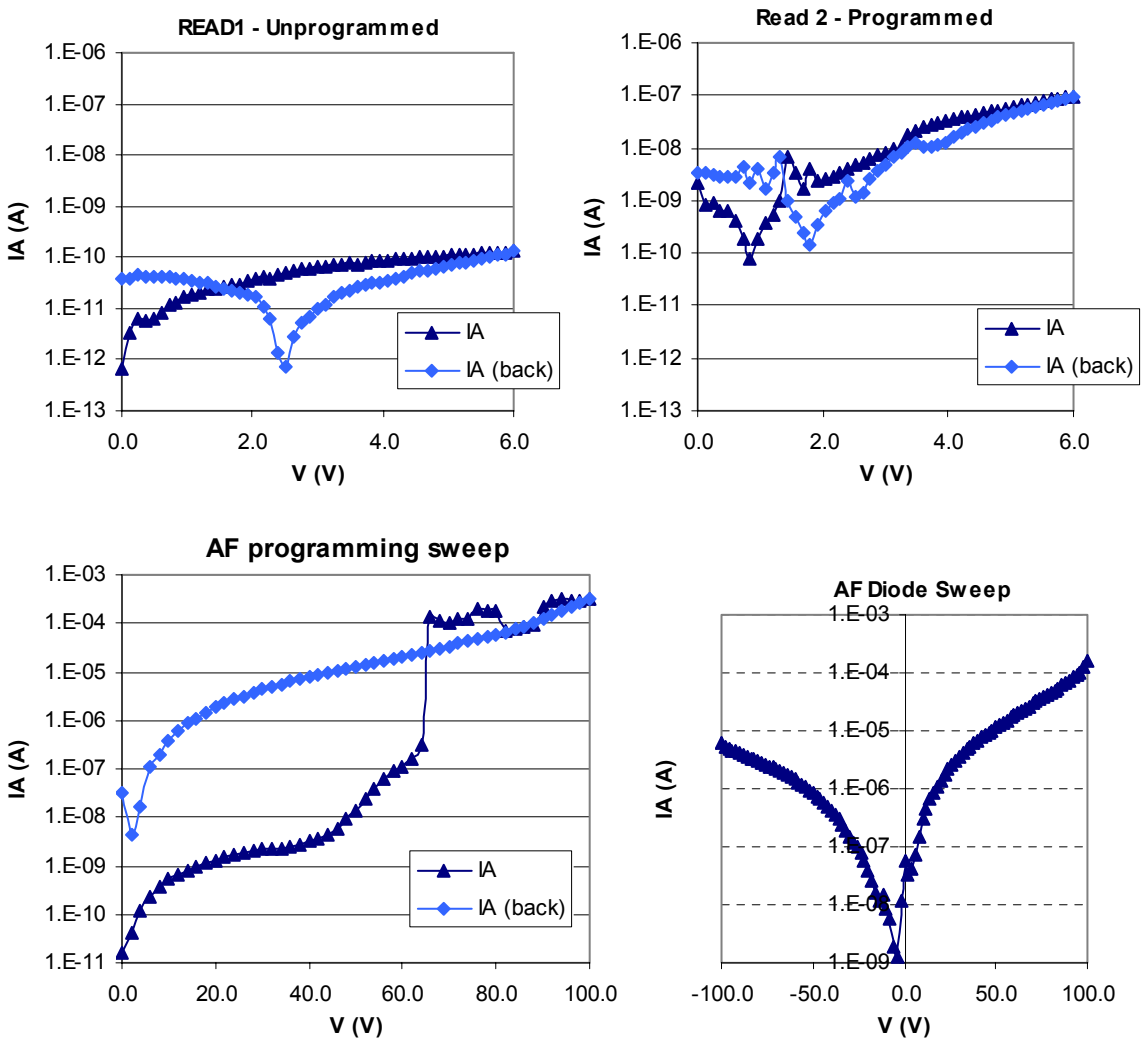

Figure 8.39: Bottom-layer electrical characteristics of a stacked antifuse.

8.6 High-speed Programming

Another important need for these devices is a fast write time. Obviously, if large amounts of time are needed to program a single bit, the transfer of data in a gigabit scale would take unacceptably long. For example, if each bit required a 1ms write pulse, the programming of a single layer 1Gb array would take over 16 minutes. Of course, incorporating vertical stacking enables different layers to be written simultaneously. Even so, a short bit programming time

would be beneficial in enabling rapid data transfer. Using an HP8011A pulse generator, organic antifuses were successfully programmed with a single 25ns pulse at 16V. As shown in Figure 8.40, more than 65% of the devices were successfully programmed with a 25ns pulse, and all devices were programmed with a 1μs pulse. This speed is already significantly faster than the programming pulses used by all inorganic antifuse systems, which can be as high as 100ms [91]. ONO MIM antifuses used in industry require programming times in excess of 200μsec at 18V [92]. Even state-of-the-art inorganic antifuse systems require 2μs programming times [88]. As a result, organic antifuses demonstrate yet another significant advantage over their inorganic counterparts.

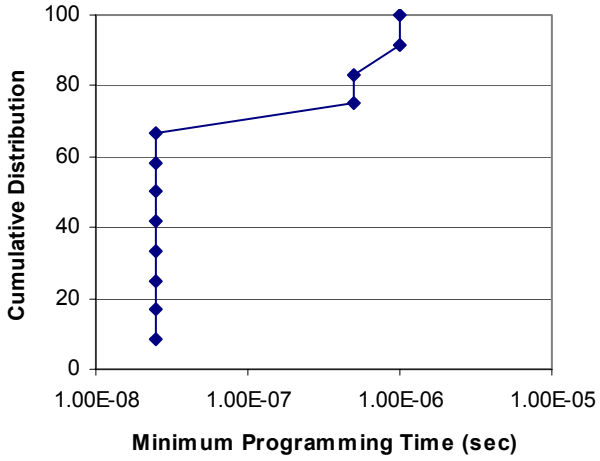

Figure 8.40: Programming pulse time required to program an antifuse bit.

From the programming time, we can establish the power and energy required to induce filament formation in the dielectric. By examining the pre-program current of bits breaking down at 16V, we find a power requirement of less than 1nW. Similarly, using the 25ns pulse, we calculate that the bits use less than 4×10^{-17} Joules, which is far below the energetic needs of

inorganic antifuses. As a result, organic antifuse memory arrays are well-suited for low-power applications, such as RFID.

8.7 Applications

As discussed in Chapter 2, low-cost RFID would greatly benefit from this technology. The capabilities of the organic antifuses fill a need technological need that has yet to be filled by any other technology. The addressed antifuse memory created here incorporates:

- High performance
- Low Power
- Reel-to-reel compatible materials
- The use of flexible plastic substrates
- Vertical stacking, enabling high density
- One-time Programmable

Because of this, an antifuse-based memory technology solves the RFID memory needs, and is a critical component in creating reel-to-reel ultra-low-cost RFID tags capable of being profitable in the item-level tagging arena.

Besides being an excellent fit in the RFID market space, many other avenues exist for the commercialization of organic antifuses. Another large potential market for this low-cost memory would be the integration of organic memory onto clothing. With the use of high-temperature flexible plastics, this technology could easily be built into cloth. Also, the thermal

budget of organic antifuses is well above the temperatures encountered during the laundering of apparel. Specific applications could include activewear with built-in mp3 players, with built-in pockets for the swapping of plastic antifuse memory cards. Or, if the technology were integrated with flexible OLED displays, organic antifuses could be used to store image files to be displayed on the display mounted on the shirt surface. Suddenly, shirts with a single graphic could be a thing of the past. This idea could be expanded to include commercial signage with no silicon components, and images stored on built-in organic antifuses. Both of these ideas are enabled by the extreme low-cost of the organic antifuse solution, as the realm of disposable memory is being approached.

The flexible nature of the organic antifuse is also a valuable attribute that cannot be achieved by its silicon counterparts. By combining with electrochromic displays [93][94], antifuse memories could be used to create electronic maps on paper or plastic substrates. Unlike GPS systems with expensive handheld devices, these reel-to-reel maps could be folded into a back pocket, and could be created at such low cost via the reel-to-reel fabrication that they could be entirely disposable. The antifuse array itself would be responsible for the map data, and could be integrated directly below the electrochromic display area, so that no net surface area would be consumed by them. This collaboration of technologies could also include low-power display systems for emerging countries, as well as reusable electronic newspapers [95].

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Chapter 9: CONCLUSIONS

Through the previous eight chapters, a technology suite has been developed to fulfill the memory needs of low-cost RFID. The background of organic electronics, printing technologies, and RFID was explored in Chapter 2 to create a foundation for the work investigated here. Within RFID, the memory array containing the identity of the individual tag is explored. This component is comprised of a transistor-driven addressing circuitry, and a discrete memory element. To enable a cost-effective solution for these critical RFID components and the eventual replacement of the UPC barcode, solution-deposited materials were investigated to enable low-cost printing fabrication.

In Chapters 3 and 4, performance enhancing methods and electrical isolation techniques were developed to create high-performance addressing transistors. Through the increase in mobility and on/off ratio associated with thermal cycling, P3HT was proven to obtain high performance despite a lack of purification processes. The on/off ratio and subthreshold swing were improved even further with isolation techniques using either e-beam or water-soluble PVA resists. By combining these methods with the stackable reel-to-reel transistor process flow generated in Chapter 5, high-performance addressing OTFTs for reel-to-reel memory arrays were produced.

In the second half of the work presented here, a novel reel-to-reel compatible memory technology was developed. Borrowing ideas from inorganic devices, organic antifuses were created to provide fill the memory needs of low-cost RFID. To our knowledge, this is the first

demonstration of organic antifuse memory elements. By integrating into a cross-array structure, nonvolatile 100-bit memory arrays were produced that showed the ability to overcome disturb-effect programming errors. Through the design of optimized complementary structures, vertically stacked antifuse memory arrays with shared wordlines and bitlines were developed to achieve high density. By also utilizing the low thermal budget of the process, plastic substrates were incorporated to bring the technology into the frame of reel-to-reel processing. Through speed measurements it was also determined that the organic antifuses could be programmed within 25ns, at power and energy levels far below those of their inorganic counterparts. Combined with their exceptional programming margins, the organic antifuses shown here demonstrate performances well above the needs of RFID memory elements, at a compatible cost point.

Through combining the organic addressing and antifuse technologies, the in-plane addressing of antifuse memories can be achieved, enabling potentially endless levels of vertical stacking. This robust design facilitates ultra-high density memory arrays without the need for costly high-precision patterning tools. In parallel, the low processing temperatures and use of solution-deposited materials enables low-cost plastic substrates and high-throughput printing technologies. The final result: a complete addressing and memory solution for creating dense, cheap, and low-power memories for low-cost RFID.

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