Digital Control of PWM Converters: Analysis and Application to Voltage Regulation Modules

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Technical Report No. UCB/EECS-2006-146
http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-146.html

November 13, 2006

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by

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B.A. (Harvard University, Cambridge) 1999

A dissertation submitted in partial satisfaction of the
requirements for the degree of
Master of Science

in

Engineering-Electrical Engineering and Computer Sciences

in the

GRADUATE DIVISION
of the
UNIVERSITY of CALIFORNIA at BERKELEY

Committee in charge:

Professor Seth R. Sanders, Chair
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Spring 2002

Abstract

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Digital controllers have become an attractive choice in switching voltage regulators for low-cost, high-performance applications such as microprocessor voltage regulation modules (VRM's) and portable electronics such as mobile phones and personal digital assistants (PDA's). This report discusses issues related to the use of digital control in pulse-width modulation (PWM) converters, with emphasis on VRM applications . The presence of steady-state limit cycles in digitally controlled PWM converters is analyzed, and conditions for their elimination are suggested. Digital dither is introduced as a means of increasing the effective resolution of digital PWM (DPWM) modules. VRM passive current sharing and transient response are discussed from the perspective of digital control. A VRM sensing scheme using a single low-resolution window analog-to-digital converter (ADC) is proposed. The above discussions are illustrated with simulations and experimental results.

Approval for the Report and Comprehensive Examination:

Committee:

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Research Advisor

Date

* * * * * *

Professor Jan M. Rabaey

Second Reader

Date

In memory of my grandparents, Bistra and Andrey,

To my mother Antonina,

To my engineering mentors Prof. Seth Sanders and Mr. Winfield Hill.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Overview

Digital controllers are currently attracting increased attention in the field of pulse-width modulation (PWM) power converters for applications such as microprocessor voltage regulation modules (VRM's) and portable consumer electronics (mobile phones, personal digital assistants, *etc.*). The rapid increase of the computational power and speed of digital circuits, accompanied by a reduction of their cost, has made digital controllers eligible for these low-cost, high-performance applications, which are presently still dominated by analog solutions. Digital circuits offer low quiescent power, immunity to analog component variations, ease of integration with other digital systems, ability to implement sophisticated control schemes, and potentially faster design process, considering the availability of advanced CAD tools for high level digital design. In particular, the ability of digital controllers to accurately match multiple pulse-width modulation (PWM) signals, may allow for the use of passive current sharing schemes in multi-phase VRM's, thus reducing the units' cost and complexity. Further, the ease of

interface between a digital controller and other digital hardware can be advantageous in microprocessor and communication systems. In addition, the low power dissipation of digital controllers makes them an attractive choice for portable applications. Finally, digital controllers can implement complex control techniques such as on-line power optimization or spread-spectrum switching, which would present a substantial challenge to conventional analog controllers.

In this work we discuss issues related to the use of digital controllers in PWM converters, with particular emphasis on their application in microprocessor VRM's. The Introduction gives an overview of the structure of digital PWM controllers. Chapter 2 describes limit cycles in digitally controlled PWM converters and presents conditions for their elimination. Chapter 3 introduces digital dither as a technique that effectively increases the resolution of digital PWM (DPWM) modules, allowing for the use of low resolution DPWM modules in applications requiring high regulation accuracy, such as VRM's. The use of low resolution DPWM modules in these applications, without incurring limit cycles, can result in substantial power and silicon area savings. In the following chapters we analyze digitally controlled VRM's, and discuss architecture aspects of an integrated circuit (IC) controller implementation. In Chapter 4 we analyze passive current sharing in multi-phase VRM's, and derive estimates for the possible phase current mismatch due to power train parameter variations. In Chapter 5 we discuss the VRM transient response with non-zero controller delay, and introduce an implementation of optimal voltage positioning with a digital controller. In Chapter 6 we propose a low resolution analog-to-digital converter (ADC) window topology that can be used in VRM's. Chapter 7 presents results from a prototype VRM, demonstrating some of the issues discussed in the other chapters.

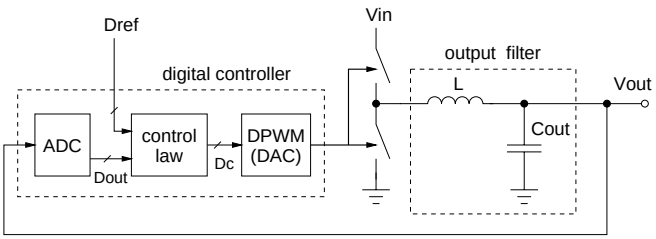


Figure 1.1: Block diagram of a digitally controlled PWM converter.

1.2 Digital Controller Structure

A block diagram of a digitally controlled PWM buck converter is shown in Fig. 1.1. Controllers with similar structure have been discussed in a number of publications (*e.g.* [1], [2], [3], [4], [5], [6]). The controller consists of an ADC which digitizes the regulated quantity (*e.g.* the output voltage V_{out}), a DPWM module, and a discrete-time control law. A discrete-time proportional-integral-derivative (PID) control law has the form

$$\begin{aligned} D_c(k+1) = -K_p D_e(k) - K_d[D_e(k) - D_e(k-1)] - \\ - K_i D_i(k) + D_{ref}(k) \end{aligned} \tag{1.1}$$

where $D_c(k)$ is the duty cycle command at discrete time k, $D_e(k)$ is the error signal

$$D_e(k) = D_{out}(k) - D_{ref}(k), \tag{1.2}$$

and $D_i(k)$ is the state of an integrator

$$D_i(k+1) = D_i(k) + D_e(k). \tag{1.3}$$

Further, K_p is the proportional gain, K_d is the derivative gain, and K_i is the integral gain. Variable $D_{ref}(k)$ represents the reference voltage, and $D_{out}(k)$ is the digital representation of V_{out}. All variables are normalized to the input voltage, V_{in}. Variable D_{ref} is used as a feedforward term in (1.1). Note that

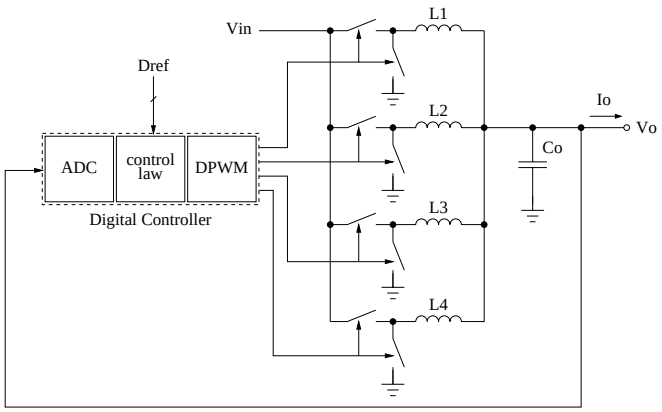


Figure 1.2: Block diagram of a digitally controlled multi-phase VRM.

D_{ref} by itself would give the correct duty cycle command for steady state operation with constant load, if there were no load-dependent voltage drop along the power train and no other non-idealities in the output stage [2].

Microprocessor VRM's commonly use a multi-phase buck converter topology to deliver large load currents at reduced input current ripple and output voltage ripple. A block diagram of a digitally controlled 4-phase buck VRM is shown in Fig. 1.2. The converter operation here is the same as that of the single phase converter in Fig. 1.1, with the difference that the DPWM module generates gating signals for the power train switches which are $360^{\circ}/4 = 90^{\circ}$ phase shifted with respect to each other.

Chapter 2

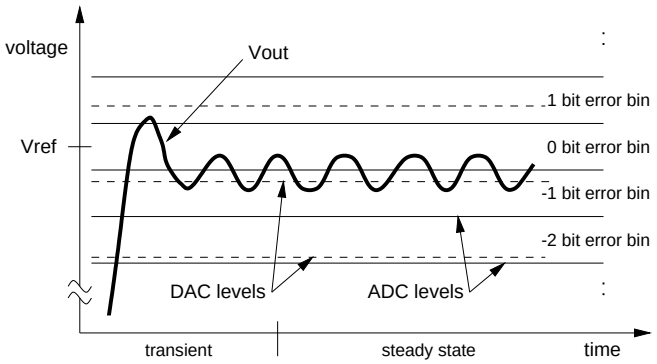
Quantization and Limit Cycles

2.1 Limit Cycles

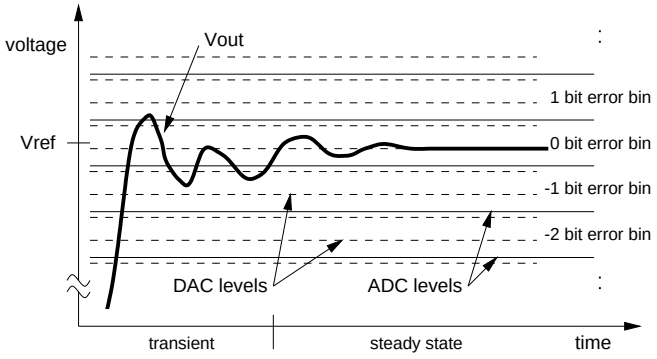
For the converter of Fig. 1.1, limit cycles refer to steady-state oscillations of V_{out} and other system variables at frequencies lower than the converter switching frequency f_{sw}. Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. Steady-state limit cycling may be undesirable if it leads to large amplitude (or unpredicted) output voltage variation. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the resulting V_{out} noise and the electro-magnetic interference (EMI) produced by the converter.

Let us consider a system with ADC resolution of N_{adc} bits and DPWM resolution of N_{dpwm} bits. For a buck converter, this will correspond to voltage quantization of $\Delta V_{adc} = V_{in}/2^{N_{adc}}$ steps for the ADC, and $\Delta V_{dpwm} = V_{in}/2^{N_{dpwm}}$ for the DPWM. Fig. 2.1(a)[1] illustrates qualitatively the behavior

[1] In all simulations the data is sampled at the switching frequency, therefore the switching ripple on V_{out} cannot be seen. For the discussions in this paper the switching ripple is not of interest and its omission makes the plots clearer.



(a)



(b)

Figure 2.1: Qualitative behavior of V_{out} with (a) DPWM resolution lower than the ADC resolution, and (b) DPWM resolution two times the ADC resolution and with integral term included in control law.

of V_{out} in steady state when the DPWM resolution is less than the ADC resolution, and there is no DPWM level that maps into the ADC bin corresponding to the reference voltage V_{ref} (this ADC bin will be referred to as the *zero-error bin*). In steady state, the controller will be attempting to drive V_{out} to the zero-error bin, however due to the lack of a DPWM level there, it will alternate between the DPWM levels around the zero-error bin. This results in non-equilibrium behavior, such as steady-state limit cycling.

2.2 Conditions for elimination of limit cycles

Here we develop a set of sufficient conditions ensuring that the PWM converter does not exhibit limit cycling in steady state. The first step towards eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC. A one-bit difference in the resolutions, $N_{dpwm} = N_{adc} + 1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level.

No Limit Cycle Condition # 1

$$\boldsymbol{resolution(DPWM) > resolution(ADC)} \tag{2.1}$$

Yet, even if the above condition is met, limit cycling may still occur if the feedforward term is not perfect and the control law has no integral term ($K_i = 0$). In this case, the controller relies on non-zero error signal D_e to drive V_{out} towards the zero-error bin. However, once V_{out} is in the zero-error bin, the error signal becomes zero, and V_{out} droops back below the zero-error bin. This sequence repeats over and over again, resulting in steady-state limit cycling. This problem can be solved by the inclusion of an integral term in the control law. After a transient, the integrator will gradually converge to a value that drives V_{out} into the zero-error bin, where it will remain as long as $D_e = 0$, since a digital integrator is perfect (Fig. 2.1(b)) .

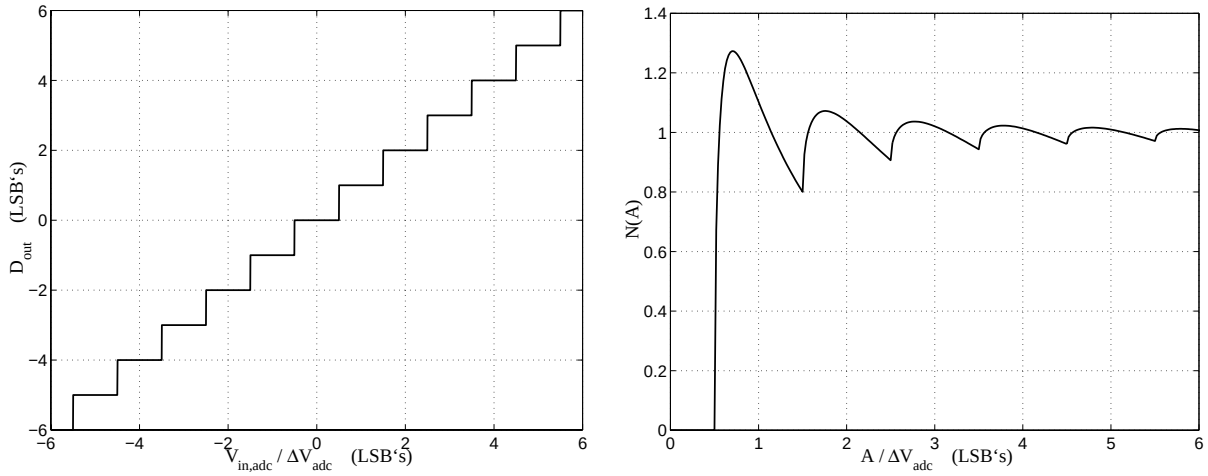
No Limit Cycle Condition # 2

$$\boldsymbol{0 < K_i \leq 1} \tag{2.2}$$

An upper bound of unity is imposed on the integral gain, since the digital integrator is intended to fine-tune the output voltage, therefore it has to be able to adjust the duty cycle command by steps as small as

a least significant bit (LSB).

The two conditions suggested above are not sufficient for the elimination of steady-state limit cycles, since the non-linearity of the quantizers in the feedback loop may still cause limit cycling for high loop gains. Non-linear system analysis tools, such as describing functions ([7, 8, 3]), can be used to determine the maximum allowable loop gain not inducing limit cycles. The feedback loop of the converter includes two quantizers—the ADC and the DPWM—however in the present analysis we will consider only the ADC non-linearity, since it performs coarser quantization if the DPWM resolution is made higher than that of the ADC (as recommended above). The describing function of an ADC (a round-off quantizier) represents its effective gain as a function of the input signal AC amplitude and DC bias. When the control law contains an integral term, only limit cycles that have zero DC component can be stable, because the integrator drives the DC component of the error signal to the zero-error bin. Since in steady state the DC bias is driven to zero, and since the loop transmission, $L(j\omega)$, from the output of the ADC to its input has a low-pass characteristic, the sinusoidal-input describing function of a round-off quantizer can be used to analyze the stability of the system. The characteristic of a round-off quantizer is plotted in Fig. 2.2(a), where $V_{in,adc}$ is the ADC input voltage, ΔV_{adc} is the ADC quantization bin size corresponding to one LSB, and D_{out} is the quantized representation of $V_{in,adc}$. The corresponding describing function, $N(A)$, is plotted in Fig. 2.2(b), where A is the AC amplitude of $V_{in,adc}$. From the plot it can be seen that the describing function has a maximum value of about 1.3, corresponding to maximum effective ADC gain. The control law (1.1), and hence $L(j\omega)$, can then be designed to exclude



(a) (b)

Figure 2.2: Characteristic of a round-off quantizer (a) and the corresponding describing function for sinusoidal signals with zero DC bias (b).

limit cycles by ensuring that

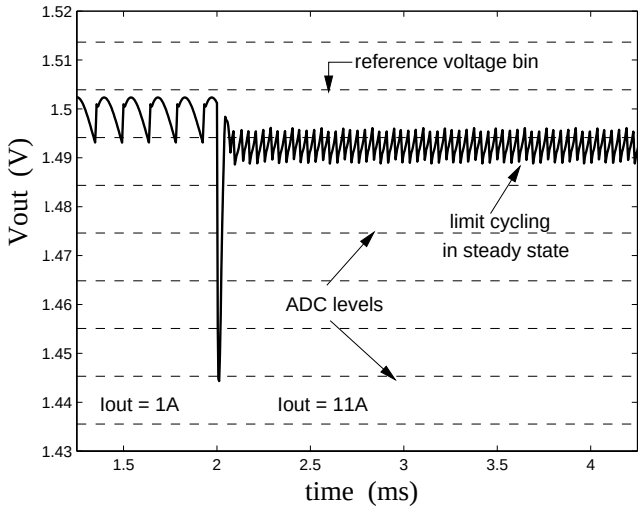
No Limit Cycle Condition # 3

$$\mathbf{1} + \boldsymbol{N}(\boldsymbol{A})\boldsymbol{L}(\boldsymbol{j\omega}) \neq \mathbf{0} \tag{2.3}$$

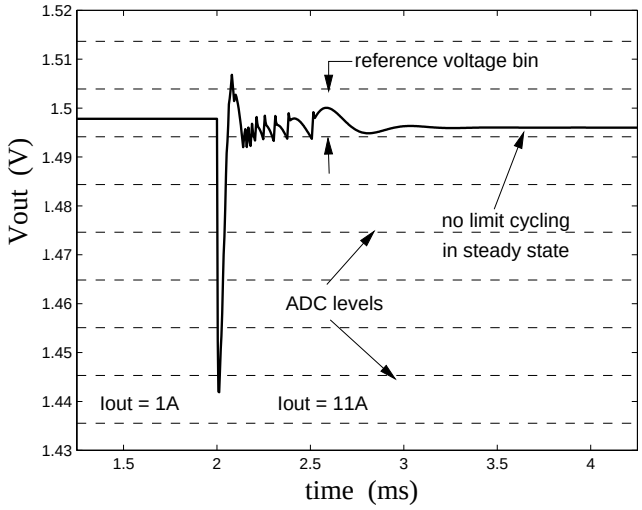
(Nyquist Criterion)

holds for all non-zero finite signal amplitudes A and frequencies ω.

Fig. 2.3(a) shows a simulation of the transient response of a digitally controlled PWM converter. The resolution of the DPWM module, $N_{dpwm} = 10$ bits, is higher than the resolution of the ADC, $N_{adc} = 9$ bits, however steady-state limit cycling is observed both before and after the load current step, since no integral term was used in the control law. On the other hand, in Fig. 2.3(b) an integral term is added to the control law, and the steady-state limit cycling is eliminated.



(a)



(b)

Figure 2.3: Simulation of a DPWM converter output voltage under a load current transient with integral term (a) not included and (b) included in control law. $V_{in} = 5$V, $V_{ref} = 1.5$V, $f_{sw} = 250$kHz, $N_{adc} = 9$ bits, and $N_{dpwm} = 10$ bits.

Chapter 3

DPWM Resolution and Digital Dither

3.1 Quantization Resolution

The precision with which a digital controller regulates V_{out} is determined by the resolution of the ADC. In particular, V_{out} can be regulated with a tolerance of one LSB of the ADC. Many present-day applications, such as microprocessor VRM's, demand regulation precision at the order of tens of millivolts [9], requiring ADC's and DPWM modules with very high resolution. For example, regulation resolution of 10mV at $V_{in} = 5$V corresponds to ADC resolution of $N_{adc} = \log_2(5V/10mV) = 9$ bits, implying DPWM resolution of at least $N_{dpwm} = 10$ bits to avoid steady-state limit-cycling. For a converter switching frequency of $f_{sw} = 1$MHz, such resolution would require a $2^{10} f_{sw} = 1$GHz fast clock in a counter-comparator implementation of the DPWM module, or $2^{10} = 1024$ stages in a ring oscillator implementation, resulting in high power dissipation or large area ([6, 3, 4]). Thus, it is beneficial to look for ways to use low-resolution DPWM modules to achieve the desired high V_{out} resolution.

One method which can increase the effective resolution of a DPWM module is dithering. It amounts to adding high-frequency periodic or random signals to a certain quantized signal, which is later filtered to produce averaged DC levels with increased resolution. Analog dither has been used to increase the effective resolution of a DPWM module [10], however in this case an analog controller was used. Analog dither is difficult to generate and control, it is sensitive to analog component variations, and it can be mixed only with analog signals in the converter, and not with signals inside a digital controller. On the other hand, digital dither generated inside the controller is simpler to implement and control, is insensitive to analog component variations, and can offer more flexibility. Therefore, the use of digital dither to improve the resolution of DPWM modules is discussed in the present section.

3.2 Single-phase Dither

The idea behind digital dither is to vary the duty cycle by an LSB over a few switching periods, so that the *average* duty cycle has a value *between* two adjacent quantized duty cycle levels. The averaging action is implemented by the output LC filter. The dither concept is illustrated in Fig. 3.1. Let D_{c1} and D_{c2} correspond to two adjacent quantized duty cycle levels put out by the DPWM module, $D_{c2} = D_{c1} + LSB$. If the duty cycle is made to alternate between D_{c1} and D_{c2} every next switching period, the average duty cycle over time will equal $(D_{c1} + D_{c2})/2 = D_{c1} + \frac{1}{2}LSB$. Thus, an intermediate $\frac{1}{2}LSB$ sub-bit level can be implemented by averaging over two switching periods, resulting in an increase of the effective DPWM resolution of one bit. Using the same reasoning, $\frac{1}{4}LSB$ and $\frac{3}{4}LSB$ levels can be implemented by averaging over four switching periods (Fig. 3.2), which increases the effective DPWM resolution by 2 bits. Finally, it can be seen that by using dither patterns spanning 2^M switching

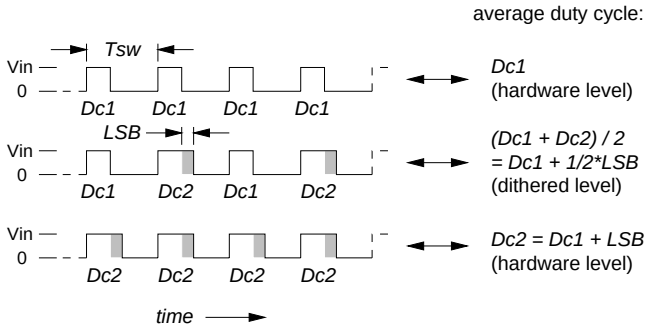


Figure 3.1: Use of switching waveform dither to realize a $\frac{1}{2}LSB$ DPWM level (1-bit dither).

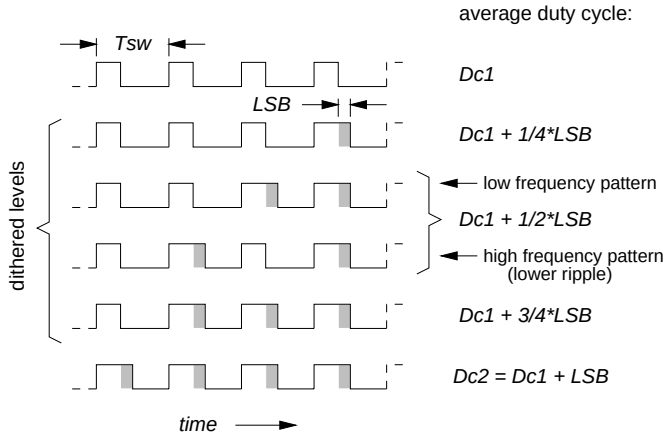


Figure 3.2: Switching waveform dither patterns realizing $\frac{1}{4}LSB$, $\frac{1}{2}LSB$, and $\frac{3}{4}LSB$ DPWM levels (2-bit dither).

periods, the effective DPWM resolution can be increased by M bits,

$$N_{dpwm,eff} = N_{dpwm} + M \tag{3.1}$$

where N_{dpwm} is the hardware DPWM resolution, and $N_{dpwm,eff}$ is the effective DPWM resolution.

3.3 Dither Patterns

Of course, the effective increase in DPWM resolution by dithering does not come for free. The dithering of the duty cycle creates an additional AC ripple at the output of the *LC* filter, which is

superimposed on the ripple from the converter switching action. It is desirable to keep the amplitude of the dither ripple low, in order to avoid poor output regulation, EMI, and limit cycles (which may result from the interaction between the dither ripple and the ADC). Thus it is beneficial to select dither patterns that minimize the dither ripple.

For a dither sequence with a particular length (2^M switching cycles for M-bit dither) there may be a few different dither patterns that average to the same DC level. For example, in Fig. 3.2 the $\frac{1}{2}LSB$ level can be implemented with two different sequences: $\{D_{c1}, D_{c1}, D_{c2}, D_{c2}\}$ or $\{D_{c1}, D_{c2}, D_{c1}, D_{c2}\}$. The latter pattern has higher fundamental frequency, and thus produces less output voltage ripple, due to the low-pass characteristic of the output LC filter.

Two sets of 3-bit dither sequences are shown in Table 3.1, with "1" standing for the addition of an LSB to the duty cycle. Table 3.1(a) corresponds to a simple rectangular waveform dither discussed in [11]. The generation of these patterns is very systematic and thus easy to implement. On the other hand, the dither sequences in Table 3.1(b) were chosen with the aim of minimizing their low frequency spectral content [5]. Thus, when filtered, they produce the lowest ripple for a given average duty cycle. Notice that, while for the rectangular-waveform dither the sequences producing *lowest* ripple are $\{0, 0, 0, 0, 0, 0, 0, 1\}$ and its complement, for the minimum-ripple dither the ripple produced by any sequence does not exceed the ripple produced by $\{0, 0, 0, 0, 0, 0, 0, 1\}$ and its complement. Therefore, the minimum-ripple sequences have a clear advantage over the rectangular-waveform sequences, with respect to dither ripple size.

Yet another dither generation approach is to use $\Sigma\Delta$ modulation, however it does not guarantee minimum-ripple patterns, and further the dither spectral content is hard to predict. $\Sigma\Delta$ modulation in power electronics applications is discussed in [12], [13].

Table 3.1: 3-bit dither sequences

(a) Rectangular-waveform dither

Sequence Average	*Dither Sequence*								*Ripple*
0	0	0	0	0	0	0	0	0	—
1/8	0	0	0	0	0	0	0	1	*lowest*
2/8	0	0	0	0	0	0	1	1	
3/8	0	0	0	0	0	1	1	1	
4/8	0	0	0	0	1	1	1	1	***highest***
5/8	0	0	0	1	1	1	1	1	
6/8	0	0	1	1	1	1	1	1	
7/8	0	1	1	1	1	1	1	1	*lowest*

(b) Minimum-ripple dither

Sequence Average	*Dither Sequence*								*Ripple*
0	0	0	0	0	0	0	0	0	—
1/8	0	0	0	0	0	0	0	1	***highest***
2/8	0	0	0	1	0	0	0	1	
3/8	0	0	1	0	0	1	0	1	
4/8	0	1	0	1	0	1	0	1	*lowest*
5/8	0	1	0	1	1	0	1	1	
6/8	0	1	1	1	0	1	1	1	
7/8	0	1	1	1	1	1	1	1	***highest***

3.4 Dither Generation Scheme

Fig. 3.3 shows a dither generation scheme that can produce patterns of *any* shape, and can therefore implement minimum-ripple dither such as the one in Table 3.1(b). A look-up table stores 2^M

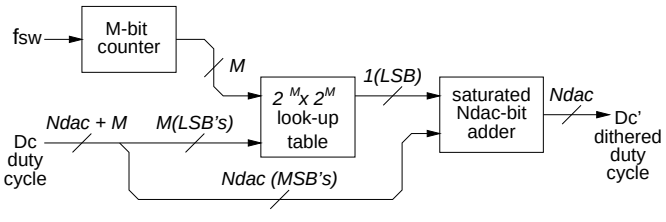


Figure 3.3: Structure for adding arbitrary dither patterns to the duty cycle.

dither sequences, each 2^M bits long, corresponding to the sub-bit levels implemented with M-bit dither. The M LSB's of the duty cycle command D_c select the dither sequence corresponding to the appropriate sub-bit level, while the M-bit counter sweeps through this dither sequence. The dither pattern is then added to the N MSBs of D_c to produce the duty cycle command D_c' which is sent to the hardware DPWM module.

3.5 Dither Ripple Size

In Section 3.2 it was shown that the longer the dither patterns used, the larger the effective DPWM resolution. However, longer dither patterns can cause higher output ripple, since they contain lower frequency components, and the *LC* filter has less attenuation at lower frequencies. This consideration puts a practical limit on the number of bits of dither that can be added to increase the resolution of the DPWM module.

For the rectangular-waveform dither in Table 3.1(a) some simple mathematical analysis (see Appendix A) can give an estimate of the maximum peak-to-peak ripple added to the output voltage as a result of the dither,

$$v_{p-p,dith} \leq \left(\frac{f_c}{f_{sw}}\right)^2 2^{2M} \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \tag{3.2}$$

for $f_c < f_{dith} < f_z$, and

$$v_{p-p,dith} \leq \frac{{f_c}^2}{f_z f_{sw}} 2^M \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \tag{3.3}$$

for $f_c < f_z < f_{dith}$, where f_{dith} is the fundamental frequency of the dither,

$$f_{dith} = f_{sw}/2^M, \tag{3.4}$$

f_c is the LC filter cutoff frequency, and f_z is the ESR zero frequency associated with the output capacitor.

Once the amplitude of the dither is known, we can develop a condition on how many bits of dither, M, can be used in a certain system, without inducing limit cycles (see Appendix A),

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2(2^{\Delta N}-1)\right] \tag{3.5}$$

for $f_c < f_{dith} < f_z$, and

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\frac{f_z f_{sw}}{{f_c}^2}(2^{\Delta N}-1)\right] \tag{3.6}$$

for $f_c < f_z < f_{dith}$, where

$$\Delta N = N_{dpwm,eff} - N_{adc} = (N_{dpwm} + M) - N_{adc} \tag{3.7}$$

is the difference between the effective resolutions of the DPWM and the ADC (in bits). For example, in Section 2.1 it was suggested that making the resolution of the DPWM one bit higher then that of the ADC adequately satisfies the condition to eliminate steady-state limit cycling, hence $\Delta N = 1$. The above equations can be used by starting with a guess for M, obtaining the corresponding dither frequency from (3.4), and then using (3.5) or (3.6), respectively, to obtain a bound on M. If the result is not consistent with the initial guess for M, the procedure should be repeated with a reduced value of M. On the other hand, if the inequalities are satisfied, the value of M can be increased, and the procedure can be repeated.

In Section 3.3 it was shown that there are dither patterns, such as the minimum-ripple dither in Table 3.1, that produce lower ripple compared to the rectangular-waveform dither on which the above analysis is based. If such dither patterns are used, (3.2) and (3.3) give an overestimate, while (3.5) and (3.6) yield an underestimate. Nevertheless, these equations are still a useful tool for conservative design, since ripple amplitude analysis of the minimum-ripple dither is far more involved.

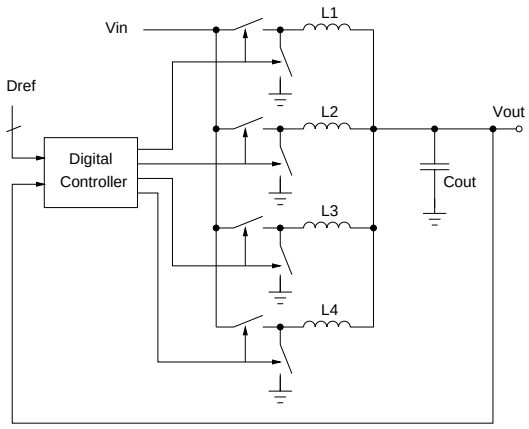


Figure 3.4: Block diagram of a 4-phase buck converter.

3.6 Multi-phase Dither

The concept of controlled dither can be extended to multi-phase (interleaved) VRM's. In a multi-phase converter, multiple single-phase power trains are connected to a common output capacitor and switched with the same duty cycle, but out of phase, which decreases the ripple in the output voltage and input current. For example, the block diagram of a 4-phase buck converter is shown in Fig. 3.4. In this case, the four power train legs are switched $360^{\circ}/4 = 90^{\circ}$ out of phase.

The controlled dither technique developed for single phase converters can be applied directly to the multi-phase case. For example, to achieve a $D_{c1} + \frac{1}{2}LSB$ level, duty cycle D_{c1} is applied to *all* phases for one switching period, followed by $D_{c2} = D_{c1} + LSB$ applied to all phases, and so on. However, in a multi-phase converter we can exploit the additional degrees of freedom associated with the independent switching of the different phases to further reduce the dither ripple, and thus allow more bits of dither, and respectively less bits of hardware resolution of the DPWM module.

Consider again the case of a $D_{c1} + \frac{1}{2}LSB$ level. This level can be implemented by commanding, in the same switching period, D_{c1} to two of the phases and D_{c2} to the other two, so that the average

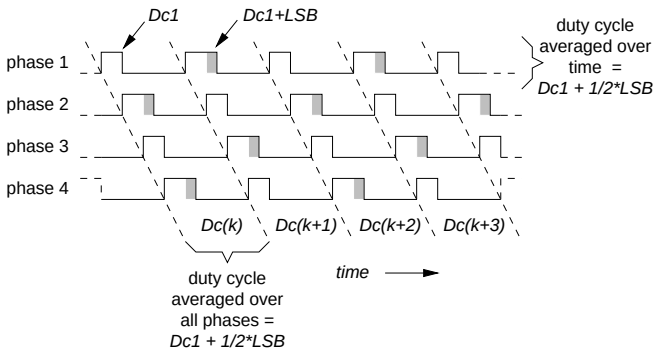


Figure 3.5: 4-phase switching waveform dither patterns implementing a $\frac{1}{2}LSB$ DPWM level.

duty cycle over all phases is $D_{c1} + \frac{1}{2}LSB$ for that period. The next switching period the duty cycle commands are toggled, so that the average over all phases is still $D_{c1} + \frac{1}{2}LSB$, however the *average over time* for each phase is $D_{c1} + \frac{1}{2}LSB$ as well (Fig. 3.5). The equal averaging over time for each phase is necessary to avoid DC current mismatch among the phases. This approach can be extended for other sub-bit levels, like $D_{c1} + \frac{1}{4}LSB$, noting that for a multi-phase converter with N_ϕ phases, $log_2 N_\phi$ bits of dither can be implemented by averaging over the phases. Multi-phase dither can increase the dither frequency seen at the output node about N_ϕ times, thus reducing the resulting ripple, and allowing approximately $log_2 N_\phi$ more bits of DPWM resolution to be implemented with dither.

Chapter 4

VRM Passive Current Sharing

4.1 Digital Control and Current Sharing

In general, like analog controllers, digital controllers for multi-phase VRM's can be used successfully with active current sharing schemes, typically involving individual current sensing of each phase. However, unlike their analog counterparts, digital controllers have the advantage of almost perfect matching of the duty cycles of the PWM signals among the different phases, potentially allowing for the use of *passive current sharing* schemes, which eliminates the need for individual sensing and control of the phase currents. The use of passive current sharing may reduce the cost of the VRM, as a result of the smaller number of current sensors needed, as well as the reduced pin count of the controller IC.

To study the DC current sharing among the different phases in a k-phase converter we model the latter with the circuit shown in Fig. 4.1. Resistors R_1, R_2, ..., R_k model the DC resistance of each phase of the power train, and $V_1, V_2, \ldots, V_k$ model the average open-circuit voltage for each phase, i.e.

$$V_i = V_{in} D(i), \qquad i = 1, 2, \ldots, k \tag{4.1}$$

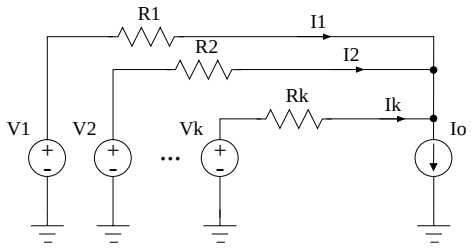


Figure 4.1: DC current sharing model of a k-phase converter.

where $D(i)$ is the duty cycle command for phase i, and V_{in} is the input voltage.

With R_1, R_2, ..., R_k having arbitrary and possibly mismatched values, as a result of power train mismatches among the phases, the total power dissipation of the system is minimized when $V_1 = V_2 = \ldots = V_k$. To see this, consider the quantity

$$\hat{P} = \sum_{i=1}^{k} R_i I_i^2 + \lambda(I_o - \sum_{i=1}^{k} I_i), \tag{4.2}$$

which is the total DC power loss in the power train with the constraint that, the sum of the individual phase currents must equal the total load current, appended with Lagrange multiplier λ. A necessary condition for a minimum of the total power loss subject to the constraint is that all first order partial derivatives of $\hat{P}$ in equation (4.2) are zero. This yields

$$2R_i I_i - \lambda = 0 \tag{4.3}$$

for each index i corresponding to each phase of the converter. The constraint (4.3) implies that the DC voltage drops $R_i I_i$ for all phases are equal, which is equivalent to the power optimality condition $V_1 = V_2 = \cdots = V_k$ stated above.

The above result implies that when the duty cycles applied to different phases are identical, the power loss is minimized regardless of the possible resistive mismatch among the phases. A digital

controller can produce acurately matched PWM waveforms for the different phases, with possible timing mismatch resulting only from parameter variations of the power FETs and gate drives, which is discussed in Section 4.3.

4.2 Phase Current Mismatch Due to Power Train Resistance Mismatch

As it was argued above, if the multi-phase converter has matched duty cycles but mismatched power train resistances among the phases, the output current distributes itself among the phases so as to minimize the power dissipation in the power train. However, the actual current mismatch is still of interest since it may have undesirable consequences such as possible saturation of the inductors.

Assume matched duty cycles among the phases, $V_1 = V_2 = \ldots = V_k = V_{in}D$. Then, a power train resistance mismatch ΔR results in worst case current mismatch through a particular phase (let this be phase i) when all other phases have the same power train resistance equal to R, while that phase has mismatched resistance $R_i = R + \Delta R$. Since the power train resistances of the different phases form a current divider for the output current I_o, the current through phase i is

$$I_i = I_o \frac{R/(k-1)}{R_i + R/(k-1)}. \tag{4.4}$$

Then, the mismatch current flowing in phase i is the difference between current I_i and the nominal phase current I_o/k,

$$\Delta I_i = I_i - \frac{I_o}{k} = -I_i \frac{k-1}{k} \frac{\Delta R}{R}. \tag{4.5}$$

Hence, the worst case phase current variation due to a power train resistance mismatch ΔR, is

$$\left(\frac{\Delta I_i}{I_i}\right)_R = -\frac{k-1}{k} \frac{\Delta R}{R}. \tag{4.6}$$

Finally, the value of the effective power train resistance for each phase can be estimated from

$$R = DR_{DS(on),h} + (1-D)R_{DS(on),l} + R_L + R_{trace} \tag{4.7}$$

where D is the duty cycle; $R_{DS(on),h}$ and $R_{DS(on),l}$ are the on-resistances of the high- and low-side MOSFET switches, respectively; R_L is the inductor DC resistance; and R_{trace} is the resistance of the printed circuit board traces in the power train for each phase. The relative variations of these parameters can be obtained from the data sheet for a particular process, and (4.7) can be used in conjunction with (4.6) to estimate the total current mismatch due to power train resistance mismatch.

4.3 Phase Current Mismatch Due to Duty Cycle Mismatch

Consider again Fig. 4.1 and let $R_1 = R_2 = \ldots = R_k = R$. However, assume that $V_1, V_2, \ldots, V_k$ are not equal as a result of duty cycle mismatch among the phases. A duty cycle mismatch ΔD results in worst case current mismatch through a particular phase (let this be phase i) when all other phases are switched with the same duty cycle D, while that phase is switched with a mismatched duty cycle $D + \Delta D$, *i.e* $V_i = V_{in}(D + \Delta D)$. The mismatch current through phase i, $\Delta I_i = I_i - I_o/k$, is then

$$\Delta I_i = \frac{V_i - V_{in}D}{R + R/(k-1)} = \frac{k-1}{k}\frac{V_{in}}{R}\Delta D. \tag{4.8}$$

The power loss in the multi-phase part of the power train is $P_{loss,mp} = I_o^2 R/k$, and the converter input power is $P_{in} \approx DV_{in}I_o$. Then the efficiency of the multi-phase part of the converter power train is

$$\eta_{mp} = 1 - \frac{P_{loss,mp}}{P_{in}} \approx 1 - \frac{I_o^2 R/k}{DV_{in}I_o}. \tag{4.9}$$

Solving (4.9) for R and substituting in (4.8), we obtain an expression for the worst case phase current

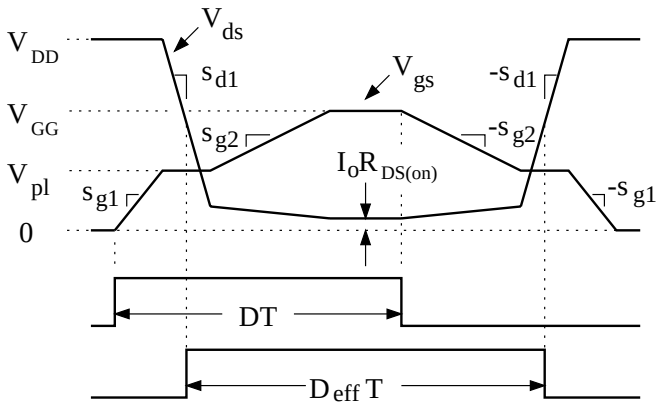


Figure 4.2: Duty cycle variation due to the MOSFET switching characteristic in continuous conduction mode.

variation, $\Delta I_i/I_i$ due to a duty cycle mismatch ΔD,

$$\left(\frac{\Delta I_i}{I_i}\right)_D \approx \frac{k-1}{k}\frac{1}{1-\eta_{mp}}\frac{\Delta D}{D}. \tag{4.10}$$

One immediate observation from (4.10) is that the current mismatch sensitivity becomes worse if the efficiency of the converter improves, or if the duty cycle decreases.

4.4 Duty Cycle Mismatch due to MOSFET Switching Parameter Variations

A digital PWM controller can provide very accurate matching among the duty cycles for the different phases, thus the main source of duty cycle mismatch are the analog gate drives and power switches. Fig. 4.2 shows a simplified model of the switching characteristic of a MOSFET which determines the relation between the duty cycle output by the controller (D) and the effective duty cycle seen at the switching node of the power train (D_{eff}). The gate drive of the MOSFET is modeled as a current source with output current $\pm I_G$ and maximum output voltage V_{GG}. Let C_{gs} and C_{gd} denote respectively

the transistor gate-source and gate-drain capacitances, and let subscripts sat and lin refer respectively to the saturation and linear regions of operation of the MOSFET.

In the beginning of the switching period ($T = 1/f_{sw}$) the gate drive sources current I_G into the high-side MOSFET gate, making its gate-source voltage V_{gs} ramp up at a rate of approximately $s_{g1} = I_G/(C_{gs} + C_{gd})_{sat}$. The drain-source voltage V_{ds} remains at the supply voltage V_{DD} until the drain current I_d reaches the value of the output current I_o. At this point, V_{gs} plateaus at a value

$$V_{pl} \approx V_{TH} + \sqrt{2I_o/k_m} \tag{4.11}$$

where k_m is the device gain factor and we assume that $I_o \gg I_G$. While $V_{gs} = V_{pl}$, V_{ds} moves down at a rate of $s_{d1} = -I_G/C_{gd(sat)}$ until the transistor goes into the linear region. Then V_{gs} continues to increase at a rate $s_{g2} = I_G/(C_{gs} + C_{gd})_{lin}$ until it reaches V_{GG}. In the linear region V_{ds} is about $I_o R_{DS(on)}$. The MOSFET turn-off is analogous.

From Fig. 4.2 it can be seen that the effective duty cycle, measured between the midpoints in the swing of V_{ds}, is

$$D_{eff} \approx D + (V_{GG} - 2V_{pl}) f_{sw}/s_g \tag{4.12}$$

where, for simplicity, we have set $s_g = s_{g1} = s_{g2}$. Then the variation of D_{eff} due to perturbations of V_{TH} and s_g is, respectively,

$$(\Delta D_{eff})_{V_{TH}} \approx -2 f_{sw}/s_g \cdot \Delta V_{TH} \tag{4.13}$$

and

$$(\Delta D_{eff})_{s_g} \approx -(V_{GG} - 2V_{pl}) f_{sw}/{s_g}^2 \cdot \Delta s_g. \tag{4.14}$$

Since typically $2V_{pl}$ is close to V_{GG}, (4.14) has small contribution to the overall D_{eff} variation relative to (4.13), and its effect may be neglected. Then, (4.13) can be used in conjunction with (4.10) to estimate the current variation among phases due to duty cycle mismatch.

4.5 A Passive Current Sharing Calculation Example

Given a certain specification on the maximum tolerable current mismatch among the phases of a multi-phase converter ($\Delta I_i/I_i$), the equations developed above can be used to estimate converter parameters such as the maximum allowable power MOSFET gate rise/fall time ($t_g = V_{GG}/s_g$), and total power train resistive mismatch among the phases ($\Delta R/R$). Equations (4.6), (4.10), and (4.13) were used to derive the constraints in Table 4.1 based on a sample converter design. Finally, it should be noted again that, while the possible 20% phase current mismatch due to duty cycle mismatch may result in non-optimal power dissipation, the 20% current mismatch due to resistive mismatch will not degrade the converter efficiency. In this example, it is seen that a modest gate drive rise/fall time of < 13ns leads to quite acceptable current-sharing behavior. Experimental results supporting the feasibility of open-loop current sharing are presented in Chapter 7, as well as in [14].

Table 4.1: A passive current sharing example

	Specifications	
$\Delta I_i/I_i$	phase current mismatch	40%
$(\Delta I_i/I_i)_R$	– due to resistive mismatch	20%
$(\Delta I_i/I_i)_D$	– due to duty cycle mismatch	20%
	Some Converter Parameters	
k	number of phases	4
f_{sw}	switching frequency	1 MHz
D	duty cycle	$1/5$
η_{mp}	multi-phase power train efficiency	90%
V_{GG}	gate drive voltage	5 V
ΔV_{TH}	threshold voltage variation	1 V
	Resulting Constraints	
s_g	power MOSFET gate rate	> 0.38 V/ns
t_g	power MOSFET gate rise/fall time	< 13 ns
$\Delta R/R$	power train resistive mismatch	$< 26\%$

Chapter 5

VRM Transient Response

5.1 Next-Generation Microprocessor Specifications

The projected transient response specifications for next generation microprocessor VRM's [9] are summarized in Table 5.1. The very low conversion ratio ($< 1/12$), the high load current and current slew rate, and the tight output regulation tolerance present a challenge to designers. In this chapter we analyze the VRM transient response from the perspective of digital control, and propose relevant architectural solutions.

Table 5.1: Next generation microprocessor VRM specifications [*]

V_{in}	input voltage	$>$ 12 V
V_{ref}	reference voltage	$<$ 1 V
$\Delta V_{o,max}$	regulation tolerance	$<$ 50 mV
$I_{o,max}$	load current	$>$ 100 A
dI_o/dt	current slew rate	$>$ 350 A/μs
T_d	regulator response time	$<$ 200 ns

(*) Source: reference [9]

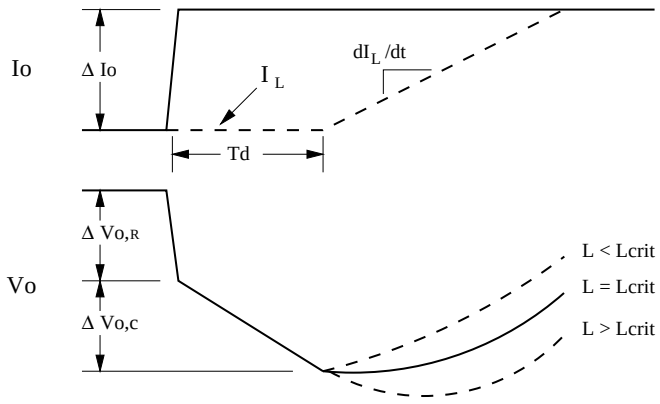


Figure 5.1: Transient response of a buck VRM due to load current step.

5.2 VRM Transient Response

An output voltage transient of a buck VRM due to an increase in the load current, I_o, by ΔI_o is illustrated in Fig. 5.1. The load current step will first cause output voltage drop of magnitude $\Delta V_{o,R} = \Delta I_o R_{ESR}$ due to the effective series resistance (R_{ESR}) of the output capacitor[1]. Then, since the controller has non-zero response delay, V_o will continue to drop due to discharge of the output capacitor C_o. Let T_d be the delay of the controller response, *i.e.* the time between the instant a step in the load current has occurred and the resulting update of the duty cycle by the controller. Then the V_o drop due to the capacitive discharge will be $\Delta V_{o,C} = \Delta I_o T_d / C_o$. After time T_d, the controller responds to the load step by increasing the duty cycle, resulting in inductor current (I_L) increase at a rate of $dI_L/dt = V_L/L$, where, assuming saturated controller response, $V_L = V_{in} - V_o$ ($V_L = -V_o$ for an unloading transient). Consequently, V_o exhibits second-order behavior and eventually starts to increase. Reference [16] gives a condition on C_o ensuring that V_o starts increasing immediately after I_L begins to ramp up. Since

[1]Here, for clarity, we are omitting the initial V_o drop due to the series inductance of the output capacitor. Recent research [15] has developed an advanced capacitor model for power applications and has indicated that the capacitor series inductance can be greatly reduced with proper capacitor packaging and power train layout.

$\tau_o = R_{ESR}C_o$ is approximately constant for a particular capacitor technology, this condition can be restated as,

$$\frac{dI_L}{dt} \geq \frac{\Delta I_o}{\tau_o} \tag{5.1}$$

which implies a critical value of L,

$$L_{crit} = \frac{\tau_o V_L}{\Delta I_o}. \tag{5.2}$$

For $L \leq L_{crit}$, V_o starts to increase immediately after I_L begins to ramp up.

5.3 Implementation of Optimal Voltage Positioning

The concept of optimal voltage positioning has been widely used in recent voltage regulator designs. The idea is to always position V_o at $V_{ref} - R_{ESR}I_o$, where V_{ref} is the reference voltage, instead of driving it to V_{ref} [16]. In that case, the converter behaves as a voltage source with value V_{ref} and output impedance that is always real and equal to R_{ESR}. If optimal voltage positioning is used, ideally C_o can be made half the size required for a stiff voltage regulator design, which can save on cost and circuit area and volume.

The optimal voltage positioning technique can be extended to include non-zero controller delays. From Fig. 5.1 it can be seen that, assuming $L \leq L_{crit}$, the V_o excursion due to a load current step ΔI_o is

$$\begin{aligned} \Delta V_o &= \Delta V_{o,R} + \Delta V_{o,C} \\ &= \Delta I_o R_{ESR} + \Delta I_o T_d / C_o \\ &= \Delta I_o R_{ESR} \left(1 + T_d/\tau_o\right). \end{aligned} \tag{5.3}$$

Equation (5.3) shows that the output voltage step is directly proportional to the output current step, with proportionality constant which is a linear combination of the output capacitor ESR and the delay of the

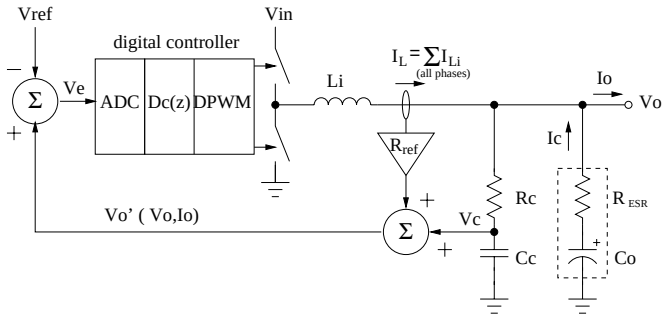


Figure 5.2: Implementation of optimal voltage positioning with a digital controller.

controller. Thus, using the reasoning behind the optimal voltage positioning technique, we can design the controller to always position V_o at

$$V_o \rightarrow V_{ref} - R_{ref} I_o \tag{5.4}$$

where

$$R_{ref} = R_{ESR}\left(1 + \frac{T_d}{\tau_o}\right). \tag{5.5}$$

This extension is particularly important for capacitor technologies with small τ_o, such as ceramic capacitors, where the term corresponding to controller delay may dominate.

A scheme for implementing optimal voltage positioning with a digital controller is shown in Fig. 5.2. The idea is to reconstruct the output current I_o by sensing the total inductor current through all phases, $I_L = \sum_{i=1}^{4} I_{Li}$, and estimating the current flowing out of the output capacitor, I_C. If the time constant τ_c of the estimator $R_c - C_c$ is equal to τ_o, the output of the estimator is the voltage across C_o,

$$V_c = V_o + R_{ESR} I_C. \tag{5.6}$$

By adding the output of the estimator to the inductor current I_L multiplied by a transresistance gain of

R_{ref}, we obtain the quantity

$$\begin{aligned} V_o' &= V_o + R_{ESR} I_C + R_{ref} I_L \\ &\approx V_o + R_{ref} I_o, \qquad \text{if} \quad R_{ref} \approx R_{ESR}. \end{aligned} \tag{5.7}$$

Subtracting V_{ref} from V_o' we form the error signal V_e. Thus, if the controller has high gain, and the system is stable, V_o will follow (5.4).

The controller implements a digital PID control law $D_c(z)$ which represented in the discrete-time domain has the form given in 1.1.

Finally, observe that the sensing approach introduced above uses only one ADC to obtain information about both V_o and I_o, and that all current sensing is done before the output capacitor to ensure low output impedance.

More discussions of VRM transient response and Optimal Voltage Positioning can be found in [16], [17], [18], [19].

Chapter 6

ADC Topology

6.1 Window ADC

The precision with which a digital controller positions the output voltage V_o is determined by the resolution of the ADC. In particular, V_o can be regulated with a precision of one LSB of the ADC. Many applications, such as next-generation microprocessor VRM's, are expected to require regulation tolerances of less than 50mV [9], demanding ADC modules with very high resolution. For example, regulation resolution of 10mV at $V_{in} = 5$V corresponds to ADC resolution of $N_{adc} = \log_2(5V/10mV) = 9$ bits. Further, next generation microprocessors are expected to have current slew rates of more than 350A/μs demanding VRM's with extremely fast responses. In addition, topologies with low ADC latency are desirable in the cases when the ADC is inside a feedback loop, since delays in the ADC correspond to phase shift that may degrade the loop response. Consequently the ADC's used in digital VRM controllers should have very low latency. While multi-stage ADC topologies may have high throughput (high sampling rate), they have larger latency due to either multiple comparisons (pipeline ADC's), or

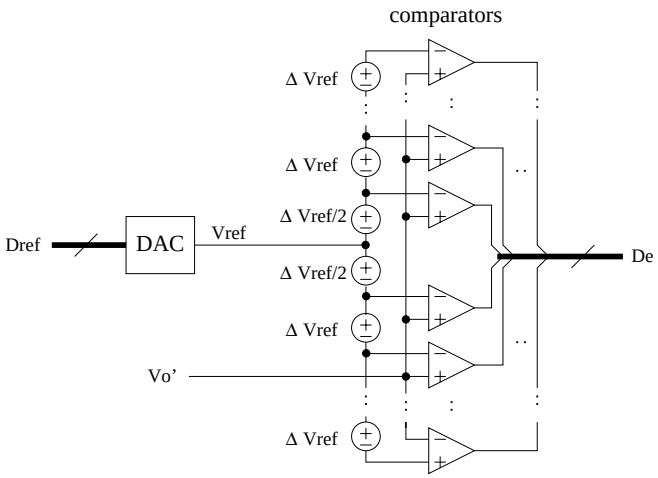


Figure 6.1: Block diagram of a window ADC. It implements both an ADC and an error amplifier.

digital filtering ($\Sigma\Delta$ ADC's). Thus a single stage (flash) topology is preferable in applications such as VRM's where the speed of response is of paramount importance. From Fig. 7.2 it can be seen that the controlled quantity V_o' does not have large excursions beyond V_{ref} in normal operation. Thus, using a high resolution flash ADC that covers the full range between ground and V_{in} will demand excessive power and silicon area. Rather, an ADC topology can be conceived of, which has high resolution only in a small window around V_{ref}.

A block-diagram of such a "window" ADC is presented in Fig. 6.1. A Digital-to-Analog Converter (DAC) converts the digital reference word D_{ref} to an analog voltage V_{ref}. Note that this DAC can be slow compared to the response time of the regulator, since D_{ref} does not change very fast, if at all. Then, a number of comparators are connected to V_{ref} through an offset network with steps ΔV_{ref}, creating a few quantization bins around V_{ref}. The controlled quantity V_o' is fed in the other input of the comparators. Note that, since V_o' is compared against V_{ref}, the resulting digital signal (D_e) is the difference between the two, which is a digital representation of the error signal V_e. Hence, the window

architecture implements both an ADC and an error amplifier.

For example, if the converter is designed for regulation tolerance of 50mV, V_o' will not exceed ± 50mV about V_{ref} under normal operation. In this case ADC resolution of $\Delta V_{ref} = 10$mV seems reasonable to provide good control of V_o within the tolerance window. Then only $2 \times 50\text{mV}/10\text{mV} = 10$ ADC bins are required to cover the range of V_o', which corresponds to ADC resolution between 3 and 4 bits. In fact, the ADC in the prototype VRM from Chapter 7 uses a window structure.

6.2 Output Voltage Clamping

A modification of the above control scheme may result in a smaller number of comparators in the ADC and faster regulator response: The number of comparators is reduced to, say, four, and the two comparators at the extremes of the ADC quantization window are sampled at a frequency higher than the switching frequency. If V_o' exceeds the range of the quantization window during a large transient, these comparators turn *all* converter phases on or off (depending on the direction of the transient), in an attempt to clamp V_o. This approach can substantially speed up the response of the regulator without changing the converter steady-state switching frequency, resulting in smaller output capacitors. It comes at the cost of implementing two very fast comparators. A similar clamping approach has been successfully used in analog VRM controllers [20].

Chapter 7

Experimental Results

A prototype digitally controlled VRM using a 4-phase buck topology with passive current sharing was built with the parameters shown in Table 7.1. The controller was implemented using a DSP board connected to a PC, and an FPGA to produce the overall timing and the multi-phase DPWM signals.

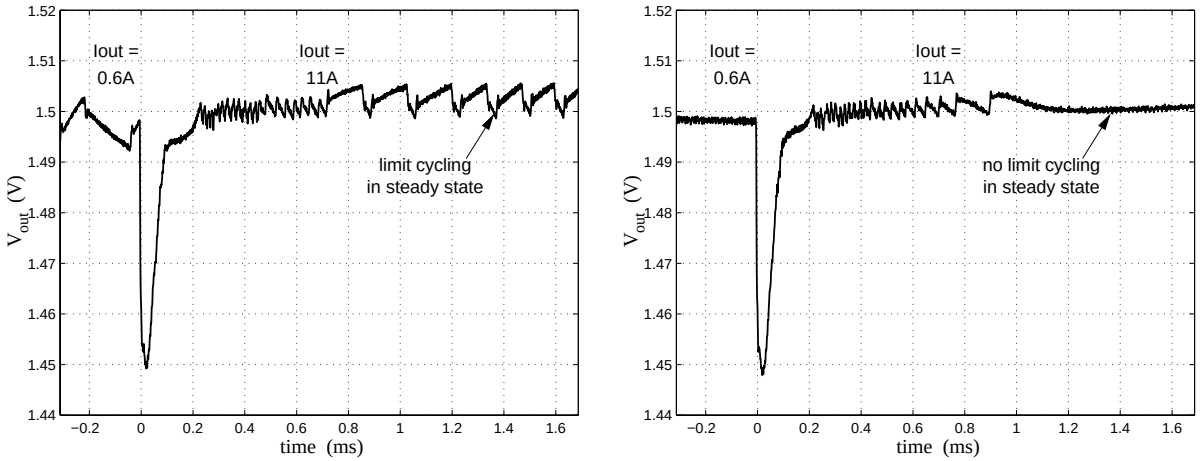
First, the digital dither technique was tested on a prototype converter with results confirming the theoretical expectations from Chapters 2 and 3. In the prototype, the ADC had 9-bit resolution and the DPWM had 7 bits of hardware resolution. The control law included an integral term, thus (2.2) was satisfied. Condition (2.3) was satisfied as well, by design of the proportional gain. The transient response of the converter due to a load current step with $R_{ref} = 0$ (no optimal voltage positioning) is shown in Fig. 7.1(a). The system exhibits steady-state limit cycling since condition (2.1) is not met. Subsequently 3-bit single-phase digital dither was introduced, using the minimum ripple sequences from Table 3.1(b), thus increasing the effective resolution of the DPWM module to 7 + 3 = 10 bits. The step response of the modified system is shown in Fig. 7.1(b). The effective resolution of the DPWM is now higher than that of the ADC, and all three *no-limit-cycle* conditions (2.1–2.3) are satisfied. Consequently, the steady

Table 7.1: Prototype VRM parameters

V_{ref}	reference voltage	1.5 V
V_{in}	input voltage	5 V
k	number of phases	4
f_{sw}	switching frequency	250 kHz
L_i	phase inductors	4.4 μH
C_o	output capacitance	4 mF (tantalum)
R_{ESR}	output capacitor ESR	4 $m\Omega$
N_{adc}	effective ADC resolution	9 bit
N_{dpwm}	effective DPWM resolution	7 bit (hardware)
		+ 3 bit (dither)
K_p	proportional gain	10
K_d	derivative gain	14
K_i	integral gain	0.25
τ_c	$R_c - C_c$ estimator time const.	10 ns
T_d	controller delay	5 μs

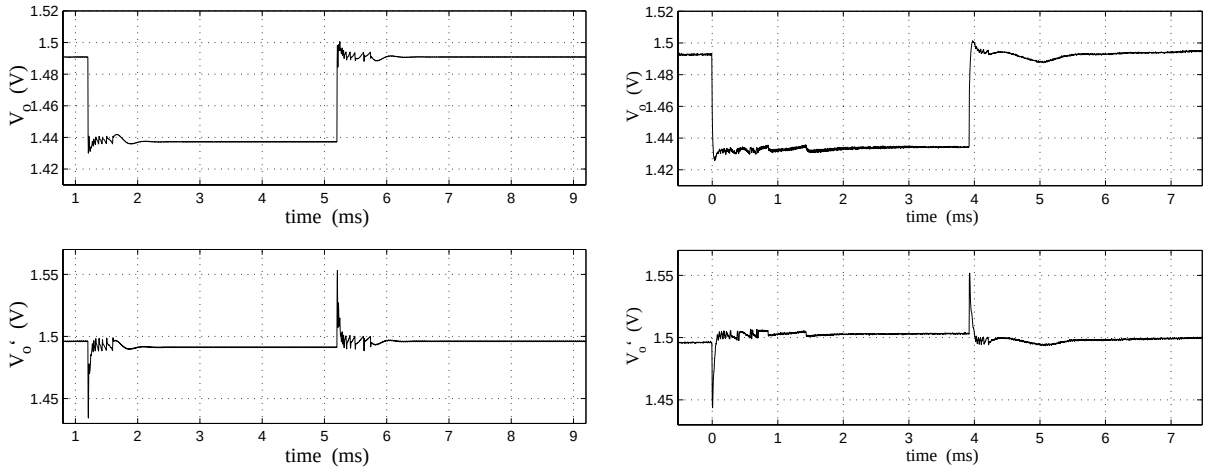
state limit cycles are eliminated. It should be noted that in this case the steady state ripple is only due to the multi-phase switching and the dither, and it does not exceed a few millivolts. This example illustrates the validity of the *no-limit-cycle* conditions, as well as the effectiveness of the digital dither.

Second, optimal voltage positioning was implemented with $R_{ref} = 5m\Omega$ using the scheme discussed in Chapter 5. The estimator time constant was adjusted so that $\tau_c \ll \tau_o$ to achieve good performance with moderate controller gain. Fig. 7.2(a) and (b) show, respectively, the simulated (with MATLAB) and experimental response of the converter to a load current change from 1A to 11A and back to 1A ($\Delta I_o = 10$A). Finally, current matching among the four phases was observed to be very good ($|\Delta I_i/I_i| < 10\%$).



(a) (b)

Figure 7.1: Experimental 4-phase buck converter transient response under a load current step with (a) N_{dpwm} = 7 bits, and
(b) $N_{dpwm,eff}$ = 7 bits + 3-bit dither = 10 bits. $N_{adc} = 9$ bits, $V_{in} = 5$V, $V_{ref} = 1.5$V, $f_{sw} = 250$kHz.



(a) (b)

Figure 7.2: Transient response of a prototype digitally controlled multi-phase buck converter with parameters from Table 7.1, resulting from a 10A load current step: (a) simulation, and (b) experimental results. V_o is the output voltage, and V_o' is the quantity compared to V_{ref} to form the error signal.

Chapter 8

Conclusion

This report discussed issues in the use of digital controllers in PWM converter applications. The presence of steady-state limit cycles in digitally controlled PWM converters was addressed, and conditions for their elimination were proposed. Digital dither was introduced as a means of increasing the effective resolution of DPWM modules, allowing for the use of low resolution DPWM units in high regulation accuracy applications. Bounds on the number of bits of dither that can be used in a particular converter were derived. Microprocessor VRM's were then discussed from the perspective of digital control. Passive current sharing was investigated, and estimates of the phase current mismatch due to power train parameter variations were derived. The VRM transient response was analyzed, considering non-zero controller delay, and a scheme for sensing a combination of the VRM output voltage and output current with a single low-resolution window ADC was proposed. Finally, experimental results from a prototype VRM were presented illustrating some of the ideas discussed in this report.

Appendix A

Dither Ripple Calculation

Since the dither constitutes switching between two adjacent quantized duty cycle levels, it can be modeled as a square wave with peak-to-peak amplitude of one hardware LSB of the DPWM module equal to $V_{in}/2^{N_{dpwm}}$. For M-bit rectangular-waveform dither (Table 3.1(a)), the dither waveform with the largest low frequency component is a square wave with 50% duty ratio at frequency

$$f_{dith} = f_{sw}/2^{M}. \tag{A.1}$$

This waveform can be used to study the worst case dither ripple. Since the dither is smoothed by the converter output LC filter, it is sufficient to consider only its fundamental frequency component, which is a sine wave with frequency f_{dith} and peak-to-peak amplitude

$$A_{p-p,dith} = \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}}. \tag{A.2}$$

The peak-to-peak output voltage ripple can then be bounded approximately as

$$v_{p-p,dith} \leq H(f_{dith})A_{p-p,dith} \tag{A.3}$$

where $H(f_{dith})$ is the attenuation of the output LC filter at frequency f_{dith}.

The LC filter has a cutoff frequency at $f_c = 1/2\pi\sqrt{L_o C_o}$ after which it rolls off at -40 dB/dec. A real capacitor has finite effective series resistance (r_{ESR}) which causes a zero in the filter characteristic at frequency $f_z = 1/2\pi r_{ESR} C_o$, changing the rolloff to -20 dB/dec. Thus,

$$H(f) \approx \left(\frac{f_c}{f}\right)^2 \quad \text{for} \quad f_c < f < f_z, \tag{A.4}$$

and

$$H(f) \approx \left(\frac{f_c}{f_z}\right)^2 \frac{f_z}{f} = \frac{{f_c}^2}{f_z f} \quad \text{for} \quad f_c < f_z < f. \tag{A.5}$$

Substituting back in (A.3), we obtain upper bounds for the peak-to-peak output voltage ripple due to dither,

$$v_{p-p,dith} \leq \left(\frac{f_c}{f_{sw}}\right)^2 2^{2M} \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \tag{A.6}$$

for $f_c < f_{dith} < f_z$, and

$$v_{p-p,dith} \leq \frac{{f_c}^2}{f_z f_{sw}} 2^M \frac{4}{\pi} \frac{V_{in}}{2^{N_{dpwm}}} \tag{A.7}$$

for $f_c < f_z < f_{dith}$.

Once the amplitude of the dither is known, a condition on how many bits of dither, M, can be used in a certain system can be developed. To ensure that the dither does not cause steady-state limit cycling, there should always be an effective DPWM level that completely fits into one ADC quantization bin, taking into account the dither ripple. With M-bit dither, the effective DPWM quantization bin size is

$$\Delta V_{dpwm,eff} = V_{in}/2^{N_{dpwm,eff}} = V_{in}/2^{N_{dpwm}+M}. \tag{A.8}$$

Geometric considerations show that the case which allows for the smallest dither ripple amplitude is when the effective DPWM levels are located at one-half effective DPWM bin size from the center of the ADC bin (Fig. A.1). Then the tolerable peak-to-peak dither ripple amplitude is bounded by

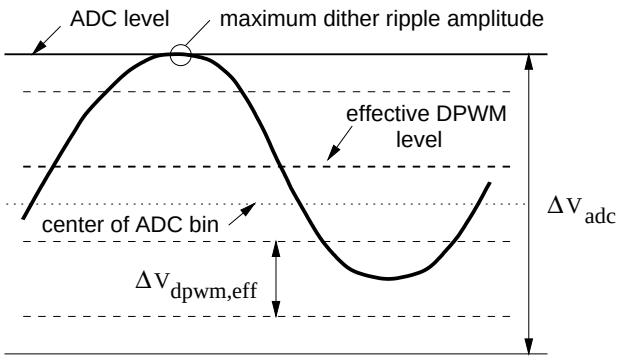


Figure A.1: Maximum dither ripple amplitude constraint. Illustrated case is for $N_{dpwm,eff} = N_{adc} + 2$

$$v_{p-p,dith} < \Delta V_{adc} - \Delta V_{dpwm,eff}. \tag{A.9}$$

Assuming that the ADC has resolution ΔN bits coarser than the effective resolution of the DPWM module,

$$N_{adc} = N_{dpwm,eff} - \Delta N = N_{dpwm} + M - \Delta N, \tag{A.10}$$

the ADC bin size is

$$\Delta V_{adc} = V_{in}/2^{N_{adc}} = V_{in}/2^{N_{dpwm}+M-\Delta N}. \tag{A.11}$$

Substituting (A.8) and (A.11) in (A.9), we obtain

$$v_{p-p,dith} < V_{in}\left(2^{\Delta N} - 1\right)/2^{N_{dpwm}+M}. \tag{A.12}$$

Combining (A.12) with (A.6) and (A.7) we obtain an upper bound on M,

$$M < \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2(2^{\Delta N} - 1)\right], \qquad \text{for } f_c < f_{dith} < f_z, \text{ and} \tag{A.13}$$

$$M < \frac{1}{2}\log_2\left[\frac{\pi}{4}\frac{f_z f_{sw}}{{f_c}^2}(2^{\Delta N} - 1)\right], \qquad \text{for } f_c < f_z < f_{dith}. \tag{A.14}$$

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