Digital Pulse-Width Modulation Control in Power Electronic Circuits: Theory and Applications

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by

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Abstract

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This thesis develops digital pulse-width-modulation (DPWM) control of switching power converters. A target application is microprocessor voltage regulation which requires high efficiency and tight output load-line control. A general framework for load-line control is developed, which encompasses relevant capacitor technologies, such as electrolytics and ceramics. It is shown that load-current feedforward can overcome the limited bandwidth of conventional feedback load-line control. The size of the output capacitor is then determined solely by transient and switching-ripple considerations, which are derived. This work enables microprocessor voltage-regulator implementations using a small number of ceramic output capacitors, while running at sub-megahertz switching frequencies.

Efficient DPWM controller implementations are discussed, addressing system sta-

bility issues unique to digital control. The existence of limit cycles is analyzed, as well as conditions for their elimination. Digital dither is introduced as a method to increase the effective DPWM resolution, thus preventing limit cycling, and enabling low-power, small-area DPWM implementations.

A method for direct control of synchronous rectifiers as a function of the load current is developed. The function relating the synchronous-rectifier timing to the load current is optimized on-line with a perturbation-based power-loss-minimizing algorithm. This approach provides fast synchronous-rectifier adjustment, robustness to disturbances, and the capability to simultaneously optimize multiple parameters. It also accomplishes an automatic, optimal transition to discontinuous-conduction mode at light load, thus improving converter efficiency. Efficiency is further enhanced by imposing a minimum duty-ratio limit to effect pulse-skipping at very light load.

Three experimental buck converters are developed to illustrate different aspects of this work. Simulations are used to further corroborate the results.

Professor Seth R. Sanders
Dissertation Committee Chair

In memory of my grandparents Bistra and Andrey,

to my mother Antonina,

with love and gratitude.

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Chapter 1

Introduction

1.1 Power Management Challenges of Digital Processing IC's

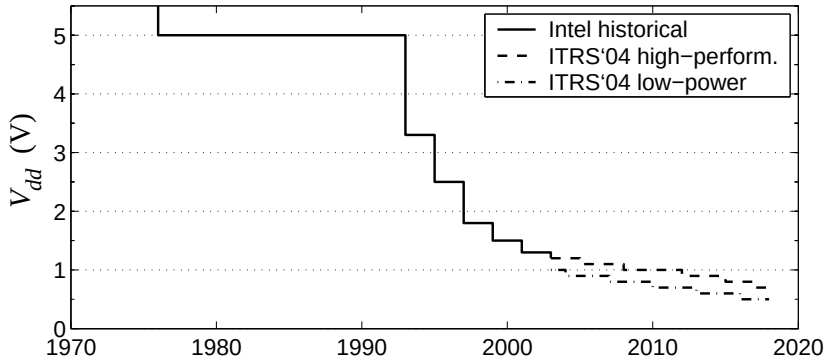
In the past decades semiconductor technology has followed "Moore's law," doubling the number of transistors in digital integrated circuits (IC's) approximately every two years [20]. As a result, IC's have become cheaper, faster, more sophisticated, and more power efficient. This, in turn, has triggered the information technology revolution, making digital processing IC's, such as microprocessors, microcontrollers, digital signal processors (DSP's), graphics processors, and memory chips, ubiquitous in home and professional applications.

A "dark side" of Moore's law is the escalating power consumption and speed of power-level transitions. Fig. 1.1 depicts the power requirement trends of microprocessors, including both historical performance and future trends according to the International Technology Roadmap for Semiconductors (ITRS) [29, 30]. The microprocessor supply voltage (a) is being scaled down to curb the processor power consumption, which is proportional to

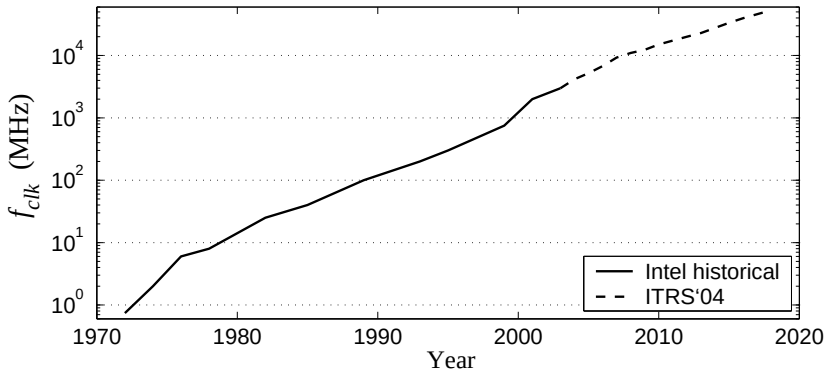
the supply voltage squared [16]. Simultaneously, the clock frequency (b) is increasing exponentially, reflecting the increase of processing speed. As a result of the supply voltage and clock frequency scaling, as well as the exponentially increasing transistor count, the processor supply current (c) is growing dramatically. Another consequence of the increasing clock speeds, power, and chip complexity is the growing processor current slew rate [Fig. 1.1(d)]. The decreasing processor voltage also requires tighter voltage tolerances. Smaller regulation tolerances together with the increasing load currents necessitate very low impedance power delivery [Fig. 1.1(e)].

These scaling trends of digital processing IC's present a set of technical challenges to the power-delivery circuitry, such as conversion efficiency, thermal management, and static and dynamic regulation accuracy. The conversion efficiency is determined by the power train components, the converter topology, and the switching operation mode. The thermal performance is linked to the efficiency, as well as to component packaging, board layout, and cooling strategies. The static regulation accuracy depends on sensing and control component tolerances, as well as possible non-equilibrium behaviors due to feedback non-linearity, as encountered in digital control. The dynamic accuracy depends further on the small-signal and large-signal behavior of the closed-loop converter system.

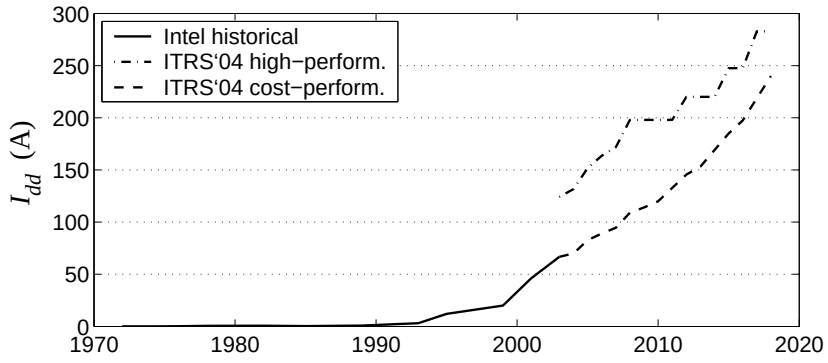
An important factor in the above considerations is manufacturing cost, since many of the end products are sold in very cost competitive mass markets such as consumer electronics. Fig. 1.2 shows a cost breakdown of a microprocessor voltage regulator (VR), and its projected makeup in the future, assuming "business as usual" [114]. Under this scenario, the number of output capacitors is expected to grow dramatically to handle the



(a) Microprocessor supply voltage. (Sources: [106, 114, 29, 30])

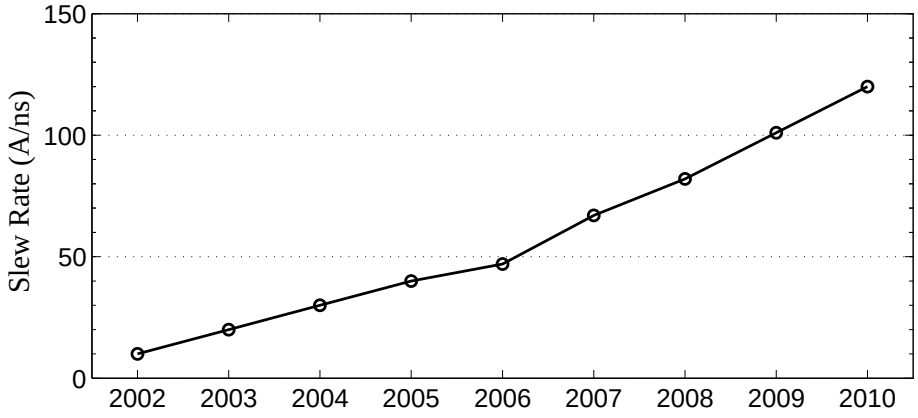


(b) Microprocessor clock frequency. (Sources: [106, 29, 30])

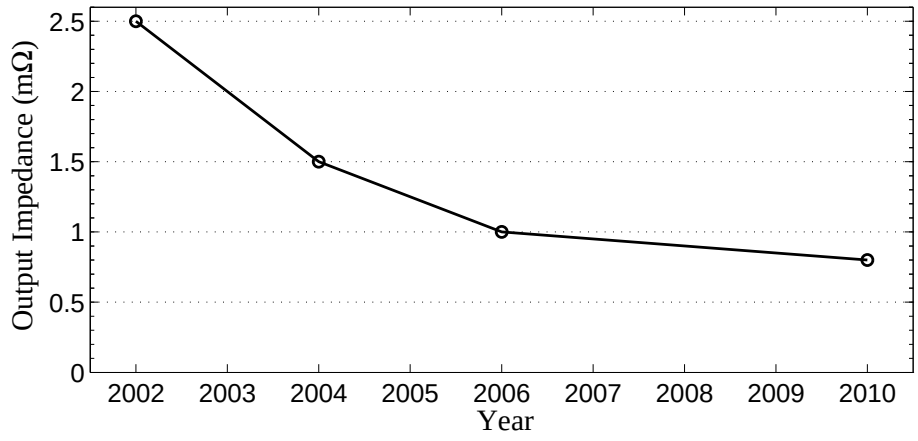


(c) Microprocessor supply current. (Sources: [51, 91, 29, 30])

Figure 1.1: Scaling of microprocessor power requirements: past and future.



(d) Microprocessor current slew rate. (Source: [114])



(e) Microprocessor power supply output impedance. (Source: [44])

Figure 1.1 (Continued)

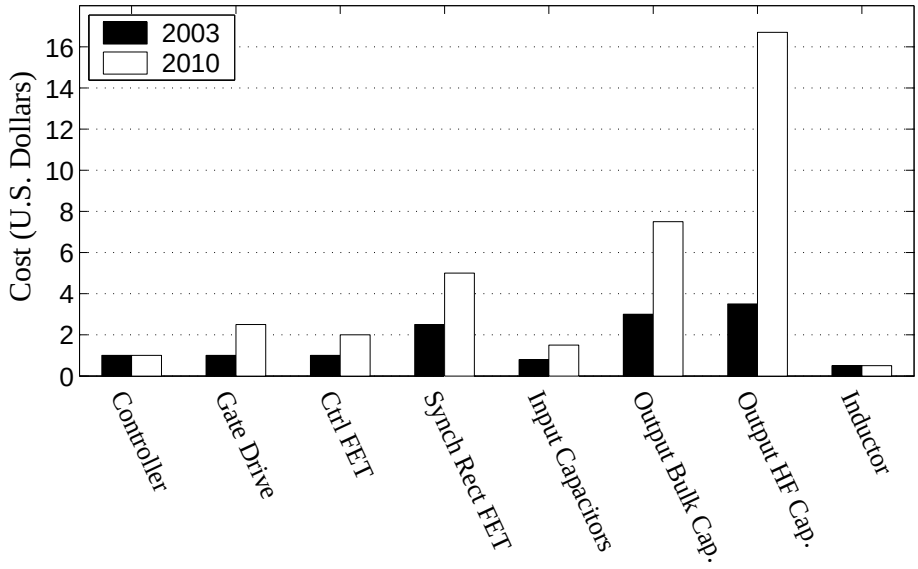


Figure 1.2: Microprocessor voltage regulator cost breakdown, assuming use of present-day multi-phase buck topology in future. (Source: [114])

increasingly violent load transients at low voltages. Further, due to the growing power and transient requirements, the VR is projected to occupy about 30% of a desktop PC motherboard by the end of the decade, compared to about 12% toady [114].

Another aspect is the cost and convenience of operation. Battery life is a critical performance metric for mobile applications, and laptops in particular. PC microprocessors typically spend more than 80% of the time operating at light load (except for servers which run at high load most of the time) [17, 13]. It has been demonstrated that by simple power management techniques at light loads in laptop VR's, such as appropriate load-line control and turning off of the synchronous rectifier, the power consumption can be reduced by some 8% with a corresponding battery life extension [17]. Another, often overlooked, facet of energy efficiency is the electricity cost and environmental impact of PC's. For example, it is estimated that improving the power-supply efficiency of the 205 million PC's in the U.S. could decrease nationwide energy use by 1 to 2% and remove $1 billion or more from yearly electricity bills, while cutting emissions from generating plants [6].

The present thesis develops control architectures and methods to tackle a number of the challenges outlined above: Chapter 2 discusses methods for dynamic voltage regulation, in view of both small-signal and large-signal constraints. These methods can reduce the number of output capacitors necessary in a VR. Chapter 3 addresses digital controller implementations and the associated quantization processes which may induce limit-cycling, adversely affecting the static regulation performance. This work enables small-die-area, power-efficient analog-digital interface blocks for integrated digital controllers. Finally, Chapter 4 develops digital control approaches which optimize the converter efficiency over

a wide load range by adaptively adjusting the switches' timing. This could decrease power consumption and extend battery life. An expanded summary of the chapters' contents is given in Section 1.3.

This thesis concentrates on switching PWM voltage regulators (VR's) which convert a pre-regulated DC voltage (typically 12 V in desktops, and 9 to 19 V in laptops) to the microprocessor supply voltage of about 1 V.[1] However, most of the material developed in this work is relevant in a broader power-converter design framework. The discussions focus on digital controller implementations, with the exception of Chapter 2 which is equally applicable to the analog domain. The advantages offered by digital control are outlined below.

1.2 Potential of Digital Power Management Controllers

Digital power controllers could harness the rapid progress of digital technology to tackle the power management challenges associated with Moore's Law. Fig. 1.3 gives a block diagram of a digital controller for a switching-mode power converter delivering power to a host digital processor. The input power is sourced from the AC power grid, from an AC–DC power supply connected to the power grid, or from a battery. The power is processed by a switching converter so that the output has voltage and impedance characteristics regulated to desired values. The converter uses switches in conjunction with inductors and capacitors to yield ideally lossless voltage level conversion (see, e.g., [28]). The output power is fed to a

[1]Microprocessor voltage regulators (VR's) are differentiated into voltage regulator-down (VRD) and voltage regulator module (VRM), depending on whether they are installed on the PC motherboard (VRD) or on a module that plugs into the motherboard (VRM). For the discussions in the present thesis this distinction is not significant.

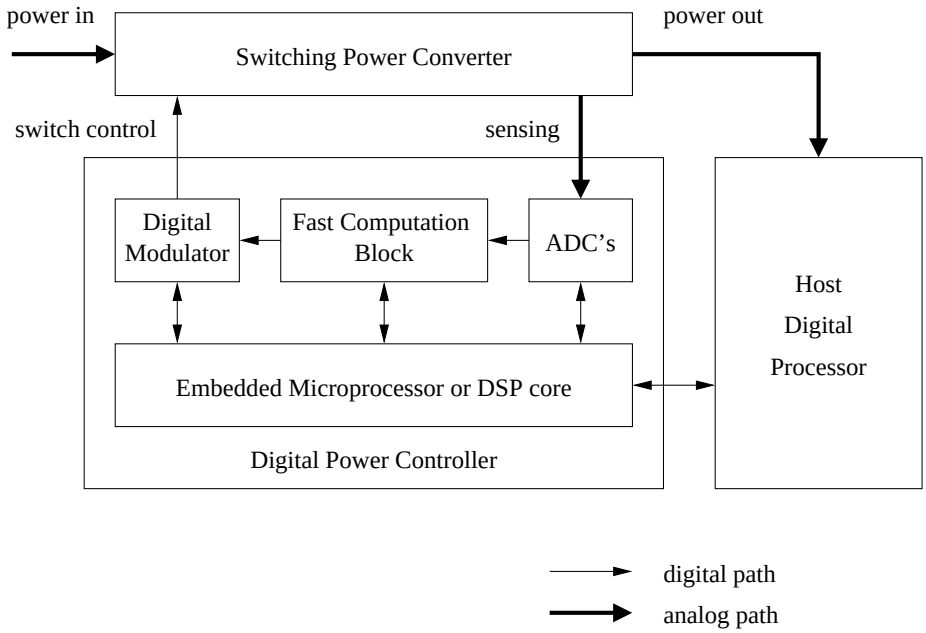


Figure 1.3: Block diagram of a digitally-controlled voltage regulator delivering power to a digital processor.

host digital system which can be a microprocessor, graphics processor, DSP, etc. The digital power controller uses analog-to-digital converters (ADC's) to sample analog power supply variables, such as voltages, currents, and temperature. These quantities are processed by control laws implemented in a fast computational block. The control laws calculate control signals which are converted to switch on/off command sequences by a digital modulator, such as a digital pulse-width modulator (DPWM). An embedded microprocessor or DSP core performs "outer-loop" functions such as control-law adaptation, efficiency optimization, fault diagnostics, communication with the host system, etc. Some salient features of this digital-power-controller architecture are listed below:

Advanced Control Strategies Analog controllers permit only a limited set of standard functions. For example, analog control loops are usually constrained to linear feed-

back methodologies (lead, lag, PID, current-mode) and to linear feedforward control when this is feasible. On the other hand, digital controllers enable the use of advanced control methods which can improve the converter performance in a number of ways: The feedback and feedforward control laws can be adaptively tuned to optimize system performance (see, for example, [8]). In fact, on-line system identification and control-law tuning can reduce the need for application-specific customization and the required human designer expertise. Coupling parameter estimation with feedforward control can provide fast and accurate response to disturbances. Estimators or state observers can be implemented to simplify sensing requirements [37]. Also, efficient but inaccurate sensing methods, such as "lossless current sensing", can be calibrated on-line to improve accuracy [121]. Further, adaptive mode control can be used to maximize efficiency over a wide range of loading conditions and component tolerances (see Chapter 4). Finally, other performance-enhancing functions, such as switching frequency modulation to mitigate electro-magnetic interference (EMI) [98], can be easily programmed in a digital controller. Many of these control methods have been studied academically, and digital control platforms could allow their broad practical application in power management.

Communication with Host System A digital power management controller can facilitate communication with the digital processing system it is supplying. This can effect improvements in power efficiency, transient performance, and fault handling. For example, dynamic voltage scaling is now commonly used in microprocessor systems to improve efficiency [12, 19, 79]. The microprocessor estimates its workload and com-

mands the voltage regulator to adjust the supply voltage, ensuring high throughput at heavy load, and low power at light load. In the future, the microprocessor could also provide a fast, predictive, load-current estimate to the voltage regulator, improving the converter transient response and thus allowing for reduced power train size and cost, as discussed in Chapter 2. Finally digital power management can allow for extensive power-supply fault detection, diagnostics, and recovery functions. The controller can detect a power train fault, report the problem to the host processor, and take corrective actions. In some cases an impending component failure can be predicted from deteriorating power train performance, and preventive steps could be taken to avoid system damage or downtime. For example, in low-end servers the power supplies tend to be oversized to provide better reliability and redundancy, resulting in common operation at only 20 to 30% of the rated load [13]. More intelligent power management could potentially reduce the need for excessive oversizing and thus cut cost and size.

Synthesizability and Programmability A large portion of the digital controller circuitry, except for the analog-digital interface, is synthesizable. Existing computer-aided design (CAD) tools can be used to reduce design effort, facilitate portability to new processes, and hence decrease the time-to-market. Factory or field programmability can eliminate the need for external components and tuning, which traditionally have been used to customize the controller operation, thus reducing cost and footprint, and improving reliability. For example, the recently released Si8250 digital power controller is in-system programmable, and does not require external components [35].

Insensitivity to Component Variation and Noise Analog controllers suffer from component tolerance variation and drift due to ambient conditions and aging. In a digital framework, there is likely to be only one source of tolerance and drift, namely in the sampling (analog-to-digital conversion) process. It is convenient to segregate all the tolerance issues into a single subcircuit, as this effects easier to predict performance and better reliability. A related issue is the sensitivity to noise and disturbances. Again, a digital system is sensitive only at its front-end, whereas an analog system suffers potential problems throughout.

Reduced Power and Area As a result of the dramatic scaling of digital technology, digital power management controllers could offer reduced power and die area in battery-powered hand-held applications like cellular phones, PDA's, and MP3 players. For example, a digital voltage controller for cellular phone applications, occupying only 2 mm^2 active area and having 4 μA quiescent power has been demonstrated in [111], competing strongly with state-of-the-art analog implementations. Although it is generally difficult to compare analog and digital performance metrics, it has been argued, in the context of analog-to-digital converters, that the scaling of CMOS technology will allow for simple analog blocks, backed by sophisticated digital processing, to replace precision analog circuits at a fraction of the area and power [61].

The attractive salient features of digital control have triggered very strong industrial interest, as witnessed at venues such as the Darnell Digital Power Forum in 2004, and the Applied Power Electronics Conference and Exposition in 2005. Recently, both established companies like Texas Instruments, and newer ones like iWatt and Silicon Labs,

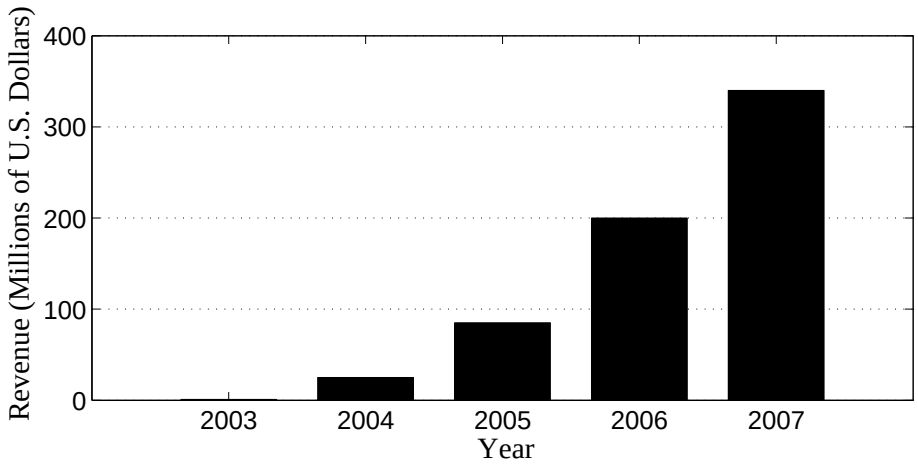


Figure 1.4: Worldwide revenue forecast for digitally-controlled power supplies. Compounded annual growth rate is 277%. (Source: [18])

have introduced highly-integrated, flexible digital power controller chips. The revenue from digitally-controlled power supplies is forecast to increase with an outstanding compounded annual growth rate of 277% (Fig. 1.4) [18]. It is estimated that about 60% of all external AC–DC, telecom DC–DC, and isolated DC–DC supplies will be digitally controlled by 2010 [34]. The emerging practical importance of digital power controllers, and the already ubiquitous use of digital processing IC's is a strong motivation for the work presented here.

Certainly, digital controllers also have some technical limitations. Most significantly, there is delay associated with the sampling process and discrete-time computation. There is generally a tradeoff between the sampling and computation frequency, and the controller power use. Thus, it is beneficial to develop specialized analog-to-digital converter (ADC) architectures which can meet the voltage regulation requirements without excessive power consumption, as discussed in Chapter 3. Importantly, applications requiring very high speed of response ($\sim$ 100 ns) tend to be high-power applications such as servers, where the power overhead of a fast, high-resolution ADC's is negligible. Another issue associated

with digital controller implementations is the possibility of undesirable non-linear system behavior, such as limit-cycling, which may result from quantization in the feedback path. This problem is addressed in Chapter 3 as well.

1.3 Thesis Overview

While all chapters in this thesis address aspects of the design of voltage regulators for digital processing IC's, the three core chapters (2–4) are largely self-contained. An overview of the chapters' contents is given below:

Chapter 2 presents a consistent framework for output impedance control of switching converters, applicable to voltage regulators for digital processing IC's, such as microprocessors. With conventional feedback output-impedance control, the required control-loop bandwidth is inversely proportional to the output capacitor size. On the other hand, the loop bandwidth is limited by the switching frequency due to stability constraints, requiring high switching frequencies when small output capacitance is used. This chapter demonstrates how load-current feedforward can be used to extend the useful bandwidth beyond the limits imposed by feedback stability constraints. In this case, the size of the output capacitor is determined solely by transient and switching-ripple considerations, which are derived in the text. The ability of estimated load-current feedforward to provide tighter output impedance regulation than pure feedback control is demonstrated with simulations and an experimental 12-to-1.3 V, 1 MHz, 4-phase, all-ceramic-capacitor buck converter. Load feedforward is demonstrated to completely eliminate a load-line overshoot of over 50% observed with pure feedback control. This work points to the feasibility of microprocessor VR

implementations using only a small number of ceramic output capacitors, while running at sub-megahertz switching frequencies. The discussion is presented in a continuous-time, analog framework, but is straightforwardly adaptable to the digital, discrete-time domain. Appendix A provides schematics for the simulations.

Chapter 3 discusses digital PWM controller implementations for switching converters, and addresses system stability issues unique to digital control. Suitable architectures of analog-to-digital converters and digital PWM modules are reviewed. The existence of limit cycles in digitally-controlled switching converters is discussed, as well as conditions for their prevention. Digital dither is introduced as a method to increase the effective DPWM resolution, thus preventing limit cycling, and enabling low-power, small-area DPWM implementations. Simulations and experimental results for a 10-to-2.5 V, 250 kHz, 4-phase buck converter are presented, demonstrating the conditions for limit-cycle elimination, and the effectiveness of digital dither to increase the effective DPWM resolution. An order of magnitude reduction of the steady-state output voltage ripple is achieved by using dither to prevent limit cycles. Appendix B gives the simulation and modeling code used.

Chapter 4 develops a multi-mode control strategy which allows for efficient operation of the buck converter over a wide load range. A method for direct control of synchronous rectifiers as a function of the load current is introduced. The function relating the synchronous-rectifier timing to the load current is optimized on-line with a perturbation-based power-loss-minimizing algorithm. Only low-bandwidth measurements of the load current and a power-loss-related quantity are required, making the technique suitable for digital controller implementations. Compared to alternative loss-minimizing approaches, this

method has superior adjustment speed and robustness to disturbances, and can simultaneously optimize multiple parameters (such as the two synchronous-rectifier dead-times). The proposed synchronous-rectifier control also accomplishes an automatic, optimal transition to discontinuous-conduction mode at light loads. It is shown how a similar adaptive scheduling approach can be used to rapidly adjust the duty-ratio in discontinuous-conduction mode, providing fast load-transient response in multi-mode operation. Further, by imposing a minimum duty-ratio the converter will automatically enter pulse-skipping mode at very light loads. Thus, the same controller structure could be used in both fixed-frequency PWM and variable-frequency pulse-skipping modes. These techniques are demonstrated on a digitally-controlled 100 W, 12-to-1.3 V, 375 kHz, 4-phase buck converter, resulting in up to 5% efficiency improvement in fixed-frequency discontinuous-conduction mode. Further, pulse skipping improves the efficiency by 18% at very light load. Finally, it is observed that disabling three of the four phases at light load can increase efficiency by some additional 17%.

Chapter 5 summarizes the contributions of this thesis and suggests directions for future research.

Earlier, partial versions of the technical material in this thesis have been published in a number of venues: Chapter 2 is based on [75, 76], with some earlier results given in [109, 78, 73, 71]. The work in Chapter 3 was developed in [87, 109, 72, 71, 78, 74], and subsequently applied in a low-power IC design in [110, 112, 111]. Chapter 4 is based on [77]. Material from chapters 3 and 4 was also presented in [88].

Chapter 2

Voltage-Regulator Output-Impedance Control with Load-Current Feedforward

2.1 Introduction

The specifications for modern microprocessor voltage regulators (VR's) require that the microprocessor supply voltage follows a prescribed load line with a slope of about one milliohm [19]. This necessitates tight regulation of the VR output impedance. A method for load-line regulation (a.k.a. adaptive voltage positioning), where the closed-loop output impedance is set equal to the output capacitor effective series resistance (ESR), was introduced in [83, 82] and widely adopted. This method allows for the output capacitance to be halved for a given transient regulation window, compared to stiff output regulation.

Load-line regulation based on feedback current-mode control [83, 82, 117] and feedback voltage-mode control with load current injection [78, 120], has been presented, using power trains with electrolytic output capacitors. Most implementations use fixed-frequency PWM control which is well-suited for interleaved multi-phase operation. With this approach, the nominal system closed-loop bandwidth is tightly related to the output capacitor ESR time constant [83, 117, 116]. With common electrolytic capacitors having such a time constant on the order of 3 to 10 μs, it is straightforward for this approach to work with conventional switching frequencies in the range of 200–500 kHz. For modern VR applications, ceramic capacitors present an attractive alternative to electrolytics due to their low ESR and low effective series inductance (ESL), better reliability, low profile, and small footprint. However, ceramic capacitors have ESR time constants between 20 and 200 ns, yielding the conventional load-line design framework unworkable, since it would require switching frequency on the order of 10 MHz [117].

In an effort to improve the performance of feedback load-line control methods, a number of alternative strategies have been proposed. A technique sometimes called "active transient response" turns all phase switches on or off when a "large" error signal with the appropriate sign is detected [66, 73, 60, 15]. This approach increases dramatically the feedback gain for large load transients. However, if the error threshold is too low this could lead to instability or a limit cycle. A related non-linear approach increases the feedback gain when a "large" load transient is detected [24]. These methods are very easy to implement with a digital controller, however the stability and closed-loop performance of the converter are difficult to predict, as is generally the case with strongly non-linear feedback control

methods. Significantly, these methods rely on a large error signal magnitude to effect large control effort, which means that the output voltage has already deviated substantially from the reference, implying poor regulation.

Multi-phase voltage-mode [1] and current-mode [95] hysteretic control has been proposed as an alternative to fixed-frequency PWM control. Hysteretic controllers are not subject to the feedback stability constraints associated with fixed-frequency methods, and can therefore potentially provide a very fast response. In practice, however, the output voltage ripple used to trigger switching in voltage-mode hysteretic control tends to be small in amplitude and noisy, potentially resulting in unpredictable switching frequency variability and irregularity. The same is true for current-mode hysteretic approaches, since the inductor current sensing or estimation produces small-amplitude signals. Importantly, in hysteretic multi-phase converters it is not straightforward to achieve proper phase interleaving, since there is no internal time reference for the phase shifting. N-phase hysteretic controllers can typically be implemented only for duty-ratio ranges (both steady-state and transient) that do not cross the singular-ripple points at $D = \{\ 1/N,\ 2/N,\ \cdots,\ (N-1)/N\ \}$.

Load-current feedforward has been used to speed up the transient response in current-mode converters with stiff voltage regulation [84, 82]. However, in [82] it is suggested that fast feedback compensation can match the performance of load-current feedforward. This may be true for particular converter designs but is not the case in general, as will be argued in this chapter.

In this chapter we present a linear, fixed-frequency, PWM control approach which uses estimated load-current feedforward to effect fast converter response. We establish a

consistent framework for output-impedance regulation design which encompasses the case of the output capacitor ESR being substantially smaller than the desired output impedance. In this case, with feedback control, the required loop bandwidth is inversely proportional to the output capacitor size. Extending the bandwidth can result in cost and board area savings, since it can reduce the required number of capacitors. However, bandwidth in a feedback-controlled converter is limited by stability constraints linked to the switching frequency [117, 116]. We propose and demonstrate the use of load-current feedforward to extend the useful bandwidth beyond the limits imposed by feedback stability constraints. With this approach, feedforward is used to handle the bulk of the regulation action, while feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. In this case, the size of the output capacitor is determined by transient and switching-ripple considerations, and not by the feedback stability constraint. The load current is estimated with lossless inductor and capacitor current sensing. This work points to the feasibility of microprocessor VR's using only a small number of multi-layer ceramic capacitors (MLCC's). The electrolytic bulk capacitors can be eliminated, and the voltage regulation can be fully supported by the ceramic capacitors in and around the microprocessor socket cavity, at sub-megahertz switching frequencies. Reducing the size and count of output capacitors can provide a significant economic benefit, since they make up a substantial fraction of a VR's cost and board footprint, as discussed in Chapter 1.

In Section 2.2 we generalize the load-line impedance to a dynamic quantity which is consistent for capacitor technologies with both large (electrolytic) and small (ceramic) ESR time constants. Section 2.3 reviews feedback load-line control methods, extends them

to a generalized output impedance, and identifies their bandwidth limitations. Section 2.4 introduces load-current feedforward to circumvent the bandwidth limitation of pure feedback control, and derives feedforward control laws for both voltage-mode and current-mode control. Section 2.5 discusses large signal constraints on the converter load-transient performance, and identifies a minimum (critical) capacitance value which can support the load transient. Section 2.6 reviews the inductor current ripple and output voltage ripple in a multi-phase buck converter. Section 2.7 applies the discussion to microprocessor VR design. Section 2.8 compares experimentally the feedback and feedforward control approaches on a 100 W, 12-to-1.3 V, 4-phase buck converter with ceramic output capacitors. Section 2.9 provides a conclusion. The theoretical discussion and experimental results in this chapter are developed in a continuous-time, analog framework. However, they can be straightforwardly adapted to discrete-time, digital controller implementations.

2.2 Output-Impedance Regulation

Fig. 2.1 shows the simplified structure of a representative four-phase buck converter, commonly used in microprocessor VR's (see e.g., [122]). In a multi-phase converter, multiple buck power trains are connected to a common output capacitor and switched with the same duty ratio, but out of phase, which decreases the input-current and output-voltage ripple. For the analysis in this chapter, the multi-phase converter is modeled as an equivalent single-phase converter for simplicity, unless stated otherwise. Conventional load-line control, as used in microprocessor VR applications, sets the desired closed-loop impedance R_{ref} equal to the output capacitor ESR r_C [83]. While this approach works well with capac-

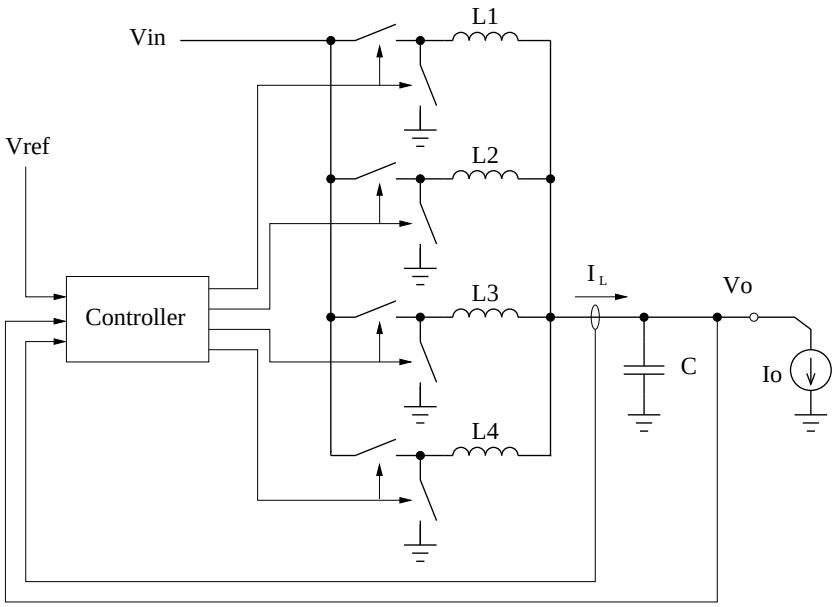


Figure 2.1: Four-phase buck converter. The phases are interleaved at 90° with respect to each other in order to reduce the input-current and output-voltage ripple.

itor technologies with large ESR time constants ($\tau_C = r_C C$), such as electrolytic capacitors, it is not applicable to small ESR time constant technologies, such as ceramic capacitors, due to their small capacitance per unit ESR [117, 116]. With ceramic capacitors, the capacitance C has to be chosen large enough so that it provides adequate ripple filtering and load transient support. Due to the small ESR time constant, this results in the ESR being much less than the desired load-line impedance. Under these circumstances, it is natural to modify the load line so that the output impedance is

$$Z_{ref} \triangleq R_{ref} \frac{1 + s\tau_C}{1 + sR_{ref}C}, \tag{2.1}$$

instead of R_{ref}. Thus, the output voltage has to follow

$$V_o \to V_{ref} - Z_{ref} I_o. \tag{2.2}$$

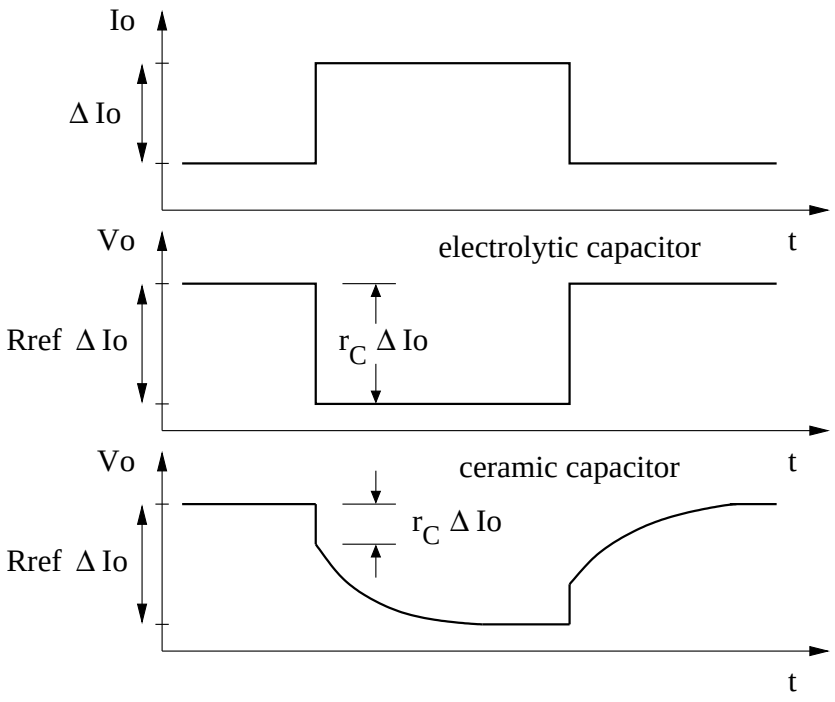


Figure 2.2: Typical current step transient response with load-line regulation, with electrolytic and ceramic capacitors, assuming no duty ratio saturation occurs.

This behavior is illustrated in Fig. 2.2. With this approach the output impedance is specified dynamically, as a generalization of the resistive output impedance in conventional load-line control. In the low-frequency limit, the output impedance is equal to R_{ref}, and in the high-frequency limit—to r_C. Importantly, the controller has to be designed so that the output impedance is regulated to Z_{ref} and not to R_{ref}, since the latter approach will result in undesirable behavior: During a load transient the controller will initially act to change the inductor current in direction *opposite* to the load step, eventually producing additional output voltage overshoot. Finally, note that this load-line impedance paradigm would be consistent with an ideal capacitor with zero ESR, where $\tau_C = 0$.

2.3 Feedback Control Approaches and Their Limitations

Traditionally, feedback control approaches have been used to implement load-line regulation. Here we review these methods, extend them to the generalized impedance regulation described in Section 2.2, and identify their bandwidth limitations.

2.3.1 Switching Stability Constraint

In fixed-frequency switching converters with feedback control there is a fundamental limit on the loop-gain bandwidth which results in stable closed-loop operation. In particular, feedback bandwidth which approaches or exceeds the switching frequency may result in non-linear behaviors such as period-doubling or chaos [9]. This stability constraint can be expressed as

$$f_c < \alpha f_{sw}, \tag{2.3}$$

where f_c is the feedback unity-gain frequency, and α is a constant. According to [25] the fundamental upper limit for naturally-sampled, triangle carrier PWM is $\alpha = 1/3$. For practical designs $\alpha = 1/6$ is recommended in [117]. In an interleaved N-phase buck converter the stable bandwidth can potentially be extended by N times, due to the reduced modulation delay [81]. However, in the presence of parameter mismatches among the phase legs, aliasing effects at the switching frequency may reduce the usable bandwidth [81]. Thus, (2.3) with $\alpha = 1/6$ stands as a practical stability guideline, with the understanding that for multi-phase designs it may be on the conservative side.

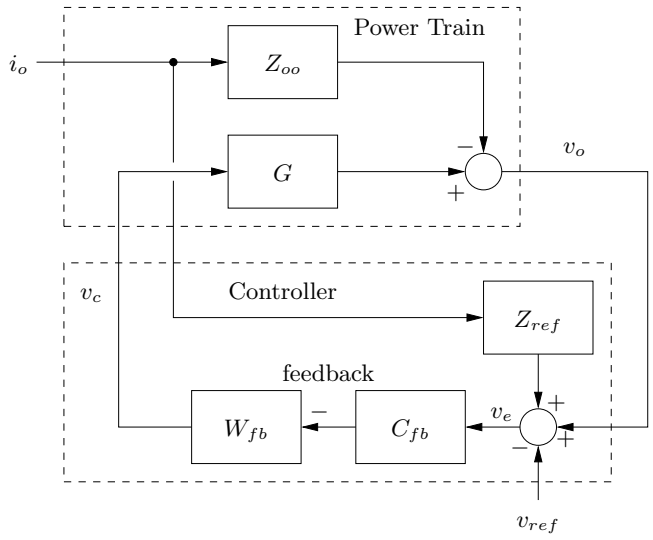


Figure 2.3: Load-line feedback block diagram with voltage-mode control.

2.3.2 Load-Line Feedback

This approach is based on the understanding that if an error signal, formed by subtracting the desired load-line trajectory from the output voltage, is fed to a high gain feedback controller, the output voltage will track the load line. This method was discussed in [78], and replicated in [120]. Similar approaches have been used in a number of commercial IC's. It can be used with both voltage-mode and current-mode control.

A block diagram of the load-line feedback scheme with a voltage-mode controller is shown in Fig. 2.3. Here,

$$G(s) = \frac{sr_C C + 1}{s^2 LC + s(r'_L + r_C)C + 1} \tag{2.4}$$

is the averaged transfer function between the controller command and the output voltage, $L = L_\phi/N$ is the total power train inductance for an N-phase converter, and r'_L is the series combination of the total inductor resistance and the average switch and input source

resistance. The averaging method used to derive this and the following transfer functions is commonly used to model switching converters, and is discussed in [38, Ch. 11] and [28, Ch. 7], for example. The open-loop output impedance is

$$Z_{oo}(s) = \frac{r'_L(sr_CC+1)(sL/r'_L+1)}{s^2LC + s(r'_L+r_C)C+1}. \tag{2.5}$$

The feedback controller uses a standard PID control law, with an extra high-frequency pole $1/\tau_C$ which ideally cancels the capacitor ESR zero,

$$C_{fb}(s) = K\left(1+\frac{1}{T_Is}+T_Ds\right)\frac{1}{s\tau_C+1}. \tag{2.6}$$

The derivative term zero and the $1/\tau_C$ pole provide a -20 dB/dec rolloff above the LC cutoff frequency, to ensure a good phase margin. Conventional design procedures can be used to choose the PID parameters to yield good phase and gain margins [28, Ch. 9]. The high-frequency dynamics of the feedback loop are modeled by

$$W_{fb}(s) = e^{-st_{d,fb}}, \tag{2.7}$$

where $t_{d,fb}$ lumps the effective delay of the modulator, the gate drivers, and the power switches.

From Fig. 2.3 the converter closed-loop output impedance is calculated to be

$$Z_o = Z_{ref}\frac{Z_{oo}/Z_{ref} + GW_{fb}C_{fb}}{1+GW_{fb}C_{fb}}. \tag{2.8}$$

Clearly, $Z_o \to Z_{ref}$ for large values of the loop gain $GW_{fb}C_{fb}$, as desired. In particular, it can be shown from (2.8) that

$$Z_o \to Z_{ref} \qquad \text{for} \qquad f_c \gg \frac{1}{2\pi R_{ref}C}, \tag{2.9}$$

where f_c is the loop unity-gain bandwidth. To avoid closed-loop instabilities, the loop bandwidth should not exceed approximately one-sixth of the switching frequency, as required by equation (2.3) in Section 2.3.1. For a given switching frequency, the output capacitor should then be selected sufficiently large to meet this constraint. Therefore, with this control approach, there is a trade-off between the number of output capacitors required and the switching frequency used.

2.3.3 Voltage Feedback with Finite DC Gain

This approach is based on the observation that a power converter with finite, non-zero DC feedback gain has a finite, non-zero closed-loop output impedance. Thus, by appropriate selection of the feedback control law, the converter closed-loop output impedance can be set to a particular value. This approach is readily implementable with current-mode control, while its use with voltage-mode control is not practical [117]. This method, developed for the special case of the output impedance equal to the output capacitor ESR, was introduced in [83]. In the discussion below it is extended to the control of a general output impedance Z_{ref}, as defined in (2.1).

Fig. 2.4 gives the model of a buck converter with a current-mode controller. Parameter I_c is the current command provided by the voltage (outer) control loop, and R_I is the effective current-loop gain. The current-loop gain is modeled as

$$R_I = F_m V_{in} = \frac{V_{in}}{M_c T}, \tag{2.10}$$

where M_c is the compensation ramp slope, and $T = 1/f_{sw}$ is the switching period [96],[28, Ch. 12]. Without a compensation ramp ($M_c = 0$), the effective current-loop gain is infinite

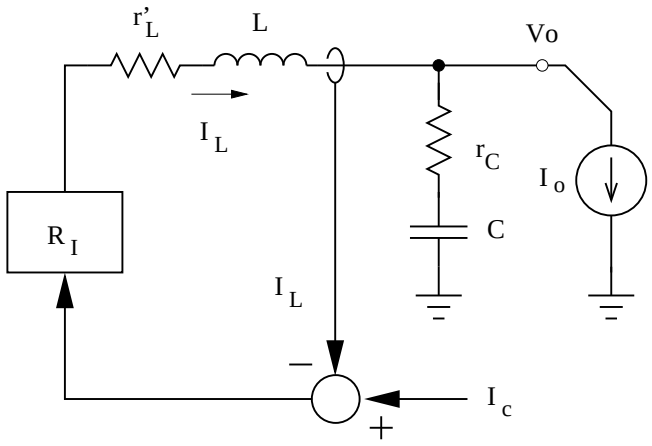


Figure 2.4: Model of current modulator with current (inner) loop closed.

($R_I \to \infty$), reflecting the sliding-mode nature of the current loop.

Fig. 2.5 shows a control block diagram of the complete controller. The transfer function between the current command and the output voltage, with the current-loop closed, is

$$\mathcal{G}(s) = \frac{NR_I(sr_CC + 1)}{s^2LC + s(R_I + r'_L + r_C)C + 1}, \tag{2.11}$$

where N is the number of phases. The corresponding open-voltage-loop output impedance is

$$\mathcal{Z}_{oo}(s) = \frac{(R_I + r'_L)(sr_CC + 1)\left(s\frac{L}{R_I + r'_L} + 1\right)}{s^2LC + s(R_I + r'_L + r_C)C + 1}. \tag{2.12}$$

Note that for high current-loop gain R_I, both (2.11) and (2.12) become independent of the inductor value L, since the current loop provides for this desensitivity [28, Ch. 12]. Finally, the closed-loop output impedance of the converter is

$$\mathcal{Z}_o = \frac{\mathcal{Z}_{oo}}{1 + \mathcal{G}\mathcal{W}_{fb}Y_{fb}}, \tag{2.13}$$

where parameter $\mathcal{W}_{fb}(s)$ models the loop delay, and Y_{fb} is the feedback control law.

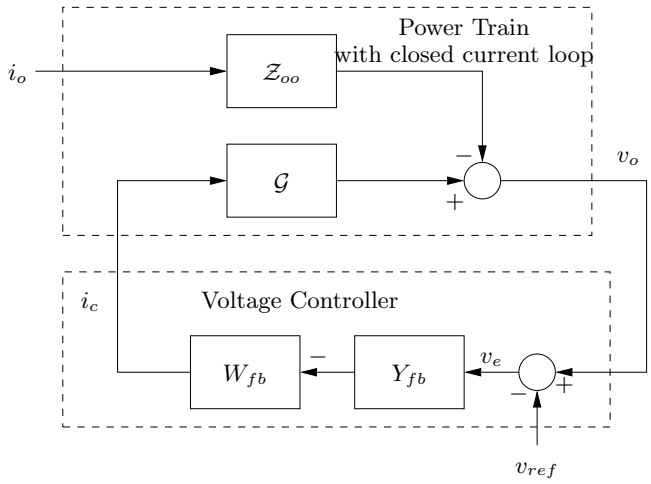


Figure 2.5: Block diagram of current-mode load-line control with finite DC gain compensator Y_{fb}.

Assuming a high value of the current-loop gain ($R_I \to \infty$), ignoring the high-frequency dynamics ($\mathcal{W}_{fb} = 1$), and requiring $\mathcal{Z}_o = Z_{ref}$, we obtain the feedback control law

$$Y_{fb} = \frac{1}{NR_{ref}(1 + s\tau_C)}, \tag{2.14}$$

which is consistent with the derivation for the case of $R_{ref} = r_C$ in [83]. Under this control law, the voltage-loop unity gain bandwidth is

$$f_c = \frac{1}{2\pi R_{ref} C}. \tag{2.15}$$

Further, the loop bandwidth should be well below the switching frequency to avoid instabilities, as required by equation (2.3) in Section 2.3.1. Therefore, with this control approach too there is a trade-off between the number of output capacitors required and the switching frequency. Indeed, for the case $R_{ref} = r_C$, equation (2.15) has been previously identified as a critical bandwidth which constrains the choice of switching frequency [117, 116].

Finally, it should be pointed out that when used with peak or valley current control

schemes, this method incurs a DC output voltage offset. Since the feedback loop controls the peak or valley inductor current rather than the average current in each phase, the output voltage is shifted from the reference load line by $NR_{ref}\Delta I_{L\phi,p-p}/2$, where $\Delta I_{L\phi,p-p}$ is the peak-to-peak phase current ripple. This problem can be remedied by appropriately adding a slow integrator to force the *average* phase inductor current to equal the current command I_c.

2.4 Load-Current Feedforward Control

In contrast to the feedback control approaches discussed above, load-current feedforward can eliminate the stability constraint linking the size of the output capacitor and the switching frequency. Since, ideally, the load current is an exogenous variable rather than a state variable, *the gain and bandwidth of the feedforward are not limited by stability considerations* [7, Ch. 7]. The problem of V_o following accurately the load line defined by (2.2) can be approached as a reference tracking problem. An effective approach in tracking problems is to use feedforward from the reference signal (the load current I_o in this case) to the controller output (the PWM duty ratio) to handle the bulk of the regulation action, and use the feedback only to damp resonances, and compensate for the imperfections of the feedforward [90, Ch. II.3],[7, Ch. 7]. Load-current feedforward can be used with both voltage-mode and current-mode impedance control, and small-signal feedforward laws for both cases are derived in this chapter.

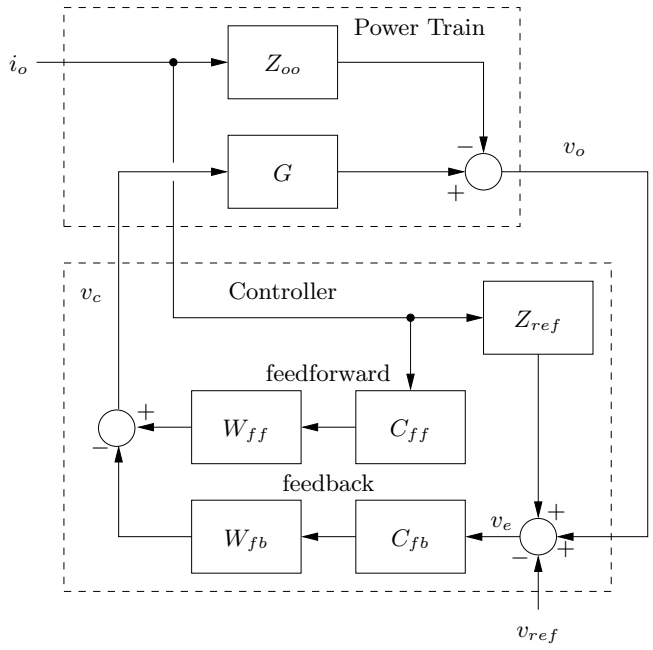


Figure 2.6: Voltage-mode load-line control block diagram with load-current feedforward.

2.4.1 Voltage-Mode Control

Fig. 2.6 shows a block diagram of the buck converter with voltage-mode load-line control from Fig. 2.3 with an added load-current feedforward path. Here C_{ff} is the feedforward control law, and

$$W_{ff}(s) = e^{-st_d} \tag{2.16}$$

models the delay of the feedforward path. The closed loop output impedance is

$$Z_o = \frac{Z_{oo} + G(Z_{ref}W_{fb}C_{fb} - W_{ff}C_{ff})}{1 + GW_{fb}C_{fb}}. \tag{2.17}$$

The feedforward control law can be derived by setting the closed-loop output impedance (2.17) equal to the desired value Z_{ref}, yielding

$$C_{ff}(s) \triangleq \frac{Z_{oo} - Z_{ref}}{W_{ff}G}. \tag{2.18}$$

Note that if the ideal feedforward in (2.18) could be implemented, the output impedance would have the desired value $Z_o = Z_{ref}$ and no feedback is necessary. In reality, this is impossible due to parameter uncertainties and the fact that W_{ff} contains delay, thus C_{ff} would be anticausal. A practical implementation C'_{ff} can approximate C_{ff} with an error δC_{ff},

$$C'_{ff} = C_{ff} + \delta C_{ff}. \tag{2.19}$$

Then the output impedance (2.17) becomes

$$Z_o = Z_{ref}\left(1 - \frac{\delta C_{ff}}{C_{ff}} \cdot \frac{Z_{oo}/Z_{ref} - 1}{1 + GW_{fb}C_{fb}}\right). \tag{2.20}$$

Thus, the feedforward carries out the bulk of the regulation action, and the feedback acts only to decrease the feedforward non-ideality. In particular, at low frequencies the uncertainty term in (2.20) approaches zero due to the high feedback gain, while at very high frequencies it is attenuated by Z_{oo}/Z_{ref} approaching unity.

Expanding (2.18) yields the exact expression for the feedforward law,

$$\begin{aligned} C_{ff}(s) = \Big\{ & s^2 LCr_C\,(1 - \tau_C R_{ref}/L) + \\ & + s\big[L + \tau_C(r'_L - 2R_{ref})\big] + r'_L - R_{ref}\Big\}\Big/ \\ & \Big/\Big\{(s\tau_C + 1)(sR_{ref}C + 1)W_{ff}(s)\Big\}. \end{aligned} \tag{2.21}$$

Noting that typically $L/R_{ref} \gg \tau_C$ and $L \gg |\tau_C(r'_L - 2R_{ref})|$, and further ignoring the delay term and the DC term, since DC regulation is handled by the integral feedback, the feedforward law can be approximated as

$$C_{ff}(s) \approx \frac{sL}{sR_{ref}C + 1}. \tag{2.22}$$

Thus, the design of the feedforward law with voltage-mode control requires an estimate of the power train inductance and output capacitance. The sensitivity of the feedforward control law to the accuracy of the relevant power-train parameter estimates may vary. For example, equation (2.22) may be more sensitive to the inductance estimate, which sets the gain, than the capacitance estimate. The requirement for reasonably accurate estimates of power-train parameters could be a drawback of the feedforward technique, however adaptive tuning of the feedforward law could resolve the issue. The adaptation aspect is not developed here, but it is recommended for future research in Section 5.2.2.

2.4.2 Current-Mode Control

The same load-current feedforward control approach can be used with current-mode control. The block diagram of the system, with the current (inner) loop closed, has the same structure as that in Fig. 2.6, except now the voltage-loop controller generates a current command which is fed to the current controller. The transfer function between the current command and the output voltage, with the current-loop closed, is given by (2.11). The open-loop output impedance is given by (2.12). The feedforward control law is derived analogously to that in the voltage-mode case,

$$\begin{aligned} \mathcal{C}_{ff}(s) = \Big\{ & s^2 LCr_C \left(1 - \tau_C R_{ref}/L\right) + \\ & + s\big[L + \tau_C(R_I + r'_L - 2R_{ref})\big] + R_I + r'_L - R_{ref} \Big\} \Big/ \\ & \Big/ \Big\{ N R_I (s\tau_C + 1)(sR_{ref}C + 1)\mathcal{W}_{ff}(s) \Big\}. \end{aligned} \tag{2.23}$$

Assuming high current-loop gain ($R_I \to \infty$) and ignoring the delay term ($\mathcal{W}_{ff} = 1$), the feedforward law can be approximated by

$$\mathcal{C}_{ff}(s) \approx \frac{1}{N(sR_{ref}C + 1)}. \tag{2.24}$$

The feedback control can use a PI law,

$$\mathcal{C}_{fb}(s) = \frac{\mathcal{K}}{N}\left(1 + \frac{1}{\mathcal{T}_I s}\right)\frac{1}{s\tau_C + 1}, \tag{2.25}$$

since current-mode control provides a -20 dB/dec rolloff up to the current-loop bandwidth, and hence no derivative term is necessary. The integral term may be necessary to provide infinite DC loop gain in the cases when the load has finite impedance or a compensation ramp is used, which limit the voltage loop DC gain. One major advantage of current-mode control is that, unlike the voltage-mode case, no precise knowledge of L is needed for the design of $\mathcal{C}_{ff}$ and $\mathcal{C}_{fb}$, thus allowing for more robust controller designs.

2.5 Large-Signal Considerations: Critical Capacitance

During large load current transients the inductor current slew rate is limited by the supply rails. The maximum voltage magnitude which can be imposed across the inductor is

$$V_L^* = \begin{cases} V_{in} - V_{ref}, & \text{for loading step,} \\ V_{ref} - R_{ref}I_o, & \text{for unloading step.} \end{cases} \tag{2.26}$$

Here we are ignoring the inductor and switch resistances, which will decrease V_L^* for the loading step, and increase it for the unloading step, by a small amount. If tight regulation is required, the output voltage should not overshoot from the specified load line during large

load transients. This requirement constrains the power filter components. In particular, for a given total (all phase inductors in parallel) inductance value, there is a minimum output capacitance value (critical capacitance) for which this requirement is met.

The original derivation of the critical capacitance [83, 82] assumes that the load line impedance is equal to the output capacitor ESR ($Z_{ref} = r_C$). As discussed in Section 2.2, this design choice is typical for converters using electrolytic output capacitors, however, it is not practical with ceramic output capacitors. Here we derive the critical capacitance for a general output impedance as defined in equation (2.1) of Section 2.2. Further, the results presented here incorporate the controller delay and the load current slew rate, as well as permissible load-line overshoot, which have not been previously accounted for.

2.5.1 Critical Capacitance Derivation

Fig. 2.7 shows a model of the buck converter response for a large unloading transient. The unloading current step can be modeled by a magnitude ΔI_o and a time constant τ_I which characterizes the slew rate,

$$I_o(t) = I_o(0) - \Delta I_o(1 - e^{-t/\tau_I}), \tag{2.27}$$

for $t \geq 0$.

Following the load step at $t = 0$, the controller reacts after some delay t_d inherent to a physical implementation (Fig. 2.7). Before the controller has reacted, for $0 \leq t < t_d$, the inductor current remains approximately at its initial value $I_L \approx I_o(0)$, since the output voltage practically stays constant. Then, the capacitor current is

$$I_C(t) = I_L - I_o(t), \tag{2.28}$$

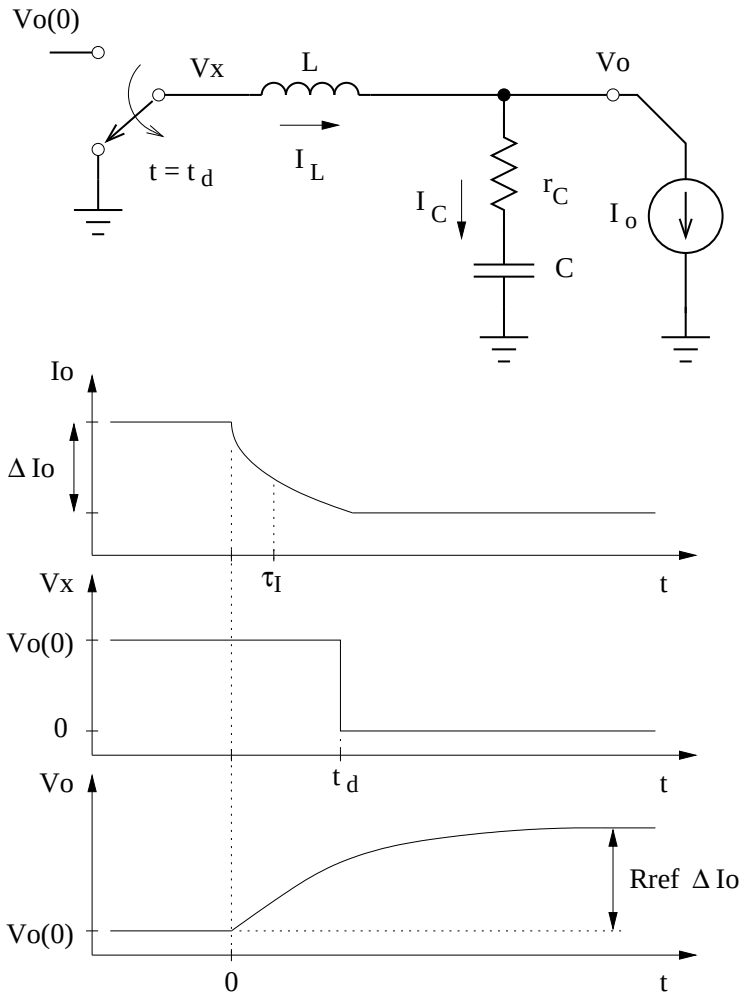


Figure 2.7: Buck converter transient response model for a large unloading current step.

and the capacitor voltage is

$$V_C(t) = \frac{1}{C}\int_0^t I_C(t')dt' + V_o(0), \tag{2.29}$$

where

$$V_o(0) = V_{ref} - R_{ref}I_o(0). \tag{2.30}$$

The output voltage is then

$$\begin{aligned} V_o(t) &= V_C(t) + r_C I_C(t) \\ &= \frac{\Delta I_o}{C}\left[t + (\tau_C - \tau_I)\left(1 - e^{-t/\tau_I}\right)\right] + V_o(0), \end{aligned} \tag{2.31}$$

for $0 \leq t < t_d$.

After the delay, the maximum control effort the controller can exert is to saturate the duty ratio to zero. Thus, for $t \geq t_d$, the inductor voltage is

$$\begin{aligned} V_L(t) &= -V_o(t) \\ &\approx -V_{ref} + R_{ref} I_o(t) \\ &\approx -V_{ref} + R_{ref}(I_o(0) - \Delta I_o) \\ &\triangleq -V_L^*, \end{aligned} \tag{2.32}$$

ignoring the load current time constant ($\tau_I = 0$). These approximations are reasonable, since under duty ratio saturation $V_L(t)$ is dominated be the constant V_{ref}. The inductor current is then

$$I_L(t) = \Delta I_o - V_L^*(t - t_d)/L. \tag{2.33}$$

Thus, the output voltage is

$$V_o(t) = \frac{\Delta I_o}{C}\left[t - \frac{1}{2t_L}(t - t_d)^2 - \frac{\tau_C}{t_L}(t - t_d) + (\tau_C - \tau_I)\left(1 - e^{-t/\tau_I}\right)\right] + V_o(0), \tag{2.34}$$

for $t \geq t_d$, where $t_L = L\Delta I_o / V_L^*$.

We require that the output voltage does not exceed the load-line specification,

$$V_o(t) \leq V_o(0) + R_{ref}\Delta I_o. \tag{2.35}$$

Since the maximum voltage value $max(V_o)$ is reached at time $t_{max} \geq t_d$, the critical capacitance can be derived from (2.34), by setting

$$max(V_o) \triangleq V_o(0) + R_{ref}\Delta I_o. \tag{2.36}$$

The time t_{max} when the maximum voltage value is reached, can be obtained by setting the first derivative of (2.34) to zero, and solving for t,

$$\frac{dV_o(t)}{dt} = \frac{\Delta I_o}{C}\left[1 - \frac{1}{t_L}(t - t_d + \tau_C) + \left(\frac{\tau_C}{\tau_I} - 1\right)e^{-t/\tau_I}\right] \triangleq 0. \tag{2.37}$$

The above equation is transcendental, and thus an analytical solution for t cannot be derived. In the general case, t_{max} can be obtained by solving (2.37) numerically. However, for the case of high slew rate load steps (small τ_I), which are most challenging in practice, the exponential term in (2.37) has negligible contribution to the solution t_{max}, and can therefore be ignored. Further, the maximum voltage cannot physically occur before time t_d, thus

$$t_{max} \approx \begin{cases} t_d, & \text{for} \quad L \leq L_{crit}, \\ t_d + t_L - \tau_C, & \text{for} \quad L > L_{crit}, \end{cases} \tag{2.38}$$

where $L_{crit} = \tau_C V_L^* / \Delta I_o$.

Combining (2.34) and (2.37) to eliminate the exponential term, and substituting t_{max} for t, yields an expression for $max(V_o)$. Inserting the result in (2.36) and solving for C we obtain

$$C_{crit} = \frac{1}{R_{ref}}\left[t_{max} + \tau_C - \frac{(t_{max} - t_d)^2}{2t_L} - \frac{(\tau_C + \tau_I)(t_{max} - t_d) + \tau_C\tau_I}{t_L}\right]. \tag{2.39}$$

Substituting the approximate value of t_{max} from (2.38) in the above expression yields

$$C_{crit} \approx \begin{cases} (\tau_C + t_d - \tau_I) \Big/ R_{ref}, & \text{for} \quad L \leq L_{crit}, \\ \left(\frac{t_L}{2} + \frac{\tau_C^2}{2t_L} + t_d - \tau_I\right) \Big/ R_{ref}, & \text{for} \quad L > L_{crit}. \end{cases} \tag{2.40}$$

Due to the low conversion ratio (≤ 0.1) in modern VR's, the critical capacitance for unloading transients is much larger than that for loading transients. Therefore, the output voltage is allowed to overshoot by some amount ΔV_{os} above the defined load line during unloading transients, thus reducing the output capacitor requirement [19]. The allowed overshoot ΔV_{os} can be added on the right-hand side in equations (2.35) and (2.36). This results in a critical capacitance value which is less stringent than (2.40),

$$C_{crit} \approx \begin{cases} (\tau_C + t_d - \tau_I) \Big/ (R_{ref} + \Delta V_{os}/\Delta I_o)\,, & \text{for} \quad L \leq L_{crit}, \\ \left(\frac{t_L}{2} + \frac{\tau_C^2}{2t_L} + t_d - \tau_I\right) \Big/ (R_{ref} + \Delta V_{os}/\Delta I_o)\,, & \text{for} \quad L > L_{crit}, \end{cases} \tag{2.41}$$

where $t_L = L\Delta I_o/V_L^*$ and $L_{crit} = \tau_C V_L^*/\Delta I_o$. Expression (2.41) yields two values for the critical capacitance—one for the loading, and one for the unloading transient—which typically have different V_L^*, as shown in (2.26). The larger critical capacitance value should be used in design. The quantity L_{crit} has been identified as a critical inductance value, below which the output voltage transient is independent of the inductance value [78, 104, 117]. In [78, 104, 117] it is suggested that the converter total inductance should be designed to match this critical inductance value. This is readily implementable in designs using electrolytic capacitors, which have a large ESR time constant. However, it is clear that for capacitor technologies with a small ESR time constant, such as ceramic capacitors, this design choice implies impractically small inductor values. The result in (2.41) presents a consistent framework for transient design with inductances above the critical value. It indicates that for designs with a small capacitor ESR time constant, where typically $L > L_{crit}$, reducing the inductance value is beneficial, from a transient performance perspective, since this decreases the required output capacitance via parameter t_L. These results also show how the converter delay and the load current slew rate affect the capacitance choice: Larger

controller delay and load slew rate require larger output capacitance to handle the transient. Finally, this derivation assumes that the inductor current ripple is small compared to the full load step. A discussion of the effect of large inductor current ripple on transient performance can be found in [54].

2.6 Switching Ripple Considerations

The switching ripple constrains the power train design with regard to both regulation performance and efficiency. The peak-to-peak inductor current ripple of a single phase is

$$\Delta I_{L\phi,p-p} = \frac{V_{in}TD(1-D)}{L_\phi}, \tag{2.42}$$

[28, Ch. 2]. The inductor current ripple incurs conductive and core losses which may aggravate the conversion efficiency, and limit high-frequency performance [28, Ch. 13]. The total-inductor-current (sum of all inductor currents) ripple of an N-phase interleaved buck converter can be shown to be

$$\Delta I_{L,p-p} = \frac{V_{in}TD^*(1-ND^*)}{L_\phi}, \tag{2.43}$$

where $D^* = mod(D, 1/N)$. The total-inductor-current ripple frequency is Nf_{sw}. The total-inductor-current ripple (2.43) results in voltage ripple across the output capacitor and its ESR. The output voltage ripple can be calculated by summing the magnitudes of the capacitor and ESR ripples, yielding

$$\Delta V_{o,r,p-p} = \frac{\Delta I_{L,p-p}}{C}\sqrt{\left(\frac{T}{8N}\right)^2 + \tau_C^2}. \tag{2.44}$$

Table 2.1: Sample Microprocessor VR specifications

V_{in}	input voltage	12 V
V_{ref}	reference output voltage	1.2 V
$I_{o,max}$	max. load current	78 A
ΔI_o	max. dynamic load step	55 A
τ_I	load step time constant	85 ns
R_{ref}	closed-loop output impedance	1.4 mΩ
ΔV_o	output tolerance band	$\pm$ 25 mV
ΔV_{os}	max. extra unloading overshoot	50 mV
Δt_{os}	max. extra overshoot duration	25 μs

Source: [19]

Note that expression (2.44) does not include the ripple contribution due to the output capacitor effective series inductance (ESL). The ESL depends strongly on the capacitor packaging and circuit layout, and should be reduced as much as possible [93, 94]. Since the output voltage ripple affects the regulation performance, it can be yet another factor constraining the choice of output capacitor. Finally, note that while the interleaved multiphase operation reduces the output voltage ripple (2.44), it does not affect the inductor current ripple in the individual phases (2.42), in a conventional, uncoupled inductor design.

2.7 Application to Microprocessor Voltage Regulators

Load line regulation is adopted as a standard control method in microprocessor VR's [19]. Hence, the discussion above can be applied directly to the design of VR's.

2.7.1 Design for Low-Conversion Ratio

The low conversion ratio required in modern VR's (currently at 1.2 V / 12 V, and going down) presents a challenge since both fast response and high efficiency are required. Decreasing the inductor value increases the speed of response, however this also increases the inductor current ripple and the resulting power loss. On the other hand, if a large inductor is used, the output capacitor has to be made large, to sustain the load line during transients, as indicated by (2.41). Increasing the capacitor count drives up the VR cost and footprint. To alleviate the problems associated with low-conversion ratios, a number of modifications to the basic multi-phase synchronous buck topology have been introduced. These are briefly discussed below:

- A two-stage approach [85] uses a two-phase buck converter to create an intermediate 5 V bus, followed by a four-phase buck stage which converts this voltage down to 1.2 V. An improved overall efficiency is reported, at the expense of an increased component count and control complexity.

- Various tapped-inductor buck topologies have been proposed to improve the low-conversion ratio performance [113, 115, 103]. However, the leakage inductance associated with these structures contributes losses, limiting the performance at high frequencies.

- An approach termed "body braking" turns off the synchronous rectifier (low-side) switch when the duty-ratio command goes to zero, forcing conduction through the body diode [21]. That way, the switching node voltage swings to a diode drop V_D

below ground, increasing the voltage drop across the inductor. With this approach, the unloading V_L^* in (2.26) is increased to $V_L^* + V_D$, reducing the unloading critical capacitance. A potential drawback is that part of the unloading energy is dissipated in the body diode.

- Appropriately coupling the phase inductors in a multi-phase converter allows for the total inductance to be decreased, without incurring a large inductor current ripple, thus reducing the critical capacitance [105, 47, 46]. Ideally, the inductor current in all phases is identical, $\Delta I_{L\phi,p-p} = \Delta I_{L,p-p}/N$, where $\Delta I_{L,p-p}$ is defined in (2.43). This method has been demonstrated to improve the converter performance even with asymmetric phase coupling associated with a practical converter layout [46].

- An "active clamp" approach uses a linear regulator in parallel with the switching converter output to source or sink current during large transients [107, 10, 119]. This reduces the number of output capacitors required, however it can incur significant power losses in the presence of a frequently varying load, such as a microprocessor.

- An "inductive clamp" approach uses an additional small inductor connected to the output to increase the total inductor current slew rate during large unloading transients [73]. The inductor is switched to ground when the duty-ratio command goes below zero, and is subsequently discharged to the input supply rail, ideally handling the excess transient energy losslessly. This approach requires an extra phase leg, and its efficiency may be limited in practice.

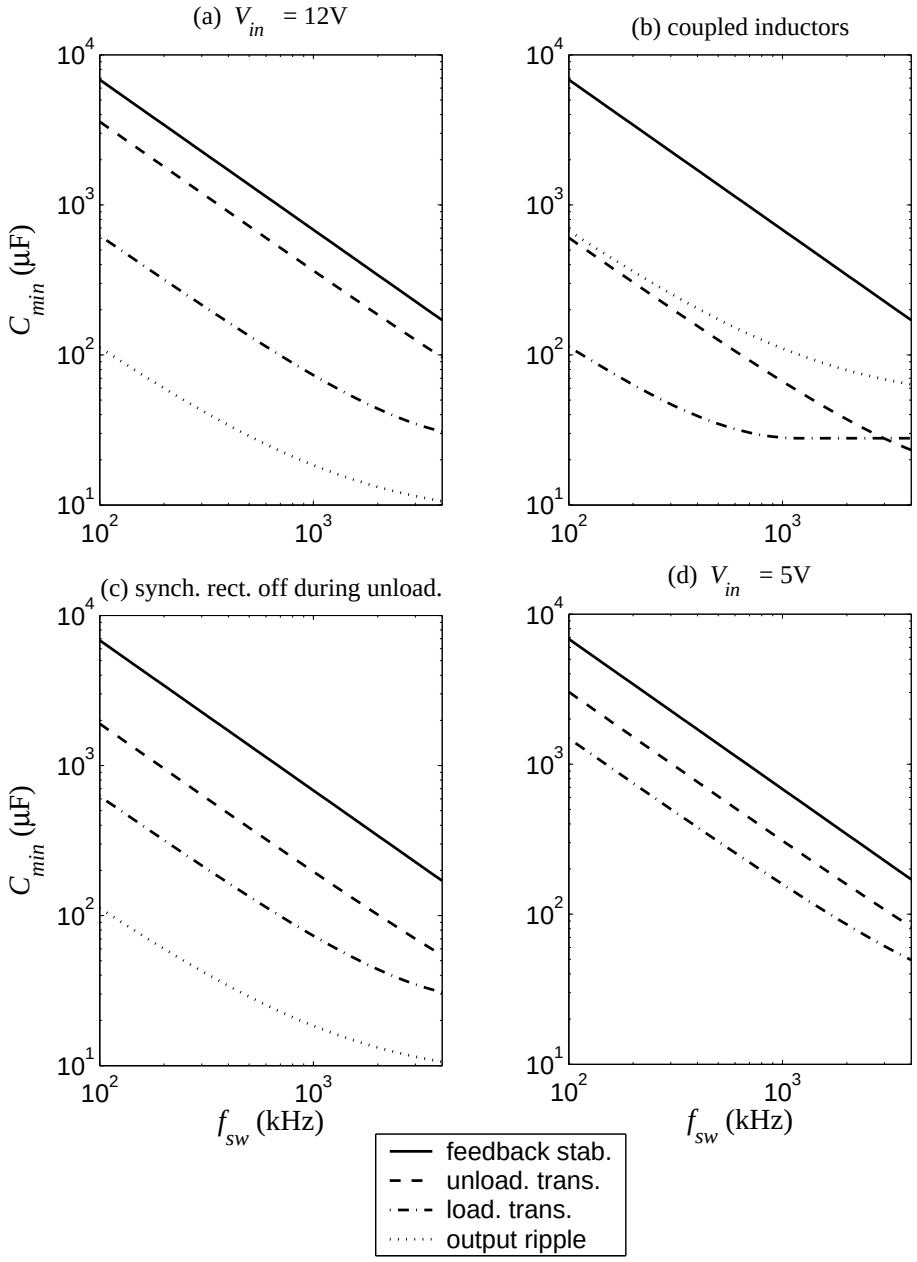


Figure 2.8: Minimum output capacitance constraints associated with unloading and loading transient response, feedback stability, and output ripple. Assumed VR parameters from Table 2.1, and $\tau_C = 24$ ns, $\Delta I_{L\phi,p-p} = 8$ A, $\Delta V_{o,r,p-p} = 16$ mV, $V_D = 1$ V, $t_d = 100$ ns, and $\alpha = 1/6$.

2.7.2 Output Capacitor Size

Three important design considerations that impose a minimum requirement on the VR's output capacitance were discussed in the previous sections: First, the stability constraint associated with feedback load-line regulation in Section 2.3 exacts

$$C \geq \frac{1}{2\pi R_{ref} \alpha f_{sw}}, \tag{2.45}$$

where $\alpha = 1/6$ is typical. Second, the critical capacitance requirement (2.41) has to be met for both the loading and unloading transients. Third, the output voltage ripple (2.44) limits the capacitor choice as well. In Fig. 2.8 these constraints are plotted versus switching frequency for a set of representative specifications, and for a few of the VR architectures discussed in Section 2.7.1. Plot (a) characterizes a standard 12 V-input VR; plot (b) addresses a coupled-inductor implementation [46]; plot (c) depicts a converter with "body braking" [21]; and plot (d) characterizes the second stage in a two-stage VR topology [85]. Note that in all cases the feedback stability requirement dominates the other constraints. This is especially true for architectures that are specifically tailored for efficient low-conversion-ratio operation Fig. 2.8(b–d). Importantly, if load-current feedforward is used, as discussed in Section 2.4, the feedback stability constraint is removed since ideally there are no stability limitations of the feedforward control path. In such case, Fig. 2.8 suggests that the size of the output capacitor can be reduced by factors of 2 to 8, depending on the architecture used. Thus, the regulation specification can be met with a small number of multi-layer ceramic capacitors (MLCC's) in the range of hundreds of μF at sub-MHz switching frequencies.

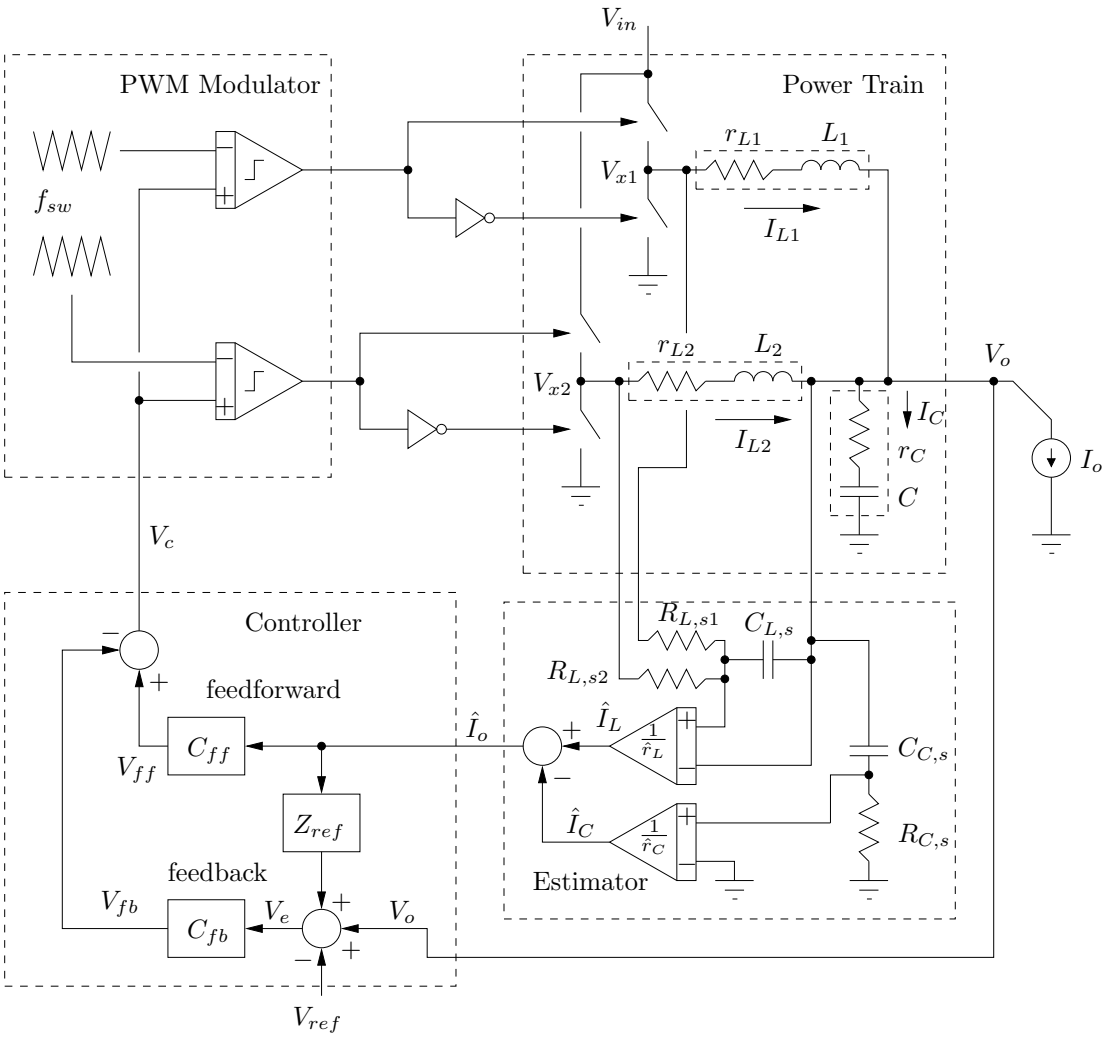


Figure 2.9: Implementation diagram of a two-phase buck converter with load-line regulation and estimated load-current feedforward.

2.7.3 Load-Current Estimation

The load feedforward control strategy discussed in Section 2.4 assumes that the load current is measured. Sensing the load current with a dedicated sense resistor in the load current path is not practical since it will increase the output impedance and power loss. On the other hand, using a lossless Hall-effect current sensor is not cost-effective. Simple, cost-effective, lossless estimation schemes are hence attractive:

Inductor and Capacitor Sensing

The load current can be reconstructed from estimates of the inductor and capacitor currents since $I_o = I_L - I_C$ [78, 120, 75]. The inductor current can be estimated with an RC filter connected in parallel with the inductor, and having time constant equal to that of the inductor [58, 21]. The capacitor current can be estimated in the same way. A VR implementation diagram, using this load current estimation approach and passively summing the inductor current estimates of the different phases [120, 75], is shown in Fig. 2.9.

In the case of perfect matching of the estimator and power train parameters, the injection of the load current estimate in the controller does not affect the closed-loop poles and zeros of the system. In practice, there typically is some mismatch between the estimator and power train parameters, resulting in the load current estimate becoming a function of the converter state variables and hence altering the system pole and zero locations. For small mismatches this effect is small, and can be tolerated in a properly designed controller.

Trace or Package Resistance Sensing

The printed-circuit-board trace resistance connecting the VR to the microprocessor, or the package resistance of the microprocessor could be used to sense the load current as well. The latter approach has been recently developed by Intel for the purposes of on-chip power management [79]. In [79] the package resistance is calibrated with a precision on-chip current source. Alternative methods for calibration could be developed using, for example, the VR input current, since it is relatively easy to measure because of the low nominal duty ratio.

2.7.4 PWM Modulator

A switch modulation scheme having a very low latency is essential for achieving a fast controller response with load-current feedforward. Good candidates among fixed-switching-frequency modulators include unlatched level-sensitive PWM (with some hysteresis for noise immunity), leading-edge latched PWM, two-sided latched PWM [57], and valley current-mode control [86]. All of these have turn-off latency equal to or less than the steady-state on-pulse-width, which is about a tenth of the switching period in 12 V-input VR's.

2.7.5 Dynamic Reference Voltage

In this discussion we have assumed that V_{ref} is constant. In modern microprocessor systems with dynamic voltage scaling, V_{ref} can be adjusted during operation. However, this happens at slow rates compared to changes in the load current (e.g., reference voltage slew rate of 2.2 mV/μs, [19]), and hence tracking it does not present a substantial challenge. In

Table 2.2: Prototype 1 MHz buck converter parameters

	Power Train	
N	number of phases	4
V_{in}	input voltage	12 V
$I_{o,max}$	max. load current	120 A
$r_{h\phi}$	high-side switch on-resistance	21 mΩ
$r_{l\phi}$	low-side switch on-resistance	3 mΩ
L_ϕ	phase inductors	390 nH @ 15 A
$r_{L\phi}$	inductor ESR & trace resistance	0.7 mΩ
C_{bulk}	output bulk capacitance	8×100 μF (ceramic)
τ_{Cbulk}	output bulk capacitor ESR time constant	0.2 μs
C_{hf}	output high-frequency decoupling capacitance	10 + 0.1 μF (ceramic)
τ_{Chf}	output high-frequency capacitor ESR time constant	24 ns
	PID Controller	
V_{ref}	reference voltage	1.3 V
R_{ref}	closed-loop output impedance	1.3 mΩ
f_{sw}	switching frequency	1 MHz
K	proportional gain	20
T_I	integral time	17 μs
T_D	derivative time	3.7 μs
	1^{st} high-frequency pole	0.55 MHz
	2^{nd} high-frequency pole	1.5 MHz
t_d	control delay before modulator	100 ns
	Loop Gain	
PM	phase margin	47°
GM	gain margin	10 dB
f_c	unity gain frequency	200 kHz

fact, a simple and effective reference voltage feedforward, providing good tracking up to the LC cutoff frequency, can be accomplished by directly adding V_{ref} to the input of the PWM modulator.

2.8 Simulations and Experimental Results

To demonstrate the use of load-current feedforward to improve load-line regulation performance, a 4-phase version of the controller structure in Fig. 2.9 was implemented. A synchronous buck converter board (International Rectifier IRDCiP2002-C) was modified to incorporate estimated load-current feedforward. The on-board PWM modulator (Intersil ISL6558) uses voltage-mode, latched trailing-edge modulation with phase-current balancing. The converter parameters are summarized in Table 2.2. The feedforward law (2.22) from Section 2.4.1 was used.

The system was simulated in PSIM (see Appendix A for simulation schematic). Figures 2.10 and 2.11 show the converter transient response to load steps of different magnitude, with and without load-current feedforward. In Fig. 2.10 a small 8 A load step is depicted. With load-current feedforward the output voltage adheres tightly to the prescribed load line [plot (a)]. In plot (b) it can be seen that the feedforward path contributes the bulk of the duty-ratio command signal, while the feedback signal has a small magnitude. In contrast, without load-current feedforward, the control effort is determined solely by the feedback path, and the output voltage deviates substantially from the desired load line. The feedback unity-gain bandwidth is limited to 200 kHz, which is one-fifth of the switching frequency, for the stability reasons discussed in Section 2.3.2. However, according to Section 2.3.2, for the load-line feedback approach to work successfully, the bandwidth has to be substantially larger than $1/2\pi R_{ref}C = 153$ kHz, which could not be achieved here due to the stability constraint. Clearly, the load-current feedforward circumvents this limitation by producing a large, fast, exogenous control signal.

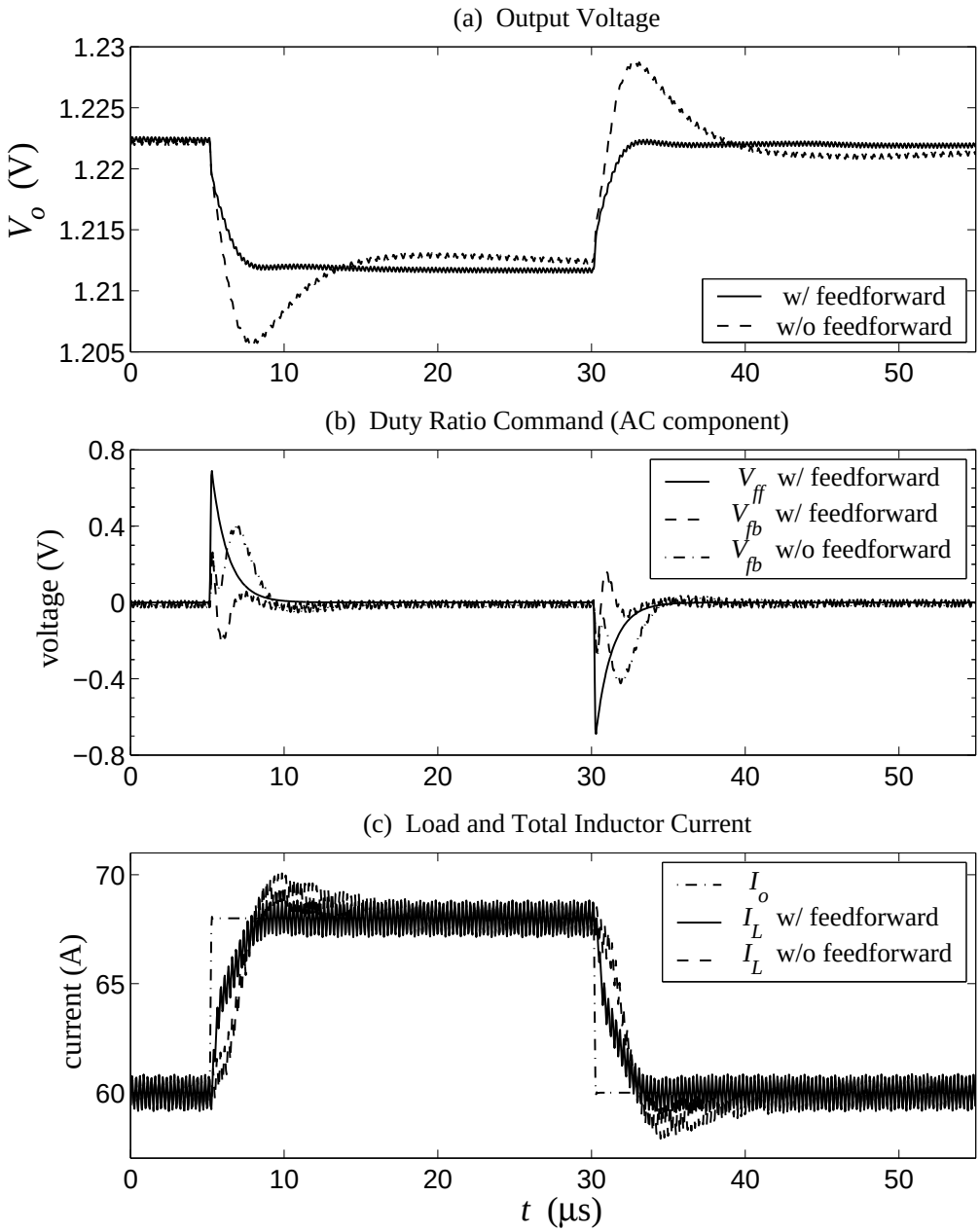


Figure 2.10: Simulated 8 A load transient, from 60 A to 68 A to 60 A, with and without load-current feedforward.

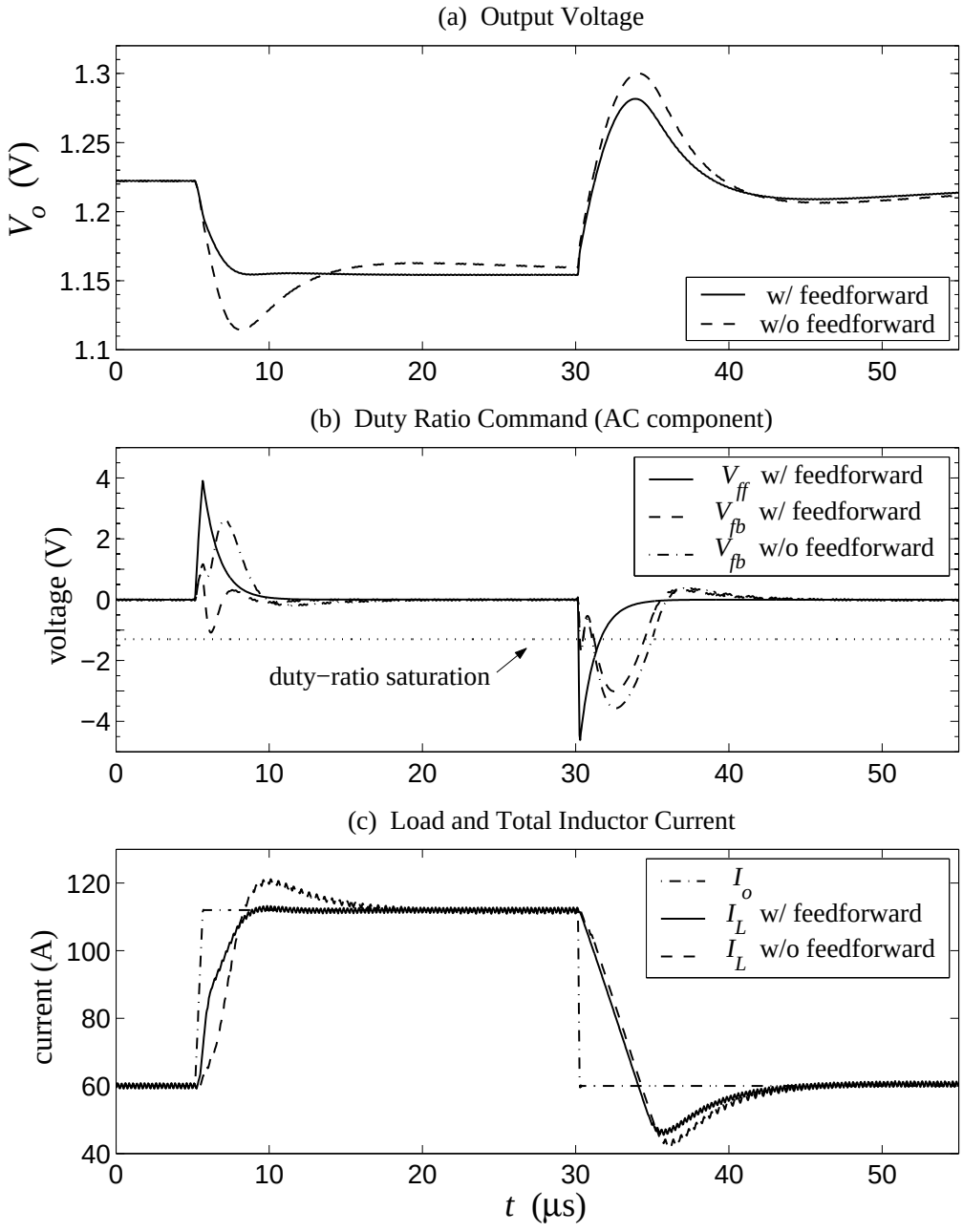
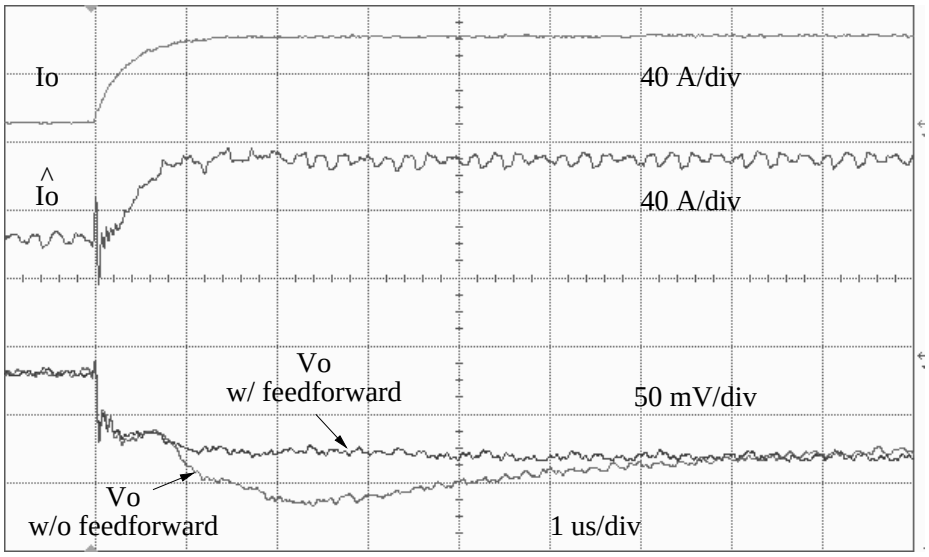
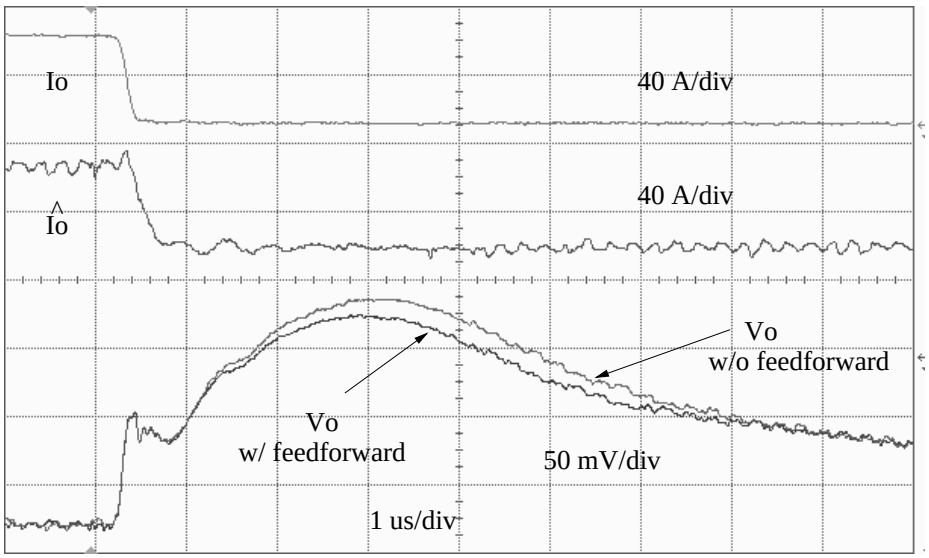


Figure 2.11: Simulated 52 A load transient, from 60 A to 112 A to 60 A, with and without load-current feedforward.



(a) Loading step from 60 A to 112 A



(b) Unloading step from 112 A to 60 A

Figure 2.12: Experimental 52 A load transient, with corresponding estimated load current, with and without load-current feedforward.

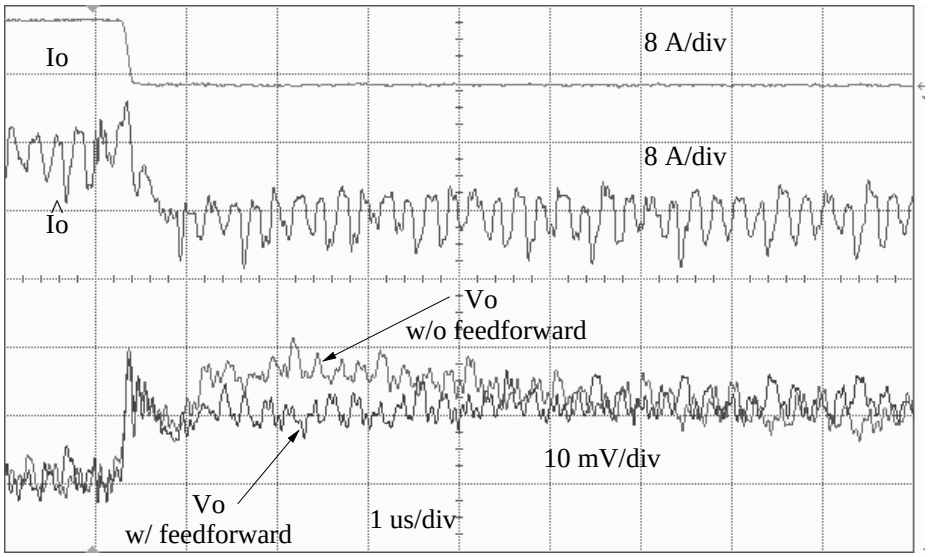


Figure 2.13: Experimental 8 A unloading transient, from 68 A to 60 A, with corresponding estimated load current, with and without load-current feedforward.

Fig. 2.11 depicts the converter response to a large 52 A load current transient. The loading transient is a scaled version of the 8 A loading response, since the system has linear average behavior. The unloading step, however, results in duty-ratio saturation at zero, due to the low output voltage. The converter behavior under duty-ratio saturation is consistent with the discussion in Section 2.5. Indeed, solving equation (2.41) for the unloading voltage overshoot yields $\Delta V_{os} = 67$ mV which matches the simulation. Notice that, compared to pure feedback control, the load-current feedforward decreases the output voltage overshoot, since it drives the duty ratio to saturation faster.

Fig. 2.12 shows the experimental prototype transient response, with and without estimated load-current feedforward, for 52 A loading and unloading transients, analogously to Fig. 2.11. Due to hardware constraints of the pulsed load circuit, the loading current step has a time constant of about 250 ns. The unloading current step is much faster, completing the step in less than 200 ns.

From the figures it can be seen that the estimated load current follows very well the measured current with a delay of about 100 ns. The 4 MHz switching noise present in the load-current estimate results from parasitic coupling to the sense wires which were soldered on top of the converter board. The switching noise does not affect the DC regulation precision because it is attenuated by the PID controller. Further, in a dedicated implementation, the sensing can be done through buried, shielded PCB traces, thus reducing both electrostatic and magnetic pickup.

The loading transient in Fig. 2.12(a) resembles closely the simulation in Fig. 2.11. With pure feedback control the output voltage sags by 35 mV below the load-line, cor-

responding to overshoot of more than 50%. On the other hand, load-current feedforward effects tight load-line regulation. The unloading transient in Fig. 2.12(b) is similar to the one in Fig. 2.11 as well. The combined feedback and feedforward control produces a slightly better voltage response than the feedback alone, implying a faster transition to duty-ratio saturation. The improvement with feedforward control is not as substantial as that for the loading transient, since the duty-ratio saturation fundamentally limits the performance. An overshoot of about 85 mV is observed, which is expected since the duty ratio saturates to zero about 300 ns after the beginning of the step, and equation (2.41) predicts overshoot of $\Delta V_{os} = 80$ mV for these conditions. The transient regulation here can be enhanced if the synchronous rectifier is turned off, or if a smaller total inductance is used, as discussed in Section 2.7.1. Finally, Fig. 2.13 shows a smaller, 8 A experimental unloading transient which parallels the simulation in Fig. 2.10 with some additional sensing and measurement noise associated with the prototype. Again, it is clear that the combination of feedback and feedforward provides tighter output impedance regulation than feedback alone.

It should be noted that, while the analysis in the preceding sections assumed that the load is a variable current source, the load in this experiment is a variable resistor. Thus, the load current is a function of the output voltage, resulting in some positive feedback of the output voltage through the feedforward control law. The magnitude of this positive feedback is small compared to the negative feedback gain, and does not result in instability, as witnessed by the experimental results.

2.9 Conclusion

This chapter presented a consistent framework for output-impedance regulation of the buck converter using output capacitors with an arbitrary ESR time constant, encompassing electrolytic and ceramic technologies. In both current-mode and voltage-mode control, load-current feedforward can extend the useful bandwidth beyond that achievable with pure feedback, since feedforward is not limited by stability constraints. The load-current feedforward is used to handle the bulk of the regulation action by providing a fast duty-ratio control signal. The feedback is used to compensate for imperfections of the feedforward and to ensure tight DC regulation. With load-current feedforward the output capacitor size is limited only by large-signal transient and switching-ripple considerations. The load current can be estimated from the inductor and capacitor voltages with simple RC networks, or with another lossless sensing method. Different types of PWM modulators can be used as long as they have low latency. An experimental prototype demonstrated tight load-line regulation with load-current feedforward, compared to an overshoot of over 50% with feedback only. These results point to the feasibility of microprocessor VR implementations using only a small number of ceramic output capacitors. The dynamic load-current feedforward approach described here for the buck converter can be extended to other converter topologies as well. The discussion was presented in a continuous-time, analog framework, but is easily convertible to the discrete-time, digital domain. The next chapter discusses some issues specific to a digital controller implementation.

Chapter 3

Digital PWM Controller Design: Quantization, Limit Cycling, and Dither

3.1 Introduction

A basic block diagram of a digitally-controlled PWM buck converter is shown in Fig. 3.1. The controller consists of an analog-to-digital converter (ADC), a discrete-time control law, and a digital PWM (DPWM) module. The ADC quantizes the regulated signal (e.g., the output voltage error $V_e = V_o - V_{ref}$) into a digital word D_e. The control law computes a digital duty-ratio command D_c based on the error D_e. The DPWM modulator takes D_c as input, and outputs a PWM waveform with the commanded duty ratio at the switching frequency f_{sw}. The DPWM waveform has finite time resolution. The sensing and

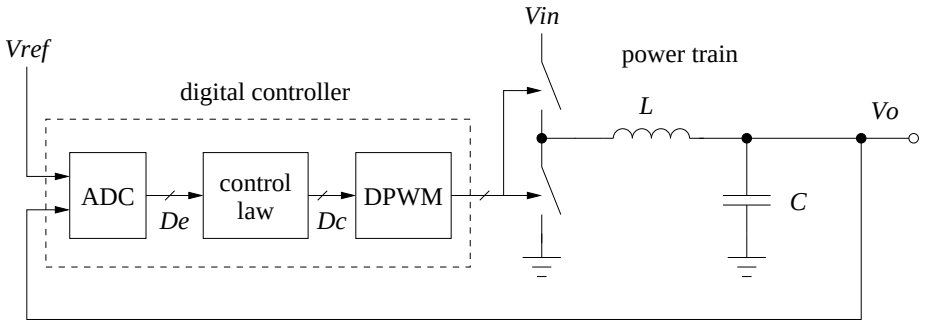


Figure 3.1: Basic block diagram of a digitally-controlled PWM buck converter.

quantization of other variables, such as the load current, can be added depending on the application and the control law used. Further, interface between the controller and other digital systems can be included, as indicated in Fig. 1.3 in Chapter 1. The digital controller can be implemented on an autonomous special-purpose IC [68, 111], integrated in a larger digital system [102], or programmed on a general-purpose microcontroller or DSP [36].

This chapter discusses implementations of the digital controller blocks, and addresses system stability issues unique to digital control. Sections 3.2 and 3.3 overview hardware architectures of ADC and DPWM blocks, respectively. Section 3.4 gives the basic digital PID control law. Section 3.5 discusses the existence of limit cycles, as well as conditions for their elimination. Section 3.6 introduces digital dither as a method to increase the effective DPWM resolution, thus preventing limit cycling, and enabling low-power, small-area DPWM implementations. Section 3.7 provides simulations and experimental results for a digitally-controlled buck converter, demonstrating the conditions for limit-cycle prevention, and the use of digital dither to increase the effective DPWM resolution. Finally, Section 3.8 concludes the chapter.

3.2 Overview of ADC Topologies

One choice to sample V_o could use an ADC that quantizes the full possible output range from ground to V_{in} [108]. An 11-bit ADC will provide 6 mV resolution for $V_{in} = 12$ V. This approach is not well suited for low-power applications, since a high quantization resolution over a wide voltage range is required. For very low power applications, the ADC can be implemented with a single comparator [23, 22]. However, this approach has poor transient performance, since excursions of the output voltage away from the reference voltage cannot be quantized appropriately. A compromise solution is based on the observation that under normal operation the output voltage of a regulator should not deviate substantially from the reference voltage. Thus, the output voltage has to be quantized only over the regulation window around the reference signal [78]. For example, in microprocessor voltage regulators the output voltage should be within ±25 mV of the reference signal [19]. Assuming 5 mV ADC quantization bin size, only 10 bins are required in this case. A block-diagram of a flash implementation of such a "window" ADC is shown in Fig. 3.2. Note that, since V_o is compared against V_{ref}, the resulting digital signal (D_e) is the difference between the two, which is a digital representation of the error signal V_e. Hence, it has the functionality of both an ADC and an error amplifier. The window concept has been successfully used in delay-line [68] and differential-ring-oscillator-counter [111] ADC implementations.

Another consideration for ADC design is sensitivity to noise. A switching converter power train is an inherently noisy environment with high-slew-rate, supply-swing voltage switching and often substantial inductor ripple currents. Consequently, there is the possibility of capacitive, inductive, and ground-plane coupling of switching noise to

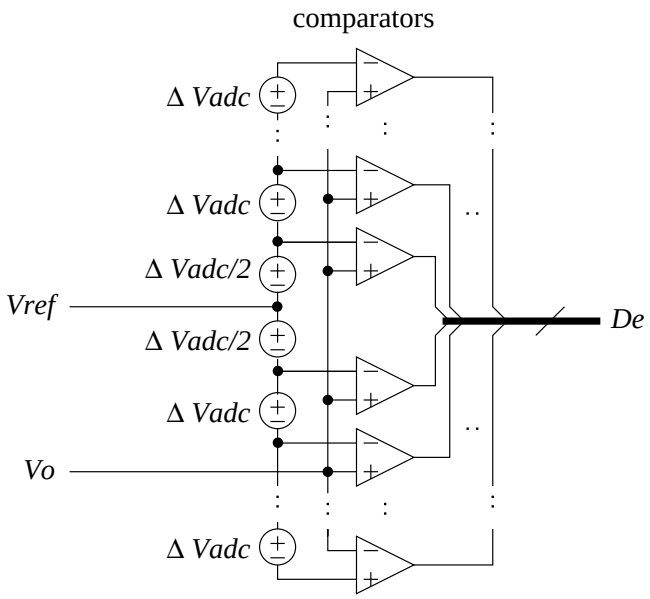


Figure 3.2: Block diagram of a flash window ADC. It implements both an ADC and an error amplifier.

the ADC input. The switching noise can produce undesirable aliasing effects in the quantization process. For example, typically the ADC is sampled at the converter switching frequency, and hence switching-frequency noise could be aliased to a DC offset. To prevent aliasing effects and to provide accurate DC regulation, ADC's which average the input signal over each sampling period are desirable. Averaging ADC's has been implemented with ring-oscillator-counter [102] and differential-ring-oscillator-counter [111] topologies.

Finally, the converter control strategy may use other system variables besides the output voltage. For example, the load-current feedforward method discussed in Section 2.4 would require quantization of the load current. In the cases when very fast transient response is required, the load current may have to be sampled at rates higher than the switching frequency. Note that with voltage-mode control the feedforward control law (2.22) is AC-coupled. The AC-coupling can be implemented before the ADC, thus a window architecture

could be used for this application as well.

3.3 Overview of Digital PWM Topologies

Two types of structures have been used to implement digital PWM modulators: counter-comparator [100, 101] and delay-line-mux or ring-oscillator-mux [23]. The counter-comparator scheme has small area but high power due to high-frequency clocking of the counter. The ring-oscillator-mux and delay-line-mux schemes have low power, since switching activity is at the converter switching frequency, however they have large area due to the large number of delay stages needed. Hybrid systems combining a ring-oscillator-mux block with a counter-comparator have emerged as a compromise, having acceptable area and power [22, 102, 68]. A ring-oscillator-mux-dither approach using current-starved differential inverters, operating in the sub-threshold regime, has been developed in [109, 111]. Digital cells in the sub-threshold regime have large delay, enabling a small-area ring oscillator running at the switching frequency. The low DPWM resolution resulting from the long cell delay is boosted by digital dither [74] (see also Section 3.6).

3.4 Digital Feedback Control Law

A standard choice for the feedback control law is the PID law (2.6) given in Section 2.3.2. Its discrete-time counterpart has the form

$$D_c[k+1] = K_p D_e[k] + K_d \left(D_e[k] - D_e[k-1]\right) + K_i D_i[k], \tag{3.1}$$

where $D_c[k]$ is the duty-ratio command at discrete time k, $D_e[k]$ is the digitized version of the error signal V_e, and $D_i[k]$ is the state of a digital integrator

$$D_i[k+1] = D_i[k] + D_e[k]. \tag{3.2}$$

Parameter K_p is the proportional gain, K_d is the derivative gain, and K_i is the integral gain. It is often practical to round off the gains to powers of two, allowing for implementations using simple binary shifts. The design methodologies for digital PID control laws are discussed in a general framework in [31] and [7], and in a power electronics framework in [53] and [26], for example. The control law can be implemented with a set of binary adders and shifts [111]; with a look-up table [68]; or with a microprocessor core (if more sophisticated computations are required).

Typically, the duty-ratio command is computed once per switching period. However, if faster response is required, it could be computed more frequently. For example, in an N-phase converter D_c could be updated at the effective switching frequency Nf_{sw} (this approach is used in the prototype in Section 4.4).

3.5 Existence and Elimination of Limit Cycles

For the converter of Fig. 3.1, limit cycles refer to steady-state oscillations of V_o and other system variables at frequencies lower than the converter switching frequency f_{sw} (subharmonic frequencies). Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop [108]. Steady-state limit cycling may be undesirable if it leads to large, unpredicted output voltage variations. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult

to analyze and compensate for the resulting V_o noise and the electro-magnetic interference (EMI) produced by the converter.

Let us consider a system with effective ADC resolution of N_{adc} bits and DPWM resolution of N_{dpwm} bits. For a buck converter, this corresponds to voltage quantization of $\Delta V_{adc} = V_{in}/2^{N_{adc}}$ steps for the ADC. The DPWM modulator will have a $T/2^{N_{dpwm}}$ time resolution, implying $\Delta V_{dpwm} = V_{in}/2^{N_{dpwm}}$ output voltage resolution. Fig. 3.3(a) illustrates qualitatively the behavior of V_o in steady state when the DPWM resolution is less than the ADC resolution, and there is no DPWM level that maps into the ADC bin corresponding to the reference voltage V_{ref} (this ADC bin will be referred to as the *zero-error bin*). In steady state, the controller will be attempting to drive V_o to the zero-error bin, however due to the lack of a DPWM level there, it will alternate between the adjacent DPWM levels. This results in non-equilibrium behavior, such as steady-state limit cycling.

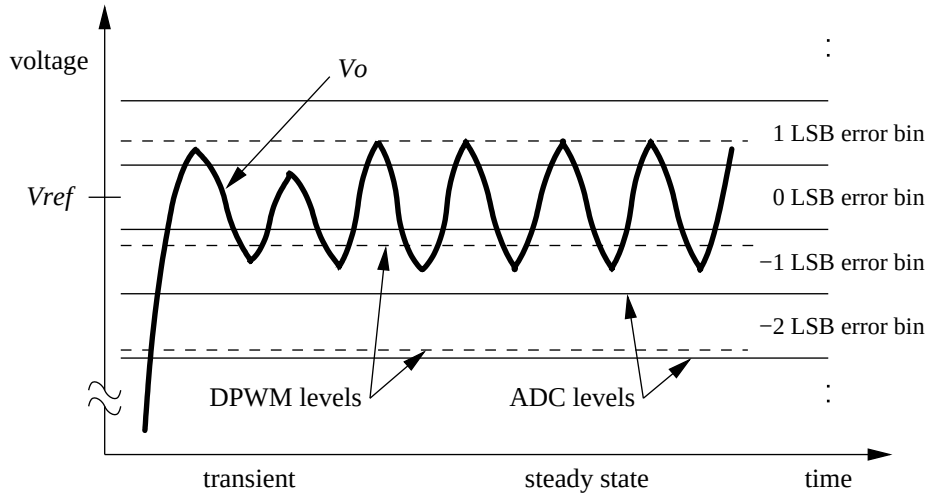
The first step towards eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC,

No Limit Cycle Condition # 1

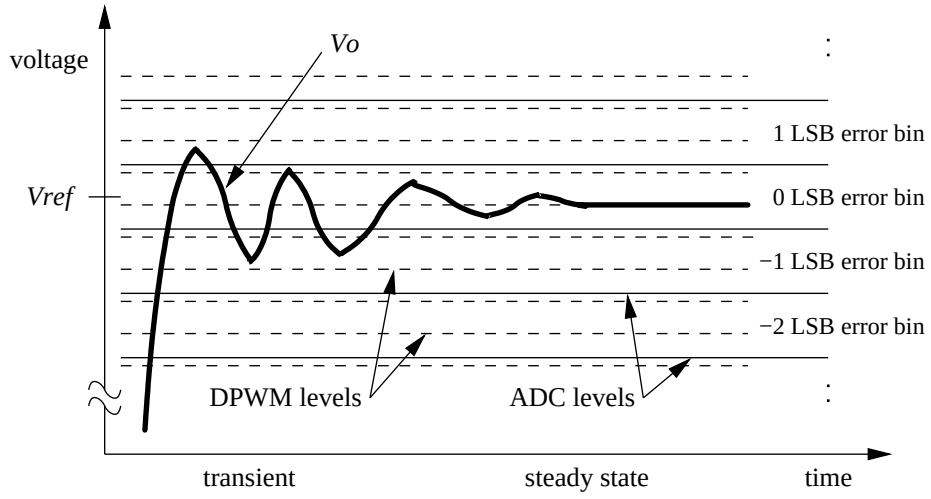
$$\Delta V_{dpwm} < \Delta V_{adc} \tag{3.3}$$

A one-bit difference in the resolutions, $N_{dpwm} = N_{adc} + 1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level.

Yet, even if the above condition is met, limit cycling may still occur if the feed-forward term is not perfect and the control law has no integral term ($K_i = 0$). In this case, the controller relies on non-zero error signal D_e to drive V_o towards the zero-error bin.



(a)



(b)

Figure 3.3: Qualitative behavior of V_o with (a) DPWM resolution lower than the ADC resolution, and (b) DPWM resolution two times the ADC resolution and with integral term included in control law. (The f_{sw} switching ripple is not shown, for clarity.)

However, once V_o is in the zero-error bin, the error signal becomes zero, and V_o droops back below the zero-error bin. This sequence repeats over and over again, resulting in a limit cycle. This problem can be solved by the inclusion of an integral term in the control law. After a transient, the integrator will gradually converge to a value that drives V_o into the zero-error bin, where it will remain as long as $D_e = 0$, since a digital integrator is perfect [Fig. 3.3(b)],

No Limit Cycle Condition # 2

$$0 < K_i \leq 1 \tag{3.4}$$

An upper bound of unity is imposed on the integral gain, since the digital integrator is intended to fine-tune the output voltage, therefore it has to be able to adjust the duty-ratio command by steps as small as a least significant bit (LSB).

The two conditions suggested above are not sufficient for the elimination of limit cycles, since the non-linearity of the quantizers in the feedback loop may still cause limit cycling for high loop gains. Non-linear system analysis tools, such as describing functions [32, 31], can be used to determine the maximum allowable loop gain not inducing limit cycles. The feedback loop includes two quantizers—the ADC and the DPWM—however in the present analysis we will consider only the ADC non-linearity, since it performs coarser quantization if the DPWM resolution is made higher than that of the ADC (as recommended above). The describing function of an ADC (a round-off quantizer) represents its effective gain as a function of the input signal AC amplitude and DC bias. When the control law contains an integral term, only limit cycles that have zero DC component can be stable, because the integrator drives the DC component of the error signal to the zero-error bin.

Since in steady state the DC bias is driven to zero, and since the loop gain $\mathcal{L}(j\omega)$ from the output of the ADC to its input has a low-pass characteristic, the sinusoidal-input describing function of a round-off quantizer can be used to analyze the stability of the system. The characteristic of a round-off quantizer is plotted in Fig. 3.4(a), where V_{adc} is the ADC input voltage, ΔV_{adc} is the ADC quantization bin size corresponding to one LSB, and D_{out} is the quantized representation of V_{adc}. The corresponding describing function $\mathcal{N}(A)$ is plotted in Fig. 3.4(b), where A is the AC amplitude of V_{adc}. From the plot it can be seen that the describing function has a maximum value of about 1.3, corresponding to maximum effective ADC gain. The control law (3.1), and hence $\mathcal{L}(j\omega)$, can then be designed to exclude limit cycles by ensuring that

No Limit Cycle Condition # 3

$$1 + \mathcal{N}(A)\mathcal{L}(j\omega) \neq 0 \tag{3.5}$$

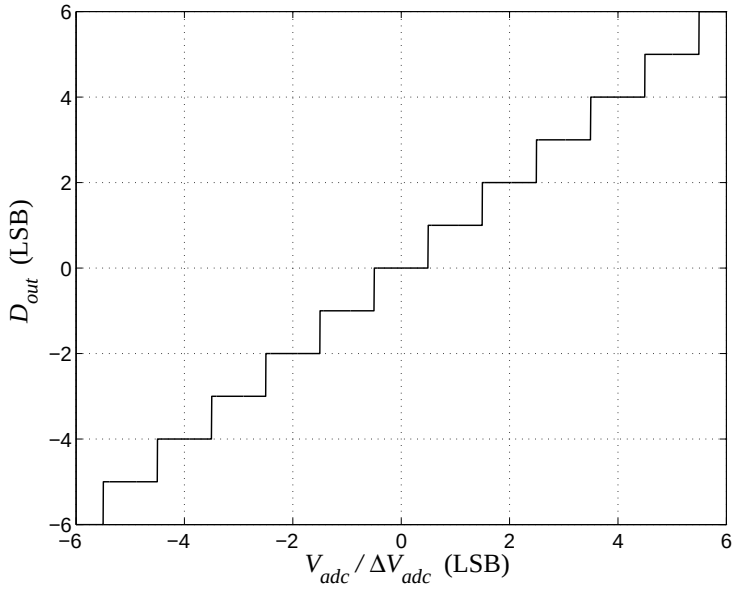
(Nyquist Criterion)

holds for all non-zero finite signal amplitudes A and frequencies ω. In practice, conventional loop design methods (e.g., Bode plots) can be used, keeping in mind that the effective ADC gain peaks somewhat above unity.

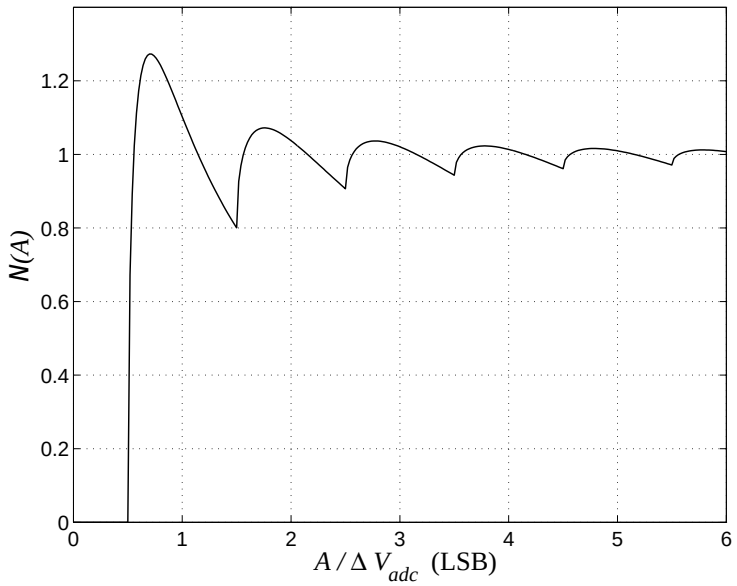
The no-limit-cycle conditions have been further explored in [69] with a more detailed analysis, largely corroborating the considerations discussed above.

3.6 Digital Dither

The precision with which a digital controller regulates the steady-state V_o is determined by the resolution of the ADC. In particular, V_o can be regulated with a tolerance



(a)



(b)

Figure 3.4: Characteristic of a round-off quantizer (a), and the corresponding describing function for sinusoidal signals with zero DC bias (b).

of one LSB of the ADC. Many present-day applications, such as microprocessor VR's, demand tight regulation tolerances [19], requiring ADC and DPWM modules with very high resolution. For example, regulation resolution of 10mV at $V_{in} = 12$V corresponds to ADC resolution of $N_{adc} = \log_2(12\text{ V}/10\text{ mV}) \approx 10$ bits, implying DPWM resolution of at least $N_{dpwm} = 11$ bits to avoid limit-cycling. For a converter switching frequency of $f_{sw} = 1$ MHz, such resolution would require a $2^{11} f_{sw} = 2$ GHz fast clock in a counter-comparator DPWM implementation, or $2^{11} = 2048$ stages in a ring-oscillator implementation, resulting in high power dissipation or large area, respectively [102, 22]. Thus, it is beneficial to look for ways to use low-resolution DPWM modules to achieve the desired high V_o resolution.

One method which can increase the effective resolution of a DPWM module is dithering. It amounts to adding high-frequency periodic or random signals to a certain quantized signal, which is later filtered to produce average DC levels with increased resolution. Analog dither has been used to increase the effective resolution of a DPWM module [14]. However, analog dither is difficult to generate and control, it is sensitive to analog component variations, and it can be mixed only with analog signals in the converter, and not with signals inside a digital controller. On the other hand, digital dither generated inside the controller is simpler to implement and control, is insensitive to analog component variations, and can offer more flexibility. Therefore, the use of digital dither to improve the resolution of DPWM hardware is discussed in the present section.

3.6.1 Programmed Digital Dither

The idea behind programmed digital dither is to vary the duty ratio by an LSB over a few switching periods, in a pre-determined way, so that the average duty ratio has a

value between two adjacent quantized levels. The averaging action is implemented by the output LC filter. The dither concept is illustrated in Fig. 3.5. Let D_{c1} and D_{c2} correspond to two adjacent quantized duty-ratio levels put out by the DPWM module, $D_{c2} = D_{c1} + LSB$. If the duty ratio is made to alternate between D_{c1} and D_{c2} every next switching period, the average duty ratio over time will equal $(D_{c1} + D_{c2})/2 = D_{c1} + (1/2)LSB$. Thus, an intermediate $(1/2)LSB$ sub-LSB level can be implemented by averaging over two switching periods, resulting in a one-bit increase of the effective DPWM resolution. Using the same reasoning, $(1/4)LSB$ and $(3/4)LSB$ levels can be implemented by averaging over four switching periods (Fig. 3.6), which increases the effective DPWM resolution by two bits. Finally, it can be seen that by using dither patterns spanning $2^{N_{dith}}$ switching periods, the effective DPWM resolution can be increased by N_{dith} bits,

$$N_{dpwm,eff} = N_{dpwm} + N_{dith}, \tag{3.6}$$

where N_{dpwm} is the hardware DPWM resolution, and $N_{dpwm,eff}$ is the effective DPWM resolution.

Of course, the effective increase in DPWM resolution by dithering does not come for free. The dithering of the duty ratio creates an additional AC ripple at the output of the LC filter, which is superimposed on the ripple from the converter switching action. It is desirable to keep the amplitude of the dither ripple low, in order to avoid poor output regulation, EMI, and limit cycles which may result from the interaction between the dither ripple and the ADC. Thus, it is beneficial to select dither patterns that minimize the dither ripple. For this reason we have restricted the discussion to dither with one LSB amplitude.

For a dither sequence with a particular length ($2^{N_{dith}}$ switching cycles for N_{dith}-bit

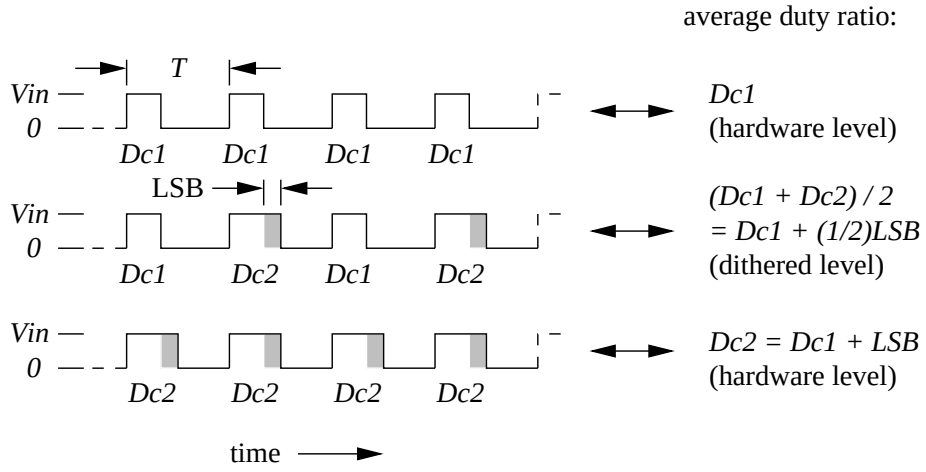


Figure 3.5: Use of switching waveform dither to realize a $(1/2)LSB$ effective DPWM level (1-bit dither).

dither) there may be a few different dither patterns that average to the same DC level. For example, in Fig. 3.6 the $(1/2)LSB$ level can be implemented with two different sequences: $\{D_{c1}, D_{c1}, D_{c2}, D_{c2}\}$ or $\{D_{c1}, D_{c2}, D_{c1}, D_{c2}\}$. The latter pattern has higher fundamental frequency, and thus produces less output voltage ripple, due to the low-pass characteristic of the output LC filter.

Two sets of 3-bit dither sequences are shown in Table 3.1, with "1" standing for the addition of an LSB to the duty ratio. Table 3.1(a) corresponds to a simple rectangular waveform dither (independently proposed in [72] and [70]). The generation of these patterns is very systematic and thus easy to implement. On the other hand, the "minimum-ripple" dither sequences in Table 3.1(b) were chosen with the aim of minimizing their low frequency spectral content. Thus, when filtered, they produce the lowest ripple for a given average duty ratio. As a result, while for the rectangular-waveform dither the sequences producing lowest ripple are $\{0, 0, 0, 0, 0, 0, 0, 1\}$ and its complement, for the minimum-ripple dither the ripple produced by any sequence does not exceed the ripple produced by $\{0, 0, 0, 0, 0, 0, 0, 1\}$

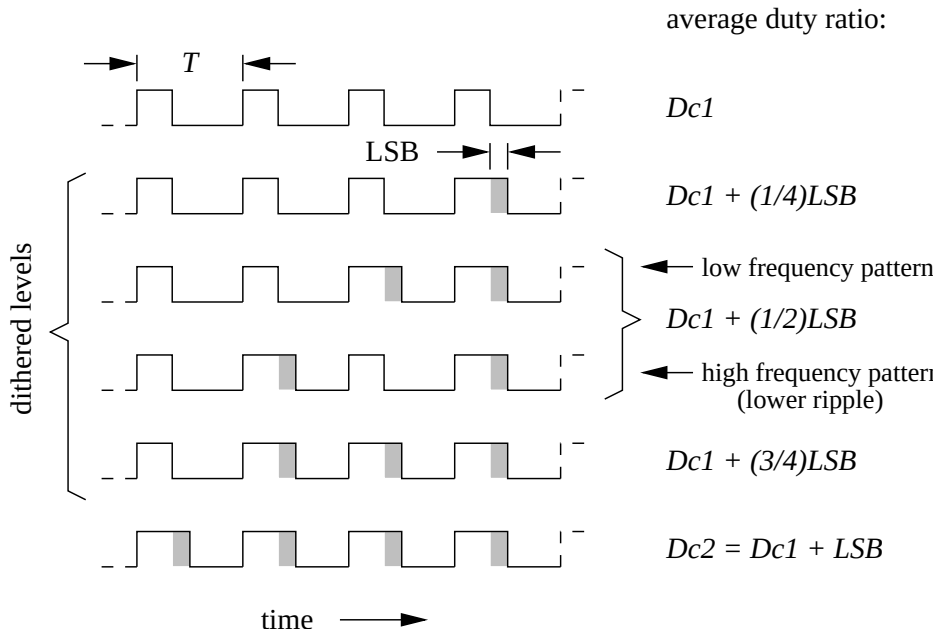


Figure 3.6: Switching waveform dither patterns realizing $(1/4)LSB$, $(1/2)LSB$, and $(3/4)LSB$ DPWM effective levels (2-bit dither).

and its complement. Therefore, the minimum-ripple sequences have a clear advantage over the rectangular-waveform sequences with respect to dither-ripple size. Finally, a set of 4-bit minimum-ripple dither sequences are given in Table 3.2.

3.6.2 Dither Generation Scheme

Fig. 3.7 shows a dither generation scheme that can produce pre-programmed patterns of any shape, and can therefore implement minimum-ripple dither such as the one in Table 3.1(b). A look-up table stores $2^{N_{dith}}$ dither sequences, each $2^{N_{dith}}$ bits long, corresponding to the sub-LSB levels implemented with N_{dith}-bit dither. The N_{dith} LSB's of the duty-ratio command D_c select the dither sequence corresponding to the appropriate sub-LSB level, while the N_{dith}-bit counter sweeps through this dither sequence. The dither pattern is then added to the N_{dpwm} MSB's of D_c to produce a dithered duty-ratio command

Table 3.1: 3-bit dither sequences

Sequence Average	*Rectangular-waveform Sequence*								*Ripple*	*Minimum-ripple Sequence*								*Ripple*
0/8	0	0	0	0	0	0	0	0	*none*	0	0	0	0	0	0	0	0	*none*
1/8	0	0	0	0	0	0	0	1	*lowest*	0	0	0	0	0	0	0	1	***highest***
2/8	0	0	0	0	0	0	1	1		0	0	0	1	0	0	0	1	
3/8	0	0	0	0	0	1	1	1		0	0	1	0	0	1	0	1	
4/8	0	0	0	0	1	1	1	1	***highest***	0	1	0	1	0	1	0	1	*lowest*
5/8	0	0	0	1	1	1	1	1		0	1	0	1	1	0	1	1	
6/8	0	0	1	1	1	1	1	1		0	1	1	1	0	1	1	1	
7/8	0	1	1	1	1	1	1	1	*lowest*	0	1	1	1	1	1	1	1	***highest***

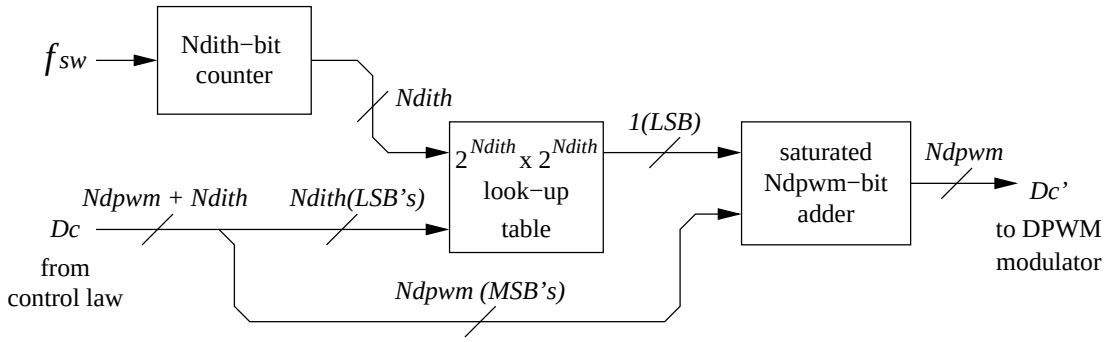


Figure 3.7: Structure for adding arbitrary dither patterns to the duty ratio, boosting the effective DPWM resolution by N_{dith} bits.

D_c' which is sent to the hardware DPWM module.

Note that it is generally true that the dither sequences with averages of $1/2 + 1/2^{N_{dith}}$ to $1 - 1/2^{N_{dith}}$ are the inverses of the sequences with averages of $1/2 - 1/2^{N_{dith}}$ to $1/2^{N_{dith}}$ (in reverse order). For example, in Table 3.2 the 9/16 to 15/16 dither sequences are the inverses of the 7/16 to 1/16 sequences. Further, the $0/2^{N_{dith}}$ dither level corresponds to a zero sequence. Thus, only $2^{N_{dith}-1}$ unique dither sequences have to be stored in the look-up

Table 3.2: 4-bit minimum-ripple dither sequence

Sequence Average	*Dither Sequence*															
0/16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1/16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2/16	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
3/16	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
4/16	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
5/16	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1
6/16	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	1
7/16	0	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
8/16	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
9/16	1	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
10/16	1	1	0	1	1	0	1	0	1	1	0	1	1	0	1	0
11/16	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0
12/16	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
13/16	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1	0
14/16	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
15/16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

table, and the rest can be generated from them via simple logic operations.

3.6.3 Dither Ripple and Bit Limit

In Section 3.6.1 it was shown that the longer the dither patterns used, the larger the effective DPWM resolution. However, longer dither patterns could cause higher output ripple, since they contain lower frequency components, receiving less LC-filter attenuation. This consideration puts a practical limit on the number of bits of dither that can be added

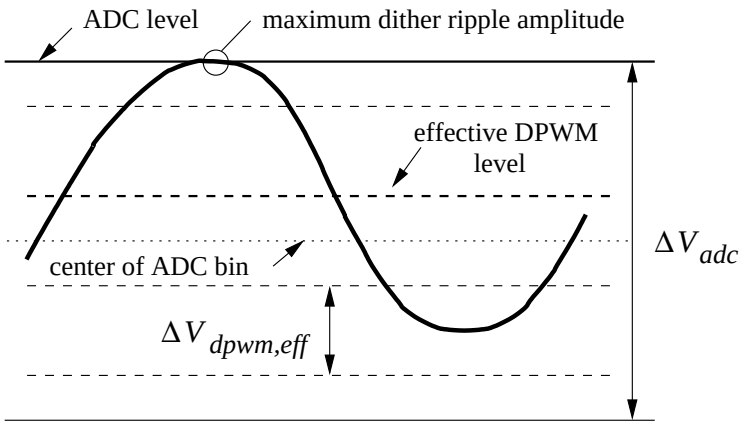


Figure 3.8: Maximum dither ripple amplitude constraint. Illustrated case is for $N_{dpwm,eff} = N_{adc} + 2$.

to increase the DPWM resolution.

To ensure that the dither does not cause steady-state limit cycling, there should always be an effective DPWM level that completely fits into one ADC quantization bin, taking into account the dither ripple. The converter switching ripple is not considered, since it is synchronous with the ADC sampling, and is thus aliased to a DC offset, which does not affect the limit cycle. With N_{dith}-bit dither, the effective DPWM quantization bin size is

$$\Delta V_{dpwm,eff} = V_{in}/2^{N_{dpwm,eff}} = V_{in}/2^{N_{dpwm}+N_{dith}}. \tag{3.7}$$

Geometric considerations show that the case which allows for the smallest dither ripple amplitude is when the effective DPWM levels are located at one-half effective DPWM bin size from the center of the ADC bin (see Fig. 3.8). Then the tolerable peak-to-peak dither ripple amplitude is bounded by

$$\Delta V_{o,dith} < \Delta V_{adc} - \Delta V_{dpwm,eff}. \tag{3.8}$$

Assuming that the ADC has resolution ΔN bits coarser than the effective DPWM resolu-

tion,

$$N_{adc} = N_{dpwm,eff} - \Delta N = N_{dpwm} + N_{dith} - \Delta N, \tag{3.9}$$

the ADC bin size is

$$\Delta V_{adc} = V_{in}/2^{N_{adc}} = V_{in}/2^{N_{dpwm}+N_{dith}-\Delta N}. \tag{3.10}$$

Substituting (3.7) and (3.10) in (3.8), we obtain

$$\Delta V_{o,dith} < V_{in}\left(2^{\Delta N} - 1\right)/2^{N_{dpwm}+N_{dith}}. \tag{3.11}$$

To determine how many bits of dither can be used in a certain converter, without causing a limit cycle, we now have to calculate $\Delta V_{o,dith}$ as a function of N_{dith}.

The dither ripple at the output depends on the DPWM resolution, the power train parameters, and the dither temporal pattern. Since the dither constitutes switching between two adjacent quantized duty-ratio levels, it can be modeled as a rectangular waveform, injected in the converter switching node, with peak-to-peak amplitude of one DPWM hardware LSB, equal to $V_{in}/2^{N_{dpwm}}$. Further, the fundamental dither frequency component is

$$f_{dith} = f_{sw}/2^{N_{dith}}. \tag{3.12}$$

We will study the ripple size and the corresponding number of bits of dither that can be used for the two dither schemes in Table 3.1.

Rectangular Dither

For the rectangular-waveform dither in Table 3.1(a), the dither waveform with the largest low frequency component is a square wave with 50% duty ratio. This waveform can

be used to study the worst-case dither ripple. Since the dither is smoothed by the power train LC filter, we will consider only its fundamental frequency component, which is a sine wave with frequency f_{dith} and peak-to-peak amplitude

$$A_{p-p,dith} = \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}}. \tag{3.13}$$

The peak-to-peak output voltage ripple can then be bounded approximately as

$$\Delta V_{o,dith} \leq |G(j2\pi f_{dith})|\, A_{p-p,dith}, \tag{3.14}$$

where $G(s)$ is the power train control-to-output voltage transfer function (2.4) from Section 2.3.2. Above the power train cutoff frequency $f_c = 1/2\pi\sqrt{LC}$, the magnitude of (2.4) is approximately

$$|G(j2\pi f_{dith})| \approx \begin{cases} \left(\frac{f_c}{f}\right)^2, & f_c < f < f_z, \quad (-40\text{dB/dec rolloff}) \\ \frac{{f_c}^2}{f_z f}, & f_z < f, \quad (-20\text{dB/dec rolloff}) \end{cases} \tag{3.15}$$

where $f_z = 1/2\pi\tau_C$ is the capacitor ESR zero frequency. Substituting back in (3.14), we derive the worst-case peak-to-peak output voltage ripple due to dither,

$$\Delta V_{o,dith} \approx \begin{cases} \left(\frac{f_c}{f_{sw}}\right)^2 2^{2N_{dith}} \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}}, & f_c < f_{dith} < f_z, \\ \frac{{f_c}^2}{f_z f_{sw}} 2^{N_{dith}} \frac{4}{\pi}\frac{V_{in}}{2^{N_{dpwm}}}, & f_z < f_{dith}. \end{cases} \tag{3.16}$$

This ripple approximation is a slight underestimate, since the higher order harmonics are ignored in (3.14), and (3.15) overestimates the attenuation in the vicinity of f_c and f_z. However, it enables the derivation of an analytical condition on how many bits of dither, N_{dith}, can be used in a certain system. Combining (3.11) with (3.16), and solving for N_{dith}, we obtain an upper bound,

$$N_{dith} < \begin{cases} \frac{1}{3}\log_2\left[\frac{\pi}{4}\left(\frac{f_{sw}}{f_c}\right)^2(2^{\Delta N}-1)\right], & f_c < f_{dith} < f_z, \\ \frac{1}{2}\log_2\left[\frac{\pi}{4}\frac{f_z f_{sw}}{{f_c}^2}(2^{\Delta N}-1)\right], & f_z < f_{dith}, \end{cases} \tag{3.17}$$

The above equation can be used by starting with a guess for N_{dith}, obtaining the corresponding dither frequency from (3.12), and then using (3.17) to obtain a bound on N_{dith}. If the result is not consistent with the initial guess for N_{dith}, the procedure should be repeated with a reduced value of N_{dith}. On the other hand, if the inequalities are satisfied, the value of N_{dith} can be increased, and the procedure can be repeated.

Minimum-Ripple Dither

For the minimum-ripple dither in Table 3.1(a), the dither sequences producing the largest ripple are the one consisting of all "0"'s and a single "1" [(1/8) LSB], and its complement [(7/8) LSB], as discussed in Section 3.6.1. Since these dither patterns have an asymmetric duty cycle, they contain significant spectral energy in harmonics beyond the fundamental. Thus, performing analysis based solely on the fundamental frequency component will yield inaccurate results. Therefore, we adopt a time domain analysis approach based on calculating the ripple charge delivered onto the output capacitor.

First, we calculate the inductor current ripple contributed by the dither. Let the duty-ratio command without dither be D_c. When one LSB is added by the dither, the duty ratio becomes $D_{c1} = D_c + 1/2^{N_{dpwm}}$. For N_{dith}-bit dither, the sequence consisting of all "0"'s and a single "1" produces average output voltage

$$\bar{V_o} = (D_c + 1/2^{N_{dpwm}+N_{dith}})V_{in}. \tag{3.18}$$

Thus, the peak-to-peak current ripple contributed by this dither pattern is

$$\Delta I_{L,dith} = \frac{T}{L}\left(D_{c1}V_{in} - \bar{V_o}\right) = \frac{TV_{in}}{L2^{N_{dpwm}}}\left(1 - \frac{1}{2^{N_{dith}}}\right). \tag{3.19}$$

The resulting ripple charge delivered onto the output capacitor is

$$\Delta Q_{C,dith} = \frac{T 2^{N_{dith}} \Delta I_{L,dith}}{8}, \tag{3.20}$$

resulting in capacitor voltage ripple

$$\Delta V_{C,dith} = \frac{\Delta Q_{C,dith}}{C} = \frac{T 2^{N_{dith}} \Delta I_{L,dith}}{8C}. \tag{3.21}$$

The total dither ripple at the output, taking into account the capacitor ESR is

$$\begin{aligned} \Delta V_{o,dith} &\approx \left(\frac{T}{8} 2^{N_{dith}} + \tau_C \right) \frac{\Delta I_{L,dith}}{C} \\ &= \left(1 + \frac{4}{\pi} \frac{f_{sw}}{f_z} \frac{1}{2^{N_{dith}}} \right) \left(\frac{f_c}{f_{sw}} \right)^2 \left(2^{N_{dith}} - 1 \right) \frac{\pi^2}{2} \frac{V_{in}}{2^{N_{dpwm}}}. \end{aligned} \tag{3.22}$$

This ripple approximation is a slight overestimate, since the capacitor and ESR voltage ripples are assumed to be in phase. Combining (3.11) with (3.22), and solving for N_{dith}, we obtain an upper bound,

$$N_{dith} < \log_2 \left[1 - \frac{4}{\pi} \frac{f_{sw}}{f_z} + \sqrt{ \left(\frac{4}{\pi} \frac{f_{sw}}{f_z} + 1 \right)^2 + \frac{8(2^{\Delta N} - 1)}{\pi^2} \left(\frac{f_{sw}}{f_c} \right)^2 } \right] - 1. \tag{3.23}$$

Fig. 3.9 compares the number of bits of dither that can be used with rectangular (3.17) and minimum-ripple (3.23) dither schemes. The plot shows N_{dith} as a function of the ratio of power train cutoff frequency to the switching frequency f_c/f_{sw}. It covers the range of 0.01 to 0.1 for f_c/f_{sw}, which is typical for voltage regulators for digital applications. The capacitor ESR zero frequency is fixed to $f_z = 0.5 f_{sw}$, which is consistent with ceramic capacitor technology at switching frequencies of about one megahertz. It is assumed that the effective DPWM resolution is one bit higher than the ADC resolution ($\Delta N = 1$). The plot indicates that using the minimum-ripple dither is advantageous, since it generally allows for the use of more dither bits than does rectangular dither, and hence enables the use of lower-resolution DPWM hardware.

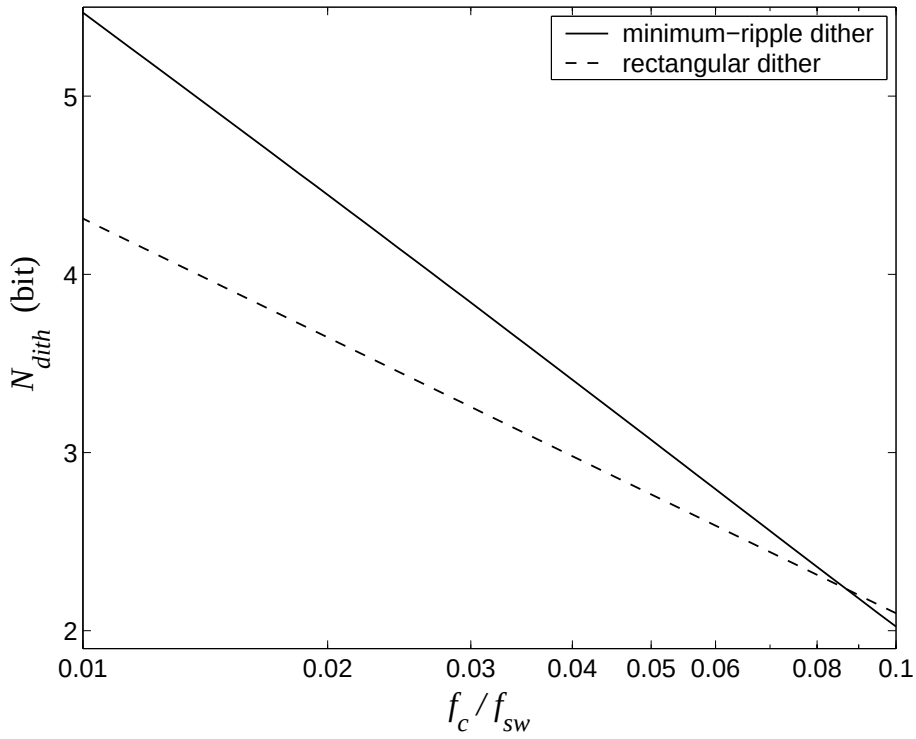


Figure 3.9: Dither bit limit vs. power train cutoff frequency, for $f_z = 0.5 f_{sw}$ and $\Delta N = 1$.

3.6.4 Multi-phase Dither

The concept of programmed dither can be extended to multi-phase (interleaved) converters like the one shown in Fig. 2.1. The programmed-dither technique developed for single-phase converters can be applied directly to the multi-phase case. For example, to achieve a $D_{c1} + (1/2)LSB$ level, duty ratio D_{c1} is applied to *all* phases for one switching period, followed by $D_{c2} = D_{c1} + LSB$ applied to all phases, and so on. However, in a multi-phase converter we can exploit the additional degrees of freedom associated with the independent switching of the phases to further reduce the dither ripple. This would allow for more bits of dither, and consequently less bits of hardware DPWM resolution.

Consider again the case of a $D_{c1} + (1/2)LSB$ level. This level can be implemented

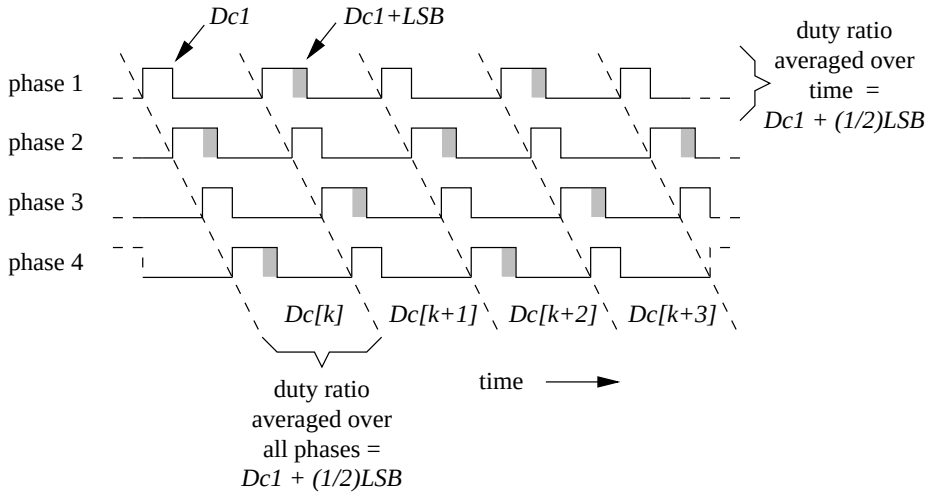


Figure 3.10: Four-phase switching waveform dither patterns implementing a $(1/2)LSB$ effective DPWM level.

by commanding, in the same switching period, D_{c1} to two of the phases and D_{c2} to the other two, so that the average duty ratio over all phases is $D_{c1} + (1/2)LSB$ for that period. The next switching period the duty ratio commands are toggled, so that the average over all phases is still $D_{c1} + (1/2)LSB$, however the average over time for each phase is $D_{c1} + (1/2)LSB$ as well (Fig. 3.10). The equal averaging over time for each phase is necessary to avoid DC current mismatch among the phases. This approach can be extended for other sub-LSB levels as well. In general, for an N-phase converter, $log_2 N$ bits of dither can be implemented by averaging over the phases. Multi-phase dither can increase the dither frequency seen at the output node about N times, thus reducing the resulting ripple, and allowing approximately $log_2 N$ more bits of DPWM resolution to be implemented with dither.

3.6.5 Sigma-Delta Dither

An alternative approach to increase the effective resolution of DPWM modulators uses sigma-delta modulation [49, 67, 50]. For a general discussion of sigma-delta modulation see, for example, [65]. The sigma-delta modulator uses local feedback of the digital duty-ratio command to generate the dither sequence, and there is no need to store pre-programmed dither patterns. This approach, however, does not guarantee minimum-ripple dither, and further the dither spectral content is generally hard to predict.

3.7 Simulations and Experimental Results

A prototype buck converter with parameters given in Table 3.3 was built to verify the no-limit-cycle conditions outlined in Section 3.5, as well as the use of the programmed dither from Section 3.6.1. The ADC quantization bin is $\Delta V_{adc} = 9.8$ mV. Fig. 3.11 shows the simulated output voltage behavior in steady-state and during a load-current transient. The results from both a switched simulation and an averaged model are given, both implemented in MATLAB (see Appendix B for MATLAB code). The switched simulation time step was fixed at one hardware DPWM LSB, $T/2^{N_{dpwm}} = 31.25$ ns, which is a natural choice for a converter with a discrete-time controller. In Fig. 3.11(a) the converter behavior without an integral feedback term ($K_i = 0$) is shown. The system exhibits a sub-harmonic limit cycle since condition (3.4) is not met. Note also that since there is no integral feedback, the DC output impedance is non-zero, as predicted by standard linear system theory. In plot (b) the integrator is enabled, however the 4-bit dither is turned off, resulting in limit cycling since the resolution of the DPWM (7-bit) is lower than the ADC resolution

Table 3.3: Prototype digitally-controlled buck converter parameters

	Power Train	
N	number of phases	4
V_{in}	input voltage	10 V
r_s	input source impedance	16 mΩ
$r_{h\phi}$	high-side switch on-resistance	65 mΩ
$r_{l\phi}$	low-side switch on-resistance	12 mΩ
L_ϕ	phase inductors	5.5 μH
$r_{L\phi}$	inductor ESR & trace resistance	12 mΩ
C_{bulk}	output bulk capacitance	6×680 μF (tantalum)
τ_{Cbulk}	output bulk capacitor ESR time constant	8.8 μs
C_{hf}	output high-frequency decoupling capacitance	6×10 μF (ceramic)
τ_{Chf}	output high-frequency capacitor ESR time constant	0.2 μs
	PID Controller	
V_{ref}	reference voltage	2.5 V
f_{sw}	switching frequency	250 kHz
f_{samp}	V_o sampling frequency	250 kHz
N_{adc}	effective ADC resolution	10 bit
N_{dpwm}	DPWM hardware resolution	7 bit
N_{dith}	dither resolution	4 bit (Table 3.2)
K_p	proportional gain	2^5
K_i	integral gain	2^{-1}
K_d	derivative gain	2^7
t_d	controller delay	5 μs
f_e	error amplifier -3 dB bandwidth	135 kHz
	Loop Gain	
PM	phase margin	48°
GM	gain margin	7 dB
f_c	unity gain frequency	12 kHz

(10-bit), violating condition (3.3). Finally, in plot (c) both the integrator and the dither are enabled, and all three no-limit-cycle conditions (3.3–3.5) are satisfied (condition (3.5) is satisfied by design of the loop gain). Consequently, limit cycles are prevented. It should be noted that in this case the steady-state ripple is only due to the multi-phase switching and the dither, and it does not exceed a couple of millivolts, compared to about 15 mV without the dither. Also note that in Fig. 3.11(b) the limit-cycle characteristic changes depending on the loading, resulting in spectral content that is difficult to predict.

Fig. 3.12 shows the experimental data from the hardware prototype. The experimental data largely corroborates the simulated results. One minor difference is that for the first 0.8 ms after the load transient in Fig. 3.12(b) the limit cycle has a higher frequency. This is due to the fact that the power supply providing the input V_{in} to the experimental converter has complex output impedance characteristic which was simplified to a real impedance r_s in the model. Further, the experimental setup uses a resistive load, while the simulation uses a current source load, which may account for some discrepancy in the results.

Finally, 5-bit programmed dither was successfully used in a low-power digital buck-converter IC to boost the effective resolution of a ring-oscillator-mux DPWM module from 5-bit to 10-bit [111].

3.8 Conclusion

To avoid limit cycling in digitally-controlled DC-DC converters, the resolution of the DPWM modulator has to be higher that that of the ADC, and an integral term has to be

used in the feedback control law. The effective resolution of the DPWM modulator can be boosted with digital dither, allowing for low-power, small-area DPWM implementations. The ripple incurred by the dither limits the number of bits of dither that can be used. Simulations and experimental results indicate an order of magnitude reduction of the steady-state output voltage ripple when limit cycling is prevented by the use of dither. This chapter discussed the digital implementation of the basic voltage regulation loop of a switching converter. The next chapter demonstrates the use of digital control for more sophisticated adaptive control tasks.

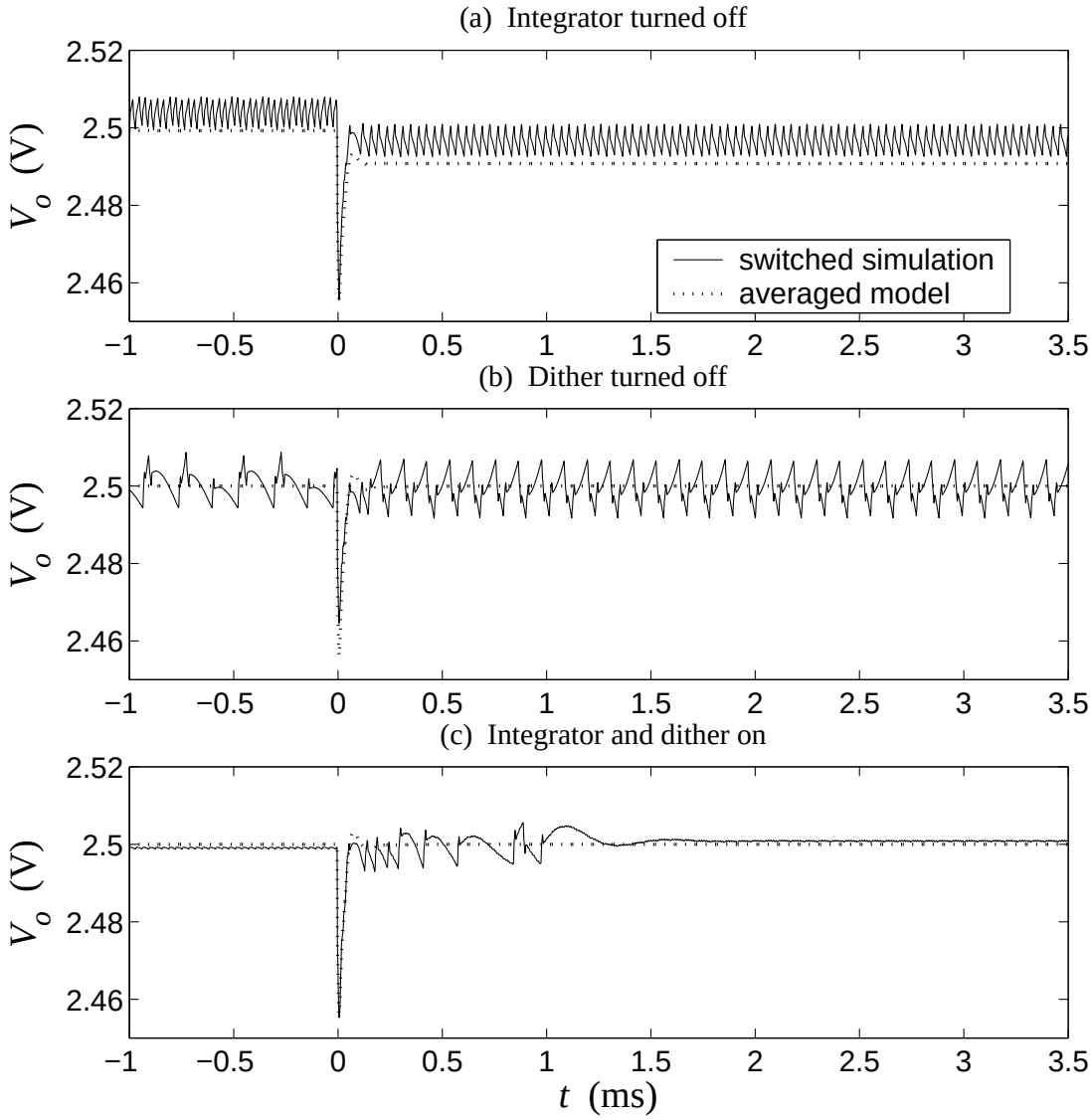


Figure 3.11: Simulated steady-state behavior and transient response of the prototype buck converter with and without integral feedback and dither. Load current steps from 0.5 A to 12 A at $t = 0$.

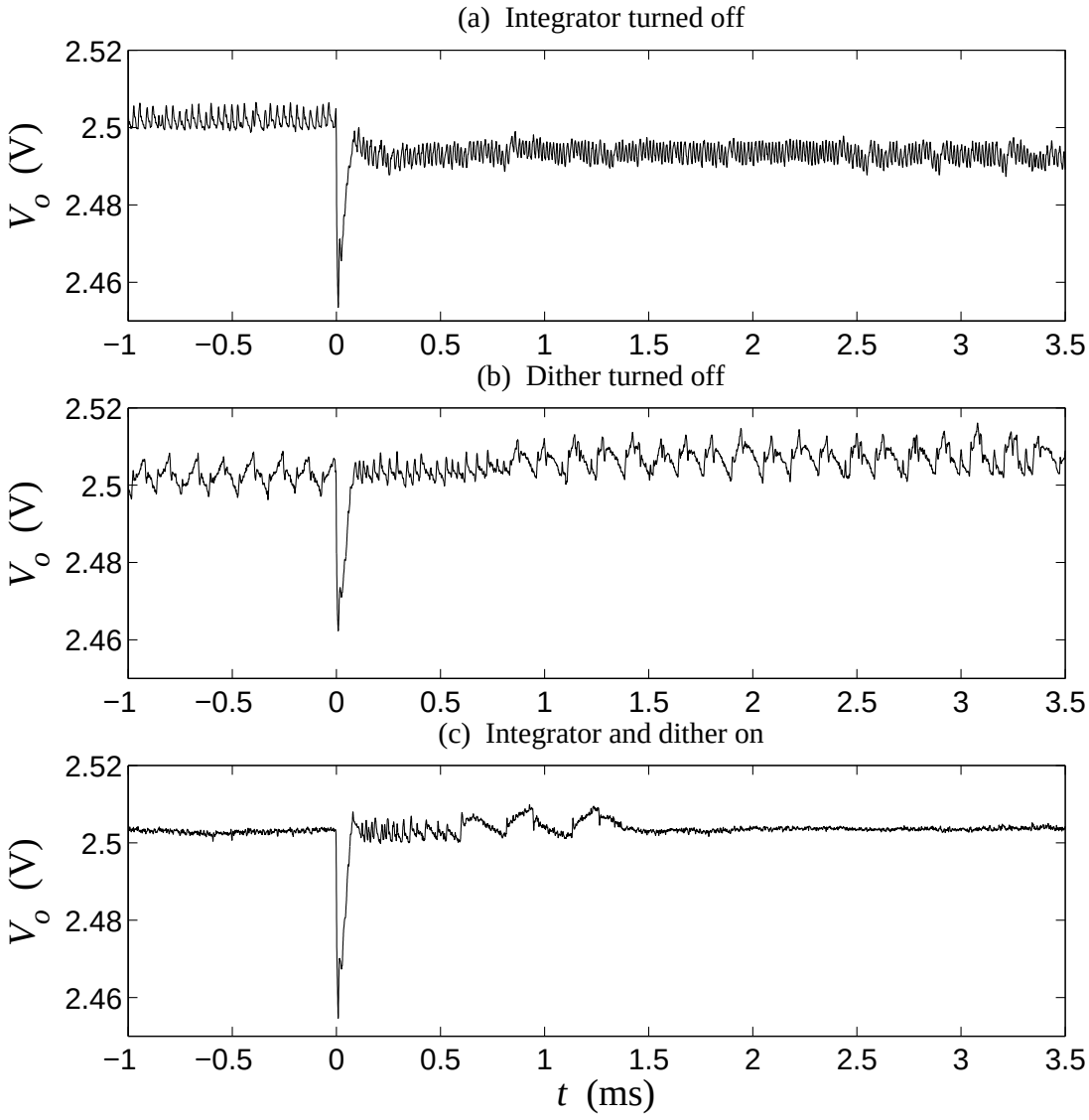


Figure 3.12: Experimental steady-state behavior and transient response of the prototype buck converter with and without integral feedback and dither. Load current steps from 0.5 A to 12 A at $t = 0$.

Chapter 4

Multi-Mode Buck Control with Adaptive Synchronous Rectifier Scheduling

4.1 Introduction

As discussed in Chapter 1 improving power-conversion efficiency is of paramount importance for both battery-operated and line-connected digital applications. The synchronous buck converter (Fig. 4.1) and its multi-phase version (Fig. 2.1 in Chapter 2) are commonly used to regulate the voltage to digital processors. Under different load conditions there are different optimal gating patterns for the switches. For large load currents the converter runs in continuous-conduction mode (CCM) characterized by strictly positive steady-state inductor current. At light load, the converter can run in discontinuous

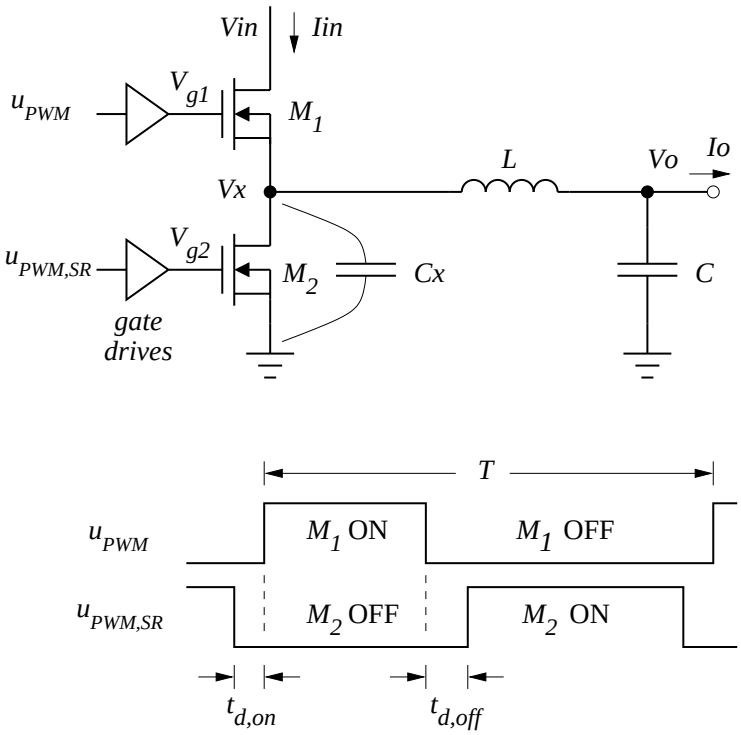


Figure 4.1: Buck converter with synchronous rectifier (M_2), and the corresponding MOSFET control signals.

conduction mode (DCM), where the inductor current is zero during part of the switching period. At no load or very light load the switching losses dominate, and thus it is advantageous to decrease the switching frequency by entering a fixed-on-time, variable-frequency mode (e.g., pulse-frequency modulation (PFM), burst mode, or pulse skipping). Finally, the synchronous rectifier (SR) switch (M_2 in Fig. 4.1) has to be gated appropriately, so as to minimize power losses while the inductor current is circulating through the ground loop.

Multi-mode control of voltage regulators for hand-held portable electronics, such as cellular phones and PDA's, is quite common since high efficiency is required over a wide load range (typically tens of mA to a few A). A plethora of approaches has been proposed: Most designs operate in CCM at heavy loads in either fixed-frequency PWM

control [80, 64, 111], hysteretic control [4], or fixed-on-time control [99]. At light loads the converter is typically operated in either PFM [99, 12, 64, 111] or fixed-frequency DCM [80]. Some commercial parts use "burst-mode" control at light loads, which produces trains of fixed-frequency pulses followed by off periods [27]. There are also designs that operate in the same mode at all loads such as variable-frequency DCM [12], and adaptive resonant fixed-frequency switching [92]. Some approaches gate the SR in DCM [99, 12], while others turn it off completely [4, 80, 111]. The transition between the low-power and high-power modes is typically implemented based on some estimate of the load current and possibly the input voltage [4, 80, 64]. Some controllers use analog implementations [92, 4, 99], while others are digital [12, 80, 64, 111].

Multi-mode control in higher-power portables such as laptops is less frequent, however it is becoming increasingly relevant. A method proposed in [17] uses PWM CCM with a SR at heavy loads and can turn off the SR based on a command from the host microprocessor indicating low-current state. On the other hand, the FAN5093 microprocessor voltage-regulator IC [89] turns off the SR when negative inductor current is detected, allowing the converter to automatically switch to DCM at light loads. This part also allows disabling one of its two phases for improved light-load efficiency.

The majority of existing methods for SR control in buck converters rely on high-bandwidth sensing of the gate and drain voltages of the switch MOSFET's, using these signals to adjust the SR timing in order to emulate an ideal diode [40]. For example, an ideal diode can be emulated by turning on the low-side MOSFET when its drain-source voltage collapses to zero, and turning off the low-side MOSFET when its drain current decays to

zero. The drain current can be sensed via the MOSFET on-state drain-source resistance. Direct implementations of this approach (e.g., in [40]) could suffer from undesirable body-diode conduction intervals due to control and MOSFET switching delays.

Adaptive SR methods have been introduced to overcome control and MOSFET switching delays by predictively setting the SR timing edges based on information from previous cycles [92, 3, 43]. This technique has been used in a commercial digital implementation [52]. It still relies on MOSFET gate and drain voltage sensing, which has to be done on each phase leg in a multi-phase converter, and may require an estimate of the MOSFET threshold voltage. Further, this method might force the converter in CCM at light loads, instead of allowing it to enter DCM which is more power efficient.

Since the ultimate objective of SR control is to decrease losses, an alternative approach is to adjust SR timing so as to directly minimize some measure of the power loss. This basic idea is behind the method developed in this chapter, and has been pursued in a number of other works as well. In power electronic systems the perturbation naturally introduced by the switching action can be used to optimize the system operation on-line [59, 48], and it has been suggested to use this approach for SR control [39]. However, this technique cannot successfully adjust parameters which are not directly related to the switching action, such as the SR dead-times. More recently, a method proposed in [2] steps the SR dead-time and measures the resulting change in the converter input current which is related to the efficiency. The dead-time is adjusted in direction of increasing efficiency. Only turn-on dead-time optimization is demonstrated, with the turn-off dead-time kept fixed. A similar method proposed in [118] adjusts the SR dead-times so that the duty-ratio

command is minimized, corresponding to maximized efficiency. Each dead-time is initially set to some large value and gradually decreased until the duty-ratio command starts to increase, at which point the algorithm stops. The algorithm is run subsequently for the turn-on and turn-off dead-times. It is turned off until a "large" transient is detected, after which it is run again. It is suggested that after a transient the algorithm starts from the point it reached during the previous optimization run. Using the duty-ratio command as a cost function for the dead-time optimization has the major benefit of not requiring sensing and analog-to-digital conversion of any additional quantities besides the output voltage.

Unfortunately, the search algorithms in both [2] and [118] have little robustness to transients and can easily converge to a sub-optimal SR timing pattern in the presence of even minor disturbances. Further, the optimization of the turn-on and turn-off dead-times cannot be done simultaneously. Finally, the speed of convergence to the new optimum after a load transient is limited by feedback stability constraints of the adaptive loop. These could be considerable disadvantages in microprocessor voltage regulator applications where the load current may change rapidly and frequently over a wide range (see Chapter 2).

We present an alternative approach based on controlling (scheduling) the SR timing as a direct function of load current, since the optimal SR timing depends strongly on the load current. A load current measurement or estimate is typically available to the controller since it is used for load-line control in VR's. The function relating the optimal SR gating to the load current can be determined off-line and programmed in the controller. Alternatively, it can be obtained on-line by dynamically minimizing the converter power loss via multi-parameter extremum seeking [42, 41, 97, 5]. The extremum-seeking method

introduces perturbations in the parameters which are to be optimized (SR dead-times in this case) and measures the gradient of a cost function (power loss, or related quantities). The gradient information is used to adjust the parameters in direction of improving cost function. Quantities besides the power loss which could be used as cost functions are the input current, temperature, or the closed-loop duty ratio, as suggested in [118].

This method does not suffer from the sensitivity to transients and the speed limitations of the algorithms in [2] and [118]. The sensitivity to transients is greatly reduced by demodulating the cost function with the perturbation signal, thus sharply attenuating disturbances at other frequencies. The load current adjusts the SR dead-times in a direct, feedforward manner, which is not limited by feedback stability constraints, and can therefore provide very fast response to load transients. This capability could be very important in applications such as modern microprocessor supplies, where the load current can change with a high frequency and slew rate. Further, this method can optimize multiple variables (such as the turn-on and turn-off dead-times) simultaneously using orthogonal perturbations. This approach requires only coarse sampling of the scheduling variable (e.g., the output current) at a rate commensurate with the desired speed of SR timing adjustment. The inductor current can be used as a scheduling variable instead of the load current. Slow variations of other converter parameters on which the power loss depends, such as input (battery) voltage and ambient temperature, are compensated for by the extremum-seeking algorithm. Only low-bandwidth sensing of the quantity characterizing the converter power loss is required for the extremum-seeking adaptation. This method is particularly well-suited for a digital controller implementation, since it uses low-rate computations and data

storage, thus not requiring analog-to-digital sampling rates beyond the converter switching frequency, which is typically in the range of hundreds of kHz to a MHz.

Importantly, with the proposed SR control method, the converter automatically enters DCM at light loads by virtue of the fact that the power-loss in DCM is lower than in CCM, and the extremum-seeking algorithm converges there. Further by imposing a minimum duty-ratio, which is straightforward to implement in a digital controller, the converter will automatically enter pulse-skipping mode at very light loads, effectively decreasing the switching frequency and the associated switching losses. Thus, the same controller structure is used in both fixed-frequency PWM and variable-frequency pulse-skipping modes. In multi-phase converters, some of the phases could be disabled at light loads to further improve efficiency.

Multi-mode control of buck converters is discussed in Section 4.2. Section 4.3 develops load-current-scheduled SR control with loss-minimizing adaptation, and further shows how a similar approach could be used for fast duty-ratio adjustment in DCM. Section 4.4 demonstrates loss-minimizing scheduled SR control and multi-mode operation on a digitally-controlled 100 W 4-phase buck converter. Finally, Section 4.5 discusses the proposed techniques in view of the experimental results.

4.2 Multi-Mode Buck Control

4.2.1 Buck Converter Modes

As discussed in Section 4.1, to ensure high efficiency over a wide load range, the buck converter could be operated in different modes depending on the load current. A

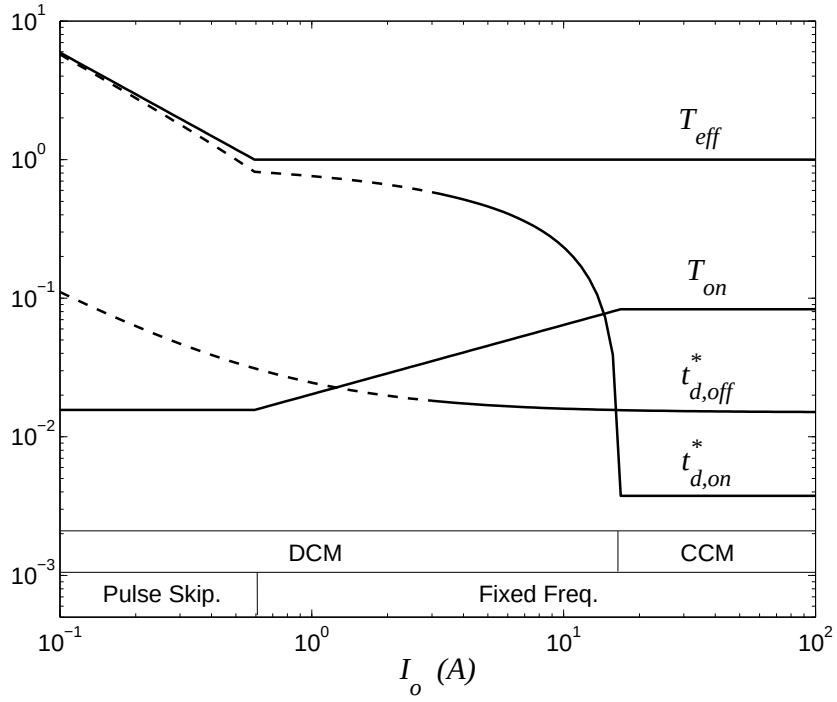


Figure 4.2: Timing parameters of the buck-converter control switch and synchronous rectifier for different modes of operation. All parameters are normalized by the fixed-frequency switching period T, and both axes are logarithmic.

representative mode diagram, giving the switches' timing parameters as a function of load, is shown in Fig. 4.2. Parameter T_{eff} is the effective switching period, which is equal to T is fixed-frequency operation (refer to Fig. 4.1). Parameter T_{on} is the on-time of control (high-side) switch M_1. Parameters $t^*_{d,on}$ and $t^*_{d,off}$ are the optimal turn-on and turn-off dead-times, respectively, of the SR (low-side) switch M_2. The modes of operation of the buck converter are cataloged below:

Fixed-frequency CCM

At heavy load the converter operates in CCM with a fixed switching period T. The control switch on-time is $T_{on} = DT = MT$, where D is the duty ratio, $M = V_o/V_{in}$ is

the conversion ratio, and V_{in} and V_o are the input and output voltages, respectively. The optimal turn-off dead time $t^*_{d,off}$ depends on the intrinsic turn-off delay $t_{d,off0}$ of the control switch M_1, and the time it takes to discharge the switching node capacitance C_x,

$$t^*_{d,off} = \frac{V_{in}C_x}{I_o} + t_{d,off0}, \tag{4.1}$$

where I_o is the load current. Further, the optimal turn-on dead time $t^*_{d,on}$ is a small constant, $t_{d,on0}$, preventing conduction overlap between the control switch and the SR.

The power losses in CCM are typically dominated by conduction losses caused by the load current and the inductor current ripple $\Delta I_{L,CCM}$ flowing through the switches and the inductor [16, Ch. 5], [43],

$$P_{loss,cond,CCM} = r'_L \left(I_o^2 + \frac{1}{12}\Delta I_{L,CCM}^2 \right), \tag{4.2}$$

where r'_L is the average switch resistance in series with the inductor resistance, and

$$\Delta I_{L,CCM} = \frac{V_{in}TM(1-M)}{L}, \tag{4.3}$$

where L is the total inductance (all inductors in parallel in a multi-phase converter).

Fixed-frequency DCM

At lighter loads, the converter enters DCM if the SR is gated so that it does not allow negative inductor currents. This happens below load current

$$I_{o,crit} = \frac{1}{2}\Delta I_{L,CCM}. \tag{4.4}$$

The duty ratio now depends on the load current,

$$D = \sqrt{\frac{2LI_oM}{V_{in}T(1-M)}}. \tag{4.5}$$

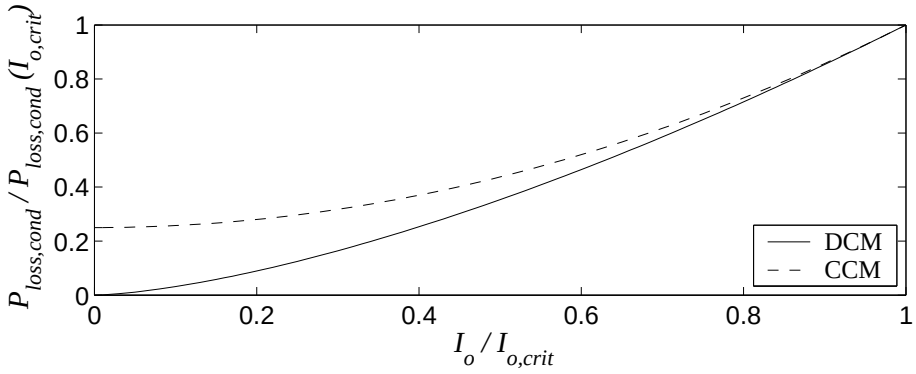


Figure 4.3: Normalized conduction power loss in discontinuous conduction mode (DCM) and continuous conduction mode (CCM).

The optimal turn-off dead time still follows (4.1). The optimal $t_{d,on}$, on the other hand, varies substantially as a function of the load current,

$$t^*_{d,on} = T\left(1 - \frac{D}{M}\right) + t_{d,on0}. \tag{4.6}$$

In DCM, this parameter corresponds to the time the inductor current is zero.

It can be shown that the conduction power loss in DCM is

$$P_{loss,cond,DCM} = \frac{r'_L}{3}(2I_o)^{3/2}\Delta I^{1/2}_{L,CCM}. \tag{4.7}$$

Fig. 4.3 gives the normalized conduction power loss in CCM (4.2) and DCM (4.7). Clearly, allowing the converter to enter DCM by appropriately timing the SR at load currents below $I_{o,crit}$ results in significant power savings.

Variable-Frequency Pulse Skipping

At very light load the converter loss is dominated by switching losses which are proportional to the switching frequency [16, Ch. 5],

$$P_{loss,sw} = \left[\frac{1}{2}C_x V^2_{in} + (C_{g1} + C_{g2})V^2_G\right] f_{sw}, \tag{4.8}$$

where C_{g1} and C_{g2} are the high-side and low-side gate capacitances, respectively, and V_G is the gate drive voltage swing. Thus, it is advantageous to allow variable frequency operation at very light loads. This can be implemented in a straightforward way with a digital controller by limiting the minimum duty ratio to a value D_{min}. (Note that there is an automatic minimum duty ratio limit of one DPWM hardware LSB.) The duty ratio limit results in pulse-skipping behavior, effectively reducing the switching frequency. The converter is pulse skipping for

$$I_o < \frac{D_{min}^2 V_{in} T (1 - M)}{2LM}, \tag{4.9}$$

with the *average* switching period following approximately

$$T_{eff} \approx \frac{V_{in} T_{on}^2 (1 - M)}{2LI_o M}. \tag{4.10}$$

The pulse width T_{on} depends on the digital PID parameters and the integrator state. The integral term forces the average error to zero, thus driving the output voltage periodically among the -1, 0, and $+1$ error bins, resulting in a V_o limit cycle centered at the zero-error bin. Hence, the V_o limit cycle typically has an amplitude of about 2 ADC bins (for examples see Fig. 4.11(d)–(f) in Section 4.4).

4.2.2 Ancillary Issues

Phase Scaling

In a multi-phase buck converter, which is the architecture typically used in microprocessor VR's, additional power savings can be realized at light load by disabling some of the phases [89]. This approach completely eliminates the switching losses which would otherwise be contributed by the disabled phase legs.

Effectiveness of Synchronous Rectification at Light Load

As discussed in Section 4.1, some low-power converter designs gate the SR in very-light-load variable-frequency operation, while others turn it off altogether. The choice depends on the efficiency contribution of the SR. The total energy dissipated in the SR per pulse with on-time T_{on}, assuming the SR is on while the inductor current discharges to zero, is

$$E_{SR} \;=\; \frac{r_l V_{in}^2 T_{on}^3 (1-M)^3}{3L^2 M} \;+\; C_{g2} V_G^2 \;+\; E_{SR,ctrl}, \tag{4.11}$$

where r_l is on-resistance of the SR, and $E_{SR,ctrl}$ is the energy overhead of the SR control circuit. The first term corresponds to the energy dissipated in the on-resistance of the SR. The second term corresponds to the gate switching loss. On the other hand, if the SR is off, the current discharges through the body diode of the low-side switch resulting in energy loss of

$$E_D \;=\; \frac{V_D V_{in} T_{on}^2 (1-M)^2}{2L(M + V_D/V_{in})} \;+\; V_{in} Q_r, \tag{4.12}$$

where V_D is the body-diode forward voltage, and Q_r is the reverse-recovery charge [28, Ch. 4]. For a particular design, it is beneficial to use the SR at light loads if the energy saved by it is more than the energy dissipated in it, namely, if $E_D > E_{SR}$.

The different modes described in this section are straightforward to implement with a digital controller. The SR timing can be scheduled as a function of the load current, and optimized on-line as discussed in the next section. Optimal SR timing ensures appropriate transition between CCM and DCM. The transition to pulse skipping is automatic, given that a minimum duty ratio is imposed. Importantly, the PID controller structure does not need to be modified for the different modes, resulting in a simple implementation. Additional

features such as scaling the number of phases and disabling the synchronous rectifier at light loads can be easily scheduled by the load current as well.

Finally, it should be noted that at light loads there is a design trade-off among the different possible modes of operation: Pulse skipping and reducing the number of phases can decrease power loss, at the price of increased output voltage ripple. Fixed-frequency DCM, on the other hand, has lower ripple, at the expense of higher switching losses. Both of these alternatives are substantially more efficient than CCM operation.

4.3 Load-Scheduled Loss-Minimizing Synchronous-Rectifier Control

As discussed above, the SR timing parameters can be scheduled as a function of the load current. The functions $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ can be derived from theoretical equations, such as (4.6) and (4.1), or obtained from off-line power-loss measurements, and programmed into a look-up table. However, these approaches do not compensate for parameter variability with time and ambient conditions. For example, the optimal SR timing could change with input (e.g., battery) voltage, temperature, component drift, etc. In this section we present an adaptive algorithm which resolves these issues by determining the optimal SR scheduling on-line.

The objective is to adjust the SR timing parameters $t_{d,on}$ and $t_{d,off}$ so as to minimize the converter power loss P_{loss} for each load current value. The algorithm is identical for $t_{d,on}$ and $t_{d,off}$, and therefore, we will present it for a general variable t_d. We

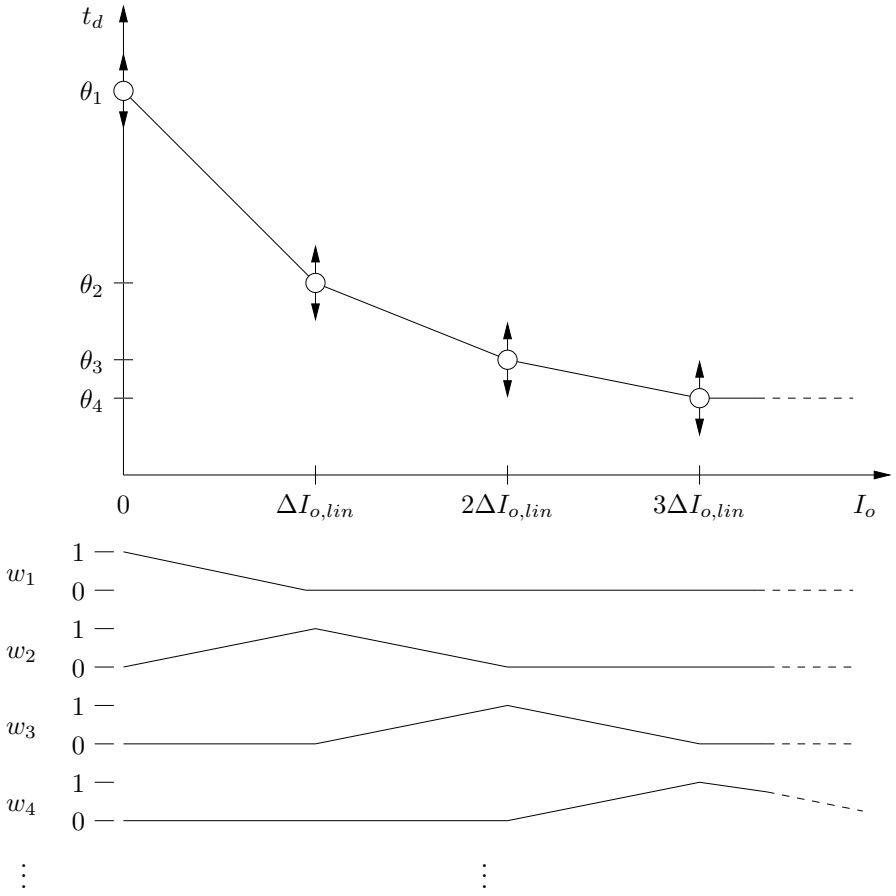


Figure 4.4: Piecewise linear function modeling dead-time $t_d(I_o)$ (top), and associated vertex weights (bottom).

parameterize each of the dead-time functions

$$t_d = t_d(I_o, \mathbf{\Theta}) \tag{4.13}$$

with parameter vector $\mathbf{\Theta} = [\theta_1, \cdots, \theta_m]$. In this work we use a piecewise linear function to implement (4.13), where θ_l is the l-th vertex of the function (Fig. 4.4). The m vertices are positioned at every $\Delta I_{o,lin}$ increment of I_o. They are weighted by a vector $\mathbf{W}(I_o) = [w_1(I_o), \cdots, w_m(I_o)]$ toward $t_d(I_o)$,

$$t_d(I_o, \mathbf{\Theta}) = \mathbf{W}(I_o)\, \mathbf{\Theta}^T. \tag{4.14}$$

The w parameters characterize the fractional distance of I_o to the two neighboring vertices,

$$\begin{aligned} w_l &= 1 - (I_o/\Delta I_{o,lin} - \lfloor I_o/\Delta I_{o,lin} \rfloor), \\ w_{l+1} &= I_o/\Delta I_{o,lin} - \lfloor I_o/\Delta I_{o,lin} \rfloor, \\ w_\lambda &= 0, \qquad \text{for} \qquad \lambda \neq l, l+1, \end{aligned} \tag{4.15}$$

(see Fig. 4.4), where the vertex index l is the integer part of $I_o/\Delta I_{o,lin}$,

$$l = \lfloor I_o/\Delta I_{o,lin} \rfloor, \tag{4.16}$$

and $\lfloor x \rfloor$ is the floor function giving the greatest integer less than or equal to x. Thus the value of $t_d(I_o)$ is obtained by linear interpolation between the two nearest vertices θ_l and θ_{l+1}. The increment size $\Delta I_{o,lin}$ can be constant or can depend on I_o to suit a particular shape of the fitted function. In the latter case the indexing in (4.16) and (4.15) should be adjusted appropriately. Other parametrization approaches could be used, such as realizing (4.13) with a smooth function, and adjusting its parameters (e.g., a polynomial with tunable coefficients).

To determine the optimal value of the parameter vector, a perturbation-based extremum seeking algorithm is used. Fig. 4.5 gives a block diagram of the adaptive controller. The controller introduces small, zero-mean perturbations $\tilde{t}_d$ in t_d, at frequency f_d, resulting in modulation of the converter power loss. This, in turn, produces modulation of the temperature of the power train, which can be measured with thermal sensors. The transfer characteristic between the converter power loss and the temperature measurement is modeled by $F_t(s)$. The power loss or temperature measurement is passed through an optional filter $F_p(s)$ yielding signal p which is to be minimized. Filter F_p can be high-pass, blocking

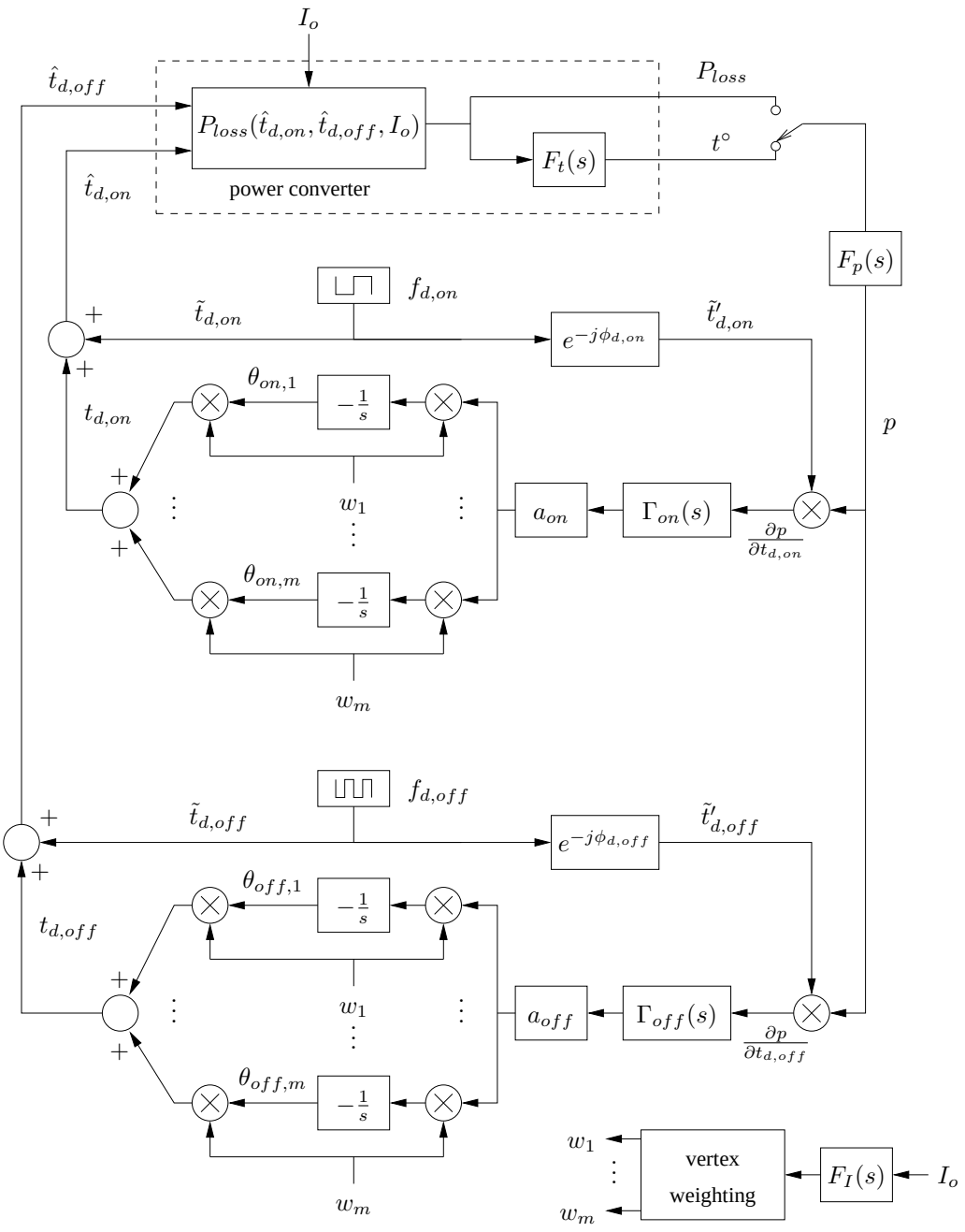


Figure 4.5: Block diagram of synchronous rectifier adaptive control using multi-parameter extremum seeking.

the DC level of the signal, since only the AC components of the signal at the perturbation frequencies are needed for the gradient estimation algorithm [97, 41]. Note that since the power loss signal p can be AC-coupled, simple window ADC structures could be used to quantize it [78]. The power loss gradient with respect to the dead-time can be obtained by demodulating the power loss with a delayed version of the perturbation signal $\tilde{t}'_d$, since

$$\frac{\partial p(t)}{\partial t_d} \propto \int_{t-1/f_d}^{t} p(t')\tilde{t}'_d(t')\, dt', \tag{4.17}$$

where $1/f_d$ is the perturbation period (see [97, 41]). The delay ϕ_d models the lag of the converter and sensor response, and the data acquisition and processing delay. Optionally, the gradient estimate can be filtered through a low-pass filter $\Gamma(s)$ to reduce the $2 \times f_d$ ripple resulting from the perturbation signal [97]. Based on the gradient, the parameter vector is adjusted in a direction which decreases the power loss,

$$\theta_\lambda[k+1] \;=\; \theta_\lambda[k] \;-\; \alpha\, w_\lambda[k]\, p[k]\, \tilde{t}'_d[k]\,, \qquad \text{for} \qquad \lambda = 1, \cdots, m. \tag{4.18}$$

This update law is given in discrete time with index k, which is appropriate for a digital implementation. Gain $\alpha = aT_{adapt}$, where T_{adapt} is the adaptive algorithm time step, is the discrete-time equivalent of continuous-time parameter a in Fig. 4.5, and determines the speed of parameter adaptation. Weighting parameter w is given by (4.15), and is hence non-zero only for $\lambda = l, l+1$. Thus, at each iteration the two vertices of $t_d(I_o, \mathbf{\Theta})$ which bracket the load current are adjusted, according to the vertex distance from I_o.[1] As a result, each vertex is adjusted based on gradient information from a $2 \times \Delta I_{o,lin}$ current

[1]Since multiplication by the weighting parameters w_λ is applied twice in the adaptive loop, in (4.14) and in (4.18), the adaptive loop gain is varied by a factor of two between the condition when I_o is centered between two vertices, and the condition when I_o coincides with a vertex. This gain variation does not affect significantly the operation of the algorithm, since the adaptation occurs at a slow rate.

bracket, resulting in robustness to sensing noise and small undulations of the power loss characteristic due to parasitic ringing. The load current could be low-pass filtered with F_I before the vertex weighting computation (4.15), thus controlling the speed of response of the dead-times to load changes. The two perturbation signals $\tilde{t}_{d,on}$ and $\tilde{t}_{d,off}$ are chosen to be zero-mean and mutually orthogonal to allow independent estimation of $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$, respectively. The perturbation signals can be sine or square waves at two different frequencies, for example. Importantly, this algorithm does not need to run fast, since it computes optimal curves for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$, thus requiring only identification of the constant or slowly varying parameters describing these functions, and not the rapidly changing parameters $t_{d,on}$ and $t_{d,off}$ themselves. The speed of response of the SR timing parameters is independent of the speed of the perturbation-based adaptation, and is set by F_I which can be made as fast as practical.

In the adaptation problem discussed above there are four time scales: the converter dynamics, the load current dynamics, the perturbation frequencies, and the parameter estimator time constant. To ensure parameter convergence to a small neighborhood of their optimal values, the system has to be designed so that the parameter estimator is slower than the perturbation signals, which should be slow compared to the converter dynamics [97]. In some applications, such as microprocessor supplies, the load current can vary at speeds comparable to the converter dynamics. This variation tends to be rejected by the adaptive algorithm since it is not correlated with the perturbation signals.

4.3.1 Other Applications: Duty-Ratio Adaptation

The SR optimization framework developed above is essentially a type of adaptive feedforward control. It consists of scheduling a control variable as a feedforward function of the load current (or any other measured exogenous parameter which varies rapidly over a wide range), and then adaptively estimating this function. This approach can be applied to number of other control problems in power converters. For example, from equation (4.5) in Section 4.2 it is clear that in DCM the steady-state duty-ratio command varies over a wide range as a function of I_o, unlike in CCM where it is ideally constant ($D = M$). The duty-ratio control laws discussed in Chapter 2, and transformed to a digital implementation in Chapter 3, are designed for operation in CCM. Although the closed-loop system is still stable in DCM, due to the first-order transfer characteristic of the power train in DCM [28, Ch. 11], the load transient response may be unsatisfactory since the integrator has to slew over a wide range (for example, see Fig. 4.12 in Section 4.4 later in the chapter). This problem can be remedied by an adaptive scheme similar to the one for synchronous rectifier timing presented above. Instead of a single integrator state D_i in the PID control law (3.1), a vector of m integrators $\mathbf{D_i} = [D_{i,1}, \cdots, D_{i,m}]$ is used, spanning the converter operating range. The integral contribution to the PID control law is now a direct function of the load current,

$$D_i(I_o) = \mathbf{W}(I_o)\,\mathbf{D_i}^T. \tag{4.19}$$

Weighting vector $\mathbf{W}(I_o)$ is defined in (4.15). The integrators are updated by a law analogous to (4.18),

$$D_{i,\lambda}[k+1] = D_{i,\lambda}[k] \;+\; w_\lambda[k]\,D_e[k], \qquad \text{for} \qquad \lambda = 1, \cdots, m, \tag{4.20}$$

where D_e is the digitized error signal. Equations (4.19) and (4.20) now replace the standard PID integrator (3.2). In general, this techniques could effect fast transient response for power converter topologies in which the duty ratio varies substantially over different loading conditions.

4.4 Experimental Results

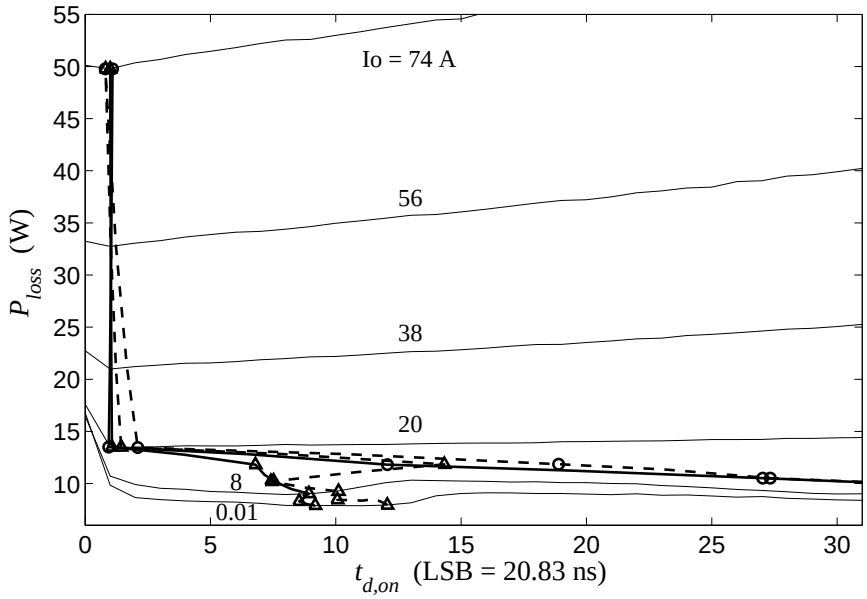
The multi-mode control strategy with adaptive SR scheduling was tested on a digitally-controlled 100 W 4-phase buck converter with parameters given in Table 4.1. The switching controller with a PID feedback law was implemented with a Xilinx FPGA board clocked at 48 MHz. The adaptive synchronous rectifier controller was implemented with a DSPACE data-acquisition board to sample the power loss and temperature data and send the $t_{d,on}$ and $t_{d,off}$ commands to the FPGA. Figures 4.6 and 4.7 show the static converter power loss (horizontally-oriented curves), measured off-line, as a function of the SR timing and parameterized by load current. If the SR is kept off, the converter enters DCM for load currents below 19 A, consistent with (4.4) in Section 4.2. As a result, at light loads the global power loss minimum shifts to large $t_{d,on}$ values [Fig. 4.6(b)], corresponding to the SR turning on when the inductor is discharging, and turning off when the inductor current becomes zero. Under these conditions another local minimum is observed for small $t_{d,on}$ values, denoted with $\vartriangle$'s in Figures 4.6(a,b), corresponding to the converter accomplishing soft-switching by letting negative inductor current charge up the switching node capacitance to V_{in} [28, Ch. 20], [92], [also see Fig. 4.11(b)]. Further note that the abrupt dips in power loss at the right end of Fig. 4.6(b) correspond to the SR being off all the time and thus not

contributing switching losses. In Fig. 4.7 the optimum $t_{d,off}$ is approximately constant at heavy loads, and decreases by a small amount at light loads, which appears due to reduced high-side switch turn-off delay. Finally, the minimum duty-ratio command is limited to two LSB's, forcing the converter to enter pulse skipping mode for load currents below about 2 A [consistent with equation (4.9)]. The abrupt drop in power loss for large $t_{d,on}$ at very light loads is due to the transition to pulse-skipping.

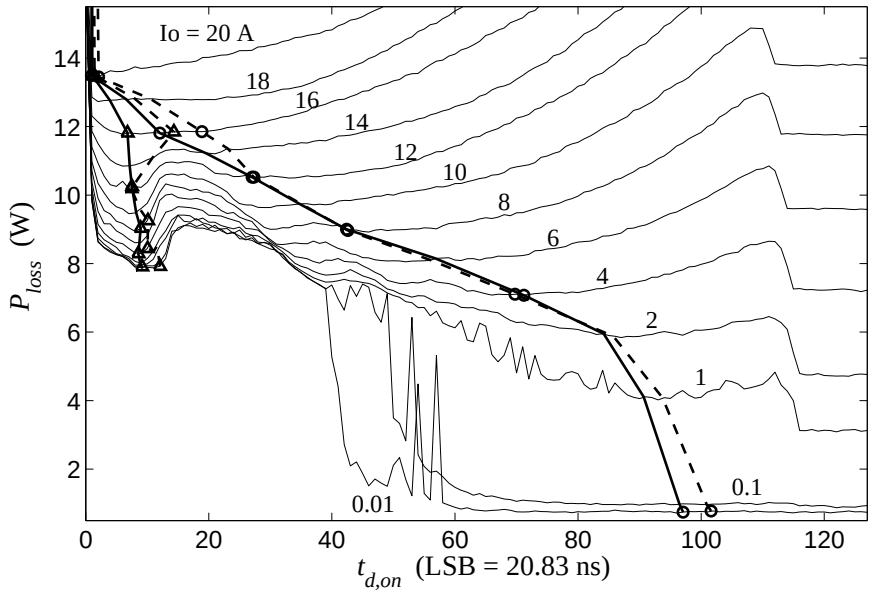
The adaptive SR timing control was implemented alternately with direct power-loss minimization and temperature minimization. The piecewise linear curves for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ have 7 vertices each: 6 of them at 4 A steps between 0 and 20 A, and another vertex at 75 A. The adaptive controller parameters corresponding to the block diagram in Fig. 4.5 are listed in Table 4.2. The power loss sensing was done by sampling the input and output voltage and current. The gain of filter $F_p(s)$ lumps the signal conditioning gain before the gradient estimator. The power loss signal is normalized by the load current (above 1 A) to reduce the gain variation of the adaptive loop over the full load range, and to alleviate the interference of load transients with the gradient estimation algorithm. Following each perturbation edge, N_{blank} samples of the power-loss (or temperature) signal $p(t)$ are discarded to reduce interaction between the voltage-loop dynamics and the gradient estimator. The bandwidth of filter $F_I(s)$ was set relatively low, since the load switching in the experiments was done manually at a slow rate (see Fig. 4.8). In applications with fast load switching, the bandwidth of $F_I(s)$ can be increased—a suitable choice could be to make it equal to the closed-loop voltage-regulation bandwidth (for this setup it is about 18 kHz).

Table 4.1: 100 W prototype buck converter parameters

	Power Train	
N	number of phases	4
V_{in}	input voltage	12 V
r_s	input source impedance	1 mΩ
$r_{h\phi}$	high-side switch on-resistance	12 mΩ
$r_{l\phi}$	low-side switch on-resistance	3.6 mΩ
L_ϕ	phase inductors	330 nH
$r_{L\phi}$	inductor ESR & trace resistance	1 mΩ
C	output capacitance	36×100 μF (ceramic)
τ_C	output capacitor ESR time constant	0.8 μs
	PID Controller	
V_{ref}	reference voltage	1.3 V
f_{sw}	switching frequency	375 kHz
f_{samp}	V_o sampling frequency	1.5 MHz
N_{adc}	effective ADC resolution	10 bit
N_{dpwm}	DPWM hardware resolution	7 bit
N_{dith}	dither resolution	4 bit
K_p	proportional gain	2^2
K_i	integral gain	2^{-4}
K_d	derivative gain	2^6
t_{delay}	controller delay	0.7 μs
f_e	error amplifier −3 dB bandwidth	160 kHz
$D_{c,min}$	minimum duty-ratio command	2 LSB (1 LSB = 20.83 ns)
	Loop Gain	
PM	phase margin	40°
GM	gain margin	18 dB
f_c	unity gain frequency	18 kHz

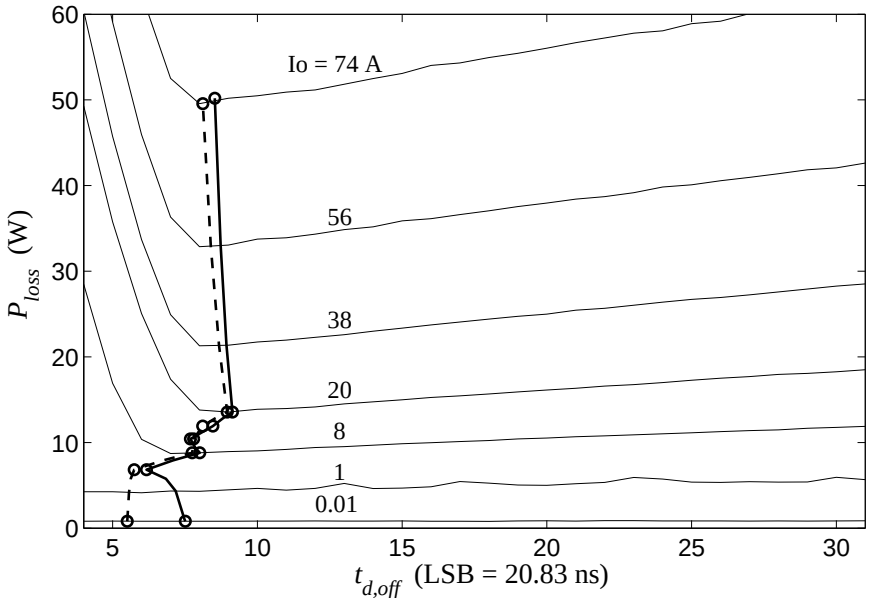


(a) heavy loads

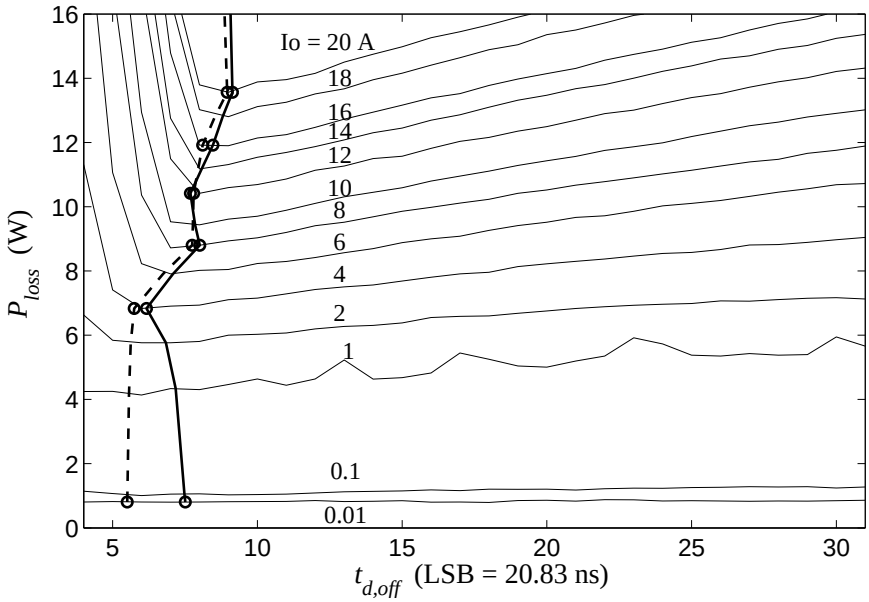


(b) light loads

Figure 4.6: Power loss as function of $t_{d,on}$ parameterized by load current. Thicker lines depict optimal $t_{d,on}$ locus, determined by on-line extremum seeking with power-loss (solid line) and temperature (dashed line) minimization. Curves denoted with $\circ$'s correspond to optimal DCM operation, while curves denoted with Δ's reflect soft-switching behavior.



(a) heavy loads



(b) light loads

Figure 4.7: Power loss as function of $t_{d,off}$ parameterized by load current. Thicker lines depict optimal $t_{d,off}$ locus, determined by on-line extremum seeking with power-loss (solid line) and temperature (dashed line) minimization.

Table 4.2: Adaptive synchronous-rectifier controller parameters

parameter	power optimization	temperature optimization
$\lvert F_t(s)\rvert$ @ 0.1 Hz	—	0.03 °C/W-s
$F_t(s)$ slow pole	—	0.001 Hz
$F_t(s)$ fast pole	—	0.5 Hz
$\lvert F_p(s)\rvert$	$1/I_o$ LSB/W	0.83 LSB-s/°C
$F_p(s)$ low-freq. −3 dB BW	—	0.016 Hz
$F_p(s)$ high-freq. −3 dB BW	3.4 kHz	64 Hz
$F_I(s)$ high-freq. −3 dB BW	3.4 kHz	100 Hz
$f_{d,on}$	100 Hz	0.2 Hz (square wave)
$\lvert\tilde{t}_{d,on}\rvert$	1 LSB	1 LSB (1 LSB = 20.83 ns)
$\phi_{d,on}$	15°	135°
$\Gamma_{on}(s)$ high-freq. −3 dB BW	2 Hz	0.004 Hz
α_{on}	$4 \cdot 10^{-2}$	$8 \cdot 10^{-3}$
$f_{d,off}$	200 Hz	0.4 Hz (square wave)
$\lvert\tilde{t}_{d,off}\rvert$	1 LSB	1 LSB (1 LSB = 20.83 ns)
$\phi_{d,off}$	31°	171°
$\Gamma_{off}(s)$ high-freq. −3 dB BW	2 Hz	0.004 Hz
α_{off}	$4 \cdot 10^{-2}$	$8 \cdot 10^{-3}$
N_{blank}	10	40
T_{adapt}	85.3 μs	85.3 μs

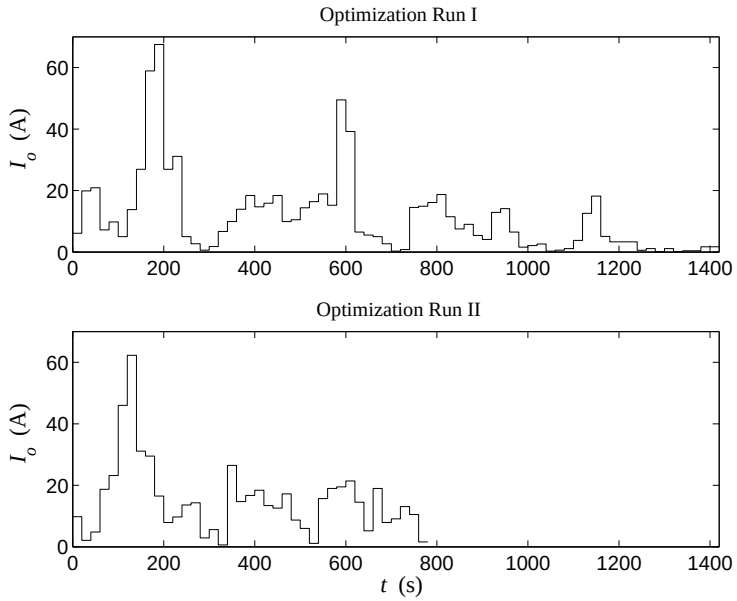
The temperature sensing was done with series-connected thermistors tightly mounted on the heat-sink tabs of all high-side and low-side power MOSFET's. One thermistor was mounted on each MOSFET. For this implementation, the temperature measurement response time (fast pole of $F_t(s)$) is at the order of a few seconds, due to the thermal impedance between each MOSFET die and its associated thermistor, requiring slow perturbation signals. (The slow pole of $F_t(s)$ is associated with the large shared heat sink on which the MOSFET's are mounted.) The temperature measurement is AC-coupled for reasons of data acquisition ADC range, as well as to reduce the impact of load transients on the gradient estimator. As a result, $F_p(s)$ is bandpass in this case. To further reduce gradient-estimator disturbances due to load transients, scaling by an appropriately filtered version of the load current could be implemented. This would be analogous to the approach used with direct-power-loss minimization above, but was not pursued in this setup.

Experimental runs testing the adaptive SR controller were conducted with direct power-loss minimization and, subsequently, with temperature minimization. The load current was varied over time, as shown in Fig. 4.8, to allow for estimation of the optimal $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ functions. The temperature minimization experiments took a few hours, due to the slow thermal sensor response in this setup. The direct power-loss minimization was much faster, taking a few minutes, mostly limited by the manual switching of the load. Two optimization runs are reported for each of the two (power-loss and temperature) experiments, corresponding to different initial conditions for $t_{d,on}$: "Optimization Run I" in Fig. 4.8 uses "initial conditions I" for $t_{d,on}$ given in Fig. 4.9(top), and the initial conditions for $t_{d,off}$ in Fig. 4.10. The resulting optimized curves for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$

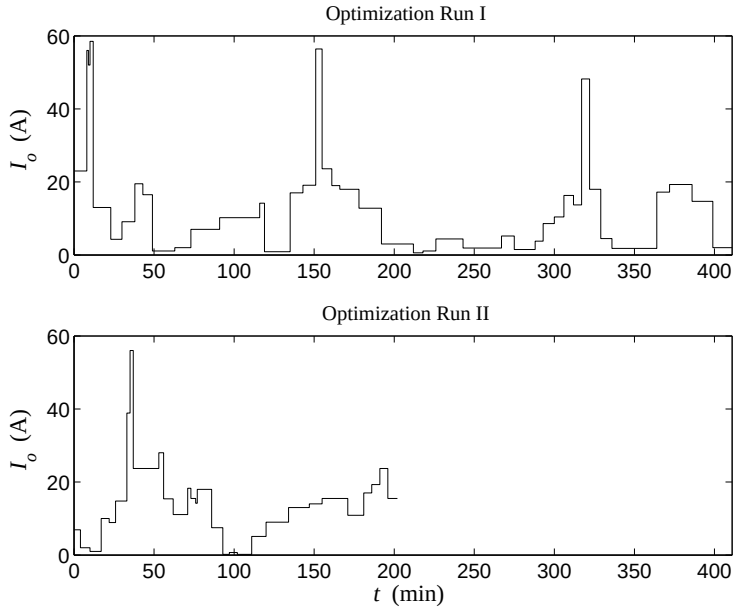
are plotted in Figures 4.9(top) and 4.10, respectively. With these initial conditions the converter converges to optimal DCM operation for load currents below 20 A. Parameter $t_{d,on}$ is constant for heavy load, but varies over a wide range for light load, since the optimal SR on-time is a strong function of the load current in DCM. This is predicted by equation (4.6) which is also plotted in Fig. 4.9(top), and matches the experimental data very well. Of course, the calculated curve requires the relevant power-train parameters to be known, which is not necessary for the on-line optimization. The optimal $t_{d,off}(Io)$ in Fig. 4.10 is dominated by the turn-off delay of the high-side switch, and is thus relatively flat.

"Optimization Run II" in Fig. 4.8 uses "initial conditions II" for $t_{d,on}$ given in Fig. 4.9(bottom), and the initial conditions for $t_{d,off}$ in Fig. 4.10. The resulting optimized curves for $t_{d,on}(I_o)$ are plotted in Fig. 4.9(bottom). In this case, the optimized $t_{d,on}(I_o)$ yields soft-switching behavior below 20 A. The results from the $t_{d,off}(I_o)$ optimization are virtually identical to the ones in Fig. 4.10 from Optimization Run I, and are therefore not plotted.

To better illustrate the optimality of the obtained $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ functions, they are also superimposed with thicker vertically-oriented curves on the power-loss plots in Figures 4.6 and 4.7, respectively. In Fig. 4.6 the optimized $t_{d,on}(I_o)$ curves corresponding to DCM operation are denoted with $\circ$'s, while the ones reflecting soft-switching behavior are denoted with Δ's. Clearly, the optimized curves follow closely the power-loss minima over the whole operating range (assuming the SR is gated). Further, the power-loss and temperature minimization experiments converge to very similar curves, with significant discrepancies occurring only at wide, flat regions of the power-loss characteristic. Thus, it



(a) power-loss minimization



(b) temperature minimization

Figure 4.8: Load current versus time for different optimization experiments. See corresponding initial and final values for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ in Figures 4.9 and 4.10, respectively.

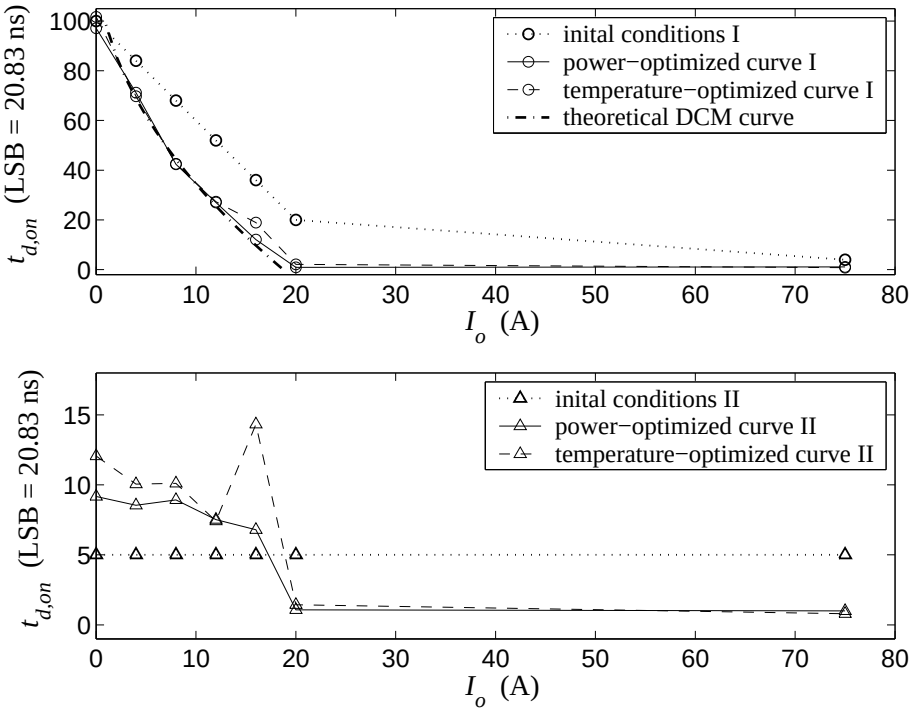


Figure 4.9: Dead-time $t_{d,on}$ versus I_o curves obtained by power-loss and temperature minimization experiments for different initial conditions. Top plot corresponds to DCM operation, while bottom plot reflects soft-switching behavior. This is alternative representation of the vertically-oriented curves in Fig. 4.6.

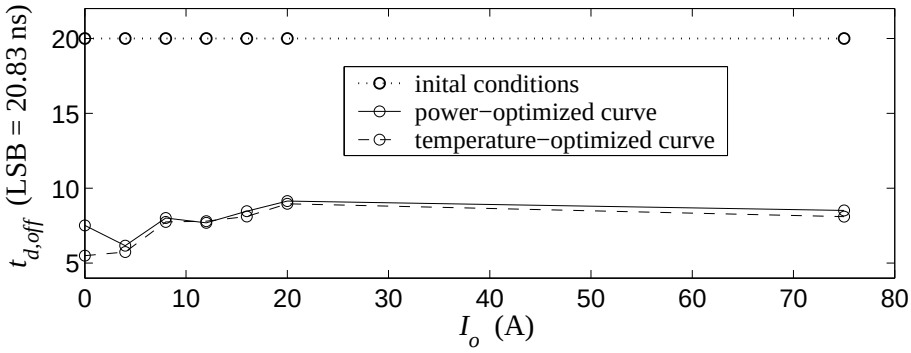


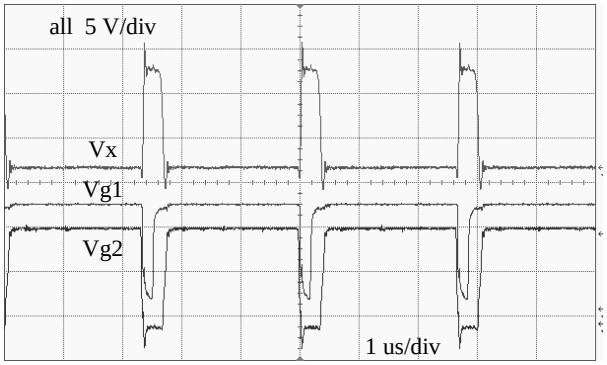
Figure 4.10: Dead-time $t_{d,off}$ versus I_o curves obtained by power-loss and temperature minimization experiments. This is alternative representation of the vertically-oriented curves in Fig. 4.7.

can be concluded that the algorithm successfully optimized the SR timing as a function of the load current with both direct-power-loss and temperature minimization. Depending on the initial condition for $t_{d,on}(I_o)$ and $t_{d,off}(I_o)$ the optimization may converge to DCM operation or to soft-switching at medium and light load. The desired mode of operation can thus be chosen by setting appropriate initial conditions, and further enforced by adding a software limit on the values $t_{d,on}(I_o)$ can take.

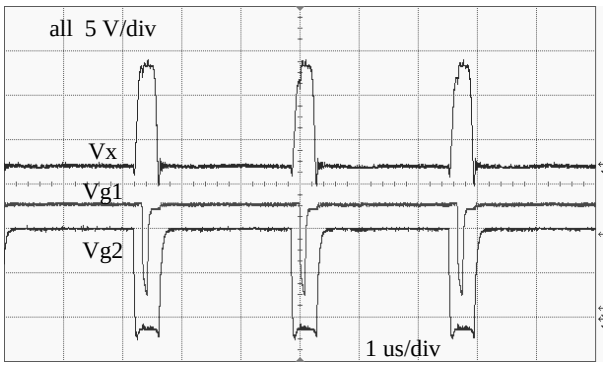
Fig. 4.11 is a gallery of the switching waveforms of one of the four converter phases, illustrating behavior at different load currents with optimized SR timing. Oscillogram (a) shows the converter in CCM at heavy load. Parameter V_{g1} is the high-side (implemented with PMOS) gate voltage, V_{g2} is the low-side (NMOS) gate voltage, and V_x is the switching node voltage (refer to the buck converter diagram in Fig. 4.1). Oscillogram (b) illustrates soft-switching behavior ($I_o = 10$ A, $t_{d,on} = 7$ LSB). Notice the switch-node voltage V_x rising before the high-side switch V_{g1} is turned on, due to negative inductor current charging up the parasitic switch-node capacitance. It could be the case that for designs with very high switching frequencies, the soft-switching mode has better performance than DCM, since it reduces the switching losses. Oscillogram (c) shows DCM operation with gated SR. Oscillograms (d)–(f) illustrate pulse skipping at very light loads. The converter settles into a quasi-limit-cycle behavior consisting of periodic switching bursts, followed by off periods. The *average* inter-pulse period is modeled by (4.10). Generally, the switching behavior within each burst is governed by the proportional and derivative terms of the PID control law: When V_o crosses from the zero-error ADC bin to the -1 error bin, an on-pulse is generated with width proportional to $K_p + K_d$. This pulse boosts V_o back into the zero-

error bin. No pulses are generated there, since the error is zero, and eventually V_o droops back into the -1 error bin, thus repeating the sequence. The repetitive transitions to the -1 error bin cause the PID integrator to slew up, eventually driving V_o in the $+1$ error bin. This forces an off-state while the integrator is discharging. Thus the alternation between burst and off state is determined by the integral term, which maintains the output voltage centered at the zero-error ADC bin. Note that the amplitude of the V_o limit cycle is about two ADC bin sizes ($\Delta V_{adc} = 11.7$ mV), implying switching among the -1, 0, and $+1$ error bins, which satisfies the zero average error condition enforced by the integral PID term.

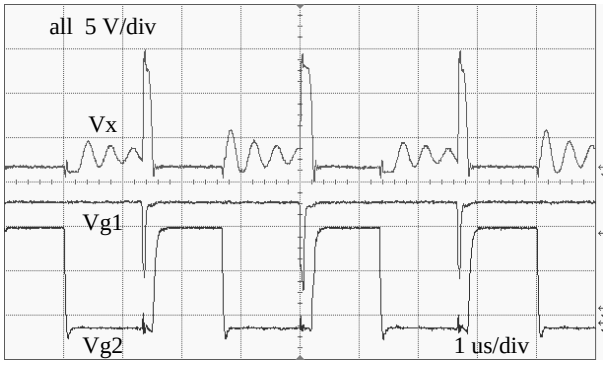
Fig. 4.12 gives the response of the converter subject to a $\Delta I_o = 85$ A load step. In CCM [plot (a)] the load step response is largely linear. Note that the voltage regulation is stiff and without load-current feedforward. Load-line regulation and load-current feedforward can be added as discussed in Chapter 2. If the converter is forced into CCM at lighter loads [plot b], by gating the SR to allow negative inductor current, the step response is identical to that in (a). If, however, the converter is allowed to enter DCM at light loads [plot (c)], the step response is dramatically different. The deterioration of the step response in DCM was anticipated in Section 4.3.1: In DCM the nominal duty ratio varies strongly with the load current, and thus the feedback integrator has to adjust over a wide range. For example, in CCM the nominal duty ratio is 1.3 V / 12 V = 0.108, while in DCM it is only 0.027 at $I_o = 1$ A, according to equation (4.5). The unloading transient in Fig. 4.12(c) is further aggravated by duty-ratio saturation to zero, due to the low conversion ratio and the resulting integrator windup. This problematic transient behavior can be addressed by scheduling the integrator state as a function of the load current, as proposed in Section



(a) CCM operation (I_o = 35 A).

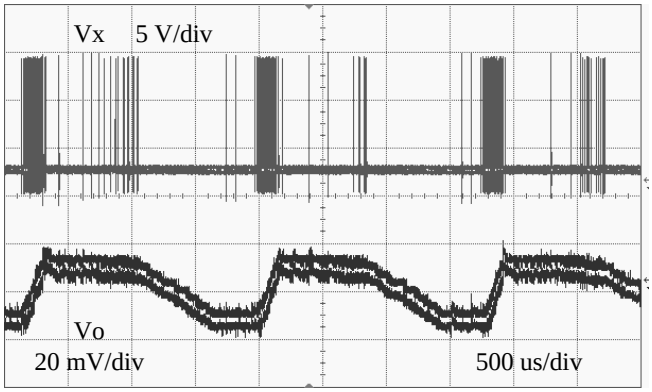


(b) Soft-switching (zero-voltage-switching) behavior (I_o = 10 A).

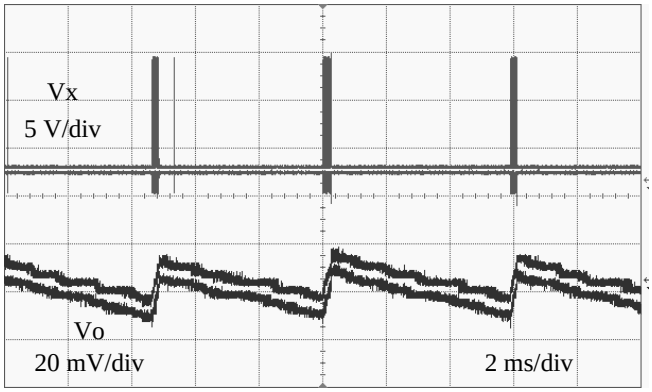


(c) DCM operation with gated synchronous rectifier (I_o = 5 A).

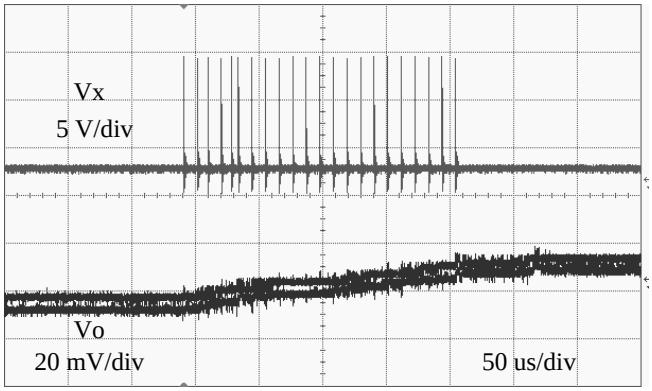
Figure 4.11: Sample switching waveforms in discontinuous and continuous conduction mode. Parameter V_{g1} is high-side (implemented with PMOS) gate voltage, V_{g2} is low-side (NMOS) gate voltage, and V_x is switching node voltage.



(d) Pulse skipping ($I_o = 0.1$ A). Periodic behavior at about 560 Hz.



(e) Pulse skipping ($I_o = 0.01$ A); bursts repeat at about 170 Hz.



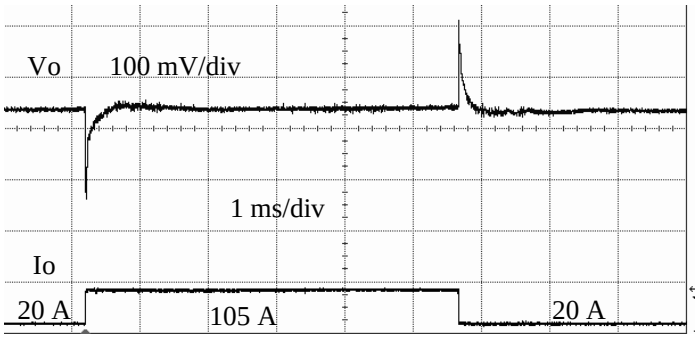
(f) Zoom of single burst in (e); pulse frequency about 94 kHz.

Figure 4.11 (Continued) [Oscilloscope in peak-detect mode to capture narrow pulses.]

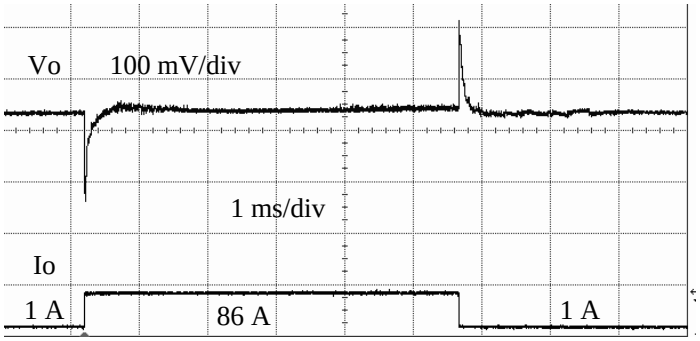
4.3.1. This approach was not implemented in the current setup, and should be tested in the future.

Fig. 4.13 shows the efficiency of the converter with various numbers of phases, and operating in various modes. The overall efficiency is not very high, due to the particular power train used. Informative, however, is the difference in efficiency among the modes. In Fig. 4.13(a), the curves corresponding to 4-phase operation in DCM and in soft-switching mode are the results of the optimization experiment above (using direct power-loss minimization; the results with temperature minimization are virtually identical). For comparison, the efficiencies associated with forced CCM ($t_{d,on} = 2$ LSB) and with the SR off ($t_{d,on} = 120$ LSB) for 4-phase operation are plotted as well. These fixed-$t_{d,on}$ curves correspond to the two modes used in controllers which nominally operate in CCM with SR, and turn off the SR completely at light load (e.g., [17]). By converging into DCM at light-to-medium load (4 A $< I_o <$ 19 A), the SR optimizer improves the efficiency by up to 5% over the better of the two fixed-$t_{d,on}$ alternatives. Below about $3.5A$ for this configuration it is better to turn off the SR altogether. In this case, discontinuous-conduction pulse skipping increases efficiency to 30%, up from 12% for nominal CCM operation at 1 A.

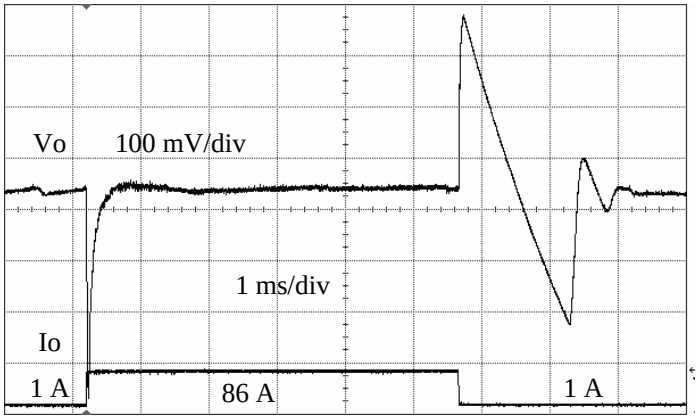
Finally, the efficiency curves for 2-phase and 1-phase operation in Fig. 4.13(b)–(c) were measured off-line. Evidently, reducing the number of phases at medium and light loads substantially decreases the power loss. Below 38 A it is advantageous to run only two phases, and below 17 A single-phase operation is optimal. These transitions among different number of phases can be straightforwardly scheduled as a function of the load current in a digital controller. This approach will work well with the adaptive SR control developed



(a) I_o = 20 A (CCM); I_o = 105 A (CCM)



(b) I_o = 1 A (forced CCM); I_o = 86 A (CCM)



(c) I_o = 1 A (DCM); I_o = 86 A (CCM)

Figure 4.12: Load step responses (ΔI_o = 85 A).

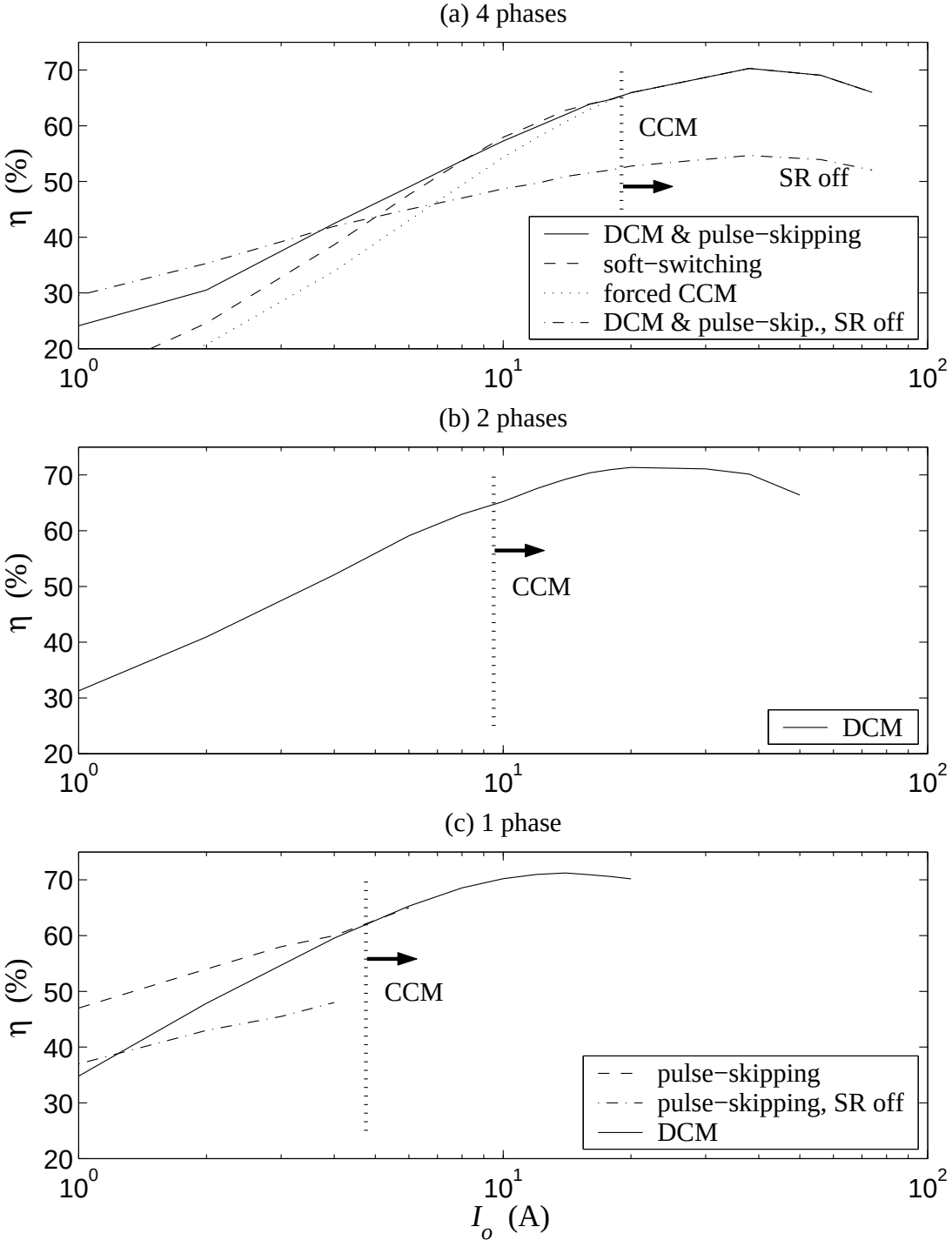


Figure 4.13: Converter efficiency η versus load current I_o for various number of phases and modes of operation. At heavy load all converters operate in CCM, as indicated. Modes of operation at light load are identified in legends.

above, since the SR timing is scheduled by the load current as well. Further, to demonstrate the light-load efficiency improvement with pulse-skipping, an aggressive minimum duty-ratio command of $D_{c,min} = 7$ LSB was imposed with a single phase enabled. The converter automatically entered pulse-skipping mode for loads below 4 A (the DCM–CCM boundary is slightly above that at 4.75 A). Single-phase pulse-skipping mode improved efficiency at 1 A by about 12% compared to single-phase fixed-frequency DCM operation, at the expense of increasing output voltage ripple to about 20 mV from 3 mV. Further, at loads of 0.1 and 0.01 A the single-phase pulse-skipping mode had an output-voltage ripple amplitude of about 20 mV, as well, equivalent to two ADC LSB's. Importantly, if the SR is disabled in single-phase pulse-skipping the efficiency drops by about 10% due to the relatively large on-time resulting in long SR conduction. Therefore, in this case it is beneficial to gate the SR in pulse-skipping.

4.5 Conclusion

This chapter developed a multi-mode control paradigm which operates the buck converter in continuous and discontinuous conduction mode, at heavy and light load, respectively, and in variable pulse-skipping mode at very light loads. The transition between continuous and discontinuous conduction is managed by scheduling the synchronous rectifier timing as a function of the load current, and optimizing it on-line so as to minimize power loss. The transition to pulse skipping is effected with a simple limit on the minimum duty-ratio command. In an experimental 100 W 4-phase buck converter the adaptive algorithm successfully optimized the synchronous rectifier timing over the full load range,

using alternately direct-power-loss and temperature minimization. Operation in discontinuous conduction mode at medium-to-light load resulted in up to 5% efficiency improvement. Further, pulse skipping improved the efficiency by 18% at very light load.

Perturbations at 100 and 200 Hz were used for the direct power loss minimization, resulting in very fast convergence of the algorithm. Slower perturbations of 0.2 and 0.4 Hz were applied in the temperature minimization experiment, due to the slow response of the thermal sensors used in the setup. In practical implementations, temperature sensors could be integrated on the MOSFET switch dies, yielding fast thermal response, in which case high-frequency perturbations could be used. Integrating temperature sensors in power MOSFET's would enable other functionality, such as fault control, and phase-current balancing based on adaptive thermal equalization among the phase legs, which could enhance the converter reliability [62, 63]. Integrated temperature sensing can be accomplished with a single diode, which has a temperature coefficient of -2 mV/°C [33, Ch. 1], as is done in some modern high-performance microprocessors (e.g., [79].

In Section 4.4 it was pointed out that the power loss signal was divided by I_o before being used in the gradient estimator. This approach successfully reduced both gradient-estimator disturbances resulting from load changes, and adaptive-loop gain variation. The algorithm could be further improved by normalizing the power loss (or temperature) by I_o^2 in CCM, and by $I_o^{3/2}$ in DCM, since these terms factor in the corresponding power loss equation (4.2) and (4.7), respectively. In should be noted that the adaptive nature of the power optimization algorithm obviates the need for accurate measurement or estimation of the load current. As long as the scheduling quantity is a monotone increasing function

of the load current, the algorithm can work. In fact, other quantities related to the load current, such as the inductor current or even the input current could be used for scheduling. Since the input current depends on the power loss, which is being optimized, using it as a scheduling variable could somewhat complicate the dynamics of the problem. However, it seems that with appropriate controller time scale separation this issue would be manageable. In general, it would be interesting to study more rigorously the convergence properties of the SR adaptation algorithm with respect to load current dynamics and small, local, power-loss minima. A good starting point for theoretical stability studies of extremum-seeking methods is the work in [42, 41, 97, 5, 11].

It was seen in Fig. 4.11(d)–(f) that at very light loads the converter exhibits pulse-skipping behavior characterized by bursts of switching, followed by periods of no switching. In existing applications, dedicated circuitry is required to implement "burst-mode" control, and switch between it and fixed-frequency operation (e.g., [27]). In contrast, the digital controller presented here automatically enters burst-mode operation at light loads by imposing a minimum duty ratio limit, without modifications of the controller structure. This behavior is closely related to the limit cycling described in Section 3.5. By enforcing a minimum duty-ratio we effectively decrease the DPWM resolution at light loads, violating no-limit-cycle condition (3.3), and thus effecting a limit cycle. The amplitude of the pulse-skipping limit cycle depends on the resolution of the output-voltage ADC, and is typically about two ADC LSB's. The limit-cycle characteristics can further be controlled by adjusting the PID parameters at light load.

Finally, in the text it was suggested that scheduling other parameters, besides

the synchronous-rectifier timing, as a function of the load current can result in additional performance improvements. For example, using an array of feedback integrators spanning the load range can enhance the transient response, as discussed in Section 4.3.1. Further, Fig. 4.13 demonstrated that adjusting the number of phases on-line as a function of the load current could effect substantial efficiency increase. For instance, disabling three of the four phases and applying aggressive pulse-skipping at light load can increase efficiency by some 17%. These techniques were not implemented in the experimental multi-mode controller, and present an exciting opportunity for future study.

Chapter 5

Contributions of Thesis and Suggestions for Future Research

5.1 Contributions of Thesis

A summary of the contributions of this thesis contrasted to previous work is given below:

Generalized Output-Impedance Control of Voltage Regulators Chapter 2 developed a consistent framework, covering both feedback and feedforward approaches, for load-line regulation which does not require the closed-loop output impedance to equal the output capacitor ESR. This framework covers capacitors technologies with a wide range of ESR times constants, such as electrolytic and ceramic capacitors. Previous work (e.g., [83, 117, 116]) had concentrated on the case when the output capacitor ESR is equal to the closed-loop output impedance.

Load-Line Control with Load-Current Feedforward In Section 2.4 it was demonstrated that load-current feedforward can extend the useful converter bandwidth without increasing the switching frequency, since feedforward is not subject to feedback stability constraints. This approach can effect a reduction of the number of output capacitors in microprocessor VR's, for example. In contrast, the bandwidth of feedback load-line control is limited to below the switching frequency [117, 116]. Previous work on microprocessor VR control had mostly focused on feedback approaches (e.g., [83, 117, 116]), or suggested that load-current feedforward does not outperform fast feedback methods [82]. Further, previous work on load-current feedforward [84, 82] was in the context of current-mode control with stiff voltage regulation. The feedforward control law, which is unity in this case, was derived from large-signal analysis. In contrast, Section 2.4 developed dynamic, small-signal load-current feedforward laws for load-line regulation with both current-mode and voltage-mode control.

Extended Critical Capacitance Analysis In Section 2.5 a large-signal critical capacitance constraint was derived, extending the analysis in [83, 82]. The critical capacitance expression allows the load-line impedance value to differ from that of the output capacitor ESR, and accounts for controller delay and load-current slew rate. The critical capacitance result allows for inductor value selection both below and above the critical inductance value discussed in [78, 104, 117]. The critical capacitance framework appears more appropriate since the inductance value is typically chosen considering inductor current ripple, and the size of the output capacitor is determined subsequently based on output voltage ripple and transient constraints.

Efficient ADC and DPWM Architectures In Chapter 3 novel approaches to high-resolution, power-efficient, small-area ADC and DPWM blocks were proposed. A "window" ADC architecture quantizes the output voltage only in a small window around the reference voltage (Section 3.2), resulting in better implementation area and efficiency compared to ADC's which quantize a wide voltage range. Further, digital dither was introduced to boost the resolution of DPWM modules, without power or area penalties (Section 3.6). In contrast to sigma-delta dither approaches [49, 67, 50], the proposed programmed-dither method uses pre-computed dither sequences which minimize the output-voltage ripple.

Conditions for Limit-Cycle Elimination It had previously been observed that closed-loop operation of a digitally-controlled power converter could result in limit cycling behavior due to the quantization in the feedback path [108]. To address this problem, conditions on the quantizer resolution and the feedback control law for limit-cycle elimination were developed in Section 3.5.

Load-Scheduled Loss-Minimizing Synchronous-Rectifier Control A method for direct control of synchronous rectifiers as a function of the load current is developed in Chapter 4. The function relating the synchronous rectifier timing to the load current is obtained on-line via loss-minimizing multi-parameter adaptation. Only low-bandwidth measurements of the load current and a power-loss-related quantity (such as input current or temperature) are required, in contrast to common synchronous rectifier control techniques [40, 92, 3, 43, 52]. Further, compared to alternative loss-minimizing approaches [2, 118], this method has superior adjustment speed and ro-

bustness to transients, and can simultaneously optimize multiple parameters. Finally, as discussed in Section 4.3.1, a similar adaptive scheduling approach can be used to rapidly adjust the duty ratio in DCM, providing fast load-transient response in multi-mode operation.

Automatic Multi-Mode Buck Operation The loss-minimizing synchronous-rectifier control accomplishes an automatic, optimal transition to DCM at light loads. Further, by imposing a minimum duty-ratio the converter will automatically enter pulse-skipping mode at very light loads, as shown in Chapter 4. Thus, the same controller structure could be used in both fixed-frequency PWM and variable-frequency pulse-skipping modes. This is in contrast to typical multi-mode designs in which a separate control law is used for light-load variable frequency operation (e.g., [27, 80, 111]). This multi-mode control strategy allows for efficient operation of the buck converter over a wide load range.

5.2 Suggestions for Future Research

Some ideas of how the work in this thesis can be extended were already discussed in the text. Here we attempt to summarize the more important suggestions, and outline directions for future work:

5.2.1 Load Current Estimators

The load-line control methods described in Chapter 2 rely on accurate estimation of the load current. Passive estimation methods such as the ones described in Section 2.7.3 rely

on matching of the estimator parameters to those of the power train, and are thus sensitive to component tolerances, temperature, and drift. More robust, adaptive estimators could be developed. For example, input-current measurements of microprocessor VR's are relatively easy to implement due to the low nominal duty ratio. The input-current measurement could be used to tune a passive load current estimator such as the one in Section 2.7.3, or an estimator based on trace or package resistance (e.g., [79]). Estimation techniques for power electronic circuits are discussed in [37], for example.

5.2.2 Adaptive Load-Current Feedforward

The load-line regulation method using load-current feedforward discussed in Section 2.4 can provide very fast converter response, however it is sensitive to mismatches between the power train parameters and the nominal values used in the feedforward control law. For example, in a voltage-mode controller implementation, which is typical for microprocessor VR's, the feedforward control law (2.22) uses the nominal values of the total inductance and output capacitance, which could differ from the actual values. This problem can be addressed by adaptively tuning the feedforward law. For example, if the feedforward is perfect, the feedback error signal will always be zero. Hence, feedforward tuning could be based on minimizing the error signal over time. Relevant discussion of adaptive control can be found in [8, 90], for example.

5.2.3 Multi-Mode Control

Over its full load range the switching power converter could span a number of modes as described in Section 4.2. Due to the different converter behavior, it is generally

appropriate to adjust some of the controller parameters in the different modes. A general framework promoted in this thesis is to schedule these parameters as a function of the load current, and to estimate an optimal value of this function either off-line or on-line. This approach was demonstrated with loss-minimizing synchronous rectifier control in Chapter 4. In the same chapter it was shown that a similar approach could provide fast integrator adjustment in all modes. It was also demonstrated that adjusting the number of active phases as a function of the load could provide high efficiency over a wide load range. The integrator scheduling and the phase scaling were not implemented experimentally in this work, and merit future study.

Further, the load-current feedforward control laws in Section 2.4 were derived for CCM. In CCM the control-to-output transfer function of the buck converter is second-order and is independent of the load current. In DCM, however, the control-to-output transfer function is first-order and is dependent on the load [28, Ch. 11]. Thus, it would be appropriate to adjust the feedforward law as a function of the load current in DCM.

Similarly, due to the changing control-to-output transfer function between DCM and CCM, the PID control law coefficients in (3.1) may have to be adjusted to ensure good closed-loop performance. Further, in the pulse-skipping mode the limit-cycle determining the pulse sequences depends on the PID coefficients. Thus, it could be appropriate to adjust the PID law as a function of the load current, as well. This approach is referred to as gain-scheduling, and is discussed in [8, Ch. 9], for example.

5.2.4 PID Self-Tuning

A related issue is that the PID control law is typically designed based on the nominal power train parameters. Due to component tolerance, ambient conditions, and aging these parameters may change, possibly resulting in degraded closed-loop performance. A digital controller can perform on-line PID tuning to overcome this problem. In the extreme case, the controller may start with little or no a priori knowledge of the power train parameters, and the controller could carry out experiments to identify these parameters and assign appropriate PID coefficients. This could eliminate the need for PID customization and the associated human expertise.

System identification and PID tuning can be carried out during an off-line calibration routine, during the converter power-up sequence, or during normal operation. For example, when the host system is turned on, the power converter typically undergoes a soft-start sequence in which the output voltage is gradually ramped up to the reference voltage. During the start-up transient the host system is not operational yet, and the digital power controller can carry out both open-loop and closed-loop experiments to characterize the power train parameters. PID coefficients can be computed based on this parameter estimates and a given PID design method. Under normal, regulated operation, closed-loop experiments can be carried out to further fine-tune the PID control law. The system can be driven into a self-oscillation with an acceptable amplitude, or a perturbation can be injected in the control signal. The latter has been used to estimate on-line the transfer characteristic of a power converter [55, 56]. Alternatively, natural disturbances such as load current transients can be used to estimate the converter parameters. Discussion of PID

controller self-tuning can be found in [7, 8], for example. An expansive reference review of modern PID controller design is given in [45].

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Appendix A

PSIM Simulation Schematic

PSIM 6.0 (Powersim Inc.) schematic and parameter list for the 4-phase VR simulation in Chapter 2:

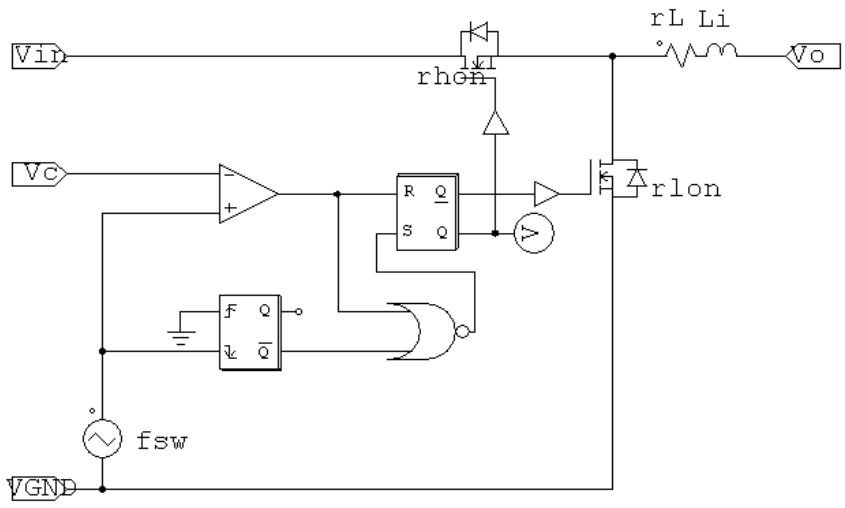

Figure A.1: Simulation schematic of phase module subcircuit in Fig. A.2.

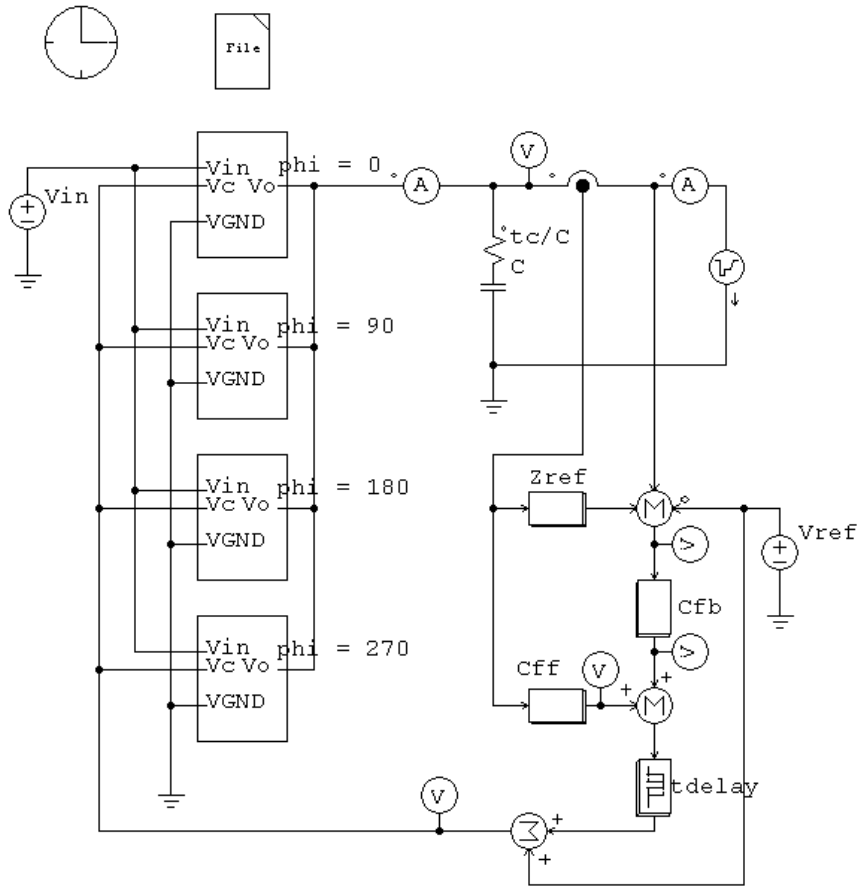

Figure A.2: Simulation schematic of 4-phase VR with load-current feedforward.

```
Vin=12
Vref=1.3
N=4
C=800u+10u+0.1u
tc=0.2u
Li=390n
rL=0.6m+0.1m
rhon=21.1m
rlon=2.6m
VD=0.6

%controller
pi=3.14
D=Vref/Vin
fsw=1MHz
Rref=1.3m
tdelay=100n

% Cfb
b0=1
b1=1.68e-5
b2=6.26e-11
b3=0
a0=0
a1=1.43e-5
a2=5.82e-12
a3=4.78e-19
K=20

% Cff
Lff = Li/N
tcff=0.2u

% load
Io0=60
dIo=8 %52
Vo0=Vref-Rref*Io0
```

Appendix B

MATLAB Simulation Source Code

MATLAB 6.5 (The MathWorks, Inc.) source code for the averaged model and switched simulation of the prototype digitally-controlled buck converter in Chapter 3:

```
%
% avg_model.m
%
% Averaged model of digitally-controlled 250 kHz 4-phase buck
% converter for MATLAB 6.5
%
% Angel Peterchev
% U.C. Berkeley
% Power Electronics Group
% (c) 1999-2005
%

% power train
Vin = 10;                       % input voltage
Vref = 2.5;                     % reference voltage
N = 4;                          % number of phases
D = Vref/Vin;                   % default duty ratio
rs  = 16e-3;                    % Vin to switch bus resistance
L = 5.5e-6/N;                   % total inductance
rL = 12e-3/N;                   % inductor + trace resistance
rh = 65e-3/N;                   % high side MOSFET Rds,on
rl = 12e-3/N;                   % low side MOSFET Rds,on
rL1 = D*(rh + rs)+(1-D)*rl+rL;  % avrg. res. in series with indictor
```

```
Cb = 6*680e-6;                  % output bulk cap
tCb = 8.8e-6;                   % output bulk cap time const
rCb = tCb/Cb;                   % output bulk cap ESR
Cf = 6*10e-6;                   % output HF filter cap
tCf = 0.2e-6;                   % output HF filter cap time const
rCf = tCf/Cf;                   % output HF filter cap ESR

% controller
Nadc = 10;                      % effective ADC resolution
Ndpwm = 7;                      % hardware DPWM resolution
Ndith = 4;                      % dither resolution
Ndpwm_eff = Ndpwm + Ndith;      % effective DPWM resolution
Kp = 2^5;                       % proportional gain
Kd = 2^7;                       % derivative gain
Ki = 2^(-1);                    % integral gain
fsw = 250e3;                    % switching frequency
T = 1/fsw;                      % switching period
fsamp = fsw;                    % sampling frequency
Tsamp = 1/fsamp;                % sampling period
Tcalc = 5e-6;                   % sampling + calculation delay
te = 1/(2*pi*135e3);            % error amp BW (before ADC)

% converter averaged continuous-time model
syms s
s = tf('s');

% power train
% duty-ratio command-to-output TF
%   with bulk and HF output cap
G = Vin*(s*tCb + 1)*(s*tCf + 1) / ...
    (s^3*L*Cb*Cf*(rCb+rCf) + ...
     s^2*(L*(Cb+Cf)+rL1*Cb*Cf*(rCb+rCf)+tCb*tCf) + ...
     s*(rL1*(Cb+Cf)+tCb+tCf) + 1);
%   with only bulk output cap
% G = (s*tCb + 1) / (s^2*L*Cb + s*(rL1+rCb)*Cb + 1);

% open-loop output impedance
%   with bulk and HF output cap
Zoo = (s*L + rL1)*(s*tCb + 1)*(s*tCf + 1) / ...
    (s^3*L*Cb*Cf*(rCb+rCf) + ...
    s^2*(L*(Cb+Cf)+rL1*Cb*Cf*(rCb+rCf)+tCb*tCf) + ...
     s*(rL1*(Cb+Cf)+tCb+tCf) + 1);
%   with only bulk output cap
% G = (s*L + rL1)*(s*tCb + 1)/(s^2*L*Cb + s*(rL1+rCb)*Cb + 1);
```

```
% PID controller
Cfbd = 2^(Nadc-Ndpwm_eff)/Vin * ...
    (tf(Kd.*[1 -1],[1 0],Tsamp)+tf(Kp,1,Tsamp)+tf(Ki.*[1 0],[1 -1],Tsamp));
Cfb = d2c(Cfbd,'tustin');                % cont.-time error-to-command TF
Td = Tsamp + Tcalc + D*T + 3/8*T;        % worst-case large signal delay
td = Tcalc + D*T + 3/8*T;                % small signal delay
                                         % (3/8*T models 4-phase delay)
Wfb = pade(tf(1,'OutputDelay',td),4);    % pade approx of delay
Fe = 1 / (s*te + 1);                     % error amplifier TF

LG = Fe*Cfb*Wfb*G;                       % loop gain
Zo = Zoo*feedback(1,LG);                 % output impedance

% end avg_model.m
```

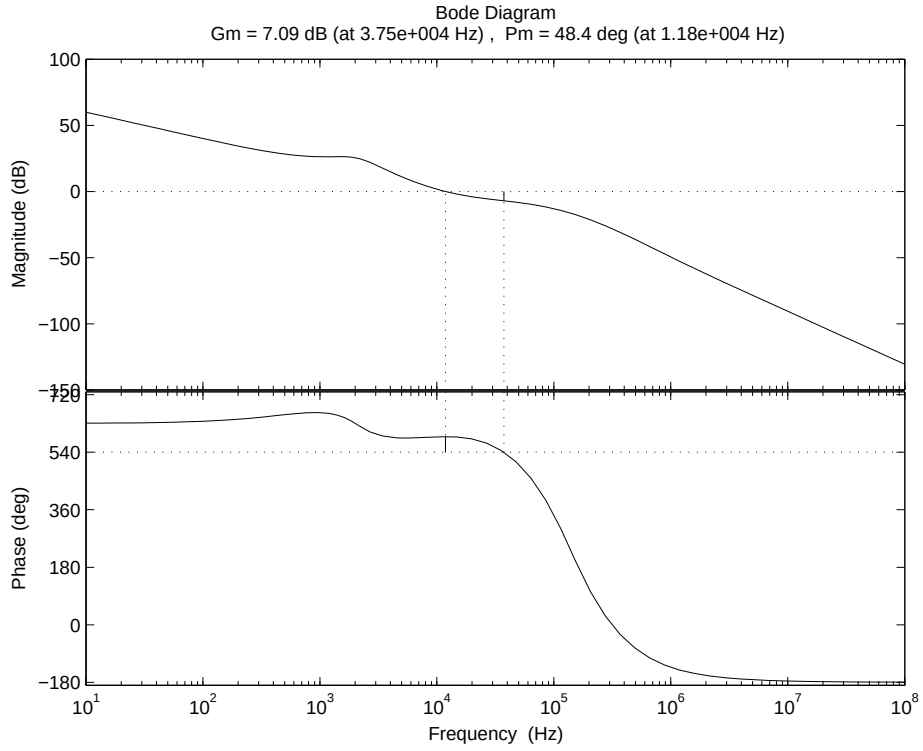

Figure B.1: Converter loop gain calculated with the averaged continuous time model.

```
%
% switched_sim.m
%
% Switched simulation of digitally-controlled 250 kHz 4-phase buck
% converter for MATLAB 6.5
%
% Angel Peterchev
% U.C. Berkeley
% Power Electronics Group
% (c) 1999-2005
%

%   Power Train
%
Vin = 10;                       % input voltage
rs  = 16e-3;                    % Vin to switch bus impedance.
L1  = 5.5e-6;                   % phase inductors
L2 = L1; L3 = L1; L4 = L1;
rh1 = 65e-3;                    % high side IRF5305 MOSFET resist.
rh2 = rh1;  rh3 = rh1;  rh4 = rh1;
rl1 = 12e-3;                    % low side IRL3103S MOSFET resist.
rl2 = rl1;  rl3 = rl1;  rl4 = rl1;
rL1 = 5e-3 + 4e-3 + 3e-3;       % sens. + induc. + trace resist.
rL2 = rL1; rL3 = rL1; rL4 = rL1;
Cb  = 6*680e-6;                 % bulk output capacitor
tCb = .013*680e-6;              % bulk output cap ESR time const
rCb = tCb/Cb;                   % bulk output capacitor ESR
Cf  = 6*10e-6;                  % HF filter output capacitor
tCf = 0.2e-6;                   % HF filter output cap ESR time const
rCf = tCf/Cf;                   % HF filter output capacitor ESR
RL  = 5;                        % output load resistor
RL_dyn1 = 3*0.33/5 + 19e-3;     % dynamic load bank 1
RL_dyn2 = (2*0.2+0.5)/3 + 19e-3;% dynamic load bank 2
RL_dyn  = RL_dyn1;              % dynamic load (res. + MOSFET RDS(on))

%   Digital Parameters
%
Nadc = 7;           % number of bits of ADC
N_adc_eff = 10;     % effective ADC res.
Ndpwm = 7;          % number of bits of DAC (DPWM)
Ndith = 4;          % output subbit level resolution (bits)
dith = 2^Ndith;     % number of subbit levels
MAXdpwm = 2^Ndpwm;  % number of DPWM quant. bins
phase1 = 0;             % switch phase offsets
```

```
phase2 = 2^Ndpwm / 4;   %
phase3 = 2^Ndpwm / 2;   %
phase4 = 2^Ndpwm * 3/4; %
dith_en = 1;        % enable dither
integ_en = 1;       % enable integrator

%   Controller clocking
%
fsw = 250e3;        % switching frequency
T = 1/fsw;          %    "      period
fcon = (2^Ndpwm)*fsw;% controller clock frequency
Tcon = 1/fcon;      %    "      period

%    Control Law
%
Vref = 2.5;         % reference voltage
Vin_ADC = 4.985;    % ADC voltage window
Kp = 2^5;           % prop. gain
Kd = 2^7;           % deriv. gain
Ki = 2^(-1);        % integ. gain
Ke = 4;             % error amplifier gain, effective Nadc = 9
td = 5e-6;          % controller delay
fe = 135e3;         % error amp. BW (AD623)

% error amp. BW
te      = 1/(2*pi*fe);              % LP time const.
a_e     = 1/(1+Tcon/te);            % DT sim. filter coeff.'s
b_e     = Tcon/te/(1+Tcon/te);      % DT sim. filter coeff.'s

%   State transition and input matrix (A|B Nstsp x Nstsp)
%   State and input vector = [Vc1 Vc2 I1 I2 I3 I4 Vin Io]'
%
%        [e(A|B)t] u1 u2 u3 u4
Nstsp = 8;                                          % number of states
eAt = zeros( Nstsp, Nstsp, 2, 2, 2, 2);         % storage for e^(A|B)t

% output equation matrix C|D, output vector = Vo
C = [rCf*RL rCb*RL rCb*rCf*RL rCb*rCf*RL rCb*rCf*RL rCb*rCf*RL ...
        0 -rCb*rCf*RL]./(rCb*RL+rCf*RL+rCb*rCf);
invL = inv(diag([1 1 L1 L2 L3 L4 1 1]));        % inductance matrix

for u1 = 0:1, for u2 = 0:1, for u3 = 0:1, for u4 = 0:1,
 C1 = [ 0 0 -u1*rs -u2*rs -u3*rs -u4*rs 1 0];
 A1 = diag([-1/tCb -1/tCf -(rL1+u1*rh1+~u1*rl1) -(rL2+u2*rh2+~u2*rl2)...
```

```
        -(rL3+u3*rh3+~u3*rl3) -(rL4+u4*rh4+~u4*rl4) 0 0]);
 A = invL*(A1 + [0 0 u1 u2 u3 u4 0 0]'*C1 + ...
     [1/tCb 1/tCf -1 -1 -1 -1 0 0]'*C);

 % exponent of state transition and input matrix e^((A|B)t)
 eAt( :, :, u1+1, u2+1, u3+1, u4+1) = expm(A*Tcon);
end; end; end; end;

%   4-bit dither table
%
dith_tab = zeros(dith,dith);

% half of dither table
dith_tab1 = [   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0;
                0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1;
                0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1;
                0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1;
                0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1;
                0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1;
                0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1;
                0 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1;
                0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1;];

% generate complete dither table
dith_tab(1:dith/2+1,:) = dith_tab1;
dith_tab(dith/2+2:dith,:) = ~dith_tab1(dith/2:-1:2,:);
if sum(dith_tab,2) ~= [0:dith-1]'
    display('Incorrect dither sequence sums! ');
    stop;
end;

%   Simulation Parameters
%
Vref_vector = [ Vref Vref Vref];            % Vset step
Io_vector = [ 0 Vref/RL_dyn 0];             % Io step
Io_SR_vector = [ 0 200 -200].*1e6;          % Io slew rate
Nstep = [ 1 625 2000 0];                    % time of step
numcycle = 1500;                            % # of sim. sw. cyc.
U = zeros(4, numcycle * 2^Ndpwm);           % switch states
Treal = [0 : T : (numcycle-1)*T] - Nstep(2)*T; % real time vector
                                            % (t=0 @ load step start)
Treal_hr = [0 : numcycle*2^Ndpwm-1].*T/2^Ndpwm - Nstep(2)*T; % hi-res
qdelay = floor((td-T)/T*MAXdpwm);           % Vo sampling time - T
                                            %  (since td=5us > T=4us)
```

```
load_time = floor(76/100*MAXdpwm);          % load timing

%   State storage variables
%
Y_mem    = zeros(numcycle, Nstsp);              % state vector
Y_hr_mem = zeros((numcycle-1)*2^Ndpwm, Nstsp);  % high-res. "
Di_mem   = zeros(numcycle, 1);                  % integrated error
De_mem   = zeros(numcycle, 1);                  % error
Dc_mem   = zeros(numcycle, 1);                  % duty cycle
Vo_mem   = zeros(numcycle, 1);                  % Vo
Vo_hr_mem = zeros((numcycle-1)*2^Ndpwm, 1);     % high-res. "

%   Initial Conditions
%
qcon    = 1;            % controller clock
step_state = 1;         % step command timing
Dek     = 0;            % error signal De(k)
Dek_1   = 0;            %   "    "     De(k-1)
Di      = -28;          % integrator value
Io      = (Io_vector(1) + Vref/RL); % initial output current
Io_cmd  = Io;           % load current command
dIo = 0;                % load current step
Ve_k    = 0;            % sampled error signal
Ve_k_1  = 0;            % old sampled error signal
Ve_filt = 0;            % error amplifier signal
Vo      = Vref;         % initial Vo
I1init  = Io/4;         % initial inductor currents
I2init  = I1init;       %
I3init  = I1init;       %
I4init  = I1init;       %
Y       = [Vo Vo I1init I2init I3init I4init Vin Io]'; % initial
                        %  state vector
Df      = floor(Vref/(Vin/2^Ndpwm) + 0.5);
De_offset   = 64;       % ADC word offset
step_state  = 1;        % step command timing

%-------------------------------------------------------------------------
%   Simulation Loop
%-------------------------------------------------------------------------

for q = 1 : numcycle,

    %  Control Law
    %
```

```
% control calculations
De = uadc( Vin_ADC, 0, Nadc, Ke*Ve_k_1+Vin_ADC/2) - De_offset;  %
                                                  %  window ADC
Di = integ_en*(Di + De);                          % integrator
Dc = floor( Kp*De + Kd*(De-Dek_1) + Ki*Di );% duty cycle cmd
Dc = usat((Ndpwm+Ndith),(Dc + Df*dith));    % saturation
Ve_k_1 = Ve_k;                                    % implements part of
                                                  %  contr. delay (1 T)
Dek_1 = De;                                       % store last error

% dither and duty ratio saturation
Dc = usat(Ndpwm,(floor(Dc/dith) + ...
    dith_tab(mod(Dc,dith)+1,dith_en*mod(q,dith)+1)));

% store variables for analysis
De_mem(q) = De;
Di_mem(q) = Di;
Dc_mem(q) = Dc;
Y_mem(q,:) = Y';

% assign switch states
U( 1, qcon : qcon+Dc) = 1;
U( 2, qcon+phase2 : qcon+phase2+Dc) = 1;
U( 3, qcon+phase3 : qcon+phase3+Dc) = 1;
U( 4, qcon+phase4 : qcon+phase4+Dc) = 1;

%   DPWM Loop
%
for m = 1 : MAXdpwm,    % loop 2^Ndpwm times

    Vo_hr_mem(qcon) = Vo;               % store Vo
    Y_hr_mem(qcon,:) = Y';              % store convert. state
    Vo = C*Y;                           % compute Vo
    Ve = Vref - Vo;                     % error signal
    Ve_filt = a_e * Ve_filt + b_e * Ve; % error amp. filter

    % PWM sampling
    if m == MAXdpwm-qdelay,         % sampling instant
        Ve_k = Ve_filt;             % sample Ve
        Vo_mem(q) = Vo;             % store sampled Vo
        Vo_mem(q) = Vo;             % store sampled filtered Vo
    end;
    % Vref / Io step
    if (m == MAXdpwm-load_time) & (q == Nstep(step_state)),
```

```
            Vref = Vref_vector(step_state);
            Io_cmd = Io_vector(step_state); % change Io
            dIo = Io_SR_vector(step_state)*T/MAXdpwm;
            step_state = step_state + 1;
        end;
        % calculate new state
        Y = eAt(:,:,U(1,qcon)+1,U(2,qcon)+1,U(3,qcon)+1,U(4,qcon)+1)*Y;
        % Io slew
        Y(8) = Y(8) + dIo*(((dIo > 0) & (Y(8) < Io_cmd)) | ...
                                    ((dIo < 0) & (Y(8) > Io_cmd)));
        if (((dIo > 0) & (Y(8) > Io_cmd)) | ...
                    ((dIo < 0) & (Y(8) < Io_cmd))) Y(8) = Io_cmd; end;

        qcon = qcon + 1;    % increment controller clock

    end;

end % switching loop

% end switched_sim.m
```

```
%-----------------------------------------------------------------------
%
% uadc.m
%
% Unsigned ADC function
%
function Dout = f(Vhigh, Vlow, N, Vin);

Vlsb = (Vhigh - Vlow) / (2^N);

if Vin <= 0
  Dout = 0;
elseif Vin >= Vhigh
  Dout = 2^N - 1;
else
  Dout = round(Vin / Vlsb);
end

% end uadc.m


%-----------------------------------------------------------------------
%
% usat.m
%
% Unsigned saturation function
%
function Dout = f (N, Din);

if Din >= (2^N-1),
  Dout = (2^N-1);
elseif Din <= 0,
  Dout = 0;
else,
  Dout = Din;
end

% end usat.m
```