Analysis and Design of Wideband LC VCOs

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Analysis and Design of Wideband *LC* VCOs

by

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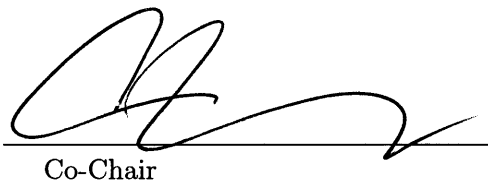

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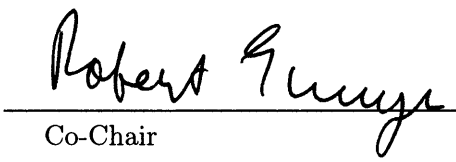

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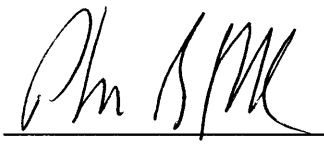

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Abstract

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Doctor of Philosophy in Electrical Engineering and Computer Sciences

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The growing demand for higher data transfer rates and lower power consumption has had a major impact on the design of RF communication systems. In both wireless and wireline applications, this has been achieved using more spectrally efficient modulations and/or wider channel bandwidth in combination with engineering techniques to lower power and fabrication costs. Furthermore, as communication standards evolve and new applications are created, systems not only have to cope with a more crowded spectrum, they must also support a larger number of legacy standards for reasons of backward compatibility. This has resulted in a trend promoting more wideband and spectrally adaptive devices.

One of the most critical components in modern communication devices is the VCO.

Being at the heart of the frequency synthesizer, the VCO performs indispensable functions in the transmission and reception of data. For systems with high dynamic range requirements, the VCO must achieve a correspondingly high degree of spectral purity so as not to degrade the SNR (or sensitivity) excessively. This can be particularly challenging for wideband systems because conventional wideband VCOs have poor phase noise performance. To this date, the only effective solution to this challenge has been to use multiple low-noise narrowband VCOs, each covering a portion of the required range. While conceptually simple, this solution is far from ideal due to its high cost and increased design complexity.

In light of the above observations, the main goal of this thesis is to identify successful measures for wideband low-noise frequency synthesis. Using an LC VCO as its main vehicle, characteristics of wideband low-noise frequency synthesis are analyzed, leading to proposed techniques. A prototype is implemented to validate our analysis and demonstrate the feasibility of wideband low-noise LC VCOs.

Professor Robert G. Meyer
Dissertation Committee Co-chair

Professor Ali M. Niknejad
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To my parents

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Chapter 1

Introduction

1.1 Recent Trends in RF Communication Systems

Over the last several decades, the rapid growth of commercial communication applications has led to a commensurate demand for better and cheaper devices. While Moore's law has continued its course mostly undisturbed for close to a half century, digital circuits have experienced continuing improvements due to a doubling of available transistors every two years [1, 2]. Such rapid technology developments revolutionized digital electronics, thereby fueling one of the fastest growing markets ever observed.

Analog circuits have also benefited from technology scaling, although at a slower pace due to the many challenges in adapting to degrading device characteristics. Because of the continuing reduction of voltage headroom and intrinsic device gain, high-precision analog building blocks have had to adopt higher degrees of design complexity

to overcome these impediments.

The evolution of integrated circuit (IC) technology has also brought faster transistors with every new generation, which has benefited both digital and analog circuits. With a minimum feature size halving every 6–7 years, as dictated by the International Technology Roadmap for Semiconductors [3], modern CMOS transistors can operate and provide substantial gain well into the millimeter-wave regime. In terms of radio-frequency (RF) communication systems, this has created an unparalleled opportunity for CMOS technology to redefine a market previously restricted to relatively expensive counterparts. Fine-line CMOS technology has also proved advantageous in terms of integration. Today's RF transceiver CMOS ICs can integrate many, if not all, of the analog and digital baseband functions.

The sustained momentum towards fully integrated single-chip radios, often referred as system-on-chip (SOC) solutions, has continuously driven down manufacturing costs. Lower costs have ultimately translated into a growing customer demand for better quality of service. To keep up with market dynamics, communication standard committees have had to establish new enabling standards for emerging applications. In a manner similar to the evolution of electronics, standards have evolved in ways that better leverage the strength of digital technology. Hence, today's communication systems rely on digital modulation techniques and make extensive use of digital signal processing. Using digital technology provides robustness, programmability, and secures cost and performance benefits for future generations of products as scaling continues. Digital

designs also prove to be much easier to maintain, repair, and upgrade.

The growing demand for higher data transfer rates and lower power consumption (while keeping cost low) has had a major impact on the design of RF communication systems. In both wireless and wireline applications, this has been achieved using more spectrally efficient modulations and/or wider channel bandwidth, in combination with engineering techniques to lower power and fabrication costs. Furthermore, as standards evolve and new applications are created, systems not only have to cope with a more crowded spectrum they must also support a larger number of legacy standards for reasons of backward compatibility. This has resulted in a trend promoting more wideband and spectrally adaptive devices [4–6]. Future applications are likely to exacerbate this trend, as evidenced by the recent emergence of more progressive initiatives such as ultra-wideband (UWB) systems, software defined radios, and 60GHz wireless personal area networks [7–9].

1.2 Modern Applications of PLL Frequency Synthesizers

Nearly all modern electronic devices need an appropriate frequency reference to operate. The particular method used to synthesize such reference frequencies is determined by the specifications of the system. In its most basic form, a frequency synthesizer consists of a standalone oscillator operating at the frequency of interest. For most appli-

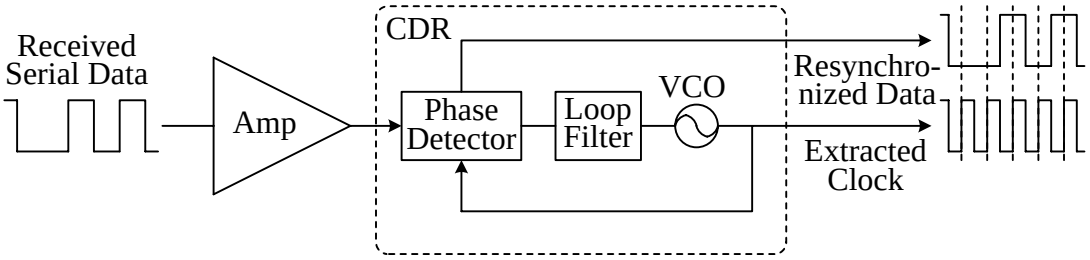


Figure 1.1: Chip-to-chip serial receiver using a CDR unit.

cations, this simple device is not adequate. While the best oscillators achieve excellent spectral accuracy, their frequency range is intrinsically limited to the necessarily high selectivity of their resonator. Furthermore, the nature of such resonators (e.g. quartz crystals) makes them expensive and very difficult to integrate on a silicon substrate. Alternatively, relaxation oscillators avoid resonators by using amplifiers in positive feedback configuration. Since their frequency is set by component delays as opposed to a resonator, it can be easily tuned and integration is no longer an issue. However, this approach generally yields relatively poor spectral purity [10].

Frequency synthesis for moderate- to high-accuracy systems is commonly achieved using a phase-locked loop (PLL). Using negative feedback, PLL synthesizers are able to precisely track the phase of an incoming signal within a certain bandwidth while simultaneously scaling its frequency by some adjustable factor. The combination of providing a very useful function at low cost with a high degree of flexibility and robustness has made the PLL frequency synthesizer a popular choice in a wide range of applications. Microprocessors use PLL synthesizers to distribute well-controlled clock

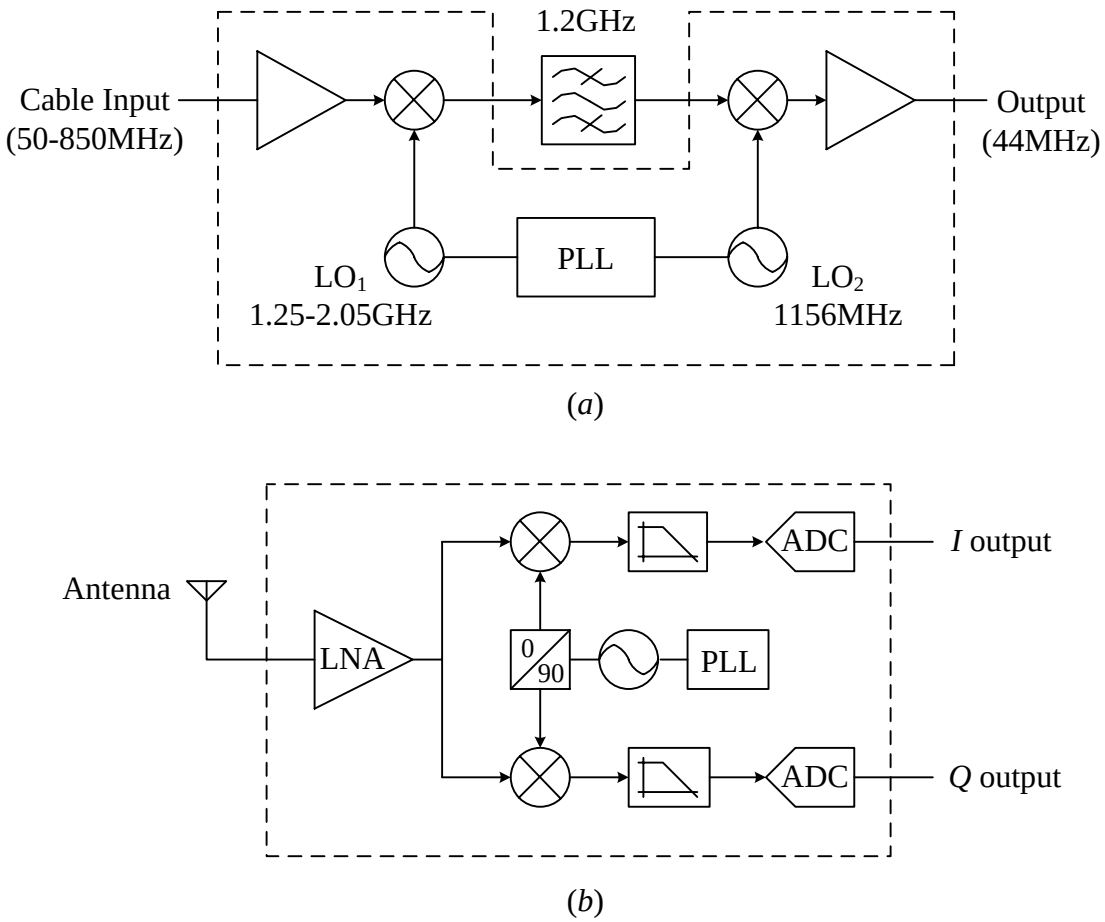


Figure 1.2: Two common applications of PLLs: (a) a cable TV tuner based on a dual-conversion architecture, (b) a wireless receiver based on a direct-conversion architecture.

signals to various parts of the chip. High precision analog-to-digital converters (ADCs) also make use of PLLs to generate the low jitter clock signals needed to achieve the required dynamic range. In chip-to-chip communication interfaces, PLLs are used as clock-data-recovery (CDR) units that extract the clock from the incoming data and resample the same data with it. Fig. 1.1 shows a typical application of a CDR.

Wireless and wired data transceivers are perhaps where PLL synthesizers are most

pervasive. Indeed, the high performance, robustness, and moderate cost of PLLs are valuable ingredients for mass-produced high data rate communication devices. Common examples are wireless radios and broadband terrestrial/cable TV tuners which use PLLs for channel selection and modulation/demodulation. Fig. 1.2 illustrates two such scenarios.

1.3 Motivation and Research Objectives

Due to their crucial role in a wide variety of modern applications, PLL frequency synthesizers have been the subject of extensive research in recent years. In particular, the tough synthesizer requirements imposed by cellular phone applications have been a key driver for PLL research. Specifically, stringent phase noise specifications provided considerable incentive for research solely focused on improving the voltage-controlled oscillator (VCO) performance, one of the most challenging aspects of PLL design. As a result, there have been considerable advances in VCO and PLL design techniques and corresponding improvements in performance.

Due to the narrowband nature of cellular applications, much of the research work mentioned above has focused on correspondingly narrowband VCO and PLL methods. Similarly, other recent research drivers such as wireless local-area networks (WLAN) and sensor networks have not differed in this regard. As a result, there has been little research on high-performance wideband VCOs and PLL synthesizers. However, current trends clearly indicate a growing customer demand for faster data rates. As stated in

Shannon's information capacity theorem, the maximum rate of error-free data transmission is directly proportional to the channel bandwidth. Hence, higher data rates are typically achieved by increasing the allocated channel bandwidth. Whereas some applications such as 60GHz radios achieve higher bandwidth by operating at higher frequencies, others like UWB widen their operating bandwidth instead. In the latter case, a wideband synthesizer is needed to cover the 3.1–10.6GHz frequency range. Furthermore, cellular applications themselves are becoming multiband due to the growing number of standards that must be supported. While each frequency band is narrow, having a dedicated VCO covering each band can become very expensive as the number of bands increases. Instead, a single wideband VCO/PLL can be use to cover several bands. Hence, wideband VCOs and PLLs are becoming important in those applications as well. Finally, future reforms to current spectrum allocations may allow the operation of smart cognizant radios. In concept, a cognizant radio would sense unused or less crowded portions of the spectrum and reconfigure itself to operate there. Thus, such ratios would have to be widely adaptive, thereby requiring a wideband frequency synthesizer as well.

In light of the above trends, the main goal of this thesis is to identify successful measures for wideband low-noise frequency synthesis. Using an LC VCO as its main vehicle, characteristics of wideband low-noise frequency synthesis are analyzed, leading to proposed techniques. A prototype is implemented to validate our analysis and demonstrate the feasibility of wideband LC VCOs.

1.4 Thesis Organization

This thesis focuses on the topic of wideband low-noise frequency synthesis, with a particular emphasis on wideband LC VCO design. Since LC VCOs are mostly found in the context of PLLs, Chapter 2 aims to provide a summary of PLL frequency synthesizer fundamentals. Spectral purity is explored in terms of phase noise and timing jitter. To support our discussion, the main building blocks are briefly described. Loop dynamics and noise characteristics are explained and some of the more common PLL architectures are discussed.

In Chapter 3, LC VCO fundamentals are introduced, covering LC tanks, start-up conditions, steady-state operation, and phase noise. Three common topologies are discussed and their performance is compared along with simulation results.

Chapter 4 explores the analysis and design of wideband LC VCOs. We discuss the impact of wide frequency variations on start-up conditions, output amplitude and phase noise. Finally, tuning range is analyzed, resulting in practical tuning range equations.

Chapter 5 describes the implementation of a wideband LC VCO prototype in a 0.18-μm CMOS technology. The design process is explained in detail and measurement results are provided.

Chapter 6 summarizes the contributions of this research and suggests future directions.

Chapter 2

PLL Frequency Synthesizer Fundamentals

2.1 Basic Operating Characteristics

Frequency synthesizers may be implemented in several ways. While some of the techniques discussed herein may be applied in other implementations, the scope of this chapter is intentionally limited to PLL frequency synthesizers. Furthermore, the ensuing discussion assumes a PLL that is used to generate a high-frequency carrier from a clean low frequency reference for the purpose of up- or down-converting a desired channel. Fig. 2.1 illustrates a basic PLL and its core constituting blocks. From Fig. 2.1, we note that a PLL operates on the principle of negative feedback. The phase detector (PD) acts as the differencing node of the feedback loop, which aligns the phase of the divided

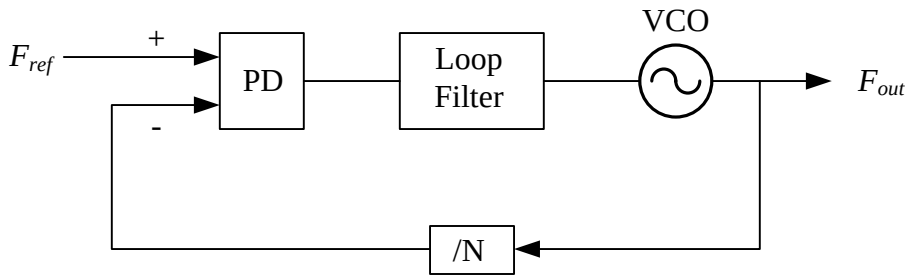


Figure 2.1: Block diagram of a basic PLL.

output with that of the input by controlling the VCO frequency through its tuning port. Under the right conditions, the PLL achieves the locked condition in steady-state and the following relationship holds

$$F_{out} = N \cdot F_{ref} \tag{2.1}$$

Hence, given a well-controlled divider modulus, a PLL can generate frequencies in precise relation to its input. Establishing stable system dynamics is critical to ensure the above condition and is the subject of Section 2.4. As implied by (2.1), the spectral quality of the output depends on that of the reference input. Moreover, noise from components within the PLL degrades the overall spectral purity at the output.

2.2 Spectral Purity

Spectral purity is one the most important characteristic of a frequency synthesizer as it has direct implications on the capabilities of the intended system. Several metrics are used to quantify the spectral purity of signal sources. High performance oscillators

and PLLs, such as those found in RF communication systems, are usually characterized in terms of phase noise. On the other hand, jitter is the more common metric for non-sinusoidal signal sources, such as clock references in analog and digital circuits. In the following subsections, phase noise and jitter definitions are introduced and related to one another.

2.2.1 Phase Noise

An oscillator is generally susceptible to undesirable amplitude and phase fluctuations as expressed by:

$$v_o(t) = A(t)\sin(2\pi f_o t + \phi(t)) \tag{2.2}$$

which spread power away from its nominal frequency f_o. However, in most practical scenarios, amplitude perturbations are greatly suppressed or at least inconsequential to the intended application. Whereas an oscillator has no intrinsic ability to restore a momentary phase disturbance, its amplitude-limiting characteristic inherently restores amplitude deviations. Moreover, PLLs are mainly utilized as precise time or frequency references where the intended systems simply do not discriminate against small amplitude fluctuations. Hence, it is common practice to approximate $A(t)$ as a constant and draw attention to $\phi(t)$ instead.

Considering a simplified case where $\phi(t)$ is a wide-sense stationary (WSS) process with a root-mean-square value much smaller than 1 radian, the small-angle approxima-

tion may be applied to (2.2), giving:

$$v_o(t) \approx A\sin(2\pi f_o t) + A\phi(t)\cos(2\pi f_o t) \tag{2.3}$$

where we may distinguish the ideal signal from the unwanted phase noise term. The statistics of $v_o(t)$ are better appreciated in the frequency domain from its double-sided power spectral density (PSD), which can be expressed as [11, 12]:

$$P_{v_o}(f) = \int_{-\infty}^{\infty} R_{v_o}(\tau) e^{-j2\pi f\tau} d\tau \tag{2.4}$$

where $R_{v_o}(\tau)$ is the autocorrelation function of $v_o(t)$ and given by:

$$\begin{aligned} R_{v_o}(\tau) &= E\left[v_o(t+\tau)v_o(t)\right] \\ &= \frac{A^2}{2}\left[\cos(2\pi f_o\tau) + R_\phi(\tau)\cos(2\pi f_o\tau)\right] \end{aligned} \tag{2.5}$$

By virtue of the assumed wide-sense stationarity of $\phi(t)$, $R_{v_o}(\tau)$ only depends on the time interval τ. Substituting (2.5) into (2.4) gives:

$$P_{v_o}(f) = \frac{A^2}{2}\left[\delta(f \pm f_o) + \frac{1}{2}P_\phi(f \pm f_o)\right] \tag{2.6}$$

where $\delta(f)$ is the Dirac impulse function. Whereas (2.6) is valid over $-\infty < f < \infty$, the single-sided PSD (nonzero for $f \geq 0$) is the basis of the standard phase noise definition and is given by:

$$S_{v_o}(f) = \frac{A^2}{2}\left[\delta(f - f_o) + \frac{1}{2}S_\phi(f - f_o) + \frac{1}{2}S_\phi(f_o - f)\right] \tag{2.7}$$

$R_\phi(\tau)$, $P_\phi(f)$, and $S_\phi(f)$ in equations (2.5), (2.6), and (2.7) represent the autocorrelation function, double-sided PSD, and single-sided PSD of $\phi(t)$, respectively. Fig. 2.2

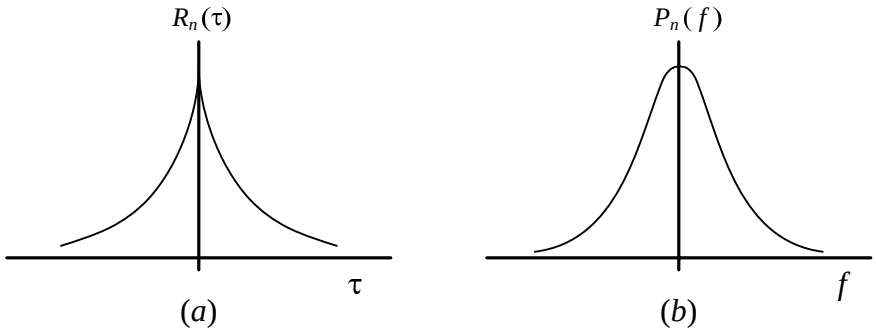


Figure 2.2: (*a*) $R_n(\tau)$ and (*b*) $P_n(f)$ of the thermal noise from a generic RC lowpass filter.

illustrates the relationship between the autocorrelation function $R(\tau)$ and the PSD $P(f)$ of a stochastic signal, $n(t)$ in this example. Since $R_n(\tau)$ is a measure of the correlation between samples of $n(t)$ taken at τ seconds intervals, its Fourier transform $P_n(f)$ is colored (i.e. frequency shaped) accordingly.

The single-sideband (SSB) phase noise is defined as the ratio in dB of the noise power in a 1Hz bandwidth at $f_o + \Delta f$ to the carrier power $A^2/2$, and is given by:

$$\begin{aligned} \mathcal{L}(\Delta f) &= 10 \log_{10} \left[\frac{\text{Noise Power in 1Hz at } f_o + \Delta f}{\text{Carrier Power}} \right] \\ &\approx 10 \log_{10} \left[\frac{S_\phi(\Delta f)}{2} \right] \end{aligned} \tag{2.8}$$

The units of (2.8) are dBc/Hz and a typical plot is shown in Fig. 2.3. As seen from Fig. 2.3, a typical free-running oscillator phase noise measurement is characterized by a $1/f^2$ slope. In practice, phase noise eventually plateaus as the system (which includes the measurement apparatus) noise floor is reached. Furthermore, the phase noise profile results from any type of noise, and is not restricted to the underlying conditions of

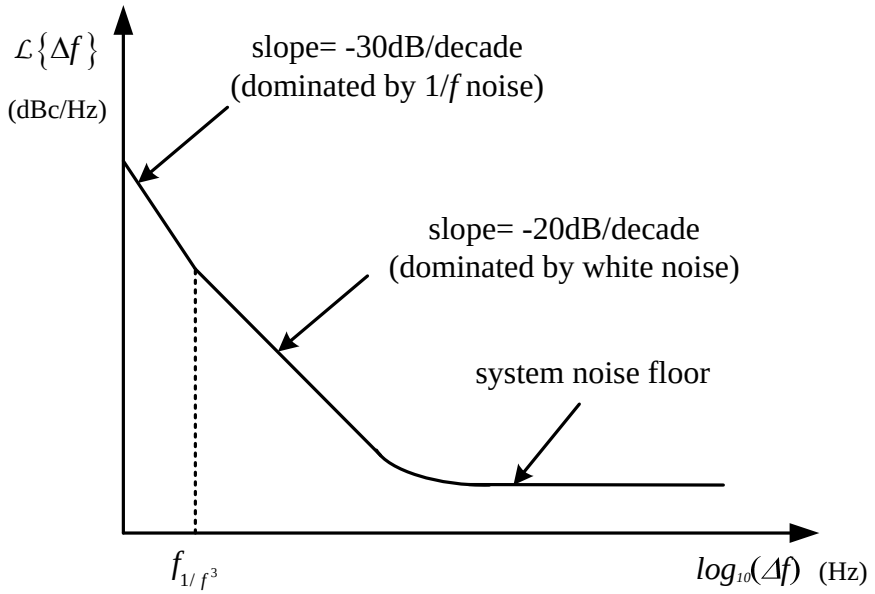


Figure 2.3: Typical measured plot of SSB free-running oscillator phase noise.

our simplified scenario where only WSS phase perturbations are considered. As such, colored and time-varying noise sources generally contribute and complicate derivations drastically [13–15]. In the presence of $1/f$ noise, the profile takes on a $1/f^3$ slope at offsets below f_{1/f^3}. Although not apparent from Fig. 2.3, the close-in phase noise does not keep rising as Δf approaches 0. This would falsely imply that phase noise is infinite at resonance. Intuitively, we expect the oscillator total output power to be finite and that its phase noise integrated from $-\infty$ to $+\infty$ is unity. In other words, we think of the output power of a noiseless oscillator as being conserved—such that noise only spreads power away from its nominal frequency while the total integrated power remains the same. Indeed, it has been shown that phase noise simplifies to a Lorentzian

spectrum in the absence of $1/f$ noise [14,16]. In cases where $1/f$ noise dominates at low offset frequencies, analytical derivations become more difficult but [16] shows that the close-in phase noise still conforms to similar characteristics—exhibiting a finite value as Δf approaches zero. Lastly, we note that lab instruments used to measure phase noise (e.g. spectrum analyzers) measure signal power in a certain resolution bandwidth swept across a chosen frequency range. Hence such instruments truly measure the (one-sided) PSD. Thus, because it simply reads off phase noise based on the measured PSD (scaled to yield the correct units), it cannot distinguish between phase and amplitude noise.

Phase noise degrades different aspects of the system, depending on the application. In RF transceivers, the local oscillator (LO) phase noise degrades the received signal signal-to-noise ratio (SNR) by a process known as reciprocal mixing. This effect is illustrated in Fig. 2.4. We note that in addition to the direct superposition of the LO phase noise on the downconverted channel, the presence of a nearby interferer further degrades the SNR of the desired signal. Thus, while close-in phase noise at offsets within the channel bandwidth is obviously important, far-out phase noise can also have significant impact on the system performance. In some applications, the LO phase noise specifications are the most difficult to meet at offsets far away from the carrier. Whereas close-in phase noise can be lowered to some extent by increasing the synthesizer loop bandwidth, far-out phase noise is typically dominated by the VCO. Hence, the design of low phase noise VCOs is key.

Sometimes phase noise is integrated over a bandwidth of interest, resulting in a

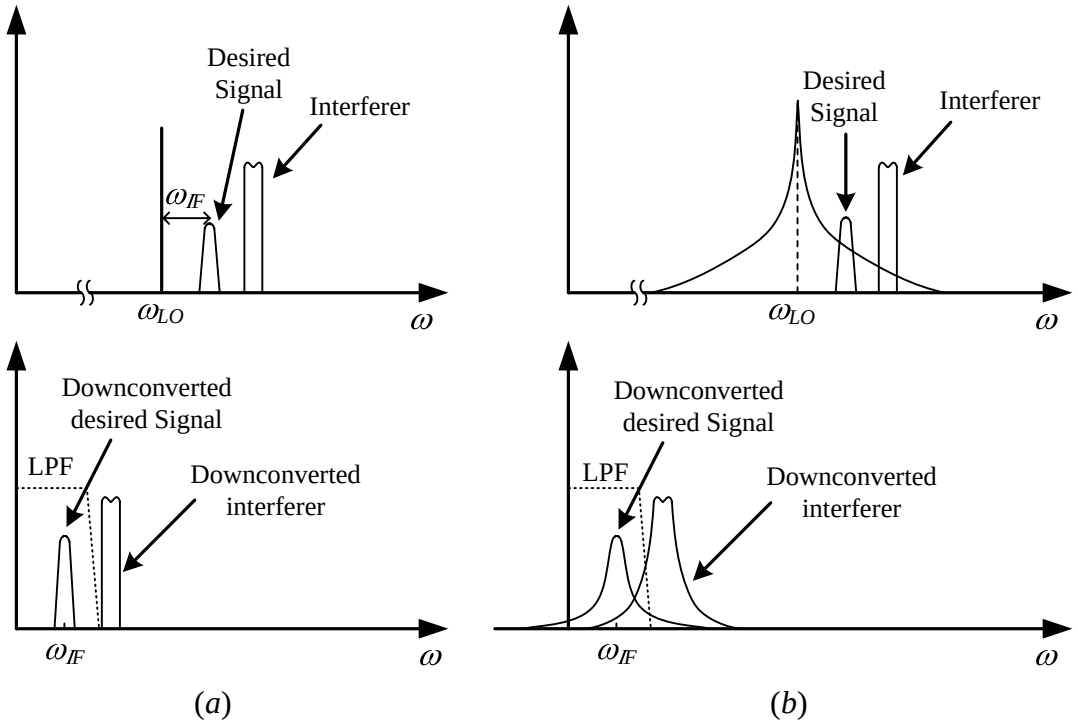


Figure 2.4: SNR degradation due to reciprocal mixing of unwanted signal.

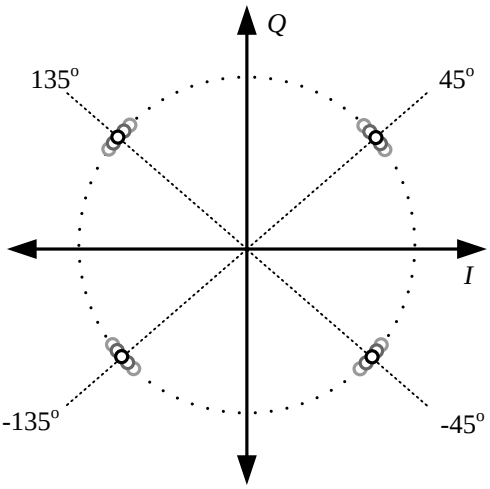


Figure 2.5: QPSK symbol constellation showing rotational error due to finite phase noise $\phi(t)$ on the LO.

quantity known as the RMS phase noise and given by:

$$\sigma_\phi^2 = \int_{\Delta f_L}^{\Delta f_H} S_\phi(\Delta f) d\Delta f \tag{2.9}$$

Phase noise also corrupts the information present in phase-modulated signals as $\phi(t)$ effectively rotates the symbol constellation. Assuming a $\phi(t)$ is Gaussian distributed, each point on the constellation spreads by about $\pm 3\sigma_\phi$ relative to its nominal phase. Hence, phase noise degrades the bit error rate (BER) of communication systems using phase modulation schemes. Fig. 2.5 shows a quadrature phase shift keying (QPSK) symbol constellation of quadrature signals (I and Q) downconverted by an LO with finite phase noise.

2.2.2 Jitter

As mentioned earlier, spectral purity is sometimes measured and quantified in the time domain. Timing jitter characterizes the deviation of signal transitions from their ideal periodicity. The presence of jitter implies that the oscillator period varies from one cycle to the next. Several definitions establish how such variations and their statistics are quantified.

The cycle jitter is defined as the difference between each cycle's period, T_k, and the average period, $\overline{T}$. Its rms value is given by [17]:

$$\sigma_c = \lim_{N\to\infty} \sqrt{\left(\frac{1}{N} \sum_{k=1}^{N} (T_k - \overline{T})^2 \right)} \tag{2.10}$$

Another common metric is the cycle-to-cycle jitter, which describes the timing error between successive periods. Its rms value is given by [17]:

$$\sigma_{cc} = \lim_{N\to\infty} \sqrt{\left(\frac{1}{N} \sum_{k=1}^{N} (T_{k+1} - T_k)^2 \right)} \tag{2.11}$$

Unlike the cycle jitter, the cycle-to-cycle jitter captures short-term variations.

The absolute, or accumulated, jitter at the N-th cycle is given by:

$$\Delta T_{abs}(N) = \sum_{k=1}^{N} (T_k - \overline{T}) \tag{2.12}$$

Fig. 2.6 illustrates jitter accumulation at the output of a free-running oscillator where the grey shaded areas represent the statistics of the transition time uncertainty. From Fig. 2.6, we may define $\sigma_{\Delta T}$ as the standard deviation or rms value of the absolute jitter. For a free-running oscillator, since the timing error of any given transition necessarily

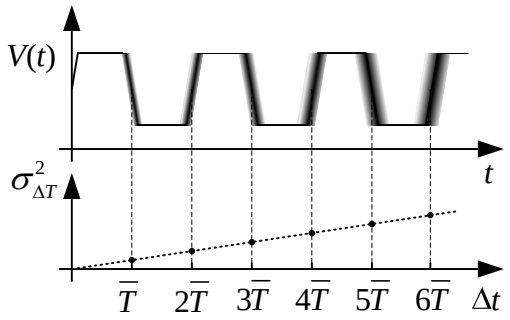


Figure 2.6: Time waveform showing jitter with statistics underneath.

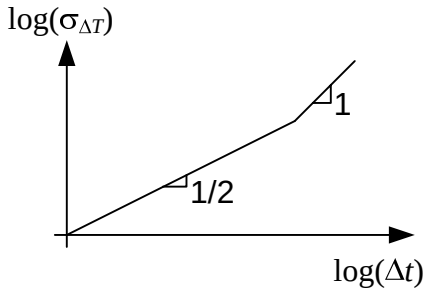


Figure 2.7: $\log(\sigma_{\Delta T})$ vs. $\log(\Delta t)$.

contributes to that of future transitions, $\sigma_{\Delta T}$ has the interesting property that it grows with the measurement interval $\Delta t = N \cdot \overline{T}$ [18, 19]. This characteristic is illustrated in Fig. 2.7 showing a typical jitter measurement, where different correlations among noise contributors result in regions of different slope [18–20]. The slope of 1/2 is attributed to uncorrelated noise sources, since $\sigma_{\Delta T}$ results from the square root of the sum of the variances (from each independent noise contributor). Correlated noise sources, such as $1/f$ and supply noise, add directly and result in a slope of unity (assuming perfect correlation).

In order to establish a link between jitter and phase noise, we may express $\sigma_{\Delta T}$ in terms of the rms phase jitter:

$$\sigma_{\Delta\phi} = 2\pi f_o \, \sigma_{\Delta T} \tag{2.13}$$

The rms phase jitter itself can be traced back to $\phi(t)$ and its statistics, which were introduced in Section 2.2.1 [20, 21]:

$$\begin{aligned} \sigma^2_{\Delta\phi} &= E\left\{[\phi(t+\Delta t) - \phi(t)]^2\right\} \\ &= 2\left[R_\phi(0) - R_\phi(\Delta t)\right] \\ &= 2\int_{-\infty}^{\infty} P_\phi(f)\left(1 - e^{j2\pi f \Delta t}\right) df \\ &= 4\int_0^{\infty} S_\phi(f)\sin^2(\pi f \Delta t) df \end{aligned} \tag{2.14}$$

Using (2.8), (2.13), and (2.14), we obtain:

$$\sigma^2_{\Delta T}(\tau) = \frac{8}{\omega_o^2}\int_0^{\infty}\left(10^{\mathcal{L}(\Delta f)/10}\right)\sin^2(\pi\Delta f\tau) d\Delta f \tag{2.15}$$

where $\omega_o = 2\pi f_o$. Equation (2.15) provides a way to estimate timing jitter given that phase noise is known and its validity is limited to all aforementioned assumptions. More general approaches are discussed in [14]. If phase noise is due to white noise only, it can be related to the cycle-to-cycle jitter by a compact expression [17, 19]:

$$\mathcal{L}(\Delta f) \approx \log_{10}\left[\frac{f_o^3\sigma_{cc}^2}{2\Delta f^2}\right] \tag{2.16}$$

which is valid at offsets where phase noise rolls off as $1/\Delta f^2$.

2.3 PLL Core Building Blocks

2.3.1 Voltage-Controlled Oscillators

The voltage-controlled oscillator (VCO) is perhaps one of the most challenging blocks to design in a high-performance PLL. It typically represents the bottleneck of the achievable noise performance. Although ring- or relaxation-type oscillators can be found in some applications (e.g. serial data links), their poor phase noise performance disqualifies them in most RF applications. Thus, this work focuses on resonator-based or LC VCOs. The output frequency of a VCO is adjustable by means of a control voltage V_{tune}, such that:

$$F_{out} = f_o + K_v \cdot V_{tune} \tag{2.17}$$

where K_v is the tuning sensitivity, also known as VCO gain, and f_o is the nominal resonant frequency of the VCO when $V_{tune} = 0$V. Typically, this function is achieved using a varactor (i.e. voltage-controlled capacitor). A generic schematic of an LC-VCO is shown in Fig. 2.8. Noting that phase is the integral of frequency, the excess phase at the output in response to V_{tune} is given by $\theta_{out} = 2\pi K_v \int_{-\infty}^{t} V_{tune}(\tau)d\tau$, which may be rearranged in the frequency domain by applying the Laplace transform:

$$\frac{\theta_{out}}{V_{tune}}(s) = 2\pi\frac{K_v}{s} \tag{2.18}$$

where $s = j2\pi f$. Thus, a VCO behaves as an ideal phase integrator in the s-domain. In practice, K_v is not constant and typically varies as a function of V_{tune}. K_v may have

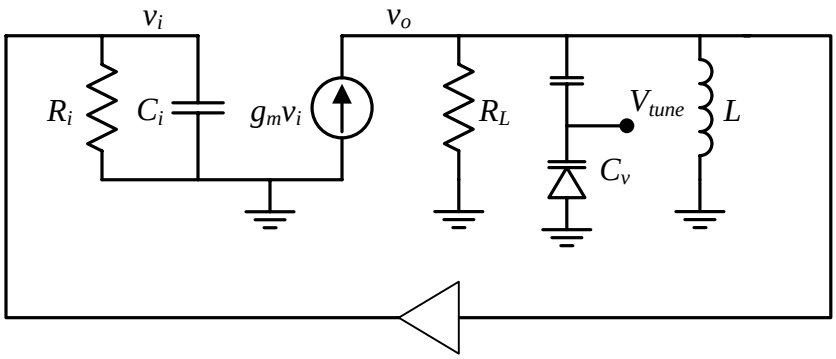


Figure 2.8: Generic *LC* VCO.

additional dependencies, depending on the particular configuration. As discussed in Section 2.5, K_v has a strong impact on the noise performance of the PLL.

2.3.2 Frequency Dividers

The frequency divider takes the VCO output and divides its frequency by some programmable number N—typically an integer. Although there are many ways to implement this functionality, a widely used architecture is known as the pulse-swallow divider and is shown in Fig. 2.9 [22]. It consists of a $M/M+1$ prescaler followed by a programmable counter and a pulse-swallowing counter. Upon reset, the prescaler divides by $M+1$. After S cycles of the pulse-swallow counter, it divides by M until the program counter has counted P cycles, upon which reset is asserted and the cycle repeats. Thus, given programmable integers P and S and $P \geq S$, a single cycle of the divided output F_{div} will contain exactly $(M+1)S + M(P-S)$ cycles of F_{out}. Hence,

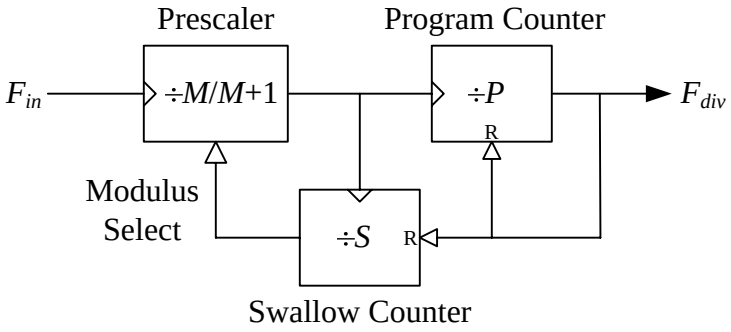


Figure 2.9: Programmable Frequency Divider.

the divide ratio is given by:

$$N = P \cdot M + S \tag{2.19}$$

From (2.19), we can see that this configuration can achieve a wide range of integer divide ratios. The achievable contiguous range is $N_{\min} = M(M-1)$ to $N_{\max} = (2^n - 1)(M+1)$, where n is the number of bits in counters P and S (and provided that $P \geq S$ and $n > \log_2(M+1)$). A frequency divider can be seen as a phase divider, for which the phase domain transfer function is given by:

$$\theta_{div}(s) = \frac{\theta_{out}(s)}{N} \tag{2.20}$$

2.3.3 Phase Detectors

The function of a phase detector is to measure the phase difference of two incoming signals and output a signal proportional to it. In practice, phase detectors may not exhibit a linear input-output relationship. Many implementations exist and provide different trade-offs to the designer [23]. In the design space of RF PLL frequency

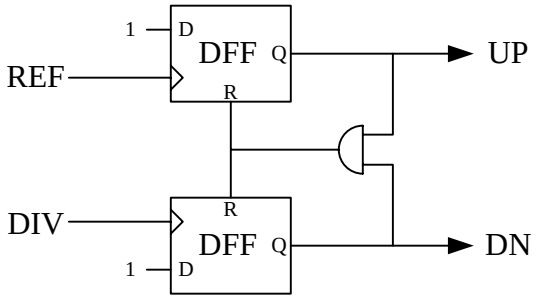


Figure 2.10: Tri-state phase-frequency detector (PFD).

synthesizers, the tri-state phase-frequency detector (PFD) is one of the most common topology. As its name implies, a PFD detects both phase and frequency and is shown in Fig. 2.10. By virtue of its configuration, the tri-state PFD outputs two signals, UP and DN, pulse-width modulated as a function of the phase and frequency difference between the REF and DIV inputs. Its transition state diagram and typical signal waveforms are shown in Fig. 2.11. The rising edge of REF makes UP=1 and the rising edge of DIV makes DN=1. However, the AND gate resets both flip-flops to 0 as soon as it detects that UP=DN=1. When UP=1, REF is leading DIV by a phase difference commensurate with its pulse width and vice versa. Thus the action of the loop will force the VCO frequency to be increased (decreased) according to the pulse width of UP (DN). Hence, the phase detector determines the polarity of the feedback loop. Finally, the edge-triggered nature of the PFD makes it insensitive to the duty cycle of its inputs. Having the phase error encoded as the width of UP and DN pulses means that some conversion must take place before it can effectively interface with the VCO. Typically,

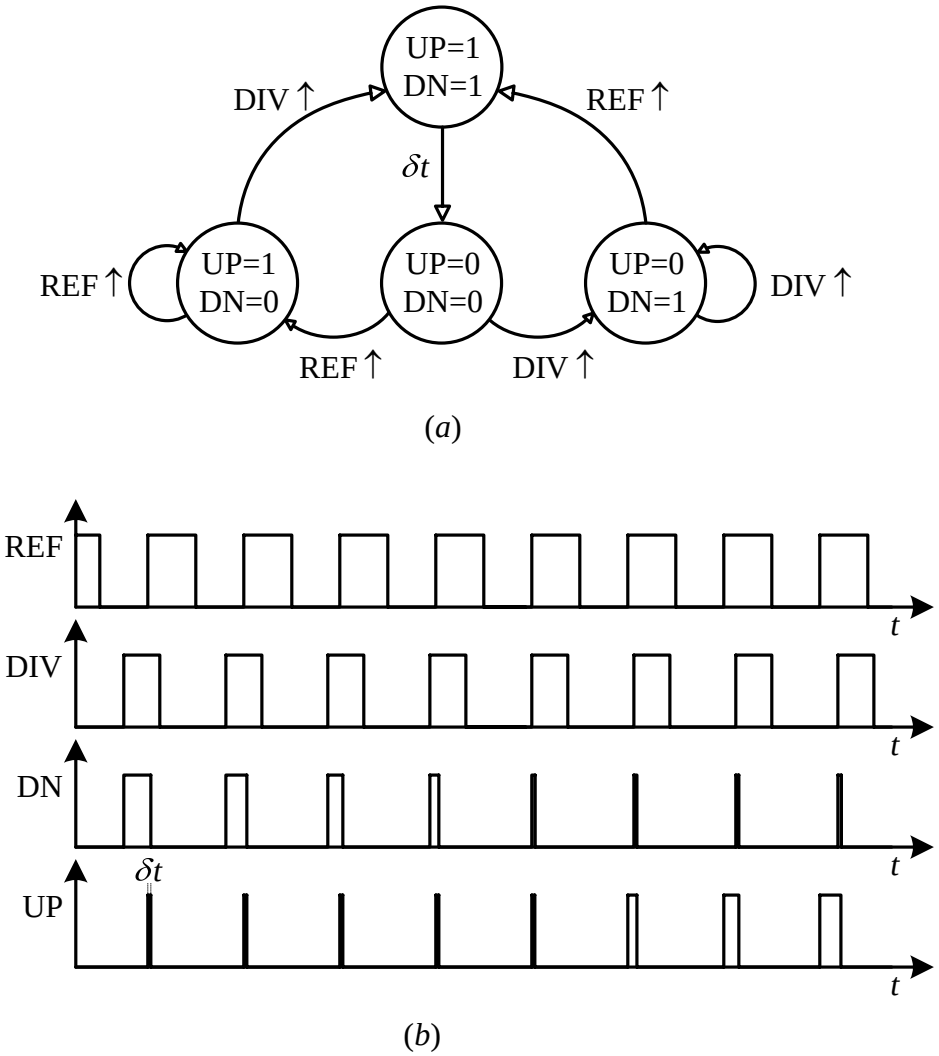


Figure 2.11: (a) Tri-state PFD transition state diagram and (b) signal waveforms.

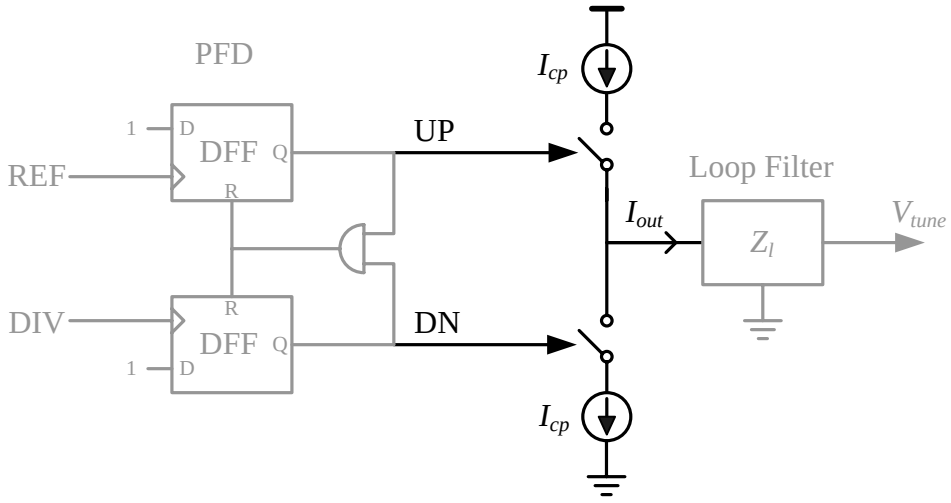


Figure 2.12: Simplified schematic of a charge-pump driven by a PFD and loaded by an arbitrary loop filter.

part of this conversion is achieved with a charge-pump. The charge-pump converts the pulse-modulated phase error into a well-defined charge. The charge is then translated to a voltage by the loop filter in order to drive the tuning port of the VCO. Fig. 2.12 shows a simplified schematic of the charge-pump. The functions of the PFD and charge-pump are so closely coupled that they are often considered a unit and described by a combined transfer characteristic as shown in Fig. 2.13. As seen from Fig. 2.13, the (tri-state) PFD-CP combination ideally yields a transfer function characterized by a constant slope of $I_{cp}/2\pi$ over the input range -2π to 2π. Outside of this range, the PFD-CP behaves as a frequency discriminator driving the VCO frequency back towards the origin. Hence, proper functionality of this particular PFD-CP is ideally sustained for arbitrarily large phase and frequency differences. As a result, the PLL pull-in range (the range of frequency difference over which the PLL is able to acquire lock) is limited

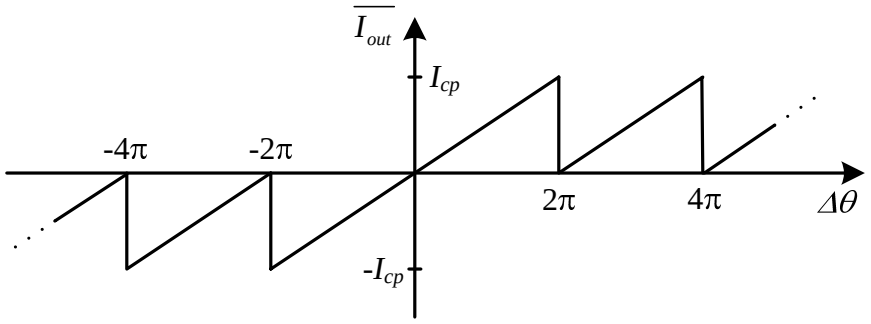


Figure 2.13: Ideal PFD-CP phase to average current transfer characteristic.

by other components in the loops. Once the PLL has reached lock, the phase error is ideally 0 and the PFD-CP transfer function can be written as follows

$$K_p = \frac{\overline{I_{out}}}{\Delta\theta} = \frac{I_{cp}}{2\pi} \tag{2.21}$$

In practice, several factors degrade the above characteristic. In the locked condition, the phase error ideally goes to 0 which makes the width of the UP and DN pulses go to 0 as well. But the charge-pump switches cannot respond to infinitesimally narrow pulses, making the loop incapable of tracking infinitesimally small phase errors. Hence, there exist a very small range of input phase in the vicinity of $\theta_e = 0$ where the loop is inactive and is known as the dead-zone [24]. Although this effect usually does not prevent the overall PLL from functioning, it typically results in degraded spectral purity at close-in offsets. Fortunately, this region can be effectively removed by adding sufficient delay to the reset signal path such that the UP and DN pulses have a finite on-time in the locked condition ensuring that the charge-pump turns on briefly during each cycle. Even though the charge-pump turns on every cycle, its net output current properly

sums to 0 once the PLL is locked. The addition of a delay to avoid the dead-zone introduces a few penalties. First, even if the charge-pump outputs zero net charge in the locked condition, it introduces noise during its brief activation. Secondly, intrinsic and extrinsic propagation delays along the reset path of the PFD shown in Fig. 2.10 limit the maximum frequency of operation to $f_{max} = 1/(2\delta t)$ [25], where δt is the total delay of the reset path. Another important impairment of the PFD-CP results from the mismatch between UP and DN charge-pump currents. This makes K_p take on a different value depending on the polarity of the phase error and thus introduces a nonlinear kink at the point of the transfer function where the PLL operates when locked. Such nonlinearities may lead to various types of spectral degradations, depending on the architecture [24].

2.3.4 Loop Filters

The main function of the loop filter is to establish the desired PLL dynamics for the intended application. The loop filter also has a profound impact on spectral purity. Intuitively, we realize that any disturbance not sufficiently filtered appears on the tuning port of the VCO and directly translates to phase noise at the output. As mentioned in Section 2.3.3, the loop filter also provides a current-to-voltage conversion necessary to interface the charge-pump with the VCO. Using a simple shunt capacitor is arguably one of the most efficient ways of achieving this. Indeed, a capacitor avoids any dynamic range penalty and conveniently provides an unrestricted DC voltage range which ensures

that the entire VCO tuning range can be exploited. However, recall that the VCO itself contributes a pole at the origin. Thus, the addition of another pole at DC (assuming the charge-pump output resistance is infinite) from the loop filter brings the total number of ideal integrators to two and the PLL is said to be of "type-II". Of course, a capacitor by itself is not sufficient as it would render the loop unstable since two integrators alone provide zero phase margin. Practical loop filters usually provide a lead-compensating zero, ω_z, followed by one or several poles, ω_i, in addition to the pole at DC. Such filters come in passive and active forms, each of which provides its own set of pros and cons. The transfer function of a generic second-order loop filter (resulting in a third-order type-II PLL) is given by:

$$Z_l(s) = \frac{Kl}{s} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_1} \tag{2.22}$$

A passive implementation of (2.22) is trivial in any technology and is very widely used. It is illustrated in Fig. 2.14(a). From Fig. 2.14(a), we obtain $K_l = 1/(C_1 + C_2)$, $\omega_z = 1/(R_1C_1)$, and $\omega_1 = R_1C_1C_2/(C_1+C_2)$. Although slight variations exist, the above implementation is popular for integrated solutions since the parasitic bottom plate of C_1 and C_2 are shorted to ground, thus preventing undesired coupling of substrate noise [31]. The loop filter is sometimes increased to third- or fourth-order. For example, a common third-order loop filter implementation is that of Fig. 2.14(a) followed by an additional RC stage. In some cases, other out-of-band RC stages may be added to further attenuate far-out reference spurs with negligible effect on the loop phase margin. Fig. 2.14(b) illustrates the analogous active implementation of the second-order

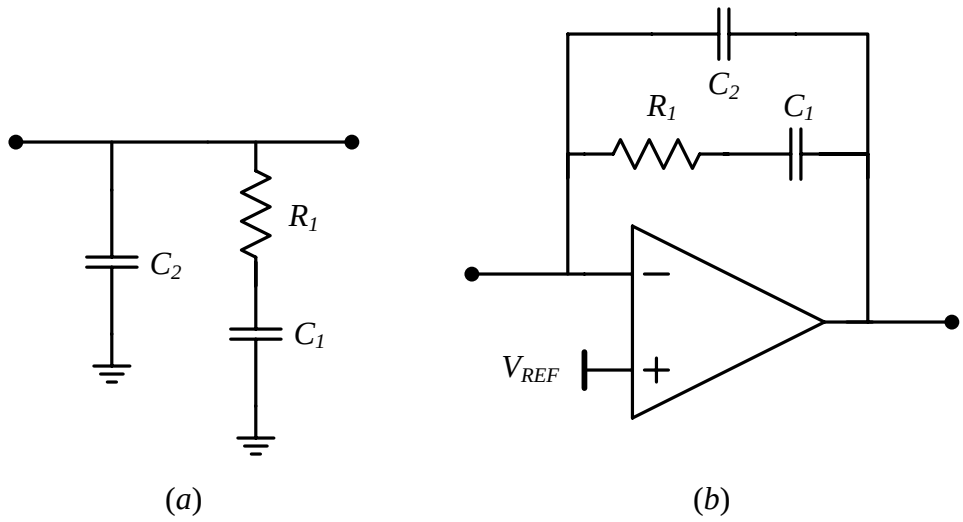


Figure 2.14: (a) second-order passive loop filter. (b) second-order active loop filter.

loop filter. While active loop filters introduce penalties in terms of noise and power consumption, they present a virtual AC ground to the charge-pump output which can be advantageous and sometimes indispensable. Furthermore, certain active loop filter configurations are able to synthesize large effective time constants without large passive devices, thus saving die area at the expense of power consumption and complexity [26, 27].

2.4 PLL Dynamics

In Section 2.3, we derived continuous-time small-signal (linearized) transfer functions for each block of a basic PLL in its steady-state locked condition. However, the dynamic operation of a PLL itself relies on a momentary nonlinear acquisition (or pull-

in) process. Furthermore, the edge-sensitive nature of the PFD-CP makes the PLL operate as a discrete-time system with a sampling rate of F_{pfd} (F_{ref} in steady-state) such the phase error is known only at each sampling instant. Hence, a general PLL model is neither linear nor continuous-time. Nevertheless, a linearized continuous-time model based on steady-state conditions is sufficiently accurate to capture many of the desired steady-state performance metrics, such as noise and stability. The smaller the loop bandwidth, F_c, is relative to F_{ref}, the better continuous-time models are able to approximate the operation of the loop (in steady-state). In practice, continuous-time approximations introduce negligible error for $F_c/F_{ref} < 1/10$ [28].

2.4.1 Linear model of third-order PLL

The foregoing discussion introduces linearized continuous-time transfer functions valid for a third-order type-II PLL (based on the second-loop filter discussed in Section 2.3.4). Practical PLLs may not only come in configurations of different order, but may also be based on different building blocks, all of which would alter our analysis. Nevertheless, this discussion is based on a very common topology and shall provide insight applicable to other scenarios. Fig. 2.15 illustrates the PLL block diagram including the transfer functions of each component. From Fig. 2.15, we may express the open-loop transfer function $T(s) = \theta'_{div}(s)/\theta_{div}(s)$ as:

$$T(s) = 2\pi \frac{K_p Z_l K_v}{sN} = K_o \cdot \frac{(1 + s/\omega_z)}{s^2(1 + s/\omega_1)} \tag{2.23}$$

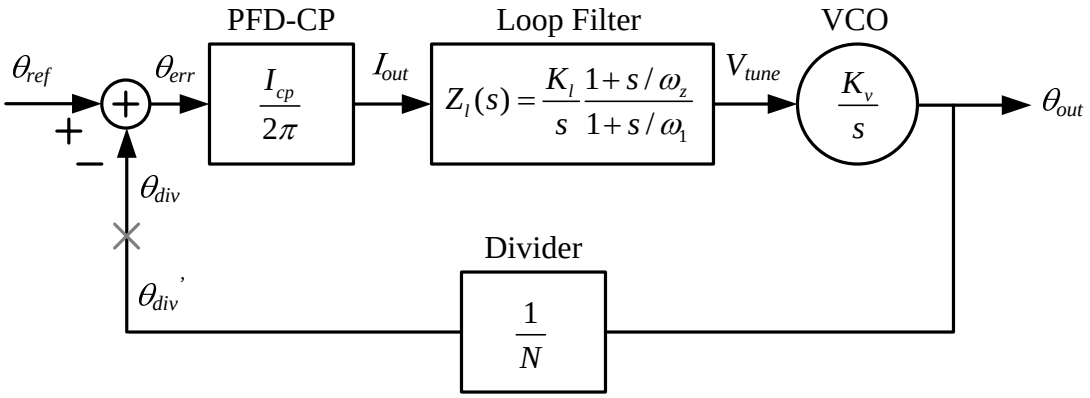


Figure 2.15: Linear model of third-order PLL.

where $K_o = I_{cp}K_lK_v/N$. The loop dynamics are completely characterized by (2.23) and are illustrated in Figs. 2.16 showing the amplitude and phase response of $T(s)$. The loop bandwidth corresponds to the frequency where $|T(s)| = 0$ dB and is labeled ω_c on Fig. 2.16. Choosing ω_c typically involves trading off lock time for spurious rejection. However, other configuration-dependent variables generally come into play as well. Fig. 2.16 clearly shows the benefit of the lead-compensation zero ω_z, providing a substantial boost to the phase margin. Beyond ω_z, ω_1 eventually begins to take effect and restores the response roll off to its original rate of -40dB/decade. The phase margin ϕ_M is given by:

$$\phi_M = \pi + \angle T(j\omega_c) = (\pi - n_i\pi/2) + tan^{-1}(\omega_c/\omega_z) - \sum_{i=1}^{n_p} tan^{-1}(\omega_c/\omega_i) \qquad (2.24)$$

where n_i and n_p are the number of integrators and poles, respectively. For the case of the third-order type-II PLL described above, (2.24) yields $\phi_M = tan^{-1}(r_z) - tan^{-1}(1/r_1)$ where $r_z = \omega_c/\omega_z$ and $r_1 = \omega_1/\omega_c$. From (2.24), it is apparent that ϕ_M is solely

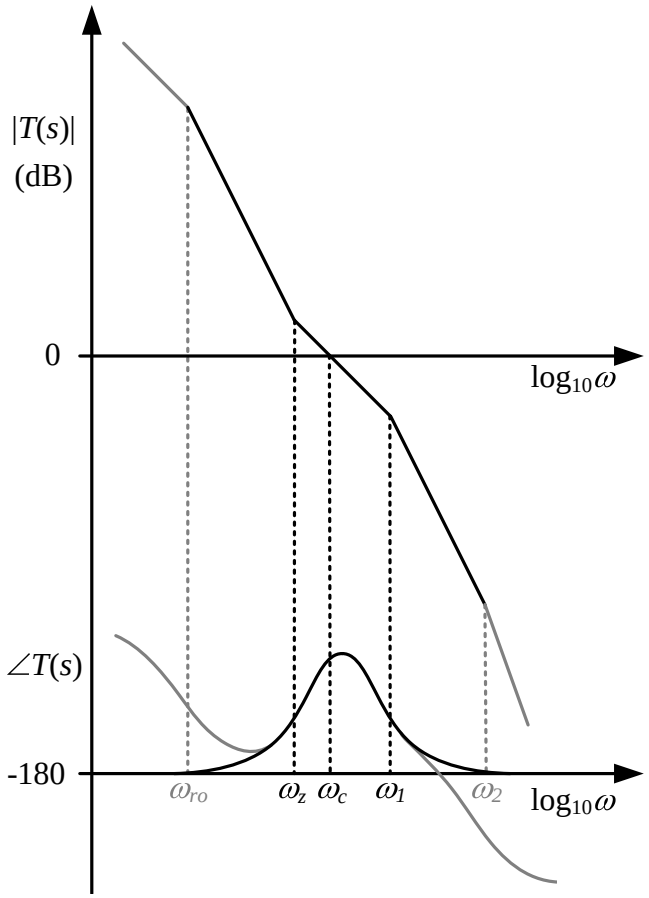


Figure 2.16: $20\log_{10}(|T(s)|)$ and $\angle T(s)$ for third-order PLL. The effects of parasitic poles from the finite output resistance of the charge-pump (ω_{ro}) and an out-of-band RC filter (ω_2) are shown in grey.

dependent on the ratios of each pole/zero to ω_c. Hence, for a chosen loop bandwidth and PLL type and order, the desired phase margin sets the location of poles/zeros relative to ω_c. Whereas maximizing ϕ_M improves stability and lessens the amount of peaking, lock time requirements typically set an upper-bound. In practice, values around 45–55 degrees are common [29]. Based on ω_c and the pole/zero spacings corresponding to the desired phase margin, K_o can be solved by setting $|T(j\omega_c)| = 1$. For the third-order type-II PLL, it is given by $K_o = (\omega_c^2/r_1) \cdot \sqrt{1+r_1^2}/\sqrt{1+r_z^2}$. And for the case where $r_z = r_1 = r$, $K_o = \omega_c^2/r$. Additional constraints, such as noise and die area, will then determine to what amount each loop parameter (I_{cp}, K_l, K_v, N) contributes to K_o. The grey line on Fig. 2.16 illustrates the effect of the finite output resistance of the charge pump. The presence of an out-of-band (parasitic or intentional) pole, ω_2, is also considered and indicated with another grey line to illustrate its effect on the amplitude and phase response. If sufficiently higher than ω_1, ω_2 has a negligible impact on ω_c and ϕ_M.

From (2.23), we may obtain the closed-loop transfer function $H(s) = T(s)/(1+T(s))$ given by:

$$\begin{aligned} H(s) &= \frac{2\pi K_p Z_l K_v/N}{s + 2\pi K_p Z_l K_v/N} \\ &= \frac{(1+s/\omega_z)}{1 + s\dfrac{1}{\omega_z} + s^2\dfrac{1}{K_o} + s^3\dfrac{1}{\omega_1 K_o}} \end{aligned} \tag{2.25}$$

where the third-order nature of the transfer function is apparent. As shown graphically in Fig. 2.17, $H(s)$ essentially follows a low-pass profile with a passband bounded by ω_c

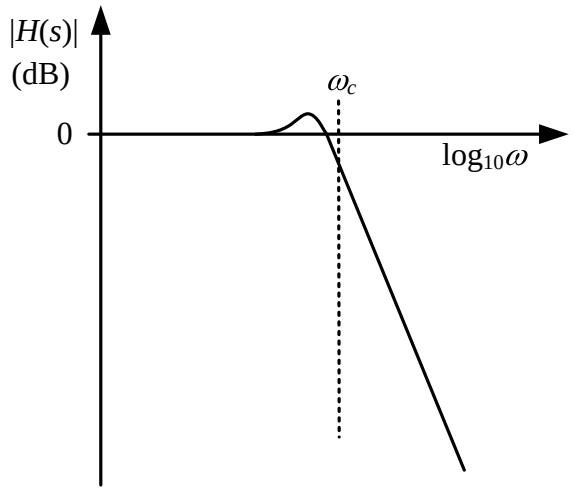


Figure 2.17: Magnitude response of $H(s)$.

and rolling off at -40dB/decade. The presence of ω_z results in some amount of peaking above 0dB just before reaching ω_c.

2.4.2 Transient Response

The lock-time is the time needed to switch and settle to a prescribed frequency within a given error. It is often one of the key specifications of a PLL. The linear component of the settling time can be determined from the step response of (2.25). For small frequency jumps, this provides a fairly good approximation of the locking process. For large frequency jumps, a nonlinear behavior (analogous to the slewing behavior of amplifiers) may be observed over a significant portion of the settling response. Let us begin with the simpler case where the locking process is approximated by the linear step response of $H(s)$.

In general, the closed-loop transfer function $H(s)$ maybe expressed as the ratio of two polynominals $N(s)$ and $D(s)$:

$$H(s) = \frac{N(s)}{D(s)} = k \cdot \frac{\prod_{i=1}^{n_z}(s - z_i)}{\prod_{i=1}^{n_p}(s - p_i)} \tag{2.26}$$

where z_i's are the zeros, p_i's are the poles, n_z and n_p are the number of zeros an poles, respectively, and k is some constant resulting from the factorization of the original polynomial (not explicitly shown). In PLL applications, $n_p \geq n_z$ and (2.26) is said to be a proper rational function. Partial fraction expansion methods are typically applied to (2.26) to achieve a form having a simple inverse Laplace transform. The step response of the output frequency, $F_{o,step}$, to an input frequency step $\Delta F_{step} = \Delta F_o/N_2$ (resulting from a change in divide ratio from N_1 to N_2) is obtained from:

$$F_{o,step}(t) = L^{-1}\left\{N_2 H(s)\frac{\Delta F_{step}}{s}\right\} = \Delta F_o \cdot s(t) \tag{2.27}$$

where $s(t)$ is the unit step response and is given by:

$$s(t) = L^{-1}\left\{H(s)\frac{1}{s}\right\} \tag{2.28}$$

Equation (2.28) gives the frequency or phase response to a unit step input of frequency (in Hz) or phase (in radians), respectively. Similarly, the error step response of the output frequency obtained from:

$$\begin{aligned} \varepsilon_{F_{o,step}}(t) &= L^{-1}\left\{(1 - H(s))\frac{\Delta F_o}{s}\right\} \\ &= \Delta F_o \cdot \varepsilon(t) \end{aligned} \tag{2.29}$$

where $\varepsilon(t)$ is the unit step error response and is given by:

$$\varepsilon(t) = 1 - s(t) = L^{-1}\left\{(1 - H(s))\frac{1}{s}\right\} \tag{2.30}$$

Similarly, (2.30) gives the frequency or phase error response to a unit step input of frequency (in Hz) or phase (in radians), respectively. While useful, (2.27)-(2.30) are not always tractable, due to the difficulty in performing the inverse Laplace transform analytically when the order of $H(s)$ is greater than two.

To gain better insight, we may ignore high-order term in (2.25) and approximate it with a second-order transfer function given by:

$$\begin{aligned} H(s) &\approx \frac{(1 + s/\omega_z)}{1 + s\dfrac{1}{\omega_z} + s^2\dfrac{1}{K_o}} \\ &= \omega_n^2 \cdot \frac{s2\zeta/\omega_n + 1}{s^2 + 2\zeta\omega_n + \omega_n^2} \end{aligned} \tag{2.31}$$

The system's natural (angular) frequency is given by $\omega_n = \sqrt{K_o}$ and the damping factor is given by $\zeta = \omega_n/(2\omega_z)$. Ignoring high-order terms of $H(s)$ leads to a poor estimate of the initial characteristics of the transient response, but often captures the long-term settling behavior with sufficient accuracy. The poles of (2.31) are given by the quadratic formula:

$$p_{1,2} = \zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1} \tag{2.32}$$

For the critically damped case where $\zeta = 1$, we have $p_{1,2} = \omega_n$; and for the common under-damped case where $0 < \zeta < 1$, (2.32) yields a complex conjugate pair of poles $p_{1,2} = \zeta\omega_n \pm j\omega_n\sqrt{1 - \zeta^2}$. The unit (normalized) step error response of (2.32) can now

be solved from the inverse Laplace transform, as in (2.30), and is given by [30]

$$\begin{aligned}\varepsilon(t) &= \frac{1}{2}\left\{\left(\frac{\zeta}{\sqrt{\zeta^2-1}}+1\right)e^{-\omega_n t\left(\zeta+\sqrt{\zeta^2-1}\right)}-\left(\frac{\zeta}{\sqrt{\zeta^2-1}}-1\right)e^{-\omega_n t\left(\zeta-\sqrt{\zeta^2-1}\right)}\right\}\\ &= \begin{cases} 0\le\zeta<1: & e^{-\zeta\omega_n t}\left[\cos\left(\omega_n t\sqrt{1-\zeta^2}\right)-\frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]\\ \zeta=1: & e^{-\omega_n t}\left[1-\omega_n t\right]\\ \zeta>1: & e^{-\zeta\omega_n t}\left[\cosh\left(\omega_n t\sqrt{\zeta^2-1}\right)-\frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(\omega_n t\sqrt{\zeta^2-1}\right)\right]\end{cases}\end{aligned} \tag{2.33}$$

and depends only on the damping factor and the natural frequency. The unit (normalized) step response is easily obtained by subtracting $\varepsilon(t)$ from unity (see (2.30)). Furthermore, (2.33) can be scaled as desired to obtain the output frequency or phase step response due to a given input frequency or phase step, respectively, as in (2.27) and (2.29). Fig. 2.18 shows the normalized error response vs. $\omega_n t$ for varying damping levels. Although, the above derivation is seldom feasible for higher order, a similar derivation can be achieved for a special case of the third-order type-II loop described above [30]. This special case was already mentioned in Section 2.4.1 and is characterized by ω_z and ω_1 being equally spaced with respect to ω_c such that $r = \omega_1/\omega_c = \omega_c/\omega_z$. Thus $H(s)$ may be expressed as:

$$\begin{aligned}H(s) &= \frac{\omega_c^2 r}{(s+\omega_c)}\cdot\frac{s+\omega_c/r}{s^2+\omega_c(r-1)s+\omega_c^2}\\ &= \frac{\omega_c^2(2\zeta_r+1)}{(s+\omega_c)}\cdot\frac{s+\omega_c/(2\zeta_r+1)}{s^2+2\zeta_r\omega_c s+\omega_c^2}\end{aligned} \tag{2.34}$$

where $\zeta_r = (r-1)/2$. Performing partial fraction methods on (2.34), followed by the

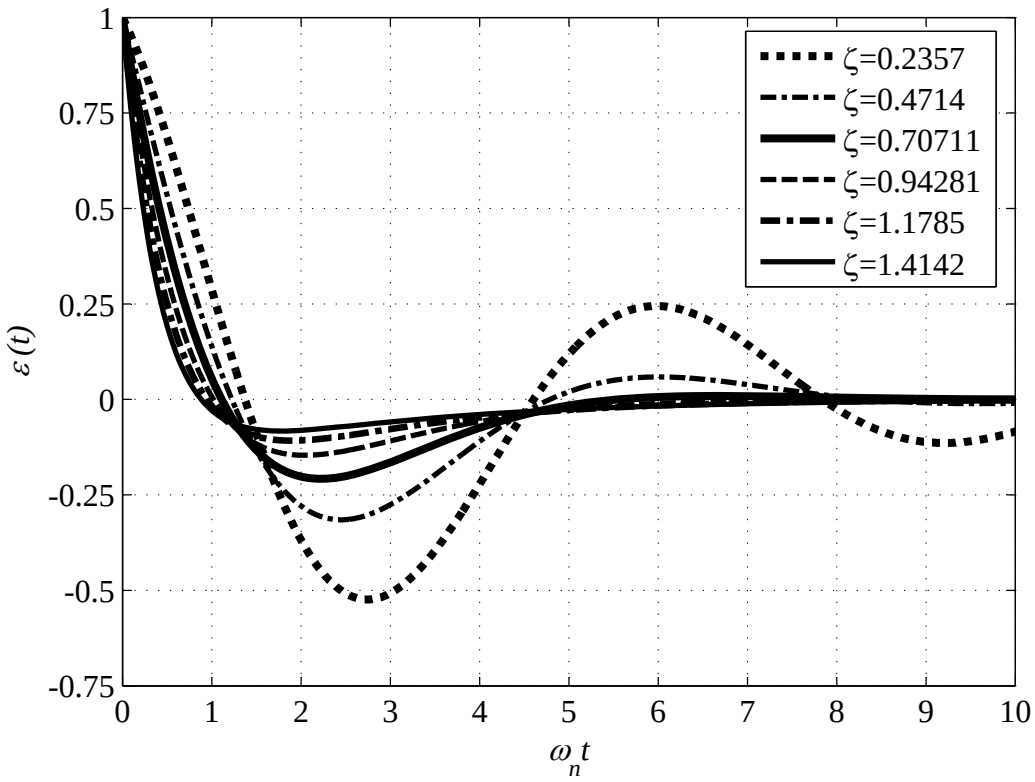


Figure 2.18: Unit step error response $\varepsilon(t)$ vs. $\omega_n t$ of second-order PLL.

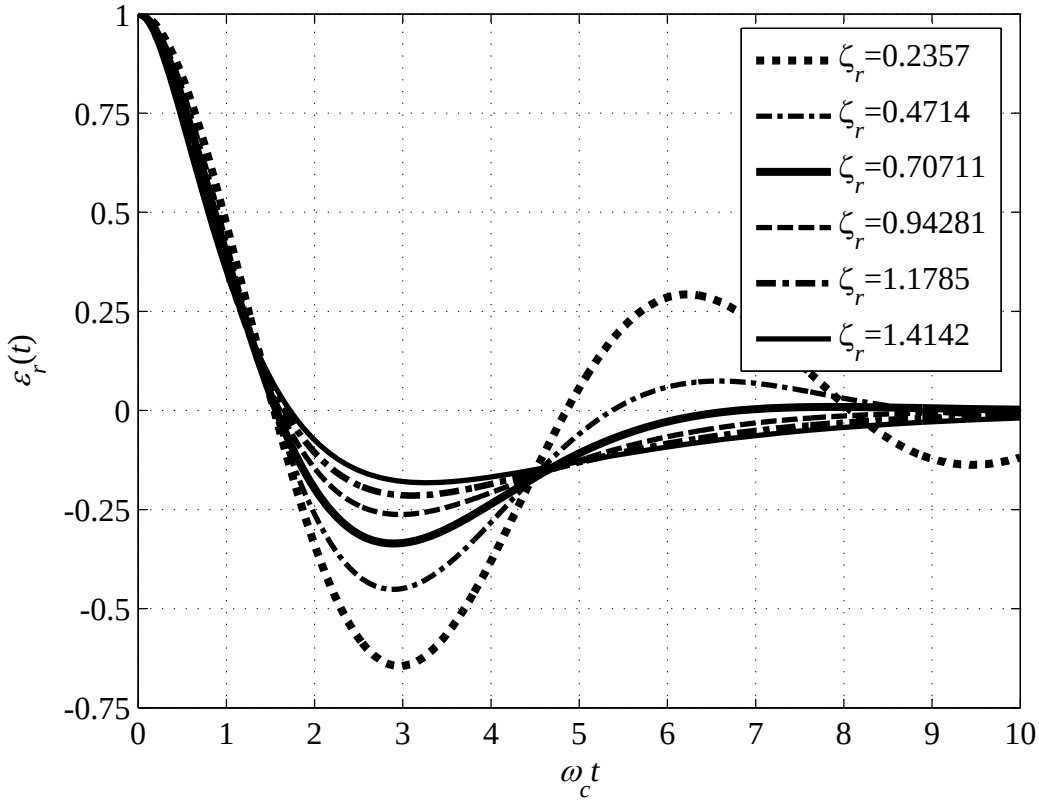


Figure 2.19: Unit step error response $\varepsilon_r(t)$ vs. $\omega_c t$ of third-order PLL with $\zeta_r = (r-1)/2$, where $r = \omega_c/\omega_z = \omega_1/\omega_c$.

application of (2.30), we obtain the error response as function of $\omega_c t$ and ζ_r [30]:

$$\varepsilon(t) = \begin{cases} 0 \le \zeta < 1: & \dfrac{1}{\zeta_r - 1}\left[\zeta_r e^{-\omega_c t} - e^{-\zeta_r \omega_c t}\cos\left(\omega_c t\sqrt{1-\zeta_r^2}\right)\right] \\ \zeta_r = 1: & e^{-\omega_c t}\left[1 + \omega_c t - \omega_c^2 t^2\right] \\ \zeta_r > 1: & \dfrac{1}{\zeta_r - 1}\left[\zeta_r e^{-\omega_c t} - e^{-\zeta_r \omega_c t}\cosh\left(\omega_c t\sqrt{\zeta_r^2-1}\right)\right] \end{cases} \tag{2.35}$$

Fig. 2.19 shows the normalized error response vs. $\omega_c t$ for varying values of ζ_r (i.e. r).

The above analysis was based on the small-signal linear settling behavior. In practice, the locking process may experience a nonlinear behavior during the initial part of its response. The duration of this nonlinear response may be significant and can

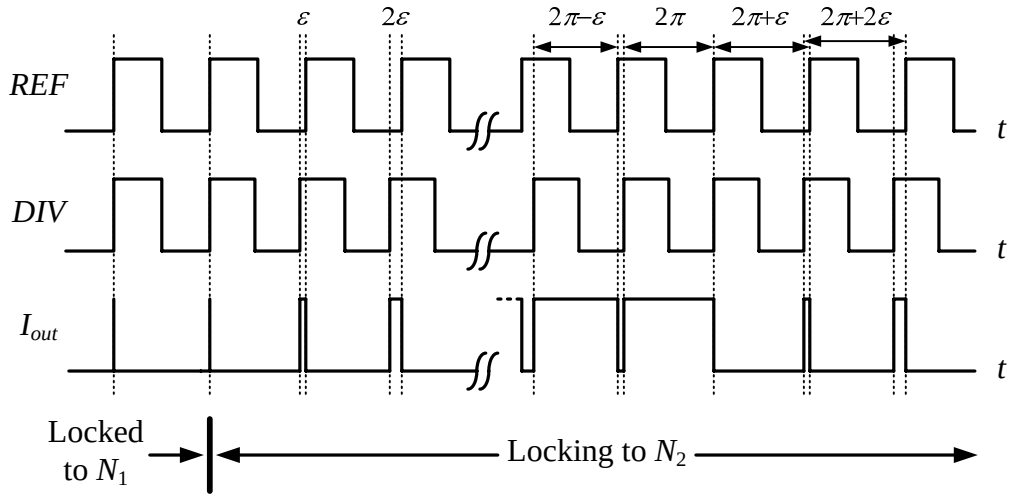


Figure 2.20: Timing diagram of REF and DIV (inputs to the PFD) and I_{out} (charge-pump output current) during cycle-slip, where ω_c is assumed to be infinitely large.

sometimes dominate the lock time. One common cause for this nonlinear response is the presence of so-called cycle-slips. Cycle slipping occurs when the phase error grows faster than the loop can correct for. Recall that the charge-pump current is pulse-width modulated as a function of the phase error. Thus, this translates to a growing charge-pump current duty-cycle. Eventually, as the phase error grows beyond 2π, the charge-pump current duty cycle drops from being near 100% to something very small, as shown in Fig. 2.20. This behavior is consistent with Fig. 2.13, which shows that the average output current drops to 0 as the phase error crosses over 2π radians (and every following increments of 2π thereafter). Although the polarity of the phase error (and charge pump current) is still correct, the large change in duty cycle disturbs V_{tune} as it reaches for its target, and in many cases, results in a momentary dip in the wrong direction. Since it is caused by the accumulation of phase error, this behavior is particularly

prevalent for large frequency jumps and/or when the loop bandwidth is very small compared to the reference frequency. This can be understood by considering the fact that a cycle-slip occurs every time the phase error has accumulated by 2π radians. Thus, assuming $F_c \ll F_{ref}$ the frequency at which cycle-slips occur may be approximated as:

$$F_{CS} \approx F_{ref} \left| \frac{\Delta F_o}{F_o} \right| \tag{2.36}$$

where F_o is the initial output frequency and ΔF_o is the frequency step and is related to the phase error ε shown in Fig. 2.20 by $\varepsilon = 2\pi|N_2 - N_1|/N_1 = 2\pi|\Delta F_o/F_o|$. The frequency given by (2.36) will gradually slow down as the feedback loop begins to correct for the phase error. Eventually, the phase error ceases to accumulate beyond 2π and the linear settling behavior described earlier takes over. Fig. 2.21 illustrates the locking process for two different settings of F_{ref} and $\Delta F_o/F_o \approx 3\%$ [29]. In the case where F_{ref} is on the order of $100F_c$, no cycle slips are observed, whereas for the case where F_{ref} is on the order of $1000F_c$, the settling response cycle-slips for a significant portion of the time.

2.5 Noise in PLLs

Due to the small-signal nature of typical noise contributors, the linear continuous-time PLL model introduced in Section 2.4 is particularly well-suited for noise analysis. While this model only captures the steady-state behavior, the unlocked noise performance is typically not relevant. Fig. 2.22(a) illustrates the PLL linear phase-domain

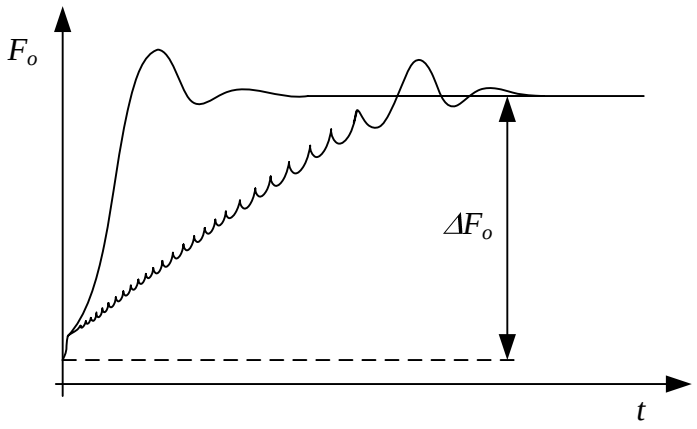


Figure 2.21: Typical locking response with and without cycle-slipping.

noise model, showing its various contributors. As shown in Fig. 2.22(b), the different noise sources may be referred to the input or output of the PLL to ease the derivation of each individual transfer function to the output phase noise $\phi_o(s)$. Thus, we see that all input-referred noise sources (ϕ_{ref}, ϕ_{div}, and ϕ_{pd}) adopt a straightforward low-pass transfer function, namely $H(s)$, scaled accordingly. On the other hand, the output-referred noise sources are shaped by a high-pass transfer function $1/(1+T(s))$, where $T(s) = I_{cp}K_vZ_l(s)/sN$. For the loop filter output voltage noise, a band-pass characteristic results since the high-pass transfer function is combined with the K_v/s term. Table 2.1 lists each contributor and its corresponding equivalent input- or output-referred noise source, along with its resulting transfer function to the output phase noise.

From the above transfer functions, the total output phase noise (single-sided) power

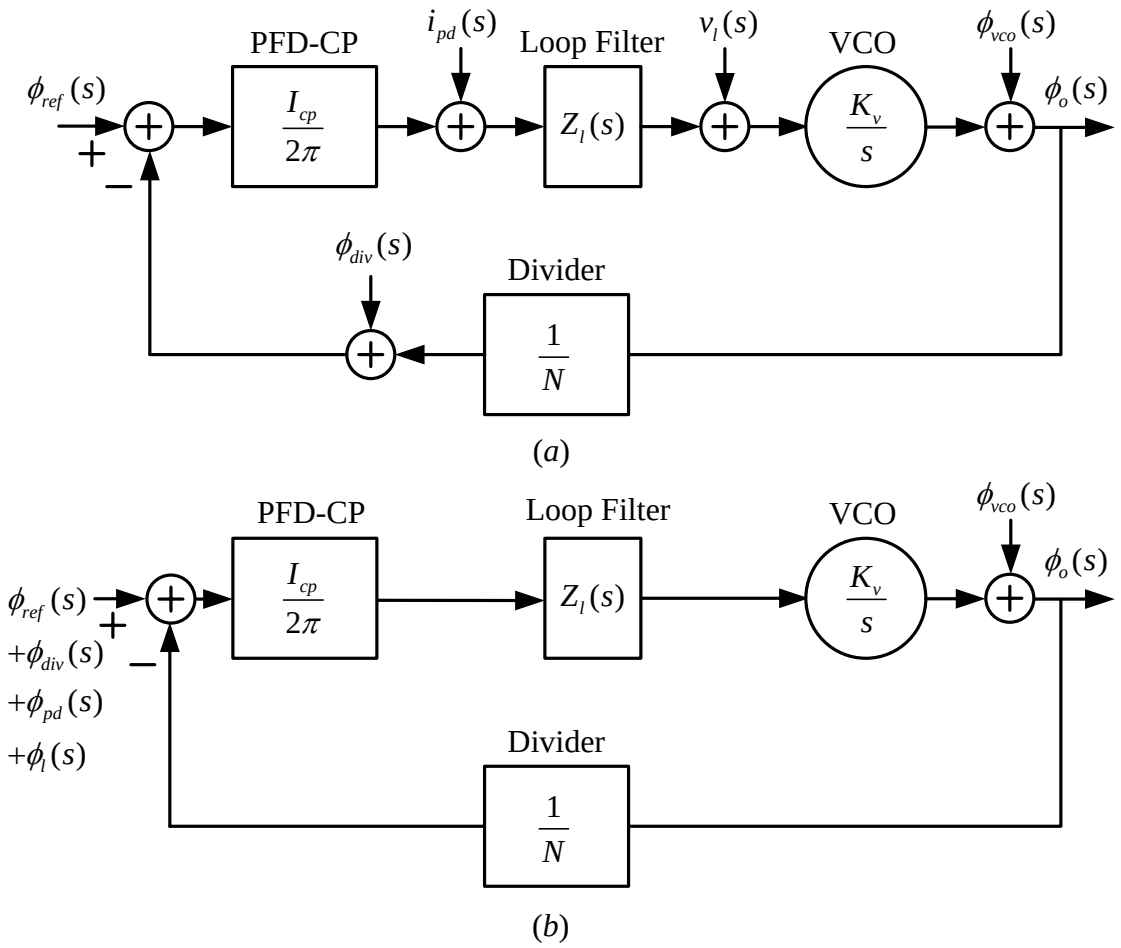


Figure 2.22: PLL linear noise model (a), and equivalent model with input- and output-referred noise sources (b).

Table 2.1: PLL Noise Sources

Equivalent Noise Generator	Transfer Function to Output Phase Noise	Description
$\phi_{ref}(s)$	$N \cdot H(s)$	Reference (input) noise
$\phi_{div}(s)$	$N \cdot H(s)$	Input-referred divider noise
$\phi_{pd}(s) = \frac{i_{cp}(s)}{I_{cp}}$	$N \cdot H(s)$	Input-referred chargepump noise
$\phi_l(s) = \frac{v_l(s)}{I_{cp}Z_l(s)}$	$N \cdot H(s)$	Input-referred loop filter noise
$\phi_{vco}(s)$	$1/(1+T(s))$	Output-referred VCO noise

spectral density may be evaluated as follows

$$\begin{aligned} S_\phi(f) &= \sum_i \cdot \left|H_i^2(f)\right| \\ &= \left(\phi_{ref}^2 + \phi_{div}^2\right) \cdot N^2 \left|H(2\pi f)\right|^2 \\ &+ i_{cp}^2 \cdot \left(\frac{N}{I_{cp}}\right)^2 \left|H(2\pi f)\right|^2 \\ &+ v_l^2 \cdot \left(\frac{N}{I_{cp}}\right)^2 \left|\frac{H(2\pi f)}{Z_l(2\pi f)}\right|^2 \\ &+ \phi_{vco}^2 \cdot \left|\frac{1}{1+T(2\pi f)}\right|^2 \end{aligned} \tag{2.37}$$

From which the phase noise in dBc/Hz can be readily obtained using (2.8). Considering the transfer functions listed in Table 2.1, it can be concluded that the out-of-band phase noise ($f > F_c$) is dominated by the VCO noise, whereas the in-band phase noise is dominated by the other contributors. Fig. 2.23 illustrates a typical PLL phase noise plot showing the individual contributions from each noise component. Remarkably, all noise transfer functions, except for that from the VCO, are proportional to N. Hence, lowering N is preferable in terms of noise performance. For given channel specifications, reducing N typically involves architectural changes, which are discussed in Section 2.6. In practice, the in-band ($f \leq F_c$) phase noise is dominated by the reference, charge-pump, and loop filter noise. Since their contribution is inversely proportional to I_{cp}, increasing the charge-pump current reduces the in-band noise. Even if the charge-pump current noise power spectral density is itself proportional to I_{cp}, the overall output noise power spectral density still improves proportionally with I_{cp}. For a given loop bandwidth, increasing I_{cp} means that another component of the loop gain must be

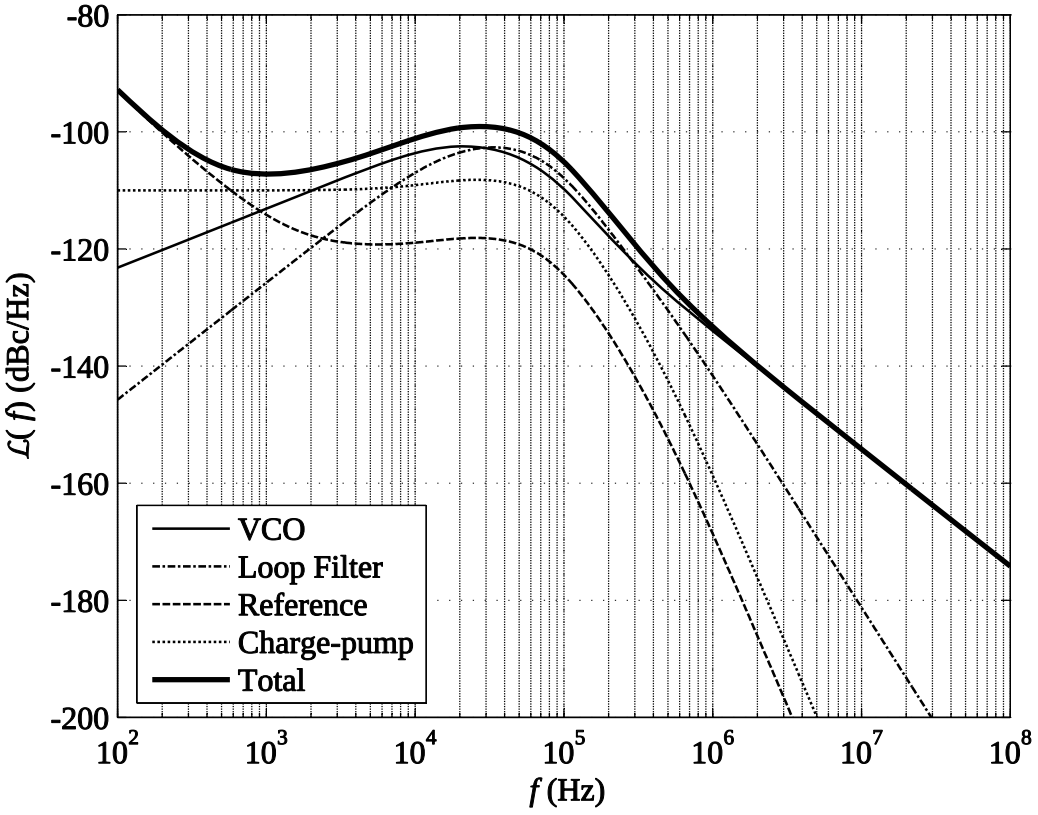


Figure 2.23: Typical PLL noise.

correspondingly decreased to keep K_o unchanged (see (2.23)). Assuming that N cannot be altered, reducing K_v is then the only way to sustain K_o. Furthermore, reducing K_v brings other benefits in terms of reduced sensitivity to parasitic-coupled contaminants (e.g. spurs, power supply noise, etc.). While highly desirable, the ability to reduce K_v may not be available for the particular VCO topology at hand.

2.6 PLL Frequency Synthesizer Architectures

Although above discussions encompass fairly general aspects of PLL operation, the most significant performance improvements are often achieved at the architecture level. This section provides a brief introduction to four commonly used architectures, although many others exist.

2.6.1 Integer-N PLL Synthesizer

The Integer-N architecture is characterized by an integer modulus divider that remains constant during steady-state operation. Its system block diagram follows the same topology as that shown in Fig. 2.1. Because the modulus is restricted to integer values, N and F_{ref} are set by channel specifications. In other words, F_{ref} itself represents the achievable frequency resolution. As discussed earlier, the loop bandwidth should not exceed $F_{ref}/10$. This imposes a hard limit on the achievable lock-time and may rule out this architecture for applications with relatively fast lock-time require-

ments. Furthermore, as F_c is brought closer to $F_{ref}/10$, the degree of reference spur rejection may decrease to unacceptable levels. Even for relaxed lock-time specifications where the loop can be made very slow, the relatively large N value in combination with the narrow loop bandwidth may cause excessive levels of phase noise at low frequency offsets. Nevertheless, its performance is easily evaluated against a given set of specifications. If its performance is determined adequate, the Integer-N architecture is typically the best choice due to its simplicity.

In summary, the Integer-N architecture offers simple and robust operation at the expense of a tightly coupled speed-resolution tradeoff. For systems with narrow channel spacing, its benefits must be weighted against its potentially poor performance in terms of lock time, phase noise, and reference spurs.

2.6.2 Fractional-N PLL Synthesizer

The main motive behind the Fractional-N architecture is to break the speed-resolution tradeoff inherent to the Integer-N PLL. As its name implies, the modulus is allowed to take on fractional values. As a result, the resolution is no longer set by F_{ref}. Thus, F_{ref} and F_c can be increased much beyond that of the Integer-N PLL. Since the settling time is (to first order) inversely proportional to F_c, Fractional-N PLLs typically lock much faster. Furthermore, a higher reference frequency translates to a proportionally smaller modulus, which significantly improves the in-band phase noise. As before, its system block diagram follows the same topology as that shown in Fig. 2.1. However,

its divider modulus is given by

$$N_{avg} = N_{int} + N_{frac} \tag{2.38}$$

The divide ratio is given as an average value because it is achieved by interpolating between integers, which results in a fractional number on a time-average basis. This functionality can be achieved using a digital k-bit accumulator and Fig. 2.24 shows a typical Fractional-N PLL configuration. D is a k-bit word representing the scaled decimal part of N_{avg}. The accumulator generates a carry-out bit D times out of every 2^k cycles of F_{div}. Thus, if the carry-out bit is used to toggle between $N_{int}+1$ and N_{int}, the divider will divide by $(N_{int}+1)$ D times and by N_{int} $(2^k - D)$ times over of a 2^k cycles interval, giving:

$$\begin{aligned} N_{avg} &= \frac{D(N_{int}+1) + (2^k - D)N_{int}}{2^k} \\ &= N_{int} + D/2^k \end{aligned} \tag{2.39}$$

Due to its very small hardware overhead (only one adder and one register are needed) relative to an Integer-N topology, the Fractional-N architecture seems to share a comparable level of simplicity. However, one major drawback has yet to be discussed. Due to the cyclical nature of the interpolative toggling between different modulus values, spurs are introduced at a fraction of the reference frequency. This is best understood by observing the phase error $\theta_{err} = \theta_{ref} - \theta_{div}$, as illustrated in Fig. 2.25 where the periodicity of $1/(N_{frac}F_{ref})$ has been annotated.

Although F_{ref} may be far above F_c, such fractional spurs may fall well within the

loop bandwidth. While some applications may tolerate such spurs, many wireless applications do not. The most common method to deal with this issue is to provide a compensation current at the charge pump output based on the accumulator output. A simplified block diagram of this architecture is illustrated in Fig. 2.26. In fact, the content of the accumulator can be shown to be a scaled replica of θ_{err}, on any given clock cycle. Ideally, the compensation current exactly cancels the phase error. However, the pulse-width modulated nature of the phase error makes a complete cancellation difficult. Furthermore, random and systematic device mismatch, as well as process and temperature variations, limit the overall compensation accuracy to no better than -60–70dB in practice [12,31]. Finally, we conclude by noting that although methods exist to combat fractional spurs and essentially salvage the main benefits of Fractional-N PLLs, the degree of design complexity has been raised significantly as a result. Nevertheless, compensated Fractional-N PLLs have successfully been used in a variety of high-end frequency synthesis products [12].

2.6.3 $\Sigma\Delta$ Fractional-N PLL Synthesizer

The presence of fractional spurs and the difficulty in suppressing them make the Fractional-N PLL architecture a lot less attractive. Since fractional spurs appear due the periodic operation of the accumulator, randomizing this process can theoretically prevent it. A $\Sigma\Delta$ Fractional-N PLL is based on the same architecture as the classical Fractional-N PLL with the addition of a $\Sigma\Delta$ modulator controlling the divide ratio, as

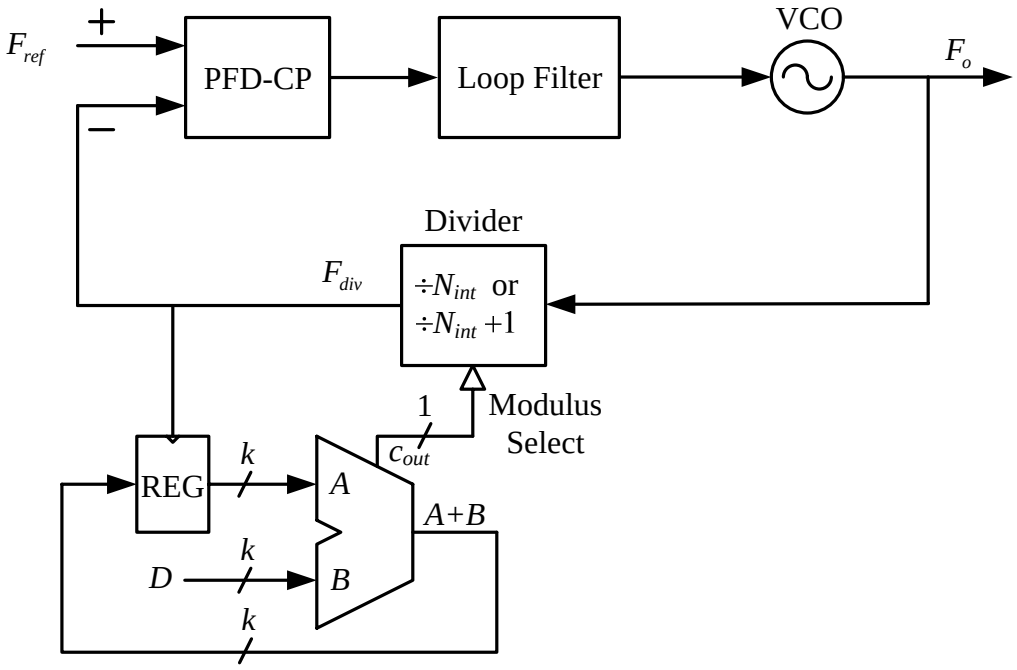


Figure 2.24: Basic Fractional-N PLL showing digital k–bit accumulator.

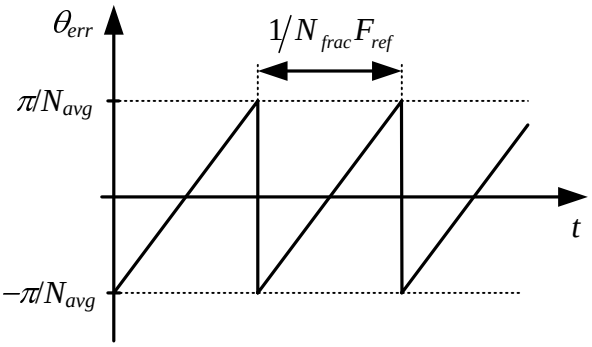


Figure 2.25: Phase error in Fractional-N PLL.

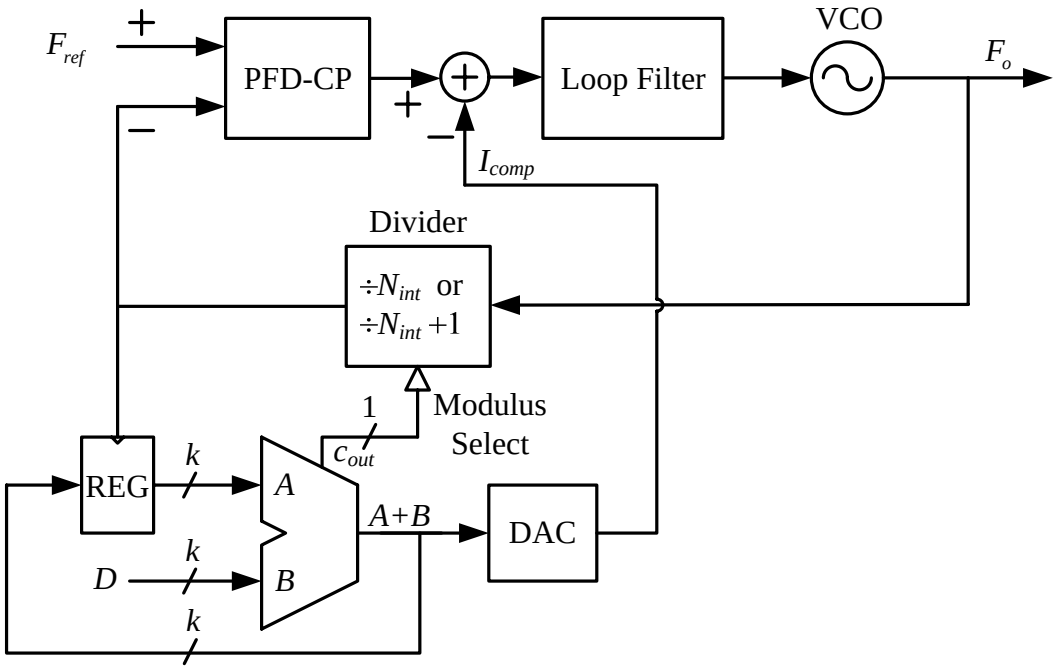


Figure 2.26: Fractional-N PLL with phase error compensation.

shown in Fig. 2.27. On a time-average basis, a $\Sigma\Delta$ modulator provides the same output as the accumulator, a well defined fractional part between 0 and 1. Thus, for a k-bit wide modulator with input word D, its divide ratio is given by (2.39) as well. However, its pseudo-random dithered nature shapes its quantization error/noise such that most of it is pushed to high frequencies. The particular noise-shaping characteristic depends on the order and type of the modulator. Owing to its simplicity and unconditionally stable operation, the MASH structure is one of the most widely used modulator topology. Its quantization noise power spectral density in rad^2/Hz, referred to the output of the divider is given by [32]:

$$S_{\phi,\Sigma\Delta}(f) = \frac{F_{ref}}{12(N_{avg}f)^2}\left[2\sin\left(\frac{\pi f}{F_{ref}}\right)\right]^{2L} \tag{2.40}$$

where L is the order of the modulator. Considering (2.40), there is a clear tradeoff between low- and high-frequency quantization noise as a function of L. Increasing L pushes quantization noise away from low frequencies and gives a steeper noise shaping characteristic, thereby causing a substantial increase in the quantization noise as f increases towards $F_{ref}/2$. Since $S_{\phi,\Sigma\Delta}$ has the same transfer function to the output as the phase noise from the reference, its high-frequency components ($f > F_c$) are attenuated by the action of the loop.

The $\Sigma\Delta$ modulator introduces only a minor hardware overhead as it is made up of digital adders, registers, and gates, all of which operate at relatively low frequencies (i.e. F_{ref}), making its design trivial (unlike analog $\Sigma\Delta$ modulators). Despite its advantages, the $\Sigma\Delta$ Fractional-N PLL still suffers from fractional spurs and quantization noise from

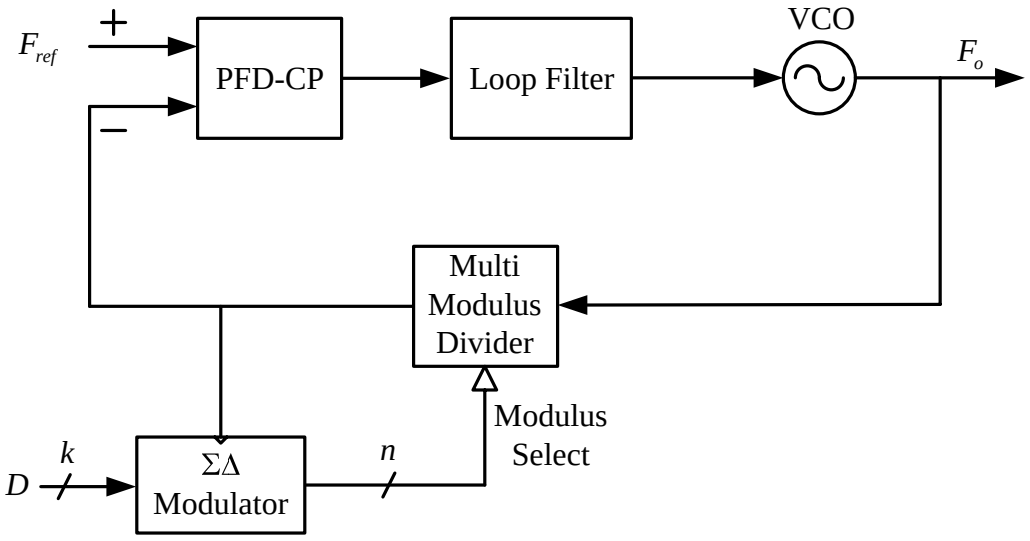


Figure 2.27: ΣΔ Fractional-N PLL Synthesizer.

the modulator. Limit cycles inherent in the operation of the modulator introduce fractional spurs, especially when N_{frac} is set to a rational fraction [32]. And nonlinearities in the building blocks of the PLL tend to fold the high-frequency quantization noise in-band, where the loop is not able to suppress it. Here as well, many techniques have been devised to cope with these issues achieving varying degrees of success.

2.6.4 Dual-Loop PLL Synthesizer

Another way to break the speed-resolution tradeoff of the Integer-N PLL is by interfacing multiple PLLs. As its name implies, this configuration uses one additional PLL. Fig. 2.28 shows one implementation of the dual-loop architecture [33], although many other arrangements exist. As illustrated in Fig. 2.28, the functionality of this

dual-loop configuration is achieved by mixing the VCO output of a main PLL (PLL1) with that of a second slower PLL (PLL2), and feeding the (low-pass filtered) output to the divider. As a result, its output frequency is given by

$$F_o = N_1 F_{ref,1} + N_2 F_{ref,2} \tag{2.41}$$

Thus, this configuration achieves a frequency resolution of $F_{ref,2}$ (it is assumed that $F_{ref,2} < F_{ref,1}$), whereby varying N_2 produces the desired frequency steps (in increments of $F_{ref,2}$). Note however, that the extent to which $F_{ref,2}$ can be reduced is limited by the settling time specification. As a compromise, $F_{ref,2}$ can be increased (to meet settling time specifications) and the output of PLL2 divided down proportionally, before feeding the mixer in the main loop [34]. In terms of phase noise, the dual-loop typically provides superior performance relative to the Integer-N configuration. Because of its low divider ratio and high loop bandwidth, PLL1 can achieve very good phase noise performance (similar to what is obtained with a Fractional-N). Typically, the phase noise contributed from PLL2 does not degrade the overall noise significantly [22]. The main drawback of the dual-loop configuration is its heavy overhead in terms of hardware (i.e. die area) and power consumption. Furthermore, the level of design complexity is drastically increased, although its larger number of degrees of freedom translates to a more flexible optimization process.

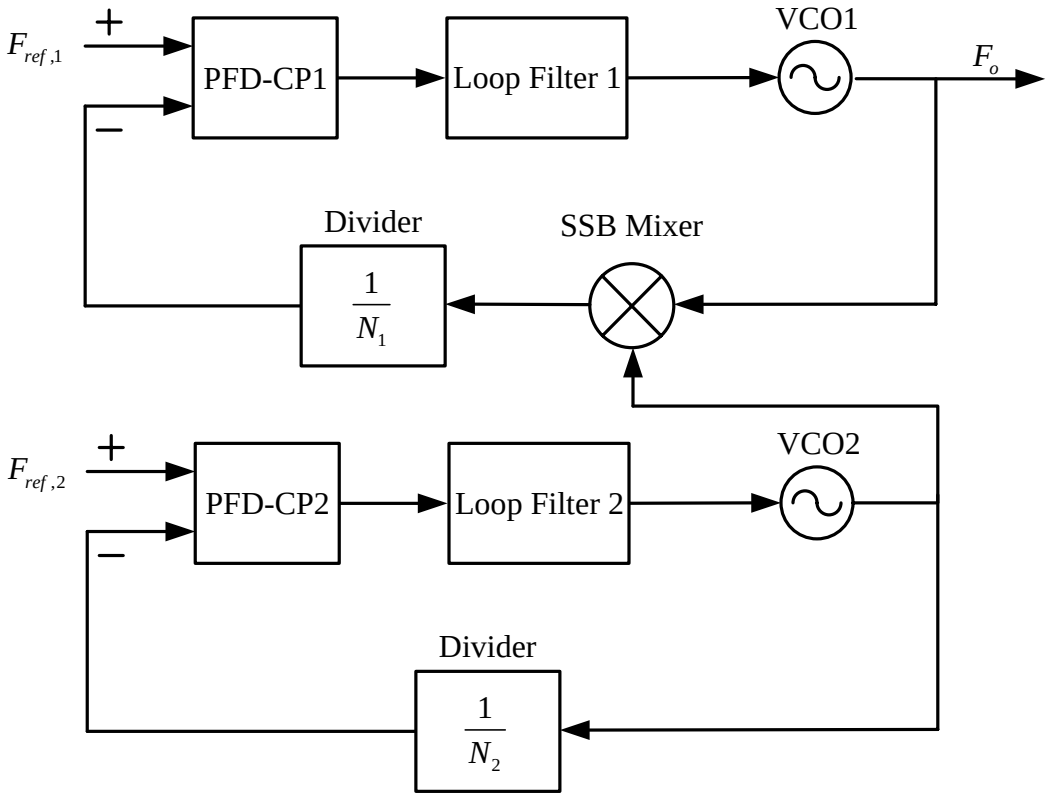


Figure 2.28: Example of a dual-loop PLL.

Chapter 3

LC VCO Fundamentals

3.1 Fundamental Oscillator Characteristics

In its most basic form, an oscillator is an autonomous circuit that generates a stable periodic output by some self-sustaining mechanism. This is generally achieved by providing the system with an appropriate amount of positive feedback, or negative resistance, such that any loss is compensated and the oscillation can be sustained.

A basic requirement to ensure oscillation start-up is the presence of at least one pair of complex conjugate poles in the right-half plane (RHP) in the system transfer function:

$$p_{1,2} = \alpha \pm j\beta \tag{3.1}$$

This requirement is necessary but not sufficient to ensure steady-state oscillation. A system with poles as in (3.1) exhibits an exponentially growing sinusoidal response when

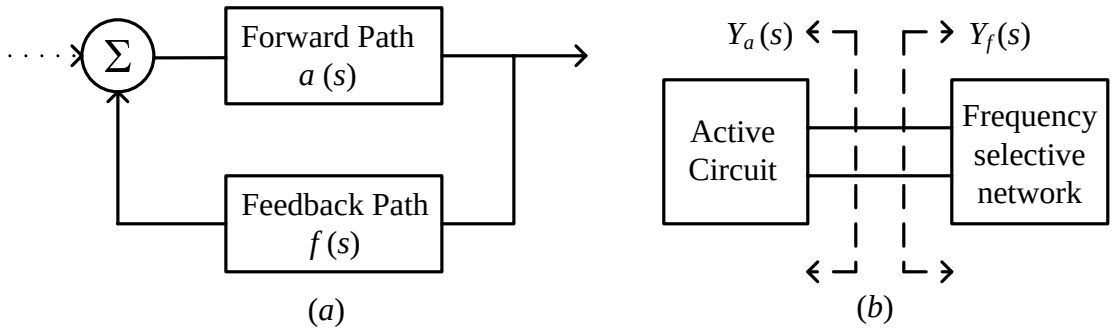


Figure 3.1: (a) Feedback model. (b) Negative-resistance model.

subjected to an excitation, such as power supply turn-on transients or any source of electronic noise:

$$x(t) = A \cdot e^{\alpha t} \cdot \cos \beta t \tag{3.2}$$

where A is determined by initial conditions. The above exponential behavior governs the beginning of oscillation build up. This rapid signal growth eventually drives the system into a nonlinear regime that ultimately reaches a steady-state mode of operation.

Oscillation start-up criteria may be analyzed using a two-port linear feedback approach, or a one-port negative-resistance approach. Though equivalent, each approach has its advantages, and one may be preferred over the other depending on the topology at hand. When considering an oscillator as a linear feedback system, as in Fig. 3.1, the loop-gain must fulfill the following necessary (but not sufficient) conditions in order to ensure start-up:

$$\angle T(j\omega_y) = 0, \quad |T(j\omega_y)| > 1 \tag{3.3}$$

where ω_y is the frequency at which the total phase shift through the forward and feedback paths is zero. As shown in Fig. 3.1, an oscillator analyzed using the negative-resistance model can be broken up into two one-port networks: an active circuit and a frequency selective circuit, modeled by admittances $Y_a = G_a + jB_a$ and $Y_f = G_f + jB_f$, respectively. The following start-up criteria have been widely used to ensure instability [35]:

$$G_a(\omega_x) + G_f(\omega_x) < 0 \tag{3.4a}$$

$$B_a(\omega_x) + B_f(\omega_x) = 0 \tag{3.4b}$$

where ω_x is the frequency at which the sum of all reactive components equals zero. It is important to note that the conditions in (3.3) and (3.4) are necessary but not sufficient to ensure oscillation start-up. Oscillatory behavior may not be sustained in situations where these conditions are met at more than one frequency [35]. The exponential signal growth described by (3.2) eventually drives the system out of the linear regime and into a large-signal steady-state mode of operation. During this nonlinear transition, the poles described by (3.1) shift such that the oscillator is brought to steady-state where the following condition is met:

$$\angle T_{osc}(j\omega_o, A_o) = 0, \quad |T_{osc}(j\omega_o, A_o)| = 1 \tag{3.5}$$

where ω_o is the steady-state oscillation frequency, and is typically very close to but not exactly equal to ω_y in (3.3); and where the dependence on oscillation amplitude, A_o, has been made explicit for the phase and magnitude of the loop. The conditions in

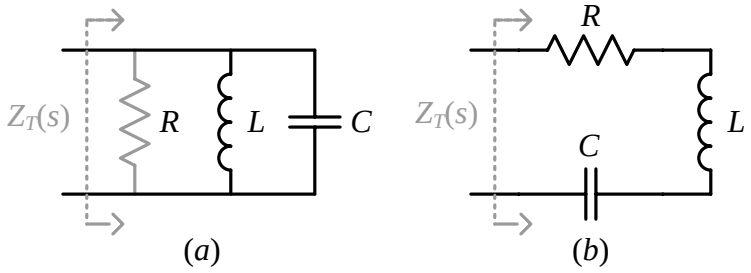


Figure 3.2: (a) Parallel LC tank. (b) Series LC tank.

(3.5) can be analogously expressed using the negative-resistance point of view [36]:

$$G_a(\omega_o, A_o) + G_f(\omega_o) = 0 \tag{3.6a}$$

$$B_a(\omega_o, A_o) + B_f(\omega_o) = 0 \tag{3.6b}$$

where ω_o is typically very close to but not exactly equal to ω_x in (3.4).

3.2 LC Tanks

3.2.1 Basic RLC networks

LC resonators, also referred as LC tanks, are made up of an inductor and a capacitor connected in series or in parallel. One or more resistive components modeling the resonator losses are generally included. Thus, in the simplest case, LC tanks are represented as series or parallel RLC networks. These simplified networks are shown in Fig. 3.2. Practical LC tanks contain additional reactive and resistive components, and cannot generally be condensed to the configurations of Fig. 3.2. However, these

simplified RLC representations provide good insight and are usually adequate during the initial design stages where rough estimates of performance are sufficient. The tank impedances of the networks shown in Fig. 3.2 are:

$$Z_T(j\omega) = \frac{1}{1/R + j \cdot (\omega C - 1/\omega L)} \qquad \text{(Parallel } RLC\text{)} \qquad (3.7a)$$

$$Z_T(j\omega) = R + j \cdot (\omega L - 1/\omega C) \qquad \text{(Series } RLC\text{)} \qquad (3.7b)$$

The reactive terms in (3.7) cancel out at one frequency, called the resonance frequency:

$$\omega_o = 1/\sqrt{LC} \qquad (3.8)$$

At ω_o, the tank impedance is purely resistive and is equal to R, and the phase of the impedance response is exactly zero. This is illustrated in Fig. 3.3. At frequencies below resonance, the tank impedance of the parallel RLC network is mainly inductive. Similarly, at frequencies above resonance, the tank impedance of the parallel RLC network is mainly capacitive. For series RLC networks, this scenario is exactly opposite. Hence, the parallel and series RLC are the dual of each other.

The resonator's quality factor, Q, embodies the various losses inherent to its elements and thus indicates its ability to retain energy. Q is a very important quantity because it often determines the phase noise performance of LC VCOs. In general, the Q of a network is defined as:

$$Q \equiv \omega \cdot \frac{\text{Energy stored}}{\text{Average power dissipated}} \qquad (3.9)$$

Q equivalently describes the steepness of $\angle Z_T(j\omega)$ near ω_o or the sharpness of the peak

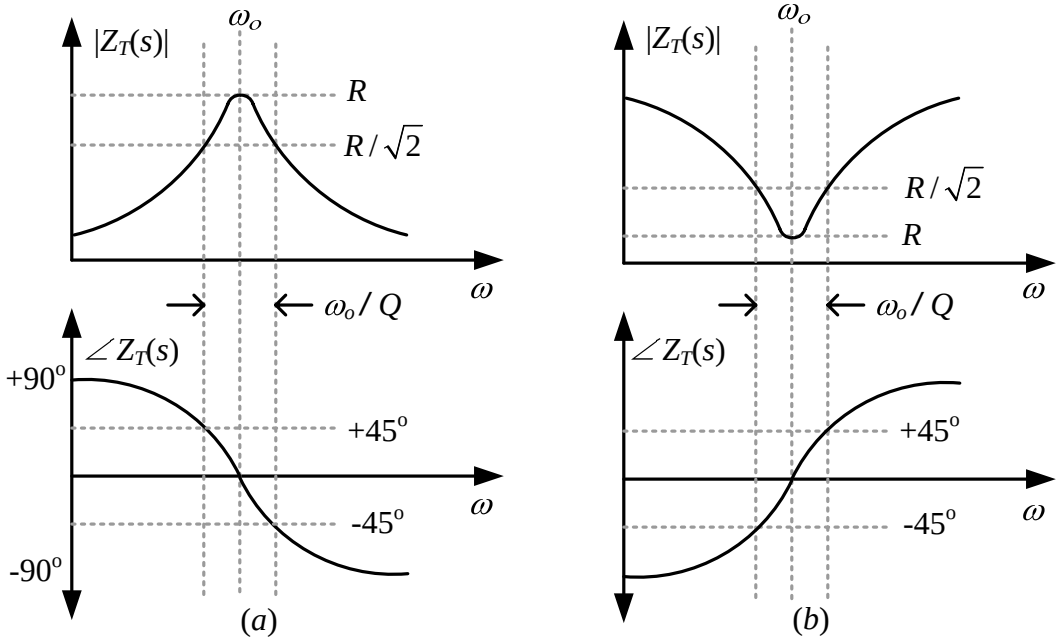


Figure 3.3: Magnitude and phase of LC tank impedance for Parallel (a) and Series (b) configurations.

at $|Z_T(j\omega_o)|$ (see Fig. 3.3). Hence, Q can alternatively be expressed as:

$$Q = \frac{\omega_o}{\Delta\omega_{-3\text{dB}}} \tag{3.10}$$

where $\Delta\omega_{-3\text{dB}}$ is the -3dB bandwidth of the impedance response. Clearly, a larger Q results in a sharper impedance response, and thus higher rejection of spectral energy away from the resonant frequency. This is the main reason why a higher resonator Q leads to more ideal oscillator output spectrum.

At resonance, the Q of the RLC networks shown in Fig. 3.2 is given by:

$$Q = \frac{R}{\omega_o L} = \omega_o RC \qquad \text{(Parallel } RLC\text{)} \tag{3.11a}$$

$$Q = \frac{\omega_o L}{R} = \frac{1}{\omega_o RC} \qquad \text{(Series } RLC\text{)} \tag{3.11b}$$

where the dual nature of series and parallel RLC networks is apparent. Using (3.11), we can rewrite (3.7) as:

$$Z_T(j\omega) = \frac{R}{1 + jQ\left(\omega/\omega_o - \omega_o/\omega\right)} \qquad \text{(Parallel } RLC\text{)} \tag{3.12a}$$

$$Z_T(j\omega) = R \cdot \left[1 + jQ\left(\omega/\omega_o - \omega_o/\omega\right)\right] \qquad \text{(Series } RLC\text{)} \tag{3.12b}$$

3.2.2 Integrated Spiral Inductors

IC Technologies have traditionally not been well-suited for realizing good quality inductors. This is mainly because the loops through which magnetic flux is established are small and are built using relatively lossy conductors. While typical metallization is sufficiently conductive for most chip interconnections, the long wires needed to produce sufficient inductance accumulate correspondingly large resistive losses. As a result of needing large loops, on-chip inductors also have poor area efficiencies, compared to capacitors and resistors. Nevertheless, the sustained cost-driven pressures to eliminate off-chip components have made on-chip inductors ubiquitous in RF transceivers. Hence, integrated inductor analysis, design, modeling, and optimization have been very active subjects of research in the last 15 years [37–41]. This section will provide a brief overview of some the design tradeoffs and modeling approaches.

As shown in Fig. 3.4, typical on-chip spiral inductor structures consist of multiple square, octagonal, or circular spiraling turns forming its coils. The top metal layer is generally preferred for its lower parasitic capacitance to the substrate, and thus higher self-resonance frequency (above which the inductor is not useful). Furthermore, the

top metal layer often benefits from a larger thickness than lower metal layers which helps reduce resistive losses. The choice of geometry is mainly based on loss and area efficiency considerations. Square spirals offer the densest inductance per area compared to octagonal or circular spiral, where area means the smallest rectangular area enclosing the structure (corner areas enclosing a spiral amount to wasted space in practice). On the other hand, circular spirals provide higher Q [42]. When foundry design rules or CAD tools do not support circular shapes, octagonal spirals are used as the next best alternative. For a given inductor area, the inductance may be increased by simply filling in more turns until the entire space is occupied. However, loss constraints typically prohibit this approach as inner turns contribute little inductance and add significant loss. Thus, spiral inductors are rarely filled to their maximum number of turns, and increasing the inductance is typically achieved by increasing the coil radius. One way of increasing the inductance without incurring an area penalty is to connect additional turns (of similar dimensions) on other metal layers in series. One penalty of this approach is that the use of lower metal layers (closer to the substrate) brings down the self-resonance of the inductor. A widely used method of improving Q is to connect multiple metal layers in parallel thereby reducing the series resistance of the coil. Again, this technique effectively brings the coil closer to the substrate, which lowers its self-resonance. Though in many cases, this tradeoff is welcome.

Another popular technique which provides many benefits is to use a differential structure, as shown in Fig. 3.5. In differential circuits that would otherwise use two

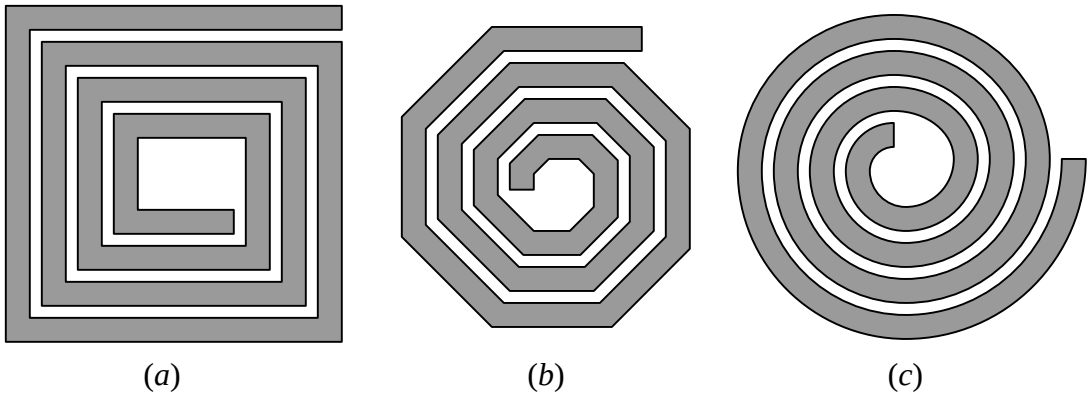


Figure 3.4: Typical integrated inductors: (a) square, (b) octagonal, and (c) circular spirals.

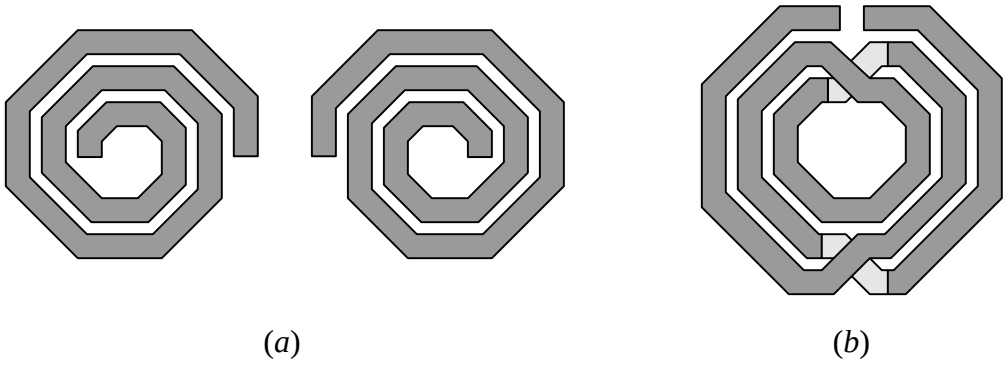


Figure 3.5: A pair of single-ended inductors (a) and a differential inductor (b) with similar total inductance.

single-ended inductors, using a single differential inductor of twice the inductance results in a much more compact layout. In addition, the differential structure suppresses common- or even-mode capacitive parasitics and associated losses [43]. These benefits can improve the self-resonance frequency and quality factor, which has made this configuration very popular.

So far, our discussion has mainly alluded to losses in terms of the series dc resis-

tance of the coil. While this is indeed the dominant loss contributor at low frequencies (<1GHz), other loss mechanisms become significant at higher frequencies and amount to a much more complicated picture. First of all, the series resistance itself is frequency-dependent and rises considerably as frequency increases, due to skin and proximity effects [39–41]. The skin depth of a good conductor is given by $\delta_s = \sqrt{\pi f \mu \sigma}$ and indicates that the current flowing inside the conductor is increasingly constricted to the surface as frequency increases. Proximity effects due to fields from adjacent turns result in a similar frequency-dependent non-uniform current distribution and corresponding loss increase. Secondly, image- or eddy-currents generated in the substrate flow in opposite direction to that of the coil. As a result, a magnetic field opposing that from the coil is generated and reduces the inductance. The flow of currents in the substrate also translates to additional losses which are a strong function of the substrate resistivity and become significant as frequency increases. These frequency-dependent trends can be seen in Figs. 3.6−3.8. Q initially rises linearly with frequency (see (3.11)) since the loss is dominated by the coil's dc series resistance. Eventually, skin and proximity effects as well as substrate losses come into the picture. Thus, Q gradually peaks to its maximal value, $Q_{\max}$, and beyond which it experiences a fast decline as f approaches the coil's self-resonance. Figs. 3.6−3.8 give some flavor for how various design and technology parameters affect the inductance and Q of a typical 3nH coil.

Due to their large physical dimensions (comparable to wavelengths of interest) and 3-dimensional electromagnetic (EM) field distributions, on-chip spiral inductors are dif-

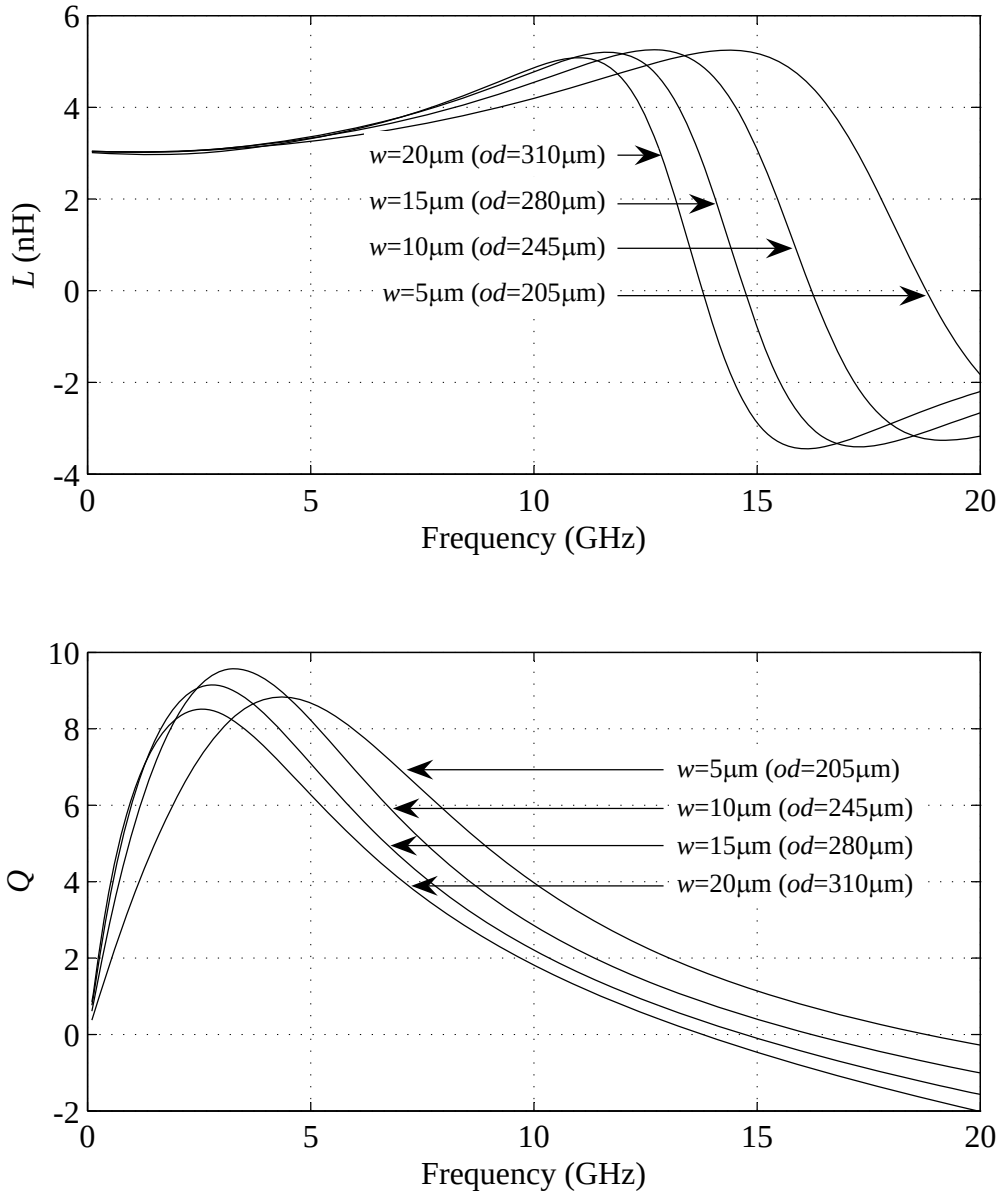


Figure 3.6: Q and L vs. f of 3nH inductor for different widths (w), and n =3, s = 4.5μm.

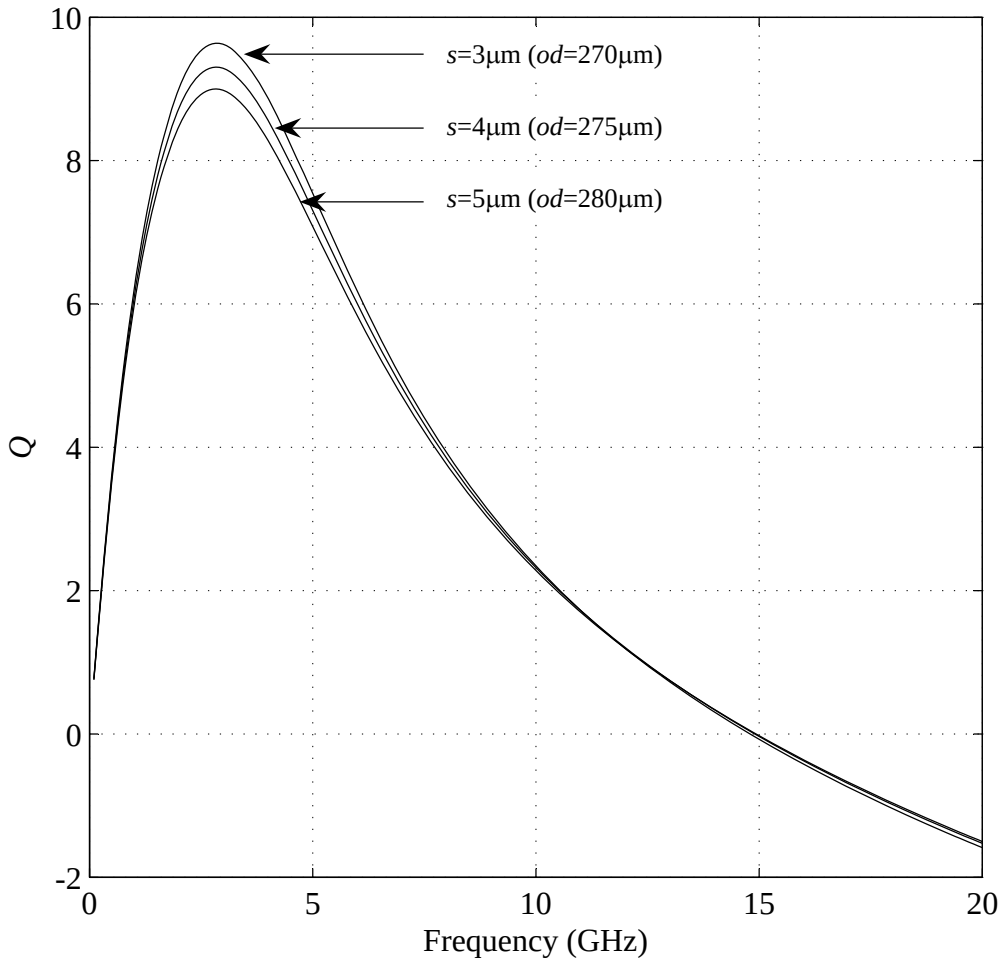


Figure 3.7: Q vs. f of 3nH inductor for different turn-turn spacing (s), and n =3, $w = 15\mu$m.

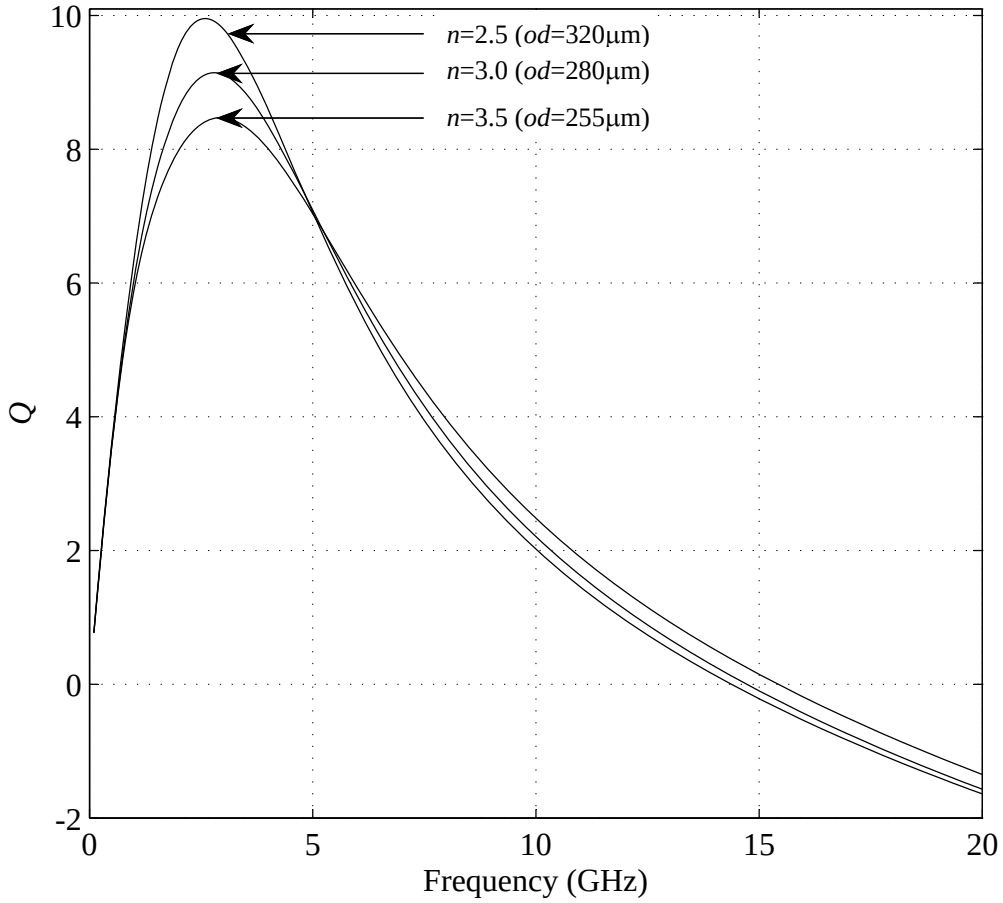


Figure 3.8: Q vs. f of 3nH inductor for different number of turns (n), and $w = 15\mu$m, $s = 4.5\mu$m.

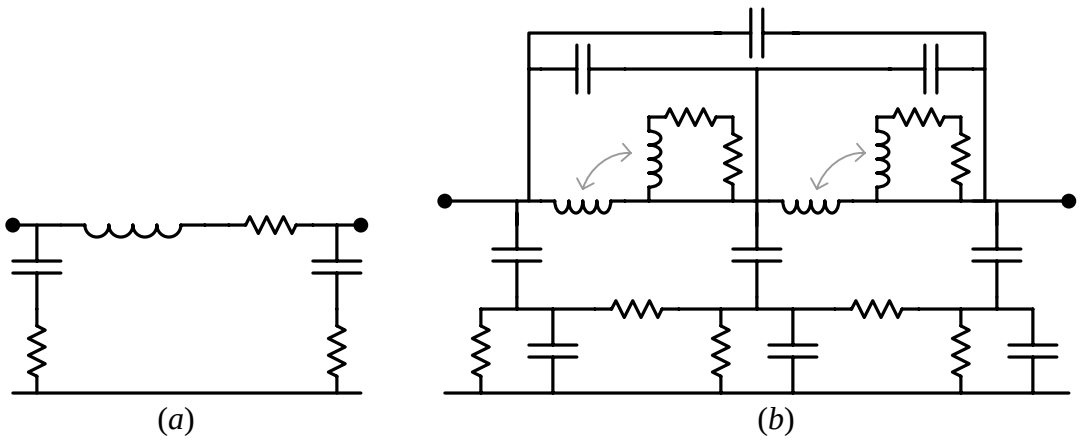


Figure 3.9: On-chip inductor models (a) pi-equivalent, (b) wideband lumped equivalent.

ficult to model accurately with simple lumped equivalent networks. However, the most accurate modeling approaches are also the most computationally consuming, and thus not convenient for analyses and derivations. Thus, the proper choice of inductor model depends on the application. Fig. 3.9 illustrates two common lumped equivalent networks with different degrees of complexity. The pi-equivalent network shown in Fig. 3.9(a) is derived at a frequency of interest. Hence, it is a narrowband model only valid in the close vicinity of that particular frequency and is not suitable in wideband designs. Despite its limited validity, this model is very popular in hand-analyses of resonant circuits. The network shown in Fig. 3.9(b) approximates the frequency dependence of the most important characteristics of the coil using an expanded lumped equivalent network. As a result, its validity holds over a much wider frequency range and it is better suited for wideband design analysis.

3.2.3 Integrated Capacitors

Capacitors can be realized in any IC process. RF designs tend to stay away from lossy polysilicon-based capacitors and use metal-plate capacitors instead. Many IC technologies provide a metal-insulator-metal (MIM) option that achieves high density (ranging from 1-2fF/μm^2), high Q (>100 at 1GHz), and low parasitic bottom plate capacitance (1% or less), as shown in Fig. 3.10(a). Its relatively high density is typically achieved using an ultra-thin layer of silicon nitride sandwiched by means of an intermediate metal layer. Hence it requires at least one additional mask. If not available, a different high-Q metal-metal capacitor can be built by combining metal fingers as densely as possible, as shown in Fig. 3.10(b). Although its matching properties and process tolerances tend to be worse than that of MIMs, its Q can be even better [44]. As technology scales and more metal layers are added to the metallization stack, its density tends to improve. Furthermore since no extra masks are needed, this capacitor is becoming a popular alternative to MIM capacitors.

Due to their relatively simple and compact geometry, MIM capacitors can be modeled by a trivial series RC network, where R represents the series loss from the finite resistance of the metal plates. The capacitance is determined from the parallel plates' area and separation and the type of dielectric. Metal finger capacitors can also be modeled by the same equivalent RC network. On the other hand, their capacitance is determined by combining multiple parallel and fringing terms. If significant, the parasitic bottom plate can be added as well. Likewise, the finite series lead inductance can

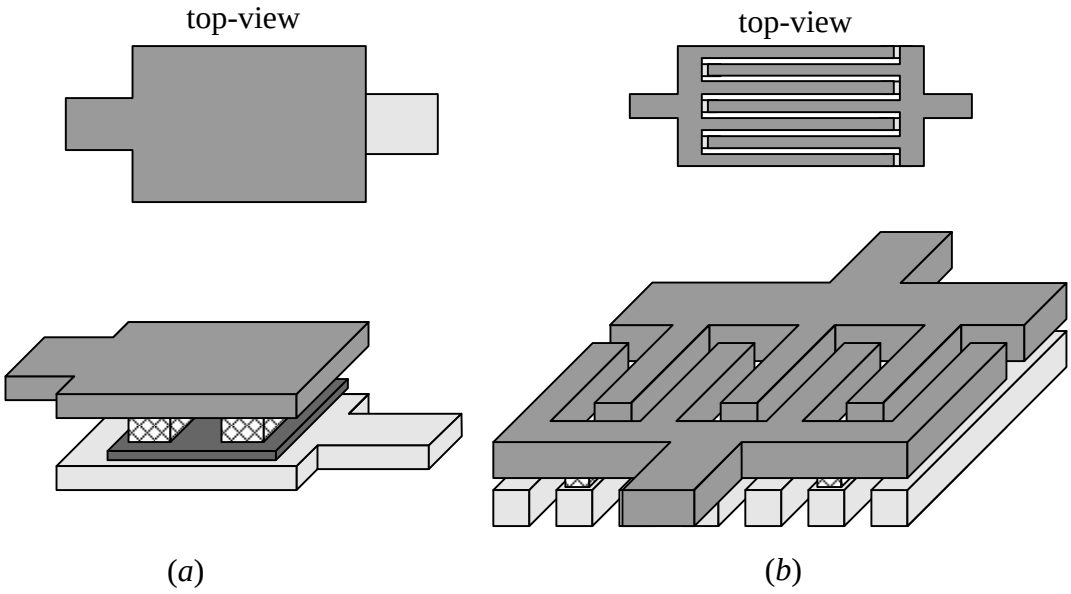


Figure 3.10: (*a*) MIM Capacitor. (*b*) Metal Finger Capacitor.

potentially affect the reactance at very high frequencies and should be modeled in those cases.

3.2.4 Integrated Varactors

In general, varactors can be implemented as reverse-biased *p*-*n* junctions. In CMOS technology, this can be accomplished using the available p^+/n^- diffusions and N- or P-Wells. Despite having a modest maximum-to-minimum capacitance ratio ($C_{\max}/C_{\min}$) that worsens as the supply voltage scales, *p*-*n* junction varactors are adequate for applications with limited tuning needs. With proper layout techniques, the achievable Q is usually good (>50 at 1GHz) as long as the junction is prevented from reaching its forward-biasing condition.

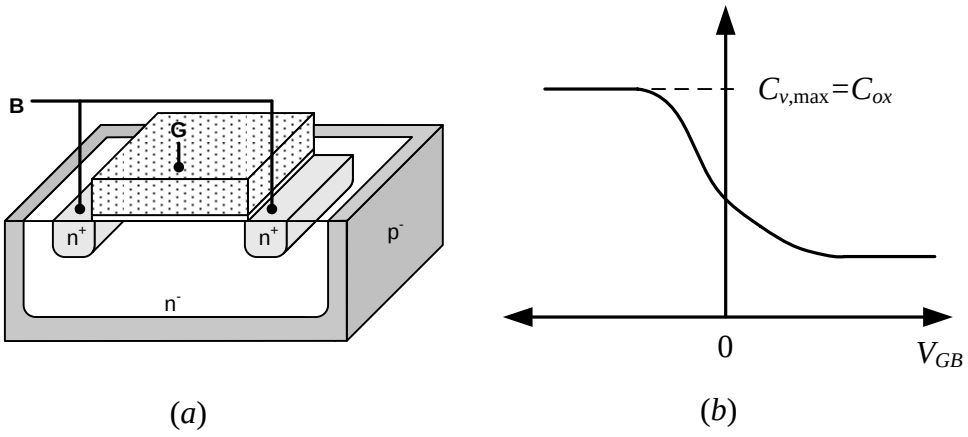


Figure 3.11: MOS varactor. (a) Physical structure. (b) C-V characteristic.

The MOSFET gate capacitance may also be used as a varactor. Its main advantage is an intrinsic $C_{\max}/C_{\min}$ that is much higher than that of p-n junction varactors [45]. Small-signal $C_{\max}/C_{\min}$ values of 2 to 5 can be achieved in practice, even with control voltage swings as small as 1V [46]. Furthermore, Q remains very good across the entire tuning range and improves with technology scaling. Inversion- and accumulation-mode are the most common varactor configurations. Because electrons are the majority carriers in the depletion and accumulation regions, the accumulation-mode device has less parasitic resistance than the inversion-mode device, which uses holes as majority carriers. Hence, accumulation-mode varactors tend to have higher Q [45, 46] and are generally the preferred device type. Its physical structure and C-V characteristic are shown in Fig. 3.11.

In VCOs, the output voltage swing may be as large as the supply voltage and all or a significant portion of it may appear across the varactor. In such cases, the effective (or

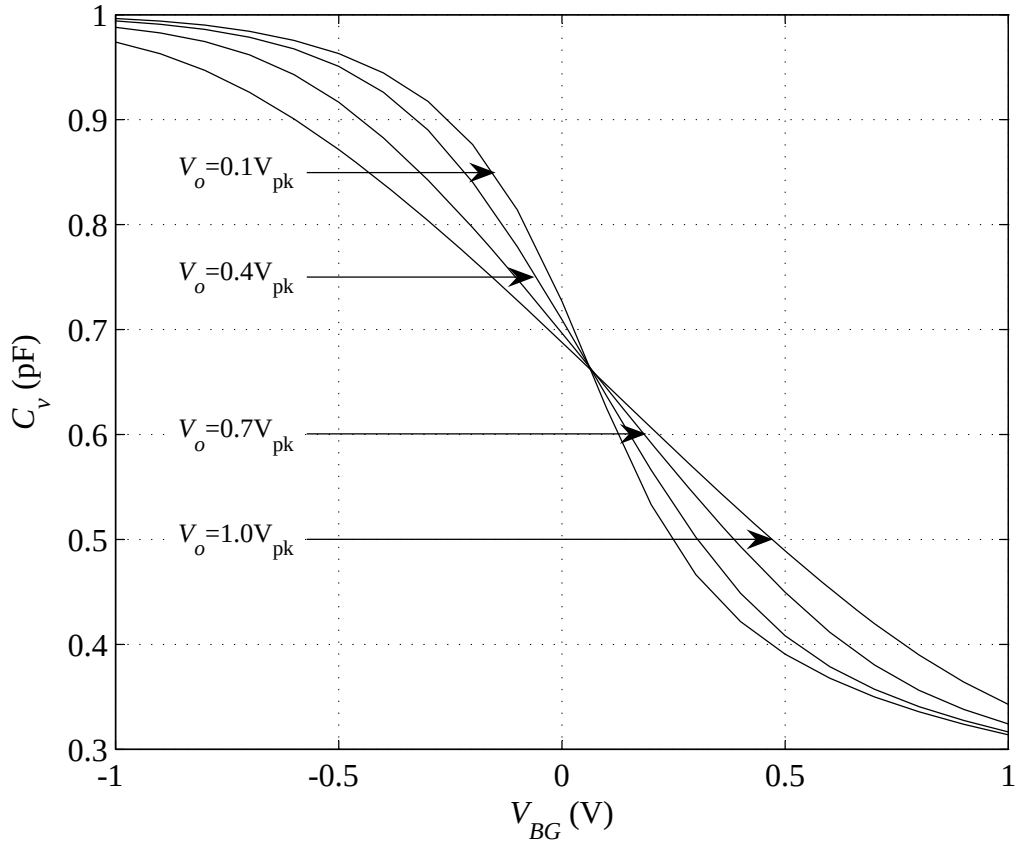


Figure 3.12: C-V characteristics for different V_o.

time-average) capacitance is no longer that given by the small-signal C-V curve depicted Fig. 3.11(b). Instead, a large-signal C-V curve may be determined by considering the periodically time-varying capacitance due to a large applied signal [47–49]. As shown in Fig. 3.12, large signal swings tend to make the C-V transition less steep and more linear.

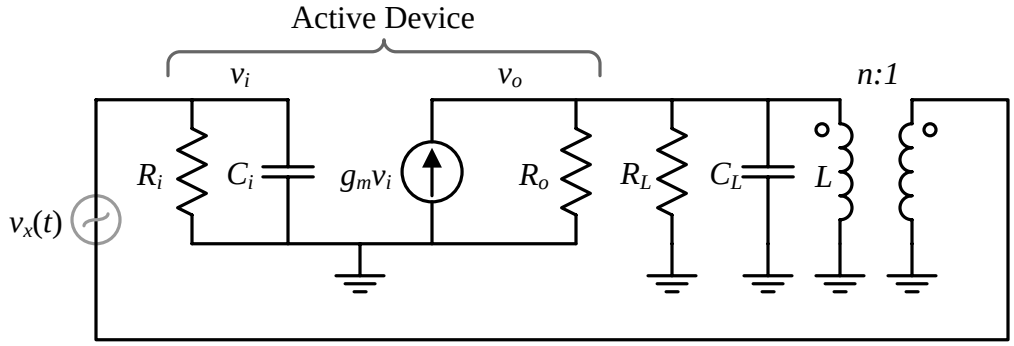


Figure 3.13: Generic small-signal LC oscillator schematic.

3.3 Start-up Considerations

As discussed earlier, a minimum amount of loop gain, or equivalently a minimum amount of negative resistance, is required to ensure start-up. Fig. 3.13 depicts a small-signal representation of a generalized LC oscillator valid during start-up (Fig. 3.13 assumes a unilateral device). The circuit shown in Fig. 3.13 has the following transfer function [50]:

$$\frac{v_o(s)}{v_i(s)} = \frac{s \cdot g_m L}{1 + sL/R_T \cdot (1 - A_l) + s^2 LC} \tag{3.13}$$

where $A_l = g_m R_T/n$,$R_T = R_o||R_L||n^2 R_i$, and $C = C_L + C_i/n^2$. The roots of the denominator of (3.13) are the poles of the transfer function and are given by:

$$s_1, s_2 = -\left(\frac{1 - A_l}{2R_T C}\right) \pm j\sqrt{\frac{1}{LC} - \left(\frac{1 - A_l}{2R_T C}\right)^2} \tag{3.14}$$

$$|s_1| = |s_2| = \sqrt{\frac{1}{LC}} = \omega_o \tag{3.15}$$

Equation (3.15) shows that the magnitude of the poles is entirely determined by the LC tank. Hence, poles s_1 and s_2 move in a perfect circle across the complex plane, as

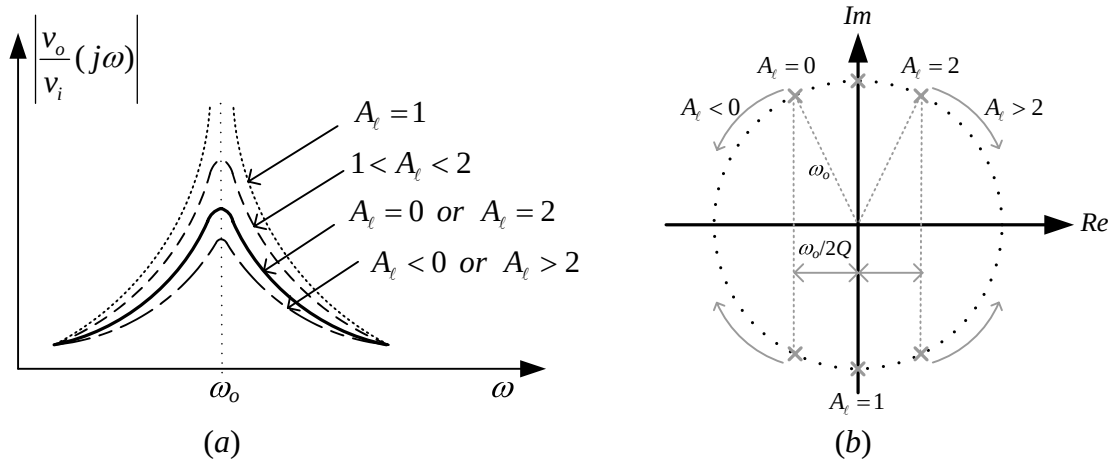


Figure 3.14: (a) Magnitude of transfer function for different values of loop gain. (b) Root locus of transfer function for different values of loop gain.

the loop gain (A_l) changes. Fig. 3.14 illustrates the effects of varying A_l.

To guarantee oscillation start-up at all operating temperatures and under worst-case process variations, practical designs are designed with A_l =3 to 5 under nominal conditions [50].

Although the approach taken above used linear feedback methods, an equivalent criterion may be reached using negative resistance concepts. The above analysis is also applicable to differential VCO topologies, which are very common in today's communication systems. Fig. 3.15 shows a widely used differential VCO topology, where start-up criteria are evaluated using both feedback and negative resistance approaches (see Section 3.1). In Fig. 3.15, R_a is the resistance looking into the differential cross-couple pair of active devices, R_f is the equivalent differential resistance of the frequency selective network (comprised of both LC tanks), R_T is the equivalent resistance of each LC tank, and g_m is the small-signal transconductance of either M_1 or M_2. Note that using either

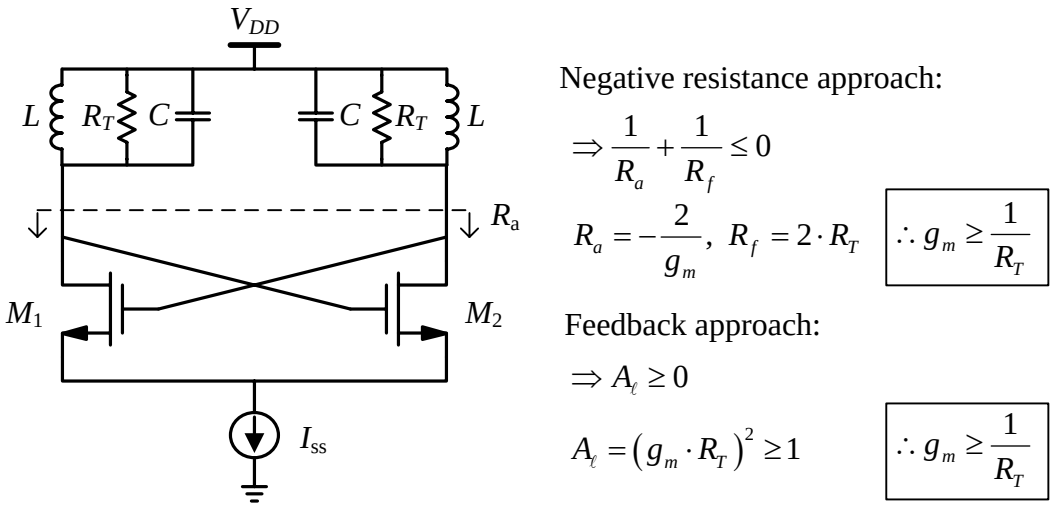


Figure 3.15: Start-up requirements of an NMOS cross-coupled LC VCO based on two different methods, the negative resistance approach and the feedback approach.

approach results in the same start-up criterion of:

$$g_m \geq 1/R_T \tag{3.16}$$

This constraint has a direct impact on the design as it imposes a fundamental lower limit on power consumption.

3.4 Steady-state Characteristics

Starting from the two-pole transfer function given in (3.13), we may solve for the natural and forced response of $v_o(t)$ due to some excitation, such as $v_x(t)$ in Fig. 3.13:

$$v_o(t) = f(v_x(t)) + A_1 \cdot e^{-\frac{\omega_o}{2Q}(1-A_l)t} \cos(\omega_o' t) \tag{3.17}$$

where A_1 depends on initial conditions and ω_o' is the frequency of zero-crossings during oscillation build-up (the imaginary term of (3.14)) and is close but not equal to the

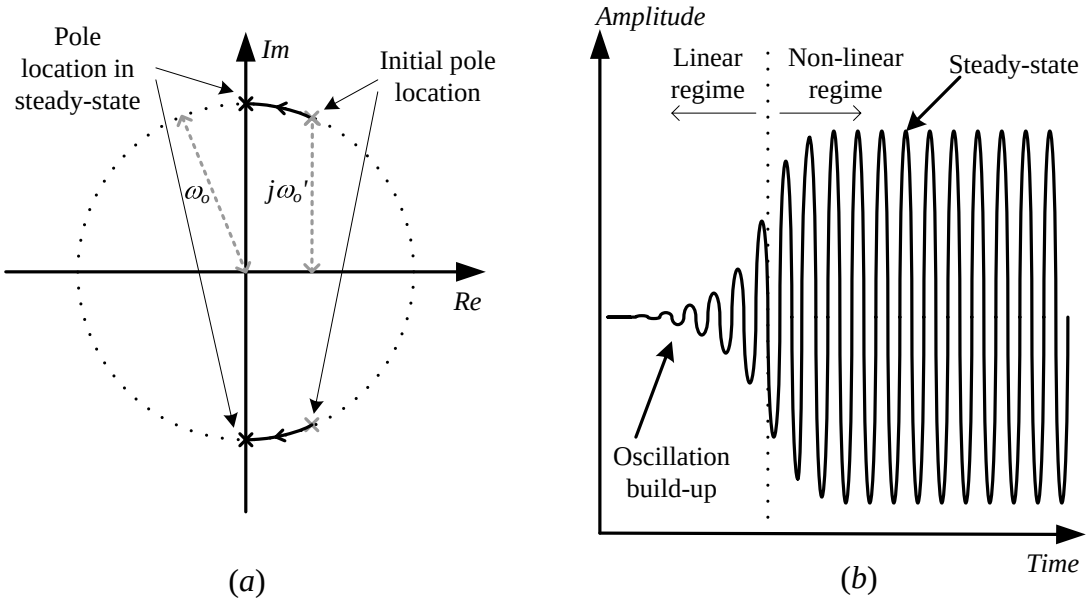


Figure 3.16: (a) Root locus of LC oscillator. (b) Output waveform of LC oscillator.

steady-state frequency of oscillation, ω_o. Note that for $A_l > 1$, the envelope of the second term grows exponentially. The exponential nature of $v_o(t)$ brings the oscillator into a nonlinear regime of operation where steady-state is eventually reached. This behavior is shown in Fig. 3.16.

In steady-state, the poles of the oscillator transfer function are positioned almost exactly on top of the imaginary axis, and the loop gain approaches unity:

$$A_{l,ss} = \frac{G_{m,L} R_T}{n} \cong 1 \tag{3.18}$$

where $G_{m,L}$ represents the large-signal transconductance in steady-state, in contrast to g_m, the small-signal transconductance, which is only relevant during start-up when signals are small. $G_{m,L}$ varies periodically in time and may be expressed as a Fourier

series [51]:

$$G_{m,L} = \sum_{k=-\infty}^{\infty} g_m^{(k)} e^{jk\omega_o t} \tag{3.19}$$

where k is the harmonic index. We note that for differential oscillators, $G_{m,L}$ is centered at $2\omega_o$ instead, and thus k should be replaced by $2k$. Although, the device transconductance may produce current at many of its harmonics, the LC tank greatly attenuates such components. Hence, the steady-state output amplitude is determined mainly by the fundamental component of the output current:

$$\hat{V}_o = |I_T(j\omega_o)| \cdot R_T \tag{3.20}$$

3.5 Phase Noise in LC Oscillators

An exact analysis of phase noise in LC oscillators is too mathematically involved to provide useful design insights. Instead, we begin with a linear time-invariant (LTI) approach to gain a basic (though somewhat limited) understanding of phase noise.

3.5.1 First-order LTI Analysis

The following analysis [50] is performed on the generalized LC oscillator schematic shown in Fig. 3.17. The circuit is treated as a positive feedback amplifier with a loop gain very close to but less than unity (i.e. $A_{l,ss} = G_{m,L}R_T/n = 1 - \epsilon$, where $\epsilon \ll 1$). In Fig. 3.17, $\overline{i_{n,1}^2}$, $\overline{i_{n,2}^2}$, and $\overline{v_{n,1}^2}$ are uncorrelated noise sources from the active device. It is

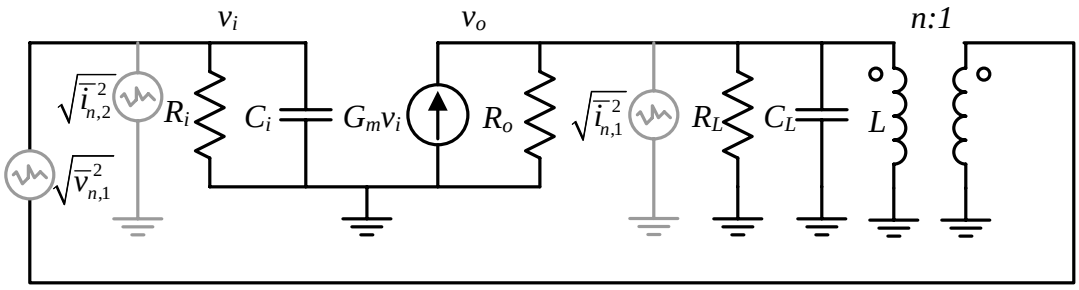


Figure 3.17: Generic LC oscillator schematic with device noise sources.

convenient to lump all noise components into a single equivalent noise generator:

$$\overline{i_n^2} = \overline{i_{n,1}^2} + \frac{\overline{i_{n,2}^2}}{n^2} + \overline{v_{n,1}^2} \cdot \left(G_m - \frac{1}{nZ_i} \right)^2 + 4k_B T \frac{1}{R_L} \Delta f \tag{3.21}$$

where Z_i is the device input impedance, k_B is Boltzman's constant, and where the last term is the thermal noise contributed by the R_L. In (3.21), G_m is the device transconductance and could be a small- or large-signal quantity, depending on the regime of operation. The equivalent noise source defined by (3.21) generates a corresponding output voltage noise density:

$$\sqrt{\overline{v_o^2}/\Delta f} = -\frac{\sqrt{\overline{i_n^2}/\Delta f} \cdot Z_T}{1 - G_m Z_T / n} \tag{3.22}$$

where Z_T is the loaded tank impedance. Phase noise is typically considered at frequency offsets relatively close to the carrier (i.e. $|\omega - \omega_o| \ll 1$). Hence, the tank impedance given by (3.7) is adequately approximated as:

$$Z_T \approx \frac{R_T}{1 + 2jQ_o \frac{\omega - \omega_o}{\omega_o}} \tag{3.23}$$

where $R_T = R_L||R_o||n^2R_i$ and Q_o is the loaded quality factor. Substituting (3.23) into (3.22), we obtain:

$$\left(\overline{v_o^2}/\Delta f\right) = \left(\overline{i_n^2}/\Delta f\right) \cdot \frac{R_T^2}{\left(1 - G_m R_T/n\right)^2 + 4Q_o^2\left(\Delta\omega/\omega_o\right)^2} \tag{3.24}$$

where $\Delta\omega = \omega - \omega_o$. We note that (3.24) will have a Lorentzian profile for white noise sources. As the oscillator transitions into steady-state, the active device begins to limit and the loop gain decreases such that (3.18) eventually holds. Thus, in steady-state, the first term of the denominator in (3.24) becomes negligible at frequency offsets $\Delta\omega$ of interest. Hence, we may normalize the total output noise power spectral density (PSD) to the mean-squared output voltage V_o^2 as follows:

$$\frac{\overline{v_o^2}/\Delta f}{V_o^2}(\Delta\omega) \approx \frac{\overline{v_n^2}/\Delta f}{V_o^2} \cdot \frac{1}{4Q_o^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3.25}$$

where $\overline{v_n^2} = \overline{i_n^2} \cdot R_T^2$. The oscillator output V_o results from the inherent noise sources amplified by the positive feedback loop. Its amplitude is established by limiting mechanisms specific to the circuit topology, and must satisfy $V_o^2 = \frac{1}{2\pi}\int_0^\infty \left(\overline{v_o^2}/\Delta f\right) \cdot d\omega$ [50].

The quantity derived in (3.25) does not take into account folding of noise sources. It has been shown that in steady-state where the large-signal transconductance is defined by (3.19), the output noise differs from (3.24) by a factor of 1/2, due to the translation of the noise originating close to the carrier back to the same frequency [51]. This factor of 1/2 has also been explained by arguments stating that oscillators inherently reject half of the noise which is amplitude-modulated (AM), and only the remaining half, comprised of the phase-modulated (PM) component, contributes to oscillator noise or

phase noise [52, 53]. A rigorous analysis based on AM/PM decomposition of noise and folding mechanisms was performed in [54]. We make a final adjustment to (3.25) to accommodate this factor of 1/2 and arrive at an LTI approximation of the single-sided noise spectral density, or phase noise, for the simplified LC oscillator shown in Fig. 3.17:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left[\frac{1}{2} \cdot \frac{\overline{v_n^2}/\Delta f}{V_o^2} \cdot \left(\frac{\omega_o}{2Q_o\Delta\omega}\right)^2\right] \tag{3.26}$$

Equation (3.26) shares many similarities with the widely used phase noise models from the work of Leeson [55]. It may also be expressed in a different form given by:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left[\frac{1}{8} \cdot \frac{\overline{i_n^2}/\Delta f}{V_o^2} \cdot \frac{1}{C^2} \cdot \left(\frac{1}{\Delta\omega}\right)^2\right] \tag{3.27}$$

Although the above analysis has largely ignored the nonlinear time-varying mechanisms contributing to phase noise in practical oscillators, (3.26) and (3.27) provide an insightful picture revealing dominant effects. For the special case, where $\overline{i_n^2}$ is only due to the tank resistance, it can be rewritten as:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left[\frac{1}{2} \cdot \frac{k_B T}{P_{dis}} \cdot \frac{1}{Q_o^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2\right] \tag{3.28}$$

Equation (3.28) approximates the phase noise of an oscillator that is ideal in all respects expect for that its LC tank has finite Q. Thus, (3.28) can be used as a benchmark for the minimum achievable phase noise per given Q_o, ω_o, and power dissipation P_{dis}.

3.5.2 LPVT Analysis

The analysis shown in the previous section was based on an LTI approximation of the oscillator. Clearly, the oscillator operates in a non-linear regime in steady-state

(Section 3.4) and its operating point is periodically time-varying. Whereas the statistics of the noise due to the tank losses are stationary, active noise generators are not (since the transistor bias point is periodically time-varying). Thus, more accurate analyses need to consider these effects. Similarly to previous work on linear periodically time varying (LPVT) mixer noise analysis by Hull et al. [56], Hajimiri et al. demonstrated that a LPVT analysis adequately captures oscillator phase noise mechanisms [53]. Despite the fact that an oscillator operates nonlinearly, they showed that its noise-to-phase transfer function is itself linear. By considering the periodically time-varying behavior of this linear relationship they established a new quantity, namely the (phase) impulse sensitivity function (ISF). The ISF describes a charge input to excess phase output transfer function vs. launch time, or, because of its periodicity, vs. the phase angle of the oscillation cycle. Noise generators inject charge disturbances from different points of the circuit. Hence, the ISF must be evaluated at each relevant node. A periodically time-varying impulse response can be defined as follows [53]:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_o\tau)}{q_{\max}} \cdot u(t-\tau) \tag{3.29}$$

where $u(\cdot)$ is the unit step function. $\Gamma(\omega_o\tau)$ is normalized to the maximum charge swing $q_{\max}$ across the capacitor (present at the node in question) in order to make $h_\phi(\cdot)$ independent of amplitude. The excess phase due to a small current disturbance at node x, $i_x(\tau)$ is then given by:

$$\phi_x(t) = \int_{-\infty}^{\infty} h_{\phi,x}(t,\tau) \cdot i_x(\tau) \cdot d\tau \tag{3.30}$$

In practice, the excess phase is computed in the frequency domain using the relevant Fourier series coefficients of $h_\phi(\cdot)$. As explained in Chapter 2, such phase fluctuations appear as pairs of equal sidebands on each side of the carrier. Contributions from all relevant noise generators in the circuit must be taken into account to arrive at the net phase noise. The phase noise due to an equivalent white noise current generator, is given by:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left[\frac{\Gamma_{\text{rms}}^2}{q_{\max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right] \tag{3.31}$$

Where $\Gamma_{\text{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi}|\Gamma(x)|^2 dx$ (or one half times the sum of all squared Fourier coefficients). The cyclostationarity of a given noise source can be handled using an effective ISF and expressing the noise source itself as being stationary, as explained in [53]. For the special case of a flicker noise generator with $1/f$ corner frequency $\omega_{1/f}$ and given by $(\overline{i_n^2}/\Delta f)\omega_{1/f}/\Delta\omega$, Γ_{rms}^2 in (3.31) simplifies to $(c_o/2)^2\omega_{1/f}/\Delta\omega$ [53], where c_o is the dc Fourier series coefficient of $\Gamma(x)$. To make a meaningful comparison with the results from our LTI analysis above, we substitute $q_{\max} = CV_{\max} = \sqrt{2}CV_o$ into (3.31) and obtain:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left[\frac{1}{4}\cdot\frac{\overline{i_n^2}/\Delta f}{V_o^2}\cdot\frac{\Gamma_{\text{rms}}^2}{C^2}\cdot\left(\frac{1}{\Delta\omega}\right)^2\right] \tag{3.32}$$

We note that (3.32) corresponds to (3.27) scaled by $2\Gamma_{\text{rms}}^2$. Hence, this shows the power of the ISF as it exclusively captures all noise translations. If we set $\Gamma_{\text{rms}}^2 = 1/2$ implying that Γ_{rms} is a perfect sinusoid at ω_o, (3.32) and (3.27) become identical, as expected. Recall that an adjustment of 1/2 was factored in to arrive at (3.27), implying that only PM noise should be considered while AM noise should be ignored (due to the fact that

amplitude deviations vanish over time). Equation (3.32) makes the same assumption since it was derived based on phase disturbances exclusively. However, actual AM noise contributions can be determined by using the same LPVT method based on an amplitude ISF [57].

The main limitation of the LPVT analysis is that determining $\Gamma(x)$ requires cumbersome simulations. Since today's simulation CAD tools (e.g. SpectreRF) are able to compute phase noise directly, it is not common practice to compute $\Gamma(x)$ separately. Nevertheless, the above method is theoretically satisfying. Many other treatments of oscillator phase noise have been proposed as the research community continues its quest for an accurate closed-form solution that depends only on fundamental device parameters [51, 53, 54, 58, 59], some being notably rigorous [60, 61]. Meanwhile, research on general numerically-stable and efficiently accurate phase noise computational methods has had a deep impact on simulation CAD tools [14, 62].

3.6 Integrated LC VCO topologies

There are many ways to realize integrated LC VCOs, and new topologies continue to emerge [63–65]. Here we limit ourselves to a subset comprised of three of the most widely used configurations, as shown in Fig. 3.18.

As seen in Fig. 3.18, these topologies are differential. As with other blocks in a typical radio, differential operation greatly suppresses the circuit's sensitivity to undesired common-mode disturbances from other blocks sharing the same substrate. Note that

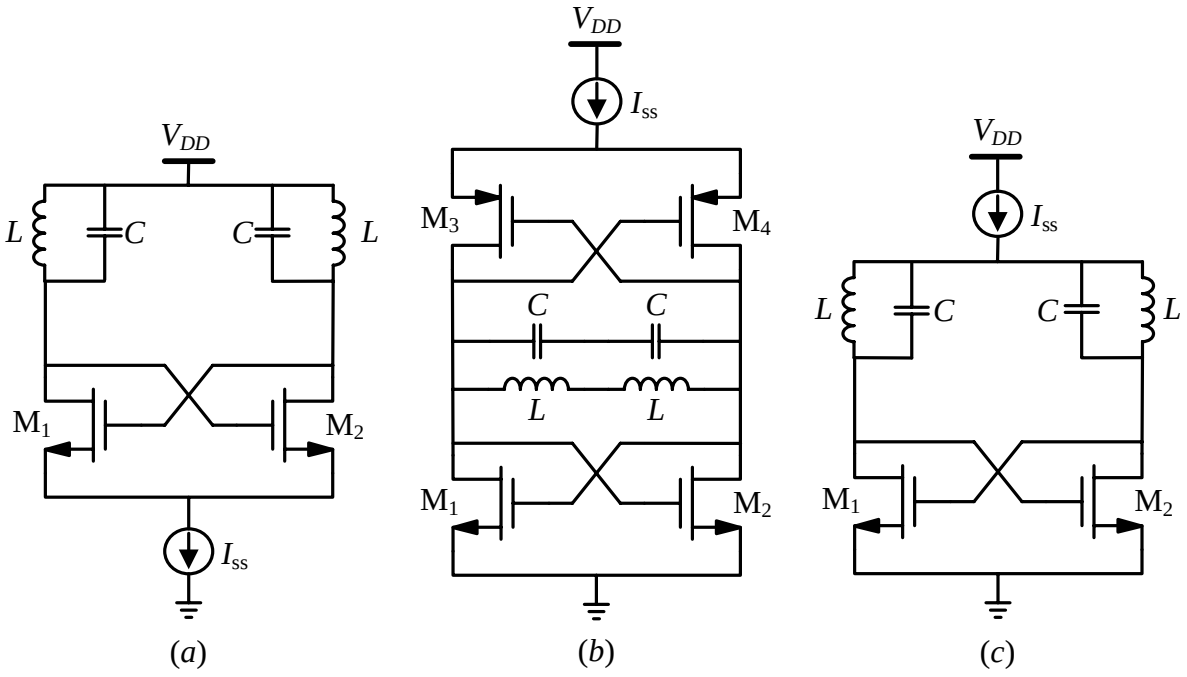


Figure 3.18: *LC* VCO topologies: (*a*) tail-biased cross-coupled, (*b*) complementary cross-coupled, (*c*) top-biased cross-coupled.

configurations (a) and (c) may be implemented with PMOS devices instead (the current source is then rearranged accordingly). In the following paragraphs, we will compare their relative performance, and discuss other second order considerations qualitatively.

3.6.1 Device Parasitics

One important characteristic for which the above configurations differ is that of how much transistor parasitic capacitance is contributed to the LC tank. Transistor parasitics bring in two undesired elements. First, such parasitics are not necessarily well modeled and face process variations which spread the VCO frequency from its nominal value. Furthermore, these parasitics constitute a fixed capacitance term that ultimately limits the achievable VCO tuning range. Secondly, transistor parasitics are partially made up of junction capacitances which, aside from not being well-modeled, are nonlinear. Such nonlinear capacitors can make the VCO frequency move as the supply varies and introduce undesired noise translations.

As seen in Fig. 3.18, each configuration is biased at some current level, I_{ss}. Although, each configuration exhibits different large-signal steady-state characteristics, their small-signal initial operation is identical, and the same as that given earlier in Section 3.3. Each configuration provides a (small-signal) negative resistance given by:

$$R_a = -2/g_m \tag{3.33}$$

where g_m is the effective transconductance per side. For configurations (a-c), g_m is given

by:

$$g_m = g_{m,n/p} \qquad \text{Fig. 3.18}(a) \qquad (3.34a)$$

$$g_m = g_{m,n} + g_{m,p} \qquad \text{Fig. 3.18}(b) \qquad (3.34b)$$

$$g_m = g_{m,n/p} \qquad \text{Fig. 3.18}(c) \qquad (3.34c)$$

For a given LC tank, R_a, and thus g_m, is set. In typical deep submicron CMOS technologies, an NMOS gives about $\sqrt{4}$ to $\sqrt{5}$ more transconductance per current than a same size PMOS transistor. As a result, NMOS-based implementations of configurations (a) and (c) are most efficient in terms of start-up. Hence, for a given current budget and required R_a, these implementations result in a smaller active area and thus less parasitic capacitance, C_p, than that of configuration (b). By the same reasoning, the converse is true for PMOS-based implementations of configurations (a) and (c).

The parasitic capacitance contributed by the transconductor has three basic components (all proportional to gate width), the gate-to-source capacitance C_{gs}, the drain-gate capacitance C_{dg}, and the drain-to-bulk capacitance C_{db}. By inspection, we obtain:

$$C_p = C_{gs} + 4C_{gd} + C_{db} \qquad \text{Fig. 3.18}(a) \qquad (3.35a)$$

$$C_p = C_{gs,n} + C_{gs,p} + 4(C_{gd,n} + C_{gd,p}) + C_{db,n} + C_{db,p} \qquad \text{Fig. 3.18}(b) \qquad (3.35b)$$

$$C_p = C_{gs} + 4C_{gd} + C_{db} \qquad \text{Fig. 3.18}(c) \qquad (3.35c)$$

Combining these observations, we can express the relative parasitic contributions of each configuration as summarized in Table 3.1.

Table 3.1: Relative parasitic capacitance contribution for given start-up requirement

Conditions: I_{ss}, g_m fixed	Tail-biased NMOS Fig. 3.18(a)	Tail-biased PMOS Fig. 3.18(a)	Tail-biased CMOS Fig. 3.18(b)	Top-biased NMOS Fig. 3.18(c)	Top-biased PMOS Fig. 3.18(c)
$C_{gs} + C_{db}$	1	4-5	1.25-1.5	1	4-5
C_{dg}	1	4-5	5-6	1	4-5

3.6.2 Output Voltage Amplitude

As discussed in Section 3.4, the steady-state amplitude is set by the nonlinear limiting characteristic of the circuit (topology-dependent) and is generally a function of bias conditions (e.g. bias current). The configurations shown in Fig. 3.18 generally provide a different output swing for a given bias current.

3.6.2.1 Current-Limited and Voltage-Limited Regimes

We begin by identifying two different regimes of steady-state operation: the Current-Limited and Voltage-Limited regimes [66]. Although these two regimes account for a simplistic and somewhat restricted view of the mechanism setting an oscillator's output amplitude, they have become widely accepted in the literature. Furthermore, simplifying the VCO operation to two regimes can provide useful insight. This section will treat the output swing in the context of these two regimes, whereas the subsequent section will establish a more general approach to quantifying the oscillator amplitude.

When the output swing is mainly a function of the bias current I_{ss}, the VCO can be described as operating in the current-limited regime. Conversely, when the output swing has grown such that it has become saturated due to the finite voltage headroom,

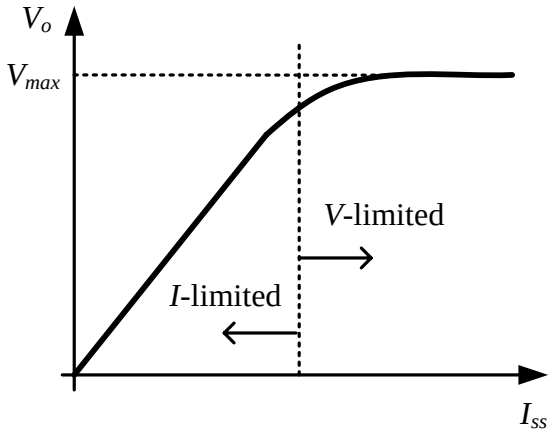


Figure 3.19: Steady-state voltage amplitude vs. I_{ss} for typical *LC* VCO.

the VCO can be described as operating in the voltage-limited regime. These two regimes are illustrated in Fig. 3.19, where the output voltage swing is plotted as a function of I_{ss} for a typical VCO design.

Let us begin with the current-limited regime, where the output swing is within the available voltage headroom. Typically, the output voltage is large enough to fully commutate I_{ss} between the left and right branches of the circuit. For the tail- and top-biased N/PMOS configurations shown in Fig. 3.18, this ideally produces a 0-I_{ss} current square wave driving each branch (with opposite polarity) and producing a voltage swing across each half of the *LC* tank. Higher harmonics are filtered by the tank capacitor, while the fundamental harmonic ($\propto I_{ss} \cdot 2/\pi$) gives rise to a voltage directly proportional to R_T (see (3.20)). For the tail-biased CMOS configuration shown in Fig. 3.18, commutation of I_{ss} takes place similarly, producing a $\pm I_{ss}$ current square-wave flowing differentially

across the LC tank. Hence, the resulting fundamental harmonic is $I_{ss} \cdot 4/\pi$ and the output voltage is also proportional to R_T. Thus, in the current-limited regime, the tail-biased CMOS configuration has twice the voltage swing efficiency as that of the tail- and top-biased N/PMOS topologies. The output voltage relationships for each configuration in the current-limited regime are given by:

$$V_{od} = \frac{2}{\pi} I_{ss} \cdot R_T \qquad (I\text{-limited}) \qquad \text{Fig. 3.18}(a) \qquad (3.36a)$$

$$V_{od} = \frac{4}{\pi} I_{ss} \cdot R_T \qquad (I\text{-limited}) \qquad \text{Fig. 3.18}(b) \qquad (3.36b)$$

$$V_{od} = \frac{2}{\pi} I_{ss} \cdot R_T \qquad (I\text{-limited}) \qquad \text{Fig. 3.18}(c) \qquad (3.36c)$$

To understand the transition from current- to voltage-limited regime, the ideal current sources shown in Fig. 3.18 must be replaced by a realistic implementation. No matter what topology is used, all current sources have a certain voltage compliance range below which no further current can be sourced/sunk. Consider the configuration shown Fig. 3.20. As I_{ss} is increased, the gate-source voltage of $M_{1,2}$ increases as well (approximately as $\sqrt{I_{ss}}$). Eventually, the drain-source voltage of M_T becomes too low and its drain current saturates, even as I_{ss} continues to rise. This also corresponds to the point where M_T enters the triode region. Alternatively, a cascode-type current source could be used to extend the compliance voltage range, and thus increase $V_{\max}$. However, high-frequency noise from the cascode transistor usually prohibits its use in RF VCOs.

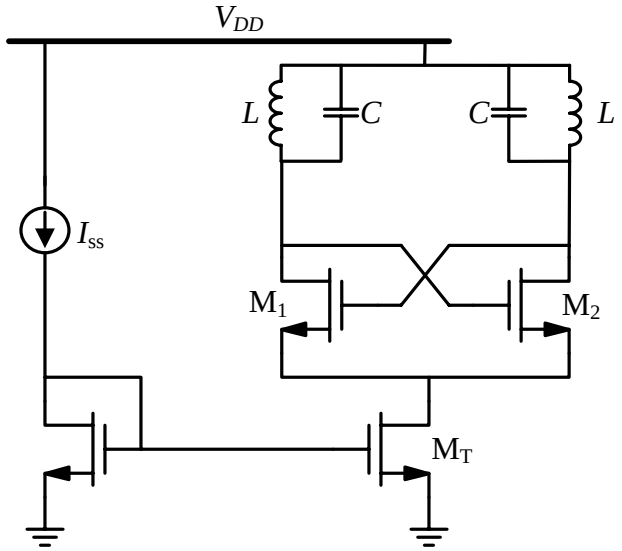


Figure 3.20: Typical bias configuration for tail-biased NMOS topology.

In the voltage-limited regime, the differential output voltage amplitude is given by:

$$V_{od} = V_{\max} \propto I_{\max} \cdot R_T \qquad (V\text{-limited}) \tag{3.37}$$

where $I_{\max}$ depends on the specific current source topology and the available voltage headroom.

As noted earlier, the tail-biased complementary (CMOS) topology is the most efficient in terms of swing-per-current in the current-limited regime. However, in the voltage-limited regime this is often not the case. As shown in Fig. 3.18, the complementary topology requires much more headroom (all else equal), as it stacks an additional transistor which requires another V_{GS}. In a low-medium supply implementation ($V_{DD} < 4V_T$), this drastically reduces the range over which M_T can source current. As a result, the complementary topology achieves a lower maximum voltage than that of

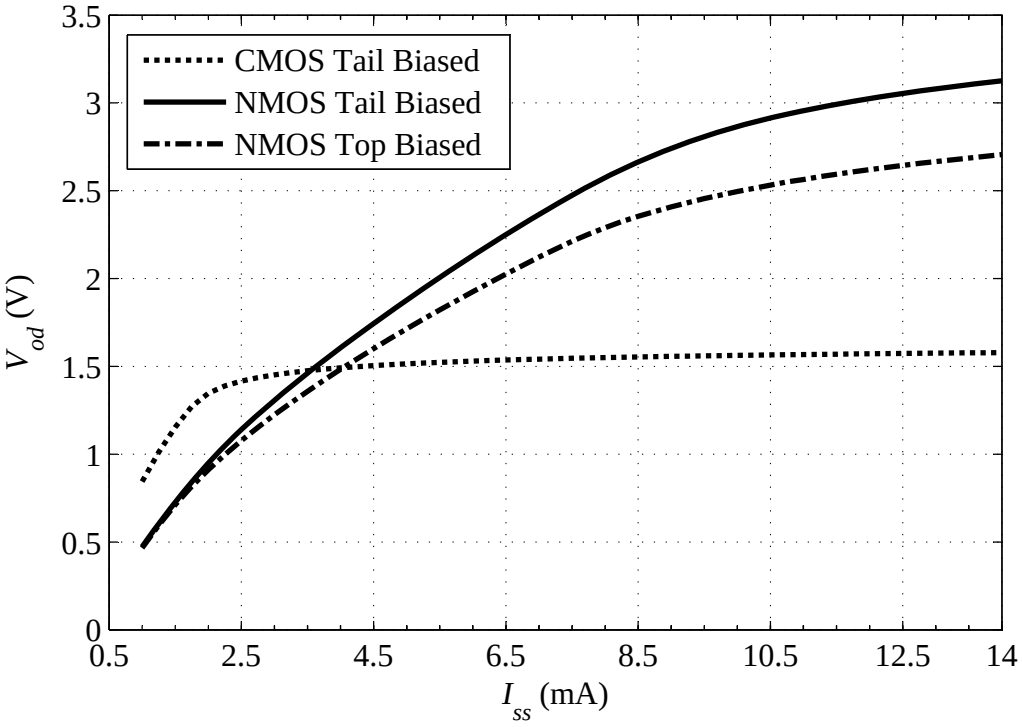


Figure 3.21: Simulated differential output swing for reference designs of each of the three basic configurations (Fig. 3.18(a)-(c)).

the tail- and top-biased N/PMOS configurations. To illustrate our observations, typical designs are implemented for each configuration of Fig. 3.18 and their output swing vs. I_{ss} characteristic is plotted in Fig. 3.21. Each configuration is designed for 2GHz operation, given the same LC tank, and sized for to give equal g_m at I_{ss}=1mA. The supply voltage is set to 2V in all cases. The inductor gives a differential Q (at 2GHz) and inductance of 11.7 and 4.2nH, respectively.

From Fig. 3.21, we note that the complementary tail-biased topology indeed saturates much earlier. Much larger output swings can be achieved with the other two configurations, at the expense of bias current. The swings of the tail- and top-biased

NMOS configurations differ only due to the different nature of the current source transistor M_T used in each implementation - the achievable swing does not necessarily favor one versus the other and M_T could have sized to show equal swing for both. Instead, the current scenario highlights the fact that the voltage compliance of current source transistor M_T affects the achievable swing.

3.6.2.2 Analysis of RF VCO Amplitude

At high frequencies, the high impedance of the current source in each of the three configurations shown in Fig. 3.18 cannot be sustained. This especially true since the tail transistor tends to be very large and, as mentioned earlier, is not commonly cascoded. A large device area is required to lower flicker noise, which appears as phase noise once up-converted by the cross-coupled switching pair(s). In practical implementations, the parasitic capacitance C_b at the drain of M_T can be anywhere between 1 to 10pF. Hence, this amounts to a low impedance at RF frequencies. Recall that the limiting behavior was described earlier as a commutating action on the bias current. As a result, the AC current would have a square-wave characteristic, which gave the basis for (3.36). However, the presence of a near AC ground at the tail- or top-node in each of the three configurations drastically alters the current waveforms and a square-wave model is no longer adequate. Figs. 3.22 and 3.23 illustrate the effect of C_b on the normalized drain current (I_D/I_L) waveforms at 100MHz and 1GHz, respectively.

Hence, at frequencies where the impedance across the current source is low, the

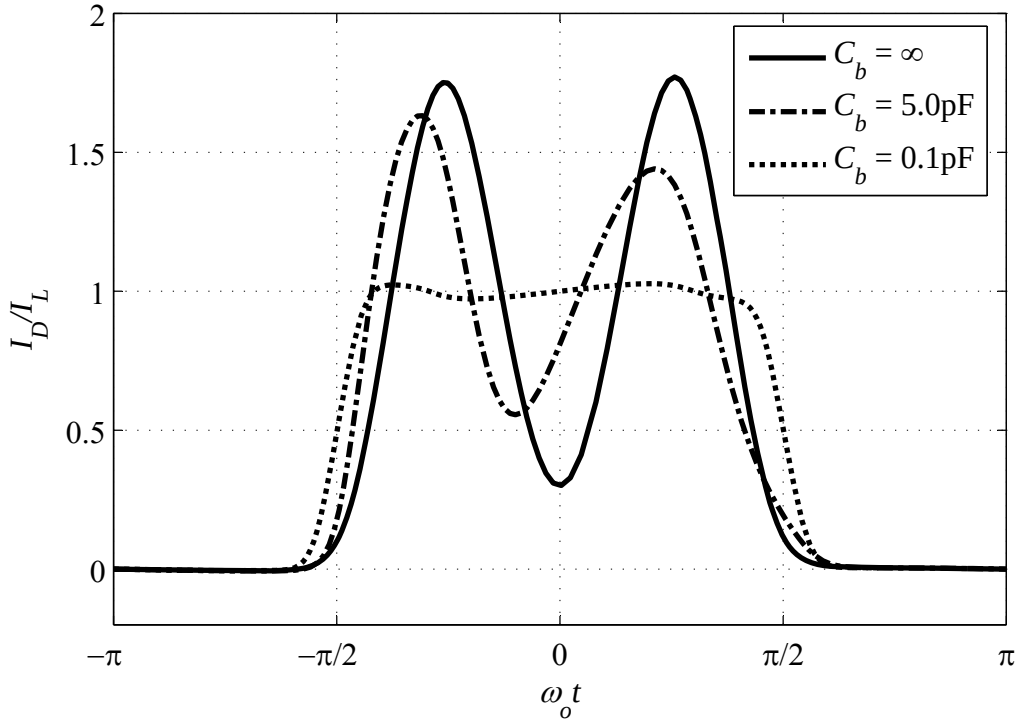


Figure 3.22: I_D/I_L vs. $\omega_o t$ for the tail- and top-biased N/PMOS topologies (Figs. 3.18 (a) and (c)) for different values of C_b at 100MHz.

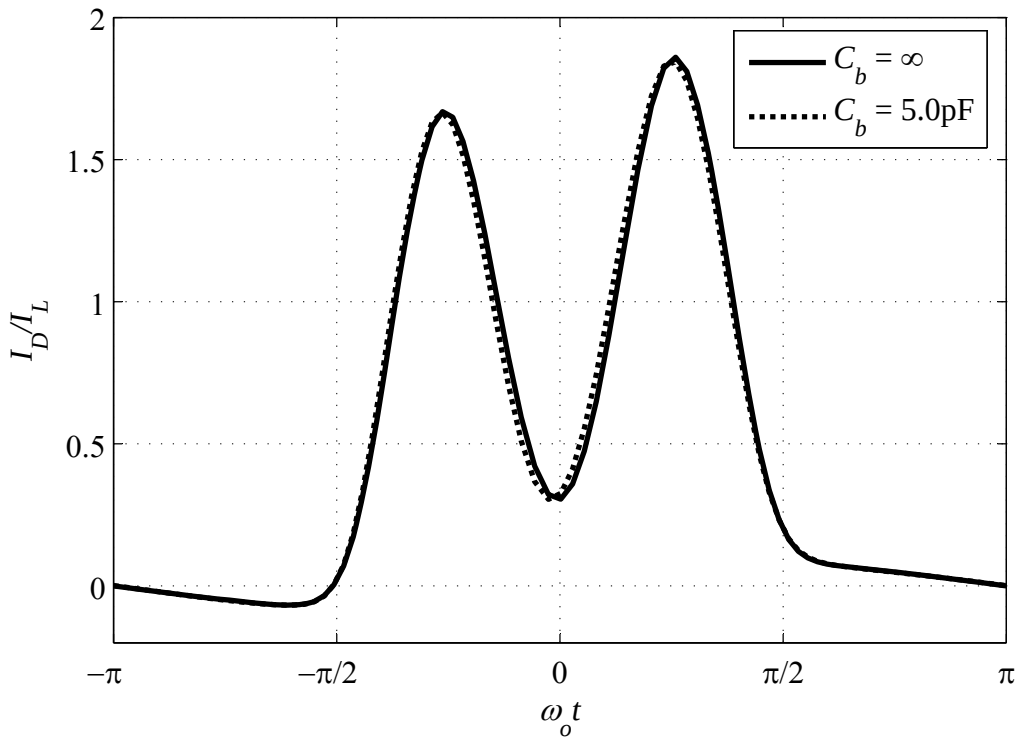


Figure 3.23: I_D/I_L vs. $\omega_o t$ for the tail- and top-biased N/PMOS topologies (Figs. 3.18 (a) and (c)) for different values of C_b at 1GHz.

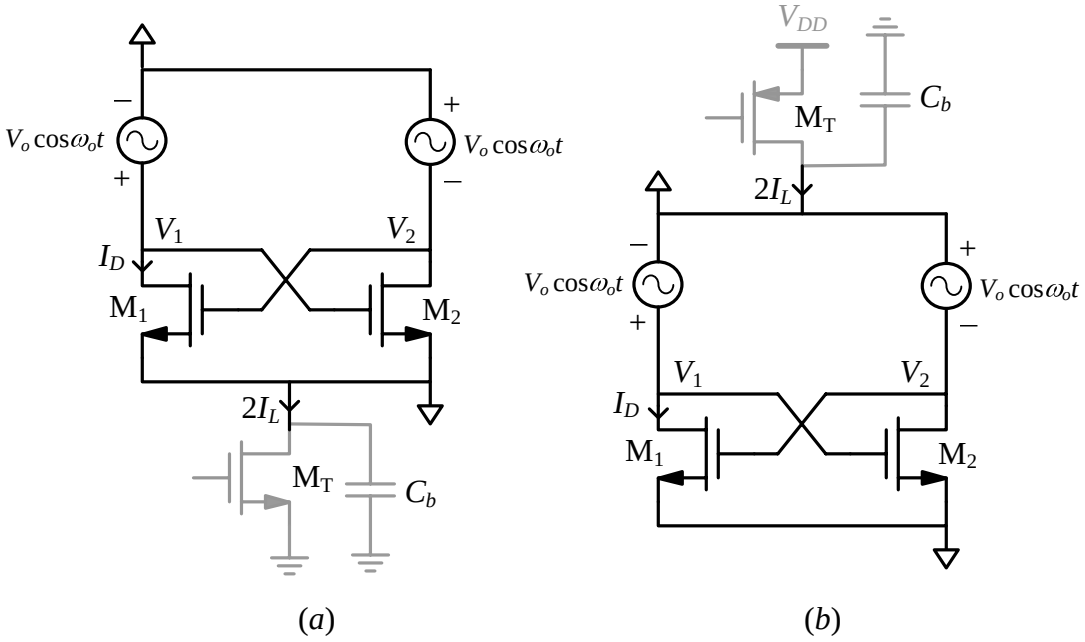


Figure 3.24: (*a*) Tail- and (*b*) top-biased NMOS configurations with current source AC shorted.

drain current is no longer set by I_{ss}. If the impedance is low enough to be assumed a perfect AC ground, the drain current is then only a function the large-signal I-V characteristic. With their current source (AC) shorted, the tail- and top-biased N/PMOS configurations shown in Fig. 3.18 become identical, as shown in Fig. 3.24.

Because I_D is set by the device large-signal I-V characteristic, the resulting current waveform is a function of V_{GS} (equivalently V_{DS}), which in turn is set by the voltage swing across the LC tank. Fig. 3.25 shows the normalized drain current as a function of the differential voltage across the devices. For small voltage swing, the devices transition back and forth between the off state and the saturation region. At times when the output voltage provides enough gate overdrive ($V_{GS} > V_T$), the device is in

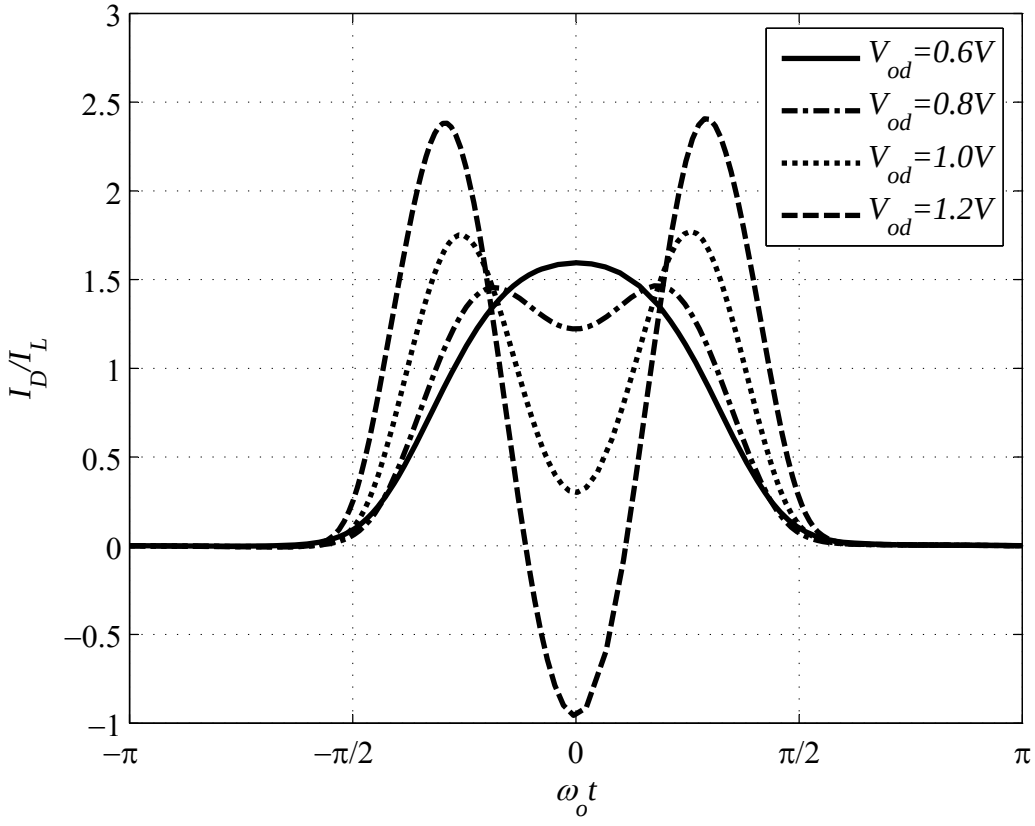


Figure 3.25: I_D/I_L vs. $\omega_o t$ for the tail- and top-biased N/PMOS topologies (Figs. 3.24 (a) and (b)) for different swings (V_{od}) at 100MHz.

saturation, otherwise it is off. As the swing is increased, the device enters the triode region for phase angles around zero (when the gate voltage is largest and the drain voltage is smallest). This occurs as V_{DS} dips below the saturation voltage ($V_{GS} - V_T$) for long channel devices. Hence, the device spends a longer part of the cycle in the triode region as the voltage swing is increased. For very large swings, it is possible for the drain current to reverse direction if $V_{DS} < 0$ as the device is pushed deep into the triode region. However, regardless of the voltage swing, the time-average drain current must stay constant at $I_{ss}/2$, as it is set by the current source. This fact will be used to derive the normalized drain current as a function of normalized voltages.

In the following analysis, the current source is assumed to be shorted out such that the source-coupled node is effectively AC grounded. The long-channel approximation is used to simplify our derivation [50]. The steady-state voltage at nodes V_1 and V_2 in Fig. 3.24 are given by:

$$V_1 = V_B + V_o \cos \omega_o t \tag{3.38a}$$

$$V_2 = V_B - V_o \cos \omega_o t \tag{3.38b}$$

where V_B is the steady-state DC bias voltage at the drain of M_1 (or M_2). The drain current of transistor M_1 (or M_2) is given by:

$$I_D = \beta(V_1 - V_T)^2 \qquad \text{Saturation} \tag{3.39a}$$

$$I_D = \beta(2(V_1 - V_T)V_2 - V_2^2) \qquad \text{Triode} \tag{3.39b}$$

$$I_D = 0 \qquad \text{Off} \tag{3.39c}$$

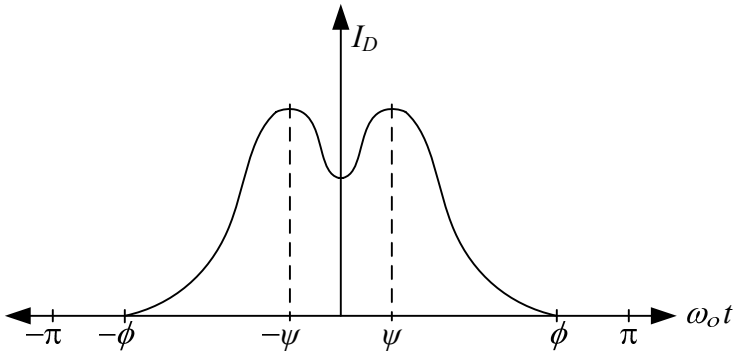


Figure 3.26: Typical I_D vs. $\omega_o t$ waveform.

where $\beta = \mu C_{ox} W/L$ and V_T is the device threshold voltage. As seen in Fig. 3.25, the calculation of I_D is complicated by the fact that M_1 (or M_2) may operate in as many as three alternate regions of operation. However, we will see that I_D can be expressed in normalized form, from which we can generate general curves that shall provide great insight into oscillator design.

Fig. 3.26 illustrates a generic drain current waveform over $-\pi \leq \omega_o t \leq \pi$, on which the operating region boundaries have been labeled. For $|\omega_o t| > \phi$, the device is off with $I_D = 0$. For $\psi \leq |\omega_o t| \leq \phi$, the device is in saturation. And for $|\omega_o t| \leq \psi$, the device is in the triode region.

Let us define a voltage V_A such that:

$$I_{D,\text{avg}} = I_L = I_{ss}/2 = \beta(V_A - V_T)^2 \tag{3.40}$$

The above implies that V_A is the quiescent (zero voltage swing) DC bias voltage for M_1 —in other words, the V_{GS} value needed to support a DC current of I_L. Thus, it is given

by:

$$V_A = \sqrt{I_L/\beta} + V_T \tag{3.41}$$

Taking the ratio of (3.39a) and (3.41) gives the normalized drain current in the saturation region:

$$\begin{aligned} \frac{I_D}{I_L} &= \frac{\beta(V_1 - V_T)^2}{\beta(V_A - V_T)^2} \\ &= \left(\frac{V_1}{V_A - V_T} - \frac{V_T}{V_A - V_T}\right)^2 \end{aligned} \tag{3.42}$$

Substituting (3.38a) into the above yields:

$$\frac{I_D}{I_L} = \left(\frac{V_B}{V_A - V_T} + \frac{V_o}{V_A - V_T}\cos\omega_o t - \frac{V_T}{V_A - V_T}\right)^2 \qquad \text{Saturation} \tag{3.43}$$

Similarly, using (3.38a), (3.38b), (3.39b), and (3.40), we have:

$$\begin{aligned} \frac{I_D}{I_L} = \quad & 2 \cdot \frac{V_B + V_o\cos\omega_o t - V_T}{V_A - V_T} \cdot \frac{V_B - V_o\cos\omega_o t}{V_A - V_T} \\ - \quad & \left(\frac{V_B - V_o\cos\omega_o t}{V_A - V_T}\right)^2 \qquad \text{Triode} \end{aligned} \tag{3.44}$$

Equations (3.43) and (3.44) describe the waveform shown in Fig. 3.26. Using the fact that $I_{D,\text{avg}} = I_L$ and applying boundary conditions for operating region transitions, it is possible to solve for V_B. First we note that at $\omega_o t = \psi$, where the device transitions from triode to saturation, $V_{GS} - V_T = V_{DS}$, which is equivalent to:

$$V_1 - V_2 = V_T \qquad (\text{at } \omega_o t = \psi) \tag{3.45}$$

Substituting (3.38) into (3.45) gives:

$$2 \cdot V_o \cos\psi = V_T \tag{3.46}$$

At the point $\omega_o t = \phi$ beyond which the device turns off, $V_{GS} = V_T$, or equivalently:

$$V_1 = V_T \qquad (\text{at } \omega_o t = \phi) \tag{3.47}$$

Substituting (3.38a) into (3.47), we have:

$$V_B = V_T - V_o \cos\phi \tag{3.48}$$

The average drain current is given by:

$$\begin{aligned} I_{D,\text{avg}} &= \frac{I_L}{\pi}\int_0^{\psi}\left(2\cdot\frac{V_o(\cos\omega_o t-\cos\phi)}{V_A-V_T}\cdot\frac{V_T-V_o(\cos\omega_o t+\cos\phi)}{V_A-V_T}\right)d\omega_o t \\ &- \frac{I_L}{\pi}\int_0^{\psi}\left(\frac{V_T-V_o(\cos\omega_o t+\cos\phi)}{V_A-V_T}\right)^2 d\omega_o t \\ &+ \frac{I_L}{\pi}\int_{\psi}^{\phi}\left(\frac{V_B}{V_A-V_T}+\frac{V_o}{V_A-V_T}\cos\omega_o t-\frac{V_T}{V_A-V_T}\right)^2 d\omega_o t \\ &= I_L \end{aligned} \tag{3.49}$$

Substituting (3.48) into (3.49) yields:

$$\begin{aligned} \pi &= \int_0^{\psi}\left(2\cdot\frac{V_o(\cos\omega_o t-\cos\phi)}{V_A-V_T}\cdot\frac{V_T-V_o(\cos\omega_o t+\cos\phi)}{V_A-V_T}\right)d\omega_o t \\ &- \int_0^{\psi}\left(\frac{V_T-V_o(\cos\omega_o t+\cos\phi)}{V_A-V_T}\right)^2 d\omega_o t \\ &+ \int_{\psi}^{\phi}\left(\frac{V_o}{V_A-V_T}(\cos\omega_o t-\cos\phi)\right)^2 d\omega_o t \end{aligned} \tag{3.50}$$

From (3.46), we have:

$$\begin{aligned} \psi &= \cos^{-1}\left(\frac{1}{2}\cdot\frac{V_T}{V_o}\right) \\ &= \cos^{-1}\left(\frac{1}{2}\cdot\frac{V_T}{V_A-V_T}\cdot\frac{V_A-V_T}{V_o}\right) \end{aligned} \tag{3.51}$$

We note that (3.51) and (3.50) are only functions of the normalized voltages $V_T/(V_A - V_T)$ and $V_o/(V_A - V_T)$. Hence, ψ is only a function of $V_T/(V_A - V_T)$ and $V_o/(V_A - V_T)$ as well. Thus, we may solve for I_D/I_L (the waveform of Fig. 3.26) as a function of normalized voltages:

$$\frac{I_D}{I_L} = f\left(\frac{V_o}{V_A - V_T}, \frac{V_T}{V_A - V_T}, \omega_o t\right) \tag{3.52}$$

In general, (3.50) is a transcendental equation that must be solved numerically. However, for the special case where $\phi = \pi$, meaning that the oscillation amplitude is never large enough to turn off the device, it can be solved explicitly and is given by (3.43) and (3.44) with $V_B/(V_A - V_T)$ substituted as:

$$\left(\frac{V_B}{V_A - V_T}\right)_{\phi=\pi} = \frac{V_T}{V_A - V_T} + \sqrt{1 - \frac{V_o^2}{(V_A - V_T)^2}\left[\frac{1}{2} - \frac{2}{\pi}(\psi + \sin\psi\cos\psi)\right] - \frac{4}{\pi}\frac{V_o V_T \sin\psi}{(V_A - V_T)^2} + \frac{V_T^2}{(V_A - V_T)^2}\frac{\psi}{\pi}} \tag{3.53}$$

For the more general cases where $\phi < \pi$, the following equation is solved numerically to find ϕ:

$$\begin{aligned} \pi &= \frac{V_o^2}{(V_A - V_T)^2} \cdot \left[\frac{\phi}{2} - 2\psi - \frac{3}{2}\sin\phi\cos\phi + \phi\cos^2\phi - 2\cos\psi\sin\psi\right] \\ &+ 4 \cdot \frac{V_o V_T}{(V_A - V_T)^2} \cdot \sin\psi - \frac{V_T^2}{(V_A - V_T)^2} \cdot \psi \end{aligned} \tag{3.54}$$

Once ϕ has been obtained, it is substituted into (3.48) and I_D/I_L can be evaluated using (3.43) and (3.44).

For the tail- or top-biased configurations shown in Fig. 3.18(a) and Fig. 3.18(c), the oscillating current that flows through each half of the LC tank is simply that of either

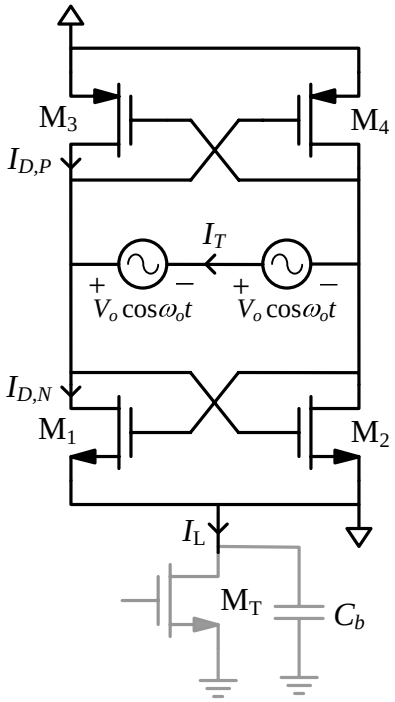


Figure 3.27: Tail-biased CMOS configuration of Fig. 3.18(b) with current source AC shorted.

device, and is thus given by:

$$I_T = I_{D,1} = I_{D,2} = I_D \tag{3.55}$$

In light of our analysis, this is more conveniently expressed in normalized form as:

$$\frac{I_T}{I_L}(\omega_o t) = \frac{I_D}{I_L}(\omega_o t) \tag{3.56}$$

where the implicit dependence on $V_o/(V_A - V_T)$ and $V_T/(V_A - V_T)$ has been omitted for clarity.

The tail-biased CMOS configuration with its current source AC-shorted somewhat differs from the other two. As shown in Fig. 3.27, this configuration now consists of two anti-parallel inverters across the *LC* tank. However, the drain current in each of

the top (PMOS) and bottom (NMOS) cross-coupled pair can be calculated using the same procedure. In the case of the CMOS topology, the oscillating current that flows through the (differential) LC tank is given by:

$$I_T = I_{D,1} - I_{D,3} = I_{D,4} - I_{D,2} \tag{3.57}$$

Hence the normalized current waveform in this case is given by:

$$\begin{aligned} \frac{I_T}{I_L}(\omega_o t) &= \frac{I_{D,N}}{I_L} \cdot \left(\frac{V_o}{V_{A,N} - V_{T,N}}, \frac{V_{T,N}}{V_{A,N} - V_{T,N}}, \omega_o t \right) \\ &- \frac{I_{D,P}}{I_L} \cdot \left(\frac{V_o}{V_{A,P} - V_{T,P}}, \frac{V_{T,P}}{V_{A,P} - V_{T,P}}, \omega_o t \right) \end{aligned} \tag{3.58}$$

If PMOS and NMOS devices are sized to provide equal drive and $V_{T,N} \approx V_{T,P}$, then:

$$\frac{I_{D,P}}{I_L}(\omega_o t) = \frac{I_{D,N}}{I_L}(\omega_o t - \pi) \tag{3.59}$$

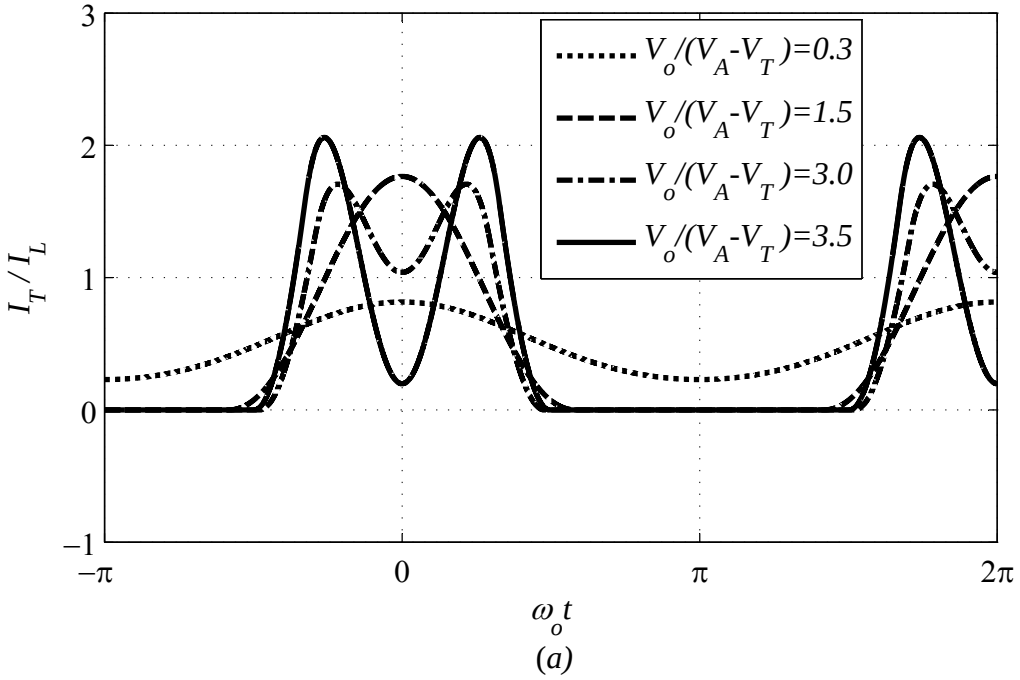
In that case, (3.58) simplifies to:

$$\frac{I_T}{I_L}(\omega_o t) = \frac{I_D}{I_L}(\omega_o t) - \frac{I_D}{I_L}(\omega_o t - \pi) \tag{3.60}$$

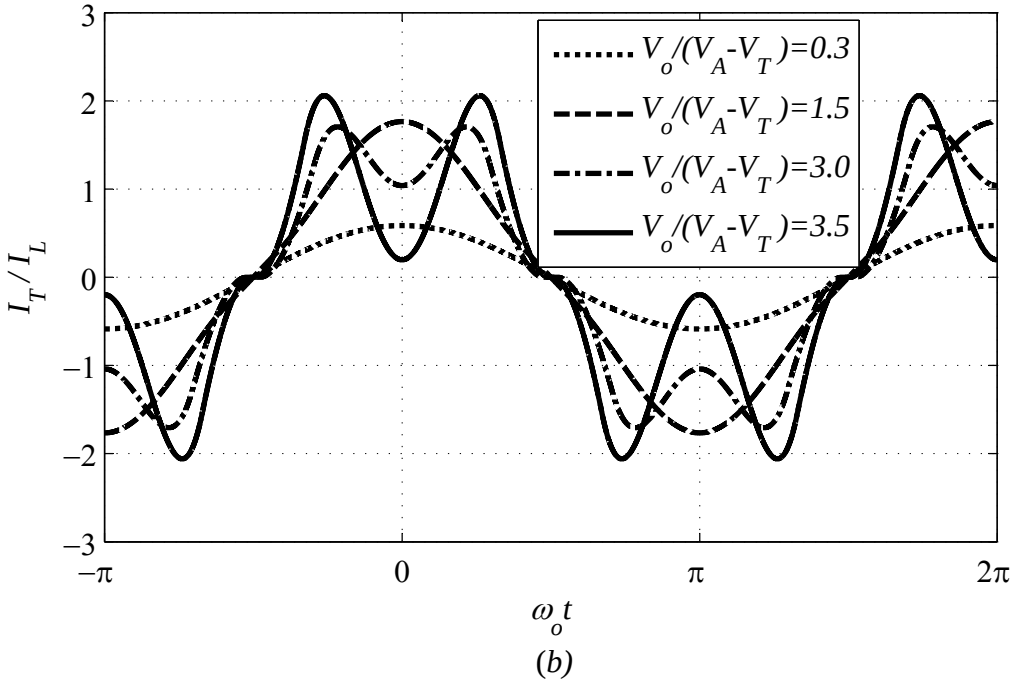
where I_D/I_L is given by (numerically) solving (3.52), as described earlier.

Figs. 3.28(a) and 3.28(b) show solutions of I_T/I_L for several values of $V_o/(V_A - V_T)$ for N/PMOS (Fig. 3.24) and CMOS (Fig. 3.27) configurations, respectively. Finally, given that (3.52) is the time-domain solution for I_D/I_L, its Fourier transform thus provides the harmonic components, from which the VCO output swing V_{od} can be calculated.

Figs. 3.29 and 3.30 yield powerful insight into the nonlinear mechanism setting the output amplitude. Worth noting is that these plots not only avoid technology dependent



(a)



(b)

Figure 3.28: I_T/I_L vs. $\omega_o t$ for different values of $V_o/(V_A - V_T)$ and $V_T/(V_A - V_T) = 3.6$ for N/PMOS (a) and CMOS (b) configurations.

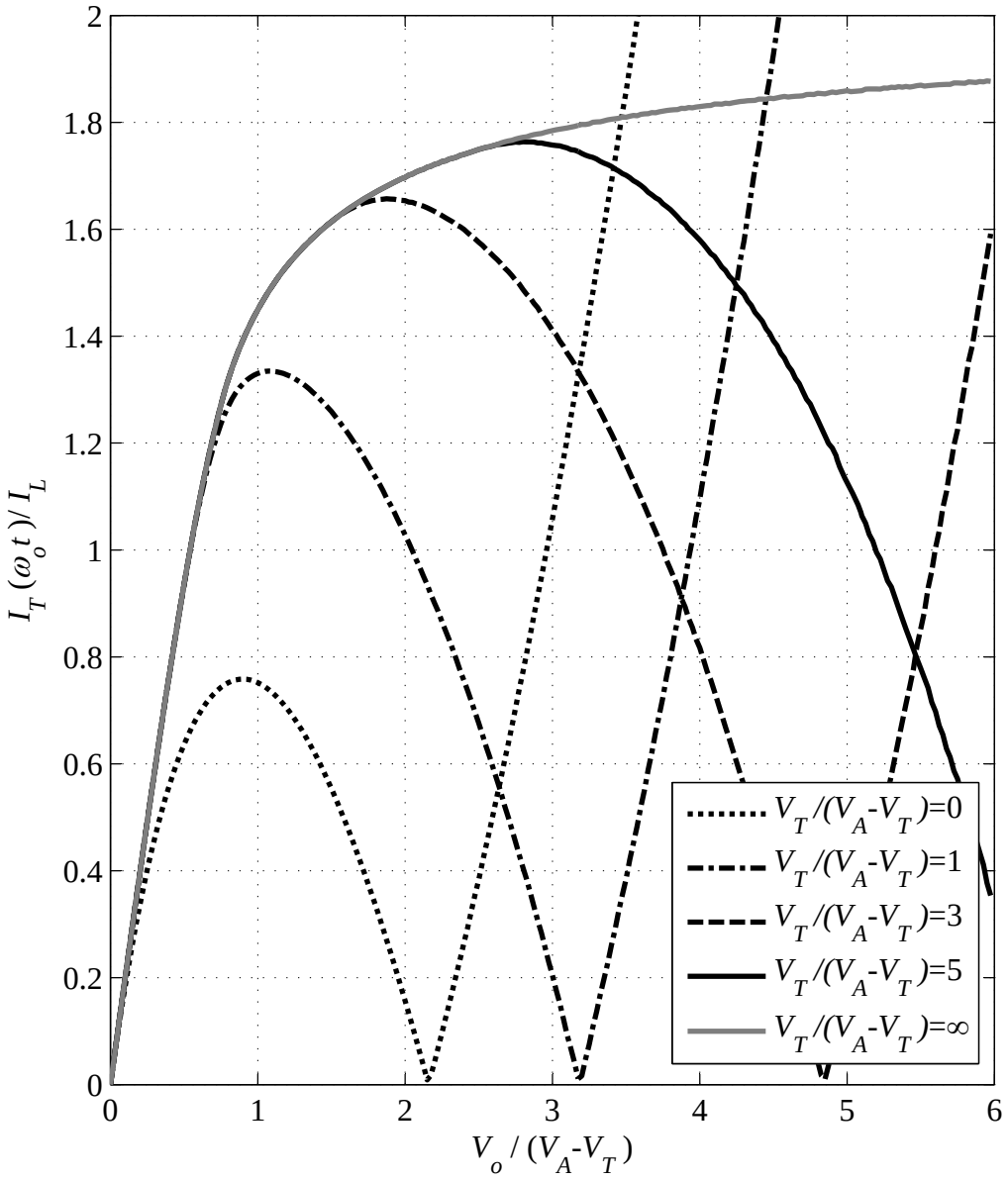


Figure 3.29: $|I_T(\omega_o)|/I_L$ vs. $V_o/(V_A - V_T)$ for the N/PMOS configurations shown in Fig. 3.24, for different values of $V_T/(V_A - V_T)$.

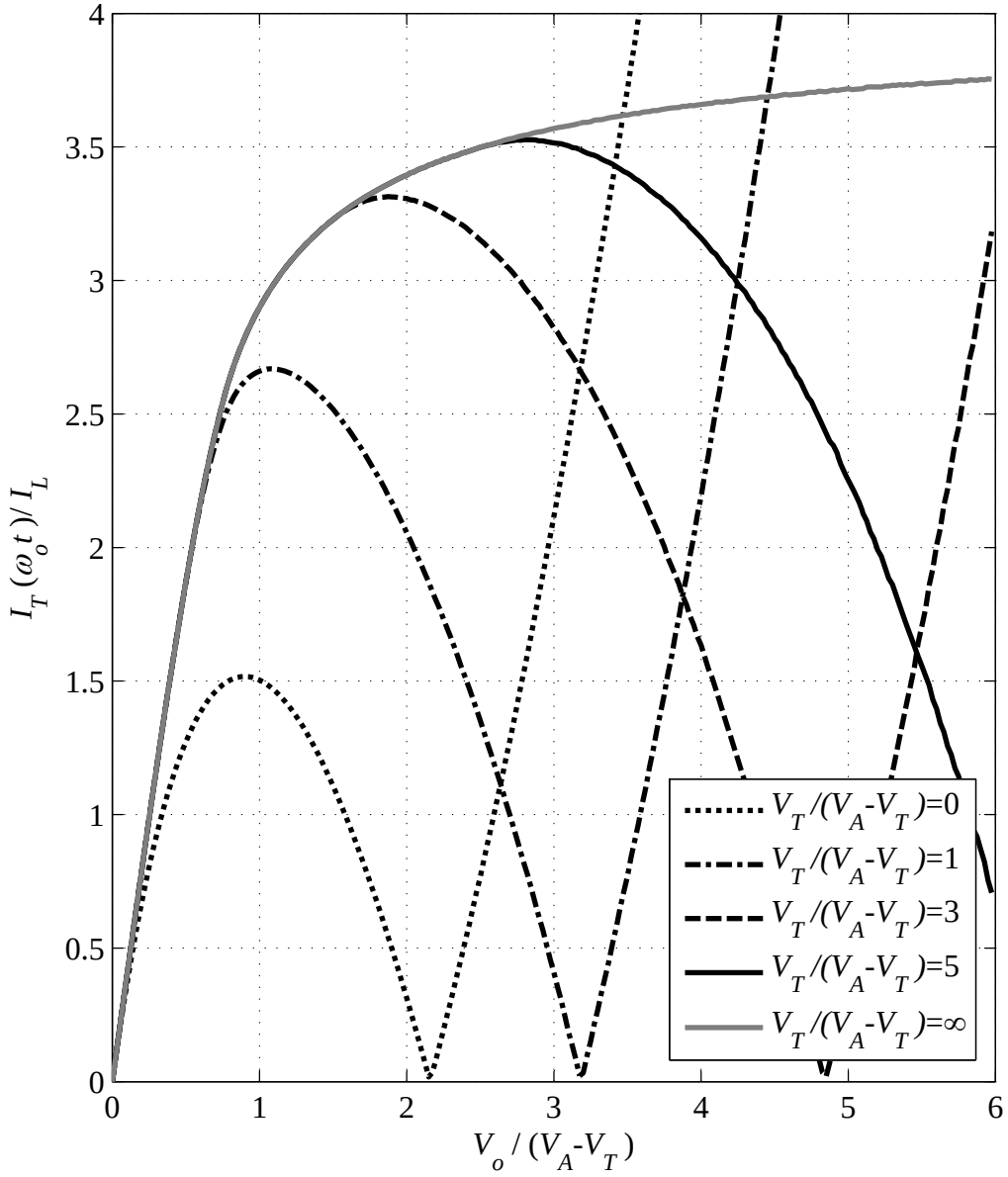


Figure 3.30: $|I_T(\omega_o)|/I_L$ vs. $V_o/(V_A - V_T)$ for the CMOS configuration shown in Figs. 3.27, for different values of $V_T/(V_A - V_T)$.

terms (except for V_T), they also exclude device sizes (as this is embodied via $V_A - V_T$). Hence the generality of such curves makes them applicable to designing such VCOs in any technology, where one only has to consider the desired output swing V_o and device threshold voltage V_T relative to the amount of overdrive $V_A - V_T$. However, while this is true for any device well approximated by a square-law I-V characteristic, designs based on short-channel devices do not precisely follow the above curves. This is mainly because velocity-saturation (due to the high lateral field across the channel) and mobility degradation (due to the high vertical field across the gate oxide) distort the square-law relationship assumed in the above derivations.

Fig. 3.31 compares calculated and simulated curves for an NMOS tail-biased reference design. As expected, some differences exist. For example, the simulated curve does not quite reach zero at its local minimum, and does so at a slightly higher value of $V_o/(V_A - V_T)$ than that of the calculated curve. Nevertheless, the strong similarity of the curves' behavior suggests that even a simple square-law model can provide a decent approximation for a design using short-channel devices.

Including short-channel effects complicates such derivations in the sense that additional variables must be included (e.g. channel length) and make it difficult to arrive at general 2-D curves like those shown in Figs. 3.29 and 3.30. Thus, for short-channel implementations, simulations tools will be better suited for the design process. However, the above derivations and resulting curves still provide good insight into the basic trends that set the output amplitude (and its harmonics).

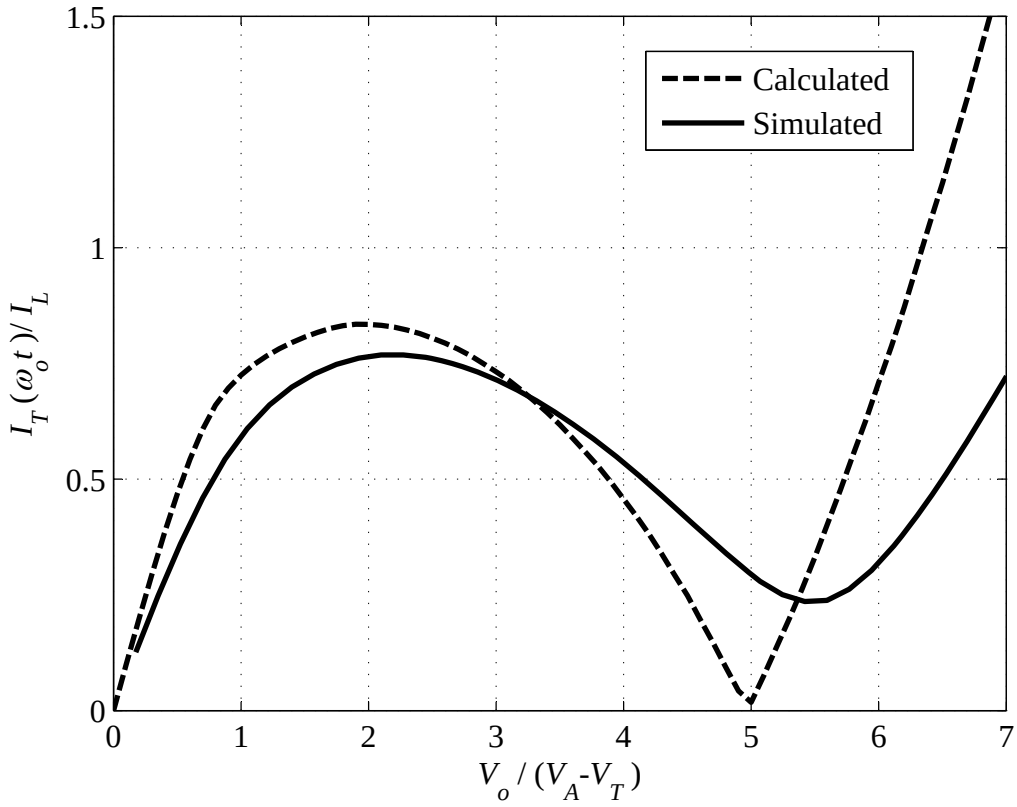


Figure 3.31: Calculated and simulated $|I_T(\omega_o)|/I_L$ vs. $V_o/(V_A - V_T)$ for the NMOS tail-biased configuration shown in Figs. 3.18(a), for $V_T/(V_A - V_T) \approx 3$, where $V_T = 0.45$V and $V_A \approx 0.6$V.

3.7 Phase Noise Performance

In light of the analysis presented in Section 3.5, the noise performance of the three basic configurations can be discussed on a first-order basis. Our discussion will assume that for each case, devices are sized to provide just enough g_m to ensure startup. As before, the three configurations use an identical LC tank and supply voltage. Having identical LC tanks and equal g_m, the $\overline{i_n^2}$ term in (3.27) will be approximately the same for each configuration. Then, the only parameter setting them apart in terms of phase noise performance is V_o, as can be seen from (3.27).

Using the voltage swing characteristics described in the previous section, we can qualitatively assess the phase noise performance of each configuration. From Fig. 3.21, it is clear that the complementary tail-biased topology is the best if relatively low voltage swings are intended ($V_{od} < 1.5$V). In such cases, the complementary configuration will produce a larger voltage swing for a given I_{ss} (and g_m). If however, lower phase noise must be achieved such that a higher swing is needed, then the other two configurations perform better since they can achieve higher V_{od} for a given I_{ss} (and g_m). Thus, we may say that the complementary topology is best suited for low-power applications, whereas the tail- or top-biased N/PMOS topologies are better for high-performance applications.

Our observations have been validated with accurate periodic-steady-state (PSS) noise simulations (SpectreRF [67]). The results are plotted in Fig. 3.32, showing the simulated single-sideband phase noise at 0.1 and 1MHz frequency offsets, as a function of

I_{ss} for each of the three basic configurations shown in Fig. 3.18. The cross-coupled device sizes have been adjusted at each value of I_{ss} to keep g_m constant over the simulated range. As expected, the resulting phase noise trends are consistent with our predictions. At low bias current levels, the complementary configuration produces higher swing, and thus achieves better phase noise. Above $I_{ss} \approx$ 3-4mA, the other two topologies perform better since their swing grows beyond that of the CMOS configuration. Again, the slight difference in the tail- and top-biased configurations stems only from the fact that M_T saturates somewhat earlier (thus limiting the swing) in the latter. M_T could have been sized to yield equal swing, and thus more similar phase noise performance for both, but this was deliberately avoided to highlight its effect on phase noise.

3.8 Summary

This chapter covered key concepts of basic *LC* VCOs. To avoid loss of generality, some of the topics discussed were kept at a simplified level, sometimes purposely avoiding second-order considerations. In practice and depending on the particular topology at hand, it is not uncommon for such effects to have a noticeable impact. Thus in some cases, it is expected that additional considerations would need to be taken into account. Furthermore, whereas our discussion has focused on major performance aspects, other parameters which were not discussed can sometimes be important as well. For example, a VCO's sensitivity to the supply voltage (i.e. $\partial f_o/\partial V_{DD}$), also known as supply pushing, is often critical. Lastly, we note that the three configurations of Fig. 3.18 may

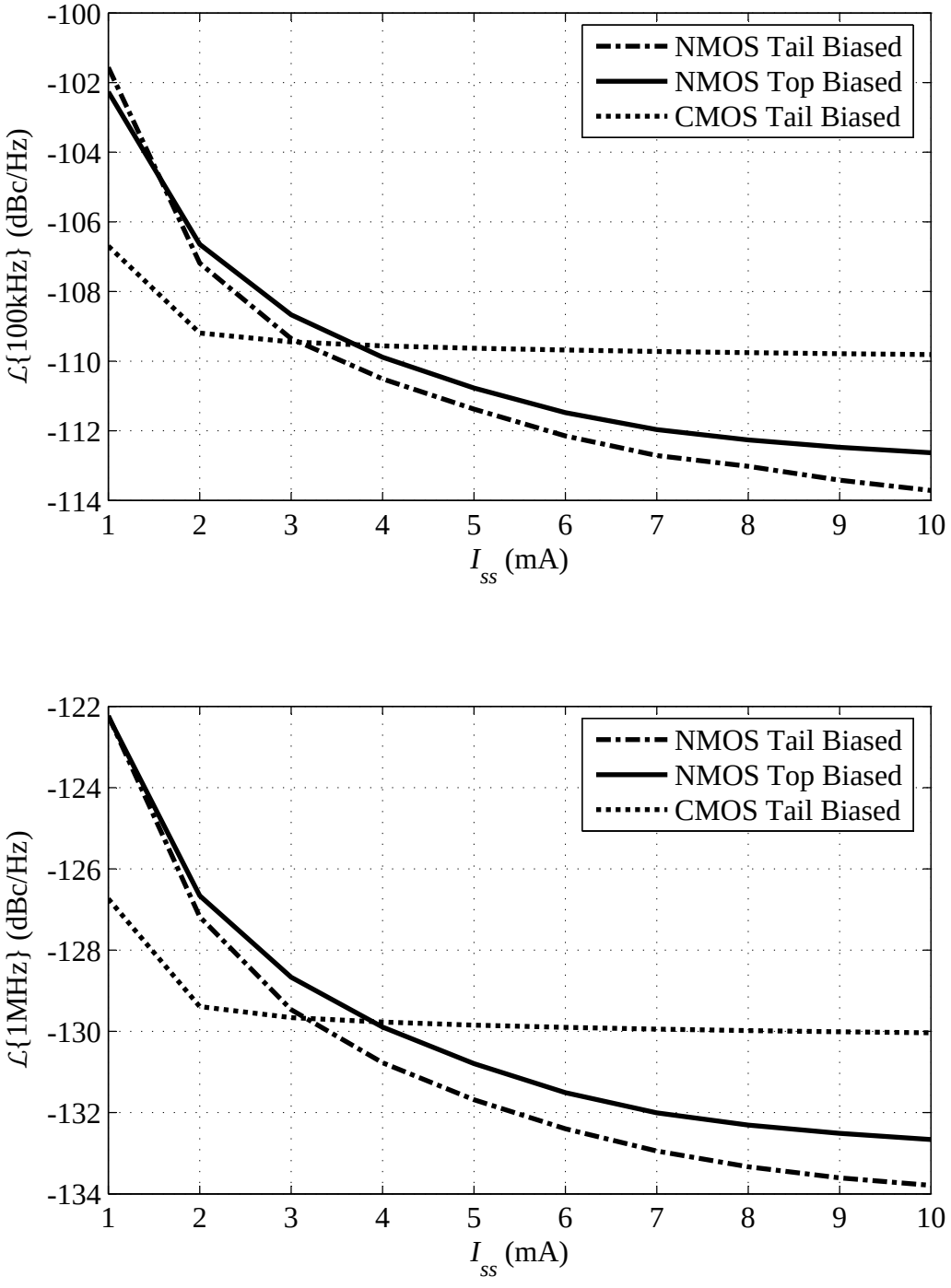


Figure 3.32: Simulated Phase Noise at 0.1- and 1-MHz offsets, for each of the three basic configurations (Fig. 3.18), resized at each value of I_{ss} to keep g_m constant.

be modified to alleviate or change the tradeoffs and characteristics we have described. In such cases, although the results may differ, the same approach may be used to gain insight for how one topology may compare to another.

Chapter 4

Analysis and Design of Wideband *LC* VCOs

4.1 Introduction

The VCO performance in terms of phase noise, tuning range, and power dissipation determines many of the basic performance characteristics of a transceiver. The current trend towards multi-band multi-standard transceivers and broadband systems has generated interest in VCOs that simultaneously achieve very wide tuning range and low phase noise performance [63, 68–75]. Whereas relaxation oscillators easily achieve very wide tuning range (i.e. 100% or more), their poor phase noise performance disqualifies them in most of today's wireless and wireline applications. Because *LC* VCOs have been successfully used in narrowband wireless transceivers, there is a growing interest in

extending their tuning range. Recently, several wideband CMOS LC VCOs have been demonstrated using a variety of techniques [68–71]. The high intrinsic $C_{v,\max}/C_{v,\min}$ of inversion- or accumulation-type MOS varactors supports a very wide tuning range and their Q is sufficiently high that good phase noise performance can be maintained [70]. However in practice, the overall phase noise performance is also highly dependent on the tuning sensitivity of the VCO, since noise from preceding stages of the frequency synthesizer is inevitably injected onto the VCO control input. Hence, aside from achieving a high basic tuning range, practical wideband VCO solutions must also control the overall VCO tuning sensitivity. Furthermore since the tank amplitude of most LC VCOs to first order changes with the square of frequency, practical implementations must often provide some way to stabilize this parameter. However, conventional amplitude control schemes that use continuous feedback methods are plagued by intrinsic noise feeding back to the oscillator [75–77].

4.2 Design Considerations for Wideband LC VCOs

4.2.1 Frequency Dependence of Start-up Constraints

In Chapter 3, start-up conditions were discussed assuming a single frequency of operation. Thus, frequency dependencies were not made explicit. For wideband VCOs, such dependencies must be considered.

The equivalent parallel tank impedance at resonance R_T is a strong function of the

oscillation frequency ω_o and inductance L, and is given by (Section 3.2.1):

$$R_T(\omega_o) = Q_T \cdot \omega_o \cdot L = \frac{(\omega_o \cdot L)^2}{r_s} \tag{4.1}$$

where the overall tank quality factor Q_T is assumed to be dominated by inductor losses characterized here by the physical series resistance r_s of the coil, which itself eventually becomes of function of frequency when skin/proximity effects begin affecting the structure. Furthermore, substrate losses typically accompany these effects and can be approximated by a corresponding increase in r_s. The validity of the above approximation is not compromised as long as the capacitive elements of the tank have a significantly higher Q than the inductor, which may not hold true at very high frequencies ($f_o > 10$GHz). Fig. 4.1 shows the simulated equivalent tank conductance of a typical LC tank versus that given by the reciprocal of (4.1). This simulation is based on the same (measurement-based) inductor model used in the simulations discussed in Chapter 3. It can be seen that (4.1) is indeed a good approximation over the selected 3:1 range of frequencies.

For any oscillator, the most fundamental design criterion consists of satisfying start-up conditions. In tunable LC oscillators, these conditions are themselves a function of frequency [72]. As seen in Section 3.3, such conditions are satisfied if the pair of complex conjugate poles of the small-signal (initial) loop-gain transfer function lies in the right-half of the s-plane which occurs when the magnitude of the loop-gain is greater

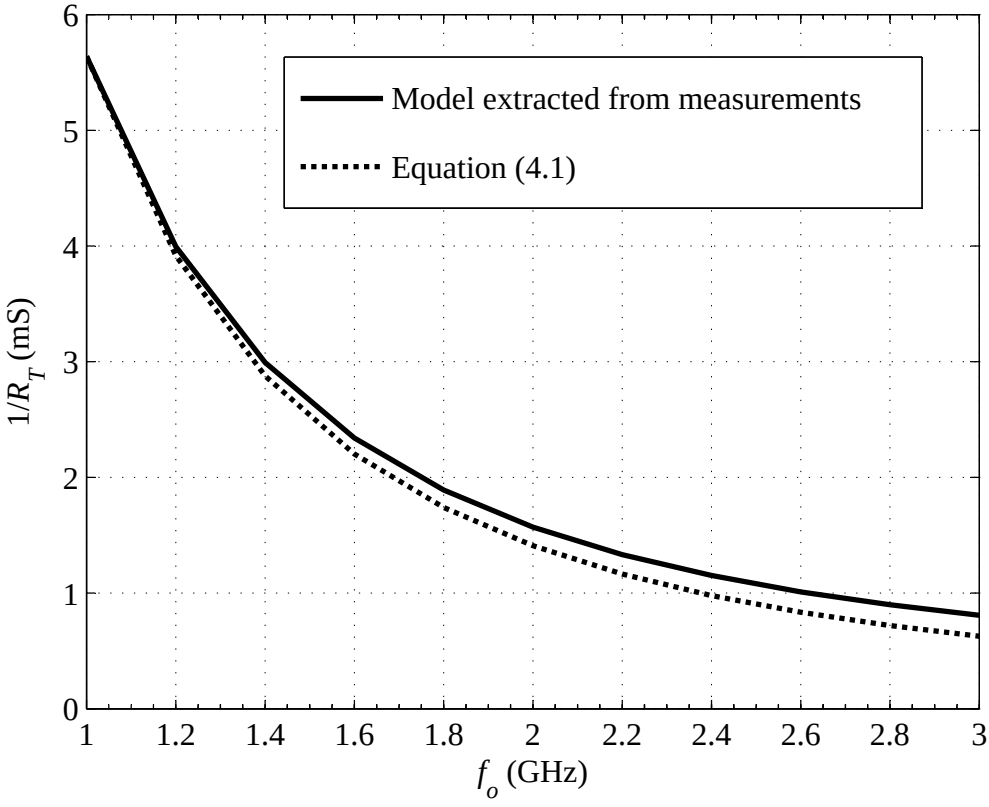


Figure 4.1: $1/R_T$ vs. f_o of typical LC tank obtained using a physical inductor model compared to that obtained using (4.1).

than unity. Substituting (4.1) into (3.16), we obtain:

$$G_m \geq \frac{1}{R_T} = \frac{r_s}{(\omega_o \cdot L)^2} \tag{4.2}$$

Equation (4.2) indicates a fundamental lower limit on the power consumption for a given transconductor and LC tank configuration. Moreover, the pronounced frequency dependence in (4.2) indicates that the worse-case scenario occurs at the low-end of the desired frequency range. In practice, G_m is set to a value that guarantees startup with a reasonable safety margin under worst-case conditions. Increasing G_m beyond this critical value generally contributes more parasitics (larger device) and noise and is thus undesirable. As frequency increases, the corresponding increase in R_T lessens the required G_m. Thus, wideband VCOs using transconductors fixed at a predetermined critical value feature significant excess-of-G_m in the upper portion of their frequency range.

4.2.2 Frequency Dependence of LC Tank Amplitude

The steady-state oscillation amplitude is an important design characteristic of oscillators, and can also have a significant impact on neighboring system blocks. As discussed in Chapter 3, the amplitude of an LC oscillator is reached by some nonlinear limiting mechanism forcing the steady-state loop gain to unity. For the widely used differential cross-coupled LC oscillator shown in Fig. 4.2, two such regimes can be discerned (Section 3.6.2.1). In the current-limited regime, the current I_{ss} from the tail current source is periodically commutated between the left and right sides of the tank. As pointed out

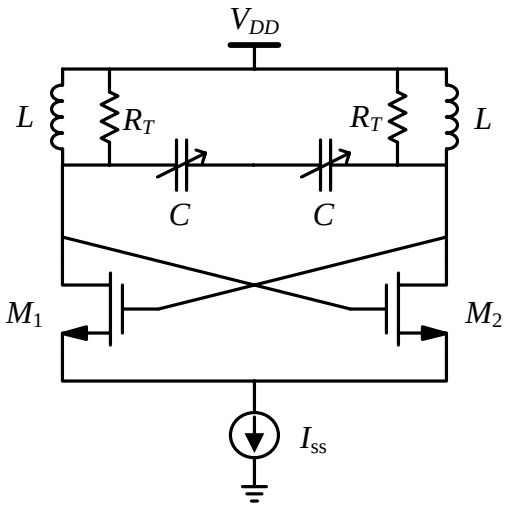


Figure 4.2: Differential cross-coupled NMOS tail-biased LC VCO.

in Section 3.6.2.2, the actual behavior is more complicated than a simple current commutation. However, assuming a simpler scenario as in Section 3.6.2.1 will help simply our discussion. Thus, the resulting fundamental amplitude is approximated as being proportional to I_{ss} and R_T, whereas higher harmonics of the commutated current are shunted to ground via capacitors in the tank. As I_{ss} is increased from its minimum value satisfying start-up conditions, the tank amplitude increases linearly. Eventually, the amplitude compresses to a plateau dictated by the available headroom from the supply voltage. This $V_o - I_{ss}$ characteristic was previously illustrated in Fig. 3.19 and is repeated here in Fig. 4.3(a) for clarity.

In wideband VCOs, large variations in R_T with frequency (see (4.1)) can also cause a transition from the current- to the voltage-limited regime as frequency increases. Although I_{ss} has not been increased to cause this transition, power is now being wasted

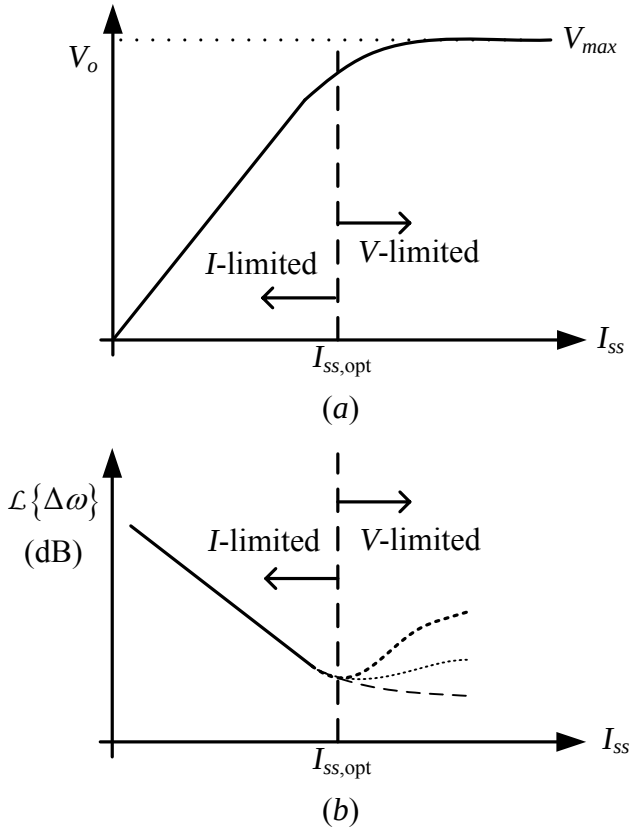


Figure 4.3: (*a*) V_o vs. I_{ss} and (b) $\mathcal{L}\{\Delta\omega\}$ vs. I_{ss}, across current- and voltage-limited regimes.

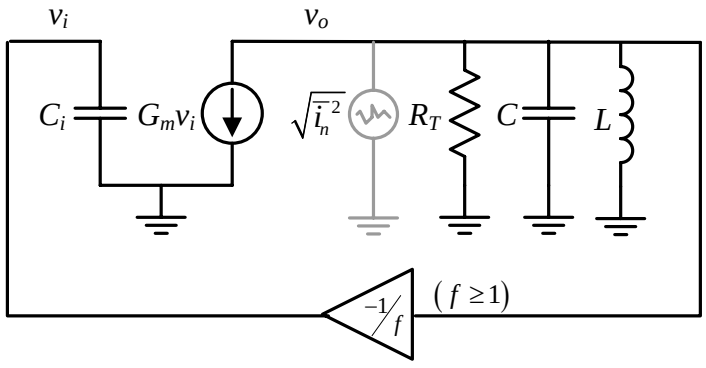


Figure 4.4: Generic *LC* oscillator with equivalent noise source $\overline{i_n^2}$.

in the sense that I_{ss} could be reduced without impairing the output swing of the VCO.

To gain insight into the impact of oscillation amplitude variations on phase noise, we consider phase noise in the simplified linear time-invariant LC oscillator illustrated in Fig. 4.4, as discussed in Section 3.5. Equation (3.27) is rewritten as:

$$\begin{aligned} \mathcal{L}\{\Delta\omega\} &\approx \frac{\overline{i_n^2}/\Delta f}{V_o^2} \cdot \frac{R_T^2}{4Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \\ &\propto \frac{G_m + 1/R_T}{V_o^2} \cdot \frac{R_T^2}{Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \end{aligned} \tag{4.3}$$

where $(G_m + 1/R_T)$ has been substituted, implying that noise generators from the energy-restoring transconductor (G_m) and from the tank loss (R_T) dominate, as is usually the case. V_o is the tank amplitude and $\Delta\omega$ is the frequency offset from the carrier ω_o. Further insight is gained by considering (4.3) across the two different regimes of operation described earlier. In the current-limited regime where $V_o = I_{ss}R_T$, (4.3) can be rewritten as follows:

$$\mathcal{L}\{\Delta\omega\} \propto \frac{G_m + 1/R_T}{I_{ss}^2} \cdot \frac{1}{Q_T^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{4.4}$$

For narrowband designs, R_T does not vary appreciably over the tuning range and thus $G_m = \alpha/R_T$ where α is a chosen start-up safety margin. Under these conditions, phase noise shows a $1/(Q_T^3 L)$ dependence. While this highlights the importance of Q_T, a careful optimization should consider Q_T as a function of L for the chosen technology and area constrains, as discussed in [69]. Also apparent in (4.4) is the direct relationship between bias current and phase noise, which provides the designer with a convenient way to trade power for noise performance. Furthermore, (4.4) can be expressed more

generally by substituting $|I_T(\omega_o)|$ for I_{ss} (see (3.20)).

In the voltage-limited regime, (4.3) can be rewritten as follows:

$$\mathcal{L}\{\Delta\omega\} \propto \frac{G_m + 1/R_T}{V_{\max}^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{4.5}$$

For narrowband designs operating in the voltage-limited regime, (4.5) indicates that phase noise cannot be improved by increasing I_{ss}. On the contrary, in some cases the phase noise may degrade as the VCO enters the voltage-limited regime [69, 78, 79]. As discussed in Section 3.6.2.1, the boundary between the two regimes of operation represents an optimum point in terms of phase noise performance per current consumption. As shown in Fig. 4.3(b), increasing I_{ss} beyond this point not only wastes power but may also degrade phase noise.

While the above observations yield important insights for narrowband designs, frequency dependencies must be taken into account in order to assess such characteristics for wideband VCOs. Here, we restrict our analysis to the current-limited regime since it is the preferred region of operation, as discussed earlier. Again starting from (4.3), a phase noise expression highlighting its frequency dependence is derived assuming a fixed current I_{ss}:

$$\mathcal{L}\{\Delta\omega\} \propto \left(\frac{G_m}{I_{ss}^2} + \frac{r_s}{(\omega_o L)^2}\right) \cdot \frac{r_s}{L^2} \tag{4.6}$$

Equation (4.6) reveals a somewhat counter-intuitive result: phase noise tends to improve as the VCO is tuned to higher frequencies. Even in cases where r_s grows linearly with frequency (equivalent to a flattening of Q_T with frequency), equation (4.6) shows

that phase noise is relatively constant with frequency. The reason that phase noise does not degrade with its classical ω_o^2 dependence is that the tank amplitude in this particular topology basically grows with ω_o^2. However, (4.6) only applies in the current-limited regime. Wideband designs operated with fixed I_{ss} experience significant amplitude growth as frequency increases, which eventually brings the VCO into its voltage-limited regime where phase noise is known to degrade [69, 78, 79]. In other words, the optimal point for lowest phase noise indicated in Fig. 4.3(b) cannot be held across frequency.

Amplitude variations in wideband VCOs cause several additional second-order effects which may be of concern, depending on the application. One such effect is the effective reduction of the varactor's capacitive range ($C_{v,\max}/C_{v,\min}$) and the associated reduction in the overall tuning sensitivity, which was previously shown in Fig. 3.12. Although the corresponding reduction of the tuning range can be accounted for and compensated, amplitude-dependent variations of the tuning sensitivity need to be addressed in the design of the frequency synthesizer (see Chapter 2). Other effects generally relate to how amplitude variations affect neighboring blocks in the system. One such example is a mixer, for which the conversion gain varies as a function of the VCO amplitude. Overall, it can be concluded that providing some way to control the frequency dependence of VCO performance is desirable.

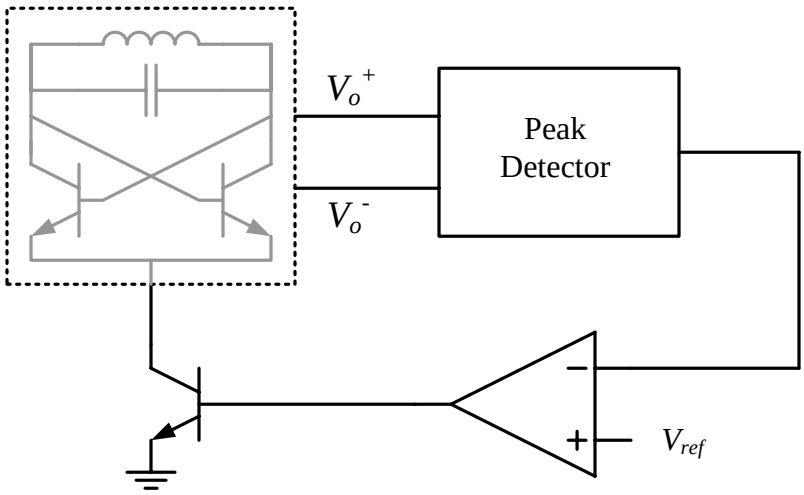


Figure 4.5: Conventional continuous-time automatic amplitude control (AAC) loop.

4.3 Amplitude Control

4.3.1 Conventional Continuous-time Amplitude Control

As discussed in the previous sections, the tank impedance variations present in wide-band designs significantly affect the VCO operation and cannot be ignored. Methods to address this issue typically consist of some form of amplitude control. A conventional method of controlling the amplitude of a VCO is by means of an automatic amplitude control (AAC) loop [76,77] and is depicted in Fig. 4.5. The feedback loop provides very accurate control of the amplitude and at the same time guarantees startup. As with all feedback systems, great care must be taken to ensure that the loop remains stable under all operating conditions. Furthermore, the presence of additional noise generators in the loop can significantly degrade the phase noise performance.

4.3.2 Proposed Digital Amplitude Control

In this work, we propose an alternative amplitude control scheme to alleviate the deficiencies inherent in the conventional approach. Instead of a continuous feedback loop, a calibration approach is used as shown in Fig. 4.6. The VCO amplitude is first peak detected and compared to a programmable reference voltage setting the desired amplitude. The output of the comparator is analyzed by a simple digital state machine that decides whether to update the programmable bias current of the VCO or to end calibration. This method has the advantage of being active only during calibration. Thus, the steady-state phase noise performance of the VCO is not affected. In addition, the power consumed by calibration circuits is negligible since they are powered off as soon as calibration ends. While a constant-amplitude vs. frequency calibration is an intuitive choice, the fully-programmable nature of this method can be exploited to implement more intricate application-specific calibration scenarios. For a constant-amplitude scenario where I_{ss} is scaled with frequency, (4.3) can be rewritten to show the resulting phase noise vs. frequency trend:

$$\mathcal{L}(\omega_o) \propto \sqrt{\beta_T V_o r_s} \cdot L^2 \omega_o^3 + r_s \omega_o^2 \tag{4.7}$$

where $\sqrt{\beta_T I_{ss}}$ has been substituted for G_m and $V_o = I_{ss} R_T$. If r_s is approximately constant over the frequency range and transconductor noise dominates, (4.7) indicates a 9dB/octave trend.

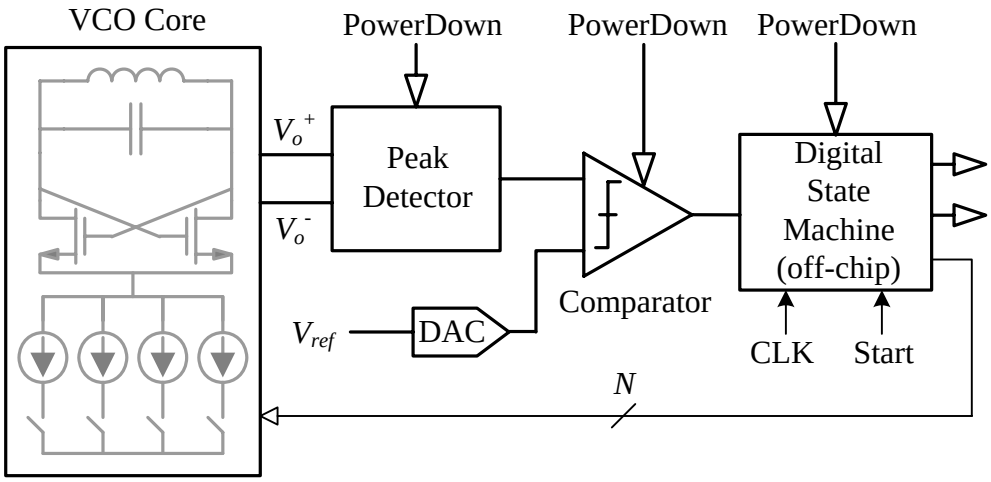


Figure 4.6: Proposed calibration-based amplitude control scheme.

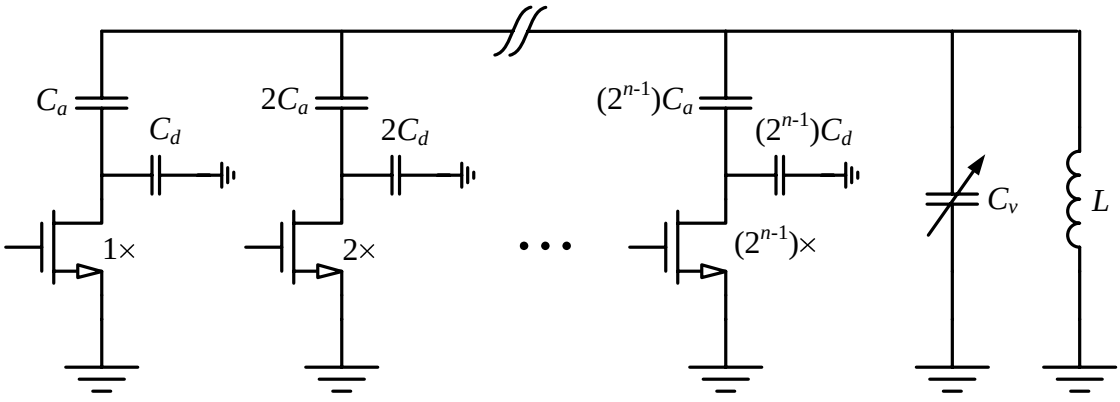


Figure 4.7: Generic binary-weighted band-switching LC tank configuration.

4.4 Tuning Range Analysis

One of the main challenges of wideband low-phase-noise LC VCO design consists of expanding an intrinsically narrow tuning range without significantly degrading noise performance or incurring excessive tuning sensitivity. In recent years, band-switching techniques have been used extensively. Inherently well adapted to the scaling of MOS technology, these techniques have proved to be successful ways to increase tuning range and/or decrease tuning sensitivity [70, 72, 80].

The following analysis is based on a generic binary-weighted band-switching LC tank configuration of size n, as shown in Fig. 4.7 [81]. The following definitions are used in subsequent derivations:

$$\beta_v = \frac{C_v}{C_{v,\min}} \tag{4.8}$$

$$\beta_a = \frac{C_a}{C_{a,\text{off}}} \tag{4.9}$$

$$\beta_p = \frac{C_{total}}{C_p} \tag{4.10}$$

$C_{v,\min}$ is the minimum varactor capacitance for the available tuning voltage range and is reached as the device enters its depletion mode. $C_{a,\text{off}}$ represents the effective capacitance of a unit branch of the array in the off state. The MOS switch in a unit branch of the array contributes a parasitic capacitance C_d that is mainly composed of its drain-to-bulk junction and drain-to-gate overlap capacitors, giving $\beta_a = 1 + C_a/C_d$. Note that if coarse-tuned varactors are used instead of switched capacitors (see [70]), β_a retains the same meaning. C_p is the total lumped parasitic capacitance and C_{total} equals the total

tank capacitance. Hence (4.10) may be equivalently expressed as $\beta_p = 1/(\omega_{o,\min}^2 LC_p)$. Furthermore, note that according to equations (4.8)−(4.10), increasing any one of the defined terms increases the achievable tuning range.

For a given set of specifications, the tuning range extremities are defined as follows:

$$\omega_{o,\min} = [L \cdot (C_v + (2^n - 1) \cdot C_a + C_p)]^{1/2} \tag{4.11}$$

$$\omega_{o,\max} = \left[L \cdot \left(\frac{C_v}{\beta_v} + (2^n - 1) \cdot \frac{C_a}{\beta_a} + C_p\right)\right]^{1/2} \tag{4.12}$$

As shown in Appendix A, in order for any two adjacent sub-bands overlap, the following condition must be satisfied:

$$\Delta C_v \geq \Delta C_a \tag{4.13}$$

where $C_v = C_v - C_{v,\min}$ and $C_a = C_a - C_{a,\text{off}}$. Using (4.8) and (4.9), (4.13) can be rewritten as:

$$C_v = k \cdot C_a \cdot \frac{\beta_v}{\beta_a} \cdot \frac{\beta_a - 1}{\beta_v - 1} \tag{4.14}$$

where k is a chosen overlap safety margin factor and is greater than unity. As shown in Appendix A, this corresponds to a frequency band overlap of approximately $(k-1)/k$ percent. Equation (4.14) can be substituted in (4.11) to solve for C_a independently of C_v, giving:

$$C_a = \frac{\left(L\omega_{o,\min}^2\right)^{-1} - C_p}{k \cdot \frac{\beta_v}{\beta_a} \cdot \frac{\beta_a - 1}{\beta_v - 1} + 2^n - 1} \tag{4.15}$$

Thus, having chosen parameters β_a, n, and L, and given design constants $\omega_{o,\min}$, k, and β_v, one can solve for C_a and C_v (using (4.14)). Considerations in choosing these parameters are discussed in subsequent paragraphs.

Taking the ratio of (4.12) and (4.12) yields the tuning range TR as a function of only β values, k, and n:

$$TR = \frac{\omega_{o,\max}}{\omega_{o,\min}} = \sqrt{\frac{\left[k \cdot \frac{\beta_v}{\beta_a} \cdot \frac{\beta_a - 1}{\beta_v - 1} + 2^n - 1\right] \cdot \left(1 + \frac{1}{\beta_p}\right)}{\left[k \cdot \frac{\beta_v}{\beta_a} \cdot \frac{\beta_a - 1}{\beta_v - 1}\right] \cdot \left(\frac{1}{\beta_v} + \frac{1}{\beta_p}\right) + (2^n - 1) \cdot \left(\frac{1}{\beta_a} + \frac{1}{\beta_p}\right)}} \tag{4.16}$$

To be able to quantify the impact of lossy switches, we note that the quality factor of the capacitor array is well approximated as $Q_a = 1/(\omega_o R_{on} C_a)$, where R_{on} is the on resistance of the unit MOS switch. Given that $\beta_a = 1 + C_a/C_d$, the resulting quality factor of the capacitor array is given by:

$$Q_a = \frac{1}{\omega_o R_{on} C_d \cdot (\beta_a - 1)} \tag{4.17}$$

Note that since the MOS switch would generally use the minimum available gate length and $C_d \propto W$, the product $R_{on}C_d$ is approximately constant for a given technology. Fig. 4.8(a) shows values of TR and Q_a from equations (4.16) and (4.17) plotted vs. β_a for a typical scenario, and clearly illustrates the direct tradeoff between tuning range and Q_a. As the MOS switches are made larger to decrease their resistance, their off-state parasitic capacitance grows proportionally thus reducing the tuning range.

Furthermore, (4.17) is substituted into (4.16), and the resulting expression is plotted in Fig. 4.8(b). Hence, Fig. 4.8(b) gives the tuning range TR as a function of Q_a, for given technology constants ($R_{on}C_d$ and β_v), chosen safety factor k, and design parameters n, and β_p. The practical significance of Fig. 4.8(b) lies in its ability to quantify the fundamental tradeoff between phase noise and tuning range. For instance, a design aiming to achieve a 2 : 1 tuning range while using an inductor with Q_L =15, would

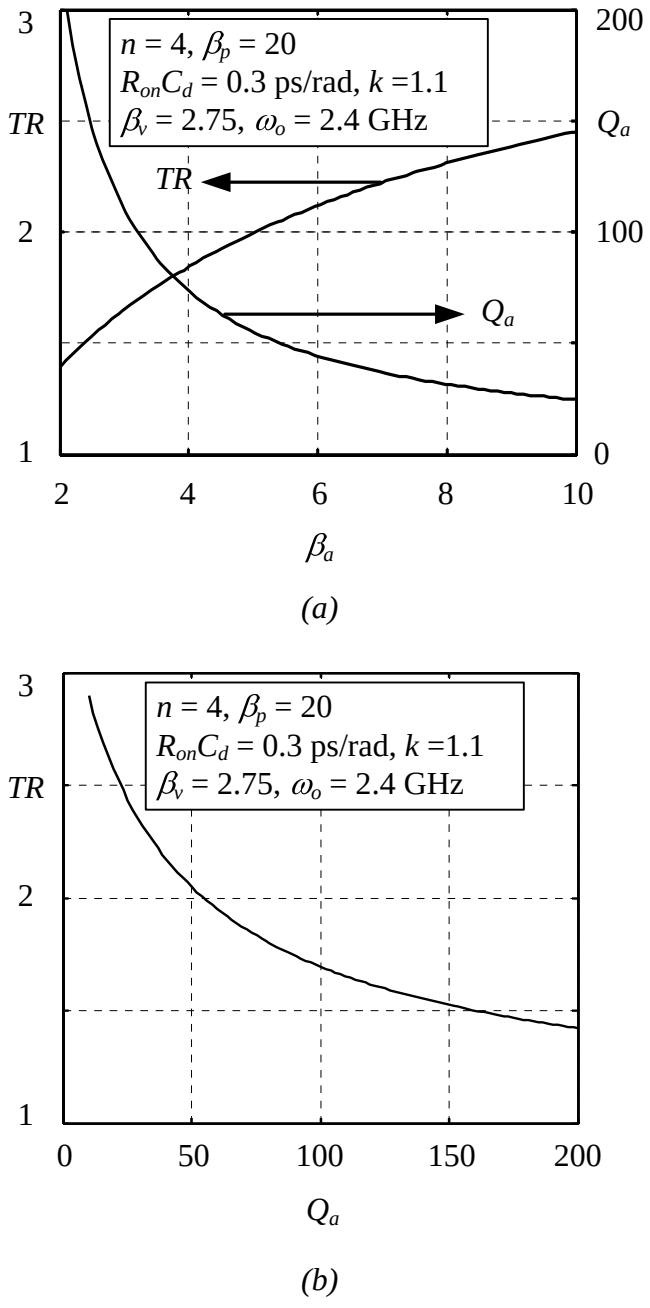
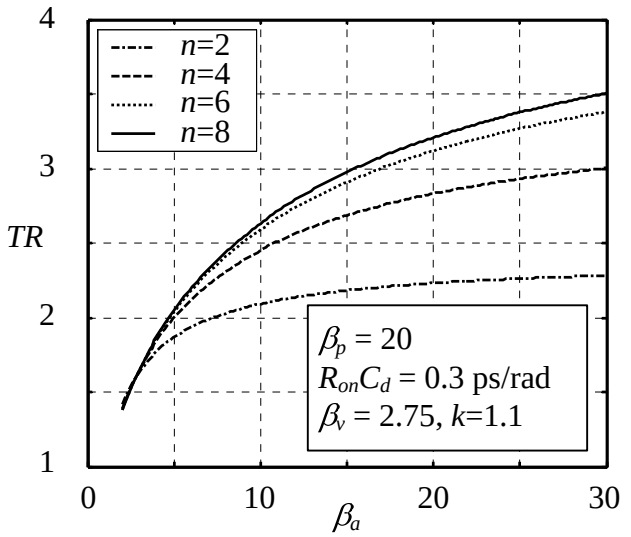


Figure 4.8: (a) Tuning range TR and capacitor array quality factor Q_a vs. L. (b) TR vs. Q_a.

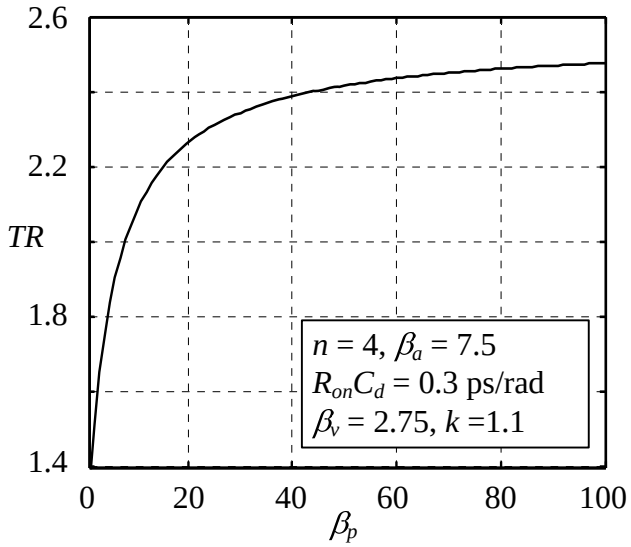
reduce the overall Q_T by about 20% (i.e. β_a =5) and thus increase the phase noise by approximately 2dB (all evaluated at 2.4GHz).

Another important design parameter of the band-switching configuration is the array size n (i.e. the number of bits making up the binary-weighted array). As one would suspect, adding more bits to the array is beneficial to the tuning range but only to a certain degree. Beyond a certain point, the minimum fixed capacitance in the design prevents any further improvement. To gain better insight for this trend, equation (4.16) is plotted for different values of n and shown in Fig. 4.9(a). From Fig. 4.9(a), it is clear that the improvement in TR from increasing n quickly saturates, especially in the useful range of β_a (i.e. low values of a corresponding to high values of Q_a). Nevertheless, increasing n still yields a proportional decrease in the tuning sensitivity. In practice, this benefit needs to be weighed against the time needed to calibrate the additional bits.

Finally, the inductance also plays a critical role for the achievable tuning range. Although this dependence may not be clear from (4.16), recall that $\beta_p = 1/(\omega_{o,\min}^2 LC_p)$. Fig. 4.9($b$) shows a typical plot of (4.16) as a function of β_p. However, a strategy for choosing the optimal inductance is difficult to generalize, as several conflicting performance tradeoffs are involved. In particular, the start-up constraint described by (4.2) gives $I_{ss} \propto 1/(Q_T L)^2$, which indicates that a large inductance is preferred in terms of power consumption. Note that although this is usually true, it may not be the case in situations where the inductor quality factor varies significantly over the considered



(a)



(b)

Figure 4.9: (a) Tuning range TR vs. β_a for different numbers of bits (n) in the capacitor array. (b) TR vs. β_p.

range of inductance. Furthermore, recall that phase noise is proportional to $1/(Q_T^3 L)$ in the current limited regime. While this may seem to favor a larger inductance as well, the dependence between the inductor's quality factor and its inductance must now be taken into account. Even if this dependence is relatively weak in many cases, the cubic term can quickly make a significant difference on phase noise. In summary, finding the optimal inductance for a given design ultimately depends on which constraints are most important to the intended application.

Chapter 5

A Wideband *LC* VCO Prototype

5.1 Introduction

In this chapter, we present the implementation of a wideband *LC* VCO prototype and provide experimental results that demonstrate the concepts described in previous chapters [82]. The prototype is implemented in a standard 0.18μm bulk CMOS process. The only Analog/RF options used are MIM capacitors and a 2μm thick Al top metal layer. To save time and allow a high-degree of prototyping flexibility, the digital calibration state-machine is implemented using an external (off-chip) FPGA.

The main motive behind this prototype is to demonstrate the feasibility of implementing a very wideband *LC* VCO with not only good but well-controlled performance across its range of operation. More specifically achieving a tuning range greater than 2:1 was set as a key design goal. The reason behind this goal is that once a 2:1 tun-

ing range is achieved, the VCO output is capable of reaching any frequency within $0 < f_{vco} < f_{vco,\max}$, by means of conventional frequency division techniques (e.g. divide-by-two circuits). Such a capability has very important implications on the design space of LC VCOs. In many applications where ring- or relaxation-type of VCOs are used to achieve wideband operation, such an LC VCO could now be used instead, bringing significant improvements in terms of jitter, phase noise, and possibly power consumption. Furthermore, such a wideband LC VCO could potentially replace the many narrowband LC VCOs needed in multi-band radio transceivers.

Although our prototype was not designed to suit a particular application, a center frequency of 1.8GHz was chosen based on its popularity in the literature and industrial applications.

5.2 A wideband *LC* VCO Prototype

5.2.1 VCO Design

The VCO core is based on a standard LC-tuned cross-coupled NMOS topology, chosen primarily for its ability to achieve low phase noise and for its higher headroom and lower parasitics compared to a tail-biased complementary cross-coupled configuration (Chapter 4). The LC tank consists of a single integrated differential spiral inductor, accumulation-mode MOS varactors allowing continuous frequency tuning, and a switched capacitor array providing coarse tuning steps. Fig. 5.1 shows a simplified

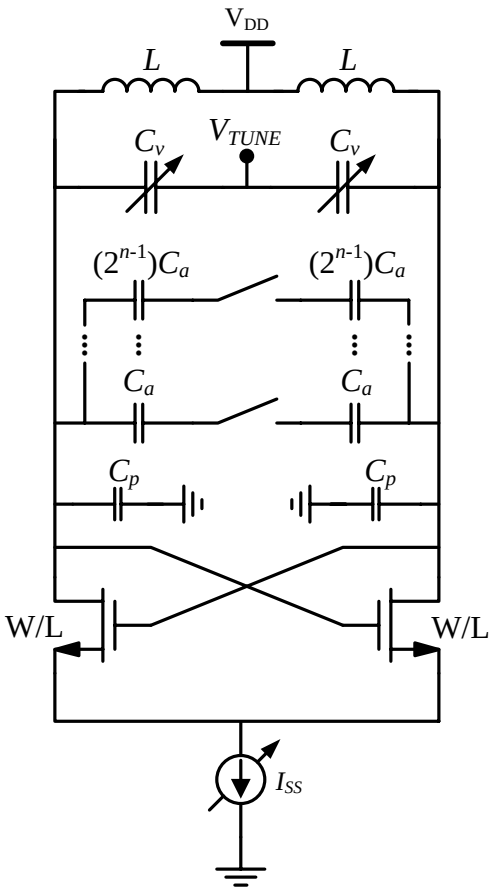


Figure 5.1: Simplified schematic of the VCO core.

schematic of the VCO core.

As discussed in Chapter 4, the design of wideband LC VCOs involves choosing among several parameters. In this technology, accumulation-mode MOS varactors achieve a maximum-to-minimum capacitance ratio of about 3, i.e. $\beta_v \approx 3$. Because varactors are AC-coupled to the LC tank (to avoid supply dependence and to be able to bias the gate with respect to a tuning voltage that stays within the supply range), its effective range is slightly reduced. In addition, the swing across the varactor will

further reduce its range (Chapter 4). Thus, a value of $\beta_v = 2.5$ is a better starting point. Another important element of this configuration is the quality of the switch used in the capacitor array. Each switch contributes additional loss to the tank due to its finite resistance, R_{on}. Thus, minimum-length NMOS devices are utilized and made as wide as can be tolerated with regards to the resulting parasitic drain-to-bulk capacitance, which ultimately limits the achievable tuning range. As discussed in Chapter 4, this tradeoff is well captured by the product $R_{on}C_d$, which stays relatively constant for minimum-length devices of varying width. In this technology, $R_{on}C_d \approx 300 \times 10^{-15}$ (1/rad). For example, a minimum-length NMOS sized to achieve a 5Ω on-resistance would have a drain-bulk parasitic capacitance of about 60fF. Next, we choose the amount of frequency overlap between adjacent sub-bands. For this design, a frequency overlap around 10% was decided upon, giving $k = 1.1$. Finally, we need to make an initial guess about the parasitic capacitance seen by the LC tank. A value of $\beta_p = 20$ was chosen as an initial guess, which corresponds to a 5% contribution to the total (maximum) tank capacitance.

Having determined the above parameters, namely $\beta_v = 2.5$, $\beta_p = 20$, $k = 1.1$, and $R_{on}C_d = 300 \times 10^{-15}$ (1/rad), we now have all the information we need to optimize the LC tank. Using equations (4.13) and (4.14), we can plot tuning range vs. Q_a, the quality factor of the array, for several values of n, the number of bits in the array. The resulting plot is shown in Fig. 5.2.

To allow for some amount of process variations, the targeted tuning range was set

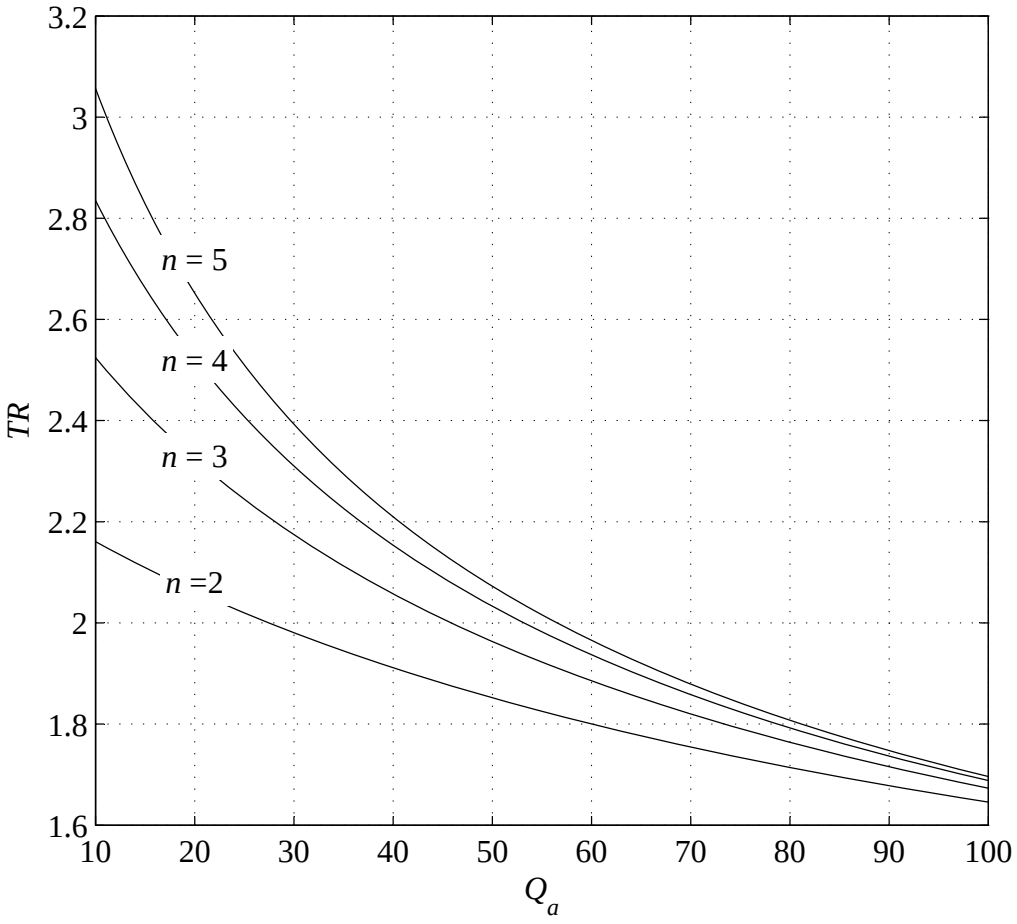


Figure 5.2: TR vs. Q_a for $\beta_v = 2.5$, $\beta_p = 20$, $k = 1.1$, and $R_{on}C_d = 300 \times 10^{-15}$ (1/rad).

to 2.2. As can be seen from Fig. 5.2, using $n = 2$ would only achieve this tuning range with fairly low Q, which would result poor phase noise performance. Going to $n = 3$ improves the design significantly and would achieve the required tuning range with a Q of around 28. Adding yet another bit to the array, i.e. $n = 4$, achieves the required tuning range with an even better Q of about 37. While further increasing the number bits would continue to improve the Q, the amount by which Q improves declines rapidly. Furthermore, for the sake of keeping the design simple, the number of bits was intentionally set to be only as large as needed. Thus, a bit length of $n = 4$ was chosen. With $n = 4$, the capacitor array switch will then be sized such that $Q_a = 37$, knowing that this will result in a tuning range of about 2.2. Given that $R_{on}C_d = 300 \times 10^{-15}$ (1/rad), (4.14) gives $\beta_a = 7$.

At this point, the inductance L is the only remaining unknown blocking the way to our design solution. Recall that from equation (4.8c), we have $\beta_p = \frac{1}{\omega_{o,\min}^2 LC_p}$. Thus, we can plot L as function of β_p to obtain the valid range of inductance for which $\beta_p > 20$, guaranteeing a tuning range greater than 2.2. This is illustrated in Fig. 5.3.

Inspecting Fig. 5.3, we see that the amount of parasitic capacitance (C_p) in the design affects the upper bound value of inductance. For $C_p = 0.25$pF, L should be smaller than 3.8nH. The particular values of C_p used in Fig. 5.3 represent the estimated range of parasitics for this design, based on the loading we expect. Part of this loading is itself a function of L, which further stresses the importance of accommodating a certain range of C_p over which the design satisfies the desired specifications. For example,

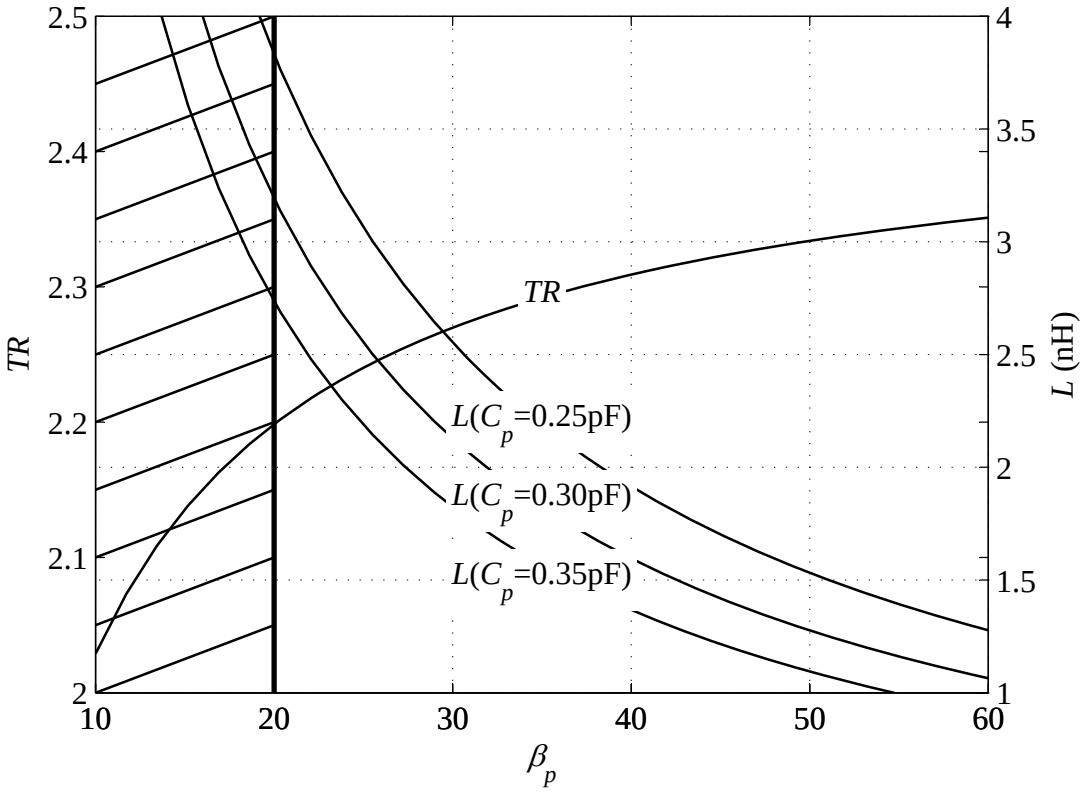


Figure 5.3: TR and L vs. β_p for $\beta_a = 7$, $\beta_v = 2.5$, $n = 4$, $k = 1.1$, and $f_{o,\min} = 1.10$GHz.

Table 5.1: LC Tank Component Values

k	n	L	C_a	C_v
1.1	4	2.8nH	400fF	780fF

choosing a smaller inductance results in a smaller impedance at resonance (assuming Q_L doesn't change significantly), which in turns implies that a larger W/L is needed (for the same bias current) to satisfy startup conditions, thus incurring more capacitive loading. Whereas bias current can be increased to get around this tradeoff, designs tend to be constrained by a power budget. In some cases, minimizing power may even be one of the main goals, which typically requires maximizing L (to the extent that Q_L doesn't drop significantly in doing so). In our case, we chose $L = 2.8$nH. This choice is consistent with our tuning range specification and results in a tank impedance that is sufficiently large to allow for a reasonable power consumption from a reasonably sized transconductor (such that its parasitics are not excessive).

We now have all the necessary information to solve for C_a and C_v. Using (4.12), we obtain $C_a = 430$fF. Substituting this result into (4.11) gives $C_v = 675$fF. Because the varactor is in series with a 5pF AC coupling MIM capacitor, its actual value should be increased to about 790fF. This completes the initial design of the LC tank and provides a good starting point for simulations. Based on the simulation results, the above process can be repeated once more to refine any assumed values which may have been slightly off. In our case, the design comes very close to our original calculations and the final values of the LC tank components are summarized in Table 5.1.

The inductor has been optimized with a 3-D EM simulator to provide optimal Q for the chosen inductance and at the frequencies of interest. It is implemented as a single differential octagonal spiral inductor using three 16μm-wide turns at 3μm spacing with an outer diameter of about 400μm. It achieves a differential Q around 12 at 2GHz. The accumulation-mode varactors are sized greater than the minimum length to increase their capacitance range (i.e. β_v). Each varactor consists of 8 strips of four 3.6μm/0.92μm fingers. Their maximum small-signal capacitance is 0.87pF. Under a 1V differential output swing, their effective maximum capacitance is very close to the desired value of $C_v = 780$fF and $\beta_v = 2.5$.

Now that the LC tank has been designed, other aspects of the VCO design can be addressed. One of the main goals of our prototype is to demonstrate the amplitude control scheme described in Chapter 4. To provide the desired flexibility in terms of programming the VCO output amplitude, the bias current feeding the VCO core must be designed to provide sufficient range. This range is also dependent on the tank impedance at the extremes of the targeted frequency range. From simulations, the tank impedance varies from 270Ω at 1.1GHz to about 800Ω at 2.4GHz. Since we would like to support a differential output swing of 1-2V, the bias current range must be approximately $1\text{V}/\left(2/\pi \cdot 800\Omega\right) \approx 2$mA to $2\text{V}/\left(2/\pi \cdot 270\Omega\right) \approx 11.6$mA. A slightly greater range was implemented using a 4-bit current source. Two additional bits were also included to provide the option to have finer control of the VCO amplitude.

The W/L of the cross-coupled NMOS devices is chosen based on oscillation startup

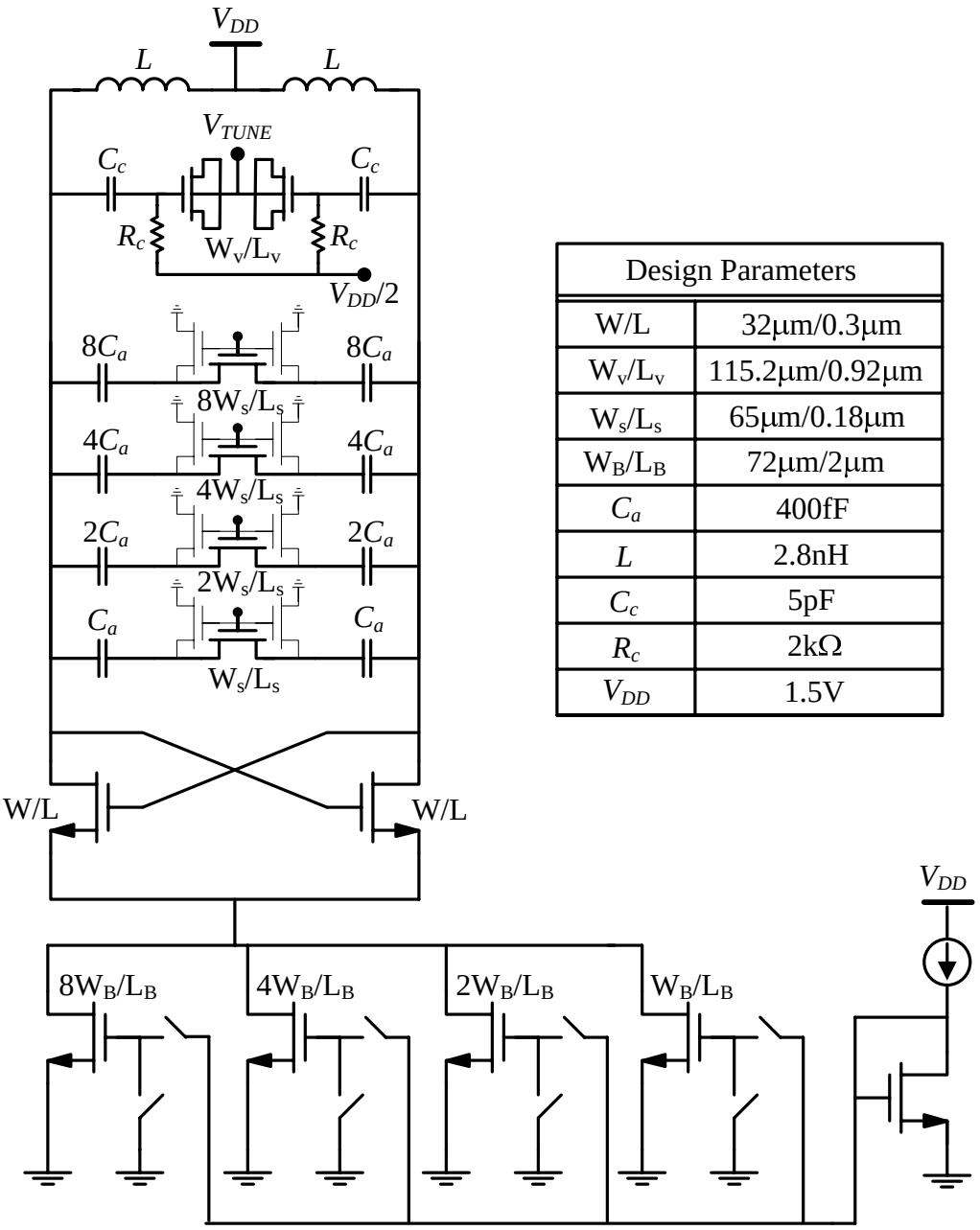
requirements at the low-end of the tuning range for the minimum expected bias current of about $1\text{V}/\left(2/\pi \cdot 270\Omega\right) \approx 5.8\text{mA}$. Since the drain noise current of the cross-coupled devices is the dominant noise contributor in this design, the lengths are made larger than minimum-size to reduce short-channel induced excess noise. This results in a device width of 32μm and length of 0.3μm, for which the gate is split into 11 fingers of 2.9μm. The final schematic of the VCO design is shown in Fig. 5.4.

5.2.2 VCO Output Buffer

A VCO output buffer was included to facilitate measurements. Its main function is to deliver sufficient power to drive the 50Ω spectrum analyzer used to measure our device. Due to the wideband nature of the VCO, the output buffer also needs to be wideband. Furthermore, since we are interested in observing the VCO amplitude during calibration, the output buffer should preferably be linear.

Linear operation was achieved using a combination of techniques. The VCO output is fed to the buffer via a capacitive divider. It reduces the VCO swing by a factor of about 5, such that it is kept within the linear input range of the buffer. It also reduces the capacitive loading seen by VCO LC tank by a factor of about 2. The buffer is implemented using a NMOS differential pair sized for a relatively low g_m/I_D in order to achieve a large linear input range at the cost of power efficiency. Minimum length devices are used to keep capacitive parasitics to a minimum.

Since the measurement apparatus is single-ended, a low-Q on-chip balun is used to



Design Parameters	
W/L	32μm/0.3μm
W_v/L_v	115.2μm/0.92μm
W_s/L_s	65μm/0.18μm
W_B/L_B	72μm/2μm
C_a	400fF
L	2.8nH
C_c	5pF
R_c	2kΩ
V_{DD}	1.5V

Figure 5.4: Final schematic of wideband *LC* VCO.

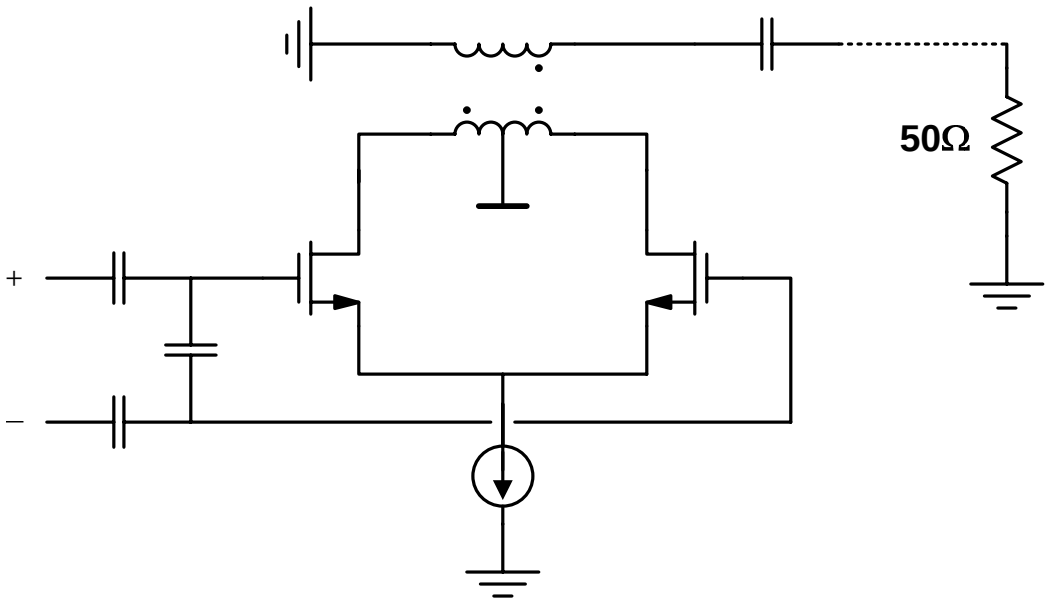


Figure 5.5: Simplified schematic of VCO output buffer.

realize a wideband linear differential-to-single-ended conversion. To provide adequate operation down to the low-end of the targeted frequency range (1.1GHz), a fairly high-inductance structure is preferable. A square geometry with narrow turn was chosen as it is more efficient in terms of inductance per area and since the intended Q is low. The voltage across the balun secondary is AC-coupled to a bondpad that is wirebonded to a very short trace on the PC board. Fig. 5.5 shows the simplified schematic of the output buffer.

5.2.3 Amplitude Calibration Circuits

The peak detector used for amplitude calibration is shown in Fig. 5.6. Sub-threshold NMOS devices are used to rectify the oscillator output. To reduce the loading on the

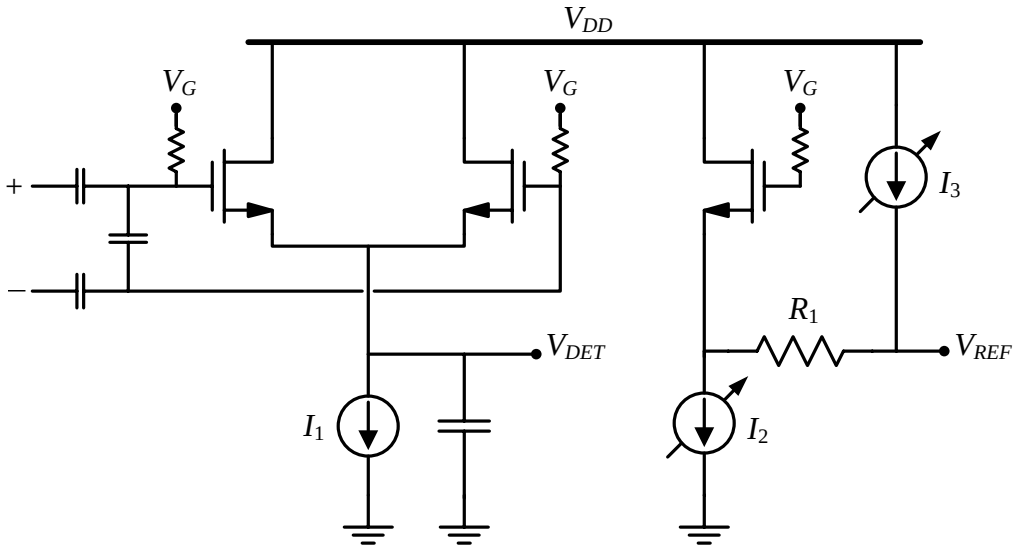


Figure 5.6: Simplified schematic of peak detector.

LC tank, a capacitive divider is used to couple the VCO outputs to the peak detector. A divider ratio of 1/2 is chosen to provide enough isolation, while sustaining sufficient voltage drive for accurate peak detection of the VCO amplitude.

The output of the peak detector is compared to a reference voltage established by a replica-bias circuit. This reference voltage is made programmable using 3 bits to control bias currents I_2 and I_3. Deriving these currents from a Bandgap-over-R bias circuit results in accurate voltage steps across resistor R_1 having minimal PVT variations. In our design, this circuit implements effective detection thresholds programmable from 1 to 2V in steps of 125mV (0-peak differential). More details on the operation of the peak detector is included in Appendix B.

The voltage comparator shown in Fig. 5.7 is used to compare the detected tank

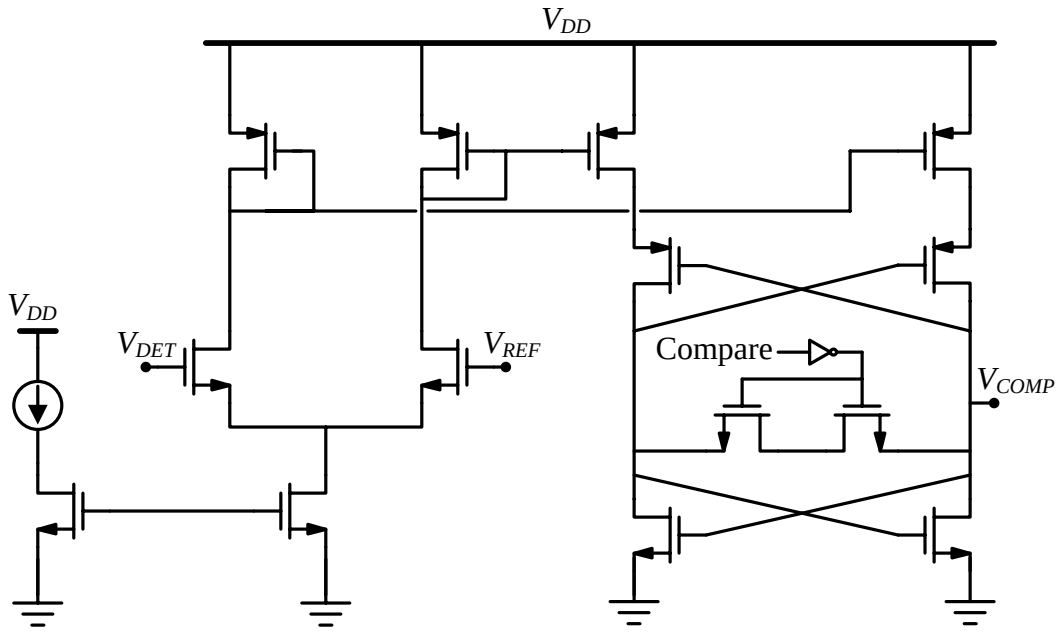


Figure 5.7: Simplified schematic of voltage comparator.

amplitude, V_{DET}, to the desired reference level, V_{REF}. The positive feedback in the second stage forces the output to latch to the positive or negative supply rail. When $V_{DET} > V_{REF}$, the output of the comparator is pulled high, otherwise the output is pulled to ground.

The output of the comparator is fed to a digital finite-state machine that is responsible for orchestrating the calibration routine. Illustrated in Fig. 5.8, a flow chart summarizes the logical operation of the calibration routine. The calibration begins by setting the bias current to its maximum value. The current source control bits are decremented until the comparator toggles low, indicating that the VCO output is now lower than the programmed reference level. Faster and more elaborate calibration routines

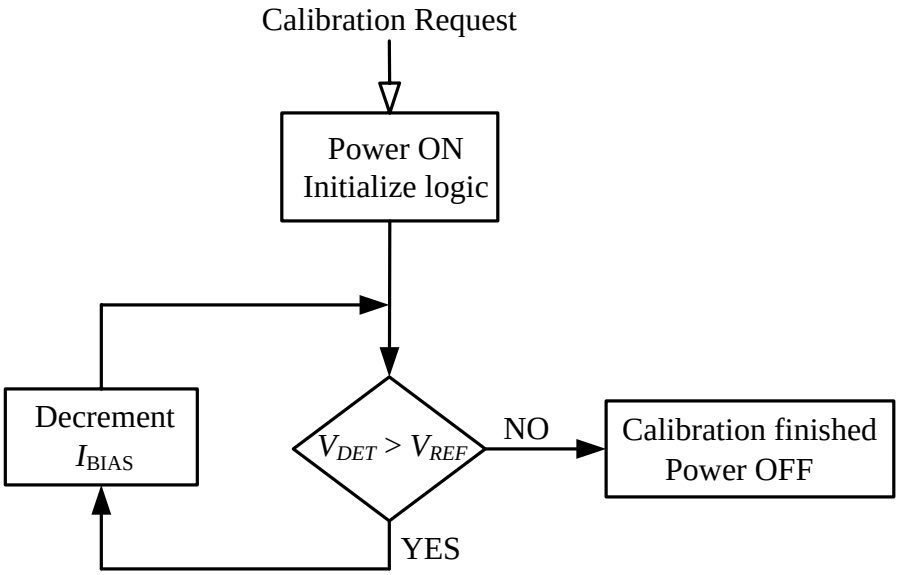


Figure 5.8: Flow chart of implemented calibration finite-state machine.

can easily be implemented by modifying the digital state machine. The time required to run the calibration routine is at most $2^N \cdot T_{CYCLE}$, where N is the number of current source control bits and T_{CYCLE} is the time needed to complete a single calibration cycle, here dominated by the settling time of the peak detector ($<$ 100ns). Hence, a conservative T_{CYCLE} of about 600ns was used as a proof of concept and does not represent the actual minimum settling time needed for this implementation. This amplitude control scheme features a basic tradeoff between amplitude accuracy and speed. This implementation uses $N = 4$, providing amplitude control from $V_{o,\min}$ to $V_{o,\max}$ in increments of $(V_{o,\max} - V_{o,\min})/16$ and a worst-case calibration run time of $16 \cdot T_{CYCLE}$. Alternatively, N could be increased to improve accuracy at the expense of a longer calibration

time. If N is large, the errors introduced by the peak detector and comparator offset could contribute to the quantization error and may need to be considered. In many applications, the calibration time can be tolerated and a calibration can be initiated every time the synthesizer is tuned to a new frequency, without adding significant overhead to the overall settling time. Alternatively, a full-set of calibrations (for each frequency sub-band) can be run at power-on and the results stored as a look-up table in memory.

5.3 Experimental Results

The VCO was measured on a test board built on standard FR4 material. The die was glued directly onto the printed circuit board (PCB) with conductive silver epoxy and wirebonds were used to connect all inputs and outputs. A photograph of the VCO die is shown in Fig. 5.9. The total chip area including bondpads is 1.7mm^2.

The setup used for the following measurements is illustrated in Fig. 5.10. A 1.5V battery was used as a low noise power supply for the device under test (DUT). Short wire cables were used to connect the DUT PCB to the FPGA test board. The FPGA device was powered separately using a 1.8V regulated supply provided on its test board.

The on-chip VCO buffer was biased with 8.5mA. It delivers a nominal output power of about -12dBm at 1.8GHz. Despite its low Q, the buffer output power varies from -16dBm (1.1GHz) to -10dBm (2.4GHz) when the VCO is calibrated to have constant output swing vs. frequency. However, such power levels are sufficient for measurement purposes.

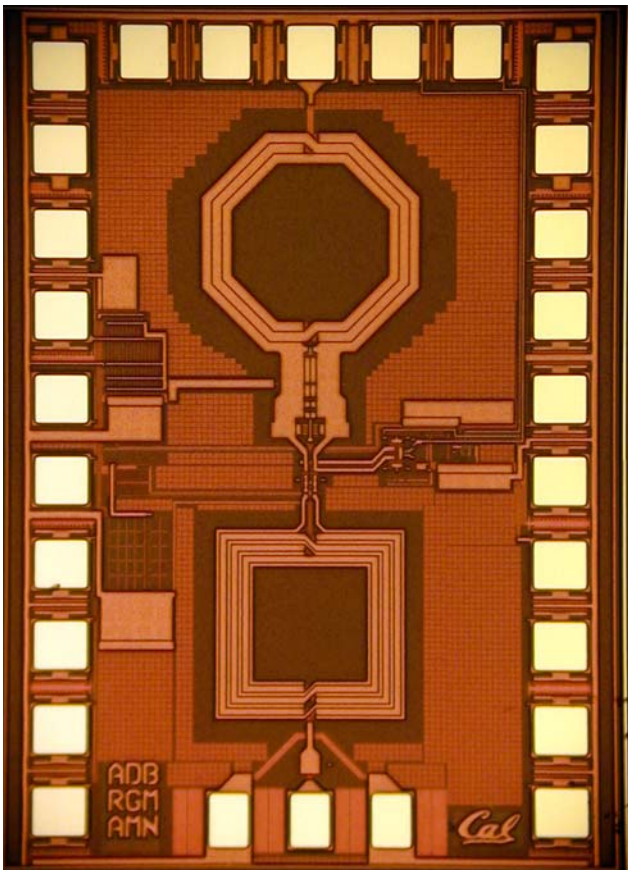


Figure 5.9: Die photograph.

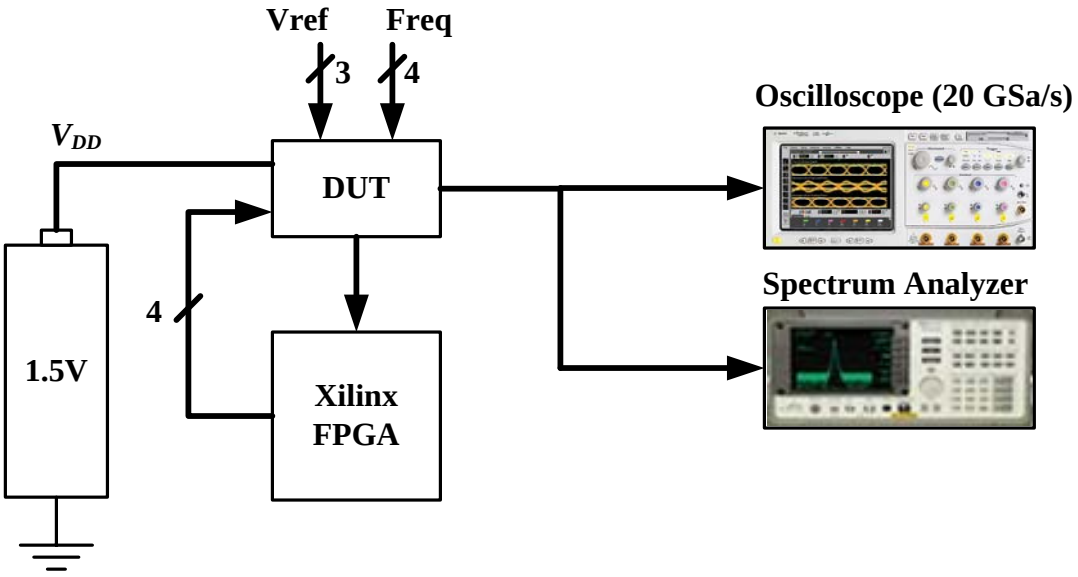


Figure 5.10: Experimental setup for measurements.

In the following measurements, a calibration of the amplitude was executed at each frequency to set the VCO amplitude approximately constant. A comparison of calibrated vs. un-calibrated scenarios will be discussed in a later part of this chapter.

Phase noise measurements were performed on a HP8563E spectrum analyzer running the phase noise measurement option. Fig. 5.11 shows the measured and simulated phase noise at the lower, middle, and upper ends of the tuning range running at a core power consumption of 10, 4.8, and 2.6mW, respectively. The drop of the core power consumption with increasing frequency is a direct result of amplitude calibration, reflecting the fact that less current is required to produce a given voltage swing since the *LC* tank impedance increases with frequency. Measurements show good agreement

with simulations. Beyond offset frequencies of about 1MHz, the measurement is limited by the noise floor of the spectrum analyzer.

The VCO tuning range was measured using the same instrument. A very wide tuning range of 73% is achieved with a control voltage tuned from 0 to 1.5V. The VCO tuning range is illustrated in Fig. 5.12, showing all 16 overlapping frequency sub-bands. The measured frequency range is 1.14-2.47GHz with a maximum tuning sensitivity of 270MHz/V. The measured tuning range agrees very well with the simulated range of 1.10-2.47GHz.

Fig. 5.13 shows the measured buffer output voltage waveform during amplitude calibration runs at 1.4, 1.8, and 2.2GHz for a VCO differential tank amplitude programmed to 1.1V. The calibration begins by setting the bias current to its maximum value. The current source control bits are decremented until the comparator toggles low, indicating that the VCO output is now lower than the programmed reference level. Fig. 5.13 also captures the transition from voltage-limited to current-limited regime at 1.8 and 2.2GHz, where the voltage amplitude responds noticeably slower to the decreasing bias current during the first several calibration cycles. Faster and more elaborate calibration routines can easily be implemented by modifying the digital state machine.

Fig. 5.14 shows the phase noise performance across the VCO frequency range for calibrated and uncalibrated scenarios. In the uncalibrated case, the bias current is set just high enough to satisfy start-up requirements at the low-end of the tuning range and remains constant. At the upper-end of the tuning range, this results in a

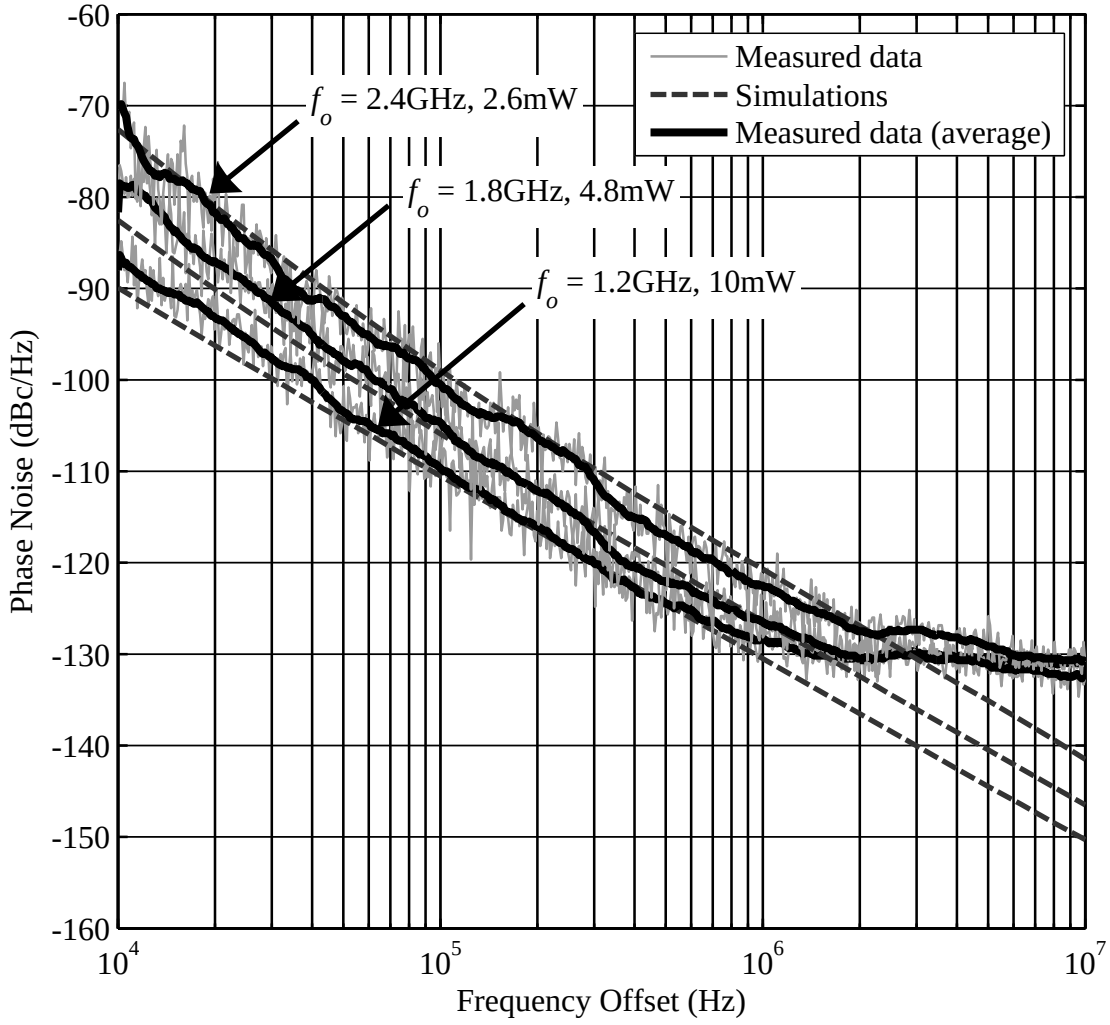


Figure 5.11: Phase Noise at 1.2, 1.8, and 2.4GHz for a core power consumption of 10, 4.8, and 2.6mW, respectively.

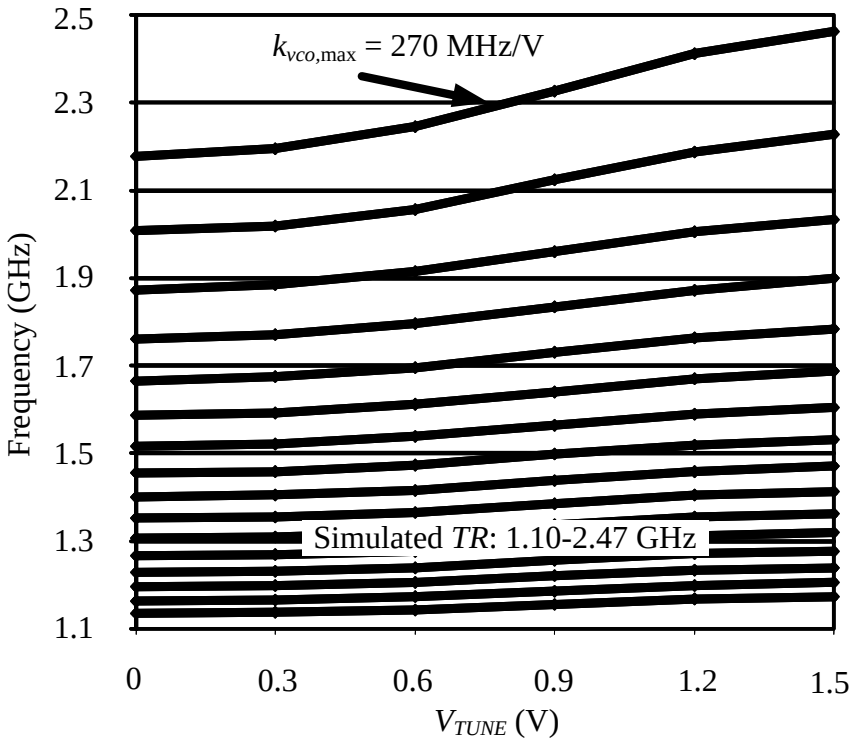


Figure 5.12: Measured frequency tuning range.

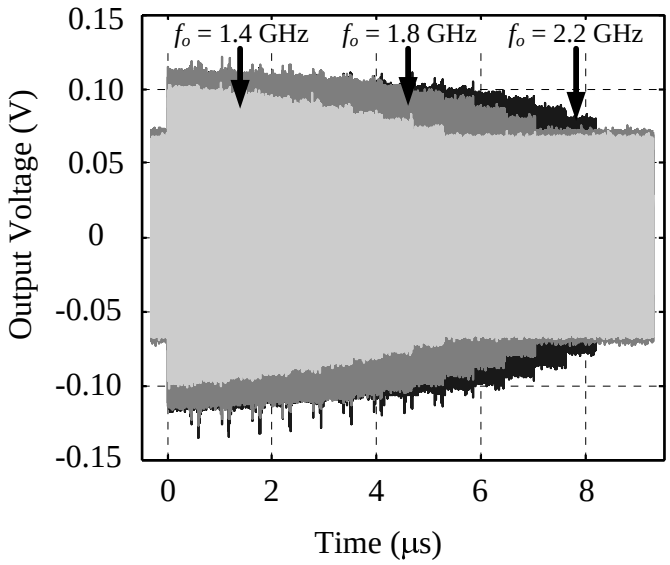


Figure 5.13: Measured amplitude calibration runs at 1.4, 1.8 and 2.2GHz.

tank amplitude that is too large and considerably degrades phase noise, as discussed in Chapter 4. In the calibrated case, the bias current is effectively scaled down with frequency to maintain the tank amplitude approximately constant, helping to sustain the phase noise performance over the upper-end of the tuning range. The 9dB/octave trend predicted by equation (4.7) is consistent with the measurements.

The VCO performance can be compared to other published VCOs by means of a power-frequency-tuning-normalized (PFTN) figure of merit (FOM), as defined in [69] and repeated here for convenience:

$$FOM = 10 \cdot \log\left(\frac{kT}{P} \cdot \left(\frac{\omega_{o,\max} - \omega_{o,\min}}{\Delta\omega}\right)\right) - \mathcal{L}\left\{\Delta\omega\right\} \tag{5.1}$$

where ω_o is the carrier frequency, $\Delta\omega$ is the frequency offset, P is the power consumed by the VCO core, and $\mathcal{L}\{\Delta\omega\}$ is the phase noise measured at an offset $\Delta\omega$ from the

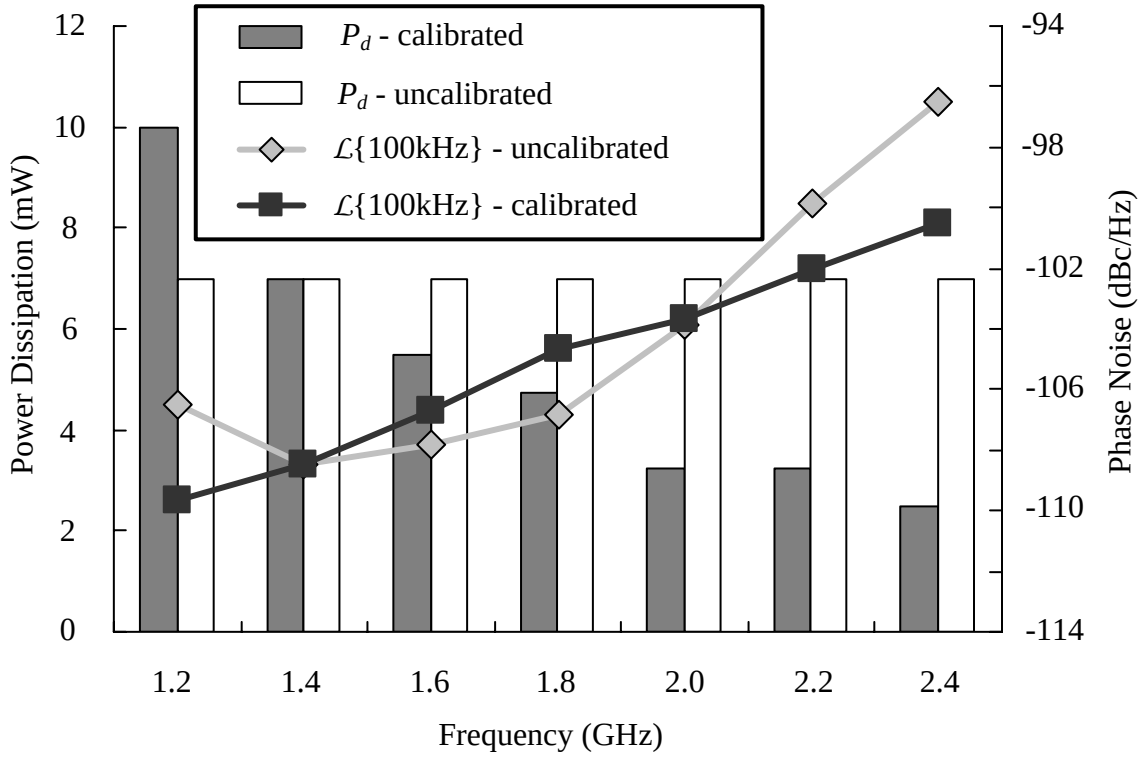


Figure 5.14: Measured phase noise at 100 kHz offset and core power consumption vs. frequency for calibrated and uncalibrated cases.

carrier. Fig. 5.15 casts the data provided in Fig. 5.14 as the PFTN FOM defined above, for calibrated and uncalibrated scenarios. The combination of lower phase noise and lower power consumption for the calibrated scenario yield a significantly improved FOM in the upper half of the frequency range. This results in a FOM ranging from 5 to 8.5dB. Table 5.2 shows how this number compares favorably with other notable published VCOs implemented in bulk CMOS.

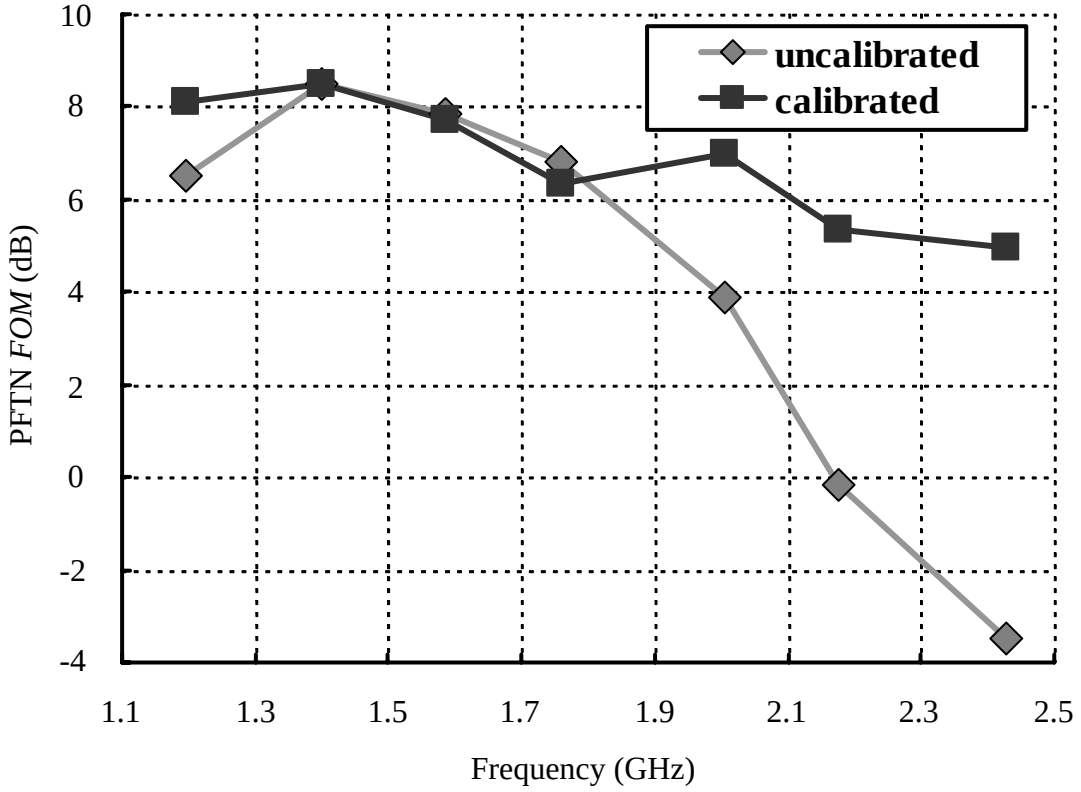


Figure 5.15: FOM vs. frequency for calibrated and uncalibrated cases.

Table 5.2: VCO Performance Summary

Technology	0.18μm CMOS
Supply Voltage	1.5V
Current Consumption (Core only)	1.67-6.67mA
Center Frequency	1.8GHz
Tuning Sensitivity (k_{VCO})	$\leq$ 270MHz
Phase Noise (f_o = 1.8GHz, Δf = 100kHz, 4.8mW)	$-$104.7dBc/Hz
Phase Noise (f_o = 1.8GHz, Δf = 600kHz, 4.8mW)	$-$104.7dBc/Hz
Phase Noise (f_o = 1.8GHz, Δf = 1MHz, 4.8mW)	$-$104.7dBc/Hz

Table 5.3: VCO Performance Comparison of Published Wideband VCOs

Reference	Technology	Center Frequency (GHz)	Core Power (mW)	Tuning Range	$k_{VCO,\max}$ (MHz/V)	FOM (dB)
[68]	CMOS	2.1	12.2	35%	330	+5.8
[69]	CMOS	2.6	10	26%	600	−3.1
[70]	SOICMOS	4.33	2-3	58.7%	2250	+5.9-10.3
[71]	CMOS	1.8	32.4	28%	500	−3.8
[72]	CMOS	1.25	7.2	28%	70	−0.2
[63]	CMOS	2.12	10	30.5%	450	+1.9
[73]	CMOS	2.1	2	28.6%	260	+5.7
[74]	BiCMOS	1.87	14-30.8	30%	45	+2-4
This work	CMOS	1.8	2.6-10	73%	270	+5-8.5

5.4 Summary

We have described a 1.8GHz *LC* VCO implemented in 0.18μm bulk CMOS that simultaneously achieves low phase noise and a very wide tuning range exceeding 2:1 (73%). Its measured performance is summarized in Table 5.2. To provide robust operation and stabilize performance over the entire frequency range, the VCO amplitude is controlled using a novel mixed-signal amplitude calibration scheme that does not degrade phase noise and consumes negligible area and power. Typical measured phase noise is −123.5dBc/Hz at 600kHz offset from 1.8GHz for a core power consumption of only 4.8mW from a 1.5V supply. As shown in Table 5.3, the VCO achieves a power-frequency-tuning-normalized phase noise *FOM* ranging from 5 to 8.5dB over the entire frequency range, which is one of the highest reported to date. All measurement results agree closely with simulations and intended design specifications.

Chapter 6

Conclusion

6.1 Thesis Summary

Current market demands and continuing trends in the electronics industry suggest that communication devices will need to support wider bandwidths and an ever-growing number of frequency bands and protocols. This poses interesting challenges for many components of such devices. This dissertation has focused one of the key enabling components, namely the frequency synthesizer. In particular, this work investigated the analysis and design of wideband LC VCOs. Whereas fully-integrated LC VCOs are conventionally restricted to narrowband applications, we have introduced techniques that reliably extend their usage to wideband/multiband applications.

Fundamental principles of PLL frequency synthesizers and LC VCOs were introduced in Chapter 2 and Chapter 3, respectively. These chapters provide the framework

supporting subsequent discussions. The impacts of wide frequency variations on several LC VCO parameters, such as startup constraints, output amplitude, and phase noise, are analyzed in Chapter 4. Based on our observations, we proposed a novel approach of stabilizing the VCO performance across its frequency range. Using a digital amplitude calibration scheme, the output voltage amplitude can be controlled independently of the frequency of operation. Unlike continuous-time feedback approaches, our solution does not impair the phase noise performance. In addition to its low complexity, digital calibration lends itself to a wide variety of control algorithms, such that different applications can optimize the VCO performance as best suited. Only two compact analog blocks, namely a peak detector and a voltage comparator, and one digital finite-state-machine are needed, all of which adapt well with technology scaling. Aside from being a compact solution, its power consumption is negligible, mainly due to its infrequent activity. In general, the presented approach presents a common tradeoff between speed and accuracy. As we decrease the quantization error of the voltage amplitude control (by dedicating additional bits to the VCO bias current source), more time is required to calibrate the device.

A conventional LC VCO using a binary-weighted switched-capacitor array was used as the vehicle for this work. Its tuning range was analyzed in terms of fundamental dimensionless design parameters yielding useful design equations. From the derivations in Chapter 4, design tradeoffs between tuning range, quality factor, and the number of bits of the capacitor array, can be readily optimized. The implementation of a proof-

of-concept prototype is detailed in Chapter 5. The measurement results confirm the effectiveness of our proposed solution and validate our analysis.

6.2 Future Research Opportunities

While this work demonstrated one example of using digital calibration to control the performance of a VCO, countless opportunities exist for applying similar concepts to a wide variety of other Analog and RF devices. Within the scope of *LC* VCOs, one obvious application is to use a similar amplitude calibration scheme on a different topology. One interesting case is the popular cross-coupled complementary CMOS *LC* VCO without a tail current source, for which the amplitude is controlled via the supply voltage. Using a digitally adjustable voltage regulator, this topology would easily accommodate a very similar calibration scheme.

Another desirable extension to this work is to encompass the overall PLL frequency synthesizer, using the current prototype as its core. Wideband operation introduces important considerations for some of the building blocks discussed in Chapter 2. Furthermore, balancing loop dynamics and noise performance across wide variations of divide ratio and VCO gain poses serious challenges.

Appendix A

LC VCO frequency sub-bands

A.1 Adjacent sub-band overlap condition

Equation (4.10) states that in order for any two adjacent sub-bands to overlap, all that is required is that the change in varactor capacitance exceeds the change in capacitance seen by a unit array capacitor, C_a, as it goes from on to off. While this may seem intuitive, this section shows why equation (4.10) holds true.

Given an LC VCO with an n-bit binary-weighted capacitor array, the net capacitance at the neighboring end-points of any two adjacent sub-band can be generally expressed as follows:

$$C_T^i\big|_{\min} = i \cdot C_a + (2^n - 1 - i) \cdot \left(\frac{1}{C_{dd}} + \frac{1}{C_a}\right)^{-1} + C_{v,\min} + C_p \tag{A.1}$$

$$C_T^{i+1}\big|_{\max} = (i-1) \cdot C_a + (2^n - i) \cdot \left(\frac{1}{C_{dd}} + \frac{1}{C_a}\right)^{-1} + C_{v,\max} + C_p \tag{A.2}$$

To ensure overlap, we must guarantee that $C^{i+1}_{T,\max} > C^{i}_{T,\min}$, where i is any positive integer over $\{0, 2^n - 1\}$.

$$C_{v,\max} - C_{v,\min} > C_a - \left(\frac{1}{C_{dd}} + \frac{1}{C_a}\right)^{-1} \tag{A.3}$$

Hence, this boundary condition does not depend on the number of bits, i, in the array or the parasitic capacitance C_p. Note that (A.3) is equivalent to (4.10).

A.2 Adjacent sub-band frequency overlap factor

Following equation (4.10), an overlap margin factor, k, was introduced such that (i.e. $k > 1$). In practice, expressing overlap as a percentage of frequency is more meaningful. In Chapter 4, we claimed that an overlap factor of k corresponds to a fractional frequency overlap of approximately $(k-1)/k$. This section shows why this is a good approximation.

The fractional frequency overlap, k_F, between any two adjacent sub-band is given by:

$$k_F = \frac{\left(\frac{1}{\sqrt{C^{i}_{T,\min}}} - \frac{1}{\sqrt{C^{i}_{T,\max}}}\right) - \left(\frac{1}{\sqrt{C^{i}_{T,\min}}} - \frac{1}{\sqrt{C^{i}_{T,\max}}}\right)}{\left(\frac{1}{\sqrt{C^{i}_{T,\min}}} - \frac{1}{\sqrt{C^{i}_{T,\max}}}\right)} \tag{A.4}$$

However, $C^{i-1}_{T,\min}$ may be expressed as $C^{i}_{T,\min} + \Delta C_a$. Thus (A.5) may be rewritten as:

$$
\begin{aligned}
k_F &= \frac{\left(\frac{1}{\sqrt{C^i_{T,\min}}} - \frac{1}{\sqrt{C^i_{T,\min}+\Delta C_v}}\right) - \left(\frac{1}{\sqrt{C^i_{T,\min}}} - \frac{1}{\sqrt{C^i_{T,\min}+\Delta C_a}}\right)}{\left(\frac{1}{\sqrt{C^i_{T,\min}}} - \frac{1}{\sqrt{C^i_{T,\min}+\Delta C_v}}\right)} \\
&= \frac{\frac{1}{\sqrt{1+\frac{\Delta C_a}{C^i_{T,\min}}}} - \frac{1}{\sqrt{1+\frac{\Delta C_v}{C^i_{T,\min}}}}}{\frac{1}{\sqrt{1+\frac{\Delta C_v}{C^i_{T,\min}}}}}
\end{aligned} \tag{A.5}
$$

Expanding each term as a binomial series and ignoring high order terms, we obtain:

$$
\begin{aligned}
k_F &\approx \frac{\Delta C_v - \Delta C_a}{\Delta C_v} \\
&= \frac{k-1}{k}.
\end{aligned} \tag{A.6}
$$

Appendix B

Sub-threshold MOS peak detector Analysis

The proposed amplitude control scheme requires an accurate peak detector circuit to measure the VCO output voltage amplitude. Precision high-frequency peak detectors are readily implemented with bipolar junction transistors acting as rectifying devices [83]. Thanks to the well-controlled I-V characteristic of bipolar devices, the peak detector response can be predicted with great accuracy [83]. Since high-speed bipolar transistors are not available in standard CMOS technology, other devices must be used. There are many ways to rectify a signal using MOS transistors. For example, diode-connected NMOS transistors can be used. However, the true challenge consists of implementing a precise and predictable rectifier that hopefully does not dependent on poorly-modeled or widely-varying process parameters.

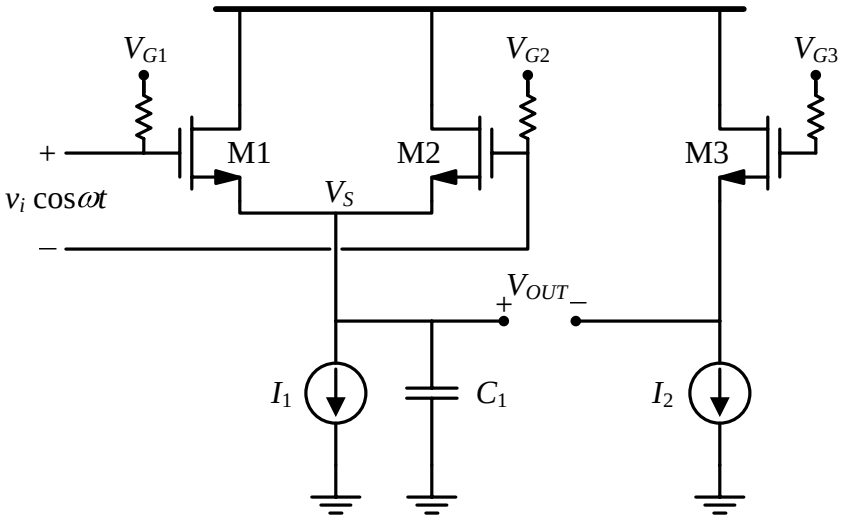


Figure B.1: Simplified MOS peak detector schematic.

One promising approach is to approximate the bipolar implementation with the same configuration using NMOS transistors operating in the subthreshold region. A simplified schematic is shown in Fig. B.1

When operating in its subthreshold region, a MOS transistor's I-V characteristic closely resembles that of a bipolar device:

$$I_{DS} = I_k \cdot \frac{W}{L} \cdot \exp\left(\frac{V_{GS}}{n \cdot V_T}\right) \cdot \exp\left(\frac{n-1}{n} \cdot \frac{V_{BS}}{V_T}\right) \tag{B.1}$$

where I_k is a technology dependent positive constant, n is a constant ranging from 1-2 and is inversely proportional the slope of the $log(I_{DS})$-V_{GS} characteristic in the subthreshold region, and V_T is the thermal voltage given by $k_B T/q$.

Using a separate P-WELL (this option is often available in modern CMOS technologies), the bulk terminal can be tied to the source, thereby eliminating the second

exponential term in (B.1). Thus we have:

$$I_{DS} = I_k \cdot \frac{W}{L} \cdot \exp\left(\frac{V_{GS}}{n \cdot V_T}\right) \tag{B.2}$$

In the presence of an input signal $v_i \cos \omega t$, the drain current in M1 and M2 is given by:

$$I_{DS1,2} = I_k \cdot \left(\frac{W}{L}\right)_{1,2} \cdot \exp\left(\frac{V_{GS1,2}}{n \cdot V_T}\right) \cdot \exp\left(\frac{v_i}{n \cdot V_T} \cdot \cos \omega t\right) \tag{B.3}$$

Note that the V_{GS} term in (B.3) is actually time-varying. The source-coupled node tracks changes in the input signal envelope. Depending on the selection of the hold capacitor C_1 and bleed current source I_1, the envelope can be tracked more or less rapidly. In typically scenarios however, the rate at which V_S moves is much slower than the input signal. Thus V_{GS} will be approximated as constant in our derivation.

Equation (B.3) may be rewritten as:

$$I_{DS1,2} = I_k \cdot \left(\frac{W}{L}\right)_{1,2} \cdot \exp\left(\frac{V_{GS1,2}}{n \cdot V_T}\right) \cdot (I_o(b) + 2 \cdot I_1(b) \cos \omega t + 2 \cdot I_2(b) \cos \omega t + ...) \tag{B.4}$$

where $I_j(b)$ are the j-th order modified Bessel functions of the first kind and $b = v_i / nV_T$. The average value of (B.4) can now be isolated:

$$\begin{aligned} I_{DS1,2,avg} &= I_k \cdot \left(\frac{W}{L}\right)_{1,2} \cdot \exp\left(\frac{V_{GS1,2}}{n \cdot V_T}\right) \cdot I_o(b) \\ &\approx I_k \cdot \left(\frac{W}{L}\right)_{1,2} \cdot \exp\left(\frac{V_{GS1,2}}{n \cdot V_T}\right) \cdot \frac{\exp(b)}{\sqrt{2\pi \cdot b}} \end{aligned} \tag{B.5}$$

The approximation in (B.5) results in less than 2% error for $b > 7$ and less than 1% error for $b > 15$. Assuming that M1 and M2 are perfectly matched, their average

current must also be equal such that:

$$I_{DS1,avg} = I_{DS2,avg} = \frac{I_1}{2} \tag{B.6}$$

Combining (B.5) and (B.6), we obtain:

$$I_1 = 2 \cdot I_k \cdot \left(\frac{W}{L}\right)_{1,2} \cdot \exp\left(\frac{V_{GS1,2}}{n \cdot V_T}\right) \cdot \frac{\exp\left(\frac{v_i}{n \cdot V_T}\right)}{\sqrt{2\pi \cdot \frac{v_i}{n \cdot V_T}}} \tag{B.7}$$

The current through reference transistor M3 is

$$I_2 = I_k \cdot \left(\frac{W}{L}\right)_3 \cdot \exp\left(\frac{V_{GS3}}{n \cdot V_T}\right) \tag{B.8}$$

Taking the ratio of (B.8) to (B.7), we get:

$$\frac{I_2}{I_1} = \frac{(W/L)_3}{2 \cdot (W/L)_{1,2}} \cdot \exp\left(\frac{V_{GS3} - V_{GS1,2}}{n \cdot V_T}\right) \cdot \frac{\sqrt{2\pi \cdot \frac{v_i}{n \cdot V_T}}}{\exp\left(\frac{v_i}{n \cdot V_T}\right)} \tag{B.9}$$

If the gates of M1-M3 are biased at the same dc voltage (i.e. $V_{G1} = V_{G2} = V_{G3}$), then $V_{OUT} = V_{GS3} - V_{GS1,2}$. Taking the natural logarithm of both sides of (B.9) results in:

$$V_{OUT} = v_i + n \cdot V_T \cdot \left(\ln\left(\frac{I_2}{I_1}\right) + \ln\left(2 \cdot \frac{(W/L)_{1,2}}{(W/L)_3}\right) - \ln\left(\sqrt{2\pi \cdot \frac{v_i}{n \cdot V_T}}\right)\right) \tag{B.10}$$

Choosing $(W/L)_3 = 2(W/L)_{1,2}$, (B.10) simplifies to

$$V_{OUT} = v_i + n \cdot V_T \cdot \left(\ln\left(\frac{I_2}{I_1}\right) - \ln\left(\sqrt{2\pi \cdot \frac{v_i}{n \cdot V_T}}\right)\right) \tag{B.11}$$

As seen in (B.11), a relatively weak nonlinear (and temperature dependent) term exists. Due to its logarithmic form, it can be neglected in many applications, especially if the input signal is large. When high precision is required, the I_2/I_1 term offers an opportunity to have some degree of correction. A variety of techniques can be used to make this correction term track the signal amplitude and temperature variations.

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