Ultra Low Power Transmitters for Wireless Sensor Networks

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Technical Report No. UCB/EECS-2006-57
http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-57.html

May 15, 2006

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by

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B.Eng. (National University of Singapore, Singapore) 1998
M.Eng. (National University of Singapore, Singapore) 2000

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY OF CALIFORNIA, BERKELEY

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Spring 2006

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Abstract

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The emerging field of wireless sensor network (WSN) potentially has a profound impact on our daily life. Widespread deployment of wireless sensor network requires each node to (1) consume less than 100μW of average power for a long usage lifetime and low operational cost, (2) cost less than $1 for a low system cost and (3) occupy less than $1cm^3$ for seamless integration into our physical environment. Among these requirements, the power constraint is the most challenging. Since communication accounts for majority of power budget in a typical sensor node, it is crucial to have an energy efficient transmitter. In WSN, the radiated power is low (< 1mW) due to the short communication distance (< 10m). As such low radiated power, the overhead power is significant and degrades the transmitter efficiency substantially. This is the reason for the low efficiency of WSN existing transmitters.

The thesis focuses on providing a solution to this problem. It first establishes the principles of obtaining an energy efficient transmitter at low radiated power. Based on

these principles, three different 1.9GHz transmitters are designed and implemented in ST 0.13μm CMOS process: direct modulation transmitter, injection locked transmitter and active antenna transmitter. To push the performance envelope of WSN transmitters, new transmitter architectures, circuit techniques, enabling technologies and co-design methodology are employed. The state-of-the-art active antenna transmitter achieves 46% efficiency and support a data rate up to 330 kbps.

Finally, to demonstrate a low power and small form factor sensor node, the active antenna transmitter is integrated into a 38 x 25 x 8.5 mm^3 wireless transmit sensor node.

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Professor Jan Rabaey
Dissertation Committee Chair

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Acknowledgements

First and foremost, I would like to my advisers, Professor Jan Rabaey and Professor Ali Niknejad. Professor Rabaey, thank you very much for your encouragement, guidance and support for the years I spent in Berkeley. You are truly visionary and a great advisor. Professor Niknejad, thank you for teaching so much about RF circuits and all the advice that you have given me. I really enjoyed those brainstorming and discussion sessions that we had. Without both of you, this research would not be possible. Thank you.

I am grateful to Professor Paul Wright and Professor Stephen Smith for their valuable advice given during my Qualifying Exam. Many thanks to Professor Robert Meyer, Professor Bernhard Boser, Professor Robert Brodersen, Professor Jan Rabaey, Professor Ali Niknejad, Professor Seth Sanders and Professor Bora Nikolic for their inspiring integrated circuit courses that have given me a deeper understanding of integrated circuit design. To all the Professors and Teaching Assistants who have taught me, I thank you.

I am thankful to our industrial collaborators, especially STMicroelectronics for supporting the chip fabrications and Agilent Technologies for sharing the FBAR technology. Thanks to Dr. Gupta Bhusan for his valuable suggestions during the design reviews and Dr. Mike Frank for his insightful discussions on the FBAR resonators.

I would also like to thank Professor Robert Brodersen and Professor Jan Rabaey for founding the Berkeley Wireless Research Center (BWRC). I have been very fortunate to earn my Ph.D. in such a stimulating and rich environment. Thanks to all the BWRC staff, especially Gary Kelson, Brian Richards, Kelvin Zimmerman, Elise Mills, Jennifer Stone, Sue Mellers, Fred Burghardt, Tom Boot, Jessica Budgin and Brenda Vanoni.

It also has been a great working with my lab-mates in BWRC. In particular, I would like to thank the PicoRadioRF team (Brian Otis, Nate Pletcher, Simone Gambini, Yanmei Li, Davide Guermandi, Michael Mark, Richard Lu, Ulrich Schuster) for the wonderful time that we spent together. Many thanks to Stanley Wang, Naratip Wongkomet, Yun Chiu, Luns Tee, En-Yi Lin, Cheol-Woong Lee, Bill Tsang, Mounir Bohsali Mike Sheets, Josie Ammer, Mike Chen and Patrick McElwee for all the insightful discussions, support and encouragement. I also greatly appreciate all the help from Pavel Monat, Ben Liu, Philip Liu, Nurrachman Liu and Fan Zhang.

I am also grateful to Professor Gamani Karunasiri (Naval Postgraduate School) and Professor Yeo-Swee Ping (National University of Singapore) for their invaluable advice over the years.

Special thanks to my family, especially my Mom and Dad, for their support and encouragement over the years.

Finally, I am thankful to my wife, Siew-Leng Teng for her love and all the little ones.

Chapter 1

Introduction

1.1 Wireless Sensor Networks

The emerging field of wireless sensor networks (WSN) creates a new paradigm in the way we interact with our environment. Recent technological advances in MEMS, energy scavenging, energy storage and IC packaging, coupled with the availability of low power, low cost digital and analog/RF electronics have made it possible to realize a dense network of inexpensive wireless sensor nodes, each having sensing, computational and communication capabilities [Rabaey02]. These ubiquitous wireless sensor networks allow us to sense, manage and actuate a vast number of autonomous sensor/actuator nodes embedded in the fabrics of our daily living environment. Such ambient intelligence provides endless possibilities like environmental control in office buildings, integrated patient monitoring, diagnostics and drug administration in hospital, smart homes, identification and personalization, automatic industrial monitoring and control systems, smart consumer electronics, warehouse inventory, automotive networks, traffic regulation and water/air quality monitoring. It is estimated that the number of sensor

nodes deployed will explode from 200,000 today to 100 million by 2008, and the worldwide market will grow from $100 million presently to more than $1 billion by 2009 [Harbor05].

Conceptually, a wireless sensor network consists of a dense network of nodes, spaced less than 10m apart as shown in Fig. 1.1. In typical deployment scenarios, a few neighboring nodes lie within the communication radius of the each node.

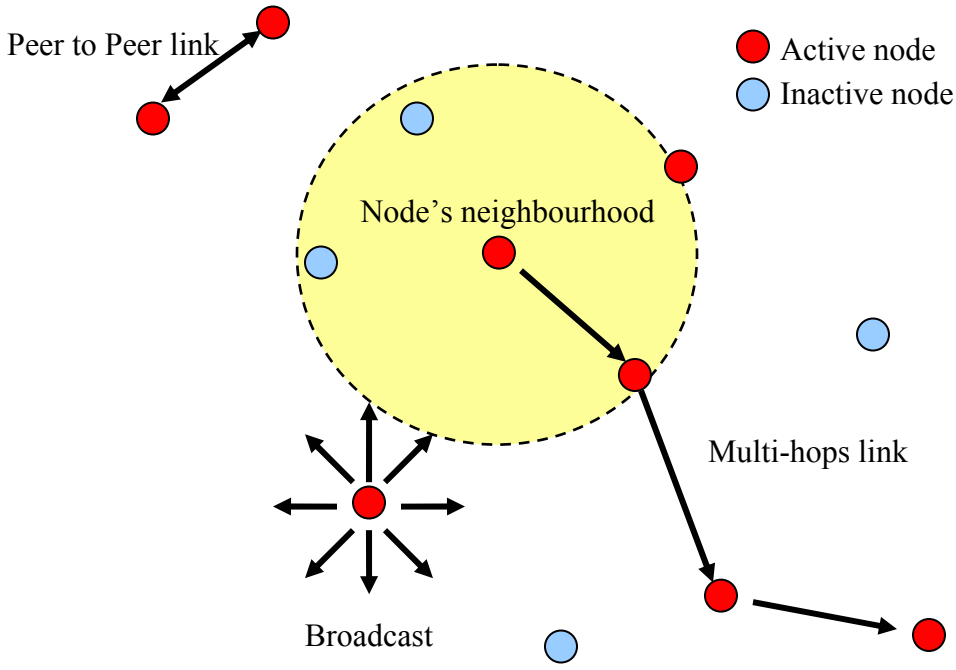


Fig 1.1: Conceptual diagram of a wireless sensor network.

Each sensor node performs several functions such as (1) sensing the physical parameters of its environment, (2) processing the raw data locally to extract the feature of interest and (3) transmitting the information to its neighbors through a wireless link. Unlike cellular networks or wireless LAN, there are no base stations or access points in wireless sensor networks. Hence, each node operates as a relay point to implement a multi-hop communication link by receiving data from one of its neighbor, and then

processing it before routing it to the next neighbor towards the destination. In some cases, more advanced functions such as data compression and encryption are also incorporated.

1.2 Challenges

For successful large scale deployment of wireless sensor networks, each node must have low power consumption, low operating and system cost and a small form factor. Fig. 1.2 shows two existing state-of-the-art wireless sensor nodes [Moteiv, Crossbow].

Fig 1.2: State-of-the art wireless sensor nodes: (left) Telos and (right) MicaZ motes.

The power, size and cost of these sensor nodes are inadequate for large scale deployment of wireless sensor networks. The electronics consume much power (10's of mW), thus requiring frequent replacement or recharging of the batteries. This makes it economically infeasible to deploy a large number of nodes as the operational cost will be too high. The node is significant in size due to the two large AA size batteries, making it difficult to embed them into the physical environment (e.g. in walls, furniture, clothing, etc). To seamlessly integrate these nodes into our environment, the node size ideally needs to be less than $1cm^3$. These nodes are also assembled from a large number of components and ICs, resulting in sub-optimal performance and high system cost. These

shortcomings clearly illustrate that further research is necessary to reduce the power, size and cost of wireless sensor nodes and understand their trade-offs to achieve the optimal performance. These challenges and tradeoffs are discussed as follows.

1.2.1 Available Power

Successful large scale deployment wireless sensor nodes require them to be energy self-sufficient for their entire useful lifetime. Otherwise, the operational cost of replenishing their energy source will be enormous, especially when deployed in areas that are not readily accessible. Some applications dictate a node lifetime to last up till ten years (e.g. seismic detection in buildings), and this can impose severe constraints on the node's power consumption. The available power is determined by the power density and the size of the energy source. Table 1.1 shows the power density of several possible low cost energy sources for powering a sensor node [Roundy05]. These sources can be classified as an energy storage device (battery) or energy scavenging device (solar cells, vibration and air flow converters).

Table 1.1: Average power density of energy sources for WSN.

Energy Source	Average Power Density	Usage Lifetime
Lithium battery	100 $\mu W/cm^3$	1 year
Solar cell	10 $\mu W/cm^2$ (indoor) – 15 mW/cm^2 (outdoor)	Very long*
Vibration converters	375 $\mu W/cm^3$	Very long*
Air flow converters	380 $\mu W/cm^3$	Very long*

* Lifetime is determined by the time to failure of the conversion device.

Among all the energy sources, the battery is the most versatile since its operation is relatively independent of its operating environment. However, its average power density is only 100 $\mu W/cm^3$ per year. For a small sensor node (e.g. ~1 cm^3), the amount of stored energy is not sufficient to operate the node for a long period of time. On the other hand, energy scavenging devices typically have a higher power density and a longer usage lifetime (until it fails) but their performance depend on specific environmental conditions. For example, solar cells perform well under strong sunlight and can be used to power sensor nodes placed near the windows, on the rooftop or outdoors during the day. Air flow energy scavengers require strong air movement and can be deployed in air-conditioning ducts. Vibrational converters work best with strong vibrations and can be employed in sensor nodes mounted on mechanical machines.

Currently, there is no universal energy source since none of the energy sources possess high energy density, long usage lifetime and are yet versatile simultaneously. Hence, it is likely that sensor nodes will be powered by a combination of different types of energy sources. One such hybrid power source is to use solar cells to charge the battery and power the node during the day, and employs the battery to operate the node at night. Combining both the energy storage and energy scavenging sources, the average power consumption of a $1cm^3$ sensor node is ~100μW. This severe power requirement is the most challenging constraint and it greatly influences the design and implementation of wireless sensor nodes.

1.2.2 Cost

Widespread deployment of wireless sensor networks is only feasible if the cost of the sensor nodes is negligible, i.e. the electronics are disposable. This translates to a target price of less than $1 per node. However, today's commercial wireless sensor nodes are priced at much more than $1 per node [Crossbow, Moteiv, Dust]. To further understand the reasons behind the high cost, consider the implementation of a state-of-the-art wireless sensor node [Moteiv] as shown in Fig. 1.3.

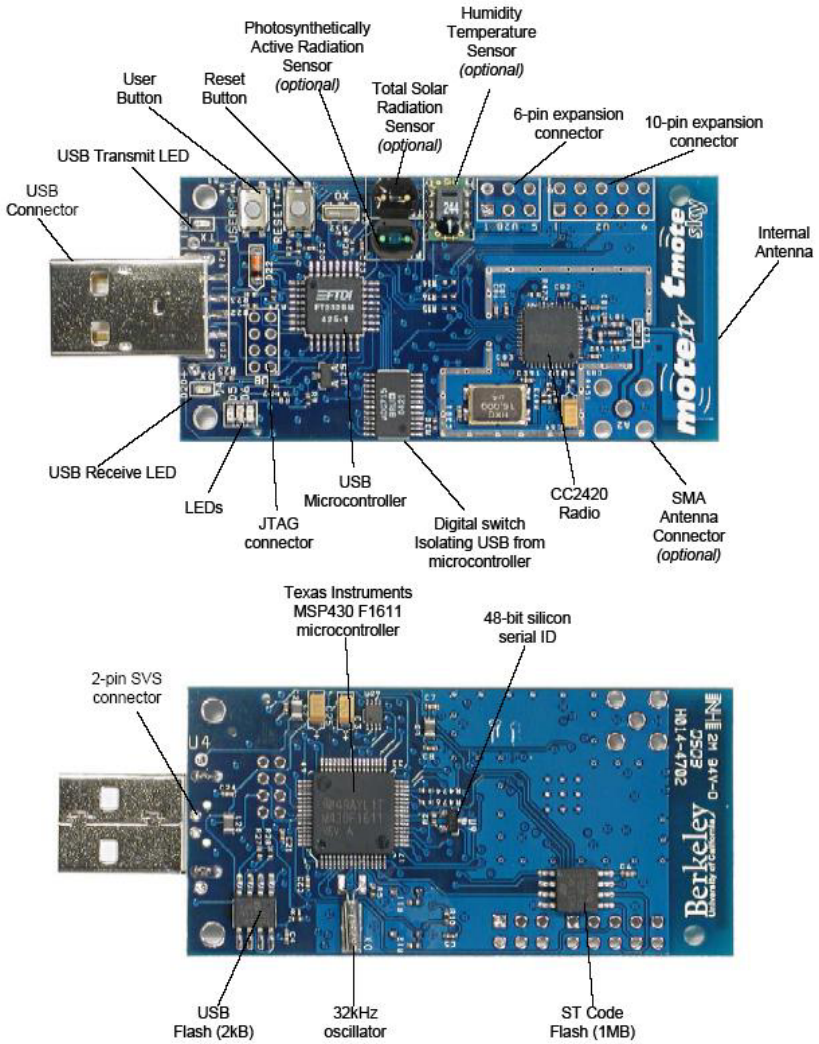


Fig. 1.3: Telos Node: (top) front side, (bottom) back side of the node.

As shown in Fig. 1.3, the sensor node consists of many ICs: radio, micro-controller, USB controller, crystal oscillator, flash memory, etc. In addition, these ICs require many other external components (e.g. capacitors, resistors, inductors). Clearly, this implementation does not yield the lowest cost solution. Achieving the target node price requires (1) using lowest cost chip fabrication, packaging and assembling technologies, (2) high integration to minimize the number of components and chips, (3) using inexpensive external components if they are unavoidable, (4) small die area, (5) large volume production to benefit from the economics of scale, and (6) high manufacturing yield.

1. Single Chip Solution

To achieve a low system cost, the digital, analog and RF circuitry should be integrated onto a single die. Amongst today's chip fabrication technologies, deep submicron CMOS process offers the highest integration at the lowest cost. Deep submicron CMOS transistors are fast enough to implement RF circuits and they offer the highest density digital circuits.

However, the submicron CMOS process also has its disadvantages. One key issue is its high leakage power. Since a sensor node is heavily duty-cycled, it spends most of its time in the sleep state, resulting in a high leakage power. To reduce leakage power, leakage reduction techniques such as high threshold voltage transistors, stacked devices, back-gate biasing and power supply gating can be employed [Borkar04]. However, these techniques lead to a higher cost and complexity.

Submicron CMOS process also gives rise to new challenges in analog/RF circuit design [Yue05]. Its low supply voltage limits the available voltage headroom in analog circuits and reduces the dynamic range of A/D converters. Submicron MOSFET has lower intrinsic gain, poorer matching characteristics and higher 1/f and thermal noise. Its thin gate oxide also reduces the ESD design window of ESD protecting circuits [Mergens05].

One key challenge in fully integrated mixed signal IC is the isolation between circuit blocks [Yue05]. The low resistive silicon substrate limits the isolation between the digital and analog/RF circuits and results in coupling of digital noise to sensitive analog and RF circuits. Noise coupling also occurs through the supply, ground, package and bond wires. To mitigate these unwanted effects, techniques such as differential topology to reject common mode noise, short bond wires to minimize inter-wire coupling, separate supply and ground for critical blocks to eliminate supply noise coupling, and guard rings and separate well to isolate sensitive blocks can be employed. Again these techniques require higher power consumption, die area, cost, complexity and more package pins.

2. Integration of Off-chip Components

To reduce the bill of materials, it is essential to integrate as many external components as possible onto the silicon IC. Examples of such components are inductors, capacitors and TX/RX switch. Due to the finite density of on-chip capacitor, up to 10's pF of capacitance can be integrated on-chip with a reasonable die area. Higher density capacitance with lower parasitic can be obtained with special process options but at a higher wafer cost. The insertion loss of an integrated TX/RX switch is much higher than

its off-chip counterpart, resulting in poorer noise figure and higher power dissipation. Fortunately, the capacitance density of on-chip capacitor and on-resistance of MOSFET transistor improve as CMOS technology scales.

While the size of digital circuits and on-chip capacitors benefits from technology scaling, on-chip inductors do not. Generally, the size of an (on-chip) inductor increases with the value of inductance. Hence transceiver architectures/circuits that require fewer inductors and smaller inductance are preferred to achieve a small die size. However, there exists inherent tradeoffs between the inductance required, power dissipation and carrier frequency. From antenna theory, the effective antenna capture area is inversely proportional to the square of the frequency f [Balanis97]. Hence, for the same receiver sensitivity, a higher carrier frequency requires a higher transmit power to maintain the same signal-to-noise ratio. Also, the power consumption of the circuits increases as the carrier frequency increases. Hence, from the power perspective, a lower carrier frequency is desirable. However, the inductance needed to resonate with a given capacitance C is given as $\frac{1}{(2\pi f)^2 C}$. Table 1.2 shows the inductance needed to resonate with 1pF of capacitance at various ISM bands. It shows that a higher operating frequency requires smaller inductance, but at the expense of a higher radiated power. Considering that a transceiver typically requires a few inductors (e.g. in matching networks and LC tanks), the maximum area per inductor is limited to about 500x500 μm^2 for a reasonable die size. This translates to a maximum inductance of ~ 10nH. Given the trade-offs between power consumption, die size and feasibility of inductor integration, a good compromise is to operate at the 2.4 GHz ISM band. The 2.4 GHz band also has another

advantage of being an ISM band in many countries (US, Europe, Japan, China, etc), which maximizes the portability of the wireless sensor nodes.

Table 1.2: Inductor integration and power consumption tradeoffs

ISM frequency, f	Inductance needed to resonate with 1pF of capacitance (nH)	$\frac{P_{rad,\min} \text{ at freq } f}{P_{rad,\min} \text{ at } f = 915MHz}$
915 MHz	30	1
2.4 GHz	4.4	7
5.2 GHz	0.94	32

Another key limitation of on-chip inductor is its low Q-factor. An on-chip inductor in a standard digital submicron CMOS process typically has a low Q-factor of about 5 to 8 [Niknejad98]. This limits the performance of RF circuits and results in higher losses in matching networks and LC tanks. Adding thick metals layers improve the Q-factor to about 15 to 20 but at the expense of a higher wafer cost. Alternatively, bond wires, which have Q-factor ~30 to 40, can be used for small inductances but they have higher manufacturing variations and are more susceptible to noise coupling from adjacent bond wires.

1.2.3 Form Factor

For a seamless integration of sensor nodes into our physical environment, the node size should be less than 1cm^3. The size of today's sensor nodes (see Fig 1.2) are about 30 cm^3. This large form factor makes it infeasible to embed sensor nodes in many applications (e.g. in clothing), thus limiting the full potential of ambient intelligence.

The size of a sensor node is mainly determined by (1) size of energy storage and/or energy scavenging device, (2) antenna dimensions and (3) footprints of its components.

The size of the energy storage or energy scavenging device depends on its energy density and the node's average power consumption. Although the power density of the energy sources has improved over the last few years, shrinking the node size still requires aggressive reduction of the average power consumption. As discussed, the node's power consumption trades off with its operating frequency, degree of integration and cost. In today's sensor nodes, the node size is dominated by the energy source as the average power consumption is much higher than the threshold of 100μW to enable energy scavenging.

The antenna also occupies a significant area/volume of the node. An efficient antenna requires dimensions in the order of $\lambda/4$ to $\lambda/2$, where λ is the operating wavelength. Hence, there exists an inherent trade off between antenna efficiency, antenna size, power consumption and operating frequency. At 2.4 GHz, $\lambda/4 \approx$ 3cm and hence on-chip antenna is not feasible. To reduce cost, printed antennas on PCB can be employed.

At low integration levels, the size and number of external components can also take up a large percentage of the area/volume of the node. Thus, a high degree of integration is crucial to both cost and size reduction. If external components are absolutely needed, low profile, small footprints components are preferred.

1.3 The Need for High Performance Transmitters in WSN

Between sensing, computational and communication, the power consumption needed for communication typically dominates node's power budget. To overcome this bottleneck, it is crucial to reduce the transceiver's power dissipation. Table 1.3 shows a breakdown of the current consumption of a state-of-the-art sensor node [Moteiv] when active. It shows that power consumption of the transmitter and receiver when active is about the same. While techniques for reducing the receiver's power consumption have been discussed in [Otis05a, Molnar04], the research in this thesis focuses on reducing the transmitter's power consumption.

Table 1.3: Nominal current consumption of a state-of-the-art sensor node when active

Components	Active current consumption (mA)	Condition
Transmitter	17.4	0 dBm output power
Receiver	19.7	-94 dBm RX sensitivity
Microprocessor	0.5	3V supply, 1MHz clock
Sensors	< 0.03	-
Voltage regulator	0.02	-

1.4 Transmitter Requirements

The main functions of a WSN transmitter are to: (1) modulate the baseband data onto a RF carrier, (2) amplify the modulated signal, and (3) provide matching to the antenna for efficient power delivery to free space. In this section, the requirements of WSN transmitter are delineated.

1.4.1 Radiated Power

The minimum radiated power $P_{rad,min}$ needed for communication between two nodes is governed by the link budget, which is given as

$$P_{rad,\min} = \left(\frac{4\pi f}{c}\right)^2 \bullet \left(\frac{d^n}{G_t G_r}\right) \bullet R_{sens} \bullet LF \,, \tag{1.1}$$

where f is the operating frequency, d is the distance between two nodes, G_r and G_t are the antenna gain of the receiver's and transmitter's antennas respectively, R_{sens} is the receiver sensitivity, c is the speed of light, n is the path loss exponent and LF is the loss factor accounting for other losses (e.g. matching, cable loss, etc).

For WSN applications, an isotropic antenna (G_r and G_t, = 1) is desired as the relative orientation between sensors nodes are not predetermined. Also, multi-path is more severe in indoor environment and the path loss exponent n is typically between 3 and 4 [Rappaport02]. For a range of about 10m, a 2.4GHz communication system requires about 0 dBm of transmit power [Rabaey02, 802.15.4].

1.4.2 Efficiency

With power consumption being the biggest obstacle in large scale deployment of WSN, one of the most important performance metrics of a WSN transmitter is its efficiency. Figure 1.4 shows average transmitter power consumption as a function of its efficiency for various duty cycles when radiating 0 dBm. If the transmitter power consumption accounts for up to 20% of the 100μW power budget, the transmitter has to be at least

25% and 50% efficient for a 0.5% and 1% duty cycle respectively. For a given transmitter power budget, a higher duty cycle demands a higher transmitter efficiency since the transmitter remains active for a longer period of time.

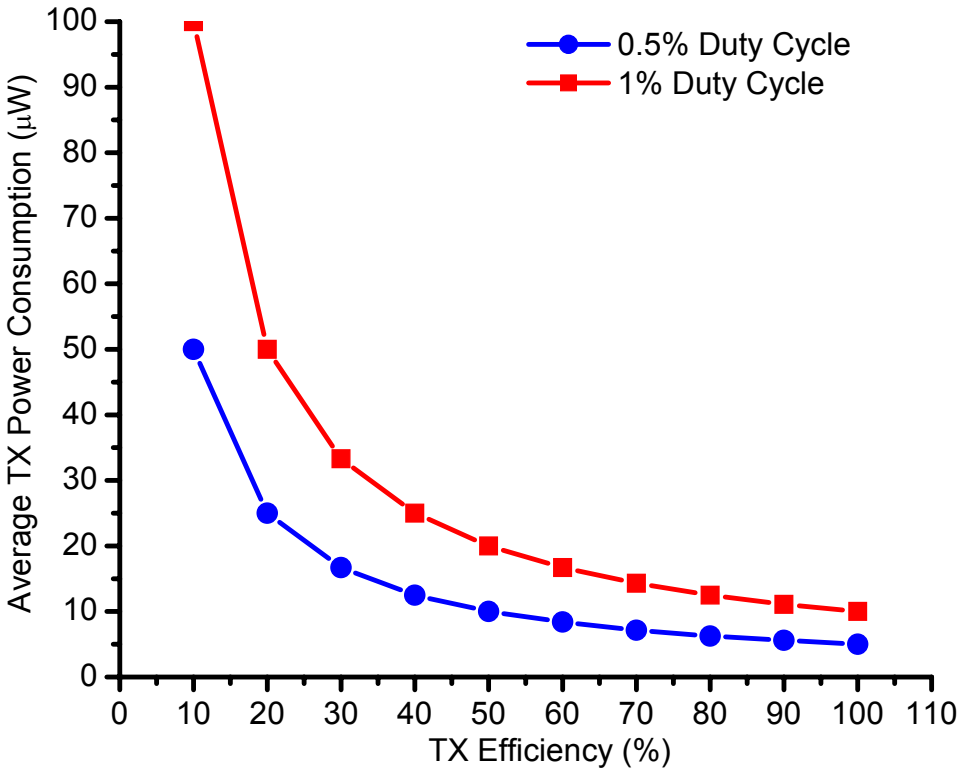


Fig. 1.4: Average TX power consumption as a function of its efficiency.

1.4.3 Integration

To reduce the system cost, the antenna matching network has to be integrated on-chip to achieve a single chip solution. However, on-chip inductors have low Q-factors and thus, results significant matching network loss. Also, these inductors occupy significant die area. Hence, there is a tradeoff between reducing the bill of materials, power consumption and die area.

Integrating the low power amplifier and frequency generation circuit on the same die can potentially cause local oscillator (LO) pulling [Razavi98]. The output power from the power amplifier can coupled to the LO through the substrate, package or bond wires and shift the frequency of the LO, causing spectrum re-growth. Thus, careful layout and package pins assignment to isolate the power amplifier and oscillator should be employed.

1.4.4 Data Throughput

In typically deployment scenarios, the parameters of interest (e.g. temperature, humidity, pressure) vary relatively slowly with time. Hence, sensor data only need to be acquired periodically at a relatively low rate (e.g. once per second) or when triggered by an occasional external events. In addition, the packet size is usually less than 1000 bits. With data rates of 10's to 100's kbps, this translates to a duty cycle of ~ 0.1% to 10%.

1.5 State-of-the-Art

There already exist some efforts to overcome the challenges in designing low cost, high efficiency and small form factor transmitters for WSN applications. These transmitters either adapt existing transmitter architectures that work well for WLAN and cellular transceiver to WSN applications or utilize the inherent characteristics of WSN to reduce its complexity and power consumption. In this section, two of these state-of-the-art WSN transmitters are reviewed.

1.5.1 Direct Conversion Transmitter

The block diagram of a direct conversion transmitter is shown in Fig. 1.5. It uses two mixers to up convert the baseband signal to the RF band with a pair of quadrature LO signals. This solution is very versatile as it supports any modulation scheme. However, it requires more circuit blocks (mixers and quadrature LO generator, low pass filters, etc), which results in a high overhead power and low transmitter efficiency.

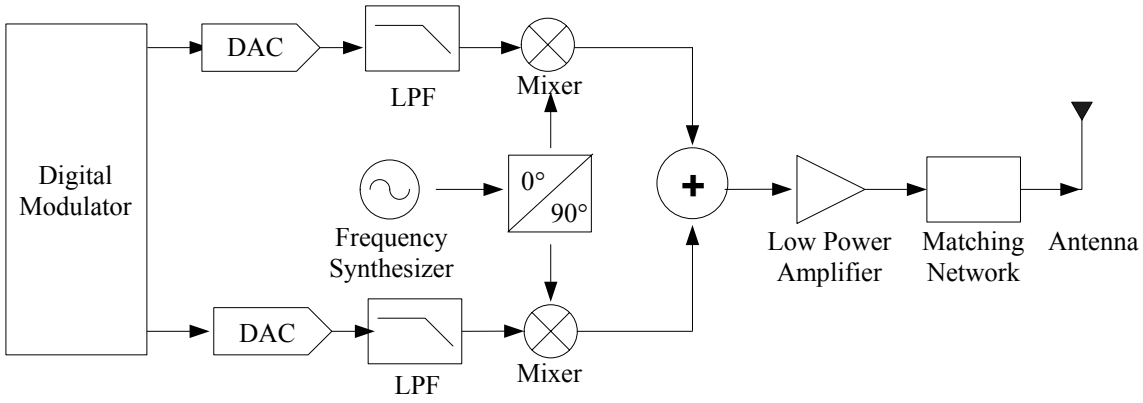


Fig 1.5: Block diagram of a direct conversion transmitter.

An example of a WSN transmitter that uses this architecture is described in [Choi03]. The author implemented a 2.4 GHz direct conversion transmitter for WSN in a 0.18μm CMOS process. The transmitter consumes 30mW while delivering 0 dBm to the antenna, resulting in an overall transmitter efficiency of only 3.3%. A breakdown of the power consumption when active is shown in Fig. 1.6. It shows that the low efficiency is due to the low power amplifier efficiency and high power consumption by all the stages prior to the power amplifier. In addition, the phase-lock loop in the frequency synthesizer requires a long settling time of 150μs, incurring a high overhead power. The transmitter

uses an off-chip antenna matching network and supports a data rate of 250kbps with GMSK modulation.

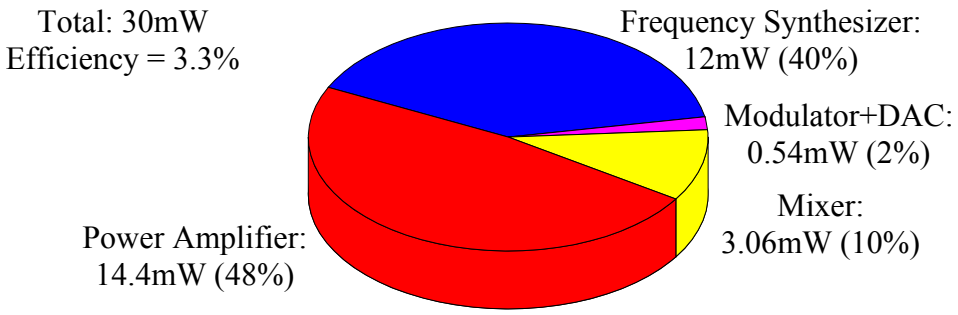


Fig 1.6: Power breakdown of direct conversion transmitter in [Choi03].

1.5.2 Direct Modulation Transmitter

Taking advantage of the low data rate requirement for WSN applications, simpler modulation schemes such as on-off keying (OOK) or frequency shift keying (FSK) can be employed at the expense of spectral efficiency. These simpler modulation schemes allow the use of the less complex direct modulation transmitter as shown in Fig. 1.7.

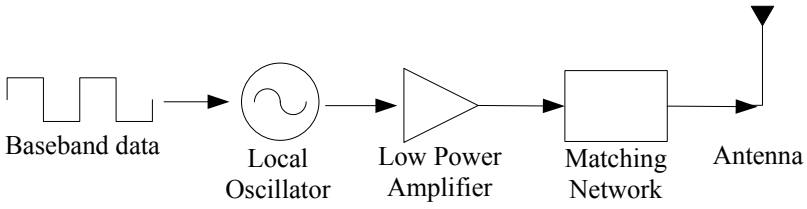


Fig 1.7: Block diagram of the direct modulation transmitter.

In the direct modulation transmitter, the baseband data directly modulates the local oscillator. FSK is achieved by modulating the frequency of the LO, while OOK is

accomplished by power cycling the transmitter. The direct modulation transmitter uses fewer circuit blocks and hence incurs less overhead power.

In the WSN transceiver described in [Molnar04], the author employs the direct modulation transmitter architecture. The 900MHz FSK transmitter consumes 1.3mW while radiating 250μW. In the transmitter, the author stacked the output devices to provide for better antenna matching and achieve a power amplifier efficiency of 40%. However, the high power consumption the LO (accounts for 55% of the power budget) degrades the overall efficiency to only 19%. The transmitter could deliver 0 dBm by operating the two stacked power amplifiers in parallel and combining their output power, resulting in an overall transmitter efficiency of 13%. The transmitter supports a data rate of 100kbps and requires 1 external inductor.

1.6 Contributions and Scope of this Thesis

The previous sections have discussed the three main challenges in widespread deployment of wireless sensor networks: (1) node's average power consumption has to be less than 100μW for a long usage life time, (2) node's cost has to be less than $1 for a reasonable system cost and (3) node's volume has to be less than $1cm^3$ for a seamless integration with our environment. The power consumption of today's sensor nodes far exceeds the threshold of 100μW, mainly due to the high power consumption need for communication between nodes. With the transmitter accounting for about half the communication power budget when active, it is important to have a highly integrated and efficient transmitter with a fast start-up time to reduce power consumption.

Unfortunately, none of the state-of-the art transmitters meets the stringent requirements of a WSN transmitter.

This thesis focuses on providing a solution to this problem. It contributes to the advancement of transmitter design for wireless sensor network in three major thrusts:

1. Establish the principles and techniques of a high performance WSN transmitter.

Traditional transmitter design in cellular and WLAN applications focuses mainly on improving the power amplifier's efficiency to boost the overall efficiency. However, the radiated power in WSN is low and these transmitters perform poorly when adapted to WSN applications due to their high overhead power and long settling time. Thus, achieving a high performance WSN transmitter requires rethinking of the transmitter design principles and techniques.

Considering the unique requirements and operating environment of WSN, the main design principles to achieve a high performance WSN transmitter are established: (1) minimize overhead power, (2) maximize circuit efficiency, (3) minimize active time, and (4) radiate the minimum power need for communication. Based on these principles, low power design techniques at the system, circuit and technology levels are investigated. Adhering to these design principles and techniques result in a high efficiency, low power, low cost and small form factor transmitter.

2. Push the performance envelope of WSN transmitters.

To demonstrate the effectiveness of these low power design principles and techniques, three different 1.9 GHz transmitters are designed and implemented in ST Microelectronics 0.13μm digital CMOS process. The first transmitter is based on the direct modulation architecture It employs a MEMS resonator (FBAR) and the transmit chain is co-designed together to achieve an efficiency of 23% while transmitting 0.5mW. The transmitter supports a maximum data rate of 83kbps. The second transmitter employs injection locking to reduce the FBAR oscillator power further, improving the efficiency to 28% while delivering 1mW and increasing the data rate to 156kbps. The third transmitter incorporates the antenna into the power amplifier design to eliminate the matching network, boosting the efficiency to 46% while radiating 1.2mW. It uses dual amplifiers during oscillator startup, improving the data rate to 330kbps. The performance of these transmitters compare favorably to the state-of-the-art as shown in Fig 1.8.

The improvements in TX efficiency and data rate lead to a reduction of the transmitter average power consumption $P_{TX,ave}$. Table 1.4 shows the $P_{TX,ave}$ for a typical WSN traffic load of 1 pkt/sec with 1000 bits/pkt, assuming that data has an equal probability of '1' and '0'. It shows that $P_{TX,ave}$ of the transmitters in [Choi03], [CC2420], [CC1000] and [TR1000] exceed the threshold of 100μW for an energy self-sufficient node. The transmitter in [Cho04] consumes 72% of the entire node's power budget, leaving little room for other circuitry. On the other hand, the transmitters reported in this thesis and [Molnar04] consume less than 13% of the power budget, making them suitable for WSN applications. In particular, the active antenna transmitter has the lowest $P_{TX,ave}$ of 4μW.

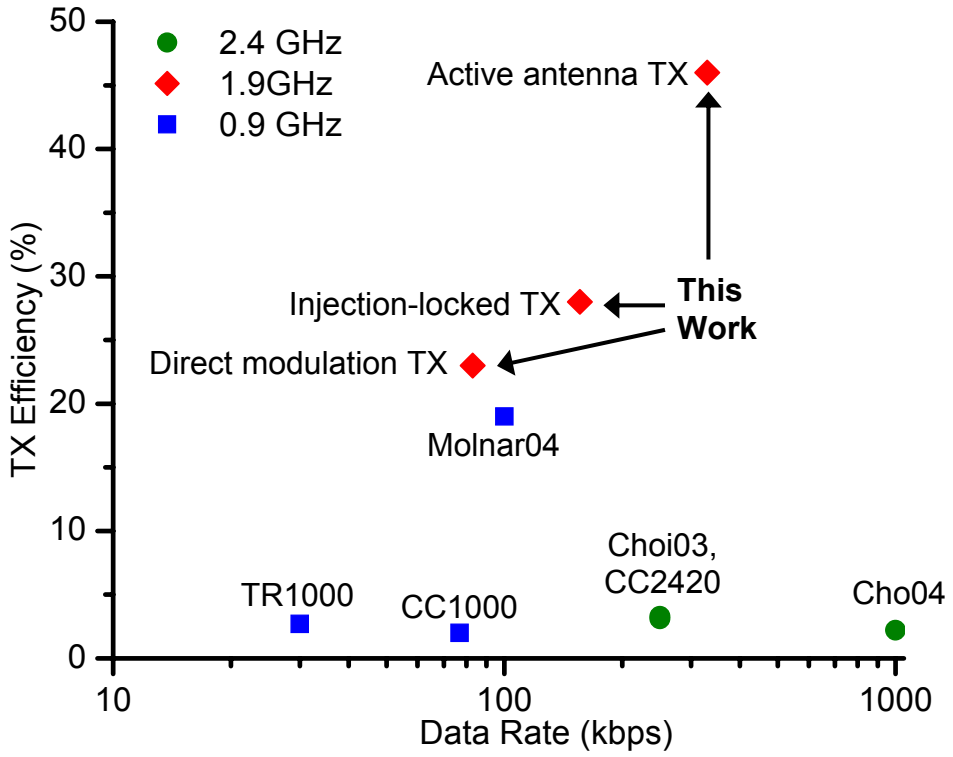


Fig 1.8: Performance of state-of-the-art WSN transmitters.

Table 1.4: Average TX power $P_{TX,ave}$ for traffic load of 1 pkt/sec, 1000 bits/pkt

Transmitter	Modulation	Standard	P_{rad} (mW)	$P_{TX,ave}$ (μW)
Active antenna TX	OOK	Propriety	1.2	4
Injection-locked TX	OOK	Propriety	1	11
Direct modulation TX	OOK	Propriety	0.5	13
[Molnar04]	FSK	Propriety	0.25	13
[Cho04]	GFSK	Bluetooth	1	72
[Choi03]	GMSK*	802.15.4	1	120
[CC2420]	OQPSK	802.15.4	1	129
[CC1000]	FSK	Propriety	1	651
[TR1000]	OOK	Propriety	1.4	870

P_{rad} : Radiated power; *Experimental work targeted for 802.15.4

3. Demonstrate a fully functional transmit sensor node.

As a proof of concept of a low power, low cost and small form factor sensor node, the active antenna transmitter is integrated into a wireless transmit sensor node. The 38 x 25 x 8.5 mm^3 sensor node runs on two small rechargeable batteries and it has power conversion circuits, a low power microcontroller, an active antenna transmitter, a printed antenna and three sensors to measure temperature, humidity, tilt and acceleration. In this design, the batteries are recharged from solar cells but it can be adapted to operate with other energy scavenging sources.

The remaining parts of the thesis elaborate on these contributions and are organized as follows. Chapter 2 explains the principles and design techniques to achieve a low power, low cost and small size WSN transmitter. Based on these principles and design techniques, three different transmitters are designed and implemented. In chapter 3, a direct modulation transmitter utilizing RF MEMS is presented. In this transmitter, the oscillator and low power amplifier are co-designed together for optimal efficiency. Chapter 4 introduces the use of injection locking technique to reduce the overhead power to further enhance the efficiency and increase the data rate. In chapter 5, the antenna is incorporated into the power amplifier to eliminate the matching network and its loss, further improving the performance of the transmitter. Dual amplifiers are also employed during startup to boost the data rate further. Chapter 6 describes the design of a highly integrated low power, low cost and small form factor energy self-sufficient transmit sensor node.

Chapter 2

Energy Efficient Transmitter Design

2.1 Design Principles

Consider modeling a transmitter as a power amplifier (PA) providing power amplification, an output network matching the antenna to the PA and a pre-PA block accounting for all the stages prior to the PA (pre-PA stages) that perform data modulation and carrier generation as shown in Fig. 2.1.

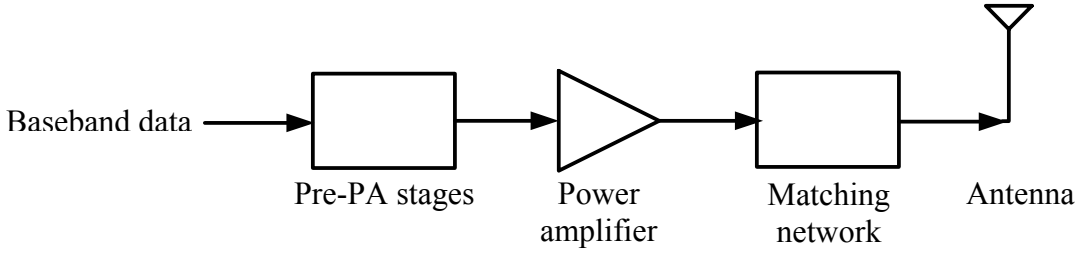


Fig. 2.1: Model of a wireless transmitter.

The average power consumption of the transmitter $P_{TX,ave}$ is given as:

$$P_{TX,ave} = \frac{T_{setup} \bullet \left[P_{\Pr e-PA} + P_{PA,inactive}\right] + T_{transmit} \bullet \left[P_{\Pr e-PA} + \frac{P_{rad}}{\eta_d \bullet \eta_{MN}}\right]}{T_{data}}, \quad (2.1)$$

where T_{setup} is the transmitter setup time, $T_{transmit}$ is the data transmission time, T_{data} is the duration between data packets, $P_{PA,inactive}$ is the PA power consumption when it is not transmitting, $P_{Pre\text{-}PA}$ is the power consumption of the pre-PA stages, P_{rad} is the radiated power, η_d is the PA drain efficiency and η_{MN} is the matching network efficiency. Certainly, a lower packet rate or packet size reduces the average power consumption but they are usually determined by non-transmitter related factors such as the MAC protocol, synchronization header, error correction bits, payload and allowable latency. Thus, for a given packet size and packet rate, minimizing the transmitter energy consumption requires:

1. minimizing the overhead power: $P_{Pre\text{-}PA}$ and $P_{PA,inactive}$,
2. minimizing losses in the power amplifier's device and matching network,
3. minimizing the duration which the transmitter is active: T_{setup} and $T_{transmit}$
4. radiating the minimum power required for the communication link: P_{rad}

Adhering to these design principles leads to an energy efficient transmitter. Though these principles are universal to all transmitters, their relative importance is different for a WSN transmitter compared to cellular/WLAN transmitters due to different requirements. In cellular/WLAN applications, the radiated power is much higher than then circuit power and hence the transmitter's power consumption is dominated by the power amplifier. On the other hand, the WSN transmitter requires lower radiated power due to shorter communication distance, lower power consumption to enable energy scavenging, lower data rate and faster wake up time. These unique requirements require re-thinking

of the design methodology, transmitter architectures, circuit techniques and new enabling technologies to achieve an ultra low power and low cost WSN transmitter.

2.2 Design Considerations

2.2.1 Design Methodology

In cellular and WLAN applications, P_{rad} is large (~ 100's of milliwatts to 1 watt). Thus $P_{rad} >> P_{Pre\text{-}PA}$ and PA efficiency dominates the transmitter efficiency. Hence, the research efforts mainly focus on improving the PA efficiency and techniques to obtain high efficiency at large power back off (e.g. when operating close to the access point or base station) to achieve low transmitter power dissipation. However, in WSN applications, P_{rad} is much smaller (~1mW) due to a shorter communication distance. Since $P_{Pre\text{-}PA}$ is independent on the communication range, it becomes comparable or larger than P_{rad}. When $P_{Pre\text{-}PA}$ dominates, equation (2.1) becomes $P_{TX,ave} \approx DC_{TX} \bullet P_{Pre-PA}$, where $DC_{TX} = (T_{setup} + T_{transmit})/T_{data}$ is the transmitter duty cycle. Therefore, reducing P_{rad} (e.g. by improving the receiver sensitivity with higher receiver power) or improving the PA efficiency no longer gives significant power savings. This is the main reason for the low efficiency in existing transmitters as they all suffer from high $P_{Pre\text{-}PA}$. ***Hence it is critical to first achieve a low $P_{Pre\text{-}PA}$ for a WSN transmitter***.

When $P_{Pre\text{-}PA}$ power is reduced to less than P_{rad}, improving the PA efficiency and decreasing P_{rad} using power control techniques become effective in reducing the average power consumption. However, a more efficient PA often requires higher drive requirements, which translate to higher $P_{Pre\text{-}PA}$. This makes it challenging to design an

efficient transmitter at low radiated power, since it must have both a high efficiency PA and low pre-PA power simultaneously. ***This requires optimizing the entire transmit chain concurrently, rather than just the power amplifier alone.***

2.2.2 Transmitter Architectures

Existing state-of-the-art transmitters suffer from low efficiency because of their high pre-PA power. Pre-PA power arises from the data modulation and carrier generation circuits. Thus, the most effective way to reduce the pre-PA power is to ***employ a transmitter architecture that minimizes the number of pre-PA circuit blocks and their power consumption.***

1. Direct Conversion Transmitter

The direct conversion transmitter, shown in Fig. 2.2, employs two mixers to up convert the baseband signal to the RF band with a pair of quadrature LO signals. This architecture is very versatile as it supports any modulation schemes and very high data rates. However, it requires many circuit blocks with some blocks such as the frequency synthesizer and mixers being very power hungry. This result in high pre-PA power and poor transmitter efficiency as evident in the transmitters reported in [Choi03] and [CC2420], whose efficiencies are only ~3.3%.

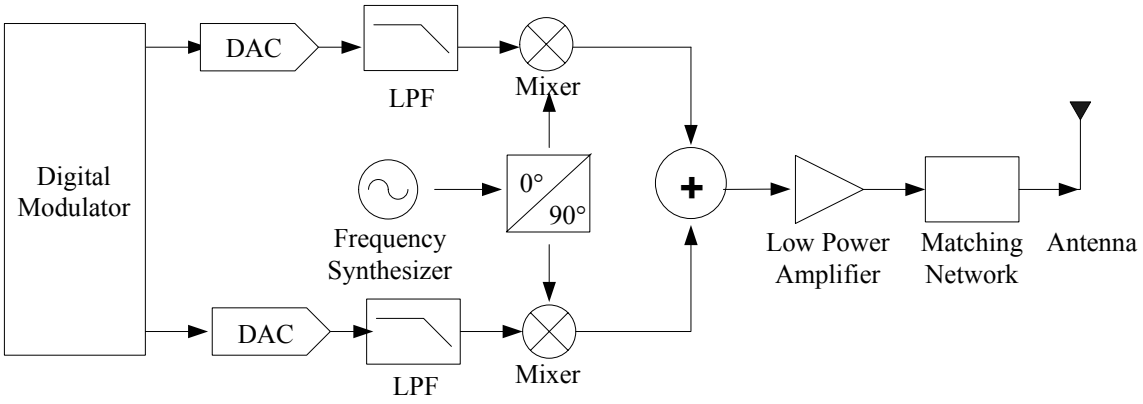


Fig 2.2: Block diagram of the direct conversion transmitter.

2. Direct Modulation Transmitter

In WSN applications, the data rate does not need to be very high due to the low data throughput. With lower data rate, simpler modulation schemes such as on-off keying (OOK) and frequency shift keying (FSK) can be employed. These schemes allow the use of the less complex direct modulation transmitter as shown in Fig. 2.3.

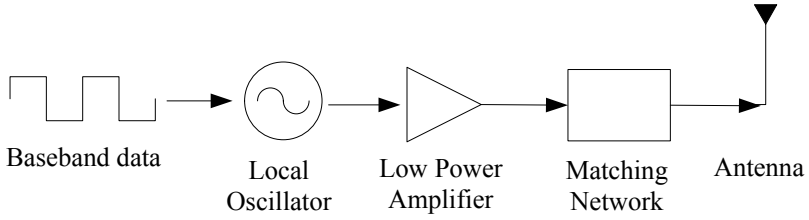


Fig. 2.3: Block diagram of the direct modulation transmitter.

In the direct modulation transmitter, the baseband data directly modulates the local oscillator. This eliminates the power hungry digital modulator, DACs, I/Q mixers and I/Q generation circuit, resulting in lower pre-PA power and higher transmitter efficiency. FSK is achieved by modulating the frequency of the LO, while OOK is accomplished by power cycling the transmitter. Also, both OOK and FSK relax the PA linearity

requirement and allow the use of more efficient PA. The design and implementation of a direct modulation transmitter is discussed in Chapter 3.

3. Injection Locked Transmitter

Often, a higher efficiency PA requires higher drive requirements, leading to a higher pre-PA power. To achieve a better compromise between the pre-PA power and PA efficiency, the injection locked transmitter shown in Fig. 2.4 can be employed.

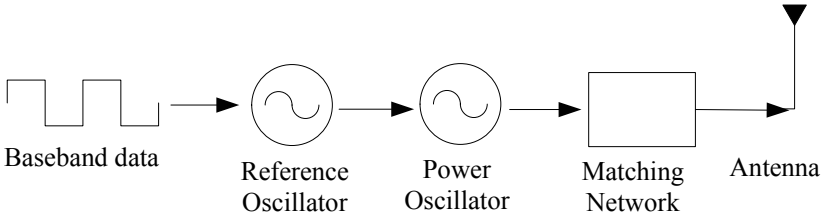


Fig. 2.4: Block diagram of the injection-locked transmitter.

In the injection locked transmitter, the power amplifier is replaced by an efficient power oscillator. The power oscillator is self-driven and does not load the reference oscillator. Due to its low output tank Q, the power oscillator suffers from poor phase noise performance and has an unstable RF carrier. To obtain an accurate carrier frequency, the power oscillator is locked to a low power reference oscillator. Baseband data is modulated onto the carrier by power cycling the power oscillator for OOK. FSK can be employed by tuning the frequency of the local oscillator. The design and implementation of an injection locked transmitter is presented in Chapter 4.

4. Active Antenna Transmitter

One of the key factors limiting the transmitter efficiency is its matching network loss. The matching network, consisting of inductors and capacitors, transforms the 50Ω antenna to the optimal impedance that maximizes the PA efficiency. However, on-chip inductors suffer from low Q-factor and have significant power loss. To overcome this problem, the active antenna transmitter shown in Fig. 2.5 can be employed.

In this architecture, the antenna provides the optimal impedance to the power amplifier and the matching network is eliminated. Thus, no matching network loss is incurred and higher efficiency is obtained. FSK is achieved by modulating the frequency of the LO, while OOK is accomplished by power cycling the transmitter. The design and implementation of an active antenna transmitter is described in Chapter 5.

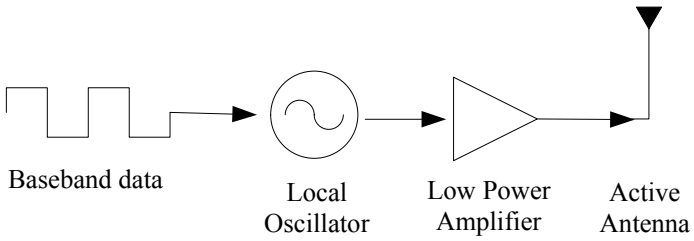


Fig. 2.5: Block diagram of the active antenna transmitter

2.2.3 Active Time

In wireless sensor network, the transceiver is heavily duty cycled and the transmitter has to wake up, transmit the data and then goes back to sleep for a long time before the next data transmission. Equation (2.1) shows that the average power consumption is proportional active time of the transmitter, which comprises of the setup time T_{setup} and the transmit time $T_{transmit}$.

1. Transmit Time

For a given packet size and packet rate, the transmit time is inversely proportional to the data rate for OOK and FSK modulation. To maintain the same energy per bit, P_{rad} has to increase proportionally as data rate increases (see Fig. 2.6). On the other hand, $P_{Pre\text{-}PA}$ increases only slightly at higher data rates since the oscillator only need to consume more current during start up to reach its steady state faster to support higher data rates and the startup time is only a small fraction (e.g. 10%) of the bit period. Hence, $P_{Pre\text{-}PA}$ is relatively independent of the data rate as compared to P_{rad}.

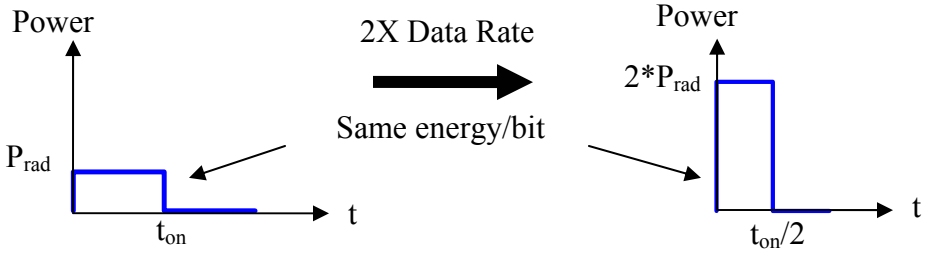


Fig. 2.6: Effect on increasing data rate on transmit power.

Thus, the average power consumption of the transmitter $P_{TX,transmit}$ during data transmission as a function of data rate can be modeled to the first order as:

$$P_{TX,transmit} = \frac{PS \bullet PR}{DR} \bullet \left[P_{Pre-PA} + \frac{1}{\eta_d \bullet \eta_{MN}} \frac{P_{rad,ref}}{DR_{ref}} DR \right]$$

$$= PS \bullet PR \bullet \left[\frac{P_{Pre-PA}}{DR} + \frac{1}{\eta_d \bullet \eta_{MN}} \frac{P_{rad,ref}}{DR_{ref}} \right] \qquad (2.2)$$

where PS is the packet size, PR is the packet rate, DR is the data rate, $P_{rad,ref}$ is the reference radiated power when transmitting at the reference data rate DR_{ref} to achieve the desired signal to noise ratio at the receiver. Equation (2.2) shows that a higher data rate

decreases the overall power consumption by reducing the duration in which the pre-PA stages stay active. With increasing data rate, the impact of $P_{Pre\text{-}PA}$ diminishes and the transmitter approaches its minimum achievable $P_{TX,transmit}$ given by the second term of equation (2.2). Fig. 2.7 shows $P_{TX,transmit}$ as a function of data rate for various $P_{Pre\text{-}PA}$ assuming PR = 1 pkt/sec, PS = 500 bits, $P_{rad,ref}$ = 1mW, DR_{ref} = 250kbps, η_d = 0.4 and η_{MN} = 0.8.

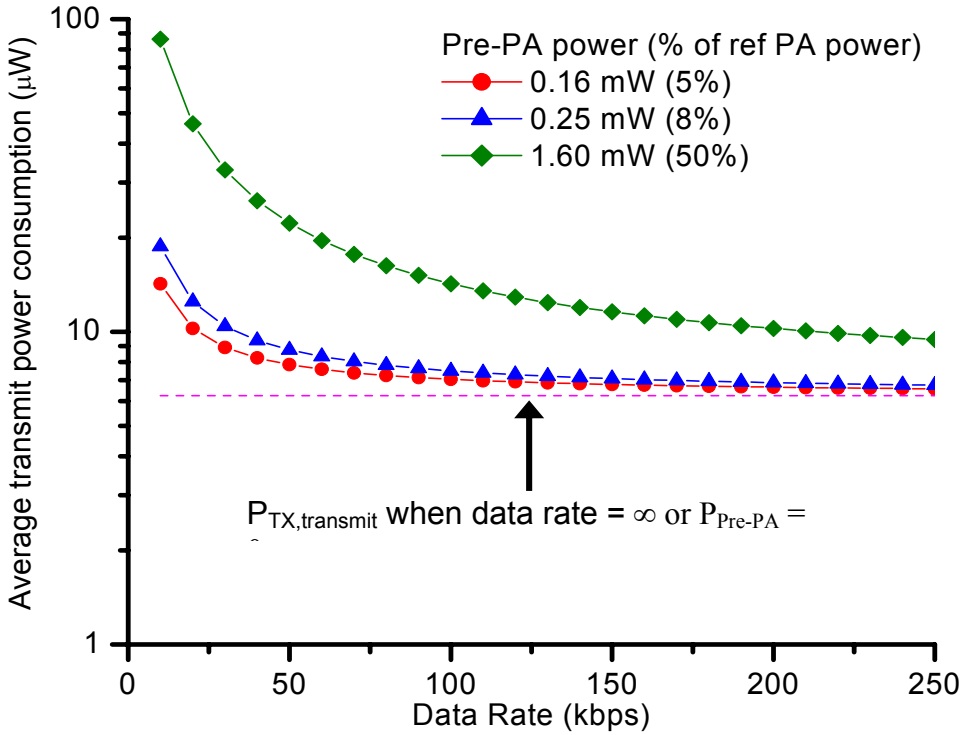


Fig. 2.7: Average transmitter power consumption as a function of data rate.

It shows that increasing the data rate is effective in reducing $P_{TX,transmit}$ when $P_{Pre\text{-}PA}$ is significant. For example, when $P_{Pre\text{-}PA}$ is 50% of the reference PA power ($P_{PA,ref} = \frac{P_{L,ref}}{\eta_d \eta_{MN}}$), the average power consumption reduces from 86μW to 9μW when the

data rate increases from 10 kbps to 250 kbps. Further increase in the data rate continues to yield a lower power consumption but at a diminishing rate. With smaller $P_{Pre\text{-}PA}$, the transmitter enjoys less power savings with increasing data rate. For instance, when $P_{Pre\text{-}PA}$ is 5% of the reference PA power, increasing the data rate higher than 130 kbps does not result in significant power savings as $P_{TX,transmit}$ is already within 10% of the minimum achievable $P_{TX,transmit}$.

Although increasing the data rate reduces the transmitter power consumption, it also increases the power consumption in other parts of the transceiver. A higher data rate requires a tighter constraint on timing recovery, channel equalization to combat inter-symbol interference, higher A/D sampling rate and possibly requiring more complex modulation schemes to improve spectral efficiency. All these stricter requirements lead to higher complexity and power. Thus, the power savings in the transmitter due to higher data rate has to be weighed against the increase in power in other parts of the transceiver.

Setup time

The setup time comprises of the transmitter wake up time and turnaround time when the transceiver switches from the receiver to the transmitter. Since no data transmission occurs during the wake up or turnaround period, these setup times constitute an overhead and should therefore be minimized.

If $P_{Pre\text{-}PA}$ is significant and the setup time dominates the transmit time, equation (2.1) shows that $P_{TX,ave} \approx \left(T_{setup} \bullet P_{Pre-PA}\right) / T_{data}$. In this case, increasing the data rate does not result in power savings since setup time is independent of the data rate. Thus, it is

crucial to reduce the setup time to be much less than the transmit time. For example, it takes only 1 millisecond to transmit a 200 bits packet with a data rate of 200kbps. If 10% overhead is acceptable, the wakeup time has to be less than 100 μs. This imposes strict requirements in the frequency synthesizer as it typically takes 100's of microseconds to several milliseconds to startup. To overcome this problem, a RF MEMS based oscillator, which requires only a few microseconds to reach its steady state, is used for frequency generation instead. The design and implementation of the RF MEMS oscillator is presented in Chapter 3.

Another important factor in determining the transmitter setup time is the time needed the circuits to reach their biasing points. For example, the PA is ready for data transmission only after its gate voltage reaches the desired operating bias. Often, the gate of the PA transistor is biased via a large resistor as shown in Fig. 2.8. This resistance and the total capacitance at the gate node determine the time constant for the gate voltage to reach its steady state. Thus, it is important to ensure that this time constant is much less than the transmit time.

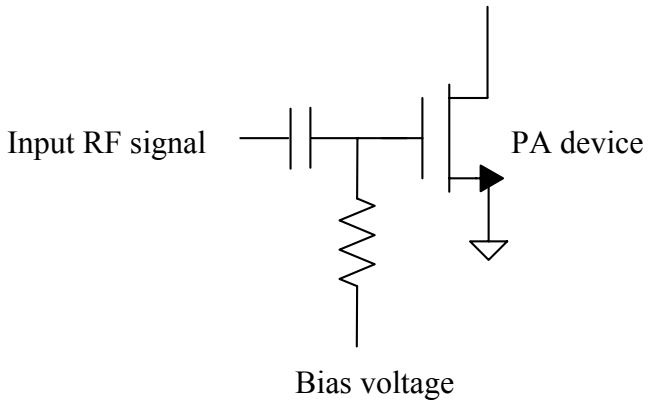


Fig 2.8: Typical biasing technique for a power amplifier

2.2.4 Power Control

When two nodes are located close to each other or experience a good channel response between them (e.g. line of sight between the two nodes), P_{rad} can be reduced. Equation (2.1) shows that power control is effective in reducing the average power consumption only when $P_{Pre\text{-}PA} << P_{rad}$. Power control can be achieved by changing the (1) bias current of the power amplifier, (2) the supply voltage of the power amplifier, (3) the impedance transformation ratio of the matching network or (4) combining the output power from multiple devices.

2.3 Low Power Circuit Techniques

2.3.1 Subthreshold MOSFET Operation

With technology scaling, the transit frequency f_T of today's submicron CMOS transistors exceeds 100 GHz. This made it possible to design GHz circuits using MOSFET operating in the subthreshold regime, which has higher transconductance efficiency (g_m/I_d). Transconductance efficiency is important since the performance of many analog/RF circuits is related to device g_m and a higher g_m/I_d allows the circuit to achieve the same performance at lower power. Fig. 2.9 shows the g_m/I_d and f_T as a function of the inversion coefficient of a submicron NMOS transistor.

The inversion coefficient IC measures the degree of inversion in the channel of a MOSFET. It is defined as [Enz95]

$$\mathrm{IC} = \frac{1}{2n\mu C_{ox} V_{th}^2}\left(\frac{I_d}{W/L}\right), \tag{2.3}$$

where n is the subthreshold slope factor, μ is the electron mobility, C_{ox} is the gate capacitance per unit area, $V_{th} = kT/q$ is the thermal voltage, W and L are the transistor's width and length respectively and I_d is the MOSFET drain current,. IC << 1 signifies weak inversion, IC ≈ 1 represents moderate inversion and IC >> 1 indicates strong inversion. Fig 2.9 shows that as IC decreases, g_m/I_d increases but f_T decreases. A good tradeoff between g_m/I_d and f_T is to operate the MOSFET in the moderate inversion regime, where the inversion coefficient is about 1. Further decrease in the inversion coefficient gives only marginal increase in g_m/I_d but substantial decrease in f_T.

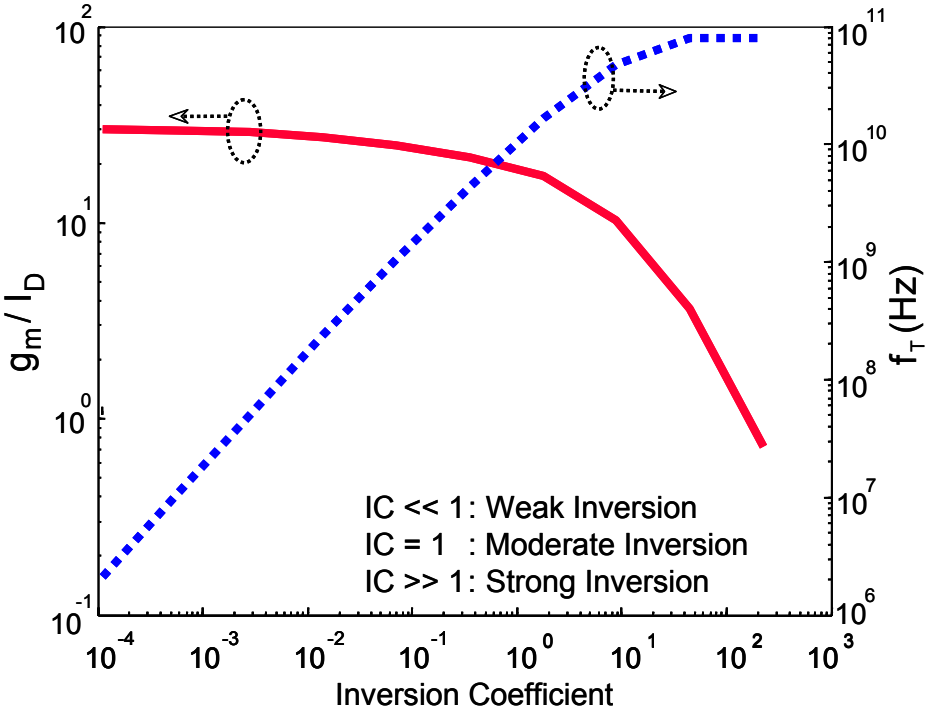


Fig. 2.9: g_m/I_d and f_T versus inversion coefficient of a submicron NMOS transistor.

2.3.2 Supply Voltage Reduction

For analog and RF circuits, decreasing the supply voltage V_{dd} reduces the power consumption since it is proportional to V_{dd}. For digital circuits, the power consumption is proportional to V_{dd}^2. A lower V_{dd} also reduces the electric fields in the device and improves its long term reliability. However, reducing V_{dd} limits the dynamic range of the ADC and reduces the voltage headroom needed for the cascode transistors in analog/RF circuits.

2.4 Enabling Technologies – RF MEMS

Recent advances in MEMS technology have made it possible to design and fabricate MEMS devices that operate at RF frequency. RF MEMS devices offer potential for integration and miniaturization, lower power consumption, lower losses, higher linearity, higher Q-factors than conventional communications components [Bouchaud05]. They also enable new transceiver's architectures that are easily reconfigurable and operate over a wide frequency range [Nyguen04]. Examples of such RF MEMS devices are RF MEMS switches, BAW and micro-mechanical resonators, tunable capacitors, micro-machined inductors, micro-machined antennas, micro-transmission lines, micro-mechanical resonators, cavity resonators. In this research work, the film bulk acoustic resonator (FBAR), which is one type of BAW resonator, is employed to overcome some of the challenges of WSN transmitters.

2.4.1 FBAR Resonator

The FBAR resonator [Ruby01] consists of a thin layer of Aluminum-Nitride piezoelectric material sandwiched between two metal electrodes. The entire structure is supported by a micro-machined silicon substrate as shown in Fig. 2.10. The metal/air interfaces serve as excellent reflectors, forming a high Q acoustic resonator. The FBAR has a small form factor and occupies only about 100μm x 100μm.

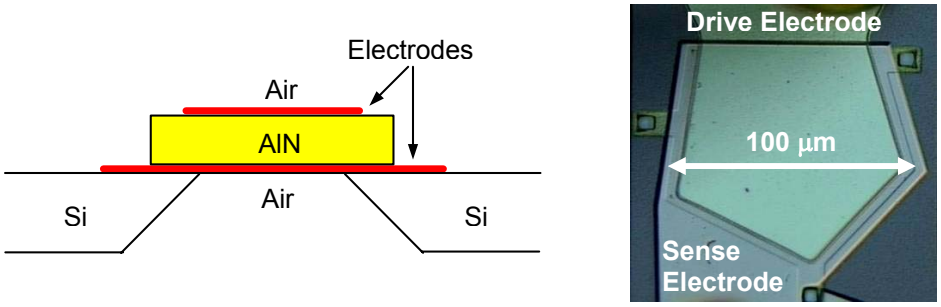


Fig. 2.10: (Left) structure (right) photograph of a FBAR resonator.

The FBAR resonator can be modeled using the Modified Butterworth Van Dyke circuit as shown in Fig. 2.11 [Larson00]. L_m, C_m and R_m are its motional inductance, capacitance and resistance respectively. C_o models the parasitic parallel plate capacitance between the two electrodes and C_{p1} and C_{p2} accounts for the electrode to ground capacitances. Losses in the electrode are given by R_0, R_{p1} and R_{p2}.

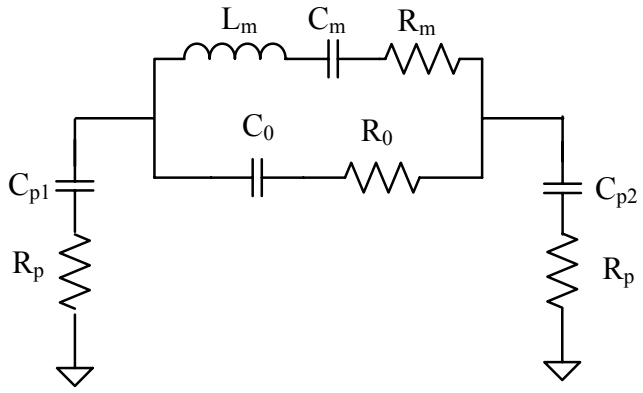


Fig. 2.11 Circuit model of the FBAR resonator.

The frequency response of the FBAR resonator is shown in Fig. 2.12. The FBAR behaves like a capacitor except at its series and parallel resonance. It achieves an unloaded Q of more than a 1000.

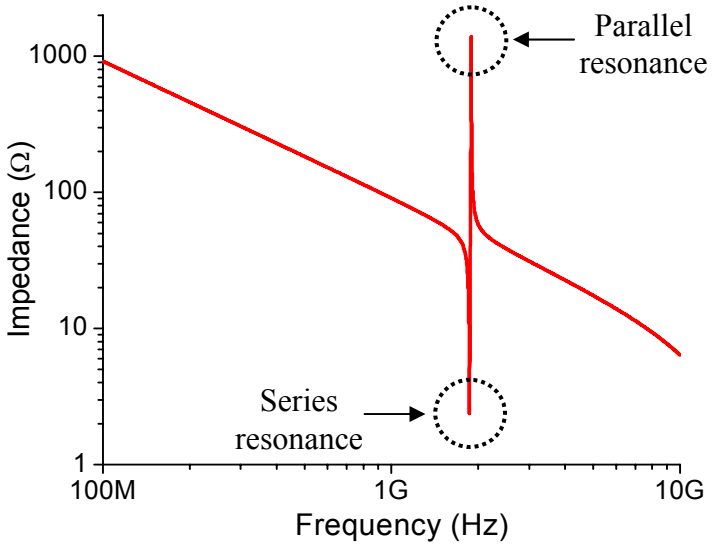


Fig. 2.12 Frequency response of the FBAR resonator.

2.4.2 Advantages of FBAR Resonator

1. High Q factor

The Q factor of the FBAR resonator is more than 1000, which is much higher than the Q-factor of an on-chip LC resonator. The high Q factor allows implementation of low loss filters and duplexers to attenuate the out of band blockers and reject the image signals. In some applications, the bandwidth of these FBAR filters is sufficiently small for channel filtering, relaxing the linearity requirement of mixers and removing the need for baseband/IF filters. The high Q FBAR resonator also substantially improves oscillator's phase noise and reduces its power consumption. It could also potentially

replace the traditional frequency synthesizer, resulting in substantial power savings, shorter startup time and RX/TX turnaround time.

2. CMOS Process Integration

The FBAR resonator occupies only 100μm x 100μm, which is smaller than the size of an on-chip inductor at 2 GHz. Unlike SAW and ceramic resonators, the material and fabrication thermal budget of the FBAR resonator are compatible for CMOS post processing, making them amenable to CMOS integration. Fig. 2.13 shows one such monolithic integration where the WCDMA RF front end uses an integrated BAW filter to relax the linearity requirements of the mixers [Carpentier05]. The BAW filter consists of eight BAW resonators, which are fabricated above the final BiCMOS passivation layer and connected to the integrated circuit through its top metal layer of the IC. This integration results in smaller form factor, lower power, greater reliability and higher performance circuits.

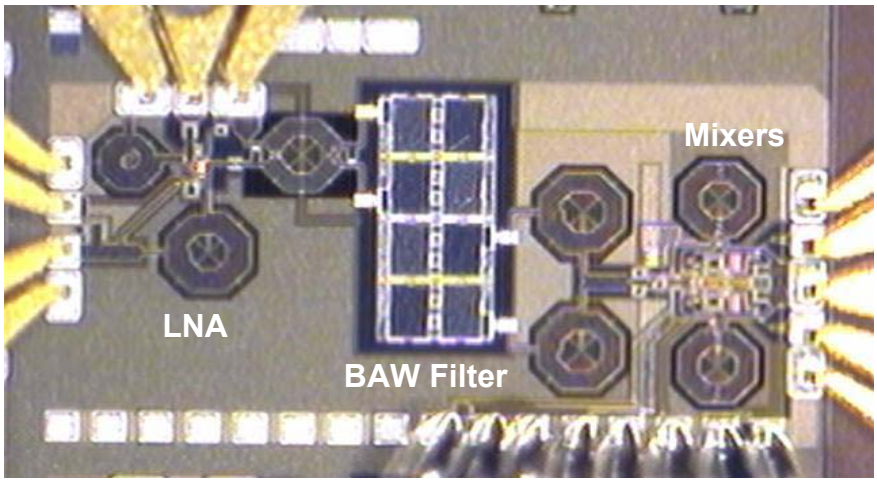


Fig 2.13: Monolithic integration of FBAR with integrated circuits.

3. Circuit/MEMS Co-design

With monolithic integration, the physical dimension of the FBAR can be easily tailored to achieve the optimal terminating impedance and frequency response for different circuits. This enables circuits/MEMS co-design to achieve better performance at lower power consumption. This is certainly advantageous compared to off-chip SAW and ceramic resonators, which have a 50 Ω terminating impedance and frequency response that is pre-determined by the manufacturer. In addition, off chip resonators are bulky and expensive.

Chapter 3

Direct Modulation Transmitter

At low radiated power, the direct conversion transmitter suffers from low efficiency due to its high pre-PA power. To overcome this problem, the direct modulation transmitter can be employed. This chapter presents the design and implementation of a FBAR-based direct modulation transmitter [Otis05b]. The direct modulation transmitter eliminates the I/Q mixers, DACs and digital modulator, and replaces the power hungry frequency synthesizer with a low power FBAR oscillator to reduce the pre-PA power. The FBAR oscillator is co-designed together with the low power amplifier to optimize the entire transmit chain.

This chapter is organized as follows: the transmitter architecture is first introduced, followed by a discussion on the design of each individual circuit blocks. Then the implementation and performance of the transmitter are presented.

3.1 Architecture

The block diagram of a direct modulation transmitter is repeated in Fig. 3.1.

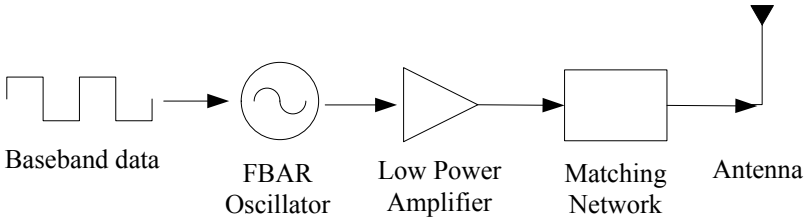


Fig. 3.1: Block diagram of FBAR-based direct modulation transmitter.

The transmitter has only two active circuit blocks - an FBAR oscillator and a low power amplifier. With fewer pre-PA circuits than the direct conversion transmitter, it has a lower pre-PA power and higher transmitter efficiency. To reduce the pre-PA power further, the power hungry frequency synthesizer is replaced by a FBAR oscillator. The high Q FBAR provides a stable carrier frequency at 1.9GHz at very low power consumption.

The transmitter employs OOK modulation by using the baseband data to power cycle the FBAR oscillator via a foot switch and the low power amplifier through a switch in its gate bias. This is preferred over power cycling the supply as the time to charge and discharge the supply's decoupling cap is much longer, limiting the data rate. FSK modulation can be employed by modifying the FBAR oscillator into a digitally controlled oscillator with a switched capacitor bank.

Employing OOK or FSK relaxes the PA linearity requirement and allows the use of more efficient switching PA. However, a switching PA typically requires a higher drive requirement, which increases the pre-PA power consumption substantially and degrades the overall efficiency. As such, a non-switching PA with lower drive requirement is employed. The FBAR oscillator is co-designed with the low power amplifier to achieve the optimal power consumption.

To match the PA to the 50 Ω antenna, a capacitive transformer is used instead of a conventional LC matching network to reduce loss. A short bond wire inductor is employed to resonate with the capacitances at the drain node of the PA device.

3.2 Low Power FBAR Oscillator

3.2.1 Low Power Oscillator Design

In the direct modulation transmitter, the pre-PA circuit consists of only the oscillator and hence, minimizing its power consumption is important. The oscillator can be modeled as an equivalent LC circuit in parallel with a conductance G representing the finite resonator Q and a negative conductance –G provided by the active circuits to compensate for the resonator loss (see Fig. 3.2). Since G is proportional to 1/Q and a larger –G requires higher current, a higher Q factor leads to lower power consumption.

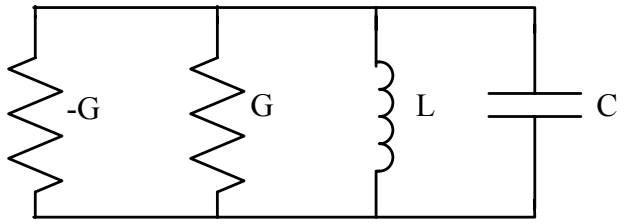


Fig. 3.2: Model of an oscillator

The Q-factor of on-chip inductors in standard CMOS process is ~ 5 to 8. The Q-factor is improved 10 to 15 with the use of thick top metal but at a higher cost. With such low Q factors, CMOS LC oscillators have high power consumption and mediocre phase noise performance. On the other hand, the Q-factor of FBAR resonator exceeds 1000 [Ruby01]. Unlike ceramic and SAW filters, it is small in size and amenable to CMOS integration. Coupled with good circuit design, this leads to low power and high

performance oscillators [Chee05a].

The schematic of the low power FBAR oscillator is shown in Fig. 3.3. The Pierce oscillator uses a CMOS inverting amplifier comprising of transistors M_1 and M_2. The FBAR is modeled using the modified Butterworth Van Dyke model [Larson00]. Capacitance C_1 and C_2 include the capacitances due to the FBAR electrodes, transistors, pad and interconnects. A large resistor R_b is used to bias the gate and drain voltage of the transistors at Vdd/2 to maximize the allowable voltage swing and minimize its loading on the FBAR. Transistors M_1 and M_2 share the same current but their transconductances g_{m1} and g_{m2} sum, reducing the current needed for oscillation by half. The transistors are also designed to operate in the sub-threshold regime to obtain higher current efficiency.

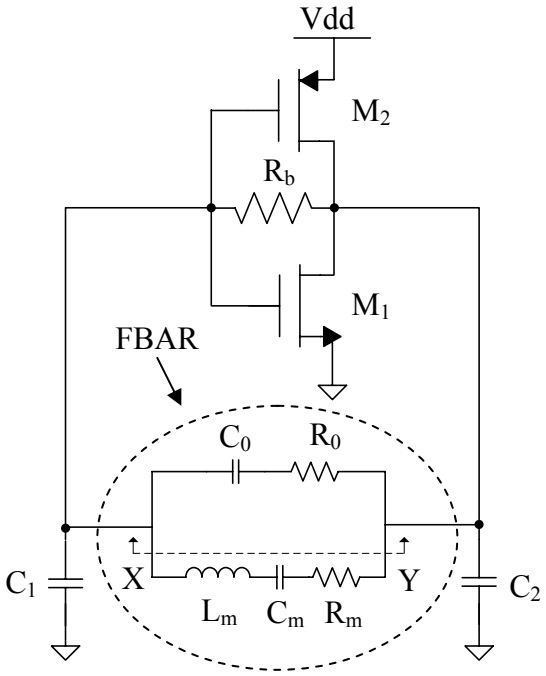


Fig. 3.3: Schematic of an ultra low power FBAR oscillator.

Capacitors C_1 and C_2 transform the amplifier's transconductance $g_m = g_{m1} + g_{m2}$ into a negative resistance $-\frac{g_{m1} + g_{m2}}{\omega^2 C_1 C_2}$ at frequency ω. Thus, a higher negative resistance

requires higher current consumption since g_m is proportional to the device current. The impedance looking across node X and node Y is the given as [Vittoz88]

$$Z_{XY} = \frac{Z_1 Z_3 + Z_2 Z_3 + g_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + g_m Z_1 Z_2} \tag{3.1}$$

where $Z_1 = \frac{1}{j\omega C_1}$, $Z_2 = \frac{1}{j\omega C_2}$ and $Z_3 = R_0 + \frac{1}{j\omega C_0}$. To ensure oscillator startup, the $Re[Z_{XY}]$ is typically 2 to 3 times higher than $-R_m$. When the output voltage swing grows to a sufficiently large amplitude, it pushes M_1 and M_2 into gain compression, which reduces g_m and $Re[Z_{XY}]$. Steady state oscillation is achieved when $-R_m$ is equal to the large signal $Re[Z_{XY}]$.

Fig. 3.4 shows a plot of $Re[Z_{XY}]$ as a function of C_1 and C_2 for g_m = 7.8mS, C_0 = 1.6 pF and R_0 = 0.6 Ω.

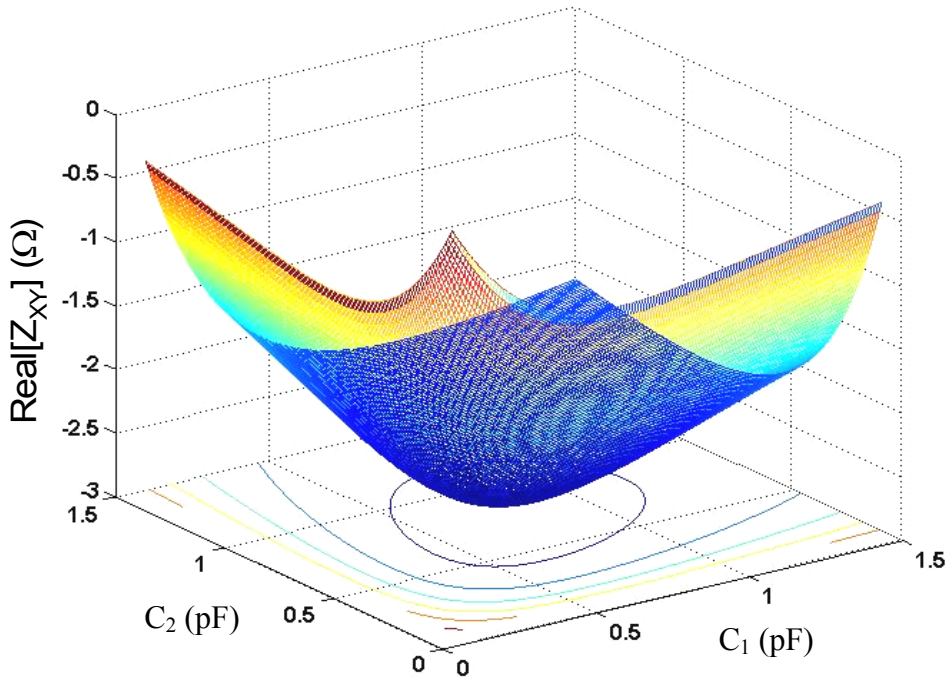


Fig 3.4: Negative resistance of FBAR oscillator as a function of C_1 and C_2.

It shows that for any given g_m, there is a pair of C_1 and C_2 that minimizes $Re[Z_{XY}]$ when $C_1 = C_2$. By varying g_m, the minimum achievable $Re[Z_{XY}]$ is be plotted as a function of g_m as shown in Fig. 3.5. With $R_m \sim 0.9\Omega$ and $Re[Z_{XY}]$ chosen to be 3 times - R_m to ensure startup, a g_m of ~ 7.8 mS is needed and the corresponding $C_1 = C_2 = 700$ fF. With current reuse using complementary devices, the transconductance of each MOSFET is 3.9 mS. For $g_m/I_d = 19$, the minimum bias current is ~ 205 μA.

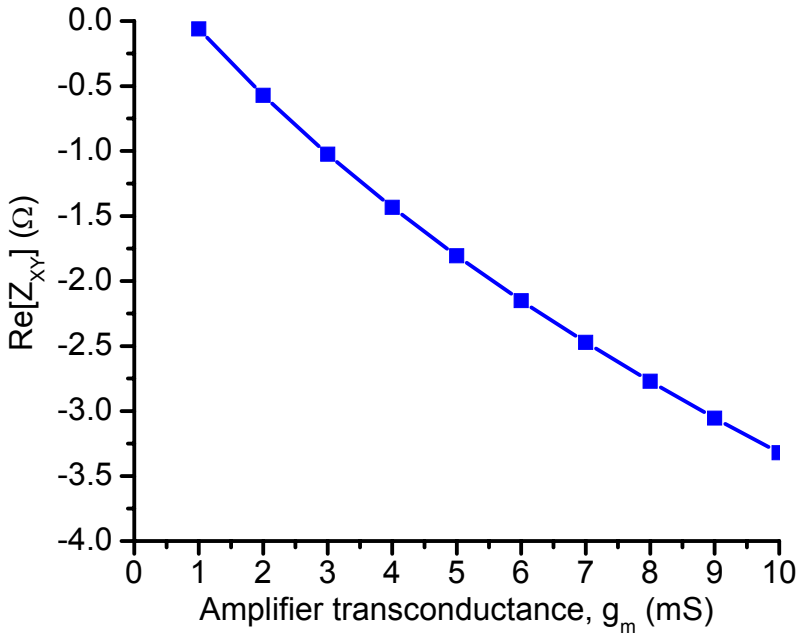


Fig 3.5: Negative resistance of FBAR oscillator versus amplifier g_m.

3.2.2 Start up time

In the direct modulation transmitter, the data rate is determined by the oscillator's startup time. The startup process of the FBAR oscillator is shown in Fig. 3.6. It consists of three phases [Toki92] describes as follows:

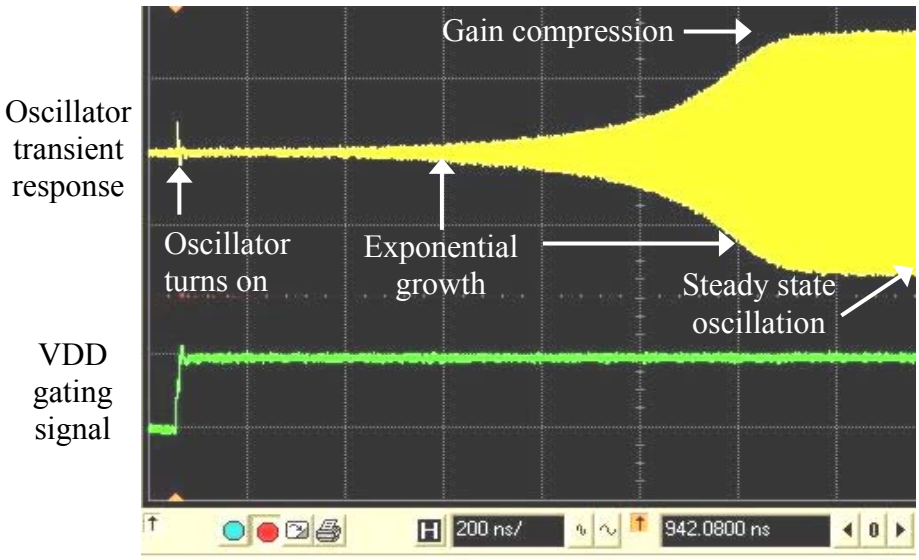


Fig. 3.6: Measured startup transients of an FBAR oscillator.

1. ***Initial power up***. When the oscillator is powered up, the supply charges the gate of the transistors to their biasing voltage through R_b with a time constant $\tau_{initial} \sim R_bC_1$. With R_b = 60 kΩ and C_1 = 700 fF, the biasing point can be reached in ~ $3*\tau_{initial}$. (~126 ns). Smaller R_b results in a shorter $\tau_{initial}$ but increases its loading on the resonator. With the FBAR impedance equals to ~ 2 kΩ at parallel resonance, R_b loads the resonator by ~ 3%.

2. ***Exponential growth***. Once the operating point is reached, the amplifier acquires sufficient loop gain and the oscillation amplitude builds up exponentially with a time constant $\tau_{exp} = -\frac{L_m}{\mathrm{Re}[Z_{XY}] + R_m}$. A higher Q resonator has a larger L_m and/or smaller R_m, which leads to a lower steady state power consumption but longer startup time for a given $\mathrm{Re}[Z_{XY}]$. For L_m = 147 nH, R_m = 0.9Ω and if $\mathrm{Re}[Z_{XY}]$ is chosen to be $-3*R_m$, τ_{exp} = 82 ns. With an initial voltage of ~1μV, it takes $12.6\tau_{exp} \approx$

1.03 μs to reach 300 mV of voltage swing. Faster startup time can be achieved by increasing Re[Z_{XY}] at the expense of a higher start-up current consumption.

3. ***Saturation***. When the output voltage is sufficiently large, it pushes the transistors into the triode region, reducing the loop gain. When the large signal Re[Z_{XY}] = -R_m, the oscillator reaches steady state. The time from the onset of gain compression to steady state is very difficult to determine analytically since it is a highly nonlinear. Based on simulation, this period is ~ 100 ns to 200 ns.

Thus, the startup time of the FBAR oscillator is ~1.25μs. If the startup time constitutes 10% of the bit period, the oscillator is able to support data rates up to 80 kbps with on-off keying modulation. To achieve a higher data rate, the startup current can be increased to achieve a faster τ_{exp}.

3.2.3 Implementation

The FBAR oscillator is implemented in a standard 0.13μm CMOS process from ST Microelectronics [Chee05a]. The FBAR resonator and the CMOS die are packaged together onto a test board using chip-on-board assembly as shown in Fig. 3.7. Two short bond wires are used to connect the FBAR to the CMOS die to minimize parasitic and avoid any spurious oscillations. Each bond wire is estimated to be ~ 250pH and is taken into account in the design. Due to the number of test and biasing pads needed, the entire CMOS oscillator occupies about 0.8 x 0.8 mm^2. When integrated as part of a transceiver, only the oscillator core is needed and it occupies 40 x 40 μm^2.

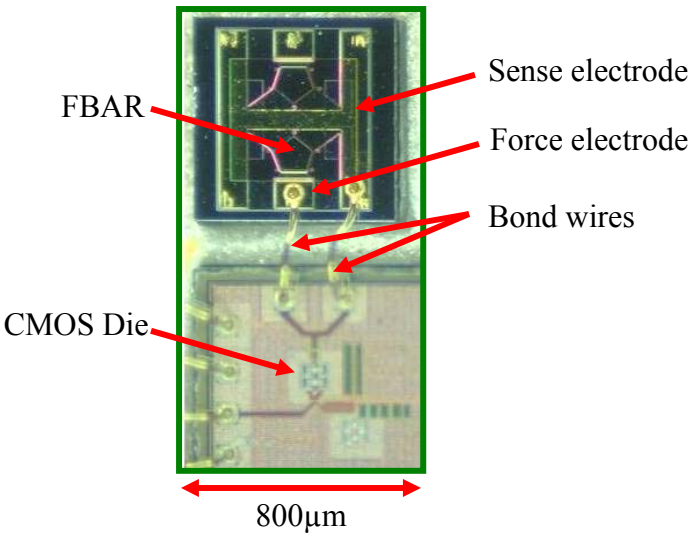


Fig. 3.7: Die photo of the FBAR oscillator

3.2.4 Measured Results

The oscillator is self-biased with a 430mV supply and dissipates 89µW for sustained oscillation at 1.882 GHz. The measured zero to peak output voltage swing is 142mV. The output spectrum of the oscillator is shown in Fig. 3.8. A clean output signal is obtained and no close-in spurs are observed. Second, third, fourth and fifth harmonics are measured to be -43.8 dBc, -45.5 dBc, -68.8 dBc and -69.7 dBc respectively.

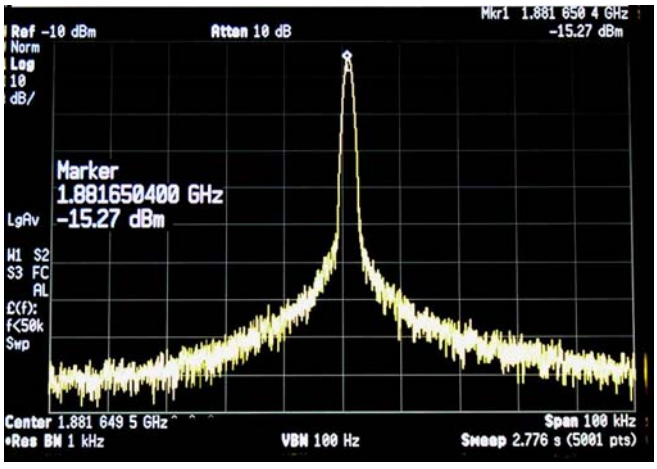


Fig. 3.8: Output frequency spectrum of FBAR oscillator.

The measured phase noise performance is shown in Fig. 3.9. The oscillator achieves a phase noise of -98dBc/Hz and -120dBc/Hz at 10kHz and 100kHz offsets respectively. The good phase noise performance is mainly attributed to the high Q FBAR resonator.

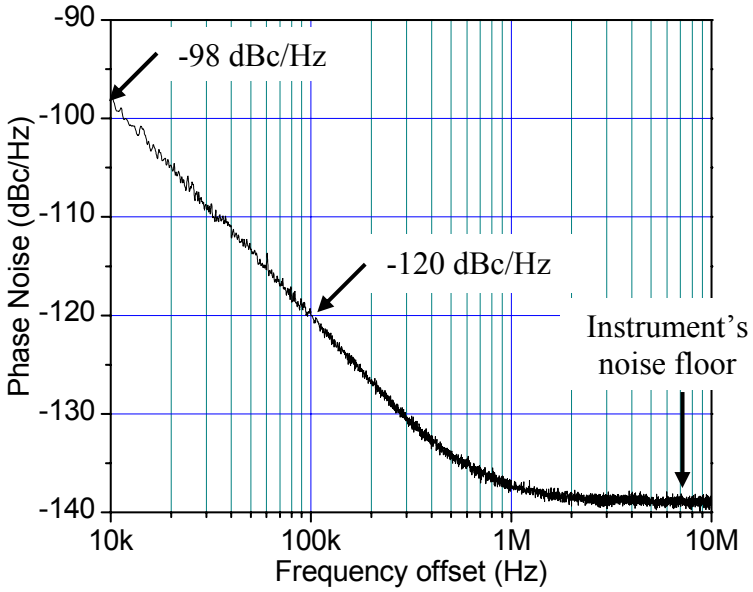


Fig. 3.9: Measured phase noise performance of FBAR oscillator.

A better phase noise performance is obtained by operating the oscillator at the edge of the current limited regime [Ham01]. Fig. 3.10 shows the output voltage swing and measured phase noise at various power consumptions. The optimal measured phase noise is -100 dBc/Hz at 10kHz offset and -122 dBc/Hz at 100kHz offset and it occurs when the output voltage swing is 167mV with the oscillator consuming 104μW. Beyond this operating point, the oscillator transits into the voltage limited regime which the transistor's output resistance decreases and loads the FBAR, resulting in a poorer phase noise performance.

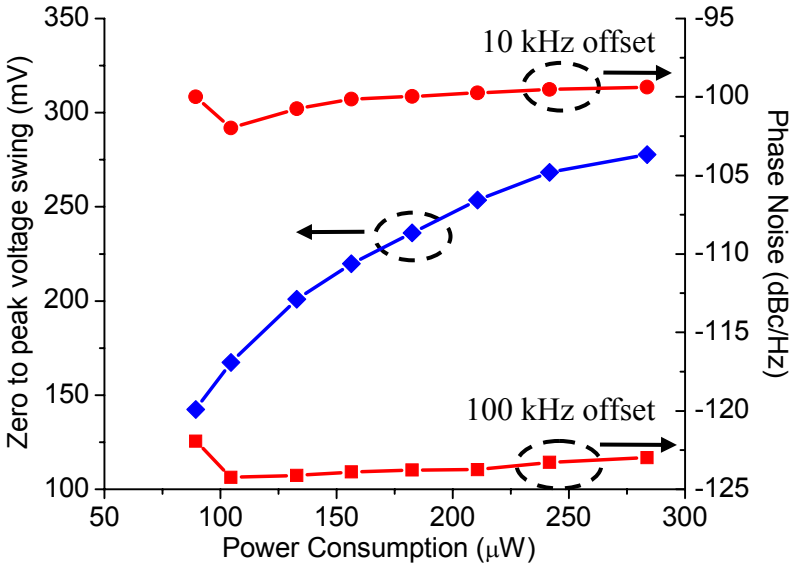


Fig. 3.10: Measured output voltage swing and phase noise performance of FBAR oscillator for various power consumptions.

To benchmark the performance of this oscillator with the existing state-of-the-art, a dimensionless power-frequency-normalized figure of merit (FOM) is used [Ham01]. The FOM is defined as:

$$\text{FOM} = 10\log\left[\frac{kT}{P_{DC}}\left(\frac{f_{OSC}}{f_{OFFSET}}\right)^2\right] - L\{f_{OFFSET}\} \tag{3.2}$$

where P_{DC} is the oscillator power consumption, $L\{f_{OFFSET}\}$ is the oscillator phase noise at an offset frequency f_{OFFSET} from its oscillation frequency f_{OSC}, k is the Boltzmann constant and T is the temperature in Kelvin. Table 3.1 shows that this FBAR oscillator has the best FOM compared to other state-of-the-art GHz-range oscillators. Its FOM is ~470 times better (~27dB) than the on-chip LC oscillator. The excellent FOM is due to the high Q FBAR and low power circuit techniques.

Table 3.1: Comparison of FBAR oscillator with state of the art.

Ref.	f_{OSC} (GHz)	P_{DC} (mW)	Phase Noise	Process (μm)	Resonator / Inductor	FOM (dB)
[Chee05a]	1.9	0.104	-122 dBc/Hz @ 100 kHz offset	0.13 CMOS	FBAR	43.64
[Otis01]	1.9	0.3	-120 dBc/Hz @ 100 kHz offset	0.18 CMOS	FBAR	37.05
[Steinkamp03]	5.8	40	-106 dBc/Hz @ 10 kHz offset	0.8 SiGe BiCMOS	SAW resonator	31.11
[Linten04]	5.8	0.328	-115 dBc/Hz @ 1 MHz offset	0.09 CMOS	Thin film inductor	21.28
[Cheng03]	2.4	39	-121 dBc/Hz @ 100 kHz offset	Si Bipolar	LTCC ceramic resonator	18.75
[Song04]	5.9	7.65	-124 dBc/Hz @ 1 MHz offset	0.18 CMOS	On-chip LC	16.89

3.3 Low Power Amplifier

3.3.1 Principles of Efficient Power Amplification

Besides reducing the pre-PA power, it is also crucial to provide efficient power amplification to minimize the PA power consumption. The schematic of a typical PA is shown Fig 3.11.

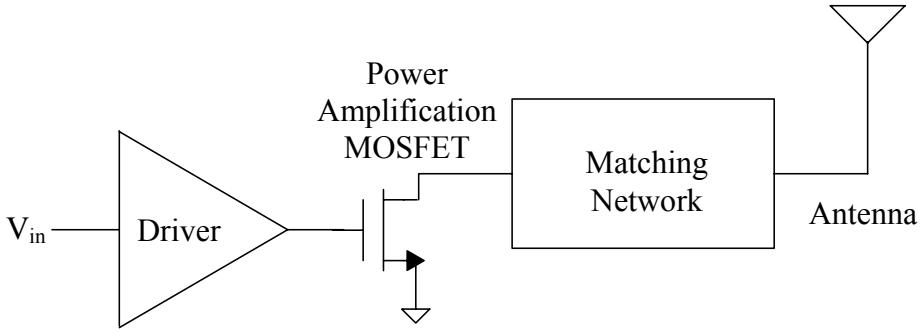


Fig 3.11: Schematic of a low power amplifier

Efficient power amplification is achieved by:

1. ***Maximizing PA transistor efficiency.*** The PA transistor typically consumes the most power and hence, it is crucial to maximize its efficiency. This is achieved by using a matching network to minimize the product of the current through the device and voltage across the device (i.e. I_{ds}*V_{ds}) and their overlap time.

2. ***Minimizing matching network loss.*** The matching network, consisting of inductors and capacitors, is used to transform the antenna impedance (e.g. 50Ω) to the optimal impedance needed to maximize the device efficiency. Due to low Q on-chip inductors, significant matching network loss can occur in a fully integrated solution. This loss can be reduced by employing higher Q off-chip or bond wire inductors, or an active antenna.

3. ***Minimizing driver power.*** At a low radiated power, the power consumption of the driver stage contributes to a significant overhead. This can be eliminated by driving the PA transistor directly with the FBAR oscillator. Though this increases the oscillator power consumption, eliminating the driver stage and co-designing the oscillator with the power amplification MOSFET leads to a more optimal solution.

3.3.2 Switching and Non-Switching Power Amplifiers

Power amplifiers can be classified as switching and non-switching power amplifiers. Switching PA operates the transistor as a switch. Since an ideal switch has either zero voltage across it or zero current through it at all times, it dissipates no power. Hence switching power amplifiers can theoretically achieve 100% efficiency [Krauss80]. In reality, component non-idealities result in losses and degrade the efficiency. Power loss occurs due to finite on-resistance of the switch, finite Q of inductors and capacitors in the matching network and sub-optimal operating conditions.

For high efficiency operation, switching power amplifiers typically require a larger device or a higher drive voltage to achieve smaller on-resistance. However, this higher drive requirement increases the pre-PA power substantially and degrades the overall transmitter efficiency significantly. Hence, switching power amplifiers are not suitable at low radiated power due to its large pre-PA power. In addition, their matching networks are more complex and require more inductors, resulting in larger silicon area.

Non-switching power amplifiers employ the transistor as a transconductor, instead of a switch. As such, it suffers from device loss as its I_{ds}*V_{ds} product is non-zero and hence its theoretical efficiency is lower than that of switching power amplifiers. However, it requires less drive requirement, resulting in a lower pre-PA power and higher transmitter efficiency at low radiated power.

The schematic of a non-switching power amplifier is shown in Fig 3.12 [Chee04]. Transistor M_1 operates as a transconductor and converts its input voltage signal V_{in} into its output drain current I_{ds}. The RF tank, formed by inductor L_1 and all the capacitances

at node X, filters out the harmonics in the drain current and only allows the fundamental drain current to flow to the load, thus resulting in a sinusoidal drain voltage V_{ds}.

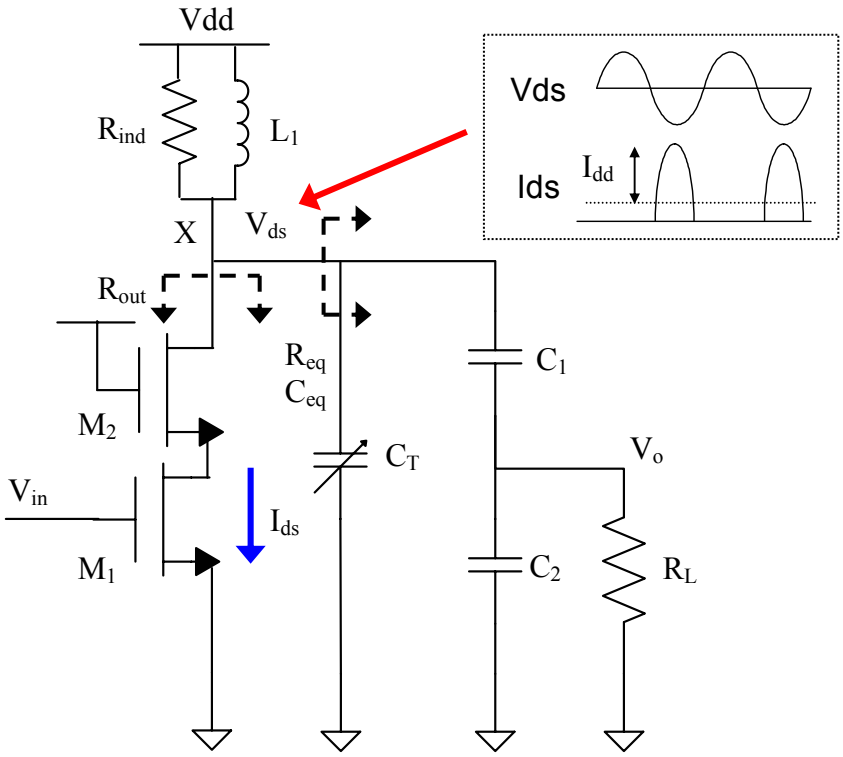


Fig 3.12: Schematic of a non-switching power amplifier.

The fundamental component of the drain current I_1, DC current I_{dc} and output power P_{out} are given as :

$$I_{dc} = \frac{I_{dd}}{\pi}(\sin y - y\cos y), \tag{3.3}$$

$$I_1 = \frac{I_{dd}}{2\pi}(2y - \sin 2y), \tag{3.4}$$

$$P_{out} = \frac{1}{2} I_1^2 \left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}} \right)^2 R_{eq} \tag{3.5}$$

where 2y is the conduction angle, R_{out} is the output resistance of the cascoded transistors, R_{ind} is the loss in inductor L_1, R_{eq} is the transformed load resistance, V_{ds} is the sinusoidal

drain voltage at node X and I_{dd} is the amplitude of the drain current when the conduction angle is π. The drain efficiency η_d of the amplifier is given as:

$$\eta_d = \frac{P_{out}}{P_{dc}} \tag{3.6}$$

$$= \frac{1}{2}\left(\frac{I_1}{I_{dc}}\right)\left(\frac{V_{ds}}{V_{dd}}\right)\left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}}\right)^2 \bullet \left(\frac{R_{eq}}{R_{ind} // R_{out} // R_{eq}}\right) \tag{3.7}$$

$$= \frac{1}{2}\left(\frac{I_1}{I_{dc}}\right)\left(\frac{V_{ds}}{V_{dd}}\right)\left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}}\right). \tag{3.8}$$

Maximizing the drain efficiency at a given output power requires the output voltage swing V_{ds} and $R_{ind}//R_{out}$ to be maximized. For a 1V supply with a saturation voltage of ~100mV, the maximum achievable swing is 0.9V. This translates to a transformed resistance of ~810 Ω to deliver 0.5mW if the loading due to R_{out} and R_{ind} are negligible. The required impedance matching is achieved by the capacitive transformer C_1 and C_2. Capacitive transformers are preferred over LC matching networks or inductive transformers because on-chip capacitors have much higher Q-factor (Q > 30) than on-chip inductors (Q ~ 5 to 8), resulting in much lower loss. The impedance looking into the transformer Z_{eq} is given as:

$$Z_{eq} = \frac{1}{j\omega C_1} + \left(R_L // \frac{1}{j\omega C_2}\right). \tag{3.9}$$

Capacitors C_1 and C_2 are chosen to provide the required impedance. The equivalent capacitance C_{eq} and the parasitic capacitance at node X resonate with inductor L_1 to form a RF tank. By making C_1 and C_2 tunable to provide different transformed resistances but

approximately the same equivalent capacitance, certain discrete levels of power control are possible.

In this design, the total capacitance at node X is ~ 2.5pF and it comprises of C_{eq}, bond pad capacitance, tuning capacitance C_T, interconnect capacitance and drain capacitance of transistor M_2. The inductance L_1 needed to resonate with this capacitance at 1.9GHz is ~ 2.8nH. If L_1 is implemented using on-chip inductor with Q of ~ 5, R_{ind} is about 170Ω. The low R_{ind} diverts the signal current away from the load, and consequently degrades the efficiency by 83%. To overcome this problem, inductor L_1 is implemented using a bond wire inductor, which has much higher Q (~ 25). To compensate for variations in the bond wire inductance, a 5-bit switched capacitor array is used to provide for ~ 24% tuning range. Alternatively, an external inductor can be used [Otis04].

The peak voltage at node X is ~ 2*Vdd. This exceeds the maximum voltage rating in a 0.13μm CMOS process (~1.3V). To alleviate this problem, a cascode transistor M_2 is added and biased such that its gate-drain voltage does not exceed the maximum voltage rating. Cascoding also increases the input-output isolation and improves the efficiency by boosting $R_{out.}$

Since the drain voltage at node X is always sinusoidal, improving the device efficiency requires decreasing the conduction angle to reduce its I_{ds}*V_{ds} product. However, decreasing the conduction angle also reduces the fundamental current and output power. Thus, a larger transistor or higher drive voltage is needed to deliver the same output power and this result in an increased drive requirements and pre-PA power. Fig. 3.13 shows the size of transistor M_1 (normalized to its size when the conduction angle equals

360°) and its maximum device efficiency as a function of the conduction angle for the same output power and input drive voltage. Reducing the conduction angle beyond 180° improves the device efficiency at a diminishing rate but the transistor size increases drastically. For example, when the conduction angle is reduced from 360° to 180°, the device efficiency improves by 28.5% (from 50% to 78.5%) and requires doubling the input device size to deliver the same output power. However, doubling the device size further reduces the conduction angle to ~130° and improves the efficiency by only another 10%.

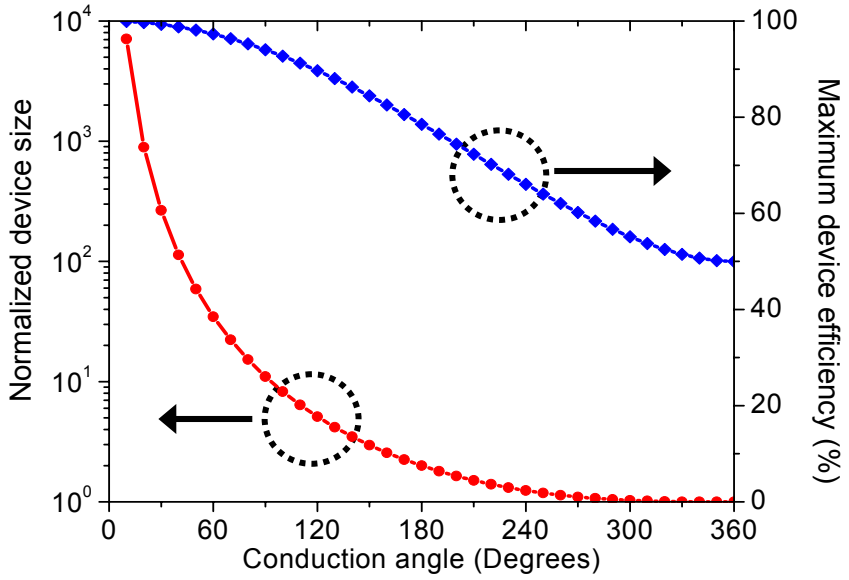


Fig 3.13: Normalized device size and maximum efficiency versus conduction angle.

3.4 Transmitter Prototype

3.4.1 Implementation

The schematic of the direct modulation transmitter is shown in Fig. 3.14. It consists of a FBAR oscillator co-designed with a non-switching low power amplifier. The FBAR

oscillator is similar to that discussed in section 3.2 except for a slightly larger loading and foot switch to turn it on and off. The FBAR oscillator provides a stable RF carrier and the low power amplifier provides efficient power amplification and antenna matching. Baseband data is modulated onto the carrier using on-off keying by power cycling the oscillator and the power amplifier via its foot switch and bias circuit respectively.

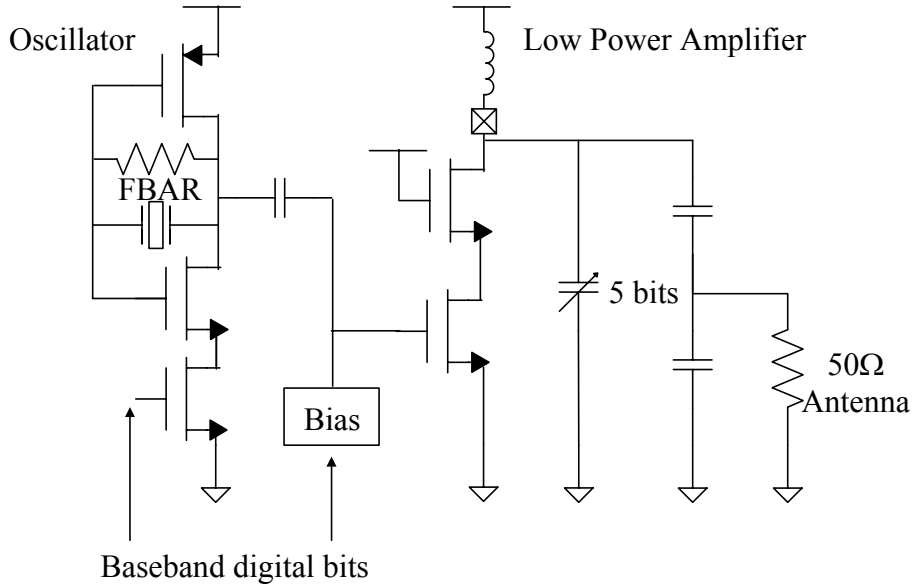


Fig 3.14: Schematic of the direct modulation transmitter.

The transmitter is implemented as part of a super regenerative transceiver [Otis05b] in a standard 0.13μm CMOS process from ST Microelectronics. The die is mounted on a test board using chip on board assembly as shown in Fig. 3.15. The FBAR is wire bonded to the oscillator circuit using two short bond wires to minimize parasitic and any unwanted spurs. The transmitter die area occupies 0.8 x 1 mm^2. A ~ 2.5 mm long bond wire is used as the bond wire inductor for the matching network.

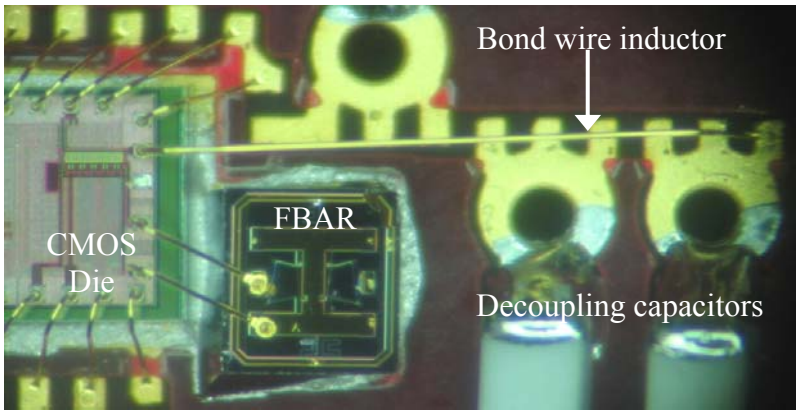


Fig 3.15: Die photo of the direct modulation transmitter.

3.4.2 Measured Results

The transmitter's power consumption and efficiency at various output power are shown in Fig. 3.16. It achieves a peak efficiency of 23% while delivering 0.5mW. The transmitter consumes ~ 2.15mW when turned on and dissipated zero power when switched off. Hence, it consumes ~ 1.1mW for OOK modulation assuming equal probability of transmitting a '0' and '1'. The transmitter efficiency varies by only 3% as the output power changes from 0.3mW to 0.6mW, allowing for efficient power control.

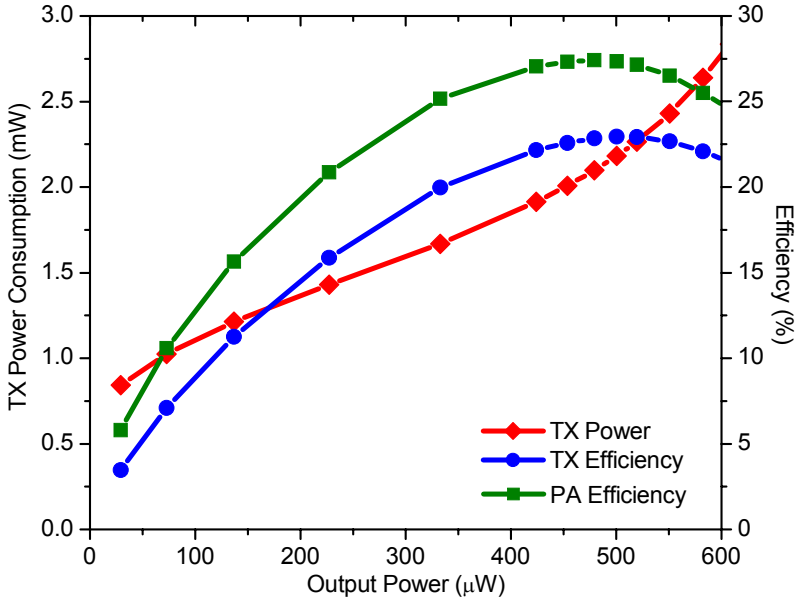


Fig. 3.16: Power consumption and efficiency of the direct modulation transmitter.

For OOK modulation, the data rate is limited by the startup time of the FBAR oscillator. Fig. 3.17 shows the oscillator's startup time as a function of its power consumption. Generally, increasing the oscillator's power decreases the startup time, but increases the power beyond ~ 300μW yields diminishing returns in reduction of the startup time. At nominal operating conditions, the oscillator consumes ~ 350μW and has a startup time of ~ 1.2 μs. If the startup time accounts for 10% of the bit period, the oscillator is capable of supporting data rate up till ~ 83kbps. The oscillator's startup waveform at different power consumption is shown in Fig. 3.18.

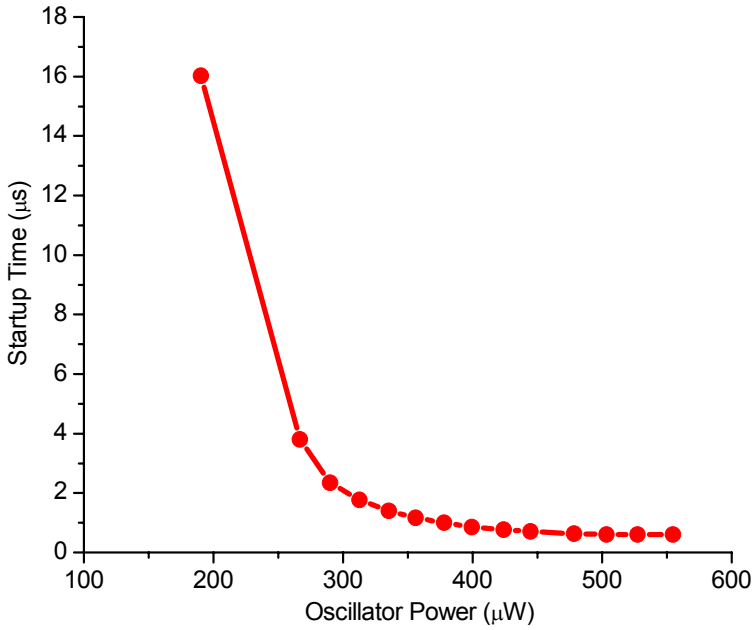


Fig. 3.17: Oscillator startup time as a function of power consumption.

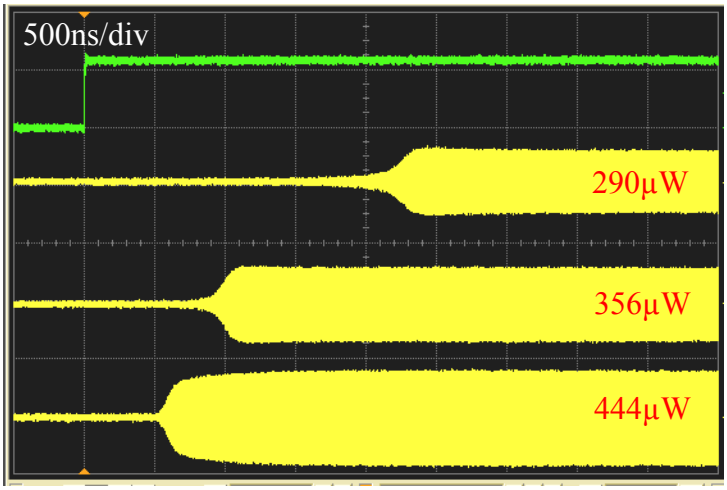


Fig. 3.18: Oscillator's startup waveforms at various power consumptions.

The transmitter output spectrum is shown in Fig. 3.19. A clean output signal is obtained at 1.865 GHz and no close-in spurs are observed. The output waveform when the transmitter is modulated using on-off keying is shown in Fig 3.20.

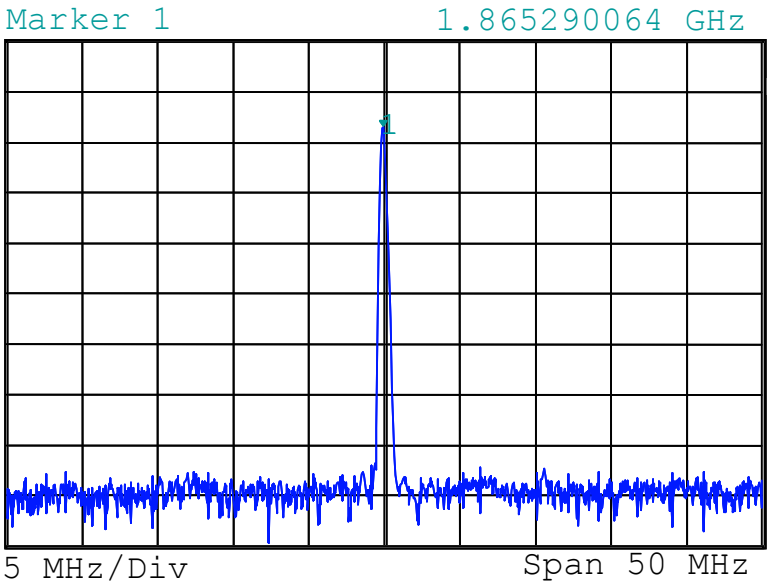


Fig 3.19: Output spectrum of the direct modulation transmitter.

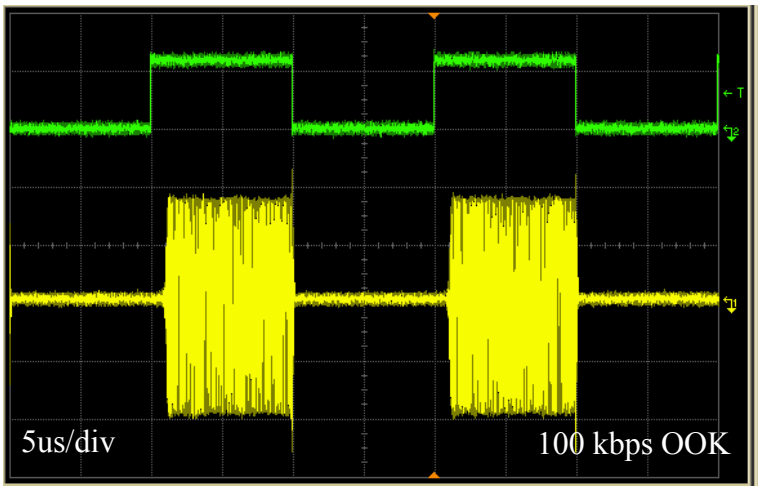


Fig 3.20: Modulated on-off keying transient waveforms.

The pitch of the landing pads on the PCB for the bond wire inductor is designed to be 0.2 mm for different bond wire length implementations. Fig 3.21 shows the output power as a function of the capacitor array bit code. The 5-bits capacitor array is able to resonate with any bond wire inductor having length ranging from ~ 2.4 to 3.6 mm. This is sufficient to mitigate the variability in bond wire length due to manufacturing variations.

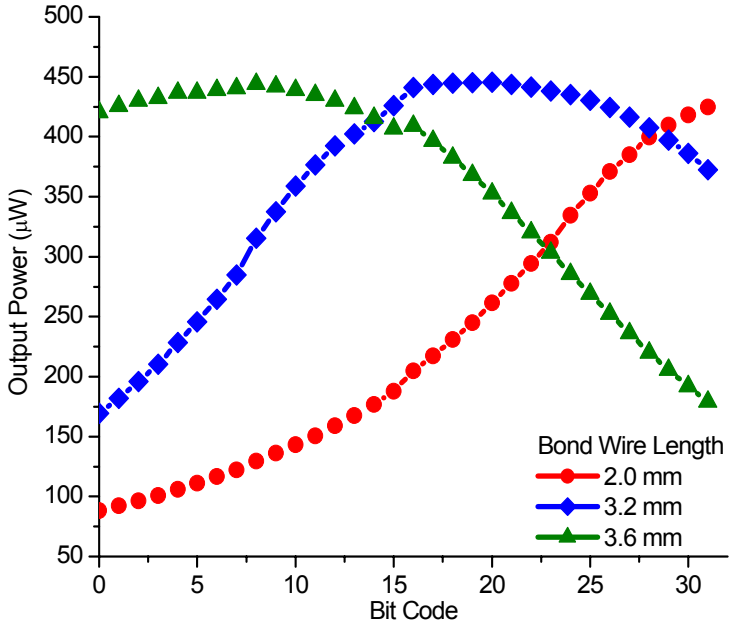


Fig 3.21: Output tank tuning using capacitor array with various bond wire length.

The effect of supply pushing on the oscillator frequency is shown in Fig. 3.22. With a nominal supply voltage of 0.5V, a ±10% change in the supply changes the RF carrier frequency by ±120 kHz. This is well within the 500 kHz receiver bandwidth [Otis05b].

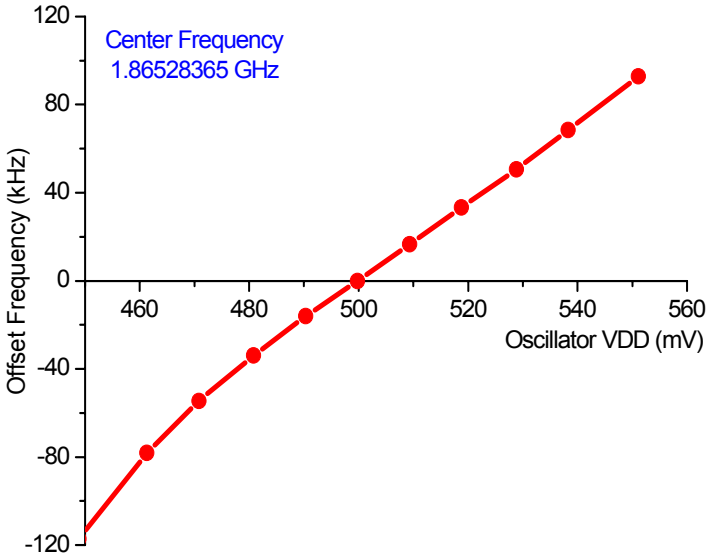


Fig 3.22: Oscillator supply pushing.

The breakdown of the transmitter's power budget compared to the direct conversion transmitter [Choi03] is shown in Fig 3.27.

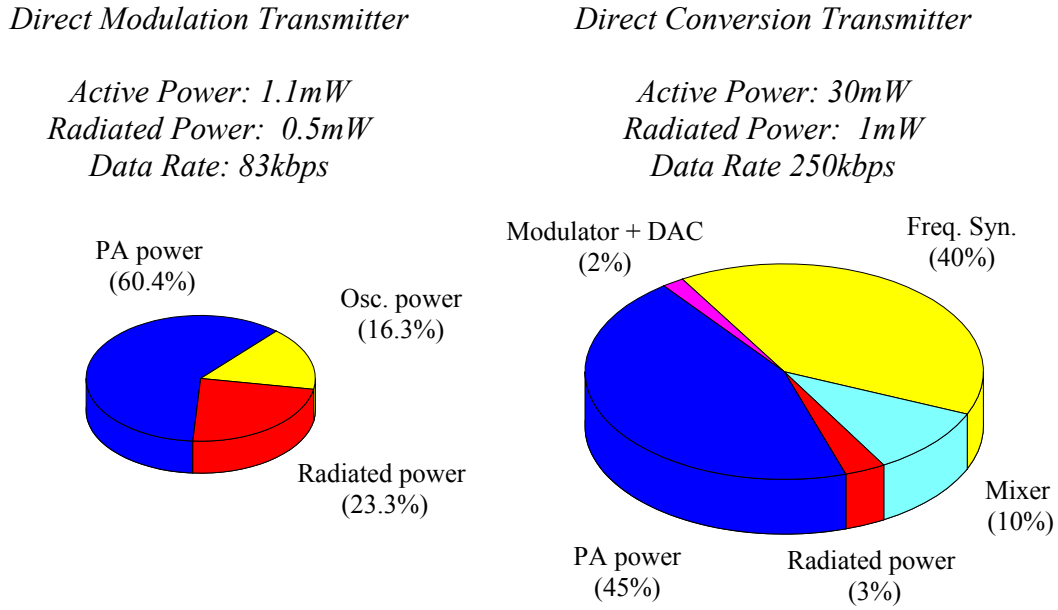


Fig. 3.23: Power budget of (left) direct modulation TX, (right) direct conversion TX.

The efficiency of the direct modulation transmitter is much higher than that of the direct conversion transmitter. This is achieved by (1) reducing the pre-PA power by using a less complex transmitter architecture (i.e. less active circuits), (2) replacing the power hungry frequency synthesizer with a low power FBAR oscillator, and (3) optimizing the entire transmit chain by co-designing the PA and the oscillator.

Fig. 3.23 shows that the efficiency of the direct modulation transmitter is still limited by the power loss in the PA. PA power loss is mainly due to loss in its matching network, which can be eliminated if an active antenna is used instead of the standard 50Ω antenna. An active antenna provides the optimal impedance needed to maximize the PA efficiency. Another limitation of the transmitter efficiency is the pre-PA power (oscillator power). The pre-PA power can be reduced by replacing the low power amplifier with a power oscillator and employing injection locking to obtain a stable carrier. A power oscillator is self-driven and does not load the FBAR oscillator significantly, hence resulting in lower pre-PA power.

Besides improving the efficiency, the data rate should also be increased to reduce the active time. It can be improved by decreasing the oscillator's startup time using two amplifiers during startup or reducing the oscillator's power consumption by minimizing its loading using injection locking so that it can be kept active at all times during data transmission.

These efficiency and data rate enhancement techniques are presented in the injection locked transmitter and the active antenna transmitter in the next two chapters.

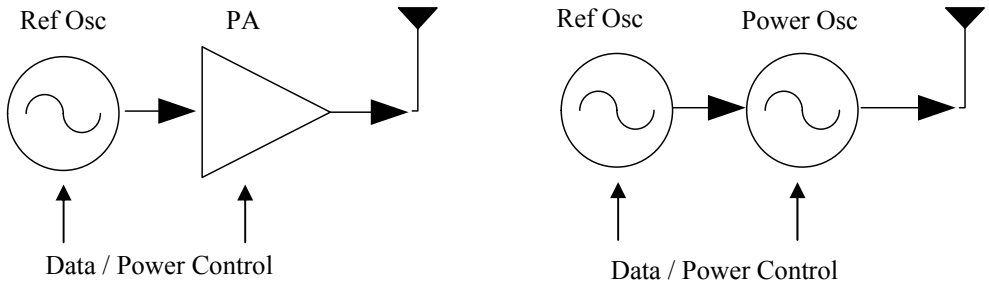
Chapter 4

Injection Locked Transmitter

Obtaining high PA efficiency and low pre-PA power concurrently at low radiated power levels is particularly challenging since an efficient PA often requires a higher drive voltage or loads its driving stage considerably. The higher drive requirement increases the pre-PA power and degrades the overall transmitter efficiency. This inherent tradeoff between the pre-PA power and PA efficiency limits the overall transmitter efficiency in the direct modulation transmitter. To obtain a better compromise between the pre-PA power and PA efficiency at low radiated power, a power oscillator can be used instead of a power amplifier. A power oscillator is self-driven and requires only minimal drive requirements [Tsai99]. However, due to the antenna loading, its oscillation frequency is not precise and it has to be locked to a reference oscillator to obtain an accurate RF carrier. This results in the injection locked transmitter.

4.1 Architecture

The block diagram of a direct modulation transmitter and the injection locked transmitter [Chee05b, Chee06a] are compared in Fig. 4.1.



(a) Direct modulation transmitter (b) Injection locked transmitter

Fig. 4.1: Block diagram of (a) direct modulation TX and (b) injection locked TX

In the injection locked transmitter, the power amplifier is replaced by an efficient power oscillator. A power oscillator is necessary since the FBAR oscillator cannot deliver 1mW to the antenna without degrading its Q-factor substantially. The power oscillator is driven into the voltage-limited regime to allow the output voltage to swing closer to the supply. This reduces the device loss (I_{ds}*V_{ds}) and improves its efficiency. The power oscillator is self-driven and hence does not load the reference oscillator significantly. Thus the pre-PA power, consisting of the reference oscillator power, is minimized.

The 50Ω antenna loads the power oscillator's output tank and degrades its Q-factor. Thus the power oscillator suffers from a poor phase noise performance and an imprecise oscillation frequency. To obtain a stable RF carrier, the power oscillator is locked to an ultra-low power reference oscillator, whose oscillation frequency is stabilized by a high Q FBAR resonator.

Baseband data can be modulated onto the carrier using on-off keying by power cycling the entire transmitter. In this case, the data rate is determined by both the startup time of

the FBAR oscillator and the lock-in time of the power oscillator. Alternatively, the ultra low FBAR oscillator can remain active throughout data transmission and only the power oscillator is power cycled to achieve OOK modulation. This allows for higher data rates as it is determined only by the lock-in time of the power oscillator. Frequency shift keying can also be employed by using a tunable FBAR oscillator.

4.2 Injection Locking

Injection locking is a non-linear phenomenon whereby a free running oscillator, when perturbed by an external signal, changes its frequency to that of the perturbation signal when their frequencies are close. This phenomenon was discovered as early as the 17th century when the Dutch scientist Christian Huygens noticed that the pendulums of two clocks on the wall moved in unison if the clocks are hung close to each other. However, this process was not well understood until Adler derived analytical expressions describing the behavior of injection locking of LC oscillators under small perturbations [Adler73].

Figure 4.2 shows the schematic of a LC oscillator under a small perturbation signal I_{inj}.

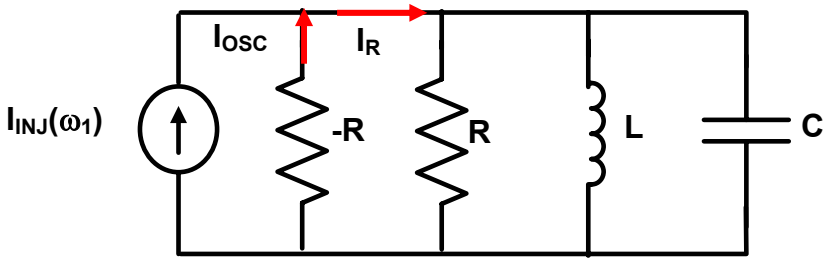


Fig. 4.2: Diagram of LC oscillator with a small perturbation signal

In the absence of an injected signal I_{INJ}, the oscillator oscillates at its free running

frequency $\omega_0=\frac{1}{\sqrt{LC}}$ and I_{OSC} is equal to I_R in both magnitude and phase. When a small signal whose frequency ω_1 is in the vicinity of ω_0 is injected, it introduces a phase shift between I_{OSC} and I_{INJ}. This causes the LC tank to provide the necessary phase shift ϕ_0 and the oscillator oscillates at ω_1 to maintain the phasor relationship

$$\vec{I}_R = \vec{I}_{INJ} + \vec{I}_{OSC} . \tag{4.1}$$

The frequency response of the tank with a small injected signal and the phasor relationship between I_R, I_{INJ}, and I_{OSC} is shown in Fig. 4.3 [Razavi04].

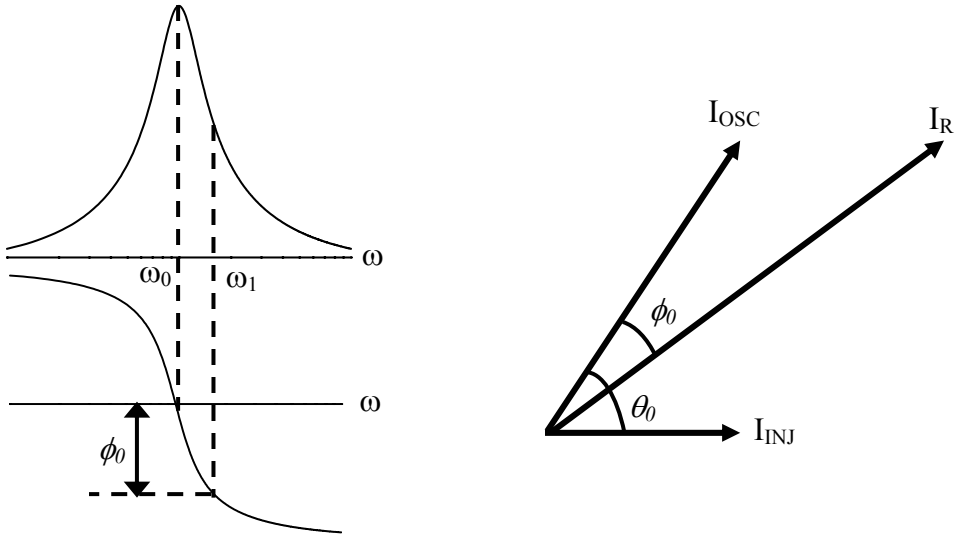


Fig 4.3: (left) Frequency response of tank under injection and (right) phasor diagram.

For small perturbation (i.e. small I_{INJ} and $I_R \approx I_{OSC}$), ω_0 will be pulled towards ω_1. The dynamics of this pull-in process is described by the Adler's equation [Alder73] given as:

$$\frac{d\theta}{dt} = \omega_0 - \omega_1 - \frac{\omega_0 I_{INJ}}{2Q I_{OSC}} \sin\theta , \tag{4.2}$$

where I_{OSC} is the current through the negative resistance, Q is the quality factor, $\frac{d\theta}{dt}$ is

the instantaneous beat frequency and θ is the phase difference between I_{INJ} and I_{OSC}. When the oscillator achieves lock, $\frac{d\theta}{dt} = 0$ and the single sided lock-in range ω_L is:

$$\omega_L = \omega_0 - \omega_1 = \frac{\omega_0 \, I_{INJ}}{2Q \, I_{OSC}}. \tag{4.3}$$

At the edge of the lock-in range (i.e. $\omega=\omega_0\pm\omega_L$), $\theta=90°$ and I_{OSC} is in quadrature with I_{INJ}.

Equation (4.3) shows that the lock-in range is proportional to I_{INJ} and inversely proportional to Q. A higher injected signal I_{INJ} requires a larger phase shift ϕ_0 to satisfy equation (4.1) and a lower Q has a smaller $\frac{d\phi}{d\omega}$ at ω_0. In both cases, they allow for a larger frequency deviation, leading to a higher lock-in range.

The pull-in process is obtained by solving the differential equation (4.2), which gives:

$$\theta(t) = 2\tan^{-1}\left[\frac{1}{\sin\theta_0} - \cot\theta_0 \tanh\left(\frac{\omega_L \cos\theta_0}{2}(t - t_0)\right)\right], \tag{4.4}$$

where $\theta_0 = \sin^{-1}[(\omega_0-\omega_1)/\omega_L)]$ is the steady state phase shift between I_{INJ} and I_{OSC}, and t_0 is the integration constant that depends on the initial phase difference θ_i between I_{INJ} and I_{OSC} at t = 0. When ω approaches ω_1, $\theta(t)$ approaches θ_0. The process becomes exponential with time constant $1/\omega_L$ when $\theta(t)$ is close to θ_0, The lock-in time is obtained by solving equation (4.5) with $\theta(t) = \theta_L \approx \theta_0$ and is given as:

$$t_L = \frac{2}{\omega_L \cos\theta_0} \tanh^{-1}\left[\frac{1 - \sin\theta_0 \tan\left(\frac{\theta_L}{2}\right)}{\cos\theta_0}\right] + t_0. \tag{4.5}$$

Equation (4.5) shows that a shorter lock-in time requires a larger lock-in range ω_L and a smaller frequency deviation (ω_0-ω_1).

4.3 Power Oscillator

The injection locked transmitter consists of an ultra low power FBAR oscillator and a LC power oscillator. The design of the ultra low power FBAR oscillator was discussed in Section 3.2 and hence only the design of the power oscillator is elaborated here.

4.3.1 Efficient Power Oscillator Design

The schematic of the power oscillator is shown in Fig. 4.4.

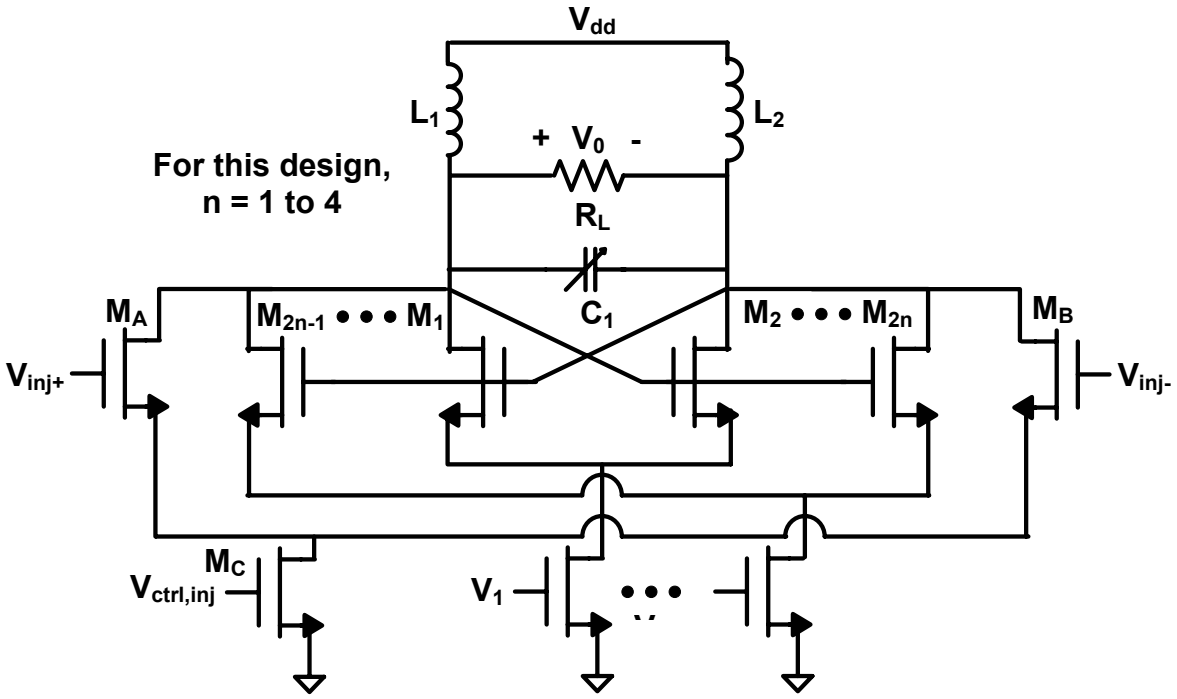


Fig. 4.4: Schematic of the injection locked oscillator.

The oscillator core consists of a pair of cross-coupled transistors M_1–M_2 providing the negative resistance needed to sustain oscillation and a LC resonator to set the oscillation frequency at ~ 1.9GHz. The LC resonator comprises of a ~ 2nH bond wire inductor, a 5-bits switch capacitor array C_1, bond pad and interconnect capacitances, and the transistors' gate and drain capacitances. High Q bond wire inductors are used to minimize loss. The 50Ω antenna is transformed into a 200Ω differential load R_L with a 1:4 balun, allowing the power oscillator to deliver 1mW from a supply of ~ 300mV. R_L loads the oscillator's output tank, hence degrading its Q-factor and frequency stability.

To obtain a stable carrier frequency, the power oscillator is injection locked to a FBAR reference oscillator using transistors M_A and M_B. Due to the high Q FBAR, the FBAR oscillator provides a stable carrier frequency ω_1 with good phase noise performance. Injection locking synchronizes the free running frequency of the power oscillator ω_0 to the stable carrier frequency ω_1. Since the power oscillator is self driven, its drive requirement is greatly reduced and transistors M_A-M_B can thus be chosen to be small in order to minimize the loading on the FBAR oscillator and improve reverse isolation.

Three parallel cross-coupled transistor pairs with binary weighted widths (M_3-M_8) are used for power control [Rofougaran94]. Parallel devices are preferred over a programmable tail current source because they eliminate the voltage headroom needed for the tail current source. This maximizes the available voltage swing and minimizes the device loss (I_{ds}*V_{ds}) in the cross-coupled transistors M_1-M_8. Further reduction in device loss is obtained by operating the oscillator in the voltage-limited regime.

A 5-bits switched capacitor array C_1 is employed to mitigate the variations of the bond wire inductance and ensure that ω_0 lies in the lock-in range. The LSB of the capacitor array C_1 is chosen such that $|f_0 - f_1| \leq 2$ MHz to reduce the lock-in time. The switches are sized such that the Q of the capacitor array is > 60 to minimize losses.

The transistor pairs M_1-M_8 and M_A-M_B are each controlled by a foot switch to allow them to be independently switched on and off. These switches are controlled by the digital bit stream for on-off keying modulation.

4.3.2 Lock-in Range and Lock-in Time

The lock-in range is inversely proportional to the tank Q and I_{OSC} and proportional to I_{INJ} as given in equation (4.3). Since the tank Q and I_{OSC} is determined by the output power, antenna load and tank inductance, I_{INJ} has to increase in order to increase ω_L. In this design, $f_0 \approx 1.9$ GHz, Q ≈ 4 and I_{INJ}/I_{OSC} is chosen to be 5% to minimize the drive requirement, which results in a lock-in range of ±12MHz. This is sufficient since the capacitive array C_1 has a resolution of 4 MHz, ensuring $|f_0 - f_1| \leq 2$ MHz.

The data rate depends on the lock-in time, which is given by equation (4.5). For a shorter lock-in time, it is desirable to have a larger lock-in range and a smaller $(f_0 - f_1)$. For $|f_0 - f_1| \leq 2$ MHz and $f_L = 12$ MHz, θ_0 is ≤ 10° and the lock-in time is estimated to be ~ 300 ns. A shorter lock-in time can be achieved by increasing I_{INJ} or using a finer resolution capacitor array to reduce $|f_0 - f_1|$.

4.3.3 Layout

The layout of the power oscillator is shown in Fig. 4.5. An L-shaped output differential trace is used to provide two orthogonal outputs to the antenna and bond wire inductor. Orthogonal outputs minimize mutual coupling between the bond wires and allow for easy placement of the balun and bond wire inductor. The cross-coupled devices are sandwiched between the output differential traces to minimize interconnect capacitance. This allows for a larger inductor to improve the efficiency or a larger capacitor array to increase the tuning range. The capacitor array and injection locking devices are placed next to the cross-coupled transistors to minimize their interconnect capacitances.

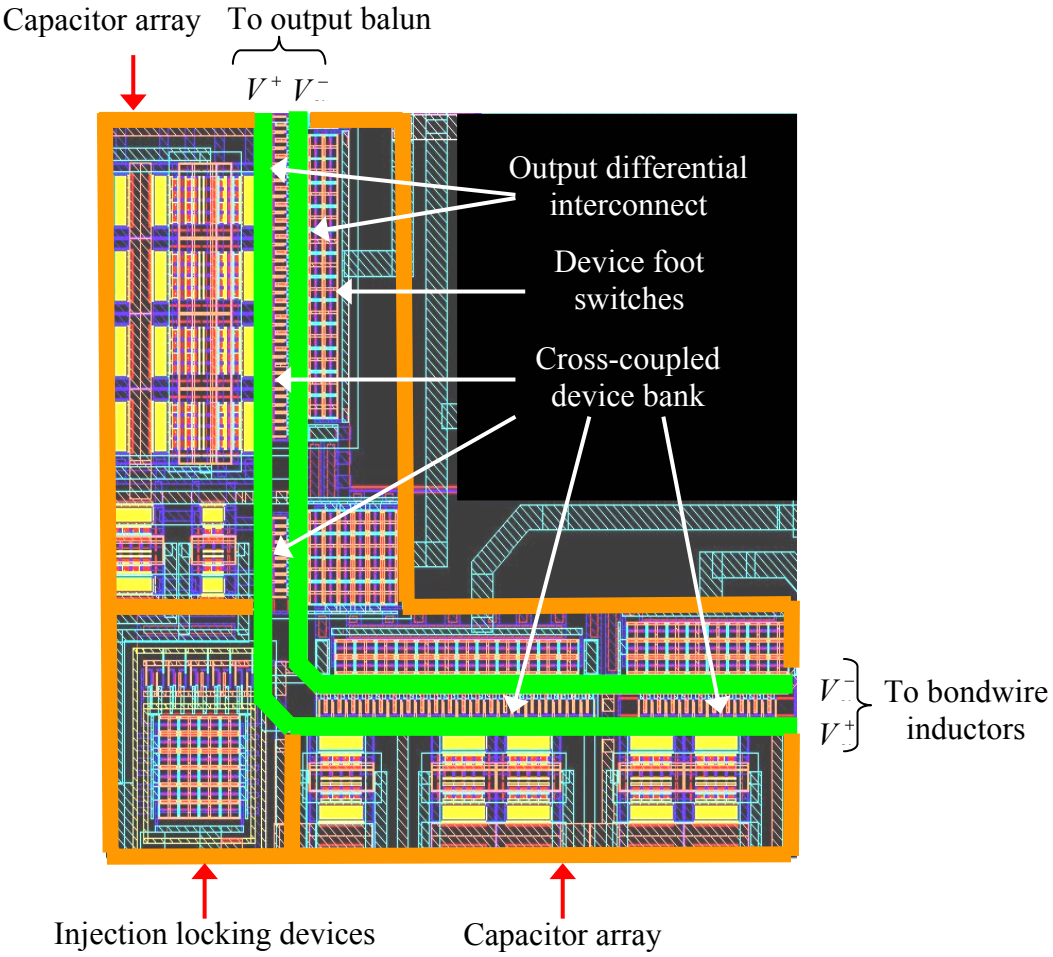


Fig. 4.5: Layout of the power oscillator.

4.4 Transmitter Prototype

4.4.1 Implementation

The power oscillator is implemented in a standard 0.13µm CMOS process from ST Microelectronics and packaged using chip-on-board assembly as shown in Fig. 4.6. Due to the large number of test pads needed, the die area occupies about 1 x 1.2 mm^2. When integrated into a transceiver, only the power oscillator core is needed. The oscillator core occupies only 550 x 650μm^2. Two parallel bond wires, each approximately 2.5mm long, are used to implement the tank inductance. The injected signal is fed from the FBAR oscillator through a balun and oscillator's output is connected to the 50 Ω antenna through a 1:4 balun to provide a 200 Ω load to the power oscillator.

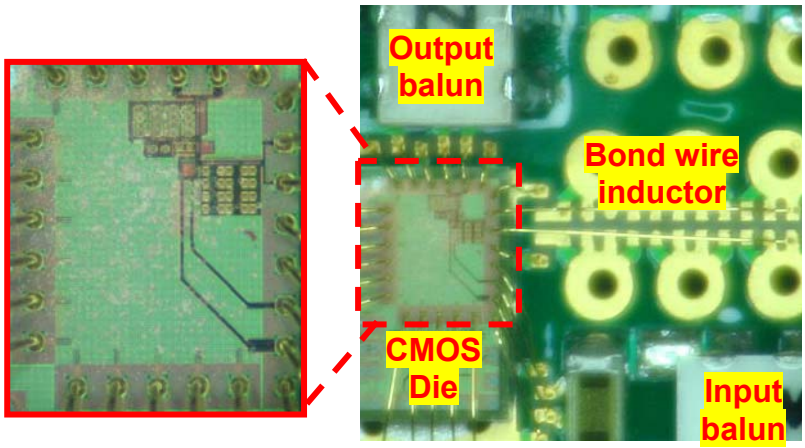


Fig. 4.6: (left) Die photo of power oscillator and (right) close-up of the PCB.

4.4.2 Measured Results

The transmitter efficiency as a function of the radiated power at various supply voltages when power oscillator is locked to the FBAR oscillator at f_1 = 1.882 GHz is shown in Fig.

4.7. Power control of the transmitter is realized using 3 binary weighted cross-coupled transistors (M_3-M_8). For a target output power, there is an optimal supply voltage that maximizes the voltage swing and minimizes the device loss. The dotted line shows the maximum achievable efficiency without constraining the supply voltage.

At the nominal supply of 280 mV, the transmitter achieves an efficiency of 32% while delivering 1 mW. The efficiency of the power oscillator is 33% and the FBAR oscillator degrades the efficiency by only 1%. This clearly demonstrates the effectiveness of using injection locking to reduce the power oscillator's drive requirement and pre-PA power. The power oscillator can operate with supply voltages as low as 210 mV. At 210 mV supply, it delivers 300 μW with 25% efficiency.

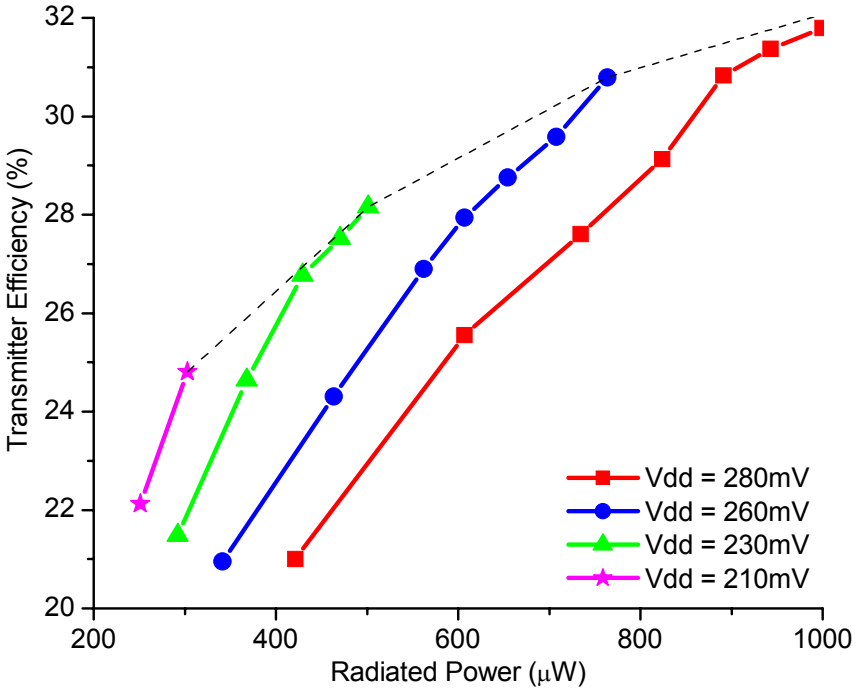


Fig. 4.7: Measured transmitter efficiency of the injection locked transmitter.

The transmitter phase noise performance is shown in Fig. 4.8. Prior to locking, the transmitter's phase noise is dominated by the power oscillator's phase noise. Due to the

antenna loading, the Q factor of the power oscillator is low and it achieves a phase noise of -98 dBc/Hz at 100kHz offset and -113 dBc/Hz at 1MHz offset. When the power oscillator is locked to the FBAR oscillator, its phase noise performance follows that of the FBAR oscillator. Due to the high Q FBAR, the FBAR oscillator has excellent phase noise performance and it improves overall transmitter's phase noise performance by ~ 20dB to -120 dBc/Hz at 100kHz offset and -132 dBc/Hz at 1MHz. The phase noise is eventually limited by the instrument noise floor.

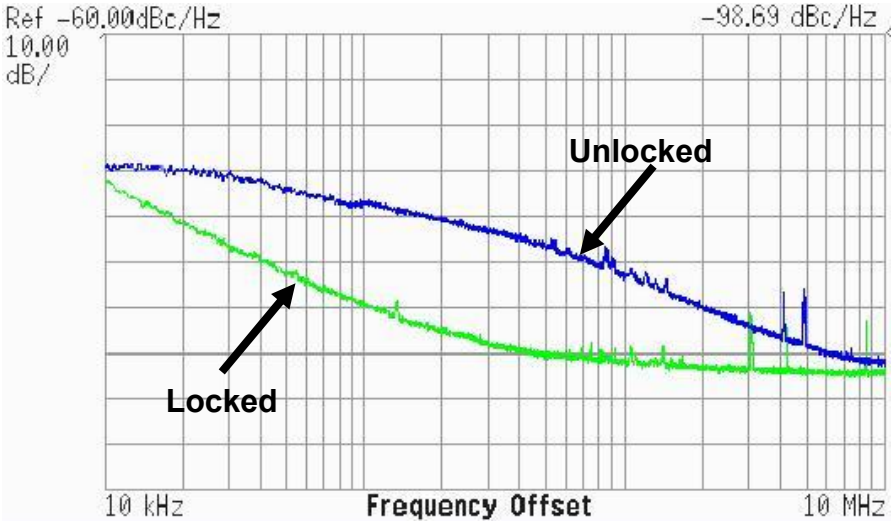


Fig 4.8: Power oscillator phase noise performance.

The improvement in phase noise before and after locking is evident in the output spectrum of the transmitter shown in Fig. 4.9. Due to the low output tank Q, the output spectrum is broad and noisy prior to locking. However, once the power oscillator acquires lock, a clean and stable carrier frequency is obtained due to the high Q FBAR.

Fig. 4.9: Output spectrum when power oscillator is (left) free running (right) locked.

Fig. 4.10 shows the single sided lock-in range f_L as a function of the bias current of the injection locking transistor M_A. A higher bias current increases the transconductance of transistor M_A and M_B, which increases the injected signal and lock-in range. However, this also increases the power consumption of transistor M_A and M_B which degrades the overall efficiency. To minimize efficiency degradation, the lock-in range f_L can be chosen to be ~7 MHz and the peak efficiency is reduced by only by ~1%.

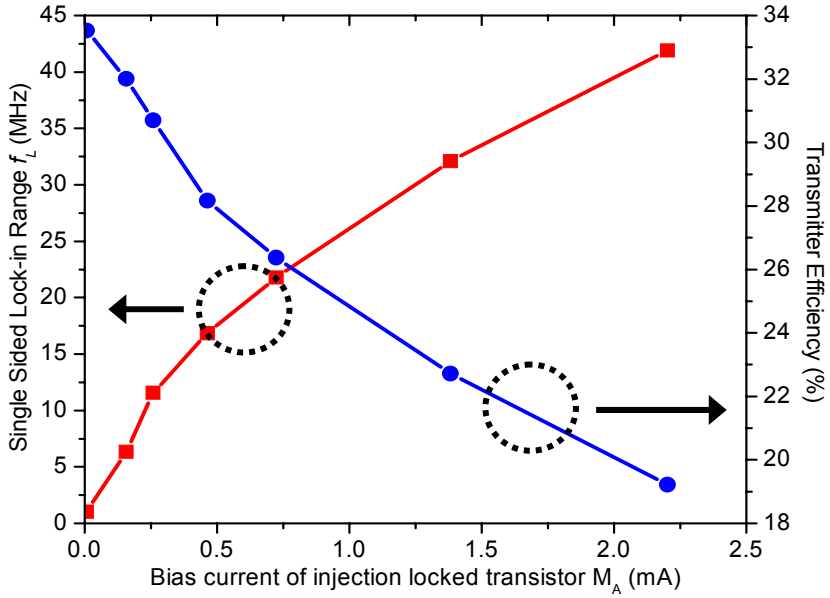


Fig. 4.10: Measured lock-in range of the injection locked transmitter.

Fig 4.11 shows the measured lock-in time for $f_0 - f_I \approx 2$ MHz as a function of the bias current of the injection locking transistor M_A. A higher bias current increases the injected signal and reduces the lock-in time. For $f_L \approx 7$ MHz, the lock-in time is ~ 1.9 µs. With the startup time of the power oscillator less than 100 ns, the total overhead time is ~ 2 µs. If the overhead time accounts for 10% of the symbol period, the transmitter can support OOK modulation at a data rate of 50 kbps with 32% efficiency while delivering 0 dBm of output power. Assuming equal probability of transmitting a '1' and '0', the transmitter's power consumption is 1.6mW. The modulated OOK waveform is shown in Fig. 4.12.

Higher data rate can be obtained by increasing the injected signal. When the bias current increases to 516µA, the lock-in time decreases to ~ 540ns. Thus, the overhead time is reduced to 640 ns and the transmitter can support data rates up to ~ 156 kbps. With a higher bias current, the transmitter efficiency is reduced to 28% and the transmitter active power consumption is increased to 1.9mW for 50% OOK data.

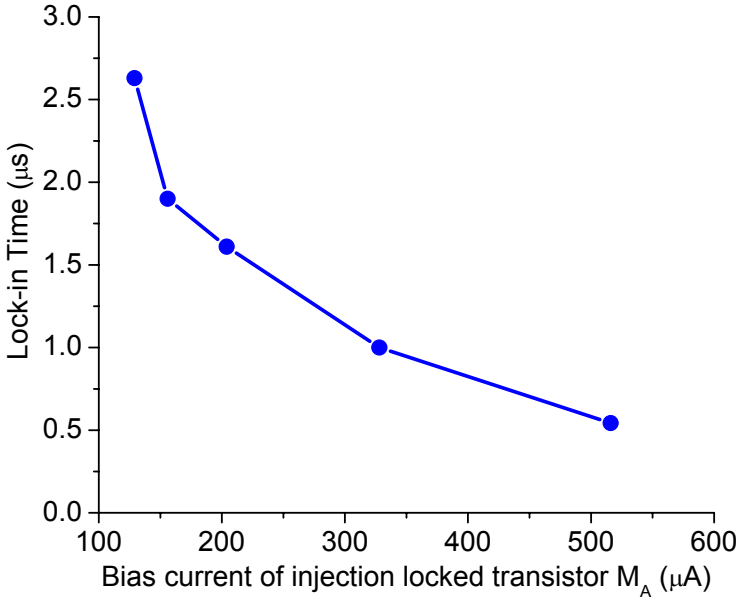


Fig 4.11: Measured lock-in time of the injection locked transmitter.

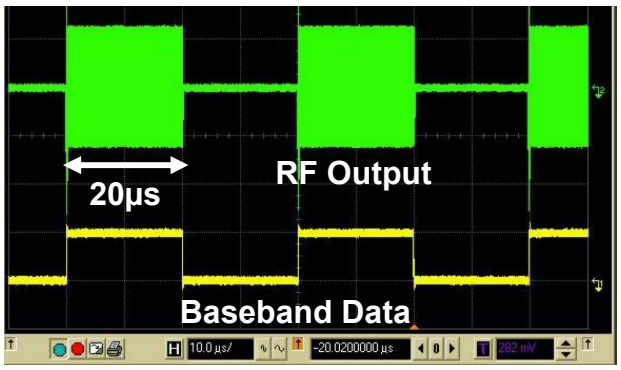


Fig 4.12: Waveform of on-off keying data of the injection locked transmitter

To reduce the lock-in power, a 5-bit capacitor array is used to tune f_0 close to f_1. Fig. 4.13 shows the frequency as a function of the capacitor code. The array has 103MHz of tuning range with ≤ 4 MHz resolution, allowing f_0 to be tuned within 2MHz of f_1.

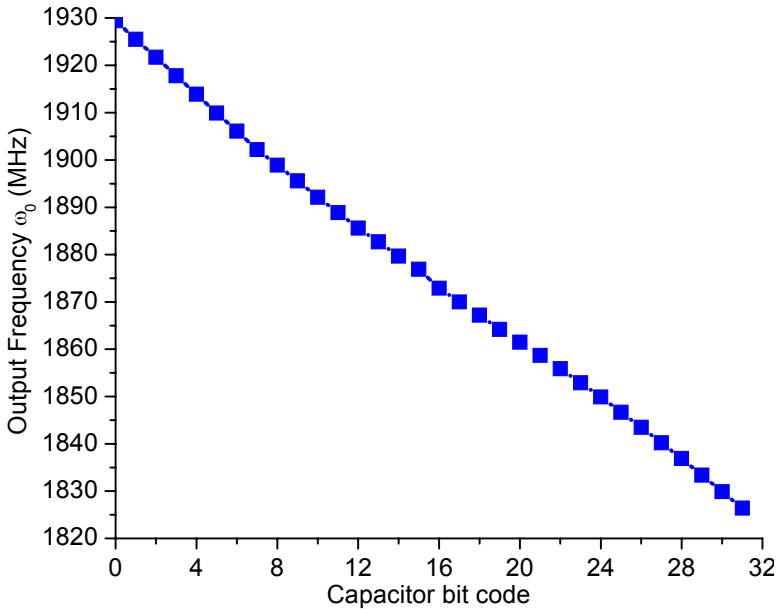


Fig. 4.13: Measured tuning range of capacitor array C_1.

Fig 4.14 shows the breakdown of the transmitter's power budget compared to the direct modulation transmitter presented in Chapter 3 with 50% on-off keying modulation.

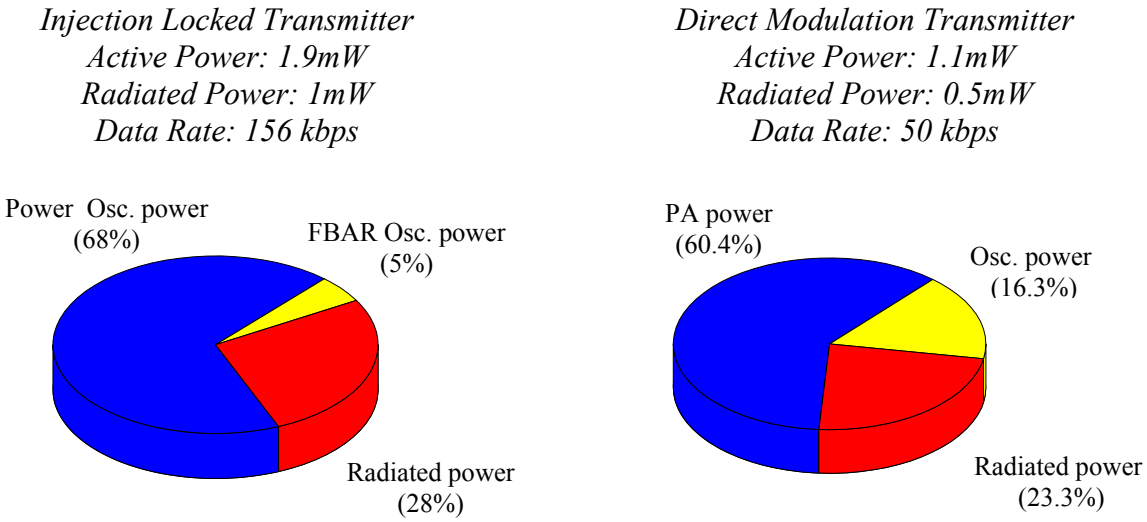


Fig. 4.14: Power budget of (left) injection locked TX, (right) direct modulation TX.

In the injection locked transmitter, the pre-PA power accounts for only 5% of the total power and the transmitter efficiency is improved to 28%. With such low active power, the FBAR oscillator can remain active throughout data transmission. This allows for a higher data rate since it is not limited by the long startup time of the FBAR oscillator. With higher data rate, the active time is reduced, leading to lower average transmitter power consumption.

The efficiency of the injection locked transmitter is still limited by the power loss in the power oscillator. This can be reduced by using an active antenna as illustrated in the active antenna transmitter presented in the next chapter.

Chapter 5

Active Antenna Transmitter

By using fewer pre-PA circuits and less complex modulation schemes, the direct modulation transmitter has a much lower pre-PA power than the direct conversion transmitter. Further reduction in pre-PA power is accomplished by using the injection locked transmitter presented in the last chapter. With the pre-PA power reduced to less than the radiated power, increasing the PA efficiency becomes effective in improving the overall transmitter efficiency.

The PA efficiency is limited by losses in the device and matching network. Device loss is minimized by reducing the product of the voltage across the device and the current through it (i.e. $I_{ds}*V_{ds}$). Typically, higher device efficiency requires larger drive requirement, which increases the pre-PA power. Thus, the optimal transmitter efficiency is obtained by co-designing the pre-PA circuits and the low power amplifier concurrently as discussed in Chapter 3.

Matching network loss is typically limited by the Q factor of the inductors. Fig. 5.1 shows the efficiency of the matching network as a function of the inductor Q for the

direct modulation transmitter presented in Chapter 3, assuming that losses in the on-chip capacitors are negligible. On chip inductors have Q-factors of ~5 to 10, resulting in a matching network efficiency of only 20% to 30%. Even with higher Q bond wire inductors (Q ~ 25 – 30), the matching network still accounts for about 45% to 50% of the power loss. To reduce loss, the matching network can be incorporated into the antenna, giving rise to the active antenna transmitter. By using an electrically large antenna, the antenna loss can be reduced to negligible levels. This results in higher transmitter efficiency.

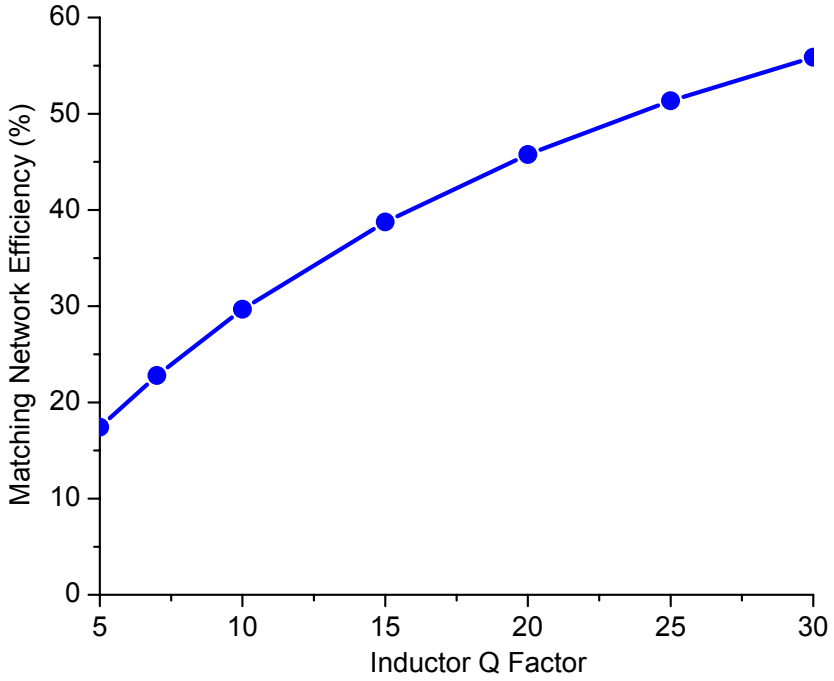


Fig. 5.1: Matching network efficiency for direct modulation transmitter.

5.1 Architecture

The block diagram of the active antenna transmitter [Chee06b] is shown in Fig. 5.2. The transmitter utilizes two distinct high Q FBAR oscillators to create two different RF

channels at ~1.9 GHz. The two channels are multiplexed together in the low power amplifier. This technique is scalable to realize multiple channels. The use of multiple FBAR oscillators are preferred over frequency tuning of the FBAR oscillator as it is difficult to obtain a wide tuning range without loading the high Q resonator significantly.

The low power amplifier is co-designed with the antenna whose impedance is designed to provide the optimal impedance needed to maximize the PA device efficiency. This eliminates the matching network and its losses and improves the overall transmitter efficiency. With only two active circuit blocks per channel, it is less complex than the direct conversion transmitter and has a lower pre-PA power.

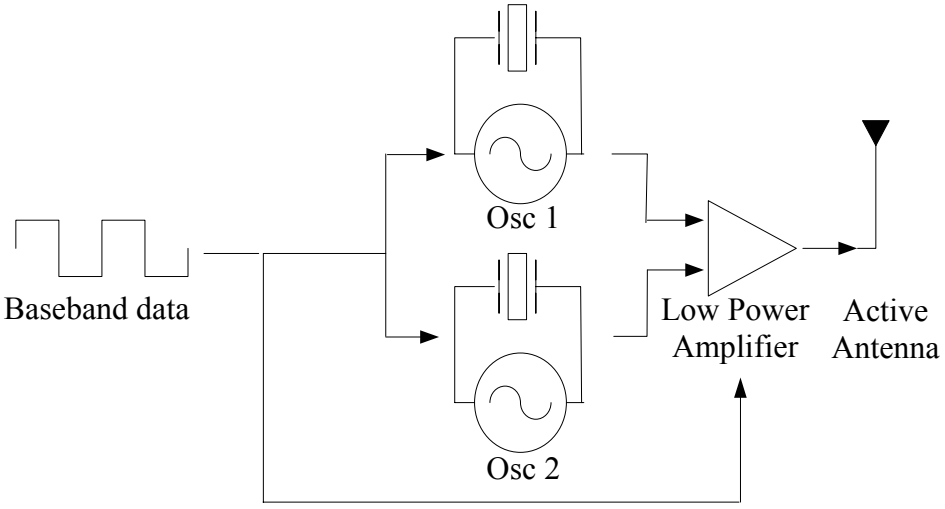


Fig. 5.2: Block diagram of the two channel active antenna transmitter.

The baseband data is directly modulated onto the RF carrier using OOK by power cycling the transmitter. The FBAR oscillator and low power amplifier are switched on and off through switches in their biasing circuits. Frequency shift keying can be employed by toggling between the two oscillators with the baseband data to create a single channel FSK transmitter.

The data rate is determined by the startup time of the FBAR oscillator. To reduce the startup time, the FBAR oscillator employs two amplifiers during start up but uses only one of them to sustain steady state oscillation. Since the startup time accounts for ~10% of the bit period, this allows for a higher data rate without a significantly increase in the pre-PA power. A higher data rate reduces the active time and hence the average power consumption.

5.2 Active Antenna

5.2.1 Design Considerations

Incorporating the matching network into the antenna requires the antenna to provide the optimal impedance to maximize the PA efficiency. The antenna needs to provide a resistance and an inductance at its input terminal as shown in Fig. 5.3. With an electrically large antenna (size >> $\lambda/10$), antenna loss is minimized and the resistive load is mainly due to the transformed radiation resistance at the antenna input terminals. The inductive component is needed to resonate with the capacitances at the output node of the PA. In addition, the antenna needs to provide a DC path for the PA and an omni-directional radiation pattern as the location of the node's neighbors are random.

With the electrical and radiation pattern requirements, several types of antenna (e.g. dipole, loops, dielectric resonator and printed antenna) can be employed. However, to reduce cost, the printed antenna is an attractive option as the printed circuit board is relatively inexpensive compared to other antennas. In addition, it has a low profile and has a small form factor when properly designed.

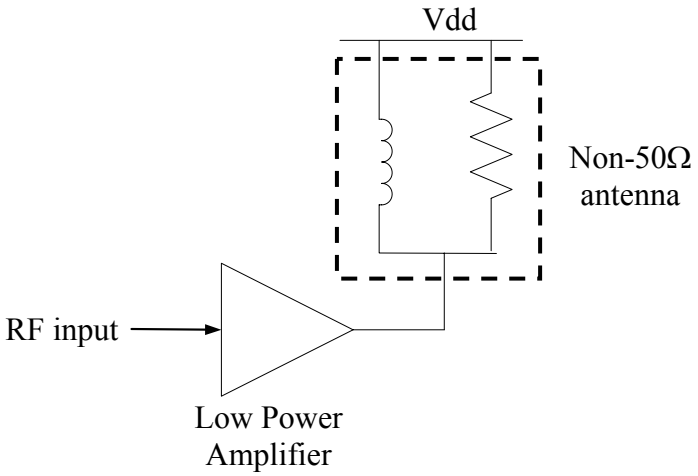


Fig. 5.3: PA-antenna co-design

5.2.2 Printed Inverted L Antenna (PILA)

To meet all the antenna requirements, the printed inverted L antenna (PILA) is proposed. Its principle of operation can be understood using the asymmetric coplanar folded dipole shown in Fig 5.4. The dipole consists of a driven strip of width W_1 and a parallel strip of width W_2. Both strips are shorted together at both ends.

The input impedance of the antenna can be obtained using the transmission line model [Uda54]. In this model, the total current flowing into the dipole I_{in} is decomposed into the transmission line mode current I_t and the antenna mode current I_d. In the transmission line mode, the current in the two strips flows in the opposite direction and no radiation occurs. The antenna acts as a shorted transmission line with length L/2 and I_t is given as:

$$I_t = \frac{V}{2Z_T} \tag{5.1}$$

where $Z_t = jZ_0\tan(k_0L)$ is the input impedance of a shorted transmission line, Z_0 is the transmission line characteristic impedance and k_0 is its wave number.

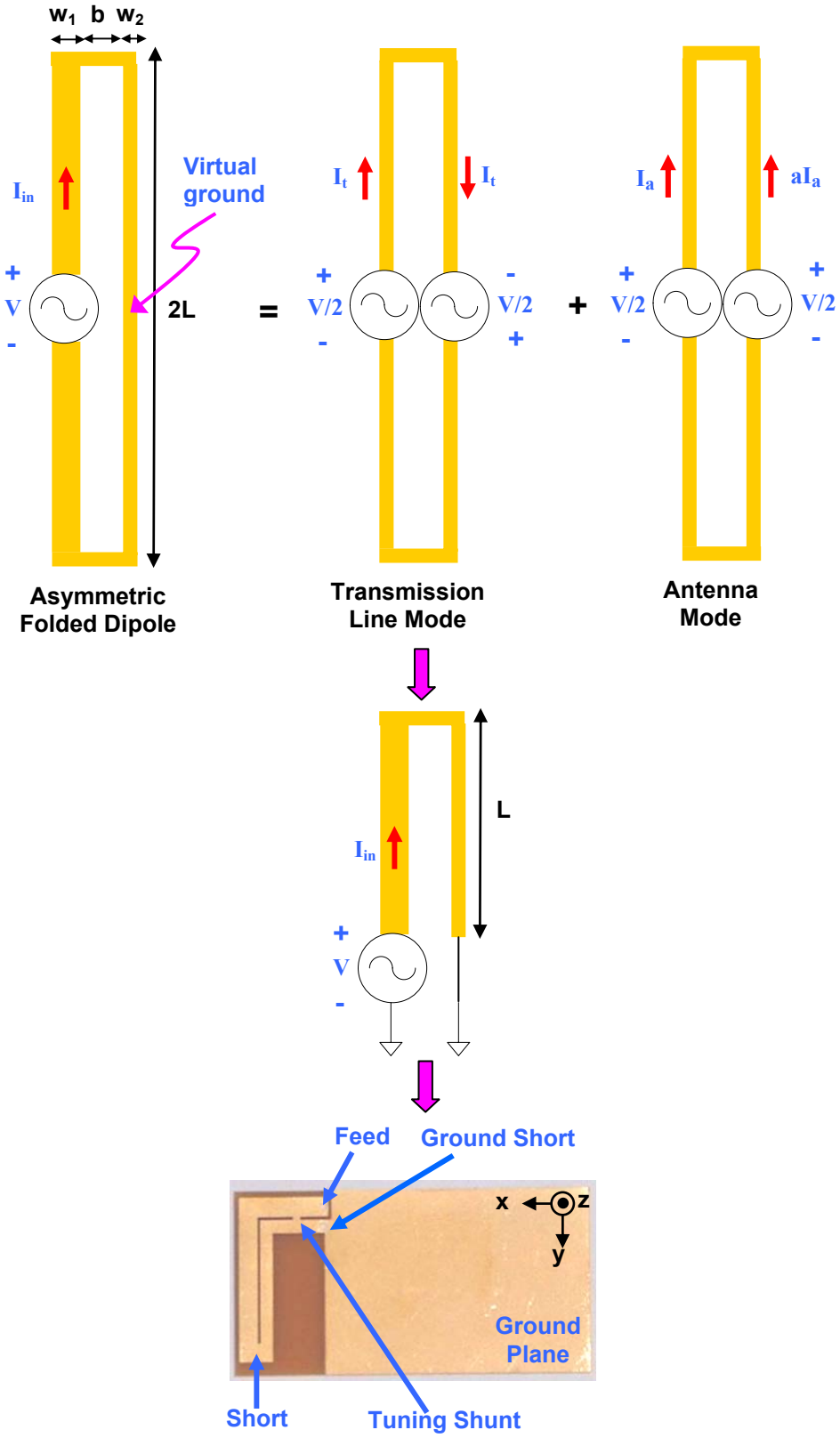


Fig. 5.4: Design of the printed inverted L antenna (PILA).

In the antenna mode, the dipole radiates with an equivalent current of $I_d = (1+a)I_a$, where I_a is the current in the driven strip and *a* is the ratio of the current flowing in the two strips. Hence the asymmetric dipole can be modeled as an equivalent dipole with an equivalent radius and I_a can be expressed as [Lampe85]

$$I_a = \frac{V}{(1+a)^2 Z_d} \tag{5.2}$$

where Z_d is the dipole impedance of a equivalent dipole. Since the total current $I_{in} = I_t + I_a$ and hence the input impedance of the antenna Z_{in} is given as

$$Z_{in} = \frac{2(1+a)^2 Z_d Z_t}{(1+a)^2 Z_d + 2Z_t}. \tag{5.3}$$

Fig. 5.4 shows that the folded dipole is symmetrical about the source and a virtual ground exists at the center of the parallel strip. Thus, the size of the folded dipole can be reduced by half by connecting the virtual ground to an existing ground plane in the printed circuit board. This also provides a DC path for the power amplifier. To further reduce the antenna area, the antenna's arm is bent into the L-shape as shown in Fig. 5.4.

To obtain the optimal impedance for the PA, a tuning shunt is added to the antenna. The input impedance is determined by the antenna length L, the impedance ratio *a*, the PCB dielectric constant ($\varepsilon_r \sim 4.4$ for FR4) and the position of the tuning shunt. For the PILA antenna, when $L \sim \lambda/4$, the impedance loci form a loop around the desired impedance on the Smith chart as shown in Fig. 5.5. This provides a wide impedance bandwidth of ~ 340MHz which helps to mitigate the effects due to manufacturing and environmental variations. The antenna is also electrically large when $L \sim \lambda/4$, resulting in a low antenna loss and an antenna efficiency of 98%.

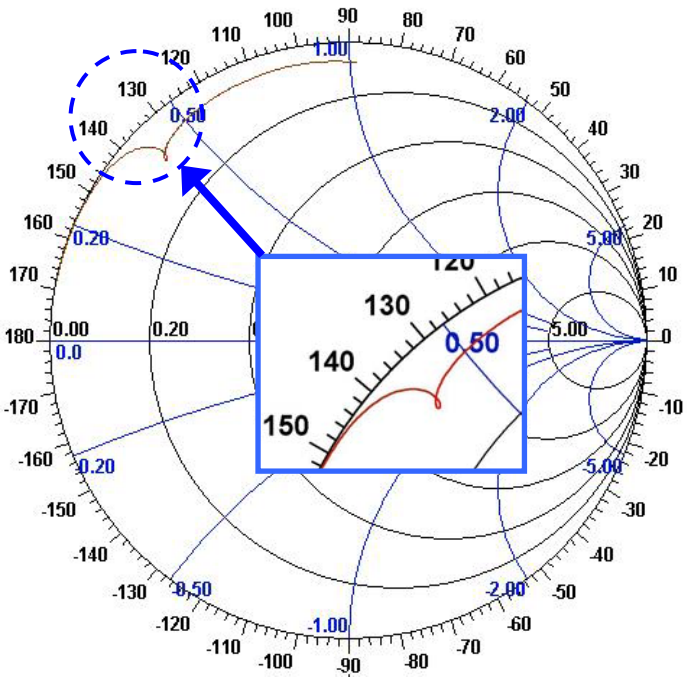


Fig 5.5: Impedance loci of the PILA antenna.

With L ~ λ/4, the real and imaginary components of the antenna impedance are determined to the first order by the impedance ratio *a* and the distance of the tuning shunt from the input terminals respectively. The impedance ratio *a* is adjusted by changing the ratio W_1/W_2. Extensive electromagnetic simulations using Ansoft HFSS are used to fine tune the impedance to the final value.

The PILA antenna has a near omni-directional radiation pattern with a peak directivity of 1.734 as shown in Fig. 5.6. With this radiation pattern, the node is capable of communicating with all neighboring nodes except for nodes that lies along its x-axis, where the antenna suffers a deep null.

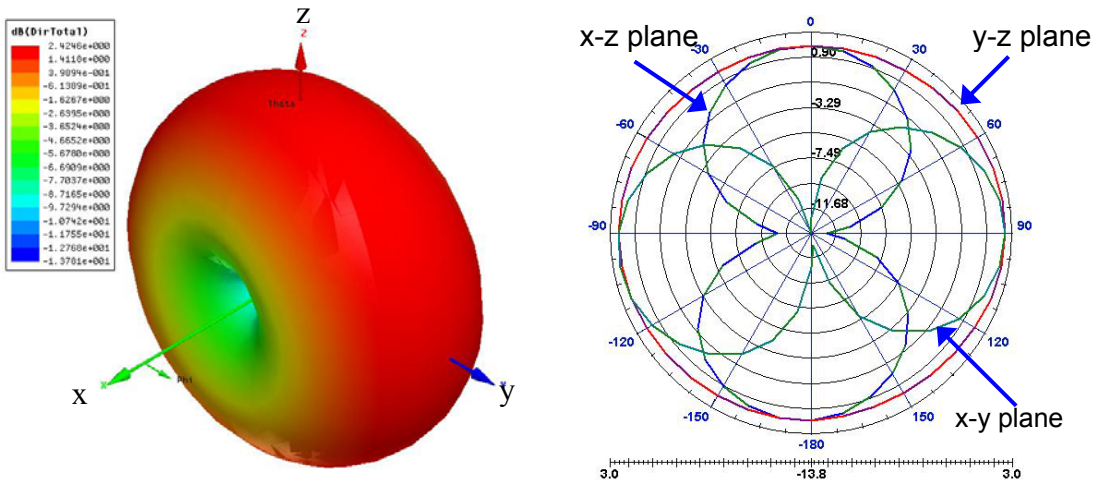


Fig. 5.6: Radiation pattern of the PILA antenna.

5.3 Fast Startup FBAR Oscillator

For a given packet size and packet rate, a higher data rate minimizes the active time and lowers the average transmitter power consumption. With OOK modulation, the data rate is limited by the startup time of the FBAR oscillator. To reduce the startup time, the FBAR oscillator employs an additional amplifier consisting of M_1-M_2 during startup (see Fig. 5.7). This increases the negative resistance and reduces the startup time constant. Once the oscillator reaches steady state, V_{C1} goes low and transistors M5, S1 and S1 are turned off, and only one amplifier stays active to sustain steady state oscillation. Since the startup time accounts for only 10% of the bit period, this improves the data rate significantly with only a slight increase in pre-PA power. A higher data rate reduces the active time and average transmitter power consumption.

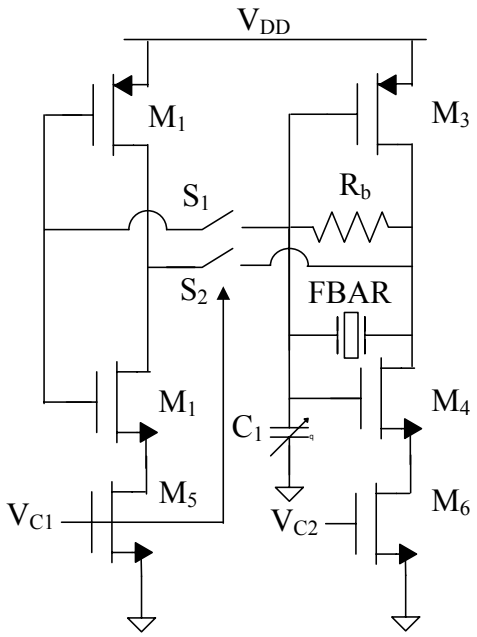


Fig. 5.7: Schematic of the fast startup FBAR oscillator.

The FBAR oscillator employs complementary gain stages to reuse its bias current, reducing the current consumption by half while achieving the same g_m. Subthreshold MOSFET operation is used to obtain a higher current efficiency (g_m/I_d). A large resistor R_b is used to bias the transistors at $V_{dd}/2$ to maximize the voltage swing and minimize its loading on the FBAR. The oscillator employs a 3-bits capacitor array C_1 for frequency tuning to mitigate process variations.

5.4 Low Power Amplifier / Antenna Co-design

The schematic of the low power amplifier is shown in Fig. 5.8. The PA consists of two transistors M_1-M_2 sharing a common drain node and their biasing circuits. The RF signals from the two FBAR oscillators drives transistors M_1 and M_2 directly. For OOK modulation, the data is used to power cycle the PA via the gate bias of M_1 and M_2. With

only one channel being employed at any instant, M_1 and M_2 will not be active concurrently. A 5 bits capacitor array C_1 is used for tuning the output tank frequency to mitigate manufacturing variations.

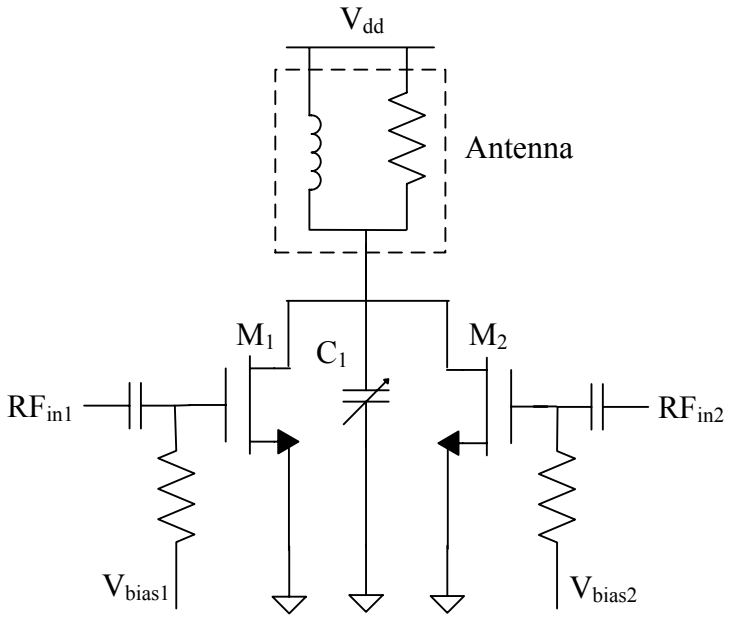
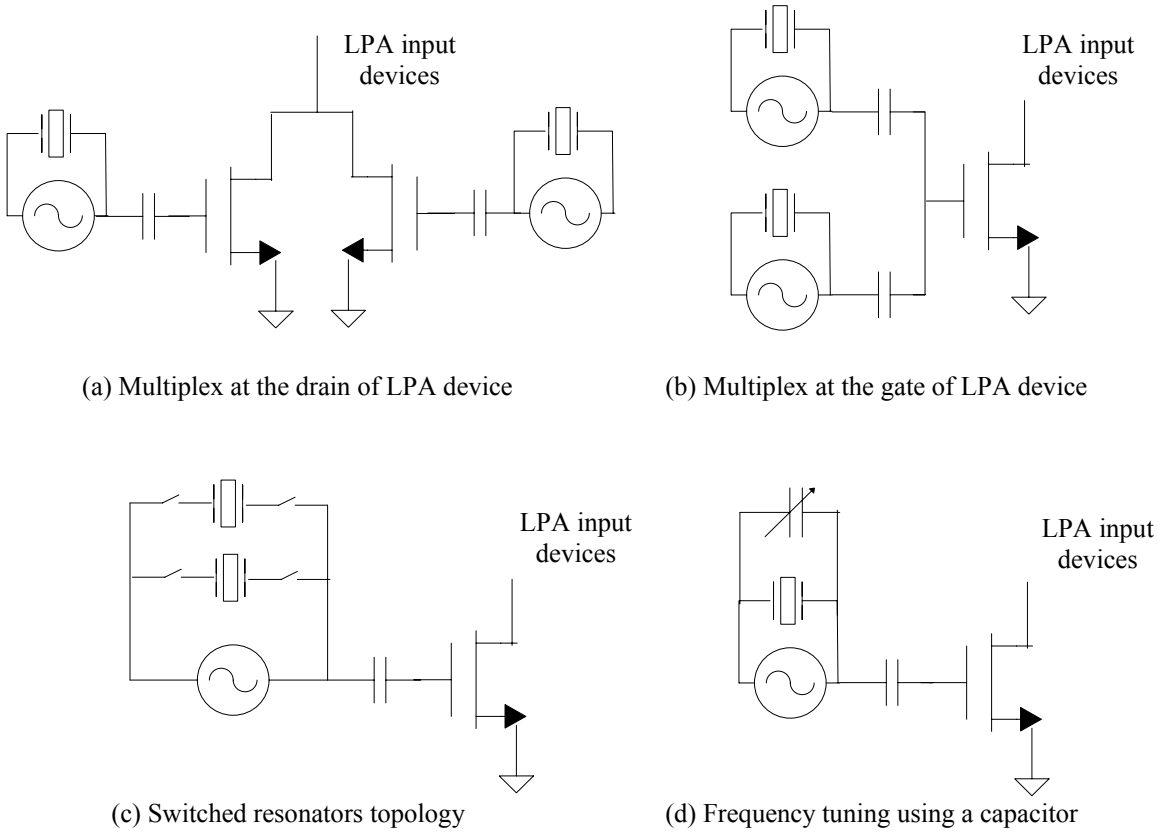


Fig. 5.8: Schematic of the low power amplifier.

The LPA is co-designed with the printed inverted L antenna (PILA) to eliminate the matching network and its loss. The antenna provides an admittance of $(5\text{-}j17)\times10^{-3}\ \Omega^{-1}$ to maximize the PA efficiency. Eliminating the matching network loss also indirectly reduces the power consumption of the FBAR oscillator. This is because smaller transistors can now be used to provide the same output power to the antenna, resulting in less loading on the FBAR oscillator.

The maximum voltage swing at the drain node is 2*Vdd. With a maximum voltage rating of 1.3V for this process, the supply voltage is chosen to be ~0.65V. This eliminates the need for a cascode transistor. To achieve the optimal tradeoff between the PA efficiency and its drive requirements, the PA is co-designed with FBAR oscillator.

Multiplexing the signal at the drain node of the PA transistors to create multiple channels is preferred over other techniques shown in Fig 5.9 because it maximizes the isolation between the FBAR oscillators and preserves the Q factor of the FBAR resonators. Multiplexing the signal at the gate reduces the isolation between FBAR resonators while using a switched resonator topology reduces the Q-factor of the FBAR resonator due to the series resistance of the switch. With the high Q factor of the FBAR resonator, a large tunable capacitor is needed to obtain a wide tuning range and it will load the FBAR resonator significantly and results in higher power consumption.



(a) Multiplex at the drain of LPA device

(b) Multiplex at the gate of LPA device

(c) Switched resonators topology

(d) Frequency tuning using a capacitor

Fig. 5.9: Techniques to create multiple channels with FBAR oscillators.

5.5 Transmitter Prototype

5.5.1 Implementation

The transmitter is implemented in a standard 0.13µm CMOS process from ST Microelectronics. The die area is 0.8 x 1.85 mm^2 and it includes the active antenna transmitter and some test circuits. The transmitter occupies 0.8 x 1.2 mm^2. The CMOS die and two FBAR resonators are assembled on a test board using chip-on-board technology as shown in Fig. 5.10. Two short bond wires are used to connect the FBAR resonator to the CMOS die to minimize any unwanted spurs. The transmitter also includes a serial to parallel interface (SPI) block to reduce the number of bond pads needed for the control signals.

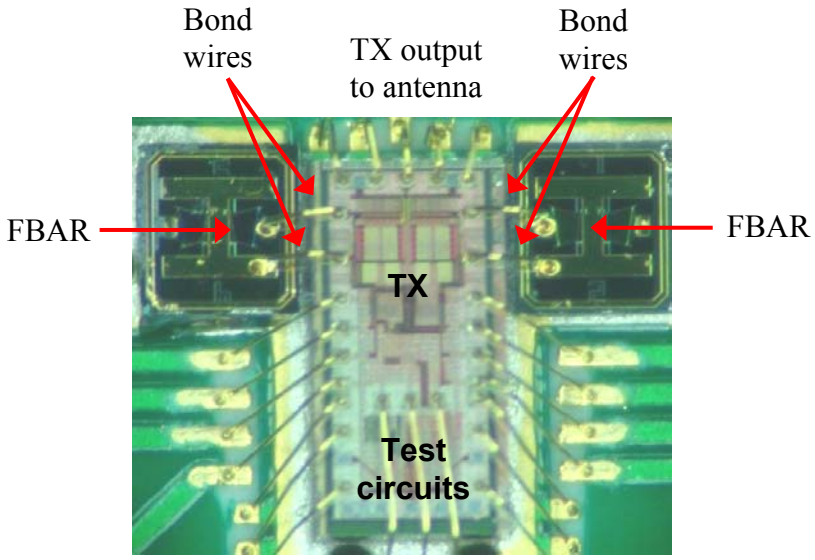


Fig. 5.10: Die photo of the active antenna transmitter.

5.5.2 Measured Results

The transmitter efficiency and power consumption as a function of output power with 0.65V supply are shown in Fig. 5.11. The transmitter achieves a maximum efficiency of

46% while delivering 1.2mW. It consumes 1.35mW when transmitting OOK data assuming equal probability of transmitting a '1' and '0'. The peak drain efficiency of the PA is 63%. The efficiency of the transmitter remains above 41% as the output power varies from 0.85mW to 1.45mW, allowing for efficient power control.

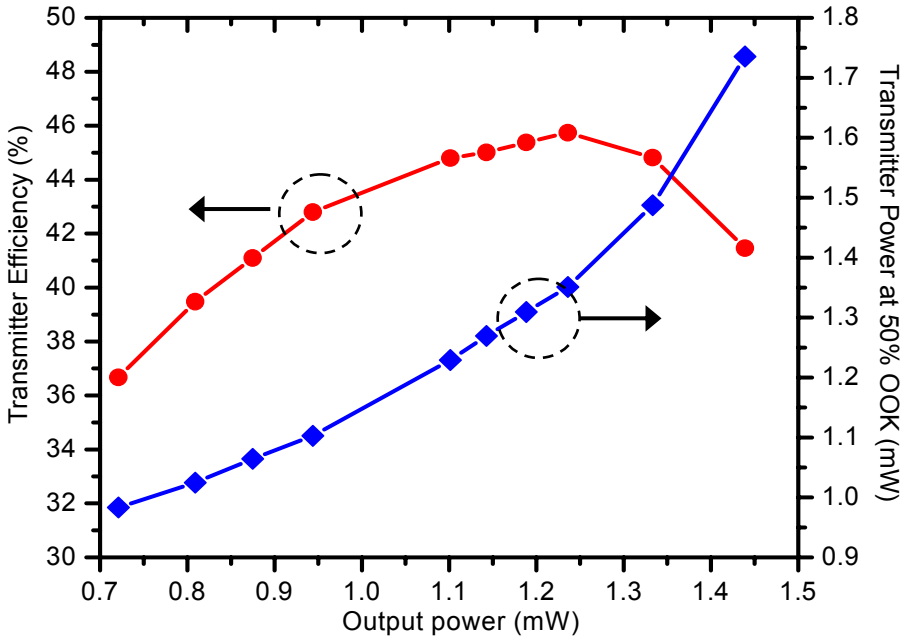


Fig. 5.11: Transmitter efficiency and power consumption as a function of output power.

The startup transient of the fast startup FBAR oscillator is shown in Fig. 5.12. During oscillator startup, both V_{C1} and V_{C2} are high and the oscillator employs two amplifiers to obtain a shorter startup time. Once the oscillator reaches its steady state, V_{C1} is set to low and only one amplifier is used to sustain the oscillation. Using this technique, the startup time is reduced from 580ns to 300ns without significant increase in the pre-PA power. If the oscillator startup accounts for 10% of the symbol period, it is capable of supporting a maximum data rate of 330kbps.

Due to the high Q FBAR, clean and stable RF carriers at 1.863GHz and 1.916GHz are obtained. Figure 5.13 shows the measured phase noise performance of the FBAR oscillator. The measured phase noise is -106dBc/Hz at 10kHz offset and -124dBc/Hz at 100kHz offset. The excellent phase noise performance is primarily due to the high Q FBAR resonators.

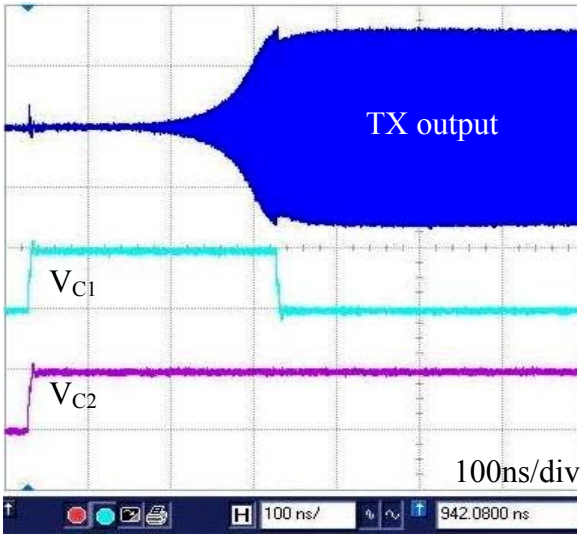


Fig. 5.12: Transient waveform of the fast startup oscillator.

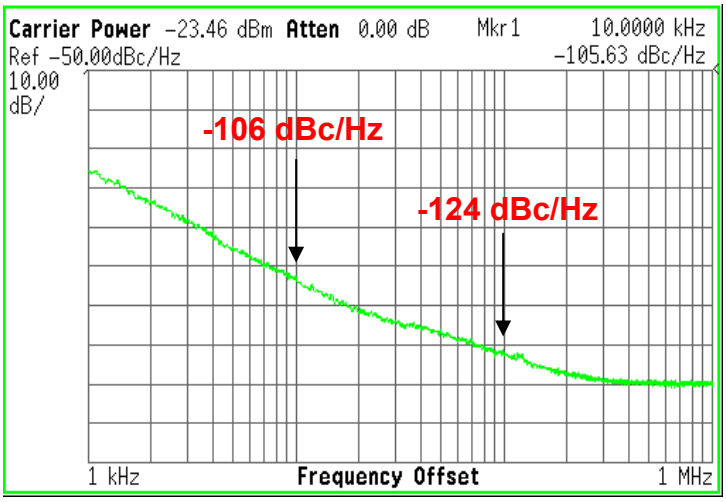


Fig. 5.13: Phase noise performance of the FBAR oscillator

The breakdown of the power budget of the active antenna transmitter and direct modulation transmitter is shown in Fig. 5.14.

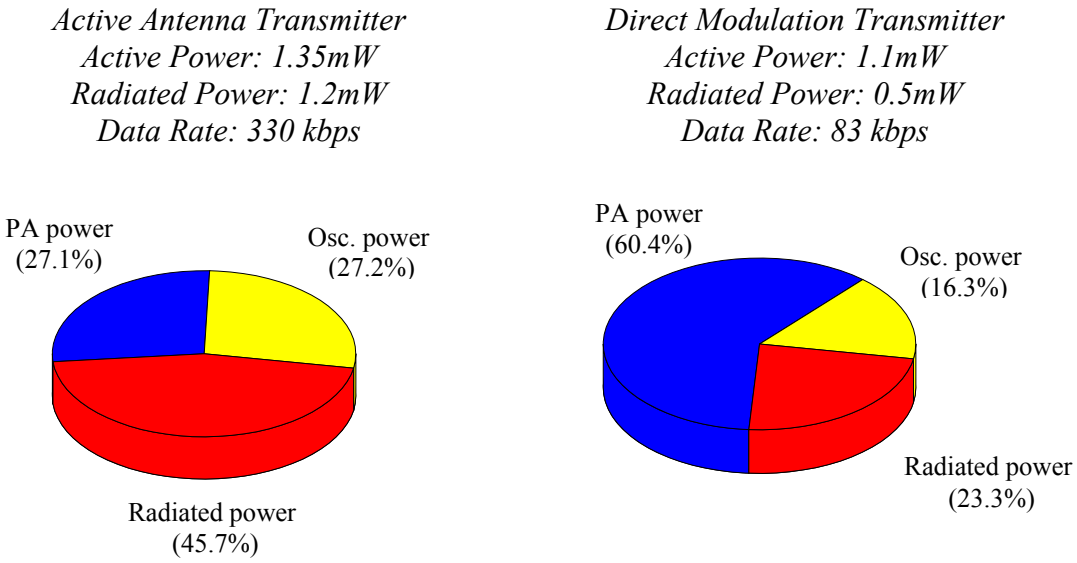


Fig. 5.14: Power budget of (left) active antenna TX, (right) direct modulation TX.

By co-designing the LPA with the antenna and eliminate the matching network, the power loss in the PA is reduced to 27.1% and nearly half of the transmitter power consumption is delivered to the antenna. This results in a higher efficiency transmitter. Due to the faster oscillator startup time, the data rate of the active antenna transmitter is about 4 times higher than of the direct modulation transmitter. This reduces the active time and average transmitter power consumption.

Chapter 6

Wireless Transmit Sensor Node

Three different low power transmitters for wireless sensor network have been designed and implemented in the previous chapters. Among the transmitters, the active antenna transmitter has the highest efficiency, data rate and the lowest average transmitter power consumption. As such, it is most feasible for integration into a small form factor wireless transmit sensor node.

The 38 x 25 x 8.5 mm^3 self contained sensor node operates on two rechargeable batteries and it has power conversion circuits, a low power microcontroller, an active antenna transmitter, a PILA antenna and three sensors to measure temperature, humidity, tilt and acceleration. The batteries can be recharged from a variety of sources including solar cells and other energy scavenging sources.

This chapter is organized as follows: It first gives an overview of the system and describes the design of each of the sub-system. The implementation of the sensor node is then presented. It concludes with a discussion on the performance of the sensor node.

6.1 Sensor Node Design

6.1.1 System Overview

The schematic of the wireless transmit sensor node is shown in Fig. 6.1.

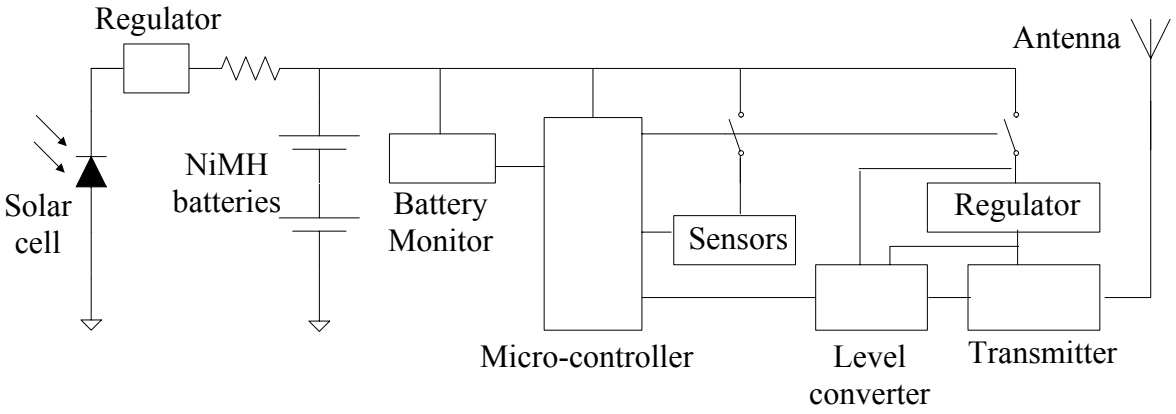


Fig. 6.1: Block diagram of the wireless transmit sensor node.

A charge pump regulator is used to regulate the power scavenged by the solar cell and charge the two NiMH batteries, which in turns power the rest of the system. A battery monitor continuously monitors the state of the battery and shuts down the system once the battery is discharged. This allows the battery to recharge before restarting the system again. The node is equipped with sensors to measure temperature, humidity, acceleration and tilt. A low power microcontroller interfaces with the sensors and the RF transmitter. The sensors and transmitter are power gated to reduce the standby power.

6.1.2 Microcontroller

The sensor node uses the MSP430F1232 ultra low power micro-controller from Texas Instrument [TI04]. The block diagram of the microcontroller is shown in Fig. 6.2.

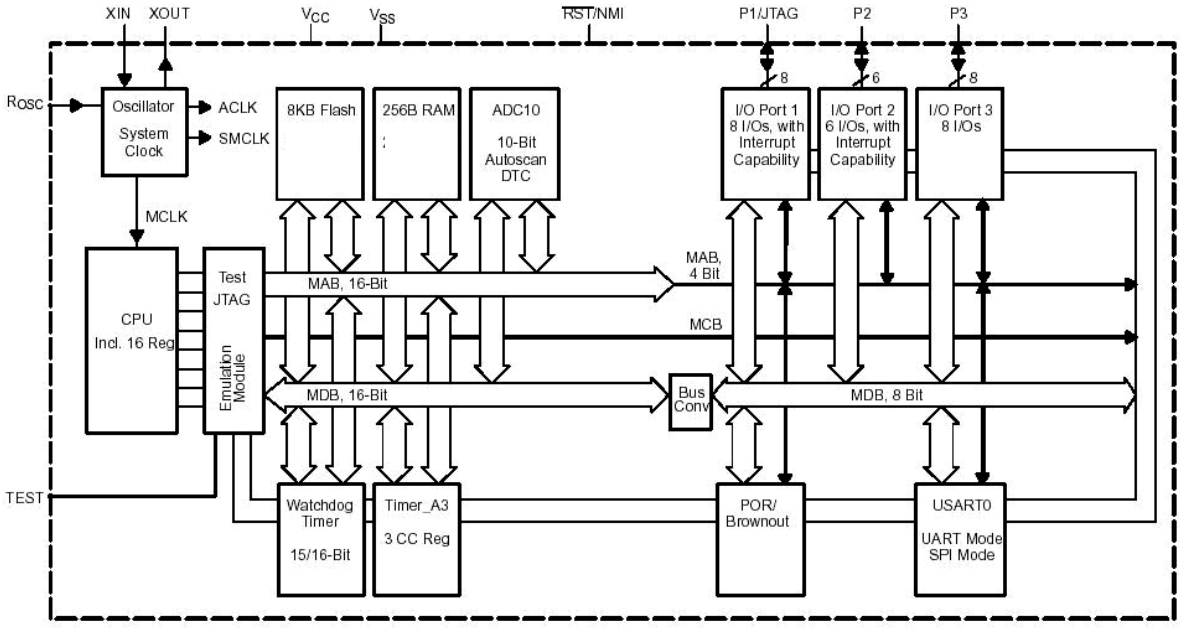


Fig. 6.2: Block diagram of MSP4301232 microcontroller.

The 16-bit RISC microcontroller features 8KB of FLASH memory and 256B of RAM with 125ns of instruction time. It has a clock module that provides a low accuracy clock using a digital control oscillator and a precision clock using a crystal oscillator and an external crystal (32kHz to 8MHz). In this design, the crystal oscillator with a surface mount 32kHz crystal is used to allow for a lower standby power and to reduce timing variations caused by supply and temperature fluctuations. The microcontroller also has a 16-bits watchdog timer and a 16-bits timer with extensive interrupt capability that supports multiple capture/compares and interval timing. These timers are used to provide a time reference to coordinate the events in the sensor node.

To interface with the sensors and RF transmitter, the microcontroller has 22 general purpose I/O and a built-in 10-bit, 200 ksps A/D converter with an internal reference, sample and hold and data transfer controller. The I/O supports digital signals from 0V to

Vdd-0.25V. With the internal A/D converter and general purpose I/O, the microcontroller is capable of interfacing with sensors having both digital and analog outputs. The microcontroller also has a built-in serial communication interface that supports UART and SPI protocol.

To reduce power consumption, the microcontroller has 5 power saving modes. In its lowest power saving mode (LPM4), the clocks, digital controlled oscillator, crystal oscillator and CPU are disabled. In this case, the microcontroller has to be wakened up by the sensors via interrupts (i.e. triggered by external events). To wake up the microcontroller at a preset time, a time base has to be provided. This is achieved by operating the microcontroller in its second lowest power saving mode (LPM3) where only its auxiliary clock is enabled and the rest of the system is disabled. In the active mode, the CPU consumes 200μA/MHz and takes 6μs to wake up from standby.

6.1.3 Sensors

The sensor node is equipped with three sensors to measure acceleration, tilt, temperature and humidity. It uses the 3-axis LIS3L02AQ linear accelerometer from STMicroelectronics [ST04]. The accelerometer is capable of measuring accelerations over a maximum bandwidth of 4kHz for the X and Y axis and 2.5kHz for the Z-axis and has a user selectable full scale of ±2g or ±6g. It includes a sensing element and integrated circuits that process the raw signals from the sensing element and provide an analog output. The accelerometer consumes ~ 850μA in the active mode and 2μA during standby.

The sensor node is also equipped with the D6B tilt sensor from Omron [Omron05]. The D6B, consisting of a Hall integrated circuit and a magnet, is capable of detecting tilt over a range of 45 to 75 degrees in right and left inclinations. It consumes ~ 10 μA and provides a digital output which interfaces with the microcontroller directly.

The sensor node employs the SHT11 sensor from Sensiron [Sensiron05] to measure temperature and humidity. The SHT11 includes a capacitive polymer humidity sensor, a bandgap temperature sensor, a 14 bit A/D converter and a 2-wire serial interface circuit to provide a digital output. The humidity sensor is capable of measuring 0 to 100% relative humidity and the temperature sensor has a range of -40°C to 124°C. The module consumes ~550μA during measurement and 0.3μA in the sleep mode.

6.1.4 Power Train

The power train consists of a solar cell, a charge pump regulator, a battery monitor and two NiMH rechargeable batteries. The node uses a 25 x 32 mm^2 thin film solar module from SolarWorld [SolarWorld05]. This solar module is rated to provide 15mA at 3V under one full sun. However, the available solar power is much less under indoor conditions. Figure 6.3 shows the measured current-voltage characteristics of the solar cell and its output power as a function of load current under typical indoor conditions. Under ambient lighting, the short circuit current is only ~ 45μA and the maximum output power is ~ 70μW. Under fluorescent light, the short circuit current improves to ~ 60μA and the maximum output power increases to ~ 100μW.

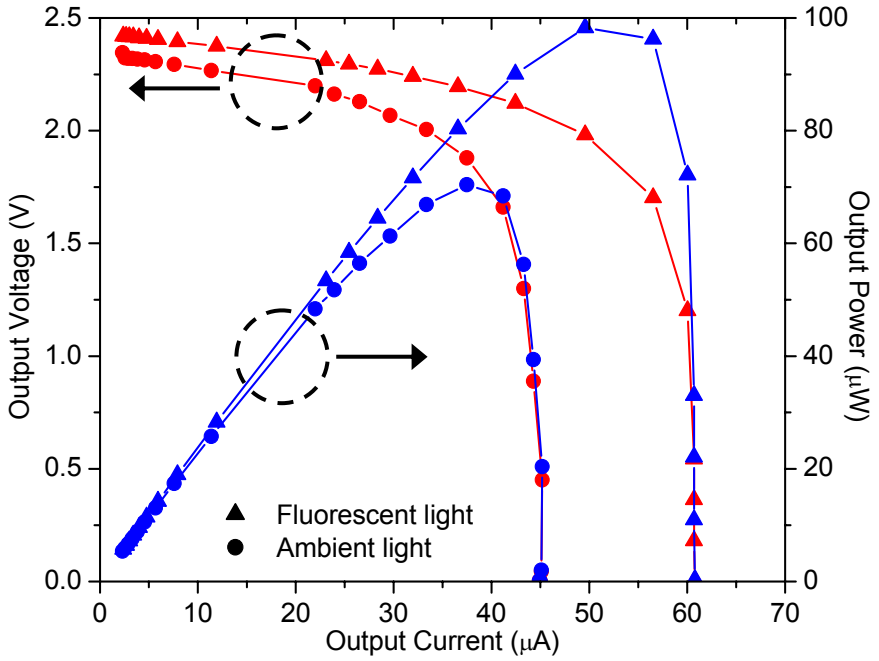


Fig. 6.3: Output power and I-V characteristics of solar cell under indoor conditions.

Since the output voltage of the solar cell fluctuates significantly under different load conditions, it has to be regulated. Thus, it is connected to the TPS60313 high efficiency charge pump regulator from Texas Instruments [TI01] to provide a regulated 3V output. The TPS60313 features a snooze mode where the quiescent current of the circuits and the feedback sampling rate is dramatically reduced at light loads (< 2mA), resulting in a much higher conversion efficiency as shown Fig. 6.4. This is critical for this application since the available power from the solar cell is limited and it is crucial to maintain high conversion efficiency. The regulator accepts input voltages ranging from 0.8V to 2V, which covers the desired operating range of the solar cell in indoor conditions (i.e. at high output power). To prevent electrical overstress at the regulator input (e.g. in outdoor conditions), a zener diode can be used to clamped the input voltage at a maximum of 2V. The charge pump regulator requires only 5 small capacitors and does not need any inductor, which results in a compact footprint.

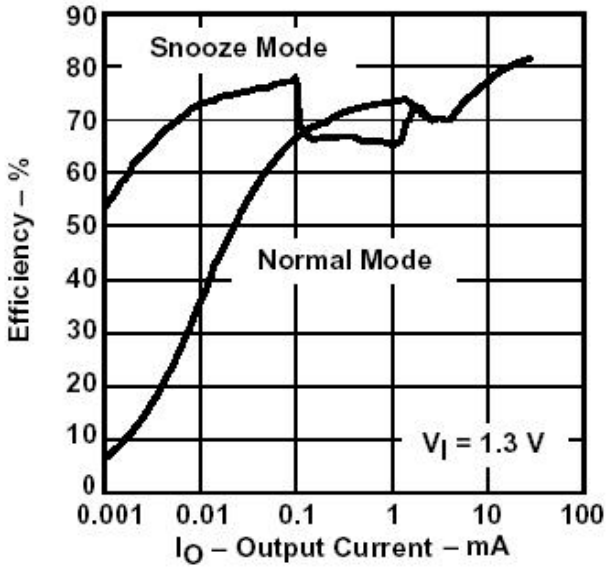


Fig. 6.4: Conversion efficiency of TPS60313 charge pump regulator.

The 3V charge pump regulator charges the two 18mAh NiMH rechargeable batteries via a resistor. The two NiMH batteries are connected in series to provide an output voltage of 2.4V (~2.8V when fully charged) to satisfies the operating voltage of the microcontroller and sensors. The battery has a very small form factor, each having a diameter and height of only 8mm and 5.3mm respectively [Godisa05].

The state of the battery is monitored using the MAX6434 battery monitor from Maxim [Maxim03]. The battery monitor employs a hysteresis that asserts its output when the power supply voltage drops below a specified low threshold (e.g. 2.35V). This shuts down the entire node and allows the solar cell to recharge the battery. When the supply voltage rises above a specified high threshold (e.g. 2.45V), the battery monitor de-asserts its output with a 140ms timeout period. The timeout period ensures that the supply voltage has stabilized before the microcontroller and sensors are enabled. The MAX6434 has user adjustable thresholds and consumes only 1μA.

6.1.5 RF Transmitter

The sensor node employs the active antenna transmitter with the PILA antenna presented in Chapter 5 for data transmission. The active antenna transmitter requires a supply voltage of 0.65V. To convert the 2.4V battery supply to 0.65V, a LTC3020 linear regulator from Linear Technology [Linear04] is used. Linear regulator is employed because existing commercial off the shelf switching regulators do not provide output voltages as low as 0.65V.

The logic high output voltage of the microcontroller general purpose I/O is Vdd-0.25. With a microcontroller supply of 2.4V, this exceeds the voltage rating (~1.3V) of the transistors in the active antenna transmitter. To interface with the transmitter, the SN74AVC8T45 level converter from Texas Instrument [TI05] is employed.

6.2 Sensor Node Operation

Before the sensor node is operational, the user has to download the program to the microcontroller FLASH memory via a JTAG interface. The user can configure the system variables such as the duty cycle for each of the sensors and RF transmitter, the type of sensors to be used and any pre-processing of the sensor data before transmission. Once the system variables are set, further changes require re-programming of the microcontroller FLASH memory.

The state diagram of the sensor node is shown in Fig. 6.5. The operation of the wireless transmit sensor node are governed by 5 states described as follows:

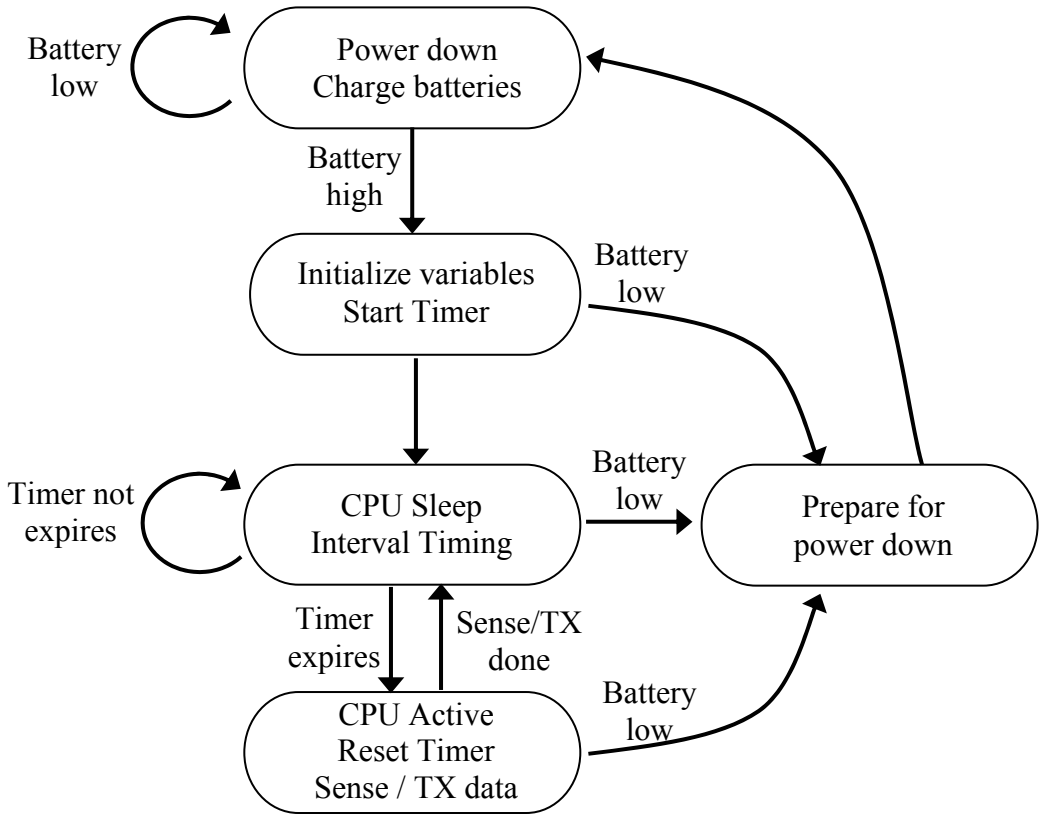


Fig 6.5: State diagram of wireless transmit sensor node.

1. ***Power down.*** In the power down mode, the entire system is shutdown except for the charge pump regulator and the battery monitor. With only minimal circuit power consumption, the excess power collected by the solar cell is used to recharge the batteries. The system stays in this state until the battery monitor indicates the batteries are sufficiently charged.

2. ***Initialization***. Once the batteries are sufficiently charged, the battery monitor de-asserts its output and the microcontroller boots up, goes into its active mode and loads the program from the FLASH memory into its RAM. The program begins to execute and initialize all the system variables. The microcontroller then sets its timer according to the user defined duty cycle and then goes into sleep.

3. ***Sleep***. The CPU and its peripherals remain inactive (except for the timer) until the timer expires. When this occurs, the timer sends an interrupt to wake up the microcontroller.

4. ***Active.*** Once the microcontroller wakes up from its sleep, it will reset and program its timer according to the next user defined interval. Depending on the duty cycle of the sensors and transmitter preset by the user, it will either power up the sensors to sense the required sensor data, or activate the RF transmitter to send out the sensor data accumulated in its memory. For example, the user can configure the node to sense the temperature once every minute and humidity once every 10 minutes, and transmit the data once every 20 minutes.

5. ***Prepare for Power Down.*** Whenever the battery monitor senses that the battery charge is low, it issues an interrupt to the microcontroller. Once the microcontroller receives this interrupt, it terminates its current activities and broadcasts a message indicating that its battery is low and will cease transmission until its battery is recharged. It then shuts down the entire system and goes into the power down state.

With this mode of operation, the microcontroller is woken up at the user defined intervals to perform an action and a clock is required to provide a timing reference at all times. Alternatively, the microcontroller can be woken up by the sensors using interrupts (triggered by external events) and no timing reference is needed. This offers lower average power consumption if the power consumption of keeping the sensor active at all times is less than that of the timer.

6.3 Sensor Node Prototype

6.3.1 Implementation

The wireless transmit sensor node is implemented using standard printed circuit board fabrication and assembly technology as shown in Fig 6.6. The RF transmitter, consisting of the CMOS die and FBAR resonators are assembled using chip on board techniques and the PILA antenna is a printed on the PCB.

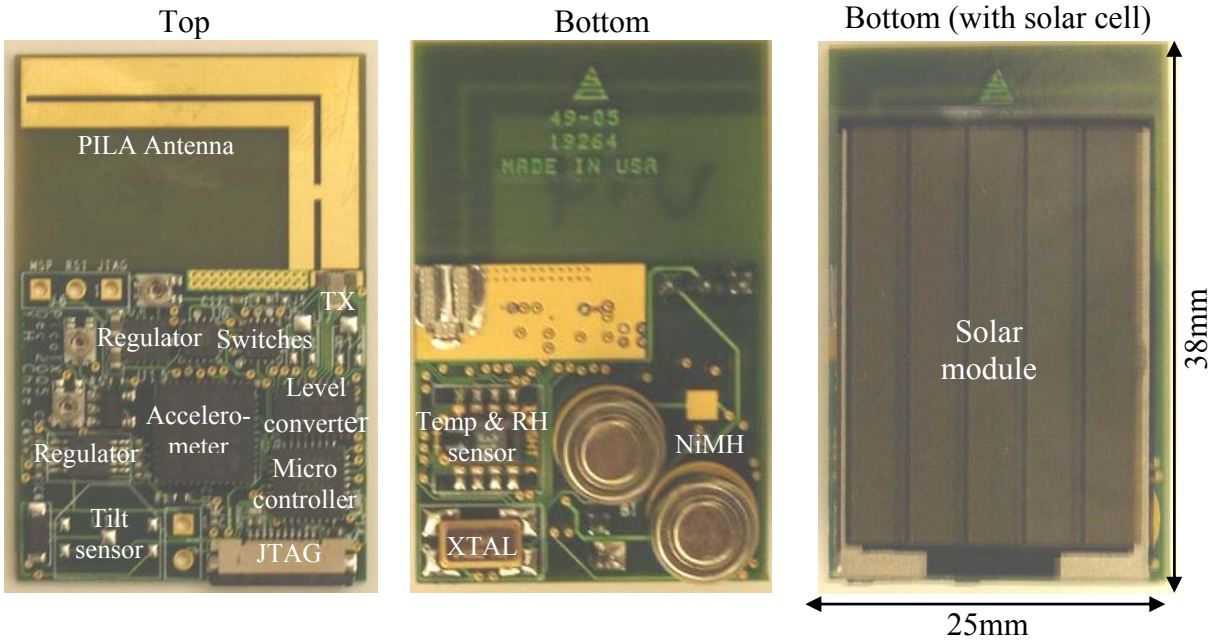


Fig. 6.6: Photo of the wireless transmit sensor node

The printed circuit board consists of 4 copper layers (Top, Bottom, GND and VDD) with minimum line width and spacing of 4 mils each. Nelco laminate is used to reduce substrate losses in the antenna. To reduce the node size, surface mount components with small packages are used as much as possible to minimize their footprints. The components are also carefully placed and oriented to minimize long routing traces and to eliminate an additional separate routing layer. Also, large components (e.g. the NiMH

batteries) are placed as far as possible from the antenna to minimize their effect on the radiated fields.

The node measures about 38 x 25 x 8.5 mm^3 with the stacked solar module and the printed antenna. The size of the board is chosen such that the solar module fits exactly on top of the board with minimal overlap with the antenna. The bill of material is given in Table 6.1.

Table 6.1: Bill of material of wireless transmit sensor node.

Item	Manufacturer	Quantity
CMOS transmitter	Custom	1
FBAR resonators	Agilent Technologies	2
Microcontroller (MSP430F1232)	Texas Instrument	1
8 bit level converter (SN74AVC8T245)	Texas Instrument	1
Charge pump regulator (TPS60313)	Texas Instrument	1
Linear regulator (LTC3020)	Linear	1
Battery Monitor (MAX6434)	Maxim	1
SPST switches (MAX4751)	Maxim	2
Accelerometer (LIS3L02AQ)	ST Microelectronics	1
Tilt Sensor (D6B)	Omron	1
Temp. and humidity sensor (SHT11)	Sensiron	1
8 MHz crystal (ABMM2)	Abracon	1
10 pin ZIF connector	Molex	1
0402 capacitor (2pF, 3pF, 100nF, 1μF)	Panasonic	29
0603 capacitor (2.2μF)	Panasonic	2

Item	Manufacturer	Quantity
Potentiometer (50kΩ, 1MΩ)	Panasonic	2
0402 resistor (0Ω, 200Ω, 50kΩ, 2MΩ)	Panasonic	4
Header (2x1, 3x1)	Digikey	2
NiMH batteries (no 13 button cell)	Godisa	2
Solar module (GTF-2x3)	SolarWorld	1

6.3.2 Measured Results

The current consumption of the wireless transmit sensor node in various states is shown in Table 6.2. During the power down mode, the battery monitor consumes only 2 μA, allowing most of the scavenged power to be used for charging the battery. The charge pump regulator features high efficiency snooze mode which allows it to maintain at high efficiency at low output current levels. During sleep, the microcontroller is shutdown, leaving only the low power 32kHz oscillator to provide an accurate time base.

Table 6.2: Current consumption of wireless transmit sensor node in various states.

State	Supply current
Power down	2 μA
Sleep	2.8 μA
Active (Data processing)	0.86 mA
Active (Transmitting with 50% OOK data)	2.81 mA

With 70μW of available power under indoor condition and the charge pump regulator operating at 75% conversion efficiency, the wireless sensor node can operate with a duty cycle of 0.63%. Under fluorescence light, the available power and duty cycle is increased to 100μW and 0.9% respectively.

Fig. 6.7 shows the received spectrum of the sensor node at about 0.5m away from the spectrum analyzer. A clean output spectrum is obtained. At 10m apart, the received power is -54dBm.

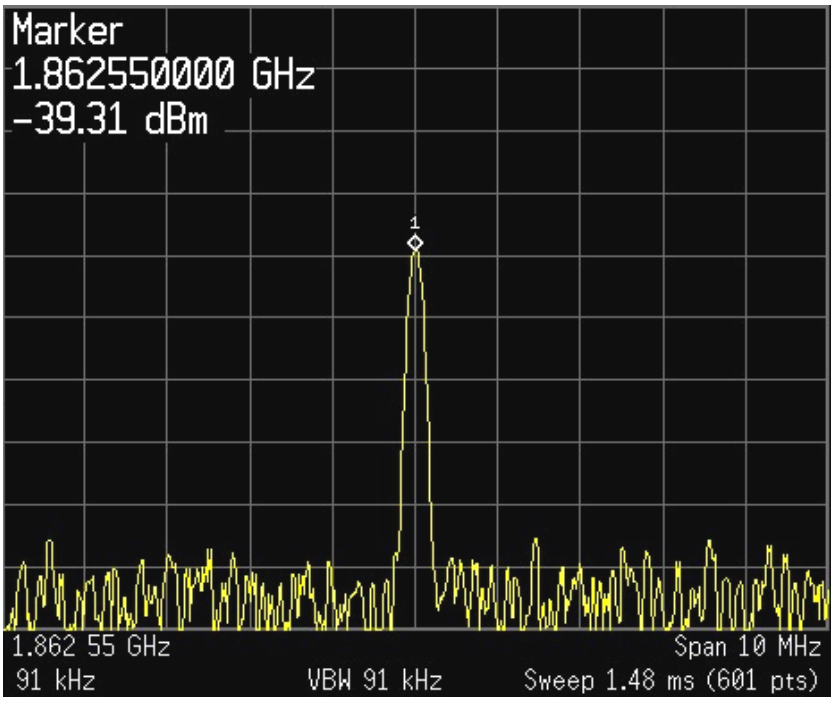


Fig. 6.7: Output spectrum of the wireless transmit sensor node

When an antenna is brought into the vicinity of different materials, its characteristic will be perturbed. Table 6.3 shows the attenuation of the output signal and frequency pulling when the wireless transmit node is placed on top of different materials. It is observed that low dielectric constant materials such as foam, plastic, books and wood do

not cause much attenuation and frequency pulling. The worst case degradation occurs when the node is placed on top of Al plate, which results in 8.7 dB attenuation in the signal power and 80kHz shift in the carrier frequency.

Table 6.3: Environmental effects on wireless transmit sensor node

Material	Signal power attenuation (dB)	Carrier frequency shift (kHz)
Foam	0.3	< 1 kHz
Book	0.8	< 1 kHz
Wood	0.7	< 1 kHz
Plastic (PVC)	0.8	-1 kHz
Solar cell	0.8	10 kHz
Human hand	7.2	-37 kHz
Metal (Aluminium)	8.7	80 kHz

Chapter 7

Conclusion

7.1 Summary

The emerging field of wireless sensor networks could potentially have a profound impact on our everyday life. These ubiquitous wireless sensor networks allow us to sense, manage and actuate a vast number of autonomous sensor/actuator nodes embedded in the fabrics of our daily living environment. Such ambient intelligence provides endless possibilities in a huge variety of application scenarios.

Successfully widespread deployment of wireless sensor networks requires each node to (1) consume less than 100μW of average power for a long usage lifetime and low operational cost, (2) cost less than $1 for a low system cost and (3) occupy less than $1cm^3$ for seamless integration into our physical environment. Among these requirements, the power constraint is the most challenging. Since communication accounts for majority of power budget in a typical sensor node, it is crucial to have an energy efficient transmitter.

In wireless sensor network, the radiated power is low (< 1mW) due to short communication distance (< 10m). As such low radiated power, the pre-PA power is

significant and degrades the transmitter efficiency. This is the main reason for the low efficiency of current state-of-the-art WSN transmitters. Obtaining an energy efficient transmitter at low radiated power requires minimizing (1) overhead power, (2) circuit losses, (3) active time and (4) radiated power.

Based on these principles, three different 1.9GHz transmitters are designed and implemented in ST 0.13μm CMOS process. The direct modulation transmitter employs fewer pre-PA circuits than the traditional direct conversion transmitter and replaces the power hungry frequency synthesizer with an ultra low power FBAR oscillator to reduce the pre-PA power. The entire transmit chain is co-designed together to achieve a transmitter efficiency of 23% at 83 kbps. The injection locked transmitter achieves a better tradeoff between the PA efficiency and its pre-PA power by replacing the power amplifier with a power oscillator and locking it to a FBAR oscillator to obtain a stable carrier frequency. A power oscillator is self-driven and does not load the FBAR oscillator significantly. This allows the FBAR oscillator to operate at its minimal power consumption (i.e. less pre-PA power) and stays active throughout data transmission, resulting in a higher data rate. The transmitter achieves an efficiency of 28% and supports a data rate up till 156kbps. The active antenna transmitter incorporates the matching network into the PILA antenna to eliminate the matching network loss, enhancing the transmitter efficiency to 46%. It also employs two amplifiers during oscillator startup to achieve a high data rate of 330 kbps.

To demonstrate a low power and small form factor sensor node, the active antenna transmitter is integrated into a 38 x 25 x 8.5 mm^3 wireless transmit sensor node. The

sensor node operates on two NiMH batteries that are recharged by a solar cell and includes power conversion circuits, a low power microcontroller, level converter and three sensors to measure temperature, humidity, tilt and acceleration. The node consumes 2.8 μA during sleep and 2.81mA when transmitter 50% OOK data. With 70μW of available power under indoor conditions, it can operate with a duty cycle of 0.63%.

By employing low power transmitter architectures, low power circuit design techniques and CMOS/MEMS co-design, the work presented this thesis has push the performance envelope of WSN transmitters significantly as shown in Fig 7.1.

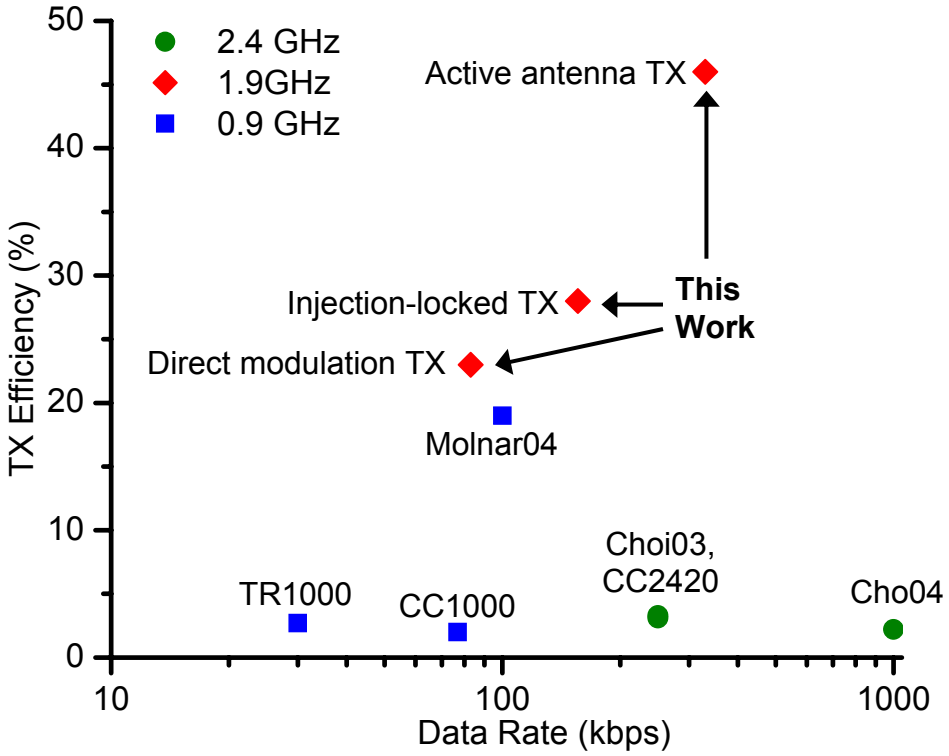


Fig 7.1: Performance of state-of-the-art WSN transmitters

7.2 Perspectives

The research work presented in this thesis has certainly brings us one step closer to realize the full potential of wireless sensor networks. However, much research is needed in the following areas to fully realize the potential of wireless sensor networks:

1. ***Device technology***. Higher performance CMOS transistors and higher Q FBAR resonators are needed to reduce the power consumption of the sensor node. Advancement in other areas of MEMS (e.g. MEMS switches, MEMS tunable antenna, etc) is also needed to overcome the limitations of CMOS technology.
2. ***Packaging and Integration***. System in package (SIP) or above-IC integration in essential to integrate high performance passives/MEMS while keeping a small form factor. Three dimensional packaging could also be used to further reduce the size of the node.
3. ***Smarter nodes***. The capabilities of the node can be extended by incorporating an ultra low power receiver, advanced power management techniques and more computation power. It can also be made more adaptive to the environment (e.g. adapt the antenna impedance and radiation pattern according the node's surrounding).

Extending the idea of wireless sensor networks, one could also further explore design and limits of much denser networks (i.e. much shorter communication distance, say < 5cm). With such short communication distance, it is possible to employ reactive communications rather than radiative communications, bringing new design challenges and limits.

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