# A Methodology for Robust System-Level Design: Theoretical Foundations and Preliminary Case-Study

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# A Methodology for Robust System-Level Design: Theoretical Foundations and Preliminary Case-Study

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## ABSTRACT

We build the theoretical foundations of a platform-based methodology for robust mixed-signal system design in the presence of process technology and design parameter variations. Differently than previous approaches, based on maximizing safety margins *generically* enforced at system and architectural levels, we leverage variability models to provide *specific*, statistical annotation and bottom-up propagation of performance deviations of platform components at system level. Hierarchical design space exploration and optimization can then be carried across the performance/yield/cost boundaries thus avoiding pessimistic worst-case approaches. The effectiveness of our formulation is illustrated on the design of regenerative comparators, key building blocks of modern A/D interfaces. After showing how behavioral, performance and variability models can be *automatically* generated from basic structural properties of the circuit topology, we exploit our abstraction as a powerful tool to deploy robust design techniques and create a reliable library element out of unreliable components.

## 1. INTRODUCTION

Embedded electronic systems are currently experiencing a growing gap between the highly demanding requirement of their software-centric applications and the nano-scale related limitations of system-on-chip technologies. A set of challenges are then posed to the electronic design automation industry in the attempt of bridging this gap and making again reliable those levels of abstractions that have been so far the key articulation points of electronic design flows. The problem is exacerbated by the presence of analog and RF components in most modern chips, bringing a number of second order effects, as well as dependencies between functionality and complex device physics, which make automation efforts either computationally intractable or unacceptably inaccurate. While reliability and process yield are being already absorbed in traditional design flows at the physical level (leading to the concept of "design for manufacturability"), there is an urgent need for rigorous methodologies and design tools that address the analog/mixed signal problem *at the system* level. System level design should embrace robust approaches for two separate reasons. From the system level, mixed signal design has to cope with model inaccuracies that are intrinsic to the behavioral models exploited in design explorations. The more complex the system, the larger the hierarchical structure of the design and the higher the risk when performing nominal design optimizations. In fact, composition of high level models may provide results whose accuracy is not easily bounded, so either a costly iterative scheme between top-down system level design and bottom-up verification or relaxed (robust) constraint propagation is adopted. From the implementation level, any performance model is subject to two kinds of inaccuracies: intrinsic modeling errors and process or environmental variability. While some control is available on the former source (even if potentially very expensive or restrictive), the latter cannot be solved with deterministic approaches.

Early approaches to robust computer aided design in an analog context date back to the early 80s [1, 2, 3] with the introduction of *statistical design* methods. These methods were based either on Monte Carlo techniques or on models to capture performance degradations and joint probability functions to compute yield expectations (design centering). However, robust optimization for analog design has not been developed at the same level as nominal optimization. The largest obstacle on the way is represented by the tremendous complexity of the resulting optimization problem, that is usually captured as a semi- infinite programming problem. A direct extension of classical robust techniques to system level analog and mixed-signal design is therefore deemed very unlikely to happen. Alternative approaches based on approximate models must be developed at the system level, where the models generated with classic approaches based on Response Surface Methodology (RSM) [4] become too expensive to build because of the number of primal parameters and the complexity of the necessary simulations.

In this project, we lay the foundations of a robust design methodology for mixed-signal systems, based on the principles of Platform-Based Design (PBD). We look at PBD [5] as the natural paradigm for mixed-system design formalization because of its two-tiered "meet-in-the-middle" approach, very suitable to represent the particular nature of analog design. While inheriting the *analog platform* abstraction from its precursor *nominal* design methodology [6, 7], Robust Platform Based Design (RPBD) originates as a *technology-aware* design discipline, where platform components are decorated with *variability models* to capture their behavior in the presence of process technology and design parameter variations. Our approach allows quantitative extension of robust techniques from design centering and yield optimization to hierarchical analog and mixed-signal designs. Moreover, analog performance figures and constraints which are critically bound to process and design variability, such as offset or matching, can be accurately

estimated via statistical models. We demonstrate the effectiveness of our formulation by generating abstractions for a crucial, intrinsically mixed-signal component such as a voltage comparator. We show that accurate modeling of undesired component behaviors where they actually originate is a powerful tool for the integration of reliable systems out of unreliable components.

# 2. BACKGROUND

## 2.1 Related Works

Several robust approaches to analog design have been proposed during the past few years. Initially, relaxation of system constraints during top-down optimizations where exploited as an attempt to overcome poor architecture models. We can date back the first rigorous attempt in this direction with the top-down constraint-driven methodology presented in [8]. Since in pure top-down approaches no detailed information is available on implementation as architectures have not been selected in the first design steps, the methodology formulates the optimization problem (constraint propagation problem) as the maximization of a set of *flexibility functions*. Flexibility functions are introduced to capture the complexity of implementing a specific set of performances. Therefore, in place of optimizing for power or area, the optimization problems maximize the "flexibility" of achieving the optimum set of performances (i.e. minimize the "effort" of implementation). Albeit rigorously formulated, the methodology was rather limited in performing aggressive optimizations because of the halo inherently inserted by the heuristic flexibility functions.

Recent advances in convex optimization [9] have revitalized analytical approaches to analog design, hence robust design. ROAD [10] introduces a robust optimization approach based on posynomial performance models. To improve accuracy, a simulator-in-the-loop approach is selected and local posynomial models generated around design points. It is then possible to deal with non-convex design spaces exploiting the possibility of exactly solving large scale convex programs. However, convex optimization approaches tend to limit designers in selecting cost function and formulating their problems. The efficiency achieved in actually solving the problem may be then counterbalanced by the effort required to model the system and validate the analytical expressions used to set the problem. Moreover, classic approaches to system design with convex optimization are based on generating a flat optimization problem, where all circuit topologies have been selected, thus setting a challenging problem as system complexity grows and mixed-signal designs are approached. Recently, a hierarchical approach to robust system level analog design has been presented [11]. Performance centering is sought through concurrent maximization of system level flexibility based on behavioral models and implementation level performance margins based on performance models. A possible limitation of the approach is still the requirement of posynomial models to capture both system level and implementation level constraints. While this assumption is certainly acceptable for some classes of analog systems, it may be in practice a hard one to satisfy as it becomes increasingly difficult to guarantee (or even assess) model convexity as design hierarchy becomes deeper and high-level behavioral models are exploited in mixed-signal design space explorations.

## 2.2 Nominal Analog Platform Based Design

The extension of PBD to analog circuits (APBD) has proved to be effective in tackling complex problems such as hierarchical design space exploration and optimization across the analog/digital boundary [6, 7]. A platform is generally expressed as a collection of components and composition rules. A design is obtained by composing components of the platform in a platform instance. The refinement process consists of mapping a functional description into a set of interconnected components. This allows a systematic exploration of the design space through a series of mapping of top-down constraints of the system onto bottom-up characterizations of the feasibility space of each component in the platform library.

Analog platform performance models originally rely on Support Vector Machines (SVMs) as a way of approximating a classifier $\mathcal{P}$ discriminating the feasible performance space. The performance space is sampled through simulation so that accurate performance models (not constrained to be posynomial) can be exploited. However, robust design strategies have only been introduced by relying on worst case approaches, or on maximization of generic margins in the performance models of the platform elements [12]. No clear indication has been provided about the sensitivity of performance figures on process variability and complicated heuristics were needed to adequately formulate the cost functions properly weighing both system level and architecture level margins.

# 3. ROBUST PLATFORM BASED DESIGN

## 3.1 Component Abstraction Formulation

Formally, a Robust Platform (RP) consists in a collection of components (e.g. mixed-signal circuits or cells), each decorated with:

- a set of input variables $u \in \mathcal{U}$, a set of output (performance) variables $y \in \mathcal{Y}$, a set of internal variables $x \in \mathcal{X}$ (including state variables), a set of configuration parameters $\kappa \in \mathcal{K}$, a set of variability (statistical) parameters $\delta \in \mathcal{D}$;
- a *functional model* that implicitly expresses all the possible component behaviors as $\mathcal{F}(u, y, x, \kappa, \delta) = 0$, where $\mathcal{F}(.)$ may include integro-differential components; in general, this set determines uniquely $x$ and $y$ given $u$, $k$ and an instance of the random variables $\delta$. Note that the variables considered here can be function of time and that the functional $\mathcal{F}$ includes constraints on the set of variables (for example, the initial conditions on the state of variables);
- *validity laws* $\mathcal{L}(u, y, x, \kappa, \delta) \leq 0$, constraints (or *assumptions*) on the variables and parameters of the component that define the range of the variables for which the functional model is *guaranteed* as being valid.

Note that the necessary information is all contained in the functional model, which is as general as, most of the times, very complicated to manage. It is therefore more practical for design exploration and optimization to rely on different *projections* of the functional model on different sets of variables of interest to the designer. In particular, we define the following projections of the functional model:

- the *behavioral model*, i.e. an *instance oriented model* $\mathcal{B}(u, y, x) = \mathcal{F}(u, y, x, \kappa, \delta)_{\kappa=\kappa_0, \delta=\delta_0} = 0$, which captures the input/state/output *dynamic* behavior of the component, as a totally ordered (continuous or discrete) or partially ordered set of events, for a fixed set of configurations (i.e. after the circuit has been already designed) and parameter deviations. An interesting behavioral model particular case is the nominal behavioral model, where all parameter deviations are equal to their expected value 0 ($\delta = \mathrm{E}\{\delta\} = 0$).

- the *feasible performance model*. Let $\phi_y(u, \kappa, \delta)_{\delta=0}$ denote the functional model projection (map) that computes the performance $y$ corresponding to a particular value of $u$ and $\kappa$ by solving the behavioral model in nominal conditions. The feasible performance set is then the set described by the relation $\mathcal{P}(y(u)) = 1 \Leftrightarrow \exists \kappa', y(u) = \phi_y(\kappa', u)$. The feasible performance set can be directly approximated as in the basic APBD approach, or it can be computed by solving the behavioral model for a number of parameters $\kappa$. While solving the circuit differential algebraic equations (DAE) is a time consuming task, a possible approach is to provide an approximation of the relation between $u$ and $\kappa$ with explicit functions. These functions can be determined by still exploiting simulation-based approximation schemes or algorithmic macromodelling techniques, as proposed in this project.

- the *variability model* which, based on statistical assumptions on parameter deviations, computes quantities such as yield or failure probability. For instance, we can assume a partial ordering among component performance vectors, defined as follows: $y_1 \preceq y_2$ iff $\forall i$, $y_{1i}$ is superior or equal to $y_{2i}$. We can then define the failure probability of a component in satisfying a specification set $y_0$ as $P_f = P(\phi_y(u, \kappa, \delta) \succeq y_0)$ for a given $\kappa$ and $u$.

## 3.2 Model Generation

Traditionally, it is deemed unfeasible to export variability information together with performance models as for each circuit configuration $\overline{\kappa}$ a function should be provided $\phi(y; \overline{\kappa})$ which computes the probability density function of performance $y$ given the circuit sizing $\overline{\kappa}$. As the approximation of $\phi$ usually relies on expensive Monte Carlo simulations around $\overline{\kappa}$, the generation of $\phi(y, \kappa)$ over the entire configuration space $\mathcal{K}$ is hardly doable.

In this project we propose a strategy to overcome this issue. We start observing that experienced mixed-circuit designers generally tend to operate with a reduced parameter set and simplified models, allowing them to intuitively reach the appropriate compromises between components in a complex system. In fact, analog circuits can be typically decomposed into elementary sub-components we denote as *analog patterns* (such as current sources, differential pairs,...) performing *atomic functions*. Recognizing such patterns allows automatic constraint generation to be used in the optimization and exploration process, and even algorithmic generation of reduced order macromodels [13]. Clearly enough, the granularity of the components from which the design is developed is a key element in our approach and will be object of future research.

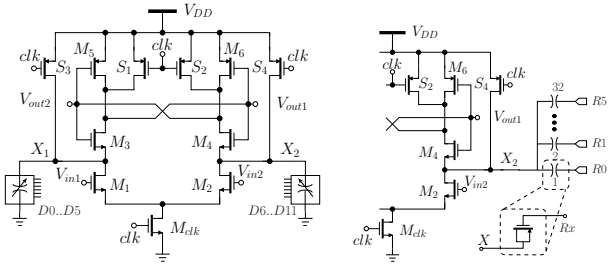


**Figure 1:** Dynamic comparator topology (left side) and calibration devices (right side). Binary scaled arrays are connected on both sides of the comparator.

# 4. ROBUST COMPARATOR DESIGN

We have applied RPBD in our formulation to the comparator (StrongArm latch) represented in Fig. 1. The abstraction domains can be defined as follows: $\mathcal{U}$ is the set of $Vin(t)$ such that $|Vin| \leq 0.5$ V, $f_{max} = 0.7$ GHz; $\mathcal{K}$ is the set of MOS sizings $W_i$ and $L_i$; $\mathcal{X}$ is the set of internal voltages and currents; $\mathcal{Y}$ is the set of {$Vout(t)$, BW, Noise, Offset}, $\mathcal{D}$ is the set of sizing and threshold voltage deviations due to process variability, $\frac{\delta\beta}{\beta}$ and $\delta V_t$. The comparator is designed in a 1.8V 0.18$\mu$m CMOS technology.

## 4.1 Behavioral model

The comparator consists of an input differential pair feeding current into a latch composed by two cross-coupled inverters. Current is supplied through transistor $M_{clk}$. Comparison and reset phases are controlled by the clock signal *clk*. When *clk* is low, no current is drawn as $M_{clk}$ is off. The input signal is tracked on the input capacitances of $M_1$ and $M_2$ (differentially). The output nodes, as well as the regenerative inverter pair $M_3 - M_6$ are linked to $V_{DD}$ through $S_1 - S_4$. When *clk* goes high, $M_1 - M_2$ force currents through the inverters $M_3 - M_5$ and $M_4 - M_6$. As $i_{D1}$ and $i_{D2}$ depend on the input signal, the input capacitances of the regenerative inverter pair are discharged with different rates triggering regeneration and latching of the result.

We then recognize the *differential pair* and the *cross-coupled inverter latch* as the two basic *patterns* in our topology. Although the circuit is a strongly non-linear time varying system, its dissection in the two main building sub-blocks makes it feasible to apply a *stepwise linear approach* to generate reduced order systems of equations capturing the dynamic behavior of the circuit. In particular, the circuit is assumed to have a finite number of *operating phases*, where the circuit is linearized and analyzed. Transitions between phases are assumed instantaneous, thus neglected. In this project, given the low complexity of the differential equations governing the equivalent circuit in each phase for this particular topology, the continuous time evolution of the output voltage is obtained by analytically solving the equations and joining results with continuity so that the starting point of each phase coincides with the final point of the previous one. A typical behavior is shown by the waveforms in Fig. 2, together with the equivalent linearized and reduced circuits used in the calculations.

## 4.2 Performance model

Once the solution of the circuit differential equations is available in a compact (analytical) form, performances can be also analytically computed and related to design param-

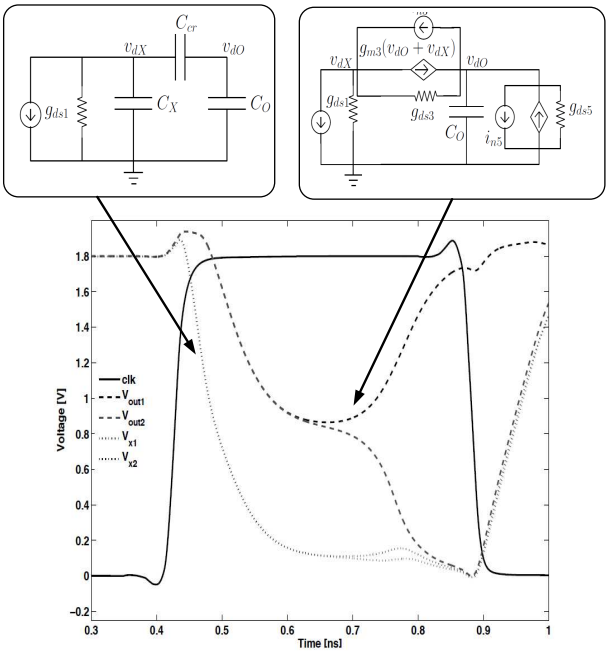


**Figure 2:** Comparator typical output waveforms and reduced order equivalent circuits in two different operation phases of the comparator.

eters. For instance, the comparator *bandwidth* can be computed starting from the time constants of the reduced linearized circuits. These time constants are both function of the circuit small signal parameters, hence, through a simplified MOS model, of the circuit configurations (design variables). When better accuracy is needed, performances can be numerically computed by executing the reduced behavioral model and more accurate, possibly reduced, MOS models. This approach could still be inferior in accuracy with respect to an (electrical) simulation based approximation scheme, but it can be generated faster and tend to be more appealing to designers.

Analogously, to compute the comparator *noise*, we can assume that the input signal voltage is zero and solve the same circuit equations as for the behavioral model. In this case, however, circuit stimuli are provided by time-varying random noise sources, and a stochastic differential equation need to be solved. However, in most of the cases, under some hypothesis on the noise probability density function (e.g. white gaussian hypothesis), these equations can be reduced to ordinary differential equations, as demonstrated in [14]. In Fig. 3 we compare our estimation of the input referred (thermal) noise with electrical simulations. The RMS noise value (noise standard deviation) is plotted as a function of the sizes of transistors $M_1$ and $M_{clk}$. Our performance model provide a *conservative approximation* in the sense that it is able to predict the comparator behavior with a maximum 20% overestimation, in spite of the oversimplified models used in this example. Further detailed formulas for the interested reader can be found in [14, 15].

## 4.3 Variability model

The comparator variability model should accurately estimate the input referred offset for a fixed set of configuration parameters. The offset can be determined using an auto-

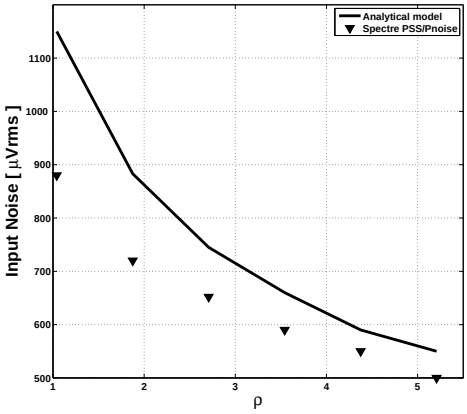


**Figure 3:** Comparator performance model projected on the (input referred) noise vs. $\rho$ ($W_1/W_{clk}$) plane ($W_3/W_{clk} = 1.33$, common mode voltage $V_{CM} = 1.65$V). The analytical compact model provides a conservative approximation tracking noise behavior with a maximum 20% over-estimation.

mated extraction procedure [16], which allows avoiding expensive statistical simulations. In fact, exploiting standard mismatch models (e.g. Pelgrom's model) we can express the total offset variance $\sigma^2_{OR}$ as:

$$\sigma^2_{OR} = \sum_{i=1}^{N} \left[ \left( \frac{\partial v_{OR}}{\partial V_{Ti}} \right)^2 \sigma^2_{V_{Ti}} + \left( \frac{\partial v_{OR}}{\partial \beta_i} \right)^2 \sigma^2_{\beta_i} \right] \qquad (1)$$

where $N$ is the total number of transistors and the standard deviations ($\sigma_{V_{Ti}}$,$\sigma_{\beta_i}$) are expressed in terms of transistor sizes and technology constants. In principle, the partial derivatives could be directly determined from the same reduced order equations we have used for both behavioral and performance models. This is equivalent to provide a rough offset estimation by linearizing the circuit equations at the comparator metastable point.

As an alternative, we propose a more efficient and, at the same time, more accurate simulation-based strategy, that can be quickly repeated on several circuit configurations to extract the complete model. In detail, the partial derivatives in (1) have been determined through finite differences according to the following approximation:

$$\frac{\partial v_{OR}}{\partial X_i} \approx \frac{\Delta v_{OR}}{\Delta X_i} = \frac{v_{OR,X_i}}{\sigma_{X_i}}. \qquad (2)$$

Based on (2) a number of electrical simulations have been performed by applying for every statistical variable its $\sigma$ value, and leaving all other variables at their mean value, and the offset in this conditions has been extracted through a bi-section method based root finder.

## 4.4 Offset-Free Comparator Abstraction

Leveraging rigorous analysis of device mismatch, we can now optimize our design across the yield/power boundary. A classical approach to low-offset comparator design consists in deciding transistor sizes so as to meet offset specifications in the worst case. In today's process technologies this would normally turn into large area and power consumptions since larger transistors also bring larger parasitic capacitances to be charged and discharged in the same amount of time.

A more interesting approach is to *orthogonalize concerns*, by relying on offset compensation and calibration techniques to decouple the power from the variability problem. The comparator input offset can indeed be compensated by exploiting the fact that any load difference $\Delta C = C_{X_1} - C_{X_2}$ at the drains of $M_1$ and $M_2$ causes a shift in the trip point given by the following first order expression:

$$V_{io} = \frac{I_D}{g_{m1}} \frac{\Delta C}{C_X} = \frac{V_{ov1}}{2} \frac{\Delta C}{C_X} \quad (3)$$

where $C_X$ is the load capacitance in the balanced case, $I_D$, $g_{m1}$ and $V_{ov1}$ are the (average) current, transconductance and overdrive, respectively, of the input pair in saturation during the initial drain node discharging phase. Binary sized array of MOS capacitors can then be inserted on both sides of the comparator with the possibility of digitally changing the value of each single capacitance [15], as shown in Fig. 1 (right side). As a result, the comparator can be calibrated both to compensate random mismatch and to configure the comparator threshold. In our case-study, the evaluation of (1) produced a $\sigma_{OR}$ as high as 20mV. As a consequence, when the comparator is used for analog-to-digital converter design, the capacitor array has to be sized to provide a minimum correction voltage less than one half of the converter least significant bit (LSB) and a maximum correction voltage larger than the $3\sigma_{OR}$. Based on electrical simulations, six binary scaled devices per side could be used, requiring a 12 bit digital calibration word for each comparator.

Compensation techniques similar to the one we have described above can be naturally integrated in our framework, since proper modeling of non-idealities in those points where they originate can better help devising an adequate correction scheme. By composing a highly mismatched comparator with adequate correction blocks, we have built a new offset-free threshold configurable component to be inserted in the library. Therefore, while being *enabled* by the PBD paradigm, robust design becomes itself an *enabler* for the methodology, since it can builds reliable layers to be used for system level exploration and optimization.

## 5. CONCLUSIONS

We have proposed a platform-based robust mixed-signal design methodology, where in addition to behavioral and performance models, variability models capture process and environmental variations in platform components. We have applied our formulation to comparator design by building a suitable component abstraction for system-level design. Comparator offset is a critical performance figure, tightly linked to circuit parameter deviations from their nominal values. We exploit the comparator variability model to create an offset-free reconfigurable library element out of a heavily mismatched component, relying on compensation and calibration techniques that can be rigorously formalized within our framework. Practically all possible component behaviors can be fully characterized within our methodology, which will be further developed in the future to become the natural context for deploying robust design/optimization techniques.

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