Energy Efficient Wireless Transmitters: Polar and Direct-Digital Modulation Architectures

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by

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Abstract

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Power consumption is an increasingly important issue in highly integrated wireless systems. While advances in semiconductor technology have driven continuous integration of features and services into portable devices, power consumption is now a major limiting factor on computational complexity and the ability to communicate over long distances. In portable communication devices, the wireless transmitter is often the dominant source of power consumption, such that in recent years there has been a major effort to improve the power efficiency of transmitter circuits, especially the power amplifier (PA). In addition to power consumption, it is now apparent that energy consumption is an important metric for transmitter circuits. Energy consumption more accurately predicts the battery life, especially when a portable system operates with a wide range of output power.

In this work, polar transmitter architectures are presented as a promising alternative to conventional Cartesian architectures. Traditional polar systems use dynamic modulation of the PA power supply to transmit amplitude information. This helps polar systems achieve higher average (energy) efficiency than Cartesian systems. Polar systems have suffered from drawbacks related to linearity, time-alignment of amplitude and phase signals, and power supply noise. Furthermore, the amplitude and phase paths require bandwidth significantly higher than the Cartesian I-Q basis vectors to represent the wideband polar representation of the wireless signal.

This work focuses on several contributions related to improving the operation of energy efficient polar transmitters. The first contribution is a power supply noise analysis framework for nominally linear power amplifiers. This analysis helps predict upconversion of supply noise to RF frequencies – a scenario that is likely in polar and envelope tracking supply-modulated transmitters. Supply noise upconversion can cause violation of the spectral mask and it is important to understand the underlying circuit mechanisms for this phenomenon.

A second contribution is an optimal operating strategy for hybrid switching-linear voltage regulators. These regulators are attractive for polar systems since they achieve the wideband, high-fidelity performance of a linear regulator with the power efficiency of a switching regulator. We show that past implementations of hybrid regulators could achieve higher efficiency with an optimized control objective. We use time-domain averaging to determine the optimum current for the DC-DC converter in the hybrid regulator. The optimized solution achieves substantially higher efficiency across the

output power range than the traditional solution. We develop expressions for optimum efficiency as a function of characteristics of the envelope signal and the supply voltage for the linear regulator.

The final contribution is a digital-polar transmitter based on pulse-density modulation of the RF carrier. Instead of using power supply modulation, the amplitude path is controlled with a digital noise-shaping process. To reduce power consumption, noise shaping is implemented in two stages: a baseband $\Delta\Sigma$ modulator operating at 100MHz and a programmed pulse-density modulator operating at 2.4GHz. A circuit implemented in 90nm CMOS uses a class D PA to achieve up to 20dBm output power. The system achieves peak efficiency of 38.5% at 2.4GHz including power of the PA drivers and filter insertion loss. EVM is approximately 2.0% for 8DQPSK and π/4DQPSK constellation trajectories. The spectral mask for Bluetooth 2.1+EDR is satisfied under normal conditions.

Overall this work highlights several techniques that help improve energy efficiency of wireless systems. Hopefully these solutions will paint a roadmap of future work that will help commercial development and lead to many challenging research problems and academic contributions.

Professor Seth R. Sanders
Dissertation Committee Chair

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Chapter 1 Introduction

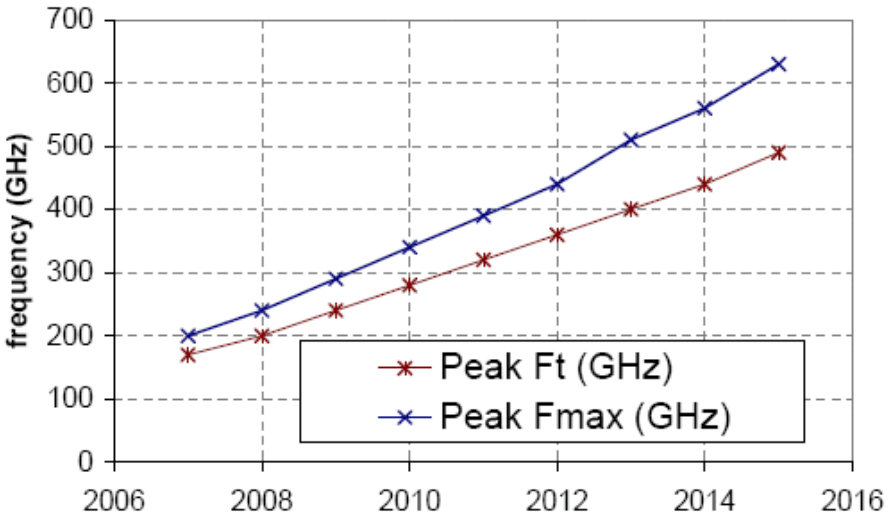


Figure 1. CMOS f_t and f_{max} (performance analog/mixed signal devices), International technology roadmap for semiconductors (ITRS) [1].

After decades of successful process and technology scaling, active semiconductor devices are now operating with current and power gain-bandwidths (f_t and f_{max}) in excess of 100GHz [1, 2]. Shown in Figure 1, this trend is expected to continue for some time into the future, expanding power efficient operation of conventional analog and digital circuitry to radio frequencies. In modern digital CMOS technologies, core libraries of standard cells can operate at low-GHz carrier frequencies. Combined with extraction of layout parasitics, standard-cell design-flow allows direct and rapid

synthesis of computational blocks at RF frequencies. These trends are enabling entirely new approaches to RF circuit design that rely on digital processing to reduce analog complexity.

Higher operating frequencies have and will continue to enable new techniques in circuit design for blocks in the radio architecture. Such techniques are important to bypass current limitations in both transmitters and receivers. Higher digital integration improves the flexibility of wireless receivers, increasing the dynamic range at the front-end and enabling digital calibration techniques for front-end circuitry [3, 4]. Higher digital integration in transmitters enables new architectures that can achieve higher linearity, lower energy consumption, and more flexibility for different standards and carrier frequencies. In both cases, digital integration can increase performance while reducing cost and pushing technology towards universal configurations such as cognitive and software-defined radio [4-6].

In this work we will describe research related to more flexible and energy efficient wireless transmitters. We will discuss traditional Cartesian architectures and the advantages of polar and envelope-tracking configurations [7]. Such architectures use dynamic voltage regulation to increase average efficiency of the power amplifier (PA) across the expected operating power range. We will discuss the merits of switching and linear voltage regulators for these applications, including hybrid switching-linear topologies and issues with power supply noise in transmitter applications. Finally, we will describe the implementation of a fully-digital transmitter circuit in 90nm digital

CMOS. The transmitter is configured as an RF digital-analog converter with a class-D power amplifier output stage. The polar architecture uses a noise-shaped pulse density modulation process to control the RF carrier amplitude and an off-chip phase-modulated RF clock.

Chapter 2 discusses the fundamentals of radio transmitters including Cartesian and polar architectures. Power amplifier circuits are reviewed in the context of an average efficiency model based on the probability density function of transmit power.

Chapter 3 discusses power management techniques for RF transmitters. Switching and linear voltage regulators are reviewed for different transmitter architectures that use dynamic voltage regulation.

Chapter 4 presents an analysis of power supply noise rejection properties of linear RF amplifiers. This problem is discussed in the context of envelope-tracking transmitters. A multi-port Volterra-series formulation is used to capture the effects of supply noise mixing with the RF carrier to create near-band spectral regrowth. The results highlight circuit-level mechanisms for supply noise upconversion, including relative contribution across frequency.

Chapter 5 describes optimum operating strategies for hybrid switching-linear voltage regulators. The optimum configuration and bias points are calculated for a number of representative envelope waveforms. The proposed method, based on time-domain averaging, is shown to have substantial power savings compared to biasing based on

conventional frequency domain analysis. The proposed system implementation is shown based on an adaptive optimization of power efficiency.

Chapter 6 discusses a direct-digital-modulation RF transmitter architecture where the PA operates as a polar digital-to-RF converter. The chapter reviews basic data conversion principles including the effects of amplitude quantization and discrete-time sampling. Also reviewed are general properties of oversampled data converters, and bandpass D-A converters. Section 6.5 presents the implementation of a digital-polar transmitter for Bluetooth 2.1+ EDR operating at 2.4GHz. The system meets the performance requirements of the standard with over 30% average efficiency.

Chapter 2 Transmitter Fundamentals

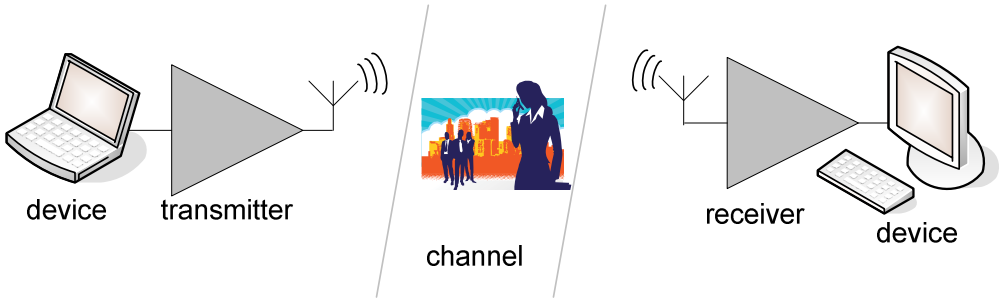


Figure 2 Wireless system: transmitter, channel, and receiver.

Modern wireless technology has opened up a vast range of possibilities for portable communication with voice and data applications dominating the space. At the heart of wireless communications hardware is the transceiver – the radio circuitry that includes both transmitter and receiver. Transceivers enable bi-directional communication between portable and fixed base-station devices, and are also the cornerstone of inter-device communication, wireless internet and cellular phones. Here, we will focus on the wireless transmitter, including basic operation, circuit implementation, and characteristics of Cartesian and polar architectures.

As shown in Figure 2, the goal of the wireless transmitter is to communicate data over a wireless channel to a receiver at a remote location. In narrowband communication systems, this requires modulating a carrier signal that is converted to an electromagnetic wave by the antenna. Conventional modulation strategies use orthogonal vectors to describe a two-dimensional space. These basis vectors are typically referred to as *in-phase, I*, and *quadrature, Q*. The RF signal trajectory is

mapped using *I(t)* and *Q(t)* baseband signals and upconverted using quadrature local oscillators:

$$v(t) = I(t)\sin(w_C t) + Q(t)\cos(w_C t), \tag{1}$$

where $I(t)$ is the in-phase vector data, $Q(t)$ is the quadrature vector data, and w_C is the RF carrier frequency.

The same RF signal trajectory can be decomposed into polar form using the amplitude and phase of the RF carrier. With a polar representation, the modulated RF signal follows:

$$v(t) = A(t)\cos\left[w_C t + \Phi(t)\right], \tag{2}$$

where *A(t)* is the amplitude of the carrier and $\Phi(t)$ is the phase of the carrier [7]. Both polar and Cartesian representations of amplitude (AM) and phase (PM) modulation suggest the phasor nature of the signal. Importantly, complex representation of the carrier signal allows many ways to encode digital information.

2.1.1 Complex Modulation

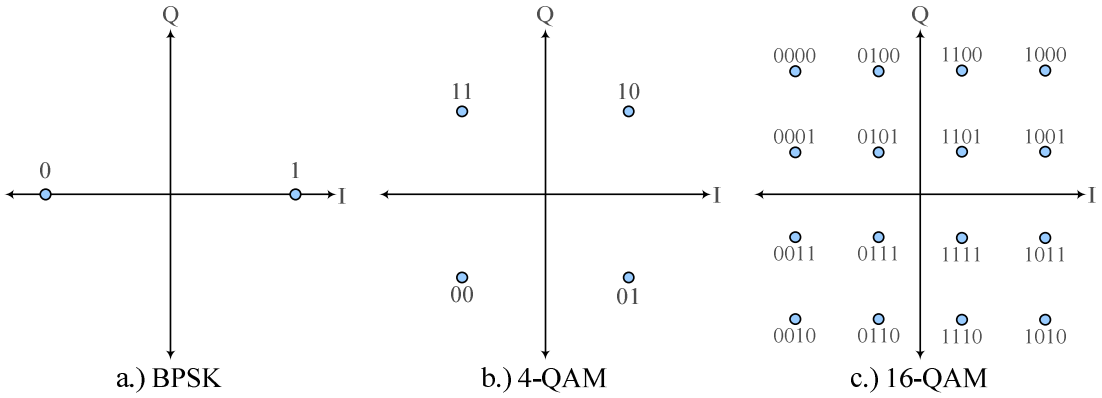


Figure 3. Symbol constellations with different numbers of bits/symbol.

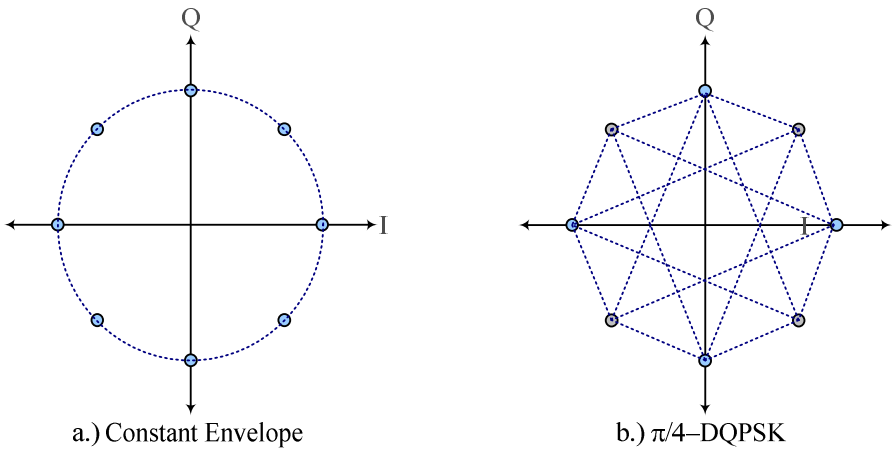


Figure 4. Complex constellation diagram and trajectory for (a) constant envelope modulation and (b) π/4DQPSK, which uses amplitude modulation for the same constellation points as (a).

Digital modulation schemes encode data in symbols which can be considered vectors with unique amplitude and phase. Each symbol can represent multiple bits of digital information, with more complex constellations representing more bits per symbol. In Figure 3(a), binary phase shift keying (BPSK) involves changing the phase of the carrier between two points 180^0 out of phase. In BPSK, only 1 bit is represented for each symbol. Higher order modulation formats have more points in the symbol constellation. Figure 3(b) shows quadrature amplitude modulation (QAM) with 4 symbol vectors. This allows two bits to be encoded for every symbol, increasing the data rate. Figure 3.c shows QAM with 16 independent symbols representing 4-bits per symbol. Higher order modulation schemes such as 16-QAM allow higher data transmission rates for a given symbol rate. This results in higher spectral efficiency, or a higher data-rate for a given amount of available spectrum [8].

It is important to note that there are many possible trajectories among the symbol points in the constellation. Figure 4(a) shows a constant envelope modulation scheme that accesses eight possible symbols, without using amplitude modulation. The same symbols can be accessed using an envelope trajectory that has amplitude modulation, as demonstrated in Figure 4(b). Here, the carrier trajectory follows π/4DQPSK modulation, a scheme that uses amplitude and phase modulation to achieve two bits per symbol. In π/4DQPSK and many other formats, amplitude modulation is used to achieve higher symbol rates for the same total spectrum utilization – achieving higher bits/s/Hz of allocated spectrum. π/4DQPSK is a common modulation format since the amplitude of the carrier does not approach zero – the trajectory avoids the origin in the constellation – and is used for the Bluetooth EDR+2.1 standard [9]. The advantage of using both amplitude and phase modulation is that the symbol rate can be increased. This is related to the fact that the distance between symbols is shorter if you cut through the center of the constellation. Another way to view the advantage of Figure 4(b) over Figure 4(a) is that for a given symbol rate, Figure 4(b) can occupy less spectrum because the amplitude of the carrier is reduced during rapid phase transitions between symbols. Constant envelope modulation schemes generally have to use lower symbol rates to keep the output spectrum within limits [8, 10].

2.1.2 Digital Modulation Limitations

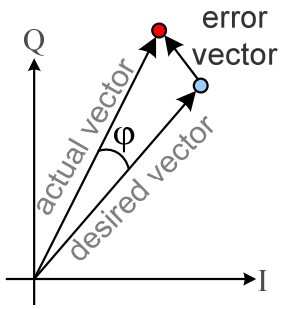


Figure 5. Error vector is the difference between the actual and ideal symbol vectors.

The tradeoff with higher order modulation schemes is that more resolution is needed to represent the symbols. In a real system, the transmitted symbol vectors will suffer from noise and distortion. Noise and distortion cause actual symbol vectors to deviate from ideal vectors. Shown in Figure 5, the discrepancy between actual and ideal symbol vectors is quantified through the error vector. A common figure of merit for fidelity of the symbol constellation is error-vector-magnitude (EVM). EVM is typically defined as a root-mean-squared quantity across a number of symbol measurements:

$$EVM = \frac{\sqrt{\frac{1}{N}\sum_{j=1}^{N}\left(V_e^2\right)}}{\left|V_m\right|}. \tag{3}$$

In (3), V_e is the magnitude of the error vector for each symbol, V_m is the magnitude of the desired symbol vector, and N is the number of measurements. The peak value for EVM may also be specified in the standard. EVM requirements vary widely depending on the standard, with the typical range falling somewhere between 3% and 35%. For 802.11a/g at 54MB/s, the rms EVM over 1000 symbols (chips) must be below 5.6% [10].

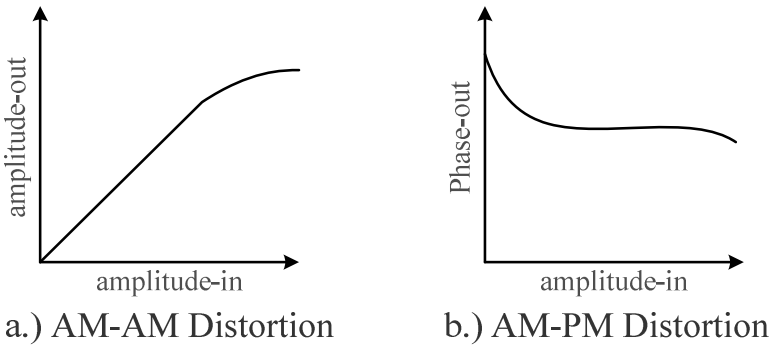


Figure 6. Typical transmitter distortion mechanisms affecting EVM.

EVM is useful to quantify the amount of noise and distortion in a transmitter. Noise will lead to random distribution of the error vectors, while distortion may cause patterns in the error vector measurements correlated with symbol amplitude and phase. In transmitters it is common to specify AM-AM (amplitude-driven amplitude) distortion and AM-PM (amplitude-driven phase) distortion, as shown in Figure 6 [11]. AM-AM distortion is caused by variation in the transmitter gain as the signal amplitude changes. A common form of AM-AM distortion is quantified through the -1dB compression point in RF amplifiers [10, 12]. Compression happens when the output amplitude is saturated and is not linearly proportional to the input amplitude. This is usually related to the voltage constraints on the active device – signal clipping occurs at the input or output terminals. AM-PM distortion results from phase shifting of the carrier correlated to the signal amplitude – this is commonly related to nonlinear capacitances in the circuit, but is sometimes caused by stray capacitive coupling in active devices [13]. This and other distortion mechanisms will be discussed in more detail later in this chapter.

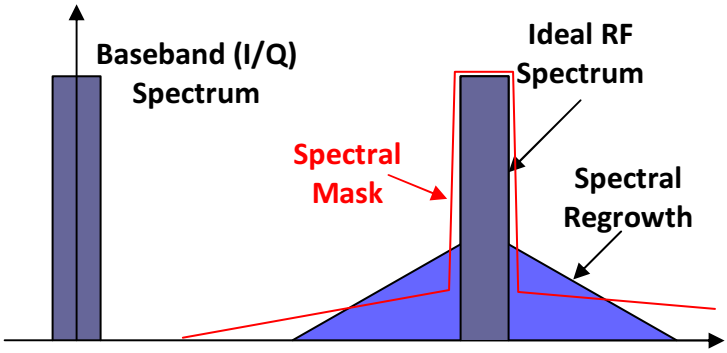


Figure 7. Transmitter output spectrum showing spectral regrowth.

Distortion will also cause undesired broadening of the output spectrum. Circuit component nonlinearity that can be quantified as AM-AM and AM-PM distortion will create spurious energy near the fundamental and harmonics of the carrier frequency. This increase in the output spectrum is commonly referred to as *spectral regrowth*. As shown in Figure 7, this can cause problems if the transmitter generates power outside the spectral mask for the standard. Spectral masks are designed for the wireless standard or by the FCC to prevent interference with adjacent channels, or with the receive channel in full-duplex systems such as WCDMA [14]. Spectral regrowth is a potentially serious problem and requires substantial attention during transmitter design. In some cases it is necessary to compensate the nonlinearities in the device using analog or digital predistortion. Predistortion attempts to invert the nonlinearities of the circuit such that the input-output behavior of the transmitter is nominally linear. Alternative distortion compensation techniques include polar and Cartesian feedback, as discussed by Dawson and Lee in [12].

2.2 Cartesian Transmitter

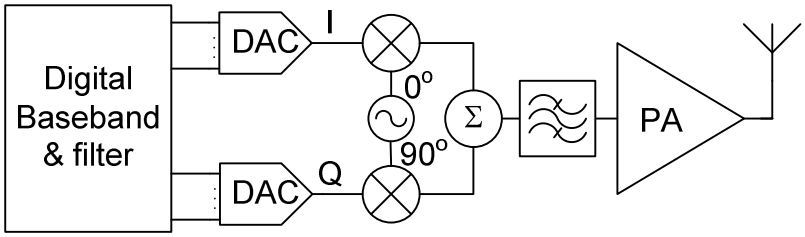


Figure 8. Direct-conversion Cartesian transmitter schematic diagram.

The Cartesian transmitter architecture is widely used in wireless systems due to simplicity – the circuit mirrors the Cartesian representation of the signal in (1). It is also popular because every block operates on ideally linear I/Q basis vectors, which simplifies the baseband representation of the symbol trajectory. Shown in Figure 8 is a direct conversion Cartesian transmitter schematic. The transmitter interfaces with a digital baseband, converting the digital representation to a modulated RF signal. The final stage of the transmitter is the power amplifier (PA), which drives the modulated RF signal into the antenna.

2.2.1 Cartesian Transmitter: General Operation and Issues

In a Cartesian architecture, the complex trajectory is encoded with *I* and *Q* basis vectors. These vectors are bandlimited with raised cosine or root-raised cosine filters in the digital baseband to constrain the output spectrum within the allocated spectral mask. A set of digital-analog converters (DACs) convert the *I* and *Q* vectors to analog signals. A quadrature mixing stage multiplies the I/Q analog representation with orthogonal (90^o out of phase) local oscillator signals. The upconverted *I* and *Q* vectors

are summed to create the modulated carrier and passed to the input of a power amplifier (PA). The PA provides power gain, driving the RF signal into the antenna which typically appears as a 50Ω resistive load.

Since the operation to convert the *I* and *Q* basis vectors to RF is ideally linear, baseband filtering is adequate to bandlimit the output RF spectrum. However, if any of the analog processes – DACs, mixers, or PA – deviate from perfect linearity, distortion can create spectral content outside of the bandlimited spectrum [14, 15]. In traditional architectures PA linearity is particularly critical since the input signal is fully modulated with amplitude and phase information. Chapter 5 will discuss PA linearity in more detail from power series and Volterra series perspectives. Other references that discuss PA linearity in great detail include Wambaq and Sansen, [15], Vuolevi, [16], and Cripps, [11].

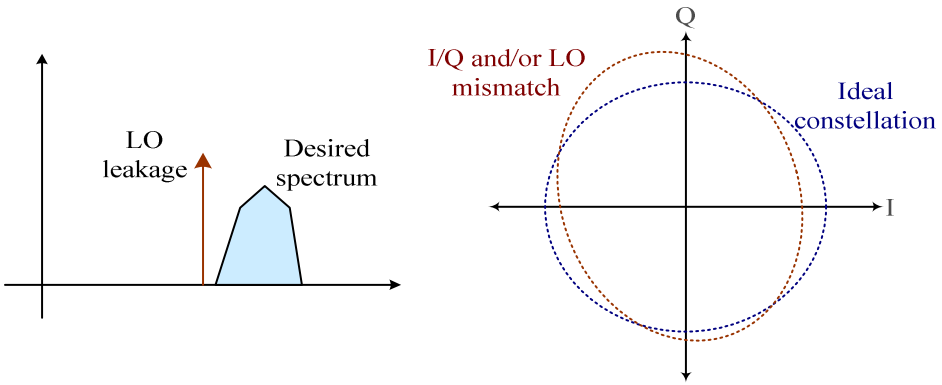


Figure 9. Effects of I/Q and quadrature LO gain and phase imbalance.

Other issues with Cartesian transmitters include LO leakage, LO pulling, and imbalance of the quadrature LO signals. Shown in Figure 9(a), LO leakage appears as a spurious tone at the carrier frequency that is caused by amplitude or phase mismatch in the I/Q path or quadrature LO signals [14]. Imbalance of the quadrature LO signals will

have an effect similar to mismatch of the I and Q signal paths. The effect can be visualized as in Figure 9(b) as deforming the constellation diagram. In Figure 9(b), LO leakage occurs if the origin or average value of the constellation deviates from (0,0). These effects can be minimized with careful design and layout of the mixers and quadrature LO synthesizer. It may also be possible to calibrate LO leakage by adding DC offsets to the I or Q baseband signals. This technique is discussed in [17] and is now commonly used in Cartesian transmitter design.

LO pulling is another common problem, especially in direct conversion architectures. This can happen if the voltage-controlled oscillator (VCO) generating the LO signals operates at the same frequency as the PA. The PA can generate substantial noise on the power supply and silicon substrate that can couple back into the VCO, causing injection locking. LO pulling is alleviated by operating the VCO at a different frequency from the LO and designing the VCO to have low voltage sensitivity, such that small noise signals have less effect on the LO output [18].

2.3 Polar Transmitters

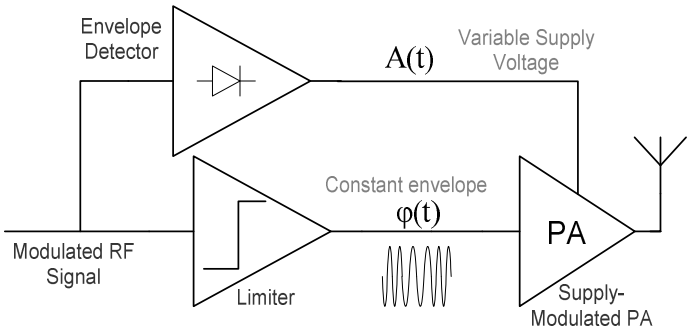


Figure 10. Kahn envelope elimination and restoration (EER) transmitter architecture [19].

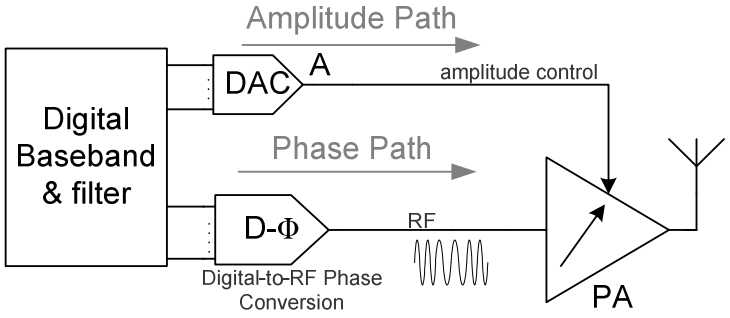


Figure 11. General representation of the polar transmitter architecture.

Polar transmitters differ from Cartesian transmitters in that the data is encoded in terms of amplitude and phase instead of Cartesian *I* and *Q*. The polar representation is mathematically straightforward to convert from the Cartesian representation as

$$A(t) = \sqrt{I(t)^2 + Q(t)^2}\text{, and} \tag{4}$$

$$\phi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right), \tag{5}$$

where *A(t)* and $\phi(t)$ are the polar amplitude and phase time-domain signals.

A major difference between the polar and Cartesian representations is that the polar basis vectors, amplitude and phase, have widely differing spectral properties compared to the I/Q basis vectors and the modulated RF output. This is clear in (4) and (5) as *A* and ϕ are derived from *I* and *Q* through nonlinear operations. Nonlinearities in (4) and (5) cause the polar basis vectors to lose the bandlimited property of the Cartesian *I/Q* representation. To design the system for high integrity – low EVM and high spectral fidelity – the wideband nature of the amplitude and phase paths has to be considered in

architecture and circuit-level design. This issue will recur throughout the discussion of polar systems.

2.3.1 Polar Implementations

The Kahn envelope elimination and restoration (EER) technique is an early example of polar modulation where the amplitude and phase are extracted directly from the modulated RF signal [19]. In the Kahn technique, shown in Figure 10, a limiter extracts the zero crossings of the RF signal, converting the PA input to a constant envelope signal while preserving phase information. The amplitude information is extracted with an envelope detector. The PA in a Kahn-type system is designed such that the envelope of the output signal is directly proportional to the supply voltage. This is the case for a range of nonlinear classes of PA, including class-C, D, E, and F [7], as will be discussed in further chapters. The amplitude information is *'restored'* to the envelope of the transmitted signal by modulating the supply voltage of the PA, leading to the EER distinction. A more recent example of this technique was presented by Raab in [20]. The Kahn technique continues to be the basis of many of the modern polar architectures, including [13, 21-25].

Figure 11 shows a generalized version of the polar architecture highlighting the wide variety of systems that could fit the polar distinction. In Figure 11, the PA is shown as a variable-gain amplifier (VGA). In the general case, any signal which modulates the amplitude of the carrier can effectively be used in a polar system. Traditional systems

use the power supply to control the amplitude of a nonlinear PA, as in [19-21]. However, other possibilities exist. An example of a polar system that does not use supply modulation will be discussed in Chapter 6.

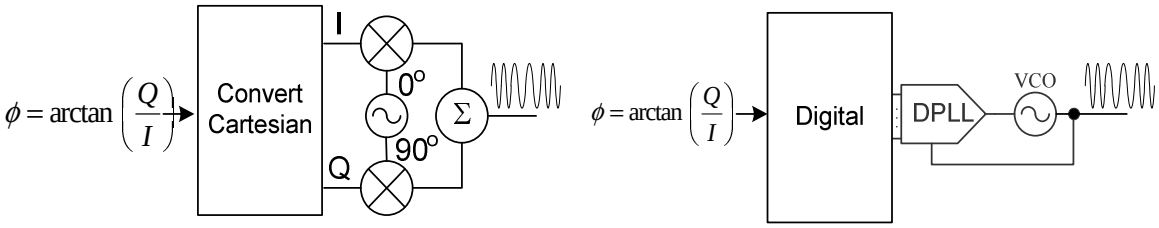


Figure 12. Phase-path circuit architectures: representative techniques

There are many ways to conceive of the phase path in a polar system. As shown in Figure 11, the goal is to convert a digital representation of the baseband phase signal to a phase-modulated RF carrier. One possibility is to use conventional Cartesian upconversion following the expression in (5). The polar phase signal is represented using I/Q basis vectors and converted to a constant envelope. The upconversion stage would be analogous to a traditional Cartesian transmitter with a constant envelope signal, as in Figure 12(a). Another possibility is to exploit developments in phase-locked-loop (PLL) or digital phase-locked-loop (DPLL) techniques, as in Figure 12(b). Such techniques permit direct synthesis of constant envelope phase-modulated RF signals, and are well matched to the requirements of polar architectures. The work of Staszewski in [26], among others, opens the range of possibilities for such techniques.

2.3.2 Issues in Polar Systems

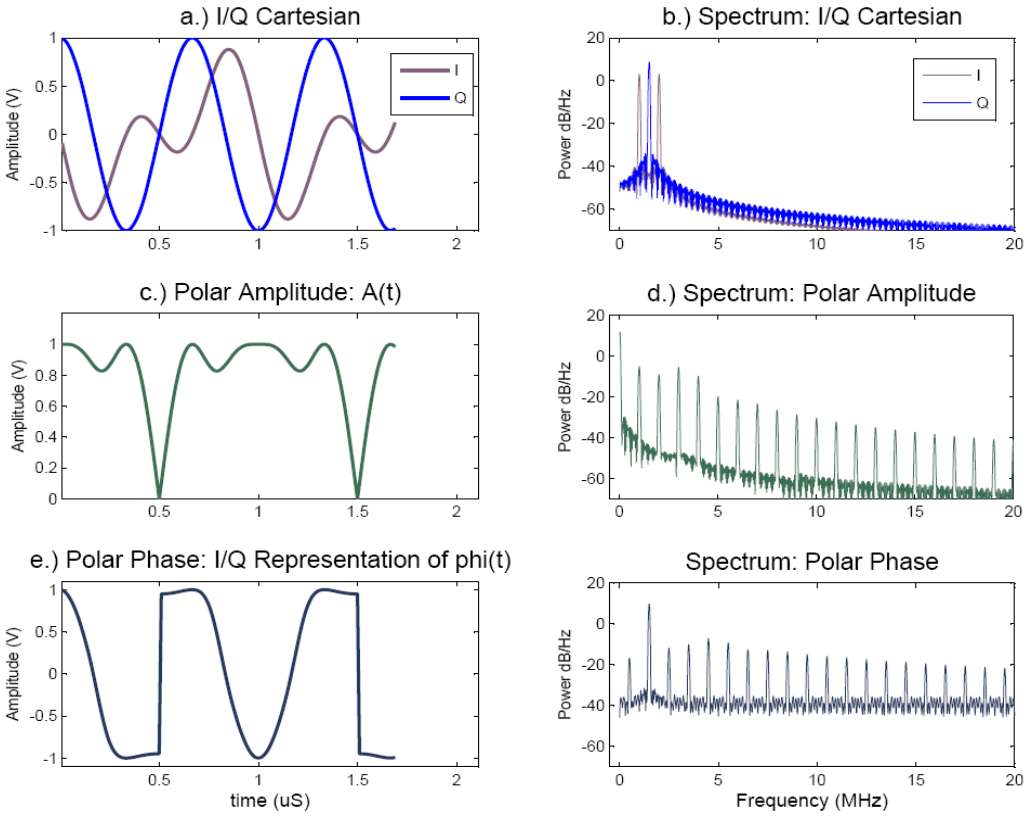


Figure 13. Time- and frequency-domain waveform comparison: Cartesian and polar systems. Baseband I/Q waveform with two-tone zero mean sinusoid.

Polar systems are difficult to design for a number of reasons. The first is the wideband nature of polar amplitude and phase signals. Shown in Figure 13, a Cartesian representation with a simple bandlimited spectrum may have wideband spectral content with an equivalent polar representation. Figure 13(a) shows the time-domain waveform of a Cartesian baseband signal defined as

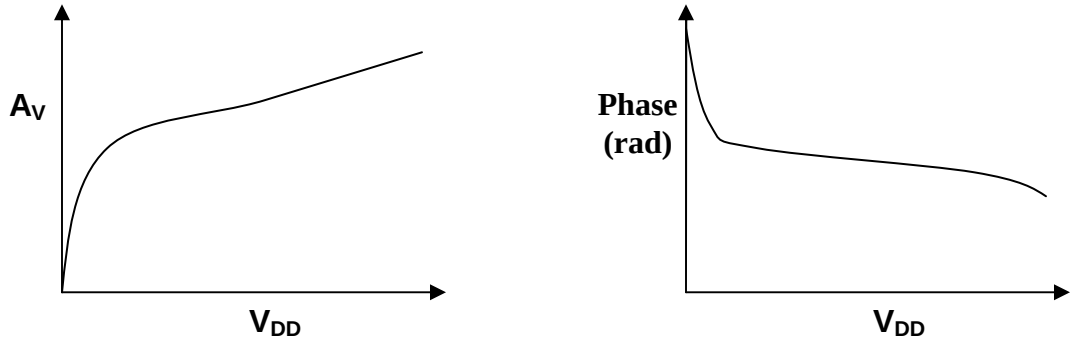
$$I(t) = \frac{1}{2}\sin(2\pi f_R t) + \frac{1}{2}\sin(4\pi f_R t) \qquad (6)$$
$$Q(t) = \cos(3\pi f_R t)$$

where f_R is 1.0 MHz. The waveforms in (6) define a baseband spectrum with three tones in the positive frequency axis. As shown in Figure 13(b), the power spectrum for the

Cartesian baseband representation is bandlimited to only the tones at 1 MHz, 1.5 MHz, and 2 MHz.

Contrasting with the Cartesian signals, the polar signals in Figure 13(b-f) show wideband frequency behavior. The amplitude signal is full-wave rectified since the envelope can never be negative. This leads to high-frequency transitions as the signal approaches zero. Capturing the full time-domain amplitude signal would require theoretically infinite frequency response, as shown in Figure 13(d). The phase signal also requires nearly infinite frequency response as shown in Figure 13(f). Here, the phase information is represented as a Cartesian I/Q channel vector, as in the architecture in Figure 12(a). The high bandwidth of the phase signal is partly related to the sharp discontinuities in phase when the constellation trajectory crosses through the origin. When this happens the phase may shift by 180^0 to capture the polarity shift of the RF carrier. In a Cartesian system, these phase inversions happen when the amplitude of the carrier is zero. However, when the Cartesian representation of the phase signal is normalized to constant envelope, phase transitions happen at full amplitude, requiring high slew rate in the phase modulator circuit.

The wideband nature of the polar representation drives the need for high-bandwidth circuit design for the amplitude and phase modulators. As will be seen in the following chapter, this is especially difficult for the amplitude path in dynamic supply architectures. In some systems, the power supply may need tracking bandwidths in excess of 10MHz to avoid degradation of EVM below system requirements [27, 28].



a.) PA voltage gain vs V_{DD} b.) Phase of RF carrier vs V_{DD}

Figure 14. Distortion mechanisms in polar systems: gain and phase vs supply voltage

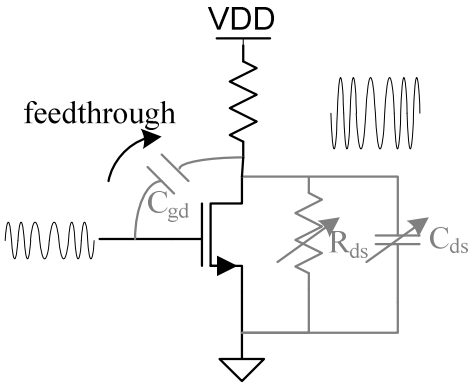


Figure 15. Common-source amplifier circuit showing mechanisms for AM-AM, AM-PM distortion

Another major issue for polar systems is distortion. In Cartesian transmitters, the PA operates with a fixed supply voltage and is only subject to the normal input-output nonlinear characteristics as discussed in detail in [15, 16]. In supply-modulated polar systems, the PA is also subject to the effects of the supply voltage on linearity. Shown in Figure 14(a), the gain of the PA may change as supply voltage varies. In some cases, particularly with short-channel CMOS devices, voltage gain is a strong function of the average drain-source potential. Figure 15 is a simplified model of a common source amplifier showing several important parasitic components. The curve in Figure 14(a)

represents a CMOS PA that may exhibit gain expansion, resulting in AM-AM distortion in the output signal [13]. Gain expansion in a CMOS common-source amplifier may be caused by increased output resistance and transconductance as a function of V_{DS}.

Figure 14(b), shows the effects of supply voltage on the phase of the RF carrier. Many active devices have voltage-dependent capacitances resulting from semiconductor junctions. The supply voltage can change the bias conditions on these parasitic varactors causing a phase shift dependent on the overall output impedance. At low supply voltages, additional AM-PM distortion may be caused by feedthrough of the PA input signal to the output, potentially through gate-drain capacitance. This is especially problematic if the phase-path signal is constant envelope – input power can leak directly to the output, pulling the phase by as much as 180^0 [13]. The phase signal can also leak through directly to the output of the PA, both through parasitic C_{gd}, and directly if there is DC offset in the amplitude path signal [7]. This is problematic because the wideband spectrum shown in Figure 13(f) can appear at the PA output, corrupting the output spectrum.

Another major issue with polar systems is noise susceptibility, especially related to the power supply. Efficient voltage regulators often use switching processes to convert voltage levels with passive energy storage components. In supply-modulated PA systems, residual switching noise can affect the performance of the PA. Specifically, supply noise can mix with the RF carrier and be upconverted into the RF spectrum, near RF carrier [29, 30]. This can be a problem if the noise is large enough to violate the

spectral mask, or affect EVM performance. Chapter 4 describes this problem in detail, including analysis techniques and methods to reduce supply noise sensitivity.

2.4 Power and Energy Efficiency: Polar and Cartesian Architectures

After EVM and spectral mask performance, power efficiency is the most important specification for wireless transmitters. In most portable applications the transmitter is the highest power consuming block in the system because of the high power requirements of the PA. Since power levels in wireless transmitters tend to be highly variable, *energy efficiency* tends to be a better metric of performance than *power efficiency*. Energy efficiency can be captured by quantifying the *average efficiency* of the transmitter, which is be calculated as

$$\eta_{avg} = \frac{E_{load}}{E_{supply}}, \tag{7}$$

where E_{load} is the energy delivered to the load and E_{supply} is the energy drawn from the supply. Because (7) is calculated across a time period that represents normal use of the device, it is closely related to the battery life of the portable system.

2.4.1 Typical Use Patterns: Probability Density Function (PDF) of Transmit Power

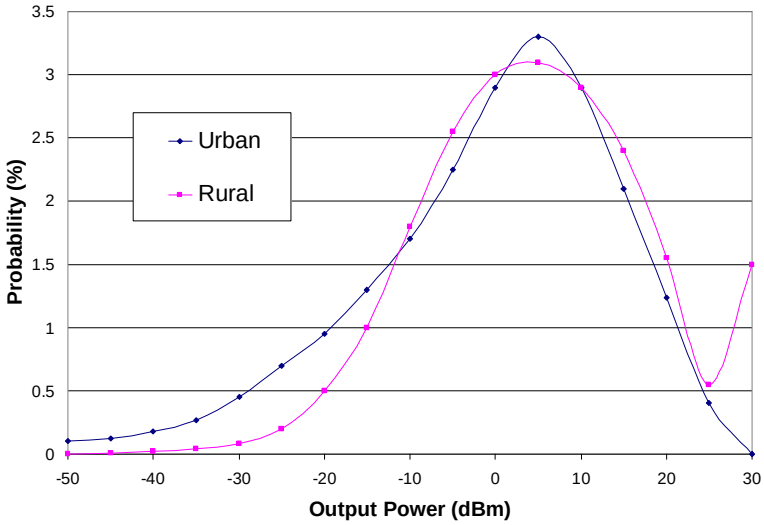


Figure 16. Representative probability distribution function (PDF) for CDMA applications [31].

In most portable communications applications, transmitters are rarely used at maximum power. In cellular systems, the transmitter power level is continuously adjusted depending on the proximity of the handset to the basestation. This is done for two reasons: to save power in the portable unit, and to prevent transmitters from interfering with each other in crowded spectrum. The second reason is known as the near-far effect and is a common problem in multiple-access wireless systems [31].

Figure 16 shows the probability of transmitting at a given output power for a CDMA system for urban and rural environments. The maximum power is 30dBm, or one watt, but the average power is closer to 5-10dBm or around 10mW. Clearly, a transmitter that is efficient only at maximum power may not be effective in a realistic environment. The average efficiency of the transmitter can be calculated using the PDF:

$$\eta_{avg} = \frac{\int_{-\infty}^{\infty} g(P_L) \cdot P_L \, dP_L}{\int_{-\infty}^{\infty} g(P_L) \cdot P_{supply}(P_L) dP_L}, \tag{8}$$

where P_L is the power delivered to the load (x-axis in Figure 16), $g(P_L)$ is the probability density function, and $P_{\sup ply}(P_L)$ is the power drawn from the supply as a function of P_L. A transmitter designed for high average efficiency will have better battery life than if average efficiency is not taken into account.

2.5 Power amplifier overview: general operation and power efficiency

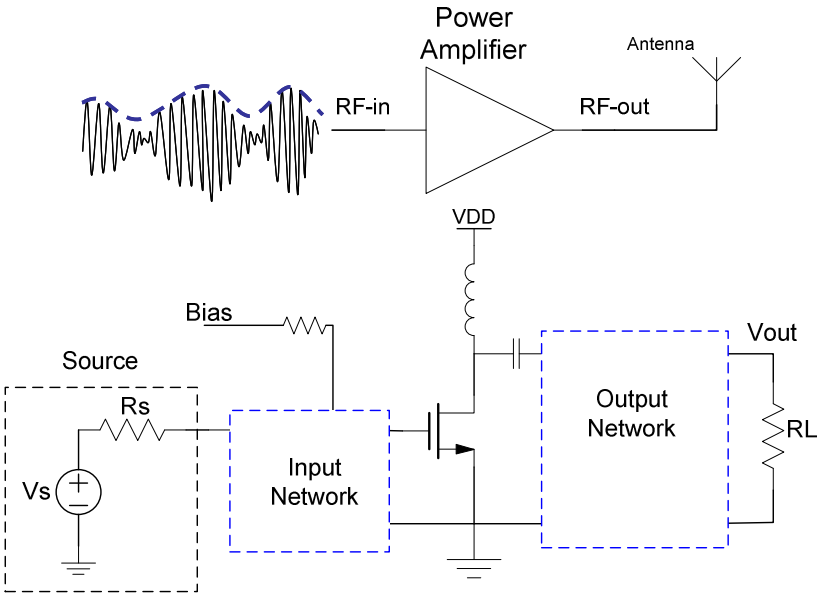


Figure 17. Power amplifier block diagram and schematic for a CMOS common-source PA

The power amplifier (PA) is the last stage in the transmitter and drives the modulated RF signal into the antenna. Efficiency is a critical specification since the PA may operate

at substantially higher power than other blocks in the system. Other critical specifications for the PA include *output power*, *power gain*, and *linearity*. This work is not meant to be a treatise on power amplifier issues and design. There are many great references on the subject including the work of Raab, [20, 32], Cripps, [11, 32], Kee, Aoki, et al, [33, 34], Reynaert and Steyaert, [7], general texts including [10, 35], and this author's own masters thesis, [36]. Instead, this section will provide a brief overview of the linear and nonlinear classes of PA, relative efficiency performance, and will motivate supply modulation in polar architectures.

2.5.1 Power Amplifier Operation

Figure 17 shows a schematic representation of a general CMOS power amplifier. We will use the notation and terminology for silicon CMOS devices, but the active device in Figure 17 could as well be implemented in BiPolar or SiGe BiPolar, or III-V semiconductor technology including GaAs, GaN, InP Mesfet or HBT devices.

The general power amplifier is configured with an input matching network and an output impedance transformation network. The input network assists in impedance matching the PA input to the previous stage, which in a Cartesian transmitter is the quadrature-mixer stage. Impedance matching improves power transfer of the RF signal into the PA, helping the transmitter achieve the required power gain [37]. The output impedance matching network transforms the load impedance, generally through

resonant structures, helping the PA meet the required output power for a fixed supply voltage [10].

Impedance matching at the PA input is conventional and is not discussed in great detail in PA literature. Impedance transformation at the output, on the other hand, is nontrivial and warrants a great deal of consideration. Lumped impedance transformation networks include L-matching networks and tapped capacitor transformers [7, 10]. Resonant transformation networks are generally limited by losses in the passive components and may only be useful at low conversion ratios. Other works use power combining to sum the outputs of multiple amplifiers achieving higher power levels with constrained supply voltage in CMOS technologies. Aoki et al. in [33] present seminal work on integrated transformer structures that use symmetry to combine the power of multiple differential-CMOS PAs, achieving high efficiency and high integration. Liu et al. present similar magnetic transformers that allow PA stages to turn off at lower power levels, improving maximum output power and average efficiency [38, 39].

2.5.2 Linear Power Amplifiers: Class AB

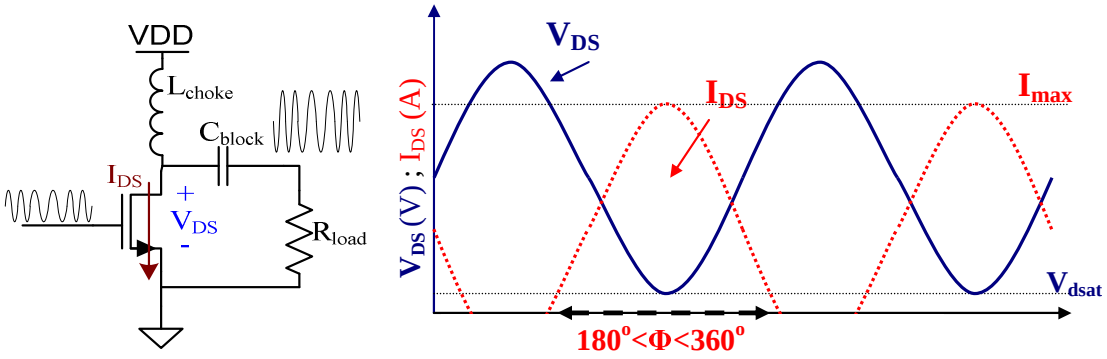


Figure 18. Class-AB PA voltage and current waveforms

There are many classes of power amplifier, distinguished by the mode of operation of the active device, the current conduction angle, and the topology of resonant network at the output. Classes A, AB, B, are considered *linear* power amplifiers, since the amplitude of the output signal is proportional to the amplitude of the input signal. Classes C, D, E, and F are considered *nonlinear* since input-output amplitude linearity is not inherent, or it is not possible to modulate the output amplitude from the input terminal. Here we will describe the general operation of class AB to give a sense of the tradeoffs inherent in PA design.

Figure 18 shows the voltage and current waveforms for the class AB PA. The active device operates as a current source, but conducts only a fraction of the full cycle – it is 'on' between 50% and 100% of the time. Traditional class AB PAs, especially in audio applications, tend to use push-pull source follower output stages [40]. At higher frequencies it is more efficient to use a single device with a pull-up inductor, L_{choke} in Figure 18. The resonant network filters unwanted output harmonics such that the drain

voltage is approximately sinusoidal. The conduction angle, or angular fraction of the full period that the device is conducting, is between 360^0 (the limiting case for class A) and 180^0 (the limiting case for class B). The device dissipates power when I_{DS} and V_{DS} overlap, as $P_{loss} = I_{DS} \cdot V_{DS}$. A common metric for power amplifier efficiency is the drain efficiency:

$$\eta_{drain} = \frac{P_L}{P_{\sup ply}}, \tag{9}$$

where P_L is the power delivered to the load and P_{supply} is the power drawn from the supply. Drain efficiency neglects the power required to drive the input of the PA, but is a useful figure of merit for the various PA classes.

The drain efficiency of class AB amplifiers is a function of the conduction angle, Φ, and the voltage swing at the drain, normalized to V_{DD} :

$$\eta_{drain} = K\frac{\hat{v}_o}{V_{DD}}, \text{ where}$$
$$K = \frac{\Phi - \sin\Phi}{4\left(\sin\frac{\Phi}{2} - \frac{\Phi}{2}\cos\frac{\Phi}{2}\right)} \tag{10}$$

where Φ is the conduction angle as defined in Figure 18, $\hat{v}_o$ is the signal amplitude at the drain of the active device, and η_{drain} is PA drain efficiency [10].

The limiting cases of efficiency for the class AB PA are the same as class A and class B operation. The minimum efficiency of 50% happens in the class A limiting case when $\Phi = 360^0$ and $\hat{v}_o = V_{DD}$. The maximum efficiency of 78.5% happens when $\Phi = 180^0$

and $\hat{v}_o = V_{DD}$. The relationship in (10) also holds for class C PAs. In the class C case, as the conduction angle, Φ, approaches zero, efficiency approaches 100% (unfortunately, output power approaches zero as Φ approaches zero). It should be noted that the efficiencies described here are based on are purely ideal circumstances using the current-voltage waveforms in the device and do not include any losses from passive components. Also, in (10), it is important to note that efficiency is linear with the signal amplitude – if the signal swing at the drain of the device is reduced, efficiency will also be reduced. We will revisit the concept of efficiency at less than maximum output power later in this chapter.

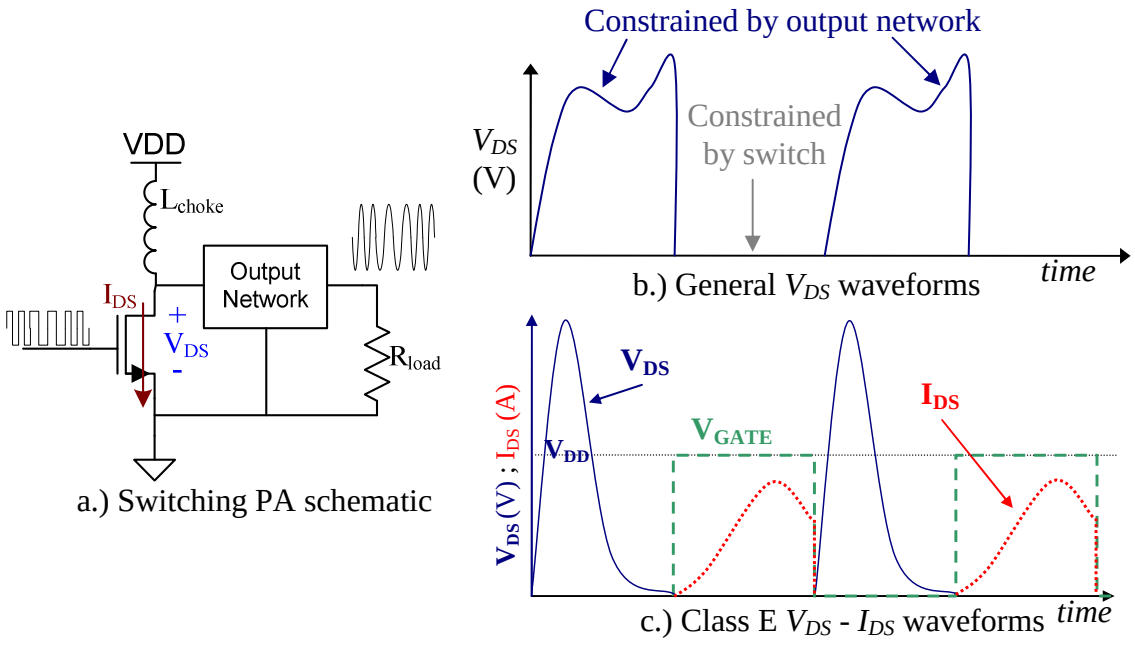


Figure 19. Switching PA schematic and time-domain waveforms

2.5.3 Switching Power Amplifiers: Class E example

Switching power amplifiers can achieve higher efficiency than linear amplifiers because the active device operates as a switch. The active device is usually driven hard enough that it operates as a resistor in the 'on' state and conducts no current in the 'off' state. With properly constrained voltage and current waveforms, switching amplifiers can achieve high output power with 100% ideal efficiency. Unfortunately this usually means that switching PAs forego the linear input-output characteristics of linear PAs and have historically been used mainly for constant envelope modulation schemes.

Figure 19(a) shows a schematic representation for a CMOS switching PA. The device is configured similarly to the linear PA device, except that the gate signal drives the device between triode and cutoff regimes. Shown in Figure 19(b), when the device is 'on,' the drain-source voltage is constrained to near zero. When the device is 'off,' the drain-source voltage is constrained by the dynamics of the output network. The output network is designed to minimize power loss by preventing overlapping V_{DS} and I_{DS} waveforms. Ideally, the active device turns on when the drain-source voltage is zero, achieving zero voltage switching (ZVS). This reduces power loss in the system by minimizing the loss incurred from switching the drain capacitance of the active device.

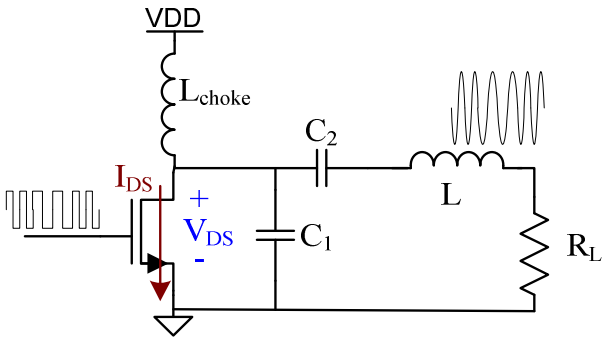


Figure 20. Class E PA schematic

Class E PAs achieve both zero voltage switching and non-overlapping V_{DS} – I_{DS} characteristics. The class E concept has been used for a range of applications including RF power amplifiers, [25, 41, 42], and resonant power converters, [41, 43]. Shown in Figure 19 (c), the drain-source voltage is approximately zero when the device turns on. Figure 20 shows a schematic representation for a typical CMOS class E PA, as in [42]. C_2 and L are physical lumped passive components that may be integrated at the device or board level. C_1 generally includes the parasitic drain-source capacitance of the active device.

There are many methods to design the output network for a class E amplifier, some of which are outlined in [7, 10, 41]. The network is generally designed in the time-domain such that the voltage and current waveforms fit the characteristic trajectories shown in Figure 19 (c). The time-domain response of the output network when the switch is opened should be such that the drain voltage reaches zero with zero first derivative in one half switching cycle. In the original paper by Sokal, [41], this condition results in the following expressions for the passive network:

$$L = \frac{\pi(\pi^2 - 4)}{16}\frac{R_L}{w_c} \approx 1.1525\frac{R_L}{w_c}, \tag{11}$$

$$C_1 = \frac{8}{\pi(\pi^2 + 4)}\frac{1}{w_c R_L} \approx 0.1836\frac{1}{w_c R_L}, \tag{12}$$

$$P_L = \frac{8}{\pi^2 + 4}\frac{V_{DD}^2}{R_L} \approx 0.5768\frac{V_{DD}^2}{R_L}, \tag{13}$$

where w_c is the carrier frequency, L, C_1, and R_L are as defined in Figure 20, and P_L is the power delivered to the load.

A drawback with the class E topology is that the drain-source voltage exceeds the supply voltage by a substantial margin. In the nominal case, $V_{DS\max} \approx 3.56 \cdot V_{DD}$. This can be problematic if the device is susceptible to high-voltage breakdown. In CMOS technology oxide breakdown can be a major issue limiting the lifetime of the active device. The high peak voltage swing turns out to be a serious issue with the class E design limiting the maximum power the amplifier can deliver relative to the supply voltage.

	class A	class B	class E
Peak Efficiency	50%	78.50%	100%
Supply constrained output power (W) (V_{DD}=1V, R_L=1Ω)	500mW	500mW	577mW
Breakdown constrained output power (W) (V_{DSmax}=2V, R_L=1Ω)	500mW	500mW	182mW

Table I. Comparison of power amplifier performance

Table I. shows the performance of class A and class B PAs compared to class E. For the same supply voltage, class E is both more efficient and has higher output power than class A and class B. However, given the breakdown constraint of the active device, class E may operate with a lower V_{DD} than linear topologies, significantly reducing output power. The breakdown problem is somewhat alleviated under zero-current conditions due to reduction of hot-carrier effects. Since class E achieves peak voltage stress at nominally zero current, the amplifier to can potentially operate with voltage

peaking 2-3 times the nominal supply voltage for certain CMOS technologies [7]. However, the robustness of CMOS class-E amplifiers with high peak voltage stress is questionable, especially when subjected to load-pull – variation in the impedance of the output network usually related to varying operating conditions of the antenna.

2.5.4 Efficiency in Power Backoff

As mentioned in section 2.4.1, transmitters rarely operate at maximum power, but are subject to a wide dynamic range of operation that is characterized by a probability density function. Average efficiency is a more accurate indicator of battery life and can be used to quantify the performance of a given power amplifier.

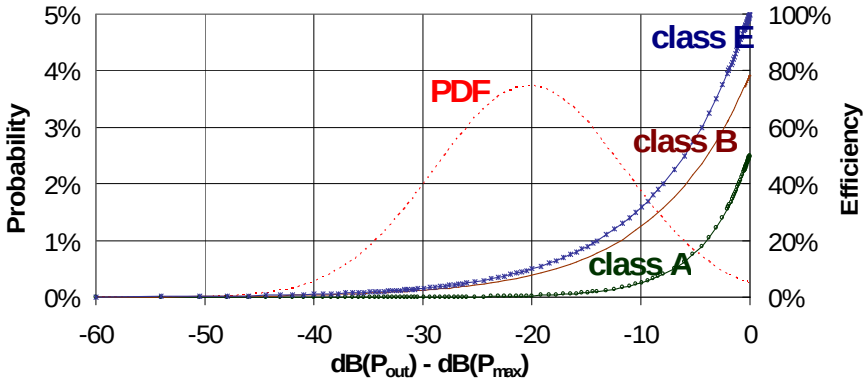


Figure 21. Power amplifier efficiency in power backoff overlaid with a representative PDF

PA Class:	Class A	Class B	Class E
Average Efficiency:	0.78%* / 9.2%**	14.46%	18.21%

Table II. Average efficiency calculations for the curves in Figure 21
*constant bias current
**variable bias current

Figure 21 shows the ideal drain efficiency of class A, class B, and class E PAs across output power. The power range is normalized to the maximum power as limited by the supply voltage. The class E efficiency curve assumes that the class E power level is modulated by resistively lowering the supply voltage (through use of a linear regulator – this concept is discussed in more detail in the next chapter). A representative PDF is overlaid with the efficiency curves. In this example, the mean operating power is 20dB below the peak power. At the mean power level, all power amplifier classes are less than 10% efficient.

The expression in (8) is used to calculate average efficiency, based on the PDF. The results of the average efficiency calculation for the curves in Figure 21 are shown in Table II. Average efficiency is significantly lower than the peak efficiency in all cases. For the class B and class E amplifiers, average efficiency is more than a factor of five less than peak efficiency. For the class A amplifier with constant bias current, it is close to a factor of fifty. The calculations in Table II are for the purely ideal case without parasitic losses. If additional loss mechanisms are included, both peak and average efficiency are substantially worse.

The following chapter will skip back to previous issues and highlight more directly the techniques in power management that may be used to improve average efficiency. Specifically, we will discuss supply-modulated polar architectures as a way to improve average efficiency of wireless transmitters. We will show that dynamic voltage

regulation can keep PA efficiency near the ideal limit, improving average efficiency substantially. This will motivate the later work in chapters 4 and 5 which describe contributions to the area of dynamic supply transmitter architectures. Chapter 6 will describe an alternative to such architectures that circumvents many of the problems associated with polar systems presented in this chapter.

Chapter 3 Power Management for RF Transmitters and Polar Systems

Power management is an increasingly important issue in highly integrated wireless systems. With scaling semiconductor technology, power density has become a major constraint on system performance [1, 44]. Heat and interconnect parasitics may limit total current levels in many systems. Transmitter and processor power levels are also constrained by battery capacity in portable systems, requiring intelligent use of available energy. Historically, power management has been a valuable tool to reduce system current consumption and to exploit tradeoffs in system power versus performance in a range of semiconductor applications [45, 46]. The same is true within the scope of wireless systems, especially as related to the power amplifier (PA), which can benefit from accurate, efficient voltage regulation strategies.

Wireless transmitters and especially power amplifiers have specific and potentially stringent power supply requirements. This chapter will describe two transmitter architectures, based on polar systems, which benefit greatly from dynamic regulation of the PA supply voltage. We will discuss different topologies for the voltage regulator, including switching DC-DC converters and linear regulators. The goal of this chapter is to introduce the issues and tradeoffs of these topologies so that the following chapters,

which provide detail on power supply rejection and hybrid voltage regulators, are put in proper context for the discussion.

3.1 Motivation: Efficiency

As outlined in Chapter 2, power amplifiers operate with a wide range of output power that can be quantified through the probability density function. Considering that average power levels may be substantially below peak power levels, *average* or *energy efficiency* is calculated based on the operating statistics in the PDF. With traditional architectures, where the PA operates with a fixed supply voltage and the power level is only controlled by the signal applied to the gate of the active device, average efficiency may be substantially less than peak efficiency. Such architectures require a linear PA to amplify the high dynamic range input signal to the output. In section 2.3 we described how nonlinear PAs can amplify linear signals using polar architectures and techniques such as Kahn EER, shown in Figure 10. However, both linear and switching amplifiers can benefit significantly from efficient regulation of the supply voltage.

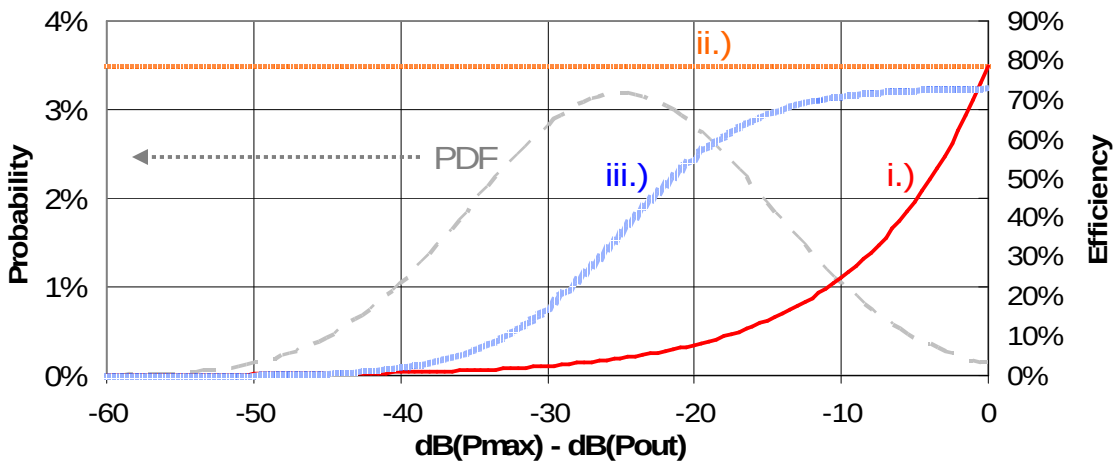


Figure 22. Efficiency versus output power: i.) conventional class B PA, ii.) class B PA with dynamic supply regulation, iii.) class B PA, dynamic VDD with realistic loss mechanisms.

Figure 22 compares the efficiency of an ideal class B PA with and without dynamic supply regulation. The power scale (x-axis) is normalized to peak power, where the class B PA achieves maximum efficiency of $\pi/4$, or 78.5%. As power is reduced, the class B efficiency falls linearly with the voltage amplitude of the RF carrier signal. Curve *i.)* is for the traditional case where the supply voltage, V_{DD}, is fixed. Curves *ii.)* and *iii.)* highlight the scenario where the supply voltage is reduced such that the PA operates always at the threshold of compression. If the carrier amplitude is time-varying, as it would be for standards that use amplitude modulation to map out the signal constellation (e.g. the $\pi/4$DQPSK constellation in Figure 4, or other standards including QAM, ASK, or many forms of PSK), then the supply voltage changes dynamically to follow the carrier amplitude or envelope.

Curve iii.) considers the actual loss mechanisms that occur because of the supply modulator – the details of the supply modulator will be discussed in detail later in this

chapter. Overall, Figure 22 shows that dynamic voltage regulation strategies maintain higher efficiency across the power range, especially at low power, where the PA is most likely to operate based on the PDF. For curve *iii.)*, average efficiency is 62.5% compared to 14.4% in curve *i.)*. This is an increase of more than 400% in average efficiency. With the potential to dramatically improve battery life such techniques motivate new circuit architectures to achieve higher efficiency.

3.1.1 Envelope Tracking System

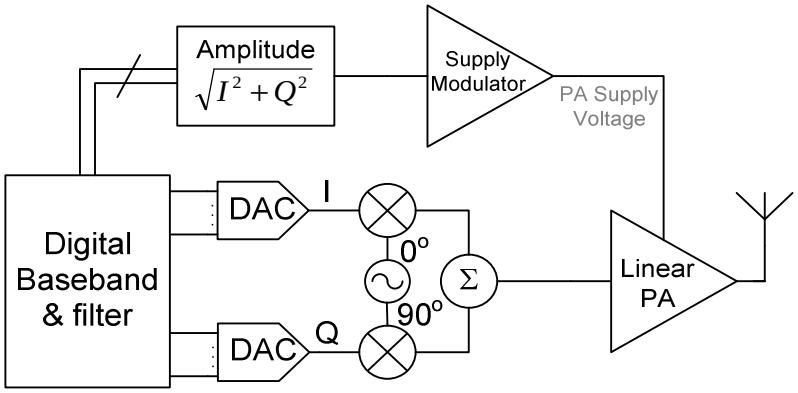
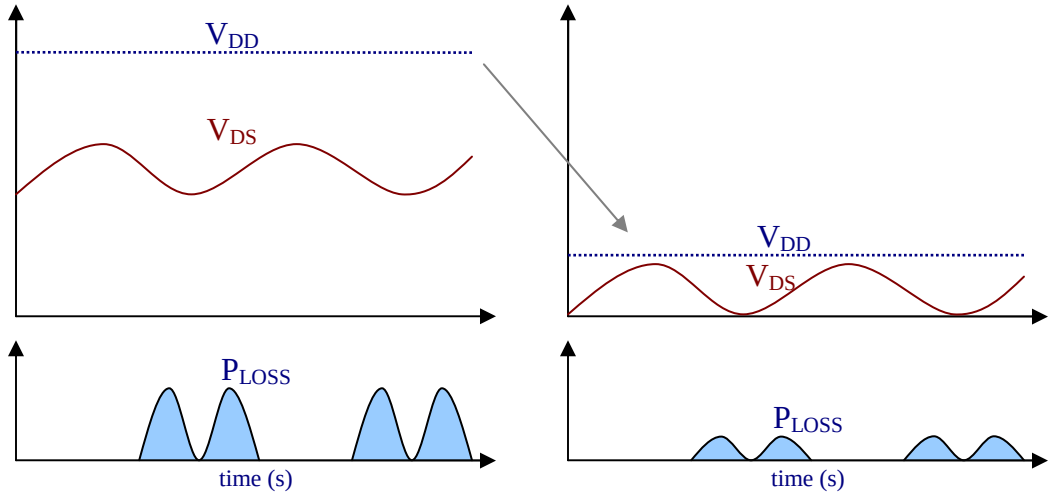


Figure 23. Envelope tracking transmitter using traditional Cartesian architecture with a dynamic supply modulator to improve average efficiency.



a.) Fixed V_{DD}, low amplitude class B b.) Dynamic V_{DD}, low amplitude class B

Figure 24. Time domain waveforms for V_{DS} RF carrier waveform and power loss: fixed V_{DD} and dynamic V_{DD}.

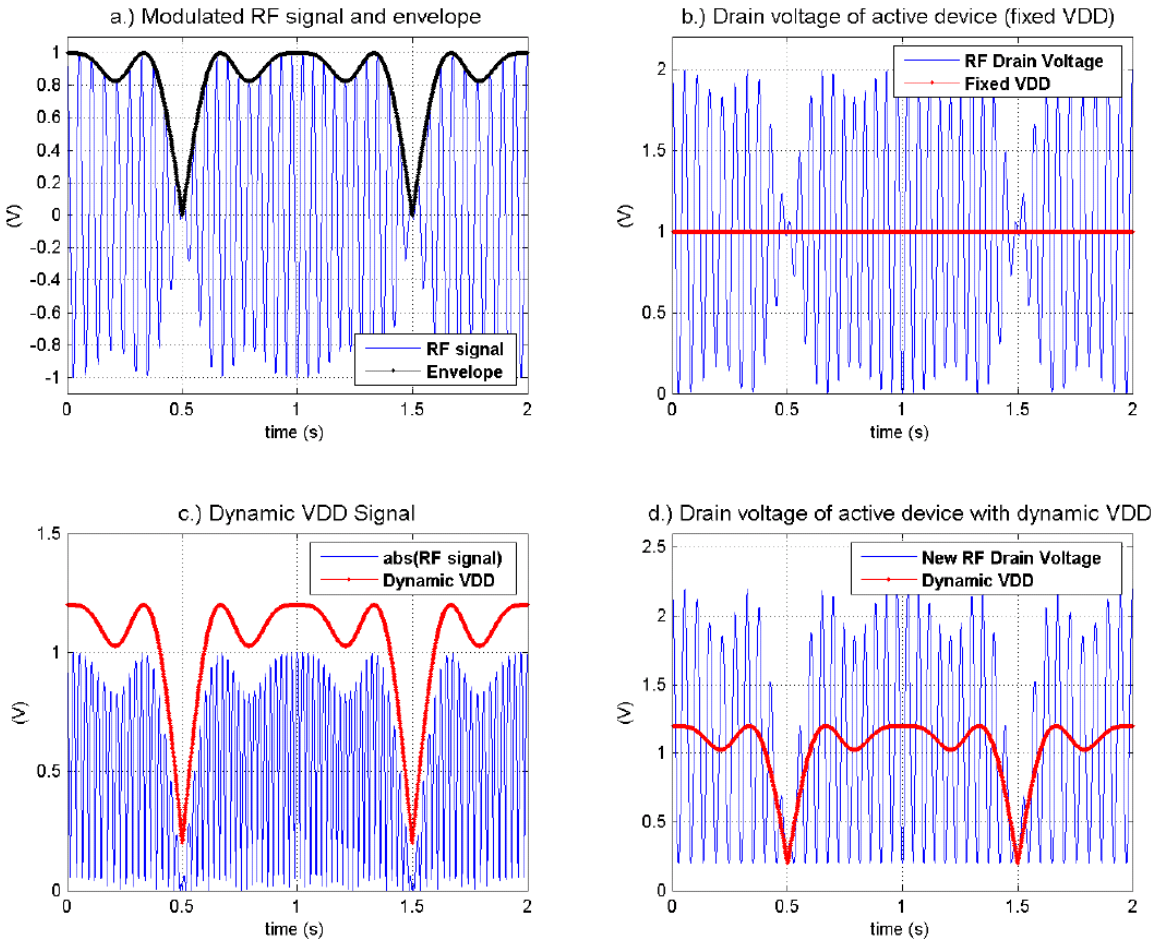


Figure 25. Time domain envelope tracking waveforms

Envelope tracking involves rapidly varying the supply voltage of a linear PA, tracking the envelope, or time varying carrier amplitude. With this technique the transmitter operates with a traditional Cartesian architecture as shown in Figure 23. Efficiency is improved in scenarios where the voltage swing at the drain of the active device is less than the supply voltage. If the supply voltage is reduced, all current drawn by the active device and delivered to the load comes from a lower voltage – reducing power loss, as shown in Figure 24. It is critical that the active supply modulator is power efficient. It is usually constructed from among the classes of switching voltage regulators or DC-DC converters. If the supply voltage is adjusted using a resistive or linear voltage regulator, there is no power savings in the envelope tracking system. Maximum power savings occur if the efficient voltage regulator adjusts the supply voltage to the minimum level where the PA is still linear. In some examples the PA even operates in weak compression, further improving efficiency at the tradeoff of linearity and supply noise susceptibility [28, 30]. The amplitude signal can be mapped from the baseband, or measured from the upconverted RF signal at the input or output of the PA [21].

Figure 25 shows an example of the time domain waveforms for an envelope tracking system. Figure 25 (a) shows the modulated RF signal and envelope waveform for the example in section 2.3.2. With a fixed V_{DD} of 1.0V, the signal swing is less than the maximum, especially at 0.5 and 1.5µs. Figure 25 (c) shows an example dynamic V_{DD} signal. Here, V_{DD} is slightly higher than the RF envelope such that V_{DS} does not reach zero as this would cause the PA to go into compression – an active CMOS device would

be in the triode region. Figure 25 (d) shows the resulting RF V_{DS} waveform. The RF signal swings twice V_{DD}, but the bottom edge of the envelope is fixed and above the minimum V_{DS} for the device. The resulting signal amplitude and output power are the same as with fixed V_{DD}, but with substantially higher average efficiency.

Examples of envelope tracking systems include the work of Hanington et al. in [21], Staudinger et al. in [22], Schlumpf et al. in [47] and many others [48-50]. Other examples operate the linear PA in compression to achieve higher efficiency. In [28], Wang et al. present an envelope tracking system for OFDM with an envelope bandwidth of 20MHz and average efficiency for the entire system between 19%-28%.

3.1.2 Dynamic Supply Polar Modulation

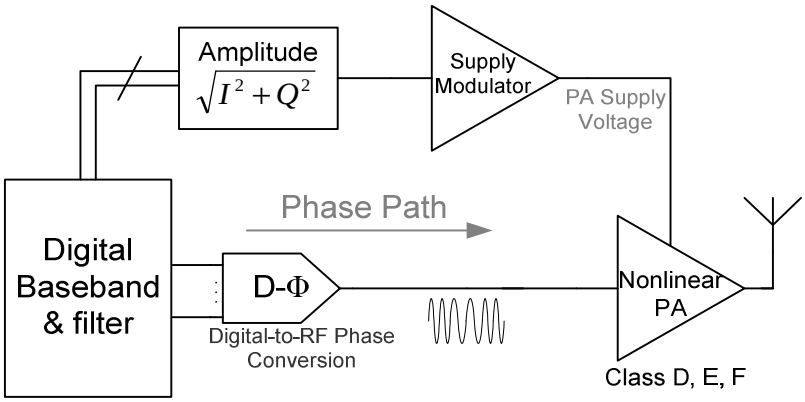


Figure 26. Dynamic supply polar modulation system

Significant efficiency gains are also possible for systems with nonlinear power amplifiers. As mentioned in section 2.3.1, switching PAs have a relationship between the supply and the output RF waveform that follows

$$v_{O-RF} = \alpha \cdot V_{DD} \cos\left(w_c t + \phi(t)\right), \tag{14}$$

where v_{O-RF} is the output RF waveform, $\phi(t)$ is the time-varying phase of the RF carrier, and α is the constant of proportionality between V_{DD} and the carrier amplitude. Parameter 'α' is generally close to one, but can include linear loss mechanisms in the PA, passive components, and interconnect [7].

The supply modulated polar system is shown in Figure 26. The amplitude and phase paths are split in the baseband, or using other methods like the Kahn technique in Figure 10. The constant envelope phase-modulated signal controls the input of the PA. The amplitude signal passes to the supply voltage regulator which modulates the amplitude of the polar vector signal. As mentioned in section 2.3.2, it is critical that there is proper time alignment of the amplitude and phase signals. It is also important to consider the AM-AM and AM-PM distortion mechanisms, as these may cause problems with EVM and the output spectrum. The supply modulator has to have high bandwidth and low noise to avoid additional degradation of transmitter performance.

This system is attractive from an efficiency perspective because nonlinear PAs are typically more efficient than linear PAs (in many but not all cases). Much of the early work on this technique was motivated to linearize switching PAs, such that they could be used for non-constant envelope modulation. The straightforward approach is to use a linear regulator to adjust the supply voltage for the PA [13, 23, 24]. This is a simple and cost effective approach as linear regulators are relatively small and robust.

An obvious improvement is to use switching voltage regulators to modulate the supply voltage. Unlike linear regulators, these voltage regulators are ideally 100% efficient. Switching regulator architectures could achieve both high peak efficiency and high efficiency in power backoff, as with the case for curve iii.) in Figure 22. However, switching regulators may be more difficult to implement because of noise and bandwidth constraints. Tradeoffs between bandwidth and efficiency reduce the effectiveness of switching topologies at high frequencies. Noise from the switching process can affect the spectral performance of the PA [30]. Careful consideration of all the system tradeoffs is necessary for a successful implementation. Successful polar implementations with dynamic switching voltage regulators include [21] and [51], the latter using an envelope reconstruction PA with a 130MHz switching voltage regulator.

3.2 Voltage Regulator Topologies

3.2.1 Linear Regulators

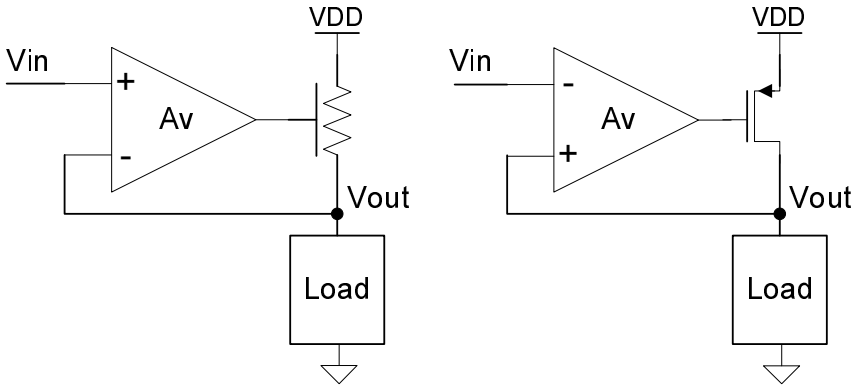


Figure 27. Linear regulator topologies

As mentioned in the previous section, linear regulators are fast, cost effective and robust. Shown in Figure 27, linear regulators use a resistive voltage drop to generate voltage *Vout* from fixed supply voltage V_{DD}. In the CMOS example in Figure 27 (b), a PMOS output device acts as a controlled current source to regulate the output voltage. It is important that the PMOS device is large enough to supply the maximum load current and maximum output voltage. The linear regulator topology can achieve high bandwidth, low steady state error, good noise performance, and high *current* efficiency [52-54]. Current efficiency is measured as the total current delivered to the load divided by the total current drawn from the supply – higher bias currents in the linear regulator circuit degrade current efficiency. However, power efficiency goes with the ratio of V_{out} to V_{DD},

$$\eta_{LR} = \frac{V_{out}}{V_{DD}}, \tag{15}$$

where η_{LR} is the efficiency of the linear regulator. This makes the linear regulator less attractive for transmitter applications where the supply voltage is less than V_{DD} for a large percentage of the time.

3.2.2 Switching Voltage Regulators

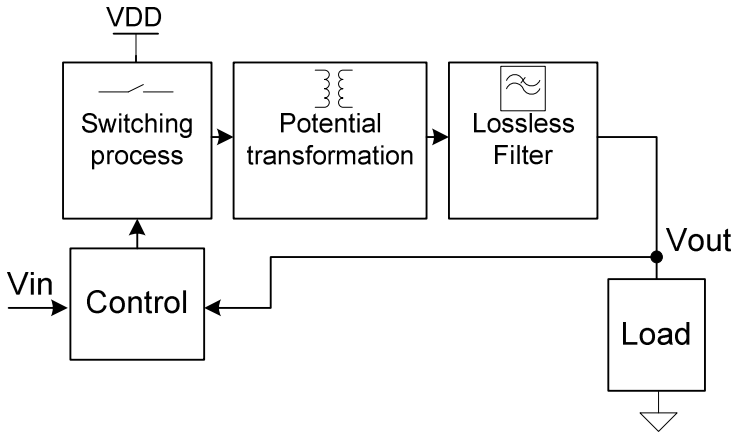


Figure 28. Generic voltage-mode switching regulator block diagram

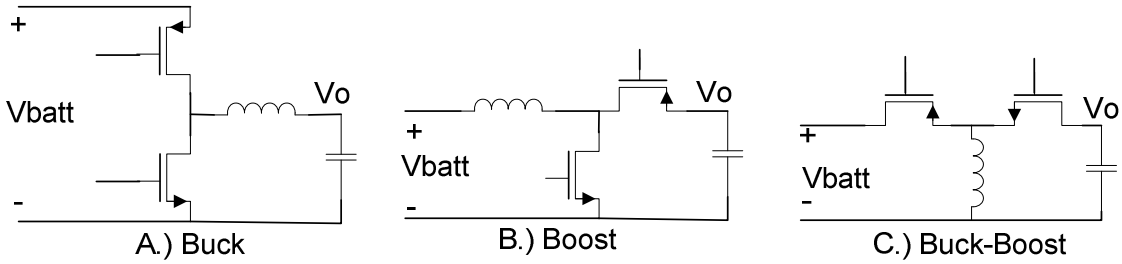


Figure 29. DC-DC conversion cells: buck, boost, and inverting buck-boost

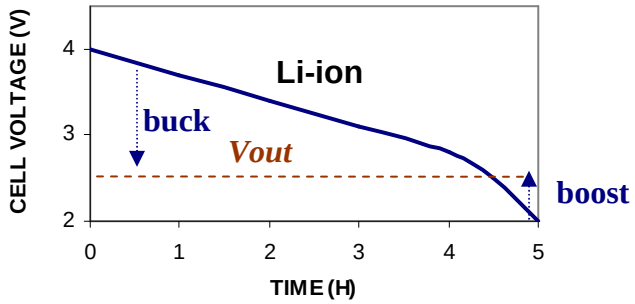


Figure 30. Typical battery discharge curve and power converter mode of operation

Switching regulators can be substantially more power efficient than linear regulators, but require more complex control processes to convert DC voltage potentials. The generic regulator shown in Figure 28 uses switching, voltage potential transformation, and filtering to convert and recover a DC output voltage. A control system measures the error and adjusts the switching process to correct for deviations in output voltage.

There are many possible architectures for switching voltage regulators that use magnetic and electrostatic voltage-transformation cells. The examples shown in Figure 29 include step down (buck), step up (boost), and step up or down (buck-boost) magnetic conversion cells. Other topologies may use magnetic transformers (flyback), or pure electrostatic switched capacitor DC-DC conversion [55-57]. Each has different tradeoffs and is appropriate for different circumstances. Buck or buck-boost converters are popular for transmitter applications that operate from a battery. Buck converters will transform the DC potential down, like a linear regulator, but are ideally 100% efficient. Buck-boost converters can both increase and decrease a voltage level, and may be useful in portable applications with widely varying battery voltage. Shown in Figure 30, if the battery level is above the required supply voltage, buck-mode will step voltage down. If V_{out} is above the battery voltage, boost-mode can increase the potential.

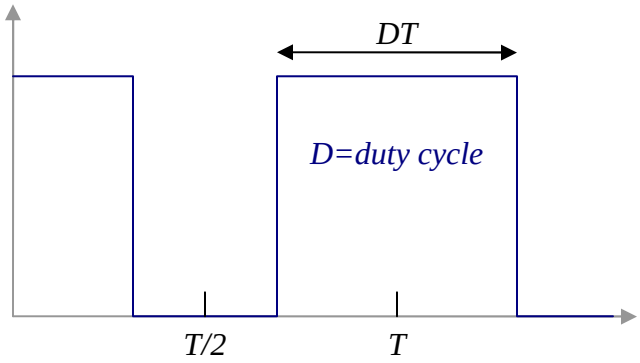


Figure 31. Pulse-width-modulation (PWM) waveform

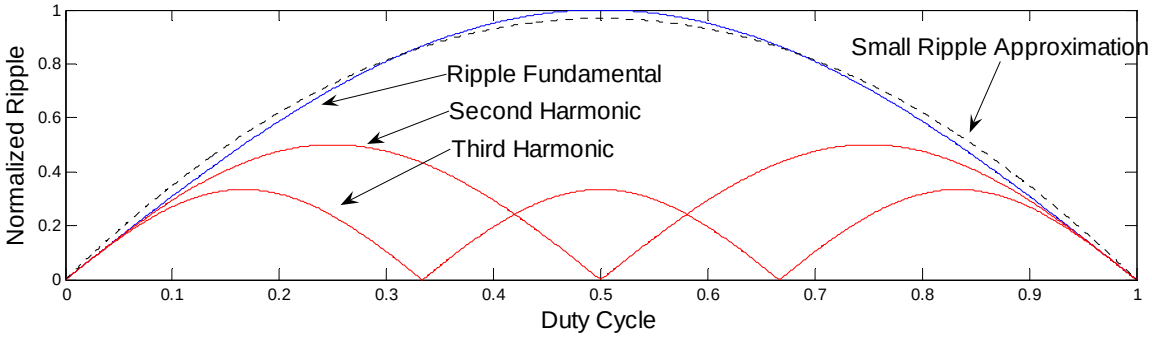


Figure 32. Fundamental and harmonics of pulse-width modulated waveform versus duty cycle, normalized to fundamental peak.

Major differences between switching and linear regulators, from design and operational perspectives, stem from the dynamics of the output filter and the switching processes. The higher order output filter in DC-DC converter topologies can be a constraint on the output impedance or stability of the regulator. Special control laws compensate for more complex dynamics to maintain low output impedance for load transients [58, 59], and to achieve high tracking bandwidths [36].

The switching process generates spectral content at the fundamental and harmonics of the switching frequency. Switching voltage regulators often use pulse-width modulation (PWM) to control the DC voltage at the output. Shown in Figure 31, with

PWM, the duty cycle of a switching waveform controls the DC component of the waveform. With PWM, the DC component is linear with duty cycle. This simplifies control as a time averaged model of the switching cell is often adequate to analyze the behavior of the DC-DC converter. However, higher harmonics of the switching waveform can complicate the output spectrum of the converter. The Fourier-series decomposition of a PWM waveform as a function of duty cycle is:

$$V(t) = V_{in}\left[D + \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{(-1)^n \cdot \sin(n\pi D) \cdot \cos(n w_{sw} t)}{n} \right], \tag{16}$$

where V_{in} is the maximum voltage of the PWM signal, w_{sw} is the switching frequency, D is the duty cycle, and n is the harmonic number. The magnitudes of the first three harmonics versus duty cycle are shown in Figure 32.

The problem with the extra spectral content generated by the switching process is that it appears as noise on the transmitter supply voltage. Power supply noise can be problematic in wireless systems because it can mix with RF signals and show up in the output spectrum. This is a well known problem for supply regulated voltage controlled oscillators (VCOs), as mentioned in section 2.2.1, and described in [52]. Supply noise is also problematic for the power amplifier, which may have supply-dependent gain and phase transfer functions – even with linear PA topologies. The problem of supply noise upconversion and mixing will be described in detail in chapter 4.

Switching noise and the output filter dynamics result in an efficiency tradeoff for dynamic supply systems. The lossless filter components are sized such that the

dynamics of the filter will not interfere with the magnitude or phase response of the regulator. Generally, poles in the filter are placed near or above the tracking bandwidth of the system, which can be over six times higher than the cartesian I/Q bandwidth [13]. With a higher filter cutoff, the switching frequency has to increase to reduce the magnitude of the switching noise. Generally, higher switching frequencies will reduce the power efficiency of the voltage regulator. References [36] and [45] describe how the minimum power loss in an optimized switching converter (with a fixed semiconductor process technology) goes with

$$P_{\min} \approx 2\sqrt{I_{rms}^2 R_O \cdot E_G \cdot fsw}\,, \tag{17}$$

where I_{rms} is the rms current to the load and f_{sw} is the switching frequency. Here, E_G is the energy to charge the input capacitance of the device per unit width, and $R_O = \frac{1}{G_O}$ is the resistance of the device per unit width. For CMOS switching devices these quantities may be written as

$$G_O = \frac{1}{l_{\min}} \mu Cox(V_{DD} - V_T - V_{ds-on})\,, \tag{18}$$

$$E_G = l_{\min} Cox V_{DD}^2\,, \text{ and} \tag{19}$$

$$W_{opt} = \sqrt{\frac{I_{rms}^2 \cdot R_O}{E_G \cdot f_{sw}}} \tag{20}$$

where $l_{\min}$ is the minimum channel length for the process, V_T is the threshold voltage of the transistor, μ is the carrier mobility, Cox is the capacitance of the gate oxide, V_{DD} is

the supply voltage, and V_{ds-on} is the average drain-source voltage of the switch. In (20), W_{opt} is the optimum width of the device for minimum power loss. If the switch operates in the triode regime, long channel approximations may hold even for short channel devices.

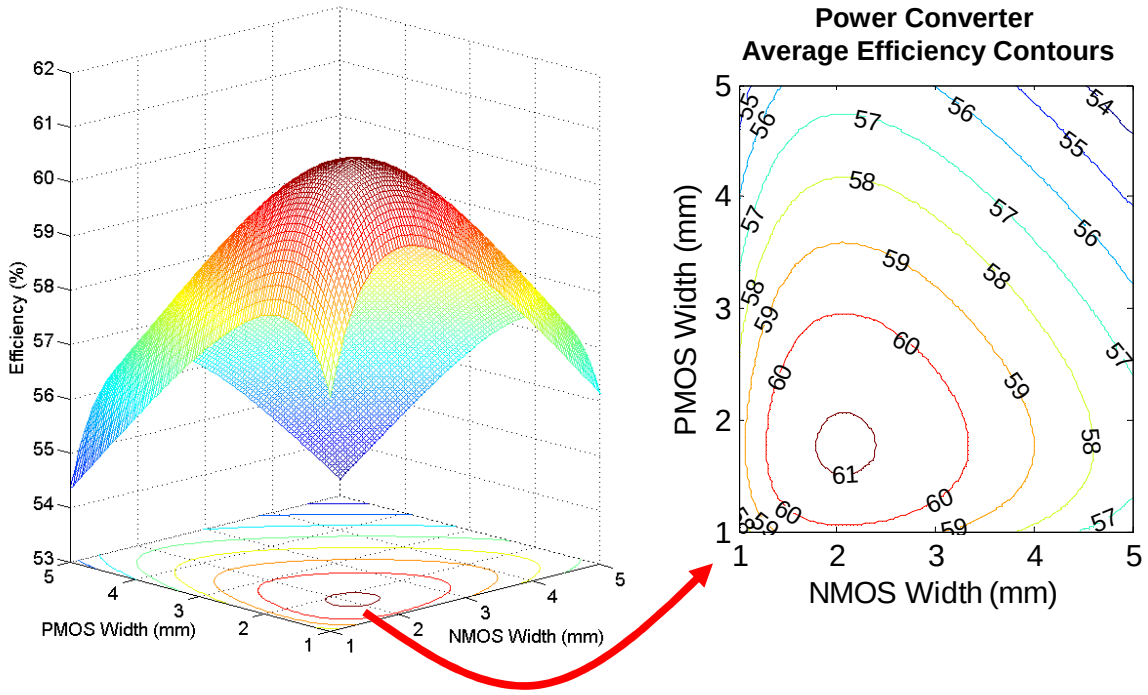
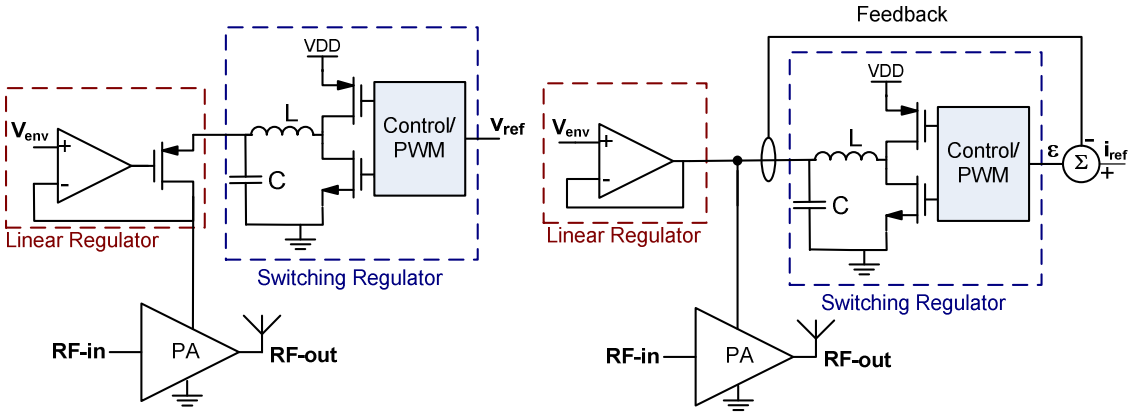


Figure 33. Contour representation of average efficiency of the switching regulator vs gate width

Equations (17) and (20) are valuable to optimize the switching regulator for a single operating point, captured with I_{rms}. In a realistic scenario, average efficiency is more important than efficiency at a single operating point. In this case, the PDF can be used to optimize the switching regulator design. Reference [36] describes how to iteratively optimize the switching regulator for maximum average efficiency. The results of this

optimization procedure are shown in Figure 33 for a 5MHz tracking bandwidth and 1.0W maximum output power in 0.18um CMOS. Here, average efficiency is shown across the gate widths of active NMOS and PMOS switching devices. The process uses the PDF and a realistic model for the PA to find the device sizes that achieve maximum average efficiency. Average efficiency for the switching regulator was over 60% even though average output power was 20dB below peak output power. Device sizes are substantially smaller (especially the PMOS devices) than if the system is optimized only at peak power level. This example demonstrated the benefit of designing for battery life, rather than the peak efficiency of the system.

3.2.3 Hybrid Voltage Regulators: Introduction



a.) Series hybrid voltage regulator b.) Parallel hybrid voltage regulator

Figure 34. Hybrid voltage regulator schematic: a.) Series hybrid, b.) Parallel hybrid

As the name suggests, hybrid voltage regulators merge concepts of both switching and linear regulators. Hybrid regulators can provide benefits of both switching and linear topologies, namely: fast dynamic response, low output noise, and high efficiency. The

two main topologies that are common for dynamic supply applications are series-hybrid and parallel-hybrid regulators, shown in Figure 34.

Series hybrid regulators operate with a conventional low-dropout (LDO) linear regulator, and a dynamic switching voltage regulator. The switching regulator adjusts its output to the minimum level where the linear regulator can achieve regulation – the linear regulator is always in a low-dropout mode of operation. Minimizing the dropout voltage on the linear output device reduces the power loss associated with the LDO. In this case, a high power-supply-rejection-ratio (PSRR) linear regulator significantly attenuates switching noise. The linear regulator can also supply fast transients to the load, as long as voltage transients do not force the active device into the triode regime. The main problem with the series hybrid is that its ability to track voltage transients in the positive direction is limited by the dropout of the active device. Additional circuitry may be needed to handle high slew rates, to prevent clipping the PA supply voltage. If this is not included, the PA supply voltage may be limited to a small dynamic range, or low peak-to-average power ratio (PAPR) modulation schemes, as in [60].

Parallel-hybrid voltage regulators operate with parallel linear and switching regulator stages. In the typical example, the linear regulator acts as a voltage follower, driving the output voltage signal to the load. The switching regulator operates as a current source, supplying some nominal amount of current through a passive filter, usually an inductor. In this case, the linear regulator output is low impedance (voltage source) and the switching regulator output is high impedance (current source). These stages have

different regulation objectives, so they do not interfere with each other. In most examples, the switching regulator supplies the DC component or average current to the load [28, 61, 62]. This improves efficiency substantially compared to a linear regulator alone. The switching regulator also has the opportunity to supply current at higher frequencies (in addition to the DC component). In most examples the higher frequency components match the power spectrum of the amplitude-path signal [62]. In chapter 5, we propose a different strategy that is based on optimizing the efficiency of the parallel-hybrid combination in the time-domain. Results show that higher efficiency is possible if the DC-DC converter current follows an optimum trajectory based on the dynamics of the envelope signal, the supply voltage, and the DC output voltage [63, 64]. If this is of interest, the reader is recommended to skip to chapter 5 where this discussion continues. Otherwise, we will segue to the topic of power supply noise and its effect on polar and envelope tracking transmitters.

Chapter 4 Power Supply Noise Analysis for RF Amplifiers

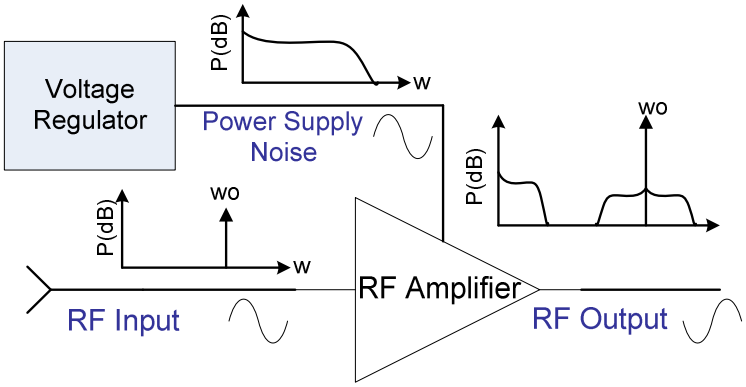


Figure 35. Effect of supply noise on RF amplifier output spectrum

4.1 Introduction

In this chapter, we present an analysis of the power supply rejection properties of RF amplifiers. The focus is on the mechanisms for upconversion of low frequency supply noise to the nearband RF spectrum. As mentioned in the previous chapter, leakage of noise signals is a well known problem that affects many components in the wireless system. Voltage-controlled oscillators (VCOs) are particularly sensitive to supply and substrate noise since they have frequency-tuned components (varactors) that are designed to be sensitive to voltage [52]. Switching power amplifiers in polar systems are also designed to respond to the power supply. From (14), polar PAs have nearly unity transfer function between the power supply and the amplitude of the RF carrier.

As such, the analysis of the mixing problem with VCOs and polar PAs may be straightforward since the conversion gain comes directly from the voltage-sensitivity transfer function.

Here we focus on the more difficult problem of supply rejection for nominally linear RF circuits. Linear PAs are ideally insensitive to the supply voltage, as long as they do not operate in compression. However, parasitic nonlinearities create mechanisms for the supply voltage to affect the gain and phase transfer functions of linear amplifiers. Modulation of gain or phase allows small signals on the power supply to mix with the RF signal. The mixing products can be difficult to filter and may violate the spectral mask requirements in transmitter applications. Figure 35 demonstrates the concept of low frequency supply noise mixing with the RF signal – the RF spectral content may appear as sidebands, side-lobes, or images of the modulated RF spectrum adjacent to or inside the band of interest [29].

This chapter and the work presented in [29] and [30] focus on supply noise rejection for weakly nonlinear CMOS common-source amplifiers, as would be the case for CMOS class A, AB, and B PAs. This work is therefore directly useful for the design of envelope tracking transmitters, especially in knowing how much ripple is acceptable on the supply voltage. Volterra series analysis is a practical and direct way to get insight into supply noise mixing phenomenon in this case. We extend the analysis to treat multi-port systems by including non-symmetric cross terms in a conventional frequency domain analysis. Specifically, this analysis is an adaptation of the method proposed by Chua in

[65], Schetzen in [66], and described by Wambacq and Sansen in [15]. The calculations are based on nonlinearities extracted from BSIM3v3 models, but result in expressions that are simple enough to use for hand design. We demonstrate the practical use and insight gained through our analysis with the design and fabrication of a linear CMOS power amplifier (PA).

Section 4.3 presents the theory for multiple-port signal intermodulation starting with the memoryless analogy. Conventional Volterra series analysis is reviewed and expanded to a multi-port formulation to treat RF amplifiers with memory. Section 4.4 describes the target problem and the method for characterizing the nonlinearities in CMOS amplifiers. Section 4.5 presents Volterra operators for the supply intermodulation sidebands. Section 4.6 compares hand analysis to simulation and experimental results. Spectral regrowth is compared for single-tone and EDGE modulated signals operating in the traditional 900MHz band as well as at 2.4GHz.

4.2 Motivation of Volterra-Series for Supply Noise Problems

In the context of supply noise upconversion, Volterra series is a direct and powerful approach to achieve an analytical understanding of the circuit. Harmonic balance (HB) techniques can also be applied to study this problem, particularly in simulation with Agilent Advanced Design Systems (ADS) or Cadence-Spectre periodic-steady state (PSS) analysis [67]. While harmonic balance techniques are useful to determine voltage and current waveforms in mixed linear and nonlinear systems, solving the harmonic balance

equation requires knowledge of the input signal. With HB, the order of computation increases with the number of input harmonics. This makes harmonic balance impractical for studying broadband performance metrics such as spectral regrowth and adjacent channel power ratio (ACPR), especially for real wireless systems with non-periodic amplitude waveforms. In this regard, Volterra series (VS) has several advantages:

- VS can describe the linear and nonlinear dynamics of a circuit without knowledge of the input signal (provided that the circuit remains in a weakly nonlinear regime).
- The Volterra kernels can provide a compact expression of the time and frequency domain behavior as a function of physical device parameters, independent of the input waveform.
- The circuit is solved only once (in contrast with harmonic balance which may need to re-iterate for different input waveforms)
- VS analysis allows rapid computation of multi-tone and broadband behavior, as in [68], and is one of few simulation techniques that is practical for rapid computation of spectral regrowth phenomenon.

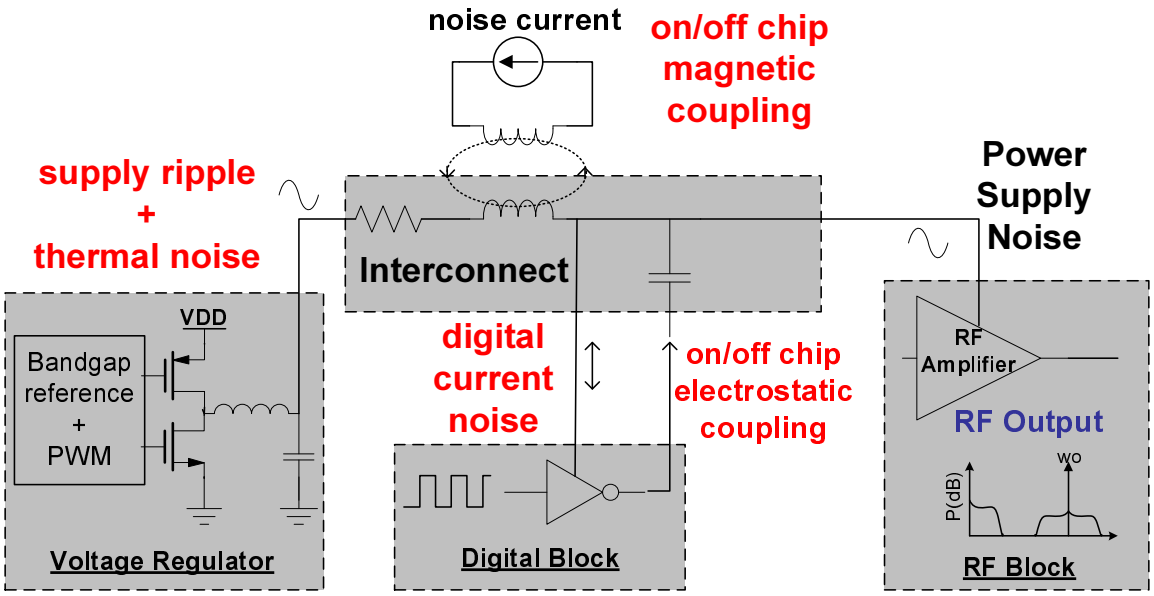


Figure 36. Noise sources in RF systems

Volterra series is effective in the context of supply noise because noise sources are typically small-signal relative to the operating point of the amplifier. Shown in Figure 36, common sources of supply noise include magnetic coupling to bondwires and power supply interconnect, electrostatic coupling between nearby traces, and current noise from analog or digital blocks passing through parasitic inductance and resistance in the power rails [69]. Supply noise may also be directly injected into the system by the voltage regulator [21, 47, 51]. In these cases supply noise is typically less than 10% and often less than 1% of the DC supply voltage level. With small supply noise amplitude, linear amplifiers typically remain in the weakly-nonlinear regime. In this case, Volterra series can often predict performance over many decades of power of the RF input signal.

It is important to note that many of the important sources of supply noise are low

frequency relative to the RF signal. Such noise sources are difficult to filter because at low frequency, bypass capacitors are less effective. With low frequency noise signals, mixing products tend to be more problematic since they create in-band or near-band frequency content. In our analysis, Volterra series analysis can be used to predict the sensitivity of the power amplifier (PA) to supply ripple through the power supply rejection ratio (PSRR). This analysis can be used to maximize the efficiency of the switching regulator for a given amount of voltage ripple, while simultaneously meeting EVM and ACPR requirements in the transmitter.

4.3 Theory of Multiple-Port Supply Intermodulation

Power supply noise can mix with the RF carrier and be upconverted to the nearband spectrum. This process happens when the amplifier has stray paths that couple the supply voltage to nodes in the amplifier that modulate the amplitude or phase of the transmitted signal. At high frequencies it may be easy to filter supply noise with choke inductors or bypass capacitors. It may be more difficult to filter low frequency supply noise due to limitations on the size of filter elements. Low frequency supply noise is also problematic because the first order intermodulation terms may be close to the band of interest.

Analysis of supply-carrier intermodulation is complicated by the dynamics and nonlinearities of the system. If the RF amplifier circuit does not have memory, the distortion products can be analyzed in a straightforward manner with traditional power

series analysis [10, 70]. This may be the case if the effects of reactive elements are not significant, or can be easily included between stages that have purely conductive or resistive nonlinearities. Such may be the case in a circuit with only diode or transconductance nonlinearity followed by a reactive filter. In this case, the small signal gain of the amplifier may be characterized as a function of the input voltage and the power supply. The nonlinearities of the topology are characterized around a bias point such that the output signal, S_{out}, can be written as a power series,

$$\begin{aligned} S_{out}(S_{in}, S_{vdd}) = a_{10}S_{in} + a_{20}S_{in}^2 + a_{30}S_{in}^3 \ldots \\ + a_{11}S_{in}S_{vdd} + a_{21}S_{in}^2 S_{vdd} + a_{12}S_{in}S_{vdd}^2 + \ldots, \\ + a_{01}S_{vdd} + a_{02}S_{vdd}^2 + a_{03}S_{vdd}^3 + \ldots \end{aligned} \tag{21}$$

where a_{ij} are the gain terms as a function of the ith power of the input signal and the jth power of the AC supply voltage noise; S_{in}, S_{out}, *and* S_{vdd}, are the signals at the input, output and supply terminals centered around the operating point. Here, a_{10} describes the first order forward gain term, a_{01} describes the forward gain from the supply terminal, and a_{11} describes the first order intermodulation term between the input signal and the supply noise. If the input signal follows $S_{in} = v_i \cos(\omega_0 t)$, and the supply noise is a single tone that follows $S_{vdd} = v_s \cos(\omega_S t)$, the amplitude of the supply ripple sideband will be at $\omega_0 \pm \omega_S$, such that,

$$v_{out}(\omega_0 \pm \omega_S) = \frac{1}{2} a_{11} v_i v_S . \tag{22}$$

In this case, a useful figure of merit is the magnitude of the supply ripple sideband in decibels-below the carrier (dBc). As seen in (22), this quantity is relevant because the

magnitude of the supply ripple sideband is directly proportional to the magnitude of the input signal for constant supply noise. It may be practical to treat the supply noise magnitude as constant to reflect worst-case analysis, or when voltage ripple from a switching regulator is of a known, fixed magnitude. The supply ripple sideband in dBc is the ratio of the forward gain term to the supply ripple sideband magnitude, the quantity expressed in decibels,

$$Sideband(dBc) = dB\left(\frac{2a_{10}}{a_{11}} \cdot \frac{1}{v_s}\right). \tag{23}$$

Expanding on this figure of merit, if the power supply noise is fixed and of constant magnitude, it may be practical to subtract its effect from the relationship in (23). In this case the ratio becomes signal-independent and is only a function of the physical properties of the amplifier. Because the ratio is amplifier specific, it has a notable similarity to the baseband figure-of-merit, the power supply rejection ratio (PSRR) [40]. In the rest of this work we will refer to this ratio as the PSRR for RF amplifiers and define it as

$$PSRR(dBV) = dB\left(\frac{2a_{10}}{a_{11}}\right). \tag{24}$$

The units of $\frac{2a_{10}}{a_{11}}$ are volts because the expression in (23) has been multiplied by the supply ripple magnitude. This leaves the units of (24) in *dBV*. The physical interpretation of *PSRR* in (24) is: *the sideband in dBc that would occur for a one-volt (zero-dBV) supply ripple magnitude*. It should be noted that (21)-(24) are defined for the

memoryless power-series analysis. Next we will describe analysis of power supply intermodulation for systems with dynamics and frequency dependent nonlinearities.

4.3.1 Single-Input (Two-Port) Volterra-Series Analysis

Volterra series can be used to analyze the behavior of nonlinear systems with memory. As long as the system is weakly nonlinear, only a few terms of the series are needed to predict important distortion phenomenon. With a Volterra series representation, the time domain output of a time-invariant nonlinear system for an input, *x(t)*, can be written as

$$y(t) = \sum_{n=0}^{\infty} F_n(x(t)), \tag{25}$$

where

$$F_n(x(t)) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n) x(t-\tau_1) \ldots x(t-\tau_n) d\tau_1 \ldots d\tau_n \quad . \tag{26}$$

In (26), the $h_n(\tau_1, \cdots \tau_n)$ are known as the nth order Volterra kernels of the system. The F_n, which represent the convolution integral in (26), are known as the Volterra operators or Volterra transfer functions [66]. From the perspective of (25) and (26), Volterra series appear as a generalized convolution in the time domain. The time domain Volterra kernels can be used in the frequency domain as Volterra operators or Volterra transfer functions to perform circuit calculations [15, 65, 66, 71]. In this case the Volterra operators are frequency dependent transfer functions, $H_n(j\omega_1, j\omega_2, \ldots, j\omega_n)$,

that capture the phase and amplitude response of the circuit for a given set of frequencies [66]. Many good references describe the use of Volterra-series transfer functions in the context of mixed time-frequency descriptions of nonlinear systems [15, 16, 65, 66, 68, 71-76].

4.3.2 Multiple-Port Volterra Analysis

The extension of 2-port Volterra analysis to multi-port systems can be done by extending the convolution integral in (26) to higher dimensions. The resulting formulation includes both direct terms between each input and the output, and cross-terms that describe intermodulation among the inputs. As in (21), the first order cross term can be used to describe mixing between supply noise and the RF carrier. The increased dimensionality of multi-port Volterra analysis complicates hand analysis, but the first and second order terms are still manageable, and can provide considerable insight into the supply noise mixing effect.

$$v_{out}(t) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} F_{mn}(v_1(t), v_2(t)) \tag{27}$$

$$F_{mn}(v_1(t), v_2(t)) = \int_{-\infty}^{\infty}\cdots\int_{-\infty}^{\infty} h_{mn}(\tau_1,\ldots,\tau_{m+n}) v_1(t-\tau_1)\ldots v_1(t-\tau_m) v_2(t-\tau_{m+1})\ldots v_2(t-\tau_{m+n}) d\tau_1\ldots d\tau_{m+n} \tag{28}$$

$$\begin{aligned} S_{out} = {} & A_{10}(j\omega_a)\circ S_1 + A_{20}(j\omega_a, j\omega_b)\circ S_1^2 + A_{30}(j\omega_a, j\omega_b, j\omega_c)\circ S_1^3 + \cdots \\ & + A_{01}(j\omega_a)\circ S_2 + A_{02}(j\omega_a, j\omega_b)\circ S_2^2 + A_{03}(j\omega_a, j\omega_b, j\omega_c)\circ S_2^3 + \cdots \\ & + A_{11}(j\omega_a, j\omega_b)\circ S_1 S_2 + A_{21}(j\omega_a, j\omega_b, j\omega_c)\circ S_1^2 S_2 + A_{12}(j\omega_a, j\omega_b, j\omega_c)\circ S_1 S_2^2 + \cdots \end{aligned} \tag{29}$$

The time domain Volterra series formulation for a system with 2 input ports and a

single output may be written as in (27), where (28) is the multi-port analogy to the convolution integral in (26). In (28), h_{mn} is the multidimensional Volterra kernel, v_1 and v_2 are the two input signals, and F_{mn} is the multidimensional Volterra operator in the time domain. In the frequency domain the Volterra series can be written as in (29). Here the notation A_{ij} denotes the Volterra operator for the i^{th} order of input S_1, and the j^{th} order of input S_2. The $j\omega_n$ terms are dummy frequency variables that can assume the relevant frequency content of the input signal. The operator "$\circ$" represents the frequency domain operation of the transfer function on the signals at the appropriate frequencies as is standard in phasor transfer function analysis. The notation in (29) is borrowed from [74]. In (29), A_{10} and A_{01} are the first order (linear) Volterra operators for each of the two input terminals. The operator A_{11} describes the second order cross term. A_{21} and A_{12} describe the third order cross terms. It should be noted that the Volterra series in (29) has structural similarity to the memoryless analogy in (21). The main difference is that the operators in (29) are a function of the frequency content of the input signal and reflect the weakly nonlinear dynamics of the system.

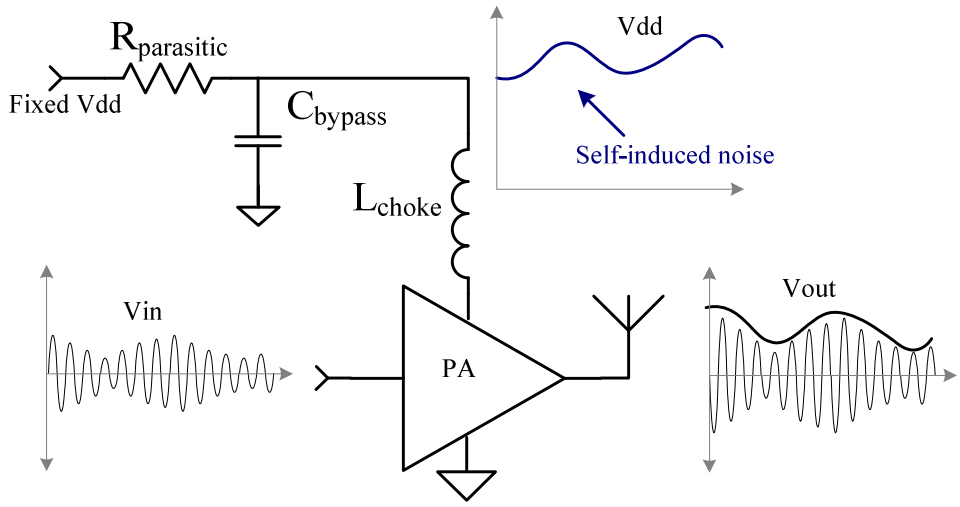


Figure 37. Self-induced power supply noise from high supply impedance at the envelope frequency

An additional source of supply modulation may be caused by the PA itself. As shown in Figure 37, this happens if the supply terminal is not low impedance to the RF or envelope signal. In this case, the supply voltage may change with the signal amplitude. This can cause problems with second order distortion as well as higher orders. These effects are captured in conventional 2-port Volterra series analysis and will be reflected in the forward-direct operators: A_{20}, A_{30}, etc. While self-induced supply noise may be a serious problem in many situations, these effects can be alleviated with good supply bypassing and voltage regulation techniques. In this case it is necessary to create a low impedance supply at frequencies correlated with the operation of the PA. In this work we focus on uncorrelated noise and treat the supply terminal as a separate input. Therefore the focus is on the A_{11} operator. It should be noted as a possible simplification of the analysis, that the self-induced noise can be characterized separately and treated as an independent noise source on the supply. In this case, the A_{11}

operator can be used to study both independent and correlated noise from the system.

In this work, we define the N-port amplifier as a black box with (*N-1)* separate inputs and a single output port. The amplifier represented in Figure 35 is defined as a 3-port system where the inputs are the conventional signal input and the supply terminal. The signal port may be either single ended or differential, whereas the supply terminal is typically referenced to ground. In this case A_{10} would correspond to the forward gain at ω_0, A_{01} would correspond to the forward supply noise gain at ω_S, A_{11} would correspond to the first sideband at $\omega_O \pm \omega_S$, and A_{12} and A_{21} would correspond to the second sidebands at $\omega_O \pm 2\,\omega_S$ and $2\,\omega_O \pm \omega_S$. The PSRR of the circuit is therefore written as

$$PSRR = dB\left|\frac{2A_{10}(j\omega_0)}{A_{11}(j\omega_0, j\omega_S)}\right|, \tag{30}$$

where the absolute value is taken to mean the magnitude of the complex operator ratio. It should be noted that the cross terms are not necessarily symmetric, since generally, $A_{11}(j\omega_1, j\omega_2) \neq A_{11}(j\omega_2, j\omega_1)$. Intuitively, this is because the signals may follow different nodal paths to the output, therefore the frequency content of signals at different ports is not necessarily interchangeable. Asymmetric Volterra transfer functions can be made *partly symmetric* with techniques presented in [71]. As in the case with conventional symmetric operators, partly symmetric operators are desirable to improve computation time and complexity.

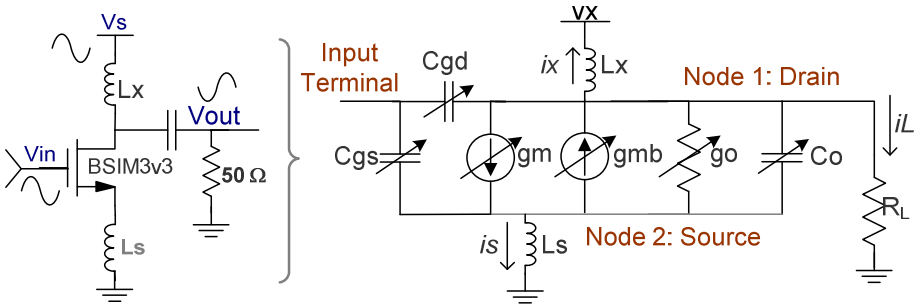


Figure 38. CMOS inductor-degenerated common source amplifier showing nonlinear elements.

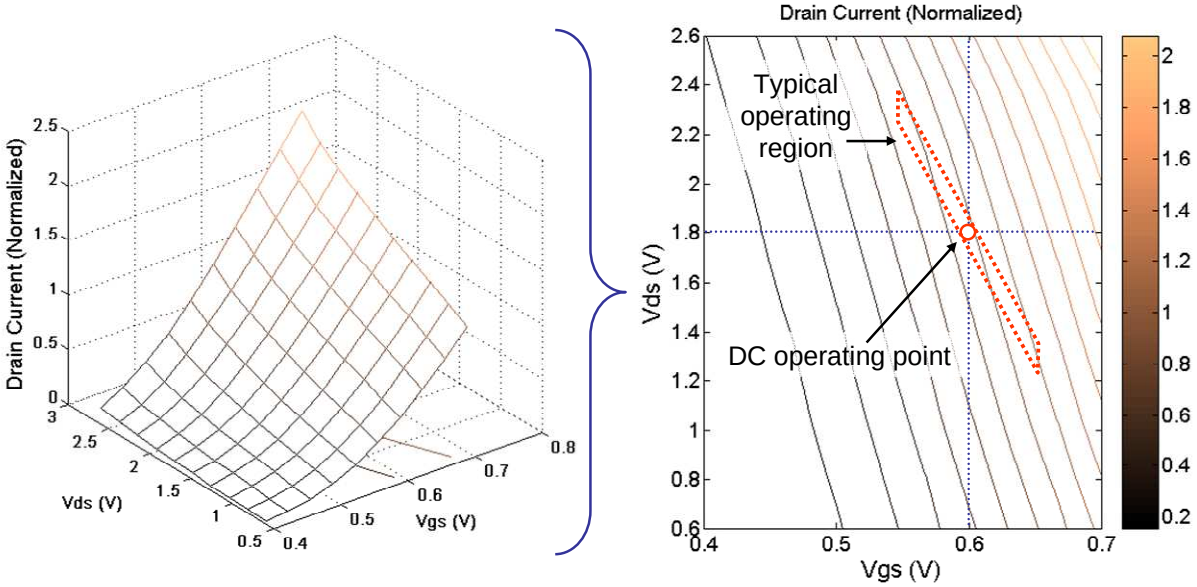


Figure 39. MOSFET drain current versus gate-source and drain-source voltage. Nonlinearities are extracted around the dc operating point highlighted in the figure.

4.4 Target Problem and Characterization of Nonlinearities

In order to demonstrate multi-port supply rejection analysis, we designed and fabricated a CMOS power amplifier in 180nm technology. Figure 38 shows the basic amplifier cell including inductance at the source and drain to model the effects of the bondwires and RF choke elements. We chose the common-source topology because it is the fundamental gain stage for many RF subsystems including PAs, and low-noise

amplifiers. Figure 38 also shows the major sources of nonlinearity in the CMOS amplifier. In this example, the dominant sources of nonlinearity are the transconductance (*gm*), output conductance (*go)* and drain-bulk junction capacitance (*Cjd*). Other distortion contributors include the body-effect transconductance and gate capacitors, although these typically have a small effect on supply noise upconversion.

Nonlinearities for the system in Figure 38 were extracted from BSIM3v3 models for static and dynamic nonlinearities. Figure 39 shows the results of Spectre simulation of the drain current versus gate-source and drain-source voltage. The planar representation of current shows direct dependence on first and higher order terms of v_{gs} and v_{ds}. Importantly, there is also cross dependence on terms related to $v_{gs} \times v_{ds}$. These cross terms result in mixing effects between the signal and supply and are important to capture for noise analysis. Figure 39 also highlights the dc operating point relative to the I-V plane. The typical operating region follows the loadline for the amplifier, but deviates from a straight line in the I-V plane because of nonlinearity, reactive dynamics, and voltage ripple on the supply. Voltage ripple extends the operating region in the vertical (v_{ds}) dimension by swinging the voltage at the drain of the active device.

The nonlinear current and charge relationships were matched to a polynomial fit with least-squares regression analysis [15, 16, 76]. The polynomial expansion is fit to physical device parameters such as transconductance and junction capacitance using both current and charge relationships:

$$\begin{aligned} id = & gm_1 vgs + gm_2 vgs^2 + gm_3 vgs^3 + \cdots \\ & - gmb_1 vsb - gmb_2 vsb^2 - gmb_3 vsb^3 - \cdots \\ & + gmo_{11} vds \cdot vgs + gmo_{12} vds \cdot vgs^2 + gmo_{21} vds^2 vgs + \cdots \\ & + go_1 vds + go_2 vds^2 + go_3 vds^3 + \cdots \\ & + C_1 \frac{d}{dt} vdb + \frac{C_2}{2} \frac{d}{dt} vdb^2 + \frac{C_3}{3} \frac{d}{dt} vdb^3 + \cdots \end{aligned} \tag{31}$$

In (31), gm_i represents the forward transconductance, gmb_i is the body transconductance, gmo_{ij} is the output-transconductance cross term as a function of the i^{th} order of *vds* and the j^{th} order of *vgs*, go_i is the output conductance, and C_i is the output capacitance. Parameter C_i represents the first and higher order parameterization of the output capacitance term (represented as C_o in Figure 38). The nonlinearity is extracted from the nominally linear charge-voltage relationship, as in [15, 66], resulting in the factors of 1/2 and 1/3 in the 2^{nd} and 3^{rd} order power series terms.

4.5 Solution of Volterra Operators

To solve for the Volterra operators in (29), nodal equations are written and the system is solved sequentially for each order of the polynomial expansion in (31), beginning with the first order term. This procedure is well described in [15, 66, 74]. A unique Volterra series is written for each independent node in the system, not including the input terminal which, in this example, is controlled by a voltage source. The notation for the multi-node system can be simplified with a superscript indicating for which node the series is intended. For the source-degenerated amplifier in Figure 38, there are two independent nodes: one at the source of the active element, and one at the drain of the

active element, assuming the blocking capacitor is a short at the frequencies of interest. Using this terminology, the Volterra series in (29) can be written as

$$S_n = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty} A_{ij}^{n}(j\omega_a,\ldots, j\omega_k) \circ S_1^i S_2^j \,, \tag{32}$$

where notation A_{ij}^{n} indicates the operator for the i^{th} order of phasor input S_1 and the j^{th} order of phasor input S_2 for the the n^{th} independent node in the circuit. For each node *n*, all of the first order terms are solved without initially including the effects of the higher order terms. It should be noted that the first order terms should match conventional small signal analysis. The second order terms are solved based on the nodal constraints of the circuit, the second order nonlinear currents, and the first order terms. This process repeats, solving the system of equations for each node in the circuit, until the desired maximum order of the analysis has been achieved [15, 66, 74].

In the rest of the analysis, *node-1* and the corresponding set of operators A_{ij}^{1} will be for the *output node*, while *node-2* and A_{ij}^{2} will be used for the *source node* of the active device. The first order transfer function for the system in Figure 38 is solved as

$$A_{10}^{1}(j\omega_a) = -y_S(j\omega_a)\frac{gm_1}{K_0(j\omega_a)}, \text{ where} \tag{33}$$

$$K_0(j\omega_a) = (gm_1 + gmb_1 + y_1)\cdot(y_X + y_L) + y_S \cdot (y_X + y_1 + y_L)\,. \tag{34}$$

where y_S is the admittance of the source degeneration. The w_a term is a dummy frequency variable that represents the frequency content of the input signal [66, 74]. For inductive degeneration, $y_S(j\omega_a) = (j\omega_a L_S)^{-1}$. The constant K_0 is the recurring

denominator in many of the operators, and is evaluated at ω_a. In (34) $y_1(j\omega_a) = go_1 + j\omega_a C_1$ is the first order drain-source admittance representing both first order conductance, go_1, and first order capacitance, C_1 as in (31). The drain-supply admittance is captured in the term $y_x(j\omega_a) = (j\omega_a L_C)^{-1}$ which represents the admittance of the choke inductance, L_C. The admittance of the load impedance is captured in $y_L = (R_L)^{-1}$. In (34) the notation for the admittance parameters $y_i(j\omega_a)$ has been simplified to y_i to condense the expression, but it should be noted that these are still a function of $j\omega_a$. For the rest of the first order terms we will not explicitly indicate the frequency dependence $(j\omega_a)$ to simplify the expressions.

The rest of the first order operators follow as:

$$A_{01}^{1}(j\omega_a) = \frac{gm_1(y_X + y_L)}{K_0}, \tag{35}$$

$$A_{10}^{2}(j\omega_a) = \frac{y_X(gm_1 + y_1 + gmb_1 + y_S)}{K_0}, \text{ and} \tag{36}$$

$$A_{01}^{2}(j\omega_a) = \frac{y_X y_L}{K_0}. \tag{37}$$

In (35)-(37), the denominator expression, K_0, is the same from (34), and is evaluated at the frequency content of the input signal, ω_a, as are all the admittance terms. For (35) and (37) the dummy frequency variable ω_a would accept the frequency of the supply noise, ω_S, while for (36), ω_a accepts the frequency of the RF carrier, ω_0. These expressions fully characterize the first order behavior between the input signals and

each node in the circuit.

The Volterra operator that characterizes mixing between the supply noise and the input signal is defined by the A_{11}^1 term. In this case, A_{11}^1 operates on both the RF input signal and the signal representing noise on the supply terminal:

$$v_{out}(\omega_o \pm \omega_S) = A_{11}^1(j\omega_0, j\omega_S) \circ [Vi(\omega_0), Vs(\omega_S)], \tag{38}$$

where ω_0 and ω_S are the frequencies of the of the RF carrier and supply ripple, respectively. As previously noted, the A_{11}^1 operator is not fully symmetric in this representation because the supply noise and RF input signal follow substantially different paths to the output.

The A_{11}^1 operator is solved by including the cross terms in the Volterra series in (29). The resulting operator is shown in (39). Here, the A_{11}^1 operator is organized by splitting out the effects of the device parameters (gm_i, y_i, *etc),* and the effects of the first order operators which are lumped into parameters K_1-K_4. In (39), $y_2 = go_2 + j(\omega_a + \omega_b)C_2$ is the second order drain-source admittance, $y_S = (j(\omega_a + \omega_b)L_S)^{-1}$ is the source admittance, and constant K_0 in the denominator is evaluated at $j(\omega_a+\omega_b)$. The K_1, K_2, K_3, K_4, terms are frequency dependent transfer functions that are a function of the first order operators. These are shown in (40)-(43). Here, the frequency of the input RF signal is represented by ω_a and the frequency of suppy noise is represented by ω_b.

$$A_{11}^1(j\omega_a, j\omega_b) = y_S \frac{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4}{K_0}, \tag{39}$$

where

$$K_1(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[1 + A_{10}^1(j\omega_a) - 2A_{10}^2(j\omega_a)\right] - A_{01}^1(j\omega_b)\left[1 - A_{10}^2(j\omega_a)\right], \quad (40)$$

$$K_2(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[A_{10}^1(j\omega_a) - A_{10}^2(j\omega_a)\right] + A_{01}^1(j\omega_b)\left[A_{10}^2(j\omega_a) - A_{10}^1(j\omega_a)\right], \quad (41)$$

$$K_3(j\omega_a, j\omega_b) = A_{01}^2(j\omega_b)\left[1 - A_{10}^1(j\omega_a)\right], \text{ and} \quad (42)$$

$$K_4(j\omega_a, j\omega_b) = \quad A_{10}^2(j\omega_a)A_{01}^2(j\omega_b). \quad (43)$$

As seen in (39), upconversion of supply ripple results from second order nonlinearity in several of the device parameters. Major contribution to upconversion happens through second order nonlinearity of *output conductance (go_2)*, *drain junction capacitance (C_2)*, and *dependence of the forward transconductance on v_{ds} (gmo_{11})*. Source inductance provides degeneration and reduces the supply noise mixing. However, large values of source degeneration increase the contribution of *second order transconductance parameters (gm_2 and gmb_2)*. Source degeneration increases the effects of *gm_2 and gmb_2* because it provides a path for supply noise to modulate the current in the device through the source terminal. Without source degeneration, there is no path from the supply that can affect the gate-source potential of the device.

Following the derivation of (24) and (30), the *PSRR* can be written as $PSRR = dB\left|\frac{2A_{10}^1}{A_{11}^1}\right|$, in which case many of the terms in (33) and (39) are cancelled. The resulting expression

for the CMOS amplifier follows as:

$$PSRR = dB\left|\frac{gm_1}{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4}\right|. \quad (44)$$

In (44), the denominators in the expressions for A_{10}^1 and A_{11}^1 are cancelled. Also, there is no dependence on the signal amplitudes. This leaves straightforward dependency only on circuit variables, device parameters, and frequency. Consequently, the PSRR can be thought of as a signal independent circuit parameter and can be used to predict supply rejection for many input signals and noise levels.

The PSRR in (44) indicates which parameters make the circuit susceptible to supply noise. This makes it useful for amplifier configuration and design. High power supply rejection is achieved by limiting the effects of several circuit variables, while simultaneously increasing the forward transconductance. Specifically, to maximize PSRR, it is best to have a high ratio of gm_1 to all sources of second order nonlinearity at the drain terminal. To improve PSRR, the designer may take the following action:

- Increase gm_1 to achieve higher forward gain
- Reduce second order conductive nonlinearity (go_2) at the drain terminal, potentially with a longer channel-length device.
- Reduce the effects of nonlinear junction capacitances (C_2)
- Reduce the transconductance cross term (gmo_{11}) by shielding the drain terminal from supply noise

In many cases a cascode transistor may be highly effective at improving PSRR since it may shield the drain of the active transconductor from supply variation. The improvement may be limited to low frequencies, however, since the cascode will still have nonlinear junction capacitance, C_{jd}, affecting the output terminal.

4.6 Comparison to Measurement

A common-source class-A/AB power amplifier was designed and fabricated in 180nm CMOS to verify the distortion model and the spectral regrowth caused by power supply noise. The amplifier circuit consisted of thin oxide active NMOS devices with off chip matching to allow the frequency band to be adjusted in the laboratory. The amplifier was sized to achieve a maximum output power of 15dBm when driving a 50Ω load. The voltage gain of the packaged amplifier was designed to be approximately 10dB at 2.4GHz with the input matched to 50Ω and 300pH of inductive source degeneration due to bondwires and board interconnect. A current-mirror bias network was included on-chip to set the quiescent point for the amplifier.

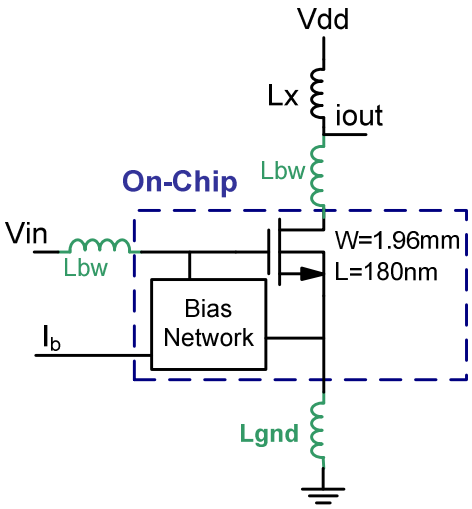


Figure 40. Common-source amplifier model

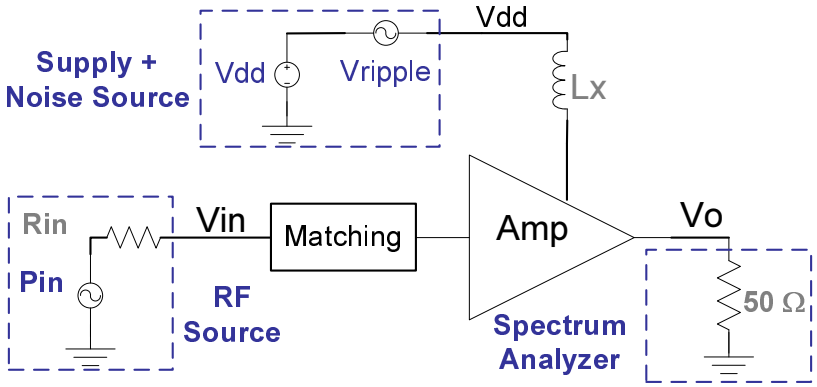


Figure 41. Laboratory test setup

Figure 40 shows the amplifier topology and bias network. Parasitic inductors are shown to represent the effects of the bondwires and printed-circuit-board trace inductance. Not shown are the blocking and bypass capacitors that are placed at the board level. Figure 41 shows the laboratory test setup. The test setup included voltage sources for biasing the amplifier, a variable RF signal generator, an arbitrary waveform generator to inject noise on the power supply, and a spectrum analyzer to measure the output harmonics. To minimize bondwire parasitics, the chip was bonded directly to the

board. A photo of the test IC bonded to the board is shown in Figure 42. Several downbonds to the ground plane were used to minimize the source inductance. The parasitic bondwire inductance was de-embedded with a network analyzer. Inductance at the input-output terminals was measured in the range of 2-4nH. Inductance between the source terminal and ground was de-embedded with s-parameter measurements and was confirmed to be less than 300pH due to multiple downbonds to the ground plane.

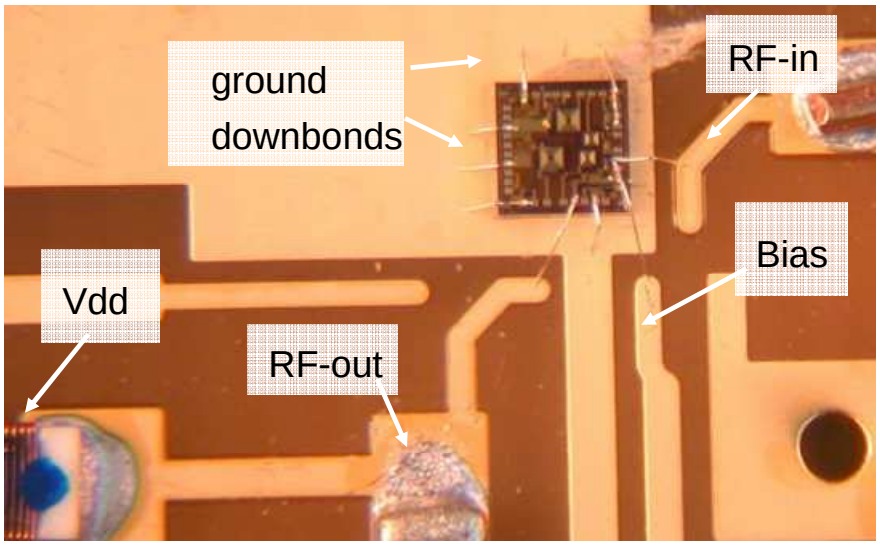


Figure 42. Photograph of the die bonded on the gold-plated test board. Die area is 1.4mmX1.4mm.

4.6.1 Sideband and PSRR Measurement

The input RF power was swept between -30dBm and 10dBm at a carrier frequency of 2.4GHz. Supply ripple was injected at a frequency of 1MHz with amplitude of 50mV to represent the first harmonic of the switching noise of a DC-DC converter. Figure 43 compares measured results to hand analysis. As predicted by the Volterra series analysis, the second order supply ripple sideband varies linearly with input power. At

low output power, the fundamental and sideband harmonics match hand analysis within 1-2 dB. At high output power the amplifier experiences moderate to strong nonlinearity as the drain voltage starts to clip. The PSRR is reduces in this case because of strong conductive nonlinearities in the CMOS device when it enters compression. In this case, higher order terms are needed to maintain the accuracy of the Volterra series analysis.

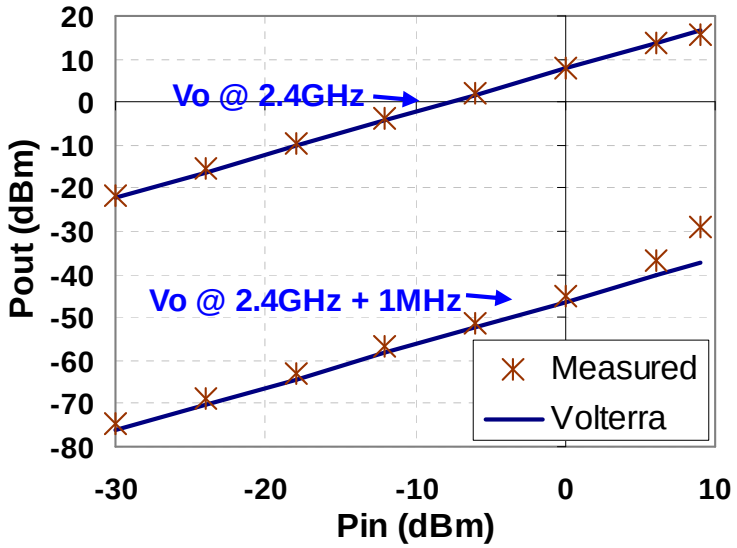


Figure 43. Comparison of measured and calculated fundamental and ripple sideband power

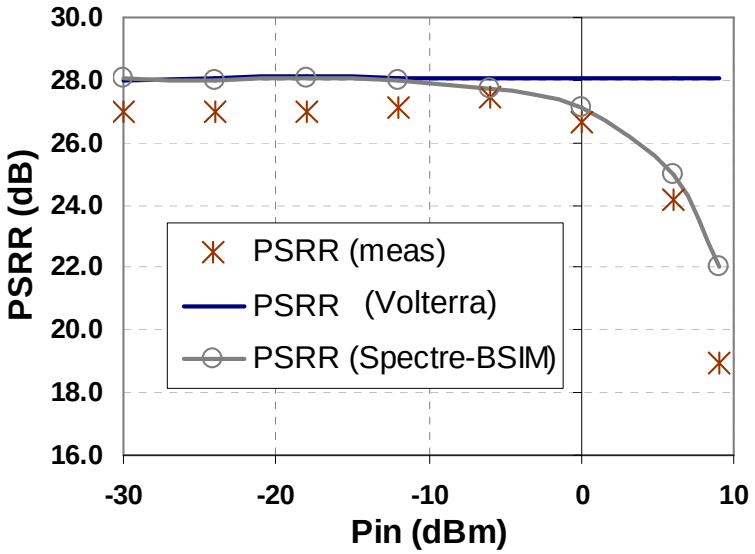


Figure 44. Comparison of measured and calculated ripple sideband in decibles-below carrier.

Figure 44 shows the PSRR of the amplifier versus input power. From (23), PSRR is related to the sideband (dBc) measurement as

$$PSRR(dBV) = Sideband(dBc) + SupplyNoise(dBV) \tag{45}$$

It is noted that this ratio should be constant and independent of the input signal level for constant supply noise levels. As described in section 4.3.2, this is a useful figure of merit for constant or worst case supply noise analysis and represents the sideband (in decibels below carrier - dBc) that would occur for a one-volt (zero-dBV) supply ripple magnitude. In Figure 44, this is also compared to the prediction in (44) using Volterra analysis as well as simulation in Spectre with BSIM3v3 models. Sideband power is seen to match hand analysis within 1-2dB for input powers less than 0dBm. Similar to Figure 43, the discrepancy between measured and calculated data increases as the amplifier enters saturation. The PSRR decreases in this case because the amplifier is more

susceptible to power supply noise. Simulated data matches well with hand analysis at low power, but deviates as the amplifier enters saturation. Simulated data also matches measured data within 1-3dB except at high power. The deviation is partly explained by variation in de-embedded values for circuit parasitics including inductive source degeneration. In Figure 43 and Figure 44, the Volterra series analysis is seen to be accurate over a 30dB range of output power. It is expected that this trend would continue to be accurate for input power less than -30dBm because the amplifier would remain in the weakly nonlinear regime.

4.6.2 Spectral Regrowth Measurements

Baseband I and Q signals were generated for 8-PSK EDGE with a symbol rate of 270kHz. The baseband signals were oversampled at 32 samples per symbol and saved in 1248-symbol-long data streams. Using the technique described in [68], the baseband signals were upconverted and applied to the Volterra model in the frequency domain to generate the predicted output spectrum. To study the generation of supply ripple sidelobes, only the first order direct and second order cross terms were used for the calculation. Spectral regrowth due to third order nonlinearity was not included because it is well treated in [68, 72] and is not dominant in supply ripple mixing.

The I and Q signals were upconverted and supplied to the CMOS amplifier in the laboratory using the National Instruments PXI-5421/5620 RF test system. To verify the model at different carrier frequencies, EDGE modulation was applied in the traditional

900MHz carrier range, and also at 2.4GHz. The output spectrum was measured and compared to the predictions of the Volterra analysis.

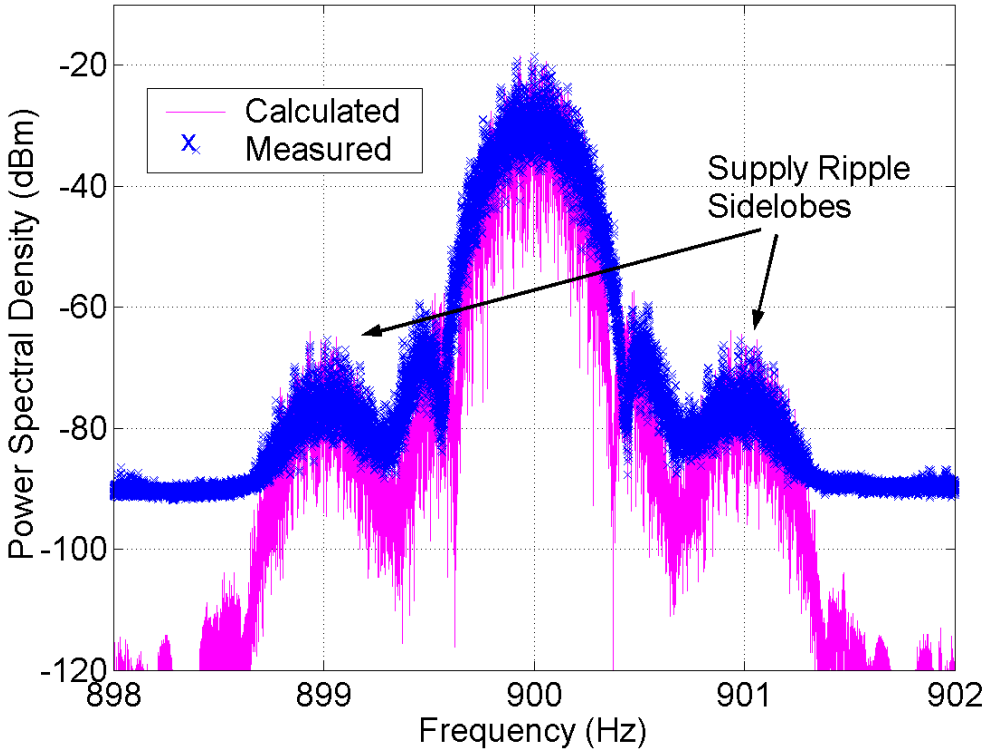


Figure 45. Measured versus calculated power spectral density at 900MHz

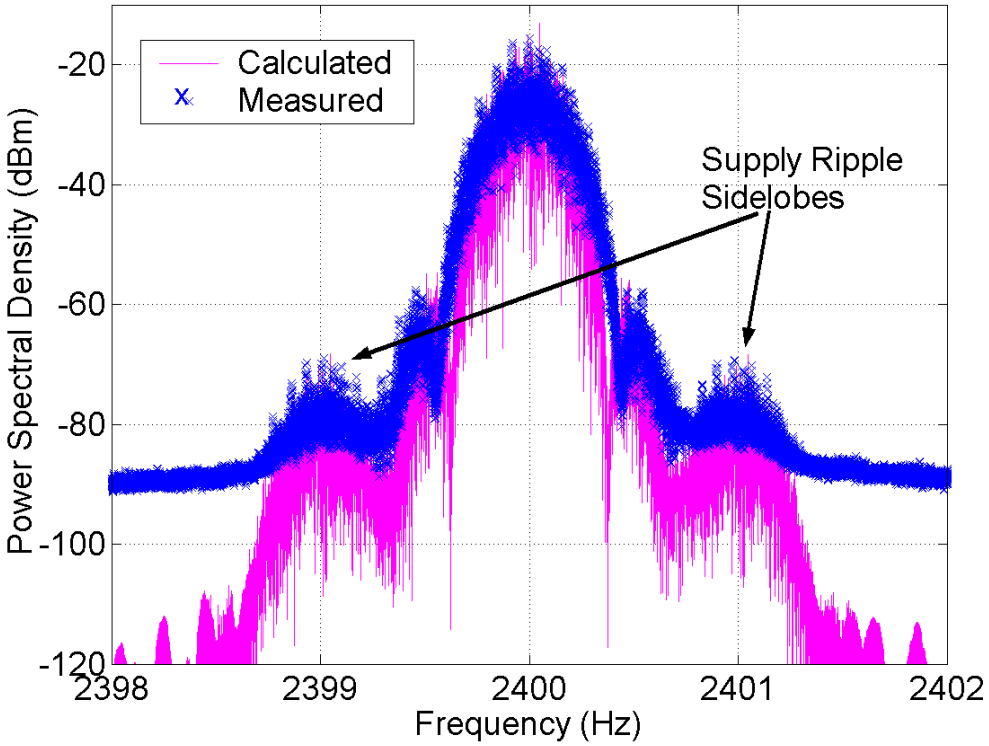


Figure 46. Measured versus calculated power spectral density at 2.4GHz

Figure 45 shows the measured output spectrum overlaid with the spectrum generated with multi-port Volterra-series analysis. The traditional EDGE spectrum is shown centered at 900MHz. Due to supply ripple injected at 1MHz, sidelobes appear centered at 899MHz and 901MHz. The sidelobes are images of the EDGE spectrum and have a peak at around 50dB below the main lobe. The calculated spectrum matches the measured spectrum within 1-3dB across the frequency range, demonstrating the accuracy of the multi-port Volterra model at 900MHz. Figure 46 shows similar spectral regrowth centered at 2.4GHz ±1MHz. In the Volterra series calculation case, the ripple sidelobes are clear since the noise floor is arbitrarily small. The measured data shows a

noise floor of -90dBm (for the settings used for the national instruments PXI downconverter), but the sidelobes are still clear and match the predicted spectrum within 1-3dB.

4.6.3 Power Supply Rejection Ratio: Component-Level Analysis

Importantly, the Volterra analysis provides a tool to study the device-level mechanisms for amplifier nonlinearity. The contribution of the circuit-level nonlinearities can be broken down, as shown in Figure 47. Here, the PSRR is shown for the three dominant sources of supply ripple upconversion: modulation of the forward transconductance by *Vdd* (gmo_{11}), second order output conductance (go_2), and second order drain junction capacitance (C2). In Figure 47, we are effectively plotting the *PSRR* as we add in the effect of dominant contributors to supply noise upconversion. It should be noted that when there is no source of supply noise upconversion, the PSRR is theoretically infinite. When the effect of gmo_{11} is added, PSRR is reduced from infinity to the edge of the shaded region in Figure 47.

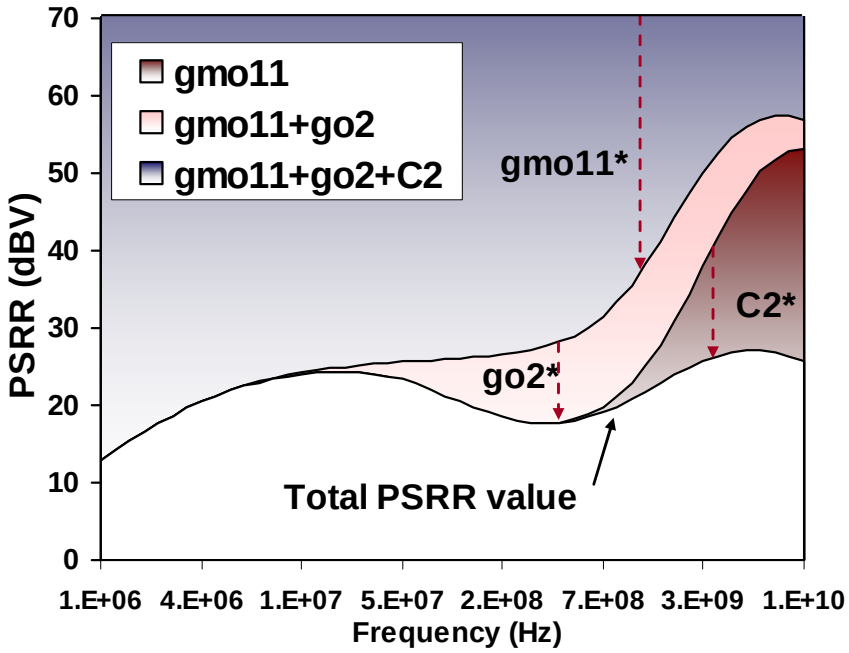


Figure 47. PSRR vs carrier frequency, from Volterra-series analysis, showing contributions of dominant circuit-level nonlinearities.

* Change in PSRR when effect of parameter is included (i.e. gmo_{11} is shown to reduce PSRR from infinite to the edge of the shaded region indicated in the legend).

At low frequencies the effect of reactive elements is minimal since they look like shorts (inductors) or opens (capacitors). Therefore, the dominant impact of supply noise is that it modulates the forward transconductance by changing the V_{ds} of the transistor (i.e. the gmo_{11} term from (31) dominates). This is shown by first nulling the effects of the second order drain-source admittance parameters, go_2 and C_2. When the effects of go_2 and C_2 are included, the PSRR drops at moderate to high carrier frequencies. The second order drain-source conductance (go_2 term) becomes important at frequencies where the output resistance of the active device is comparable to the impedance of the choke inductor. The nonlinearity of the drain junction capacitance (C_2

term) is important at high frequency when the drain capacitance dominates the output impedance of the device. The peaks in the PSRR curve are related to resonance of the choke and source inductance. At high frequency, the PSRR increases because of the increasing impedance of the inductive degeneration. However, this effect is partially reduced by the nonlinearity of the output junction capacitance, C_2. At low frequency, PSRR falls off with the impedance of the choke inductor because the forward gain is reduced. The effects of gm_2 and gmb_2 are only appreciable with high values of source degeneration. These terms are dominated by gmo_{11}, C_2, and go_2 in this example since there is only 300pH of inductive degeneration. An additional potential source of supply-carrier intermodulation is high impedance in the input signal path. This causes the supply voltage to couple through the C_{gd} directly modulating the gate terminal. For low frequency supply noise, the effect of C_{gd} coupling is small because the jwC_{gs} admittance is negligible. This effect is not included in (39)-(44) for simplicity, but can be captured by including the gate terminal as an additional node in the Volterra analysis.

As seen in Figure 47, Volterra series analysis provides a way to examine the performance of the circuit and design for robustness against power supply noise. In the common-source example, a cascode can increase PSRR substantially. The cascode topology increases the forward gain, and shields the drain of the active transconductance element from variations in Vdd. This reduces upconversion of supply noise through the gmo_{11}, go_2, and C_{gd} terms. Overall, this analysis demonstrates many benefits in providing insight into the circuit design procedure.

4.7 Conclusion

A method of predicting the interaction of power supply noise with the RF carrier was presented and compared to measured data. Conventional distortion analysis was extended to a multi-port formulation to predict supply ripple intermodulation with the RF signal. Relative measurement of ripple sideband power showed agreement within 1-2dBc of prediction. Spectral regrowth of the EDGE spectrum due to supply ripple upconversion at 900MHz and 2.4GHz was shown to match within 1-3dB. Multi-port Volterra analysis was confirmed to be a valuable tool to predict upconversion of supply noise over a range of frequency and signal input power. The analysis can dramatically reduce simulation time, as also discussed in [68], by converting lengthy time-domain simulation to narrowband frequency domain or mixed time-frequency domain computation. This can provide insight into the design of RF amplifiers to provide improved power supply rejection, more robust topologies for system-on-chip (SOC) solutions, and improved efficiency and performance of polar and envelope tracking (ET) power amplifiers.

Chapter 5 Optimum Operating Strategies for Hybrid Voltage Regulators

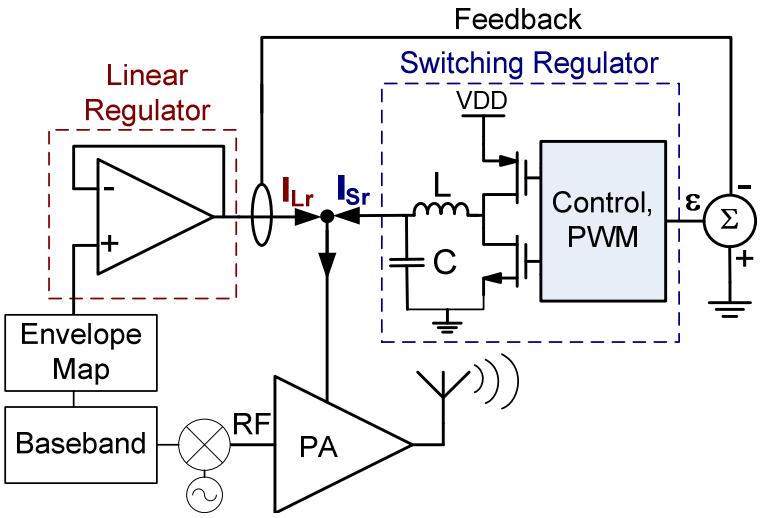


Figure 48. Traditional parallel linear-switching hybrid regulator topology

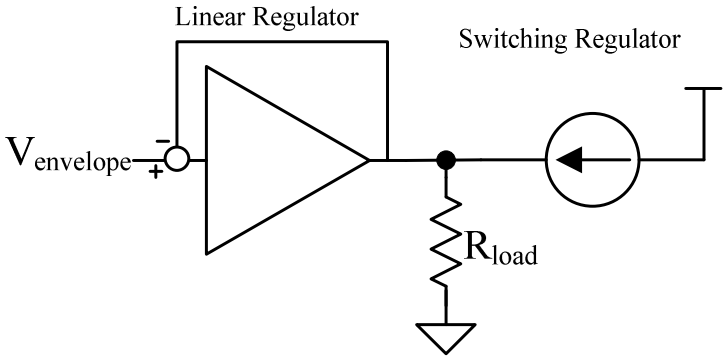


Figure 49. Model for parallel hybrid switching-linear regulator

5.1 Introduction

As discussed in Chapter 3, efficient regulation of the supply voltage can improve the average efficiency of power amplifiers in polar and envelope tracking architectures. This can improve battery life in portable communication systems, especially when the power

amplifier (PA) tends to operate at less than maximum power. Hybrid voltage regulators, such as the one shown in Figure 48, are particularly attractive for dynamic supply transmitter applications. These regulators exploit favorable properties of both linear and switching regulators to achieve high efficiency and fast dynamic response.

Figure 48 shows the parallel hybrid voltage regulator introduced in section 3.2.3. The linear regulator acts as a voltage follower, dynamically regulating the PA supply voltage. The switching regulator acts as a current source, appearing high impedance to the linear regulator, and supplying some nominal amount of the current delivered to the load. A simplified model of the parallel regulator is shown in Figure 49. In systems published in the literature, the switching regulator supplies the DC or average current to the load [77-79].

The parallel hybrid topology has advantages over the series hybrid configuration in that the linear regulator is not constrained by the dropout voltage on the active devices. In series hybrid regulators, the DC-DC converter creates a lower supply voltage for the pass transistor. This reduces losses in the linear regulator by keeping the active device in a low dropout condition at all times. However, when fast transients occur in the positive direction, it may be difficult for the series topology to maintain regulation. The active device can lose gain when the voltage headroom is less than the minimum dropout voltage (CMOS devices enter the triode region). The solution is to increase the bandwidth and/or slew rate of the DC-DC converter, but this may require increased switching frequencies among other compromises, and ultimately lower efficiency. An

additional solution is to place a shunt transistor to connect the linear regulator supply to the battery in this situation, but that may also result in additional power loss. The parallel hybrid solution can tolerate high slew conditions in both positive and negative directions, and as we will show, can be efficient for a wide range of operating conditions.

In parallel hybrid regulators, high gain-bandwidth linear regulators can provide fast voltage regulation with a high dynamic range [13, 52, 54], while properly designed switching regulators can achieve high efficiency for a large range of conversion ratios and load conditions [80, 81]. Because of the benefits of the combined solution, hybrid regulator topologies have been proposed for both transmitter applications [61, 62, 82], and high-efficiency audio amplifiers [83, 84]. In audio applications, low signal bandwidth makes the hybrid topologies less attractive compared to pure switching regulator (class-D) topologies, which have been shown to achieve high efficiency and excellent fidelity [85-87]. However, in transmitter applications, high envelope bandwidths make class-D solutions less attractive due to losses associated with high switching frequencies [36, 45, 47, 50]. In this case, hybrid topologies are practical because they can eliminate the tradeoffs among efficiency, bandwidth, and spectral fidelity [61, 62].

For the topology shown in Figure 48, several control methodologies have been proposed to combine the outputs of the two different regulator blocks. The linear regulator is typically used as a follower stage that supplies a buffered version of the

reference voltage to the regulator output. Local feedback around the linear stage is used to reduce output impedance and improve accuracy. The bandwidth of the system is determined by the gain-bandwidth product of the linear regulator which can be on the order of many tens of MHz in modern semiconductor processes [52, 54]. If the linear regulator is designed with high closed loop bandwidth, it can be used to attenuate switching harmonics from the DC-DC converter stage [83, 84], and can also supply a portion of the dynamic power of the envelope signal. Traditionally, to achieve the desired control, the output current of the linear regulator is sensed and is used as an error signal for the switching regulator. In work reported in the literature, the switching regulator forces the average or DC linear regulator current to zero with linear (proportional-integral) control, [61], or hysteretic control, [82]. The switching regulator can also have a non-zero bandwidth and supply some of the dynamic power. A method to determine the optimum bandwidth of the switching stage through simulation is proposed in [62].

5.2 Overview

This Chapter discusses the parallel hybrid topology in the context of dynamic voltage regulation for RF power amplifiers. We expand on the work in [61, 62, 82-84] with particular emphasis on the optimum bias condition. In our approach we assume that the switching regulator operates as a quasi-static current source. This assumption is valid under the practical condition that the envelope frequency is much higher than the

bandwidth of the switching regulator. This work does not consider directly the topic of the switching regulator providing part of the *AC* current to the load. Instead we generalize the analysis by treating the switching regulator current as quasi-static. In this case, by changing the time window of the quasi-static analysis, the switching regulator current can be optimized for higher frequency situations.

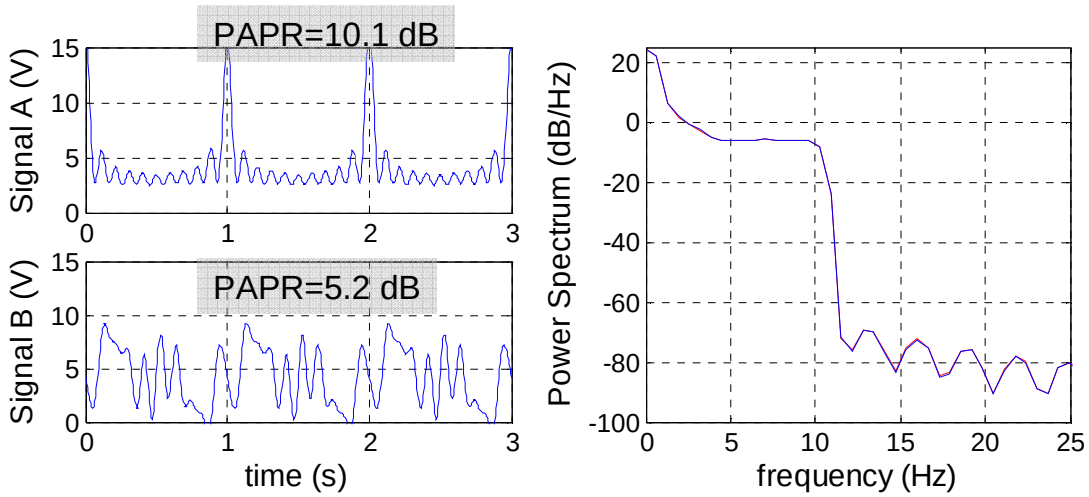


Figure 50. Two different time-domain envelope signals that share the same power spectrum: one with peak-average power ratio (PAPR) of 10.1dB, and another with PAPR or 5.2dB.

This analysis is based in the time domain as opposed to the frequency domain approach in [62]. Frequency-domain analysis is difficult in this case because many time domain signals can have the same power spectrum. An example of this is shown in Figure 50. Here, two different envelope signals are shown that have the same power spectrum. The difference is that one has a peak-average power ratio (PAPR) of 10.1dB, while the other has PAPR or 5.2dB. It is clear that a solution that is optimized for the first scenario may not be ideal for the second. This may lead to sub-optimal efficiency if

the switching regulator is optimized for bandwidth alone without consideration of the time-domain operating conditions.

In our analysis, we derive expressions for the optimum switching regulator current as a function of the supply voltage, the average output voltage, and dynamic characteristics of the envelope signal. The optimization is based on the conduction angle of the linear regulator output stage. It is shown that there is an optimum efficiency for such a configuration, and that the optimum switching regulator current varies with the power of the signal. We verify some of the conclusions of [61, 62, 82], but show that a higher efficiency methodology is possible that involves scheduling the current provided by the switching regulator. Importantly, we show that for maximum efficiency, the optimum quasi-static switching regulator current may be more than the DC current to the load. We verify our predictions with measured data and demonstrate the benefits of optimum quasi-static biasing for representative wireless communication standards including IS-95 CDMA and IEEE 802.11a/g.

5.3 Optimum Bias Point: Model and Calculation

To reduce voltage ripple, switching regulators must tradeoff transient response and/or efficiency by increasing the size of the filter components or increasing the switching frequency [45, 55]. Linear regulators, on the other hand, may provide spectral purity and high gain-bandwidth product, but have low power efficiency, especially at low conversion ratios. The hybrid topology can decouple efficiency from transient

response and voltage ripple, allowing the performance of a linear regulator with less power consumption.

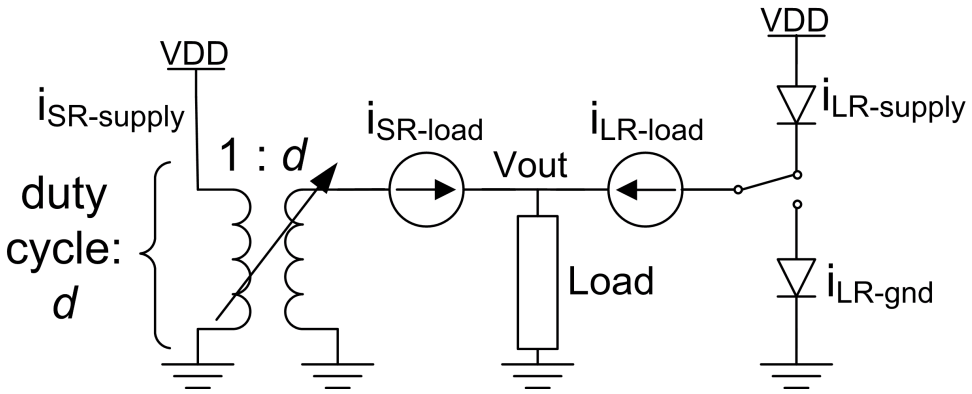


Figure 51. Proposed hybrid switching regulator model

Here the switching regulator is modeled as a quasi-static current source with average conversion ratio, *d*, between the load current and the current drawn from the supply. As shown in Figure 51, it is assumed that the switching regulator operates as an ideal transformer and has zero bandwidth over some finite time window. The average voltage across the inductor must be zero, so duty cycle is constrained to be the ratio of the average output voltage to supply voltage:

$$d = \frac{\langle V_{out} \rangle}{V_{dd}}, \tag{46}$$

where $\langle V_{out} \rangle$ is the average output voltage over some time window $a \le t \le b$, and $\langle f(t) \rangle = \frac{1}{b-a} \int_a^b f(t)dt$. For periodic *f(t)* with period *T*, *a* and *b* may be taken as *nT* and *(n+1)T* for integer *n* to reflect integration over one full period of the envelope signal.

The linear regulator is modeled as an ideal class B topology, with a push-pull rail-to-rail output stage. It can be verified that this is typically the most efficient output stage for

signals of interest [40]. With a push-pull output stage, all current sourced to the load comes from the supply, all current drawn from the load sinks to ground. For periodic modulation waveforms, the conduction angle of the linear regulator will be defined as the radial angle in degrees that the regulator draws current from the supply. The conduction angle can change because the current of the two regulator blocks is summed at the output. The switching regulator can source any portion of the average current. This allows the linear regulator to operate with any conduction angle between 0-360 degrees. The optimum bias point and conduction angle are derived based on average efficiency,

$$\langle \eta \rangle = \frac{\langle P_L \rangle}{\langle P_S \rangle}, \tag{47}$$

where $\langle P_L \rangle$ is the average power to the load and $\langle P_S \rangle$ is the average power from the supply. Assuming an ideal situation as in Figure 51, the average power from the supply follows from:

$$\langle P_S \rangle = V_{DD} \cdot \left[\langle i_{LR} \rangle + \langle i_{SR} \rangle \cdot d \right], \tag{48}$$

where i_{LR}, and i_{SR} are the linear and switching regulator currents delivered to the load, *d* is the duty cycle, and V_{DD} is the supply or battery voltage. To calculate average efficiency it is necessary to derive or measure average currents, $\langle i_{LR} \rangle$ and $\langle i_{SR} \rangle$. For simple envelope waveforms, such as sinusoidal AM and two-tone RF signals, expressions for (47) and (48) can be derived explicitly based on characteristics of the regulated voltage signal and the supply or battery voltage. It should be noted that while the

calculation in (48) is proposed for the ideal situation, the concept extends to real switching and linear regulator components that include realistic loss mechanisms. Also, for the calculations presented in section 5.4, the load is assumed to be linear and resistive. Real power amplifier loads may be nonlinear and reactive. This can complicate the calculation of average efficiency, but does not reduce the utility of the optimization procedure. The explicit calculations for the sinusoidal-AM and two-tone cases are presented as an example to highlight the benefits of optimum quasi-static biasing. For cellular and wireless internet standards, such as CDMA, UMTS and the 802.11 standards, hand calculations are difficult due to the non-periodic nature of the envelope waveform. However, assuming $\langle i_{LR} \rangle$ and $\langle i_{SR} \rangle$ can be measured, the optimum bias point can still be determined, as will be presented in section 5.6. Therefore, regardless of the complexity of the envelope waveform and losses in the switching and linear regulator components, there is significant value in optimizing the relative current contribution of the regulator stages.

5.4 Efficiency Optimization: Sinusoidal and Two-Tone Carrier Modulation

Envelope signals that result from explicit modulation of the RF carrier may allow direct solution of optimum biasing expressions. For the case of sinusoidal amplitude modulation of the RF carrier, the envelope voltage and current waveforms may be written as

$$v_o(t) = v_{DC} + v_a \cdot \cos(wt), \text{ and}$$
$$i_o(t) = i_{DC} + i_a \cdot \cos(wt). \tag{49}$$

Here, v_o and i_o are the output voltage and current respectively, v_a and i_a are the voltage and current amplitudes, and v_{DC} and i_{DC} are the DC values. In (49), and in the rest of this work, the load is assumed to be linear and resistive although reactive and nonlinear loads can be treated in a similar manner.

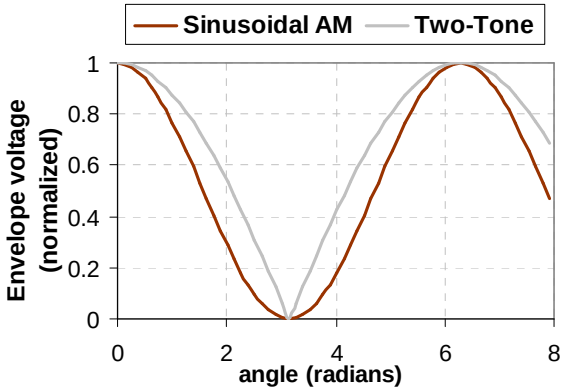


Figure 52. Envelope Waveforms: Sinusoidal AM and 2-tone modulation

Figure 52 shows normalized versions of the envelope signal for sinusoidal-AM and two-tone modulation of the carrier. In the sinusoidal-AM case the amplitude modulation is such that $v_a = v_{DC}$. The average power delivered to the load is, therefore,

$$\langle P_L \rangle = \frac{1}{T}\int_0^T v_o(t) \cdot i_o(t)dt = v_{DC} \cdot i_{DC} + \frac{v_a \cdot i_a}{2}. \tag{50}$$

To derive an expression for the average power drawn from the supply, as in (48), the value for $\langle i_{LR} \rangle$ is solved by assuming that i_{SR} is constant during the period of the

envelope signal, and finding the corresponding conduction angle, 2Φ, that the linear regulator conducts current from the supply.

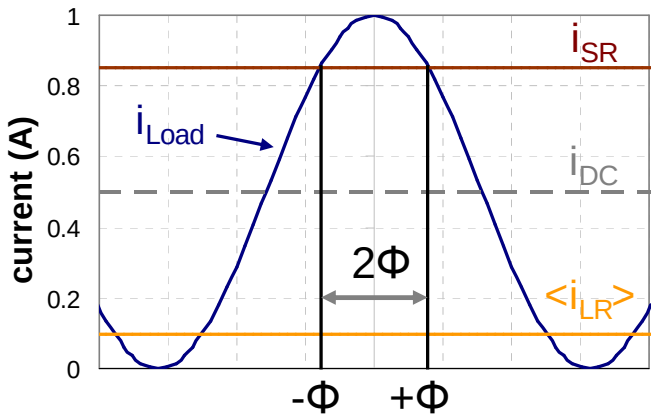


Figure 53. Conduction angle derivation: Sinusoidal AM modulation, normalized peak load current = 1A

Figure 53 shows a diagram of the current waveforms in the hybrid regulator. If the switching regulator supplies the DC current, the conduction angle of the linear regulator is exactly 180°. This would mean that in the push-pull output stage, the device that couples the output to the supply conducts half of the time. However, in the example shown in Figure 53, the switching regulator supplies more than the DC current such that 2Φ<180°. The net effect is that the average linear regulator current is reduced by the switching regulator current. For the waveform in (49), Φ can be solved for as

$$\Phi = \cos^{-1}\left(\frac{i_{SR} - i_{DC}}{i_a}\right). \tag{51}$$

Based on (51), the average linear regulator supply current can be written in terms of conduction angle as

$$\begin{aligned}\langle i_{LR}\rangle &= \frac{1}{2\pi}\int_{-\Phi}^{\Phi}(i_{DC} + i_a \cdot \cos(\phi) - i_{SR})d\phi \\ &= \frac{i_a}{\pi}[\sin\Phi - \Phi\cos\Phi].\end{aligned} \tag{52}$$

Here, the average linear regulator current is only a function of the amplitude of the load current swing and the conduction angle. The average efficiency for the ideal system, as in Figure 51, can be written in terms of the properties of the envelope waveform using (46), (48), and (52), specifically noting that the current the switching regulator draws from the supply is reduced by conversion ratio, *d*. It should be noted that (52) assumes an ideal switching regulator with no loss. Average efficiency for the sinusoidal AM envelope follows as

$$\langle\eta\rangle = \frac{v_{DC}\cdot i_{DC} + \frac{v_a \cdot i_a}{2}}{i_{SR}\cdot v_{DC} + V_{dd}\frac{i_a}{\pi}[\sin\Phi - \Phi\cos\Phi]}. \tag{53}$$

In (53), average efficiency is written purely in terms of properties of the envelope waveform, the supply voltage, and the conduction angle, 2Φ, of the linear regulator. Substituting (51) into (53), average efficiency is expressed as a function of the current supplied by the switching regulator, i_{SR}. Using this result, an algebraic minimization can be done to find the switching regulator current that provides maximum average efficiency. This is the solution to $\frac{d\langle\eta\rangle}{di_{SR}} = 0$, and can be found as

$$i_{SR}^{*} = i_{DC} + i_a \cdot \cos\left[\pi\frac{v_{DC}}{V_{dd}}\right], \tag{54}$$

where i_{SR}^{*} is the optimum quasi-static switching regulator current. The maximum average efficiency, $\langle\eta\rangle^{*}$, for this value of i_{SR}^{*} is expressed as

$$\langle\eta\rangle^{*} = \frac{v_{DC}\cdot i_{DC} + \frac{v_a \cdot i_a}{2}}{v_{DC}\cdot i_{DC} + V_{dd}\frac{i_a}{\pi}\sin\left(\Phi^{*}\right)}, \tag{55}$$

where Φ^{*} is the optimum conduction angle for the linear regulator, and can be written as

$$\Phi^{*} = \pi\frac{v_{DC}}{V_{dd}}. \tag{56}$$

As seen in (54), the optimum current supplied by the switching regulator is *not* necessarily equal to the DC current supplied to the load, but is in fact a function of the DC and dynamic characteristics of the envelope signal as well as the supply voltage. This is a departure from the control schemes presented in [61, 82], where the mean switching regulator current is the DC load current.

The calculation is similar for two-tone signals, except different expressions are obtained for the conduction angle and optimum biasing conditions. For the case that the RF carrier consists of two tones at different frequencies, w_2 and w_1, but equal magnitudes, *va*, the envelope is a full-wave rectified sinusoid with a peak value of $2\times va$, as in [62],

$$v_{env} = \left|2\cdot v_a\cos\left(\frac{w_2 - w_1}{2}t\right)\right|. \tag{57}$$

In this case, the conduction angle as a function of the switching regulator current is

$$\Phi = \cos^{-1}\left(\frac{i_{SR}}{2i_a}\right), \tag{58}$$

where $i_a = \frac{v_a}{R_{load}}$ is the amplitude of the current swing of one of the two tone signals.

Following a similar procedure to the sinusoidal envelope signal, the optimum quasi-static switching regulator current contribution for the two-tone case is

$$i_{SR}^{*} = 2 \cdot i_a \cdot \cos\left(2\frac{v_a}{V_{dd}}\right), \tag{59}$$

where V_{dd} is the supply or battery voltage. The maximum average efficiency for the two-tone envelope signal is solved for as

$$\langle \eta \rangle^{*} = \frac{\pi}{2} \frac{v_a \cdot i_a}{v_a \cdot i_{SR} + V_{dd} \cdot i_a \cdot [\sin(\Phi) - \Phi\cos(\Phi)]}. \tag{60}$$

For the two-tone case, ideal output efficiency is bounded between 93.3% for rail-rail modulation, and 78.5% ($\pi/4$) as $v_a \to 0$. In theory if the switching regulator supplied the DC current, efficiency would be bounded by 92.7% to 0%. This range fits with the efficiency of 87% for a two-tone envelope as reported in [62].

5.5 Theoretical predictions and Discussion

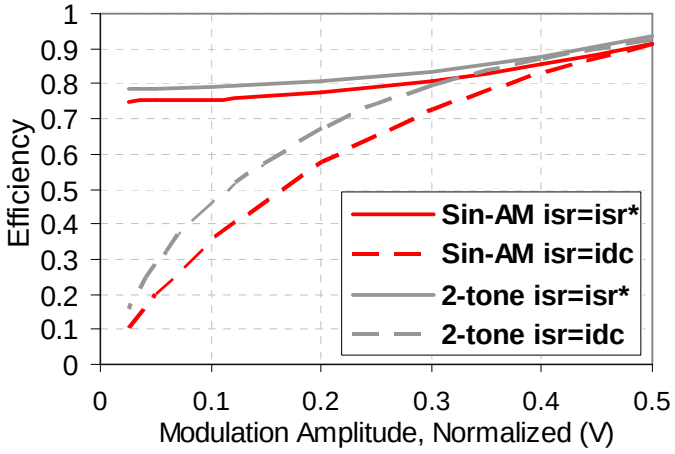


Figure 54. Theoretical efficiency vs voltage amplitude: sin-AM and two tone cases, following (55) and (60)

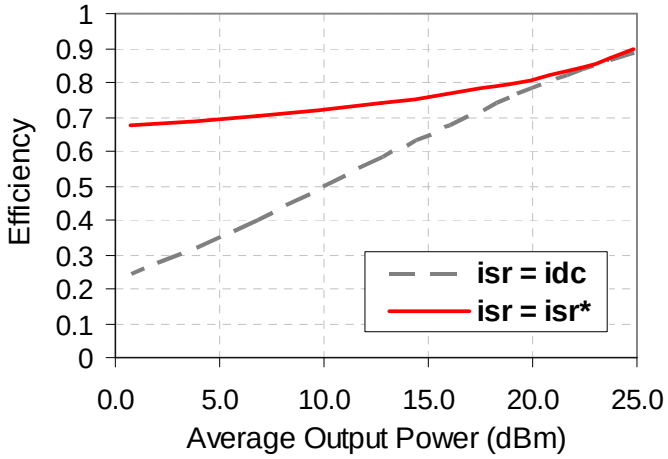


Figure 55. Efficiency vs normalized voltage amplitude: IS-95 CDMA, from simulation

Figure 54 shows the theoretical average efficiency for the sinusoidal-AM and two-tone modulated carrier as the modulation amplitude is reduced. The supply voltage is normalized to 1V, and the modulation amplitude is swept from rail-to-rail swing to nearly zero amplitude. For the sinusoidal AM signal, the carrier is fully modulated such that $v_a = v_{DC}$. The two-tone case assumes two signals at different frequencies with the same amplitude, v_a, as in (57). If the switching regulator contributes the DC load

current, average efficiency falls off to 0% as the modulation amplitude is reduced. However, if the switching regulator supplies the optimum current, i_{SR}^{*}, as derived in (54) and (59), the average efficiency can be kept higher across the entire range of operation, as follows from (55) and (60). Therefore, the preferred approach is to regulate the DC switching regulator current to the optimum value rather than the DC value. Intuitively, this can be explained based on the operation of the linear regulator:

- At high output swing levels, the switching regulator supplies the DC current. In this case the linear regulator operation approaches class B, or 180^{0} conduction angle for each push-pull output device. This causes the curves in Figure 54 to converge for high amplitudes.
- At low output swing the switching regulator sources more than the DC current, such that, for the sinusoidal-AM case, $\lim_{ia \to 0} i_{SR} = i_{DC} + i_a$. In other words, the high side pass transistor operates in class-C with the transistor conducting for less than 180^{0}. Alternatively, the low side pass transistor approaches class-A operation, drawing current only from the switching regulator output.

The trend shown in Figure 54 is also observed for real wireless communication standards. Figure 55 shows efficiency versus output power for envelope waveforms that correspond to IS-95 code-division multiple-access (CDMA). In this case the envelope waveform follows a bandlimited pseudorandom trajectory and is difficult to quantify for hand analysis. Therefore, in Figure 55, the curves are simulated with

behavioral models for the ideal case. Optimum i_{SR}^{*} values are determined empirically through simulation. The efficiency range for the CDMA waveform is similar to the curves in Figure 54. This is because the sinusoidal-AM, two-tone and CDMA waveforms have similar peak-to-average power ratio (PAPR). PAPR is a measure of the amount of amplitude modulation in the signal and can quantify the difference between the extremes in the envelope voltage and the average envelope voltage [21, 32, 88]. Generally, higher PAPR values will lead to lower efficiency. This is because the dynamic output voltage may deviate further from the average output voltage reducing the efficiency of the linear regulator.

The difference in average efficiency between the optimum case where $i_{SR} = i_{SR}^{*}$, and the traditional case where $i_{SR} = i_{DC}$ becomes more pronounced with increasing power backoff. In the case where $i_{SR} = i_{DC}$, average efficiency approaches zero as the output power level is reduced. However, in the optimum case, the efficiency of the hybrid regulator falls asymptotically towards some minimum efficiency level, $\langle \eta \rangle_{\min}$. For the cases presented in Figure 54, $\langle \eta \rangle_{\min}$ is between 70-80%. Even in the CDMA case, $\langle \eta \rangle_{\min}$ = 68%. Therefore, in situations with extreme power backoff, or when the battery voltage is much higher than the voltage required by the PA, optimum biasing can be highly advantageous. Next generation wireless standards will have power backoff ranges of up to 80dB [89]. In addition, scaling trends in modern silicon-based power amplifiers will dictate supply voltages well below current lithium-ion battery cell

voltages [44]. Both trends will result in significant power savings with the proposed biasing method.

Table III.

EXPRESSIONS FOR OPTIMUM BIASING AND EFFICIENCY FOR DIFFERENT ENVELOPE SIGNALS

	Sinusoidal AM *	**Two-tone ****	**IS-95 CDMA *****	**802.11a/g WLAN *****
i_{SR}^{*}	$i_{DC} + i_a \cdot \cos\left(\Phi^{*}\right)$	$2 \cdot i_a \cdot \cos\left(\Phi^{*}\right)$	-	-
Φ^{*}	$\pi \frac{v_{DC}}{V_{dd}}$	$2\frac{v_a}{V_{dd}}$	-	-
$\langle\eta\rangle^{*}$	$\frac{v_{DC} \cdot i_{DC} + \frac{v_a \cdot i_a}{2}}{v_{DC} \cdot i_{DC} + V_{dd}\frac{i_a}{\pi}\sin\left(\Phi^{*}\right)}$	$\frac{\pi}{2}\frac{v_a}{V_{dd}\sin\left(\Phi^{*}\right)}$	-	-
$\langle\eta\rangle_{\max}$	$\frac{3\pi}{2\pi+4} = 91.7\%$	$\frac{\pi}{4\cdot\sin(1)} = 93.3\%$	90%	75%
$\langle\eta\rangle_{\min}$	$\frac{3}{4} = 75\%$	$\frac{\pi}{4} = 78.5\%$	68%	50%

* Assume full modulation: $v_a = v_{DC}$ ** Assume two tones with same amplitude, *va*

*** Efficiency boundaries found with simulation

Table III consolidates the optimum bias point expressions and values for average efficiency for the sinusoidal-AM and two-tone cases. The average efficiency boundaries for CDMA and 802.11a envelope waveforms are also shown. For the cellular and wireless internet standards, efficiency boundaries and optimum switching regulator current contribution, i_{SR}^{*}, are found through behavioral simulation. Similar to the results shown in Figure 54, significant power savings are achieved by using the optimum current, rather than the DC current.

5.6 Experimental Results and Comparison to Theory

A prototype was created to verify the biasing model and compare predictions to experimental results. A first set of experiments was performed to confirm the optimum switching regulator current contribution, i_{SR}^{*}, as in (54). This was done by sweeping the switching regulator current and determining the maximum efficiency. A second set of experiments compared the maximum efficiency for the case where $i_{SR} = i_{SR}^{*}$ to the case where the switching regulator supplied the DC current, $i_{SR} = i_{DC}$. In the second set of experiments, measurements were taken for a range of output signal amplitudes to verify the predictions of (55) and (60). This was done for the sinusoidal-AM and two-tone modulation cases as well as for real communication standards, which included IS-95 CDMA and IEEE 802.11a wireless internet standards.

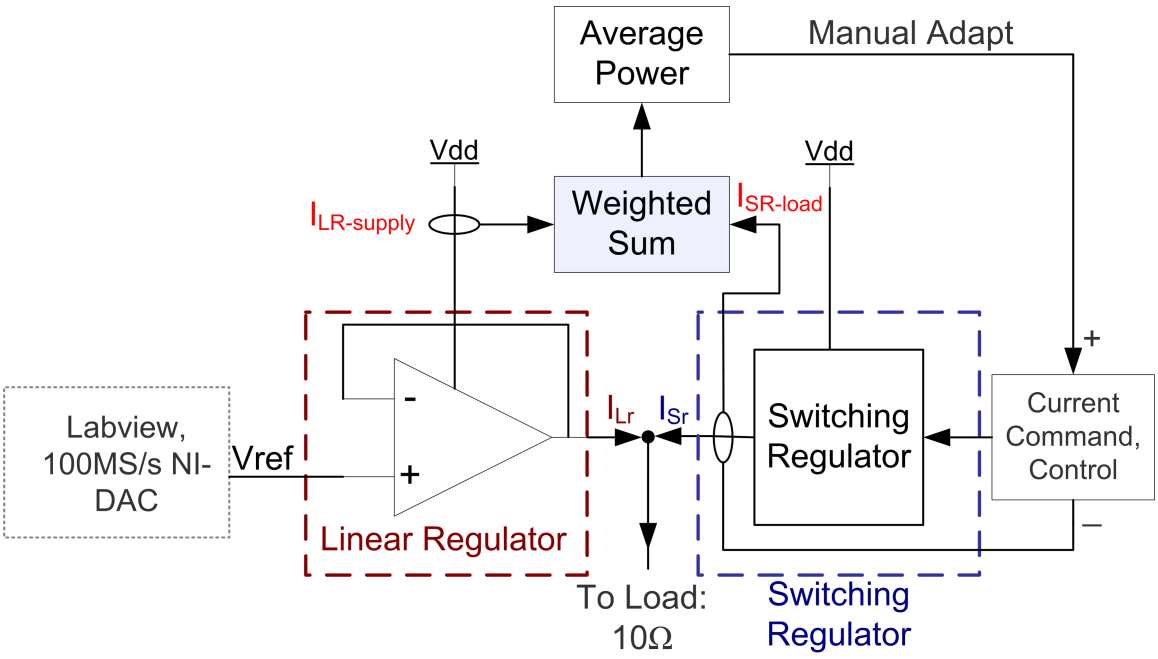


Figure 56. Experimental setup

The prototype was implemented at the board level with discrete components. A fast operational amplifier (LM7171) driving a class-B common-collector buffer stage (SS8050/8550) was used for the linear regulator. The switching regulator was operated as a voltage-controlled current source using a large, low-loss inductor. In this set of experiments, the switching regulator current was regulated manually at low frequency to control the DC currents from the two regulators. It should be noted that a more advanced implementation could use conventional current-mode control to regulate the switching regulator current as higher bandwidths. Such control methods are well developed in [55, 59, 90] as well as many other references and commercial products.

The experimental efficiency, to be compared to (55) and (60), was calculated as the sum of the average linear regulator current from the supply and the weighted output current of the switching regulator. To verify the ideal expressions in Table III, the switching regulator current was weighted by the factor, d, as in (46), to reflect lossless DC-DC voltage conversion. Lossless conversion was assumed to verify the ideal maximum efficiency case. To further reflect the ideal case, the bias current of 6mA of the linear regulator was not included in the calculation.

As shown in Figure 56, the input signal representing the dynamic envelope trajectory was delivered by a National Instruments D/A converter running at 100MS/s. The Labview software interface was used to generate and supply envelope waveform signals with up to a 20MHz bandwidth, including IS-95 CDMA and 802.11a WLAN wavefoms.

The switching regulator current command was adjusted manually to achieve the highest average efficiency for a given input signal. To simplify the experimental setup, a resistive load was used rather than an actual PA. In this case a 10Ω resistor was used for the load. The average currents from the parallel switching and linear blocks were measured with digital-multimeters.

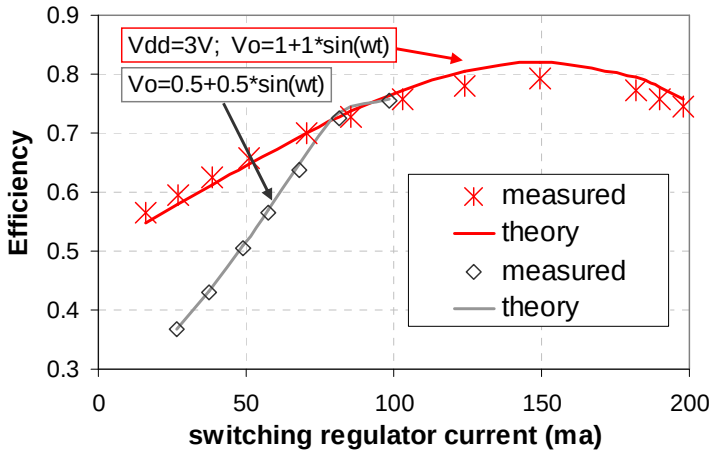


Figure 57. Average efficiency vs switching regulator current contribution: Sin-AM modulation

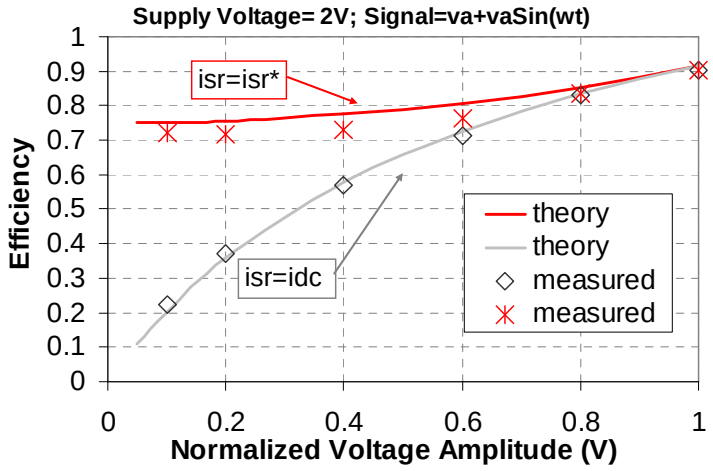


Figure 58. Average efficiency vs envelope modulation amplitude: Sinusoidal AM modulation.

Figure 57 shows average efficiency versus the current contribution of the switching regulator for 2 amplitudes of the sinusoidal-AM waveform. The results are compared to the predicted curve from (54) for a supply voltage of 3V. To compare the efficiency for the ideal situation, the 6mA DC bias current of the linear regulator (LM7171) was not included in the calculation. The average voltage delivered to the load for the two curves was 500mV and 1V, corresponding to power levels 14dB and 8dB below maximum power. Efficiency versus switching regulator current is seen to be in good agreement with theory. For the sinusoidal-AM waveforms shown, the peak efficiency is around 80%, which is 2% below the ideal efficiency as predicted in (55).

Similar curves were mapped out for amplitudes varying between $1/20^{th}$ the supply voltage and rail-to-rail swing. The results corresponding to optimum biasing are shown in Figure 58 for the sinusoidal-AM case. The measured data are overlaid with the theoretical predictions from Table III. Also shown in Figure 58 is a comparison of the optimum case where $i_{SR} = i_{SR}^{*}$, and the traditional case where $i_{SR} = i_{DC}$. For high amplitudes, the agreement between theory and measurement is good. At lower amplitudes, measured efficiency is less than predicted due to extra bias power in the class-B output stage and tolerance in setting the bias current of the switching regulator. The efficiency when the switching regulator supplies the DC power matches theory with good agreement across the range of operation.

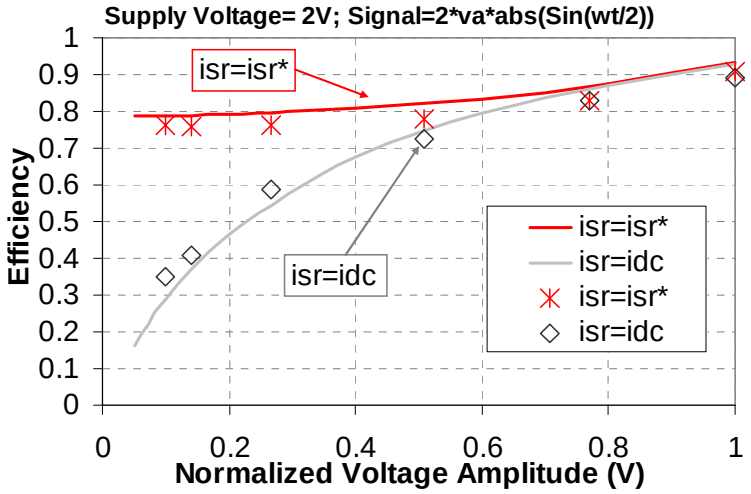


Figure 59. Two-tone modulation: comparison of theory to measurement

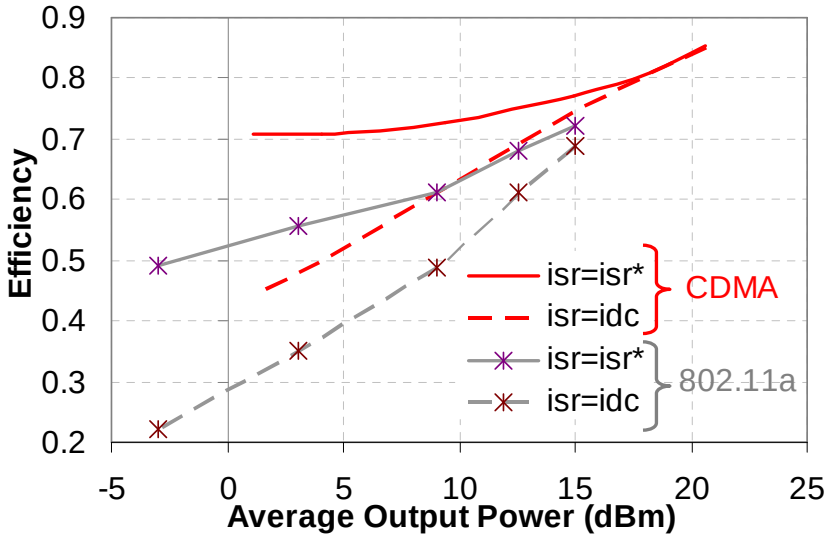


Figure 60. IS-95 CDMA, 802.11a WLAN measured efficiency

Figure 59 shows measured theoretical data for the two-tone modulated signal as analyzed in section 5.4 and summarized in Table III. The measured data are in good agreement with theory, and match with similar accuracy as the sinusoidal-AM case. The maximum efficiency for full-scale modulation is seen to be 90.6% compared to 93.3% as predicted in Table III.

Figure 60 shows measured results for CDMA and IEEE 802.11a supply modulation waveforms. These waveforms are generated with the Agilent *Advanced Design Systems* (ADS) software and converted to a format suitable for data conversion. The waveforms were delivered to the hybrid regulator with Labview and the NI 5421 DAC, as shown in Figure 56. The x-axis shows *average power* delivered to the 10Ω load. In this set of experiments the maximum *average power* delivered in the CDMA waveforms was just over 20dBm. The 802.11a waveforms were set to reflect a datarate of 54 MB/s, such that maximum *average power* was 15dBm. The higher peak-average power ratio (PAPR) of the 802.11a standard (PAPR=10.8dB) is the principal reason that average efficiency is lower than the other waveforms. The higher PAPR of 802.11a indicates that the dynamic output voltage deviates substantially from the average voltage. This reduces the average efficiency of the linear regulator. In the CDMA case, Figure 60 can be compared to the simulated results shown in Figure 55. The x-axis power scale is slightly different in the two plots because the simulation was run with a 3.3V supply voltage and a max output power of 1W.

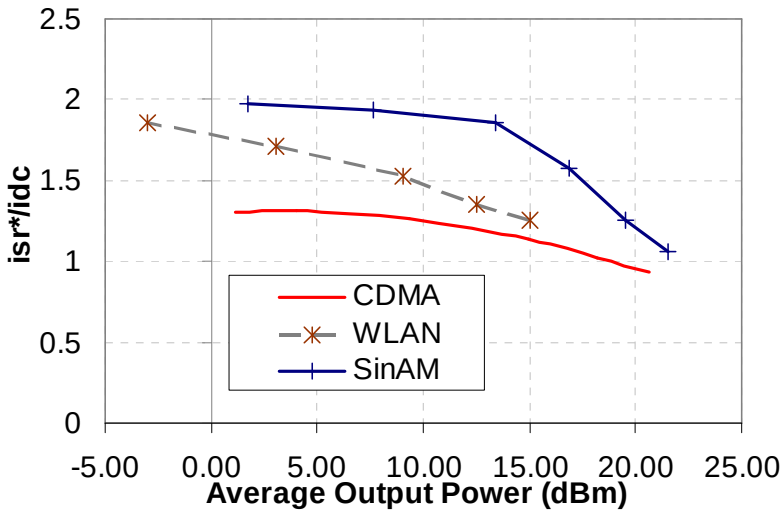


Figure 61. Optimum switching regulator current (normalized i_{SR}^{*} / i_{DC}) vs output power

Figure 61 shows the relationship between optimum switching regulator current and output power by plotting the ratio of i_{SR}^{*} / i_{DC} for several envelope signals. At high output power the Sinusoidal-AM and CDMA optimum current is nearly the same as the DC current. The WLAN optimum current is higher at maximum power because the signal has higher PAPR. In all cases, the optimum current increases as output power decreases. In the sin-AM case i_{SR}^{*} approaches $2 \cdot i_{DC}$ at low output power, as in (54). Some discrepancy is observed due to tolerances in measuring and setting the i_{SR}^{*} and i_{DC} levels. This is seen in that the CDMA i_{SR}^{*} / i_{DC} ratio falls slightly below unity at maximum power. Realistically, this is caused by measurement error and because, in the i_{SR}^{*} optimization process, efficiency versus i_{SR} is relatively flat at its peak. This makes it difficult to set the exact peak efficiency by hand, and leads to slight deviation in

optimum i_{SR}^{*} values from theoretical predictions. Fortunately, because of the shallow minimum in power dissipation, this is without major consequence to average efficiency.

Importantly, Figures 59-61 show that significant power savings are possible if the switching regulator supplies the optimum current, i_{SR}^{*}, rather than the DC current to the load. The power savings are most dramatic at low output power levels, when the average output voltage is significantly less than the supply voltage. At low power, the switching regulator supplies more than the DC current. This reduces the net current that the linear regulator draws from the supply. In the simple cases of sinusoidal-AM and two-tone modulation, i_{SR}^{*} can be found by hand calculation with reasonable accuracy. However, the better solution may be to adaptively seek i_{SR}^{*} with an extremum-seeking adaptive control architecture, such as is presented in [80] for dead-time optimization. As demonstrated in Figures 59-61, this method promises significant power savings for the hybrid regulator architecture for dynamic supply applications.

5.7 Calculation Including Load Dynamics

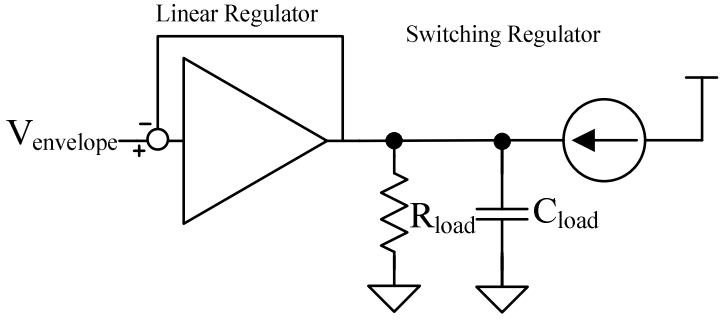


Figure 62. Hybrid regulator model including output capacitance

If the load impedance includes substantial reactive dynamics, the optimum operating conditions change slightly. Figure 62 shows a model for a hybrid voltage regulator that includes output capacitance in parallel with the resistive load. In this case, some current is supplied to the reactive part of the load impedance when the output voltage is dynamically adjusted. It is expected that additional power loss will occur due to CV^2 energy loss in the capacitor. It turns out for this example, that the power loss is related to the time constant, $\tau = RC$, of the output network relative to the frequency content of the voltage signal.

The behavior can be solved explicitly for the sinusoidal amplitude-modulation case, and so in this section we will use this case to highlight the general behavior of the hybrid regulator with load dynamics. Assuming that the output voltage trajectory follows

$$v_o(t) = v_{DC} + v_a \cdot \cos(w_a t), \tag{61}$$

where v_{DC} is the DC output voltage, v_a is the amplitude of the modulation signal, and w_a is the frequency of the amplitude modulation tone. Then the load current including the reactive dynamics follows

$$i_o(t) = \left[v_{DC} + v_a \cdot \cos(w_a t)\right] \cdot \left[jw_a C + \frac{1}{R} \right], \tag{62}$$

where $jw_a C + \frac{1}{R}$ is the admittance of the load network at the frequency of the AM tone.

The current supplied to the load by the linear regulator, following the development of section 5.4 follows as

$$i_{LR}(t) = \left[v_{DC} + v_a \cdot \cos(w_a t)\right] \cdot \left[jw_a C + \frac{1}{R} \right] - i_{SR}(t), \tag{63}$$

such that the conduction angle of the linear regulator is

$$\Phi = \cos^{-1}\left[\frac{i_{SR} - i_{DC}}{i_a + jw_a C \cdot V_a} \right]. \tag{64}$$

As seen in (64), the conduction angle is complex, but average quantities can still be found using the magnitude of this quantity,

$$\left|\Phi\right| = \cos^{-1}\left[\frac{i_{SR} - i_{DC}}{i_a} \left| \frac{1}{1 + jw_a RC} \right| \right]. \tag{65}$$

The average linear regulator current then follows as

$$\left\langle i_{LR} \right\rangle = \frac{1}{2\pi} \int_{-|\Phi|}^{|\Phi|} \left(i_{DC} - i_{SR} + V_a \cos(\phi) \cdot \left| jw_a C + 1/R \right| \right) d\phi . \tag{66}$$

(66) is then solved and simplified to

$$\left\langle i_{LR} \right\rangle = \frac{\tilde{i}_a}{\pi} \left[\sin\left|\Phi\right| - \left|\Phi\right| \cos\left|\Phi\right| \right], \text{ where}$$
$$\tilde{i}_a = i_a \left| 1 + jw_a RC \right| . \tag{67}$$

This results in nearly the same form for the previous sinusoidal AM case, except that (67) includes the first order dynamics. Using the same optimization procedure as in

previous examples, the system is solved for the minimum power loss conditions, such that $\frac{d\langle\eta\rangle}{di_{SR}} = 0$. The resulting optimum conditions follow as

$$\left|\Phi^*\right| = \frac{\pi V_{DC}}{V_{DD}}, \tag{68}$$

$$i_{SR}^* = i_{DC} + \tilde{i}_a \cos\left|\Phi^*\right|, \text{ and} \tag{69}$$

$$\eta^* = \frac{V_{DC} i_{DC} + \frac{V_a i_a}{2}}{V_{DC} i_{DC} + V_{DD} \frac{\tilde{i}_a}{\pi} \sin\left|\Phi^*\right|}. \tag{70}$$

Here, the form of (68)-(70) is similar to (54)-(56), but includes the reactive dynamics of the output capacitance. These expressions converge to the nominal resistive equations when the frequency of the amplitude modulation is well below the frequency of the pole at the output. However, if the frequency of amplitude modulation approaches or exceeds the output pole, substantial losses may occur because of the load capacitor.

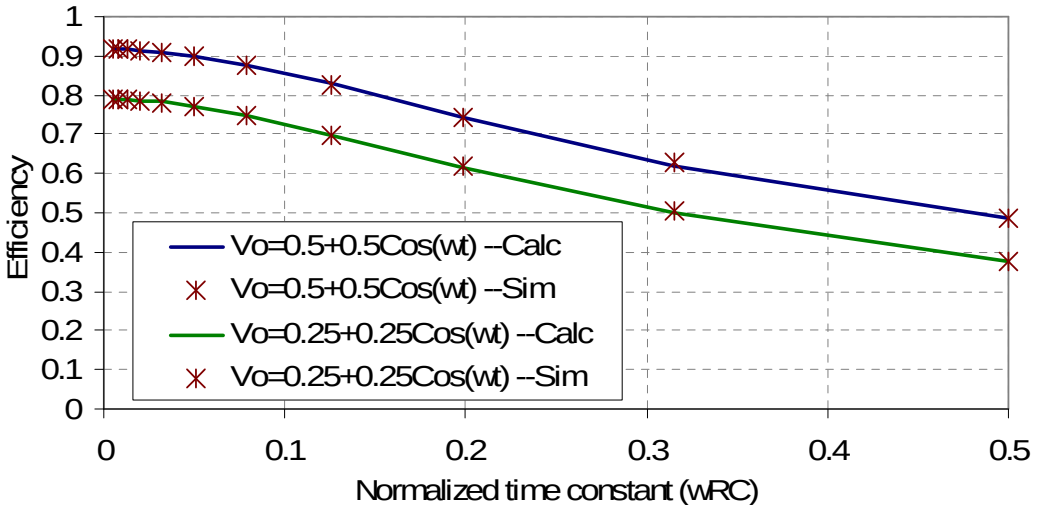


Figure 63. Hybrid regulator with load capacitance: efficiency versus normalized time constant (simulation vs theory)

Figure 63 shows the efficiency of the hybrid voltage regulator driving a first-order RC load, as in modeled in Figure 62. The x-axis is normalized to the quantity *wRC* such that the frequency of the amplitude modulation signal is a percentage of the output pole frequency. The maximum efficiency following (70) is plotted using the solid lines. Simulation results are shown with discrete points. Here, simulation matches the expressions derived in (68)-(70) with excellent agreement.

Figure 63 shows that if the frequency content of the amplitude modulation signal is less than around $1/10^{th}$ the output pole, minimal losses are associated with the reactive component. However, as the frequency content of the output signal approaches the output pole frequency, efficiency falls off rapidly. If the signal frequency approaches ½ the output pole frequency, efficiency is nearly cut in half.

The implication for hybrid regulator design is that the output pole should be placed substantially above the signal frequency. This means that bypass capacitors for the load circuitry should be designed as small as possible to avoid reactive losses. For the linear regulator in the hybrid topology this means that it is less desirable to have a dominant pole at the output of the regulator. For stability, it may be better to place the dominant pole, or the pole limiting the frequency response of the linear regulator, inside the linear regulator. This is only true if there is substantial power in the amplitude modulation signal near the linear regulator dominant pole.

5.8 Summary

Parallel hybrid voltage regulators are highly practical for dynamic supply transmitter applications. These topologies can provide fast dynamic regulation with low noise and high efficiency. If the operating conditions are carefully considered, power efficiency can be comparable to a pure switching regulator solution. The key is to consider the time-domain operation of the switching and linear regulator portions as many waveforms can have the same power spectrum. In many cases, the switching regulator should supply more than the average load current, with the linear regulator sinking more current to ground in a push-pull output stage. There are many conceivable circuit architectures that could optimize the bias conditions of the hybrid regulator through online sensing and slow adaptive feedback. A final practical consideration includes the dynamics of the load network. From an efficiency perspective, it is best to have any poles at the output be substantially higher frequency than the modulation signal to avoid reactive losses. This implies that the linear regulator may be best optimized with internal compensation rather than using a dominant pole at the output.

Chapter 6 Direct Digital Modulation: A New Approach to Polar Systems

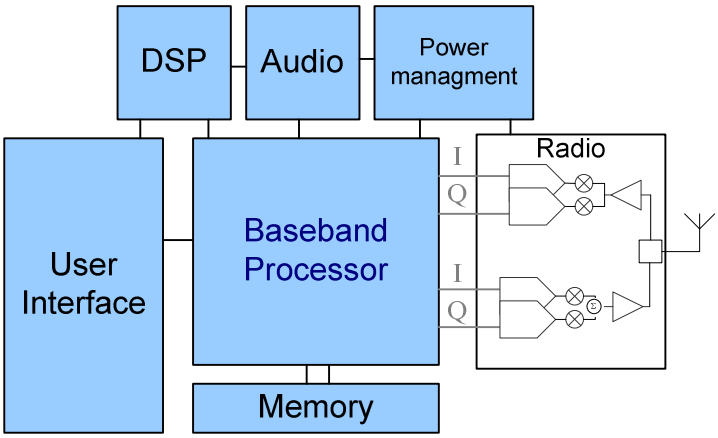


Figure 64. Conventional cellular phone block diagram: digital application processor, DSP, Audio, Power management; Radio is still largely analog

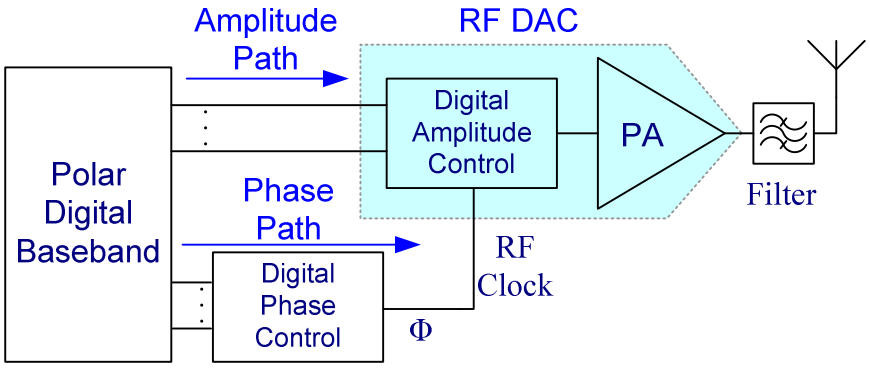


Figure 65. Proposed digital polar architecture

Modern wireless communication relies heavily on digital processing to implement complex layers of the communication protocol. Shown in Figure 64, the core of low-power portable communication includes a digital micro-processor, DSP, memory, and often digital audio and power management integrated circuits. However, even with low cost, readily available processing power, the radio circuitry remains largely analog and based on architectures that are more than 50 years old [10].

In this chapter we will describe an effort to extend the scope of modern low cost digital CMOS to the radio architecture. We will revisit the fundamental goals of the transmitter and the advantages of polar modulation. Finally we will discuss a set of test chips in standard 90nm CMOS that implement a digital-polar transmitter for Bluetooth 2.1+EDR at up to 3MB/s datarates. The proposed top-level schematic for the digital-polar architecture is shown in shown in Figure 65. Contrasting with conventional supply-modulated polar architectures, in this work the amplitude of the RF carrier is controlled directly with a digital input from the baseband. In the general case, any form of discrete amplitude control is possible as long as the digital-RF conversion process remains linear. In the case presented here, amplitude quantization is achieved with 1-bit pulse-density modulation of the RF carrier.

The concept of a direct-digital transmitter has its origins in high-frequency bandpass data conversion using $\Sigma\Delta$ modulation [91]. Early applications of bandpass $\Sigma\Delta$ to RF transmitters are described by Jayaraman et. al. in [92] and Wang in [93]. More recent work by Jerng et. al. is presented in [94] and Berland et. al. in [95]. Other relevant references include [96-98].

This work presents a new approach to the digital transmitter based on the polar architecture shown in Figure 65. Rather than using bandpass conversion with a high oversampling ratio, the polar architecture allows us to use lowpass $\Sigma\Delta$ modulation combined with digital upconversion to achieve lower digital power consumption. By carefully segmenting the data conversion process, we are able to achieve transmitter

linearity vastly exceeding the requirements of the standard with total processing power on the order of 5mW. Another major contribution in this work is the inclusion of the PA as part of the digital transmitter. This not only improves the efficiency of the transmitter, but helps to guarantee the linearity of the output stage allowing us to achieve EVM values less than %2.0 for high peak-to-average ratio modulation formats.

6.1 Transmitter concepts revisited

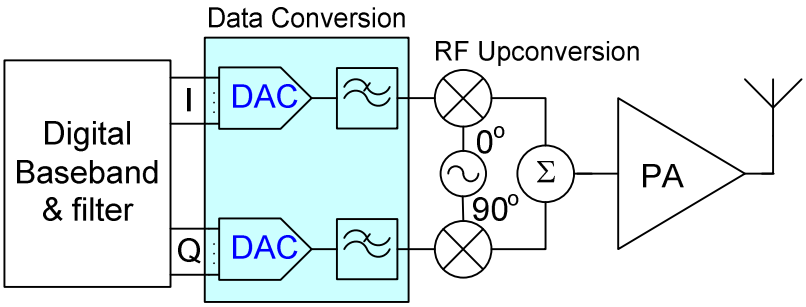


Figure 66. Traditional Cartesian transmitter architecture: lowpass data conversion followed by upconversion mixers

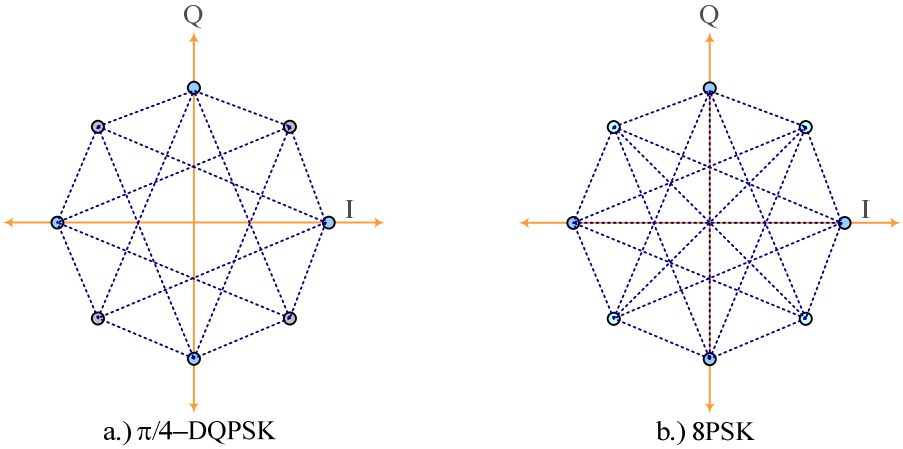


Figure 67. π/4DQPSK and 8PSK constellation diagrams

As discussed in Chapter 2, the goal of the transmitter is to drive a modulated RF signal into the antenna. Overall, the transmitter converts digital baseband vectors into an RF

vector signal that passes through constellation points. By this description, the transmitter, taken as a black-box function, operates as a digital-to-RF data converter. The integrity of the RF vector trajectory is quantified through the error-vector-magnitude (EVM) figure of merit, described in section 2.1.2. Spectral purity is verified through conformance to a spectral mask and adjacent-channel-power ratio (ACPR) measurements. The constellation trajectories for π/4DQPSK and 8DPSK (non-constant amplitude) modulation formats are shown in Figure 67. These will recur in the discussion as these are the modulation formats for the Bluetooth 2.1+EDR standard for 2MB/s and 3MB/s datarates [9]. These constellations demonstrate the use of both amplitude and phase modulation to transmit large amounts of information within the available spectrum.

The transmitter needs to have tolerable levels of noise and distortion to prevent spectral regrowth and meet *EVM* requirements. Traditional architectures rely on highly linear components to achieve these properties. The Cartesian architecture, shown in Figure 66, uses baseband digital-analog conversion followed by RF upconversion to map out the RF signal trajectory. Here, the data conversion process happens at low frequency – analog mixers are required to convert the vector signal to RF and the PA drives the modulated signal to the antenna. Because the mixers and PA follow the data converters, linearity is highly important. There are many mechanisms that reduce signal integrity including LO mismatch, gain-phase errors, and component nonlinearity.

The next section will describe basic principles of baseband data conversion such that these concepts can be extended to RF bandpass digital-analog conversion. We will review the fundamental goals of data converters including discrete-time sampling, reconstruction, and quantization noise.

6.2 Data conversion principles

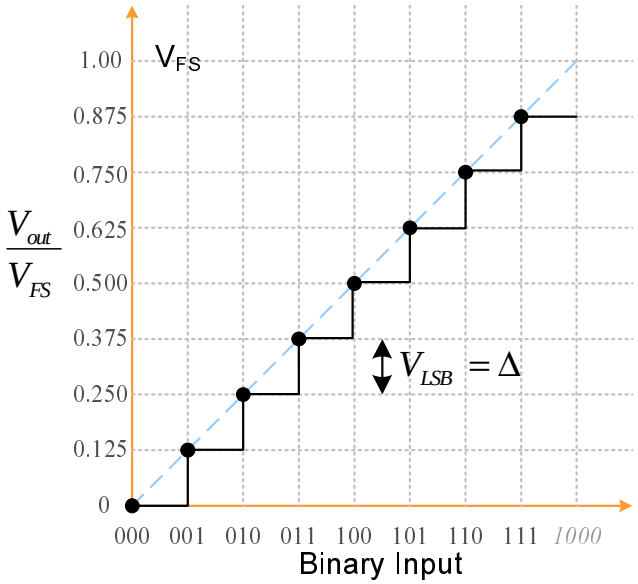


Figure 68. Input-output transfer characteristics for a 3-bit D-A converter

Data converters transfer data across digital and analog interfaces. Traditional lowpass D-A and A-D converters exhibit a voltage transfer characteristic where each binary number corresponds to a unique analog level. Figure 68 shows the voltage transfer curve for a 3-bit D-A converter. Here, the *000* code corresponds to zero volts. Each bit increment increases the voltage level by $\frac{V_{FS}}{N}$, where V_{FS} is the full-scale voltage input and *N* is the number of bits. This quantity is also referred to as the least-significant-bit

(LSB). The maximum voltage level represented in the digital-domain is $V_{FS} - V_{LSB}$. From [99], the relationship between V_{out}, V_{FS}, and the binary input b_N follows as

$$V_{out} = V_{FS}\left(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}\right). \tag{71}$$

Equation (71) highlights the fact that data conversion processes are typically based on binary weighted quantization intervals. This simplifies converting between analog and binary-digital representations. The final digital representation is discrete in both amplitude and time, resulting in unique properties of the digital signal. Discrete amplitude levels result in quantization error or noise. Discrete time samples enforce special considerations for sampling process that are related to the frequency content of the signal.

6.2.1 Quantization Noise

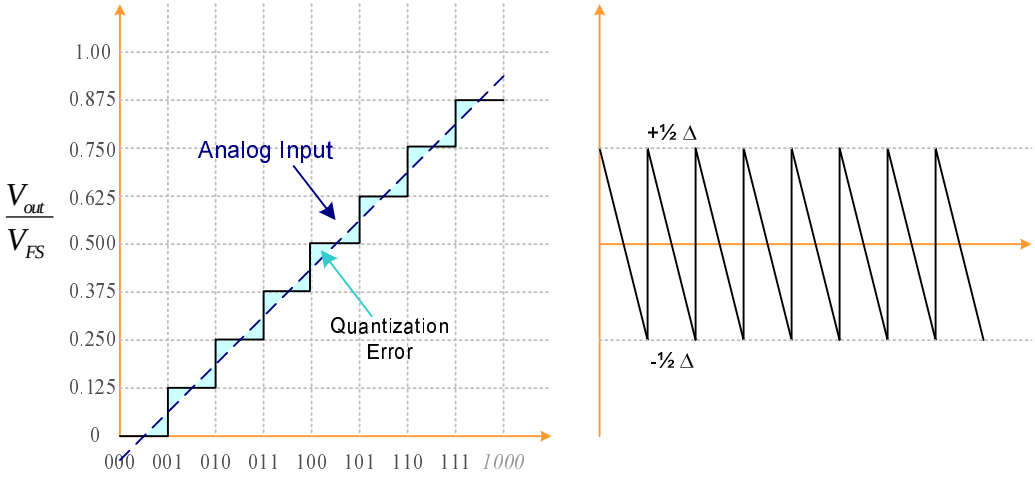


Figure 69. Comparison of continuous and quantized signal levels showing error between ±½ LSB

With a finite number of amplitude quantization levels, there is inevitably some error between the analog and digital representations of a signal. Figure 69 compares the quantized representation of a continuous full-scale analog signal, highlighting the instantaneous quantization error. This error can be characterized as quantization noise and shows unique spectral properties. For many input signals, quantization noise is treated as uniformly distributed between $\pm \frac{1}{2}\Delta$, where Δ is the quantization step size of one LSB. With this assumption, the average noise power is calculated as

$$\overline{e^2} = \int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12}. \tag{72}$$

Equation (72) assumes that the sampled error *e[n]* is a uniformly distributed white-noise process [100]. In this case the sampled noise power, $\overline{e^2}$, will be white within the Nyquist sampling interval. This property implies that the time-sampling process can affect the noise power spectrum, allowing opportunities to trade off sampling rate for the number of bits in the quantizer.

6.2.2 Discrete-time sampling

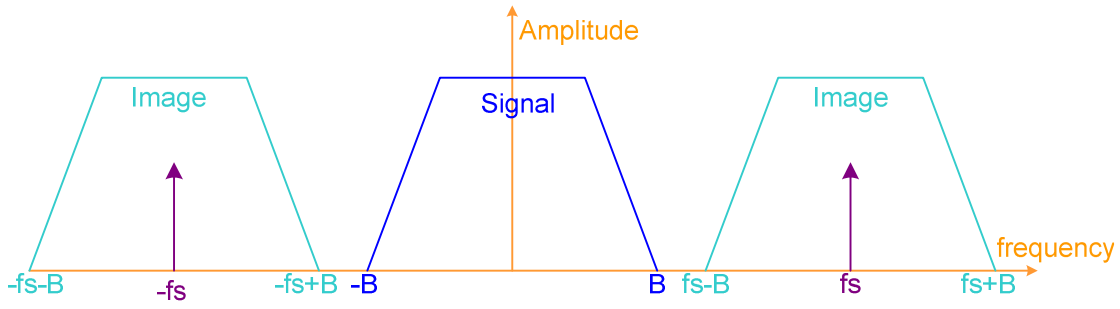


Figure 70. Frequency-domain representation of discrete-time sampling process

While most analog signals are continuous time, digital systems typically operate in discrete time. Data converters are subject to the sampling process and must consider Nyquist sampling criterion. Nyquist-Shannon sampling states that for a bandlimited signal, uniformly spaced discrete time samples completely represent the signal if the sampling rate is more than twice the signal bandwidth. If the sampling rate, $f_S < 2B$, where *B* is the bandwidth, then aliasing occurs such that the original signal can not be completely reconstructed. In the original paper by Shannon, [101], these properties are demonstrated in the conversion between time and frequency domain representations. The simple proof by Shannon assumes that:

$$\begin{aligned} f(t) &= \frac{1}{2\pi}\int_{-\infty}^{\infty} F(w)e^{iwt}dw \\ &= \frac{1}{2\pi}\int_{-2\pi B}^{2\pi B} F(w)e^{iwt}dw, \end{aligned} \tag{73}$$

where *f(t)* and *F(w)* are the time- and frequency-domain (Fourier transform) representations of a bandlimited continuous time signal with bandwidth *B*. If we let $t = \frac{n}{2B}$ where *n* is any positive or negative integer, the discrete-time series is

$$f\left(\frac{n}{2B}\right) = \frac{1}{2\pi}\int_{-2\pi B}^{2\pi B} F(w)e^{iw\frac{n}{2B}}dw, \tag{74}$$

where $f\left(\frac{n}{2B}\right)$ are the sampled values of $f(t)$. The right side of (74) represents the n^{th} coefficient in a Fourier-series expansion of $F(w)$. Since $F(w)$ completely

characterizes $f(t)$, then $f(t)$ can also be completely reconstructed from $f\left(\frac{n}{2B}\right)$. Here, reconstruction happens through the *sinc* function, such that

$$f(t)=\sum_{n=-\infty}^{\infty} x_n \frac{\sin(2\pi Bt-n\pi)}{(2\pi Bt-n\pi)}, \tag{75}$$

where x_n is the n^{th} sample.

6.2.3 Practical sampling and reconstruction

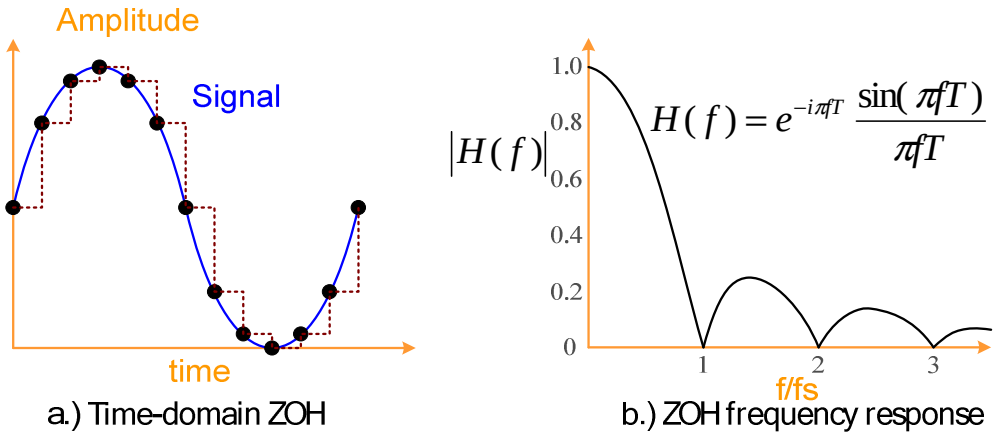


Figure 71. Time- and frequency-domain characteristics: zero order hold (ZOH) reconstruction

While sinc function reconstruction in (75) provides exact reconstruction of the sampled data series, the sinc function is not limited in time and is difficult to implement in practice. Practical reconstruction often involves a zero-order-hold (ZOH) of the sampled data set. Shown in Figure 71-a, in the time-domain the sampled values are held between sample times, resulting in a staircase waveform. Here, the ZOH function is modeled as a rectangular pulse waveform in the time-domain. This is a straightforward method of reconstruction, but does not have unity frequency response,

limiting the output spectrum to the sinc function shown in Figure 71-b. The ZOH shapes the output spectrum by a sinc function, significantly attenuating frequency content near the nyquist frequency. For this reason, ZOH is more practical for systems where the sampling frequency is substantially higher than the bandwidth of the signal.

6.2.4 Sampling with non-bandlimited signals, and relationship with quantization noise

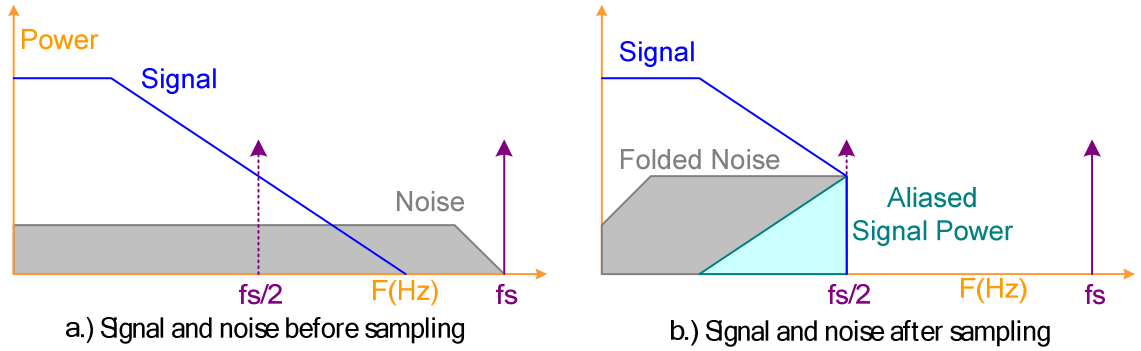


Figure 72. Signal and noise before and after sampling

If the signal is not completely bandlimited, then spectral content above $\frac{f_S}{2}$ will fold back to lower frequencies. Most sampled systems use anti-alias filters to suppress spectral content above the Nyquist frequency. Ideal brick-wall filters are impractical so some consideration of the filter attenuation above Nyquist frequencies is usually necessary. Figure 72-a shows a scenario with both signal and noise power extending beyond the Nyquist frequency. In the sampled version, the original signal is corrupted with signal and noise power folding back to lower frequencies.

The scenario shown in Figure 72 can be corrected in two ways: increasing the attenuation of the anti-alias filter, or increasing the sampling frequency. In some

circumstances, higher sampling frequencies are the most practical solution. Increasing f_S relaxes anti-alias filter requirements, such that in some cases first order filters are adequate. Higher sampling also reduces problems with high-frequency noise – often contributed by circuit components – folding down into the signal band. In addition to the obvious advantages with higher sampling rates, oversampling also provides an advantage in reducing quantization noise in a discrete-time system.

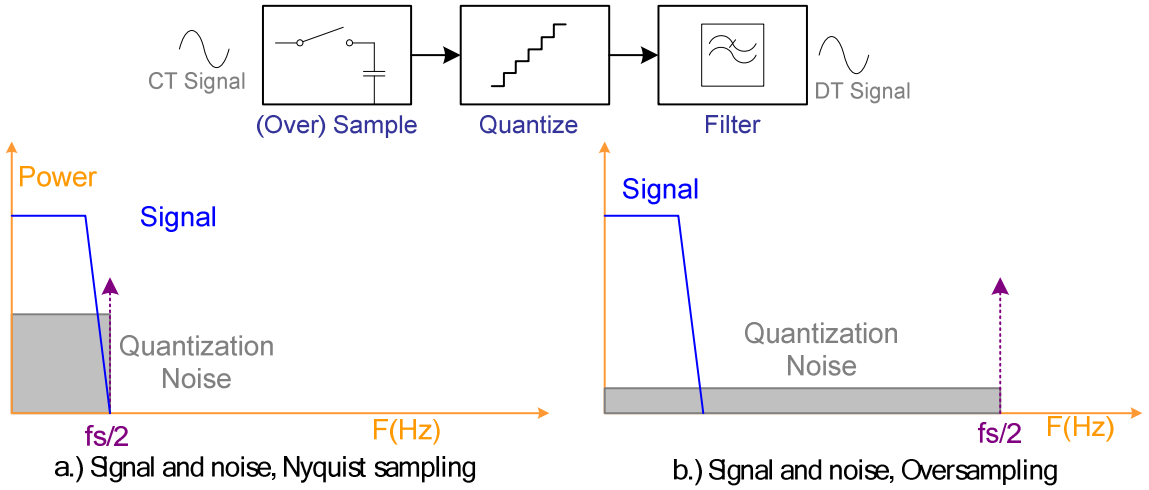


Figure 73. Quantization noise spectral density: a.) Nyquist-rate sampling, b.) Oversampling

As mentioned in section 6.2.1, quantization noise is generally treated as a white-noise process with a flat power spectral density within the Nyquist interval. If the sampling rate increases, the average noise power within the signal band decreases. Shown in Figure 73, if the signal is sampled at a rate substantially higher than the Nyquist rate, quantized, and filtered, the total noise power in the signal band is reduced. In this way, oversampling can increase the signal/noise ratio of the quantized, discrete-time signal.

As shown in the next section, this can have a similar effect to increasing the number of bits in the quantizer.

6.3 Oversampled Data Converters

Oversampled data converters exploit oversampling and signal processing to increase the effective resolution of discrete-time, quantized signals. As mentioned in the previous section, oversampling combined with filtering can increase the signal/noise ratio of a discrete-time, quantized signal. This effect is similar to adding bits to the quantizer. Most oversampled data converters take oversampling a step further by shaping the noise in the signal band, moving even more of the quantization noise into the filter stopband. Noise shaping can have tremendous benefits by increasing signal/noise substantially for a fixed sampling rate.

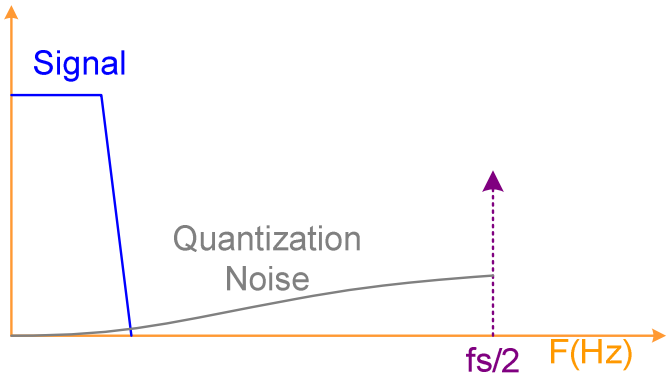


Figure 74. Signal and quantization noise with noise shaping

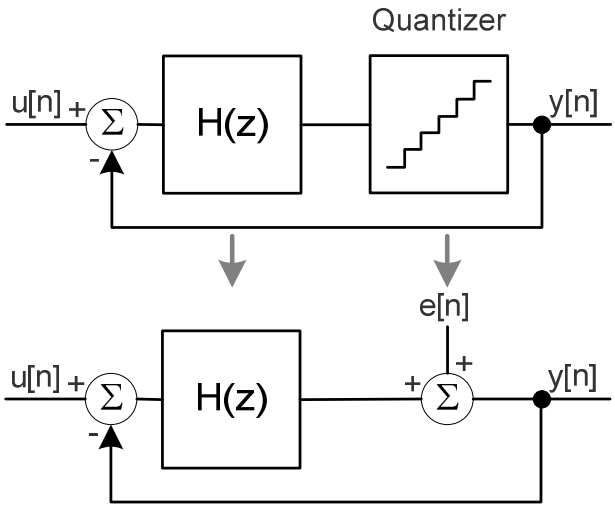


Figure 75. Linear model of the noise-shaping process: quantization noise appears as a disturbance

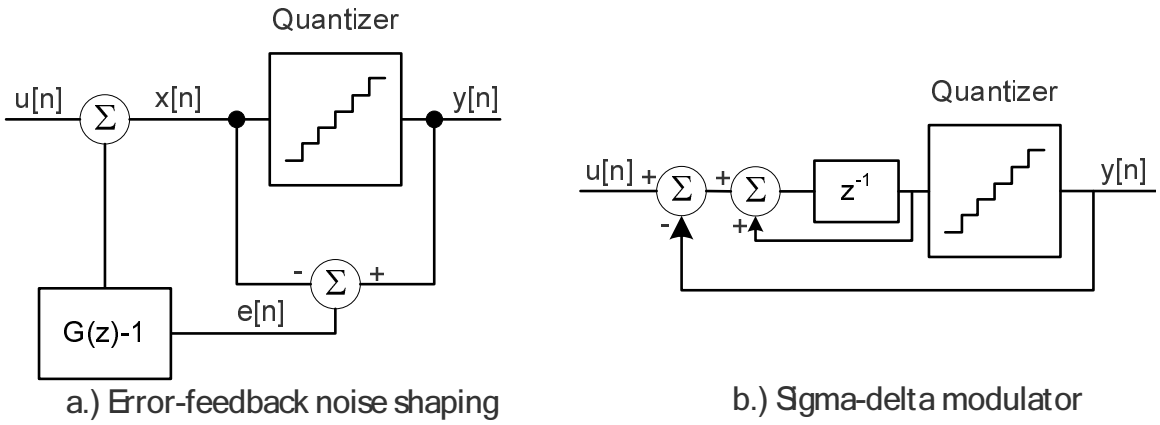


Figure 76. Noise-shaping data conversion blocks: a.) Error-feedback structure, b.) first-order sigma-delta modulator

6.3.1 Noise Shaping

The key conceptual insight to noise-shaping processes is that quantization noise can be separated from the signal through measurement. If the quantization error signal, shown in Figure 68, is measured, the error can be partly cancelled with active processing – assuming the sample rate is higher than the nyquist rate. Noise shaping

networks use feedback, such that quantization noise power appears as a disturbance and is attenuated by the network. The signal, on the other hand, passes through the system without attenuation.

Figure 75 shows the linear model for an oversampled modulator with quantization noise. The nonlinearity of the quantizer is approximated as a linear gain through the use of a describing function representation. A comprehensive discussion of the describing function approach to similar nonlinear control problems is found in [110]. In Figure 75, the quantization noise appears as a disturbance at the output of the network. With this linear model, we can derive two transfer functions for the system: the signal transfer function (STF), and the noise transfer function (NTF) [102]. Using linear network theory these transfer functions are:

$$STF = \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}, \tag{76}$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}, \tag{77}$$

where *H(z)* is the open loop signal transfer function. It is important to note that in (77), the zeros of *H(z)* are the poles of the *NTF*. To shape noise away from low frequencies, *H(z)* should have high gain in the signal band – *H(z)* often appears as an integrator at low frequencies. From (76), when *H(z)>>1*, the *STF* approaches unity such that the signal is unchanged at low frequencies.

There are many ways to implement the noise-shaping process in practice. Figure 76-b shows the conventional diagram for a first-order sigma-delta modulator. Much has

been written about this topology as a basic noise-shaping structure. Useful references include [100, 102, 103]. This topology originated as an extension of delta modulation that could be demodulated with a simple low-pass filter [102]. The input-output behavior is similar to the error feedback system in Figure 76-a, but implementation is slightly different.

In sigma-delta modulation one or more integrators are placed between the signal and the quantizer. The difference between the output (including quantization noise) and the noise-free input is integrated. With infinite gain at DC, over time the integrator forces the DC input and output voltages to be the same. With first order integration, $H(z) = \frac{z^{-1}}{1 - z^{-1}}$. The overall noise transfer function *(NTF)* follows as

$$NTF = \left(1 - z^{-1}\right), \tag{78}$$

while the signal transfer function *(STF)* is

$$STF = z^{-1}. \tag{79}$$

From (78) and (79), the quantization noise is attenuated substantially at low frequencies, while the signal passes with only a delay. The frequency domain characteristics are similar to Figure 74, where the noise spectrum is moved to higher frequencies such that a reconstruction filter is more effective at separating the signal and noise. Integrating the noise power in the signal band, the effective signal/noise ratio for first-order noise shaping becomes

$$SNR = 6.02N + 1.76 - 5.17 + 30\log(OSR), \quad (80)$$

where *N* is the number of bits in the quantizer and *OSR* is the oversampling ratio. Equation (80) implies that doubling the oversampling ratio will increase the signal/noise ratio by 9dB (or 1.5 bits). It should be noted that this neglects noise components other than quantization noise and therefore sets an ideal upper bound on the achievable SNR.

The error-feedback noise shaping structure, shown in Figure 76 a.), highlights this process of measuring the quantization error and injecting the error signal back into the system [104]. Here, the error signal passes through a transfer function $G(z)-1$ and is summed with the input signal. The signal transfer function $STF(z) = \frac{Y(z)}{U(z)} = 1$, while the noise transfer function, $NTF(z) = \frac{Y(z)}{E(z)} = G(z)$. In this system the discrete-time FIR function *G(z)* directly implements noise shaping. For first-order noise shaping the block $[G(z)-1] = (1-z^{-1})-1 = z^{-1}$, such that the net transfer function is just a delay. Design examples for the error feedback topology are highlighted in [99] and [102].

6.3.2 RF (Narrowband) Digital-Analog Conversion (DAC)

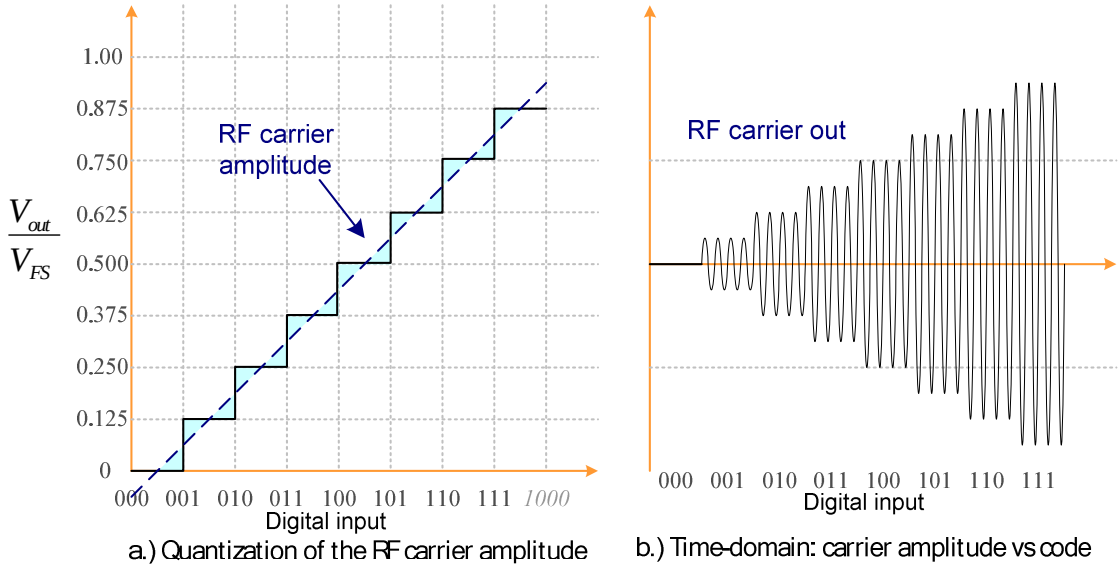


Figure 77. RF DAC: quantization of RF carrier amplitude

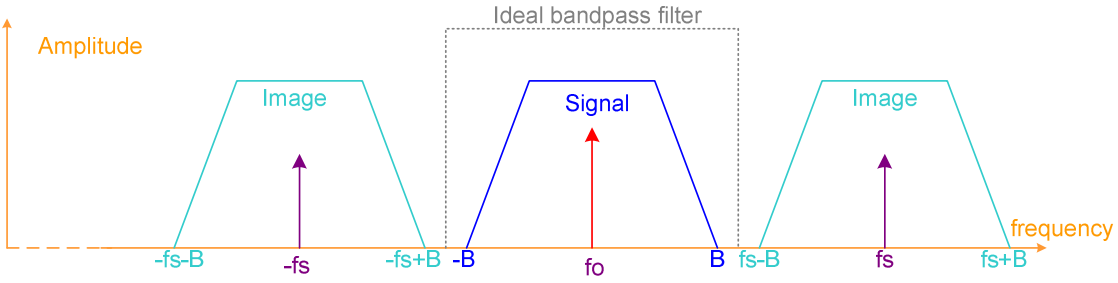


Figure 78. Frequency-domain RF DAC with sampling images

RF digital-analog conversion can have different meanings depending on the application. In this case we consider narrowband data conversion where each digital code corresponds to a unique amplitude of a continuous-wave sinusoidal carrier signal. For the data conversion process in Figure 77, the input-output behavior is similar to lowpass D-A converters except the output is centered at a carrier frequency f_0. The output spectrum is also similar to that in lowpass D-A conversion, but is now double-sided, appearing as an amplitude modulation process.

Figure 78 shows the frequency-domain representation of the narrowband data conversion process. We consider the sampling process to be independent of the carrier frequency, such that sampling images occur centered at $f_0 \pm n \cdot f_S$, where *n* is an integer. Aliasing considerations are now based on the nyquist criterion relative to the bandwidth, *2B*, of the bandpass signal. Generally, to avoid overlap of image power with signal power (aliasing), $f_S > 2B$. To filter the images and other out of band spectral content, the RF DAC is followed by a bandpass filter. An ideal bandpass filter spectral response is shown in Figure 78, although realistic filters will have finite stopband attenuation, limiting rejection of RF images.

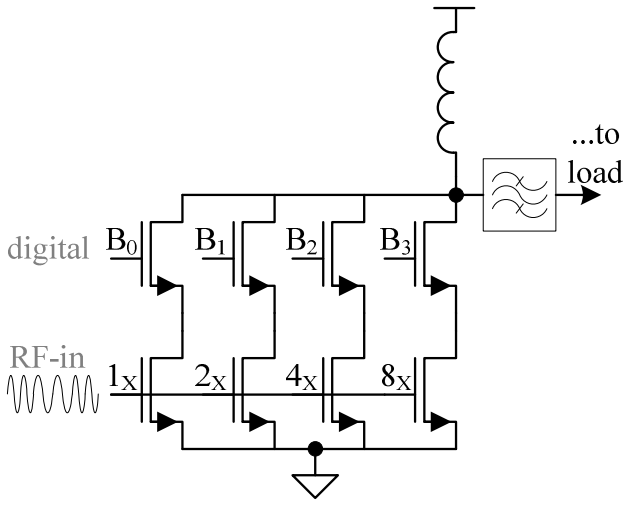


Figure 79. RF DAC example implementation: binary weighted class-A amplifier stages (current summing), as in [105]

RF data converters can be implemented in many ways. A representative circuit implementation is shown in Figure 79. Here, binary weighted RF amplifier stages sum together as in a current-summing DAC [40, 99]. The class-A (or AB) RF current sources are turned on or off with the digital input of a cascode device. The total current at the

drain node of the cascode devices scales linearly with the binary input. This current may be filtered at the output of the DAC to attenuate harmonics from the amplifier and DAC images. The digital CMOS PA described in [105] operates as a differential current mode DAC and was effective in generating OFDM waveforms with -26dB EVM.

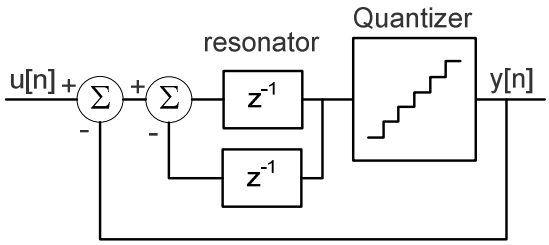


Figure 80. Bandpass ΣΔ modulator with center frequency at $\frac{f_s}{4}$

Oversampled bandpass modulators are also used for narrowband data conversion, as discussed in [91, 92, 98]. Figure 80 shows the simplified diagram of a second-order bandpass ΣΔ modulator. Here, the simple integrator of a first-order lowpass ΣΔ modulator is replaced with a resonant filter. This resonator has transfer function

$$H(z) = \frac{z^{-1}}{1+z^{-2}}, \tag{81}$$

such that the poles are at $z = \pm j$. This provides infinite gain at $\frac{f_s}{4}$ effectively shaping noise away from the $\frac{f_s}{4}$ frequency range. The oversampling ratio in this case is $\frac{f_s}{2B}$ where *2B* is the bandwidth of the narrowband signal. For traditional bandpass ΣΔ modulators, the sample rate, f_S, is higher than the narrowband center frequency, f_0.

6.4 Direct-digital modulation for RF transmitters

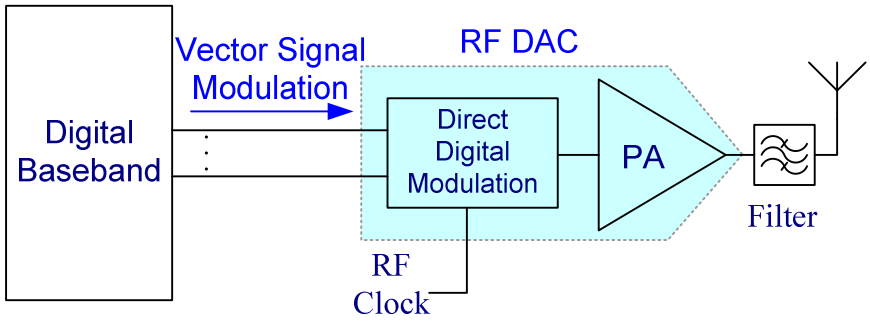


Figure 81. Direct digital modulation: transmitter operating as a D-A converter

With the description in section 6.1 of the wireless transmitter as a digital-RF converter, it is natural to re-think the transmitter architecture and look for opportunities to move the boundary between digital and RF domains. There are many ways to meet the fundamental goals of vector signal generation with low EVM and spectral mask compliance. Figure 81 shows a generic transmitter that operates as an RF D-A converter: the digital baseband controls the vector signal modulation process, and high-frequency digital circuitry converts this to a modulated RF signal.

Complicating the scenario in section 6.3.2 on RF data conversion, many wireless signals have both amplitude and phase modulation. This means that digital amplitude modulation alone is not sufficient to create the complex vector signals for modern wireless standards. Instead, we consider digital analogies for conventional polar or Cartesian transmitters that can create the necessary waveforms with both amplitude and phase information.

6.4.1 Cartesian RF Data Conversion

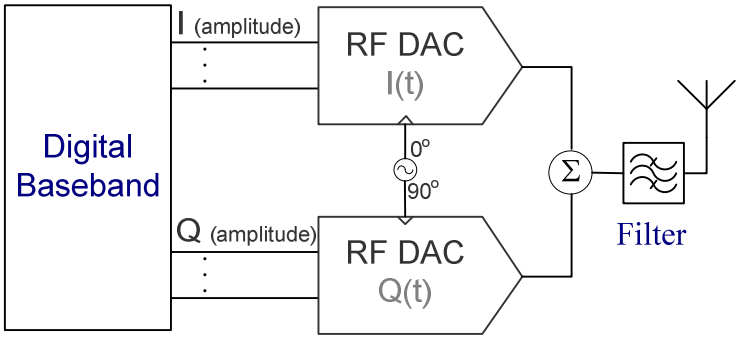


Figure 82. Cartesian RF data converter

Figure 82 shows a Cartesian version of a digital RF transmitter. Here, the *I(t)* and *Q(t)* vectors are independently generated by separate single-phase RF DACs. The DACs operate with separate quadrature clock signals to create the orthogonal *I/Q* signals. At the output of the DACs, the *I(t)* and *Q(t)* signals are summed to create the modulated RF waveform. A filter would conceivably follow the summation stage to remove unwanted spectral content from the output.

The scenario in Figure 82 is only possible if the summation stage is straightforward to implement. This may be true for current-mode signals, but is slightly more difficult for voltage mode signals. This is because adding RF voltages with high power efficiency requires electromagnetic structures such as transformers, couplers or L-C baluns. Examples of voltage mode power combining are found in [7], [33], and [38]. It is also important to note the *I(t)* and *Q(t)* signals have polarity information – i.e. they map out both positive and negative axes of the complex plane. The RF DAC needs to be able to represent both polarities to map out the full signal constellation. This may be done by

injecting the 180^0 and 270^0 clock signals to the appropriate DAC, or phase-shifting (inverting) the LO signal inside the DAC.

A current-mode 900MHz RF DAC is presented in [98], highlighting a single *I-Q* channel data converter (not the full cartesian system of Figure 82). In [98], the RF DAC cells operate as a differential version of the current-steering DAC in Figure 79. With 8-unit elements in the DAC, the system achieved an SNR of 53dB.

6.4.2 Polar RF Data Conversion

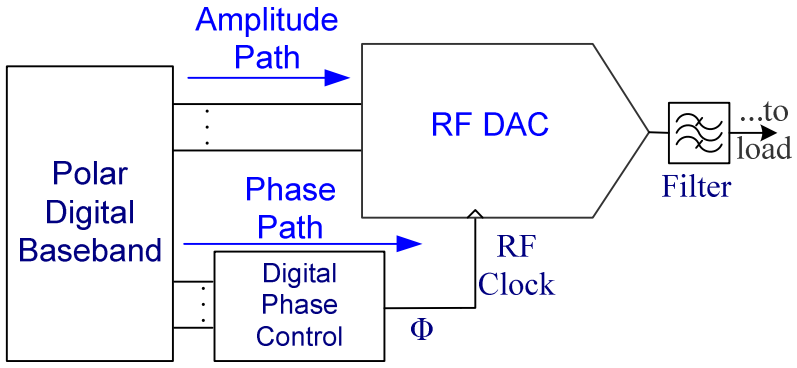


Figure 83. Polar RF data conversion: RF amplitude DAC with phase-modulated clock signal

Polar architectures are another candidate for direct digital modulation. In fact, the digital modulation process may be conceptually more straightforward than with the Cartesian example. In this case, the amplitude path is controlled directly by a single-phase RF digital-analog converter. Phase information is injected into the RF DAC with a phase-modulated RF clock signal. Figure 83 shows a general diagram for a polar RF DAC with separate amplitude and phase paths. Since the output of the polar DAC has both amplitude and phase modulation, it can generate complex vector trajectories. The

output spectrum is not necessarily symmetric as with the pure amplitude DAC in section 6.3.2 because of the addition of phase modulation.

The polar DAC has similar considerations to other polar transmitters. The amplitude and phase paths must have accurate time-alignment to prevent distortion. Also, the amplitude modulator needs to have low AM-AM and AM-PM distortion to meet EVM and spectral requirements. The RF clock with phase information has similar consideration to the conventional polar case discussed in section 2.3.1. The RF clock can be generated with a cartesian upconversion stage, or a digital PLL as in [26]. Both the amplitude and phase paths also need sufficient bandwidth to meet EVM and spectral mask requirements. While this is difficult for analog-polar implementations [28], digital implementation can exploit high sampling rates to achieve tracking bandwidths substantially higher than the nominal channel bandwidth.

Digital polar systems in the literature include [95, 105, 106]. The work in [105] employs a PA similar to the segmented DAC of Figure 79 to perform quantized RF amplitude modulation. The RF DAC uses 6-bits of amplitude quantization and achieves 7.2% power-added-efficiency (PAE) at 1.6GHz. A quadrature modulator, similar to Figure 12-a, drives the RF phase signal into the PA. Overall the system achieves -26dB EVM for 20MHz OFDM signals while delivering 13.6dBm output power. Further examples using this architecture will be discussed in section 6.5.

6.4.3 Issues with spectral images

Sampling images can be problematic in wireless systems as they can produce energy that can violate the spectral mask. Shown in Figure 78, sampling images are centered at $f_0 \pm n \cdot f_s$, where n is an integer. Problems with images result if the sampling (baseband) clock is low relative to the bandwidth of the output filter. A zero-order-hold in the data conversion process will attenuate sampling images with a sinc response as in Figure 71. However, in some circumstances, this is not sufficient to reduce spectral power below the required level.

In oversampled systems, interpolation may be effective in reducing the magnitude of the sampling images. The digital polar system in [105] takes particular consideration of spectral images. The system uses 4x oversampling combined with linear interpolation to reduce the spectral content at $f_0 \pm f_s$, where f_0 is the carrier frequency and f_s is the baseband sampling rate. This method is shown to substantially reduce the image at $f_0 \pm f_s$, approaching the output spectrum of a system originally sampled at $OSR \cdot f_s$, where *OSR* is the oversampling rate.

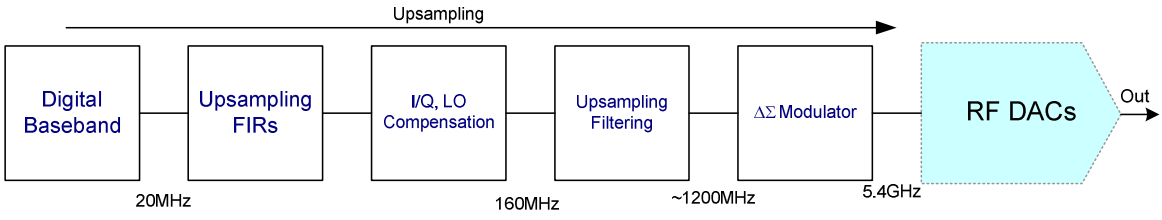


Figure 84. Upsampling to reduce spectral images, process in Pozsgay [106]

Shown in Figure 84, [106] uses an up-sampling scheme to reduce power from spectral images. The process is particularly aggressive in order to meet coexistence

requirements between WiFi/WiMax and 2G/3G cellular standards. Starting with a 12-bit *I-Q* baseband signal sampled at 20MHz, the signal is upsampled to 160MHz using FIR upsampling blocks. After *I-Q* mismatch compensation, the signal is further upsampled to $\frac{f_0}{2}$, approximately 1.2GHz. This process ideally moves the spectral images to $\frac{f_0}{2}$, substantially displacing them from the signal band and adjacent bands of interest. The RF DAC uses a current summing scheme (as in Figure 79) with various weights to achieve a peak output power of 2.6dBm. The system achieves 2.4% EVM while meeting spectral mask and coexistence requirements. Total system power consumption is 254mW for the 2.6dBm (1.8mW) rms output power level.

6.5 A 2.4GHz RF Polar Transmitter for Bluetooth 2.1+EDR

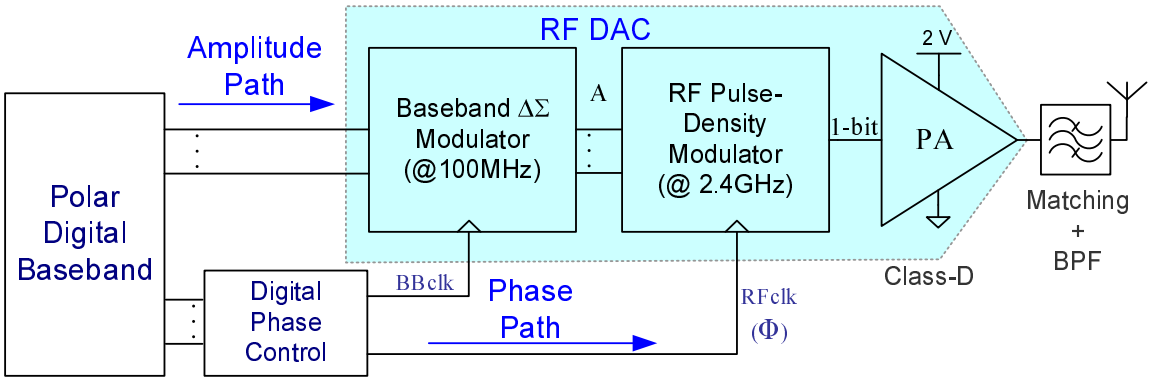


Figure 85. Digital polar modulation architecture

6.5.1 Introduction

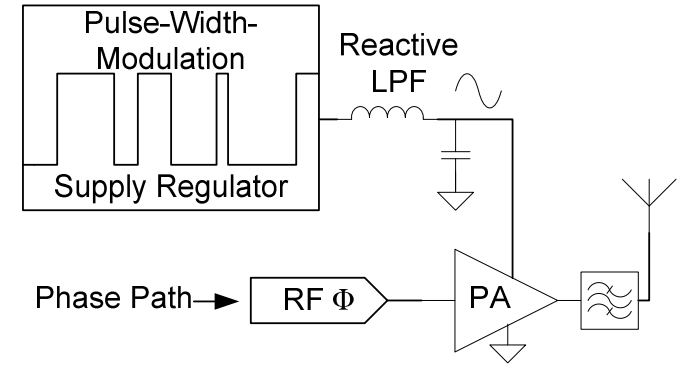
As discussed in Chapter 1, trends in semiconductor device technology, notably the f_t and f_{max} of CMOS devices, are enabling new techniques in circuit design for blocks in wireless systems. This work demonstrates a fully digital transmitter for the high-datarate Bluetooth 2.1+EDR standard. The transmitter is based on a polar architecture with digital amplitude modulation based on pulse-density modulation of the RF carrier. The system operates with a 2.4GHz clock that contains phase information. Contrasting with [94-98], which focus on RF data conversion for pre-PA signals, here the system includes the PA in the RF data conversion strategy, providing output power up to +20dBm. A major focus in this work is to reduce the power required for digital

processing (to enable practical implementation with low power Bluetooth systems). A two-stage signal processing scheme minimizes high frequency computation, enabling the digital blocks to operate with 2-8mW and average efficiency of up to 30% for the high datarate Bluetooth standard.

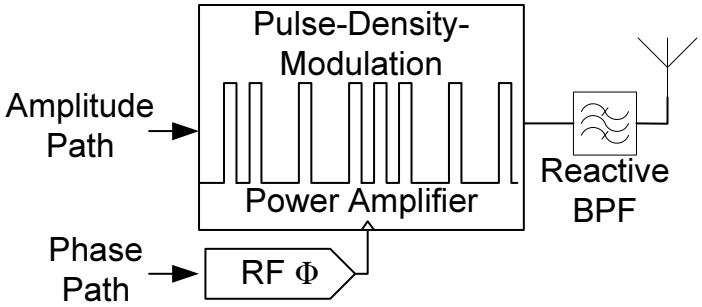
Shown in Figure 85, the system includes two stages of noise shaping and a class D PA. The class-D PA operates with both NMOS and PMOS complementary devices. With PMOS f_t on the order of 40GHz in the 90nm process, switching power loss is substantially reduced compared to previous generations of CMOS technology. A High quality factor (Q) passive filter attenuates out-of-band noise, and reduces power loss from harmonics. Matching networks and filtering are implemented at the board level to achieve higher quality factor. With appropriate passive components, we achieve unloaded Q in the range of 20-30 in the output network [107].

Pulse-density amplitude modulation provides an alternative to both conventional linear RF modulators and recent generations of polar and envelope tracking (ET) systems [7, 78]. With pulse-density modulation, switching losses scale with carrier amplitude, improving efficiency at low power levels. This improves average efficiency for standards with high peak-to-average power ratio (PAPR). Linearity is also improved because carrier amplitude is only a function of pulse-density, which can be accurately controlled by the digital system. By eliminating the need for dynamic supply regulation, the PDM system eliminates inherent problems with AM-AM, AM-PM distortion and power supply noise issues [29].

6.5.2 Architecture



a.) Polar system with PWM supply regulation



b.) Polar system with PDM in the PA

Figure 86. Candidate polar architectures

The architecture in Figure 85 is an extension of traditional supply-modulated polar architectures except that carrier amplitude is controlled with pulse-density modulation. Shown in Figure 86, the pulse-density architecture is a bandpass analogy of the PWM supply modulated architecture. To highlight the distinction, Figure 86-a shows a traditional supply-modulated polar system where the PA supply voltage is controlled with pulse-width modulation (PWM). Switching harmonics in the PWM waveform are

removed with a reactive lowpass filter leaving only the baseband amplitude modulation signal. In the proposed system of Figure 86-b, a pulse-density modulation (PDM) process generates the narrowband amplitude signal directly at the RF carrier frequency. In this case, a bandpass filter attenuates switching harmonics that occur because of the PDM process.

The pulse-density approach has several advantages over the supply-modulated PWM approach. As discussed in section 3.2.2, the PWM system is difficult to implement in terms of bandwidth and efficiency. The PA in the supply-modulated system often requires predistortion due to additional sources of AM-AM and AM-PM distortion. Also, voltage ripple from PWM switching harmonics can mix with the RF carrier, causing spectral regrowth near the band of interest.

In the PDM implementation of Figure 86-b, the system is simplified such that there are fewer distortion mechanisms. Also, the PDM process can be implemented with digital hardware, substantially reducing the analog complexity of the system. It may also be easier to achieve high bandwidth with an oversampled digital system. Oversampling lets the system achieve high resolution, while shaping the spectral components away from the carrier frequency. System bandwidth is only limited by the sampling rate and output filter characteristics.

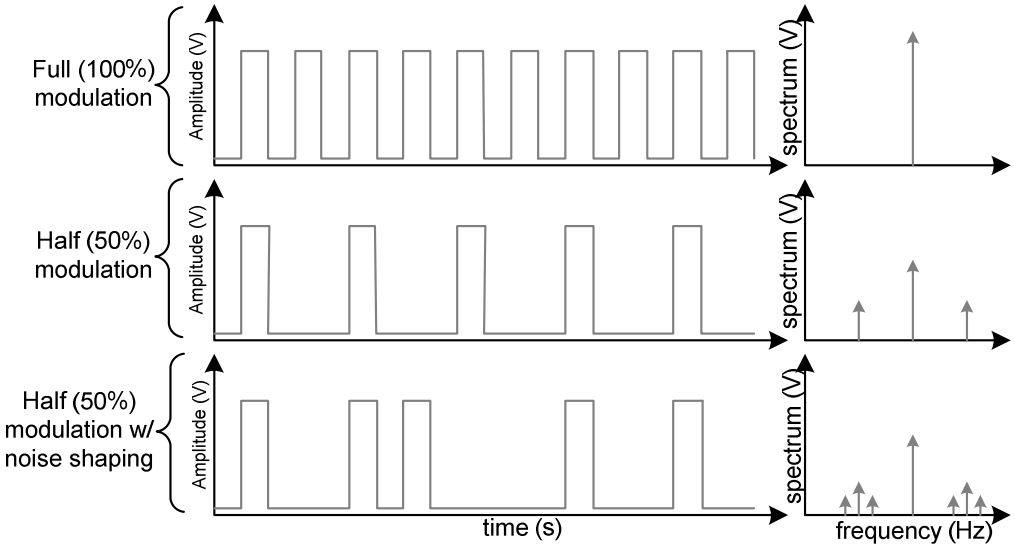


Figure 87. Time and frequency domain examples for full- and half-amplitude modulation

Shown in Figure 85, two stages of noise shaping control the pulse density modulation waveform such that unwanted spectral content is moved away from the signal band. At the output of the system, the PA drives a pulse waveform with 50% duty cycle into the matching network and bandpass filter. The high-Q output filter attenuates the harmonics and selects only frequency content at the RF carrier fundamental. The PDM process operates as an RF-DAC converting the high dynamic range baseband signal to a 1-bit representation at the carrier frequency. The first-stage $\Delta\Sigma$ modulator shapes quantization noise with a discrete-time transfer function. The output of the $\Delta\Sigma$ modulator controls the second stage pulse-density modulator. As will be discussed in section 6.5.3, the second stage modulator uses programmed binary codes to generate the pulse waveform at the RF carrier frequency. The upconversion block mixes the output with the RF carrier to generate the correct amplitude for the carrier. The PDM

process controls the amplitude of the carrier fundamental by changing the density of pulses at the carrier frequency.

The pulse-density process creates a spectrum similar to amplitude-modulation. Shown in Figure 87, the output includes harmonics symmetric around the carrier that can contaminate the output spectrum. Harmonics can also be a source of power loss in the system. As discussed in [108], the power distribution in pulse-density modulated waveforms is a function of modulation depth (pulse density) and the quality factor of the output filter. For the example in Figure 87, with loaded quality factor of $Q_{loaded} = 12$ and pulse-density of 50% (6dB power backoff), approximately 95% of the harmonic power is concentrated in the carrier [108].

This number ignores loss in active and passive components and falls off with decreasing pulse-density. The filter is designed to be high-impedance out of band to block harmonic power from reaching the antenna. For the voltage-mode class-D PA, a series resonant L-matching network is used as a first stage filter. Parallel resonant filters are also possible, but increase power loss by providing low-impedance at the output harmonics.

6.5.3 Pulse-density modulator (PDM)

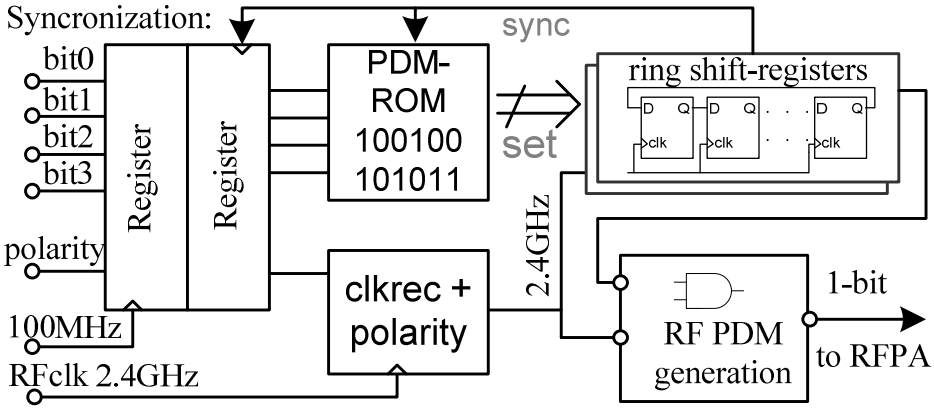


Figure 88. Pulse-density modulator block

The PDM block in Figure 88 uses programmed codes, nine pulses in length, to generate ten quantized amplitude levels between zero and full scale. The programmed codes are pre-shaped to force out-of-band noise away from the carrier.

The pulse-density modulator (PDM) block converts the output of the ΔΣ block to a 1-bit representation. The ΔΣ output is sampled with a synchronous 100MHz clock and then re-synchronized to a set of shift registers operating at 2.4GHz (*RFclk* signal with phase information). The shift registers generate a PDM waveform from pre-programmed binary codes stored in an on-chip ROM. The codes represent bit sequences corresponding to 10-level amplitude quantization. Tones from the programmed bit sequences occur far from the carrier frequency to maximize filter

attenuation. The clock recovery inverts the phase of the clock depending on the polarity bit. This allows polarity information to be synchronized with the amplitude path, eliminating wideband phase inversions in the phase path, as will be discussed in the next section. The PDM generation block mixes the PDM signal from the shift-registers with the RF clock. The RF clock contains phase information and the PDM signal contains amplitude information. The result is a polar modulated 1-bit output that is provided to the class-D PA.

For example, at half amplitude, the sequence generates alternating 'zeros' and 'ones.' In this case, the closest harmonic is at $w_0/2$ where w_0 is the carrier frequency. This concept is highlighted in Figure 87. Pre-shaped codes are used to generate amplitudes increasing at $1/9^{th}$ of the full scale amplitude. This places the worst-case tone at $w_0/9$, or 266MHz away from the 2.4GHz carrier. The spectral components of the pre-shaped codes are diversified such that the output tones are substantially reduced by the first-stage $\Delta\Sigma$ process.

6.5.4 Polarity Bit

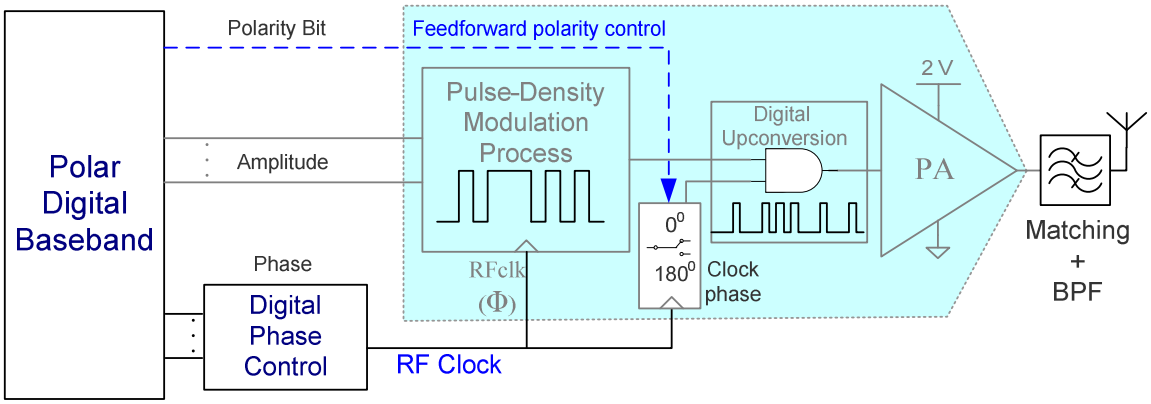


Figure 89. 1-Bit polarity feedforward to reduce power from rapid phase transitions

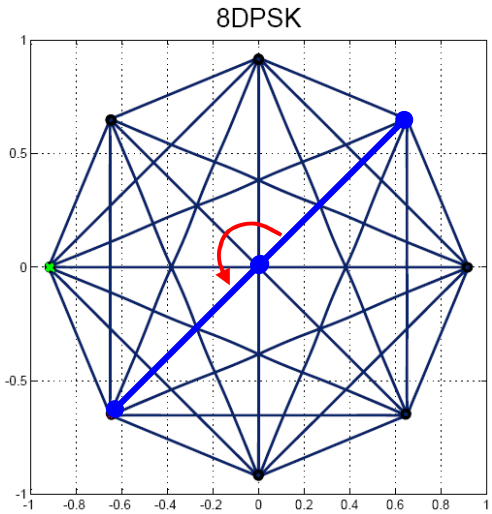


Figure 90. Constellation diagram for 8DPSK with feedforward phase transition: $\frac{\pi}{4} \rightarrow \frac{5\pi}{4}$

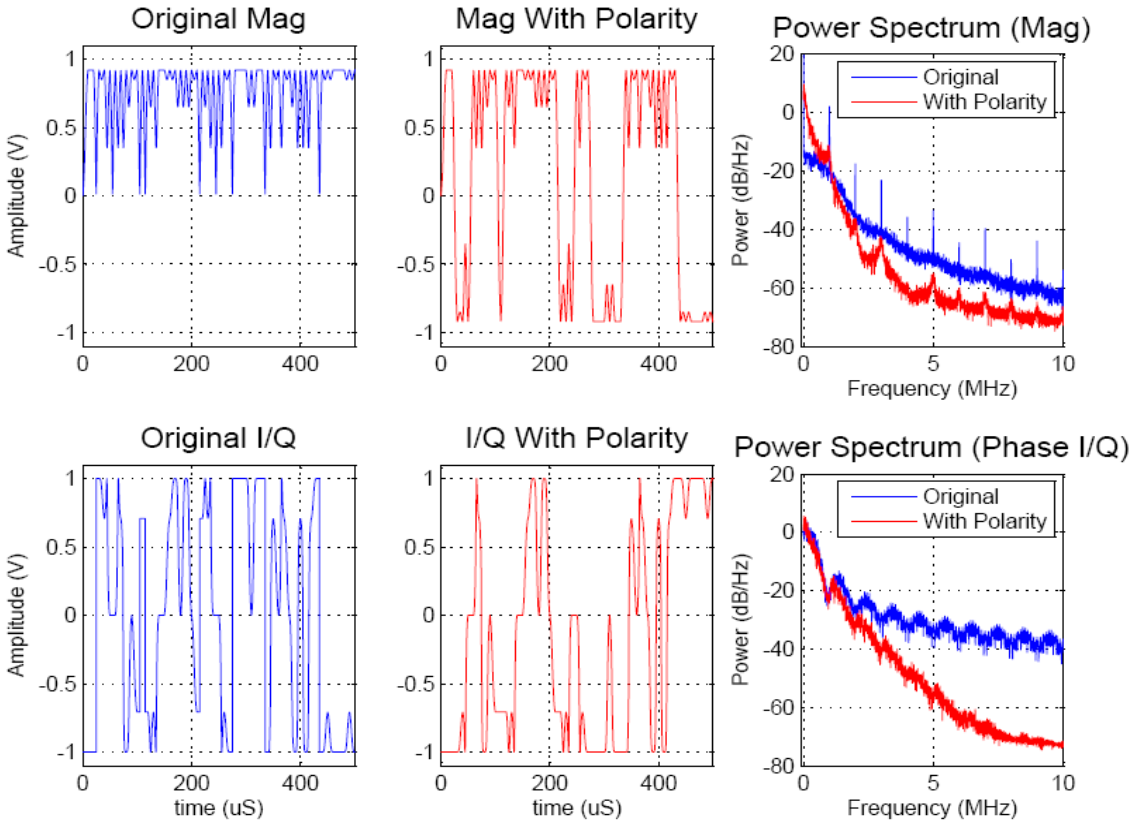


Figure 91. Polarity bit significantly reduces high frequency power in the RF clock signal waveform by smoothing phase transitions near origin

As mentioned in section 2.3.2, rapid phase transitions can occur when the constellation trajectory passes near the origin. In a conventional Cartesian architecture, the I-Q vectors remain linear since the amplitude also approaches zero in this case. However, in a polar system, the phase signal maintains full amplitude, creating high frequency spectral content. Figure 90 shows the constellation diagram for 8DPSK modulation. With 8DPSK, the signal trajectory can pass through the origin, causing up to 180^0 instantaneous phase shift. This rapid phase shift is difficult to generate in a realistic phase modulator as there is usually a limit on the bandwidth of the modulator.

To reduce the spectral content from rapid phase transitions, we use single bit feedforward of polarity information in the digital system. The polarity bit transmits phase inversions to the final digital upconversion stage in the polar architecture. The polarity bit can be thought of as a feedforward mechanism encoding rapid phase shifts in the constellation diagram. Figure 89 shows the schematic representation of the digital transmitter with polarity feedforward. The digital baseband determines when a polarity shift occurs and provides a 1-bit signal to the upconversion process. When polarity changes, the upconversion clock is inverted, or shifted by 180^0. It is also possible to multiplex between 0^0 and 180^0 local oscillators to guarantee symmetry in the inversion. In future implementations it may also be possible to use 4-phase quadrature clock signals (0^0, 90^0, 180^0, and 270^0), such that the range of the phase modulator is only one quadrant of the complex plane.

With an entirely digital transmitter, it is straightforward to synchronize polarity shifts. Because amplitude and phase need to be aligned for proper polar encoding of the signal, the baseband (or phase modulator circuitry) is aware of the timing constraints between amplitude and phase. Using this information the polarity inversion can be synchronized to the exact clock cycle where inversion occurs, preventing issues with glitches in the polar system.

Figure 91 shows the time- and frequency-domain effect of using the polarity bit. The I-Q data in Figure 91 represents a single 'I' or 'Q' basis vector as would be the case with

constant-envelope Cartesian representation of the phase-path signal. In the time-domain, the I-Q representation shows fewer rapid transitions as the 180^0 transitions are now encoded with the feedforward signal. In the frequency-domain, high frequency power in the I-Q signals is substantially reduced. At 10MHz, there is more than a 30dB reduction in the I-Q signal power. This significantly relaxes the bandwidth requirements of the phase modulator circuitry.

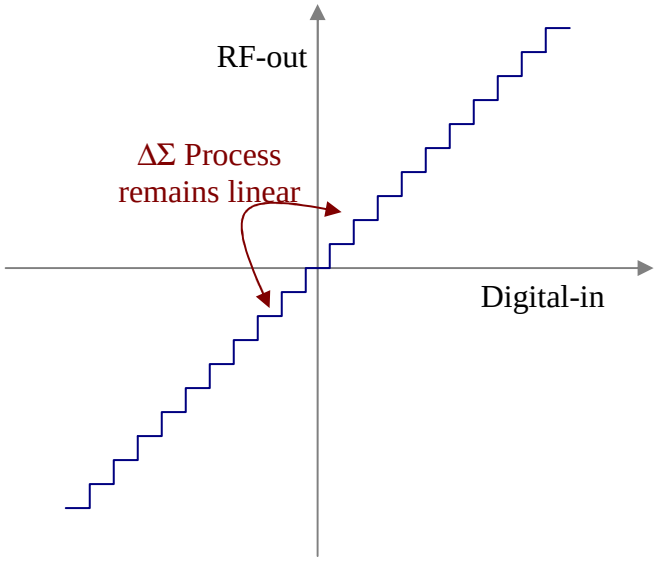


Figure 92. Effect of polarity on amplitude quantization - ΔΣ process remains linear near zero

The phase-feedforward strategy has a different effect on the amplitude path. With the polarity bit, the amplitude can be treated numerically as a bi-polar signal. Shown in Figure 91, the time- and frequency-domain representation are numerically different. However, this is only an artifact of the digital representation. Realistically, the amplitude path will require the same bandwidth as before to carry the envelope information. The benefit of polarity encoding is in the linearity of the ΔΣ noise-shaping

process. With polarity, the ΔΣ process does not saturate at zero amplitude. Instead, the noise-shaping process remains linear near zero amplitude since the trajectory can be negative. By preventing amplitude saturation at zero, the polar transmitter can generate near-zero amplitude signals without distortion. This allows the system to handle standards where the amplitude goes to zero (infinite peak-minimum ratio) more effectively than without polarity information.

6.5.5 ΔΣ Noise-shaping process

In this work, the ΔΣ modulator interfaces between the high-resolution baseband signal and the pulse-density modulator. The quantizer extracts 10 levels and the polarity of the 12-bit representation. A ROM decoder maps the bi-polar 10-level quantization to 4-bits with polarity for the next-stage PDM block. With the system clocked at the baseband frequency of 100MHz, peaks in the noise spectrum are offset from the carrier frequency by 50MHz.

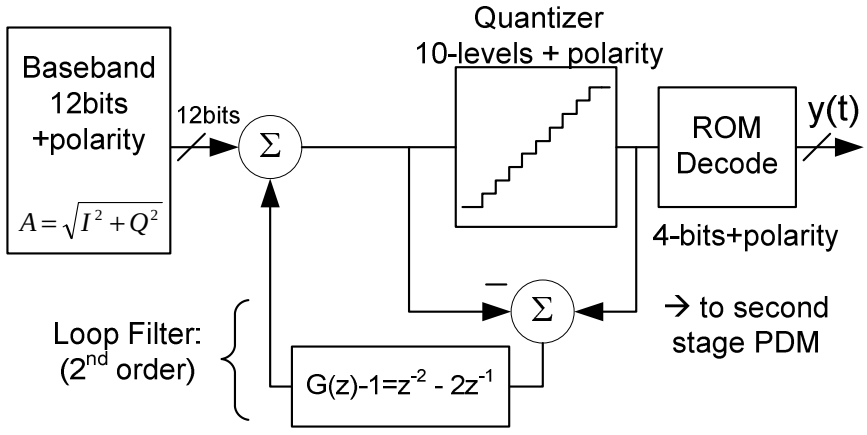


Figure 93. Error-feedback digital ΔΣ modulator

The $\Delta\Sigma$ modulator is implemented with a digital error-feedback structure, as shown in Figure 93. As discussed in section 6.3, the error feedback structure shapes quantization noise with transfer function $NTF(z) = \frac{Y(z)}{E(z)} = G(z)$, where the *error-transfer-function* is $G(z) - 1$ [99]. This provides flexibility in a fully digital system where it is straightforward to change the discrete-time *G(z)* FIR transfer function. In Figure 93, for example, $G(z) = \left(1 - z^{-1}\right)^2$, such that there are two zeros in the *NTF* at zero Hz.

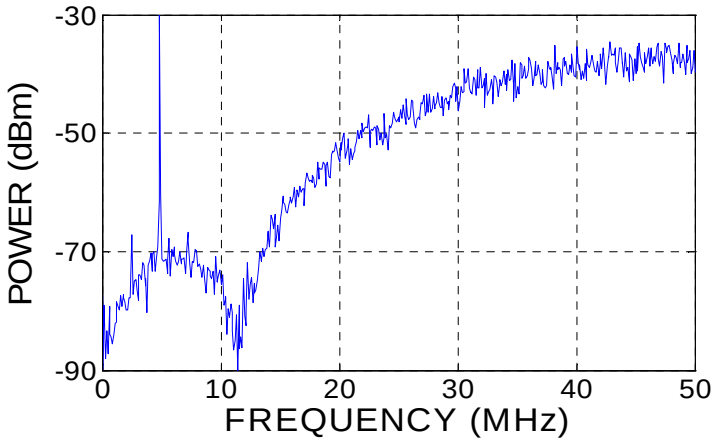


Figure 94. Example baseband 3rd order $\Delta\Sigma$ modulator spectrum with a notch at ±12MHz, $G(z) = -z^{-3} + 2.5z^{-2} - 2.5z^{-1}$

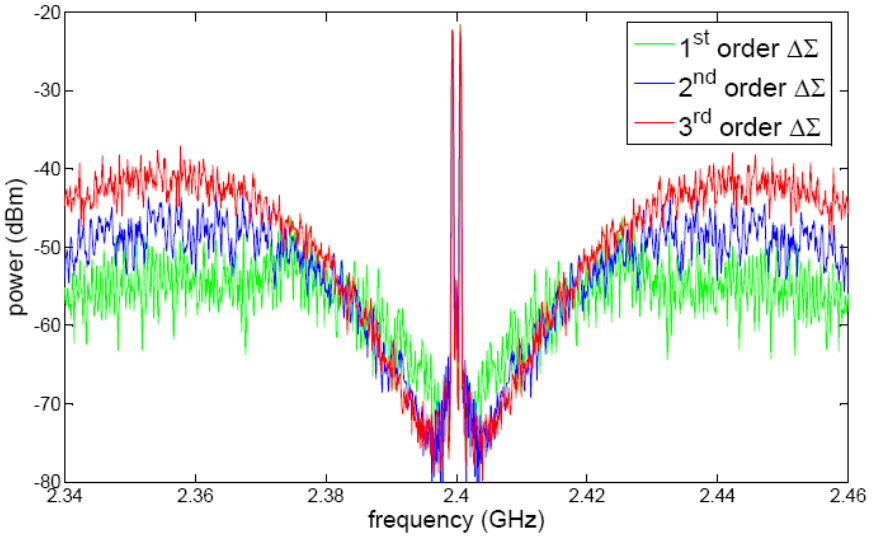


Figure 95. ΔΣ Modulator: 1st, 2nd, 3rd order comparison, all zeros at 2.4GHz

Figure 94 and Figure 95 highlight the flexibility of the error-feedback system. Figure 94 shows the simulated response of a third-order filter with two complex zeros and a zero at DC for a single tone at 5MHz. To flatten the in-band noise spectrum, a notch in the loop filter is placed approximately 12MHz from the carrier. Notches in the quantization noise spectrum may be useful to help meet spectral mask requirements in some circumstances. Unfortunately, higher order modulators also increase the peak (unfiltered) quantization noise that occurs near $f_0 \pm f_S$, where f_0 is the carrier frequency and f_S is the sampling frequency of the ΔΣ modulator. In many cases, the peak out-of-band noise is the limiting factor on spectral mask compliance. If so, lower order modulators can provide lower peak noise at the tradeoff of higher in-band noise.

Figure 95 shows the simulated frequency response of the system with various loop filters for a suppressed carrier AM signal. The 3rd order system has the lowest noise at

the center frequency, but highest peak out-of-band noise. The first-order system has lower peak out-of-band noise, but may have tones in the output spectrum for certain input signals. A second-order filter achieves both favorable noise-shaping and reduced possibility of tones in the output spectrum. The second-order filter was used in the experimental prototype.

6.5.6 Class-D PA

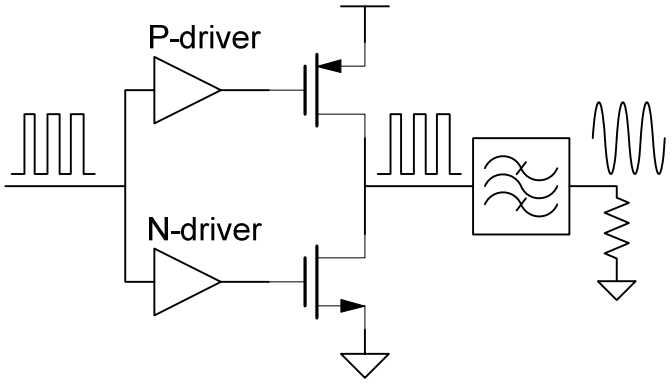


Figure 96. Complementary class D PA schematic

Switching power amplifiers traditionally use n-channel power devices because of higher mobility. This leads to smaller devices and lower switching losses. Class-E and class-F soft-switching techniques improve efficiency under normal circumstances by reducing power lost to reactive parasitic components [34]. However, these amplifiers rely on the output network to shape the voltage waveform across the active device. This can result in high voltage stress. Modern CMOS processes have fast active devices that are constrained by low breakdown voltages. In this scenario, the complementary class-D output stage has advantages over more traditional topologies.

Shown in Figure 96, by using a complementary output stage with active PMOS pull-up transistors, the drain voltage is a square wave. Importantly, the output stage is always low impedance looking back into the switching node. This enables high linearity in pulse-density operation and makes the class-D stage robust against impedance variation of the output network. Class-E and class-F topologies are sensitive to variation in the load impedance. Even if the output network is ideal, class-F topologies can only approximate a square wave by blocking various combinations of switching harmonics. In a realistic environment, these topologies are limited by oxide stress in the active devices as the drain voltage can swing above the supply voltage.

In [34], figures of merit are assigned to different switching amplifiers for comparison. Two important figures of merit (FOM) are related to the voltage and current stresses in the device:

$$F_V \equiv \frac{V_{pk}}{V_{DC}}, \tag{82}$$

$$F_I \equiv \frac{I_{rms}}{I_{DC}}. \tag{83}$$

In (82) and (83), V_{pk} and V_{DC} are the peak and DC voltages at the drain of the active device, and I_{rms} and I_{DC} are the RMS and DC currents. The F_V figure of merit is indicative of oxide stress in the active device. Higher F_V implies higher drain voltage swing relative to the supply. F_I is related to the efficiency of the amplifier topology. Higher RMS current levels from high peak currents result in increased resistive losses in the switches.

Table IV.
COMPARISON: FV-FI FIGURE OF MERIT FOR VARIOUS AMPLIFIER CLASSES
(DATA FOR CLASS E, F-1, F2,3,4,5 FROM [34])

Amplifier Class	F_V	F_I
E	3.56	1.54
F_{-1}	3.14	1.41
$E/F_{2,3,4,5}$	3.20	1.45
D	2.00	1.57

Table IV compares the class-D topology to other switching-class amplifiers. Oxide stress as a function of supply voltage is lower for class-D, especially compared to class-E. This allows the devices to deliver higher average power to the load for a given peak oxide stress. Since each switch has half-wave sinusoidal drain current, F_I is comparable to the other amplifier topologies. An important advantage of the class-D amplifier is that the output stage is always low impedance. Variation in the impedance of the output network caused by load pull from the antenna does not affect F_I and F_V ratios. This makes the class-D output stage robust against impedance variation compared to other switching amplifier topologies.

The traditional disadvantage of the complementary class-D topology is the use of p-channel devices with lower ft than the n-channel devices. This increases capacitance, reducing efficiency compared to NMOS-only topologies. However, in deep-submicron processes, p-channel devices may have ft in excess of 40GHz [2]. Device scaling further improves operation frequencies and reduces switching losses [1]. In this design the

advantage of using a low-impedance complementary output stage outweighs higher losses in the p-channel device.

Class-D is also more linear with pulse-density modulation than other amplifier classes. For the pulse-density modulation scheme, the class-D output stage has the advantage that the drain voltage waveform is not affected by pulse-skipping. For class-E or F, the startup time to achieve nominal steady state operation can lead to distortion. This second-order effect is caused by reliance on the output network to shape the drain voltage waveform. Voltage-mode class-D amplifiers force a nearly ideal drain voltage because the switching-node is always low impedance. Class-D amplifiers are less likely to need predistortion to compensate AM-AM and AM-PM distortion than class-E or class-F amplifiers due to inherent open-loop linearity in PDM operation.

6.5.7 CMOS Class D PA Implementation

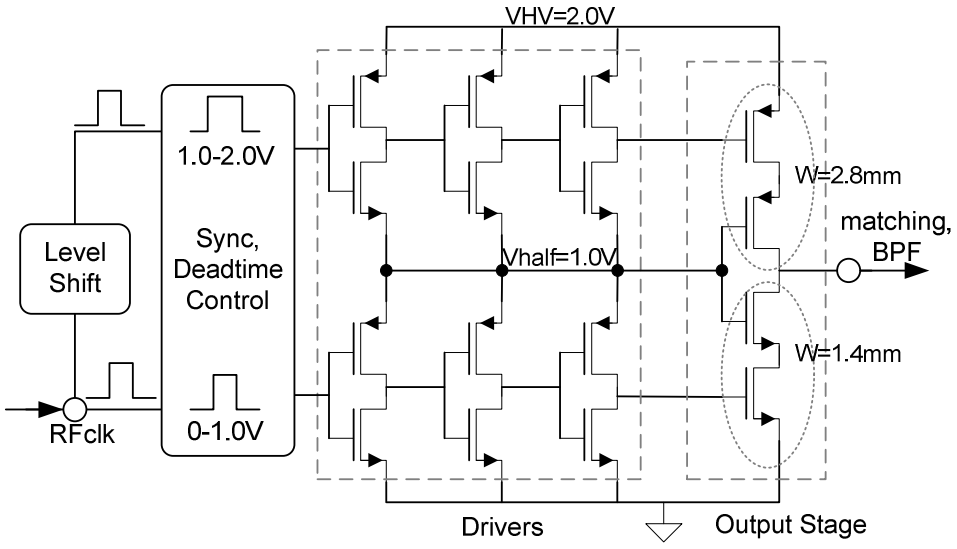


Figure 97. Schematic representation of class-D power amplifier with cascode output stage

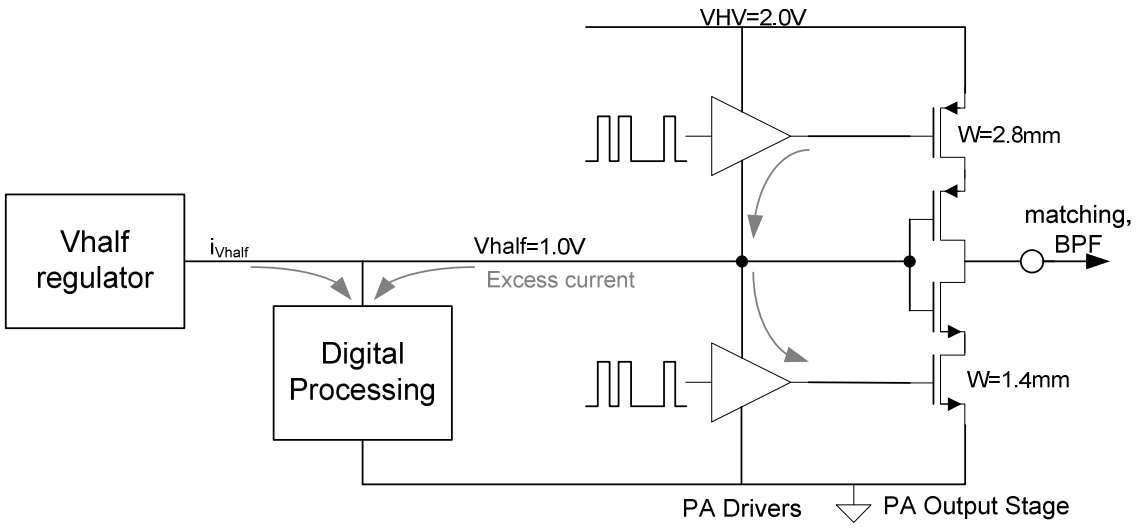


Figure 98. Current recycling scheme: excess current from PMOS drive stage used by digital processing

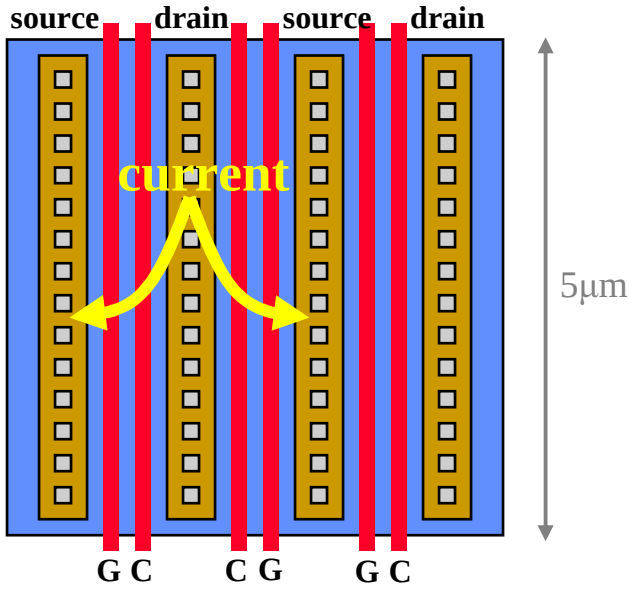


Figure 99. Class-D PA output stage NMOS layout: gate and cascode share diffusion region to reduce junction capacitance

Figure 97 shows the schematic of the CMOS class-D PA. To achieve higher output power, the output stage uses cascode devices, allowing higher voltage operation. The output devices are thin-oxide transistors with high f_t which can achieve higher efficiency

than thick-oxide devices for the same supply voltage [109]. The PA operates with a high voltage rail, *VHV=2.0V*, and a center voltage rail, *Vhalf=1.0V*. This limits the maximum oxide stress to 1.0V in normal operation.

Shown in Figure 98, the *Vhalf* node is shared by the high-side and low-side drivers such that current from driving the PMOS output device is reused to drive the NMOS device. There is typically excess current from the PMOS drivers because the PMOS is twice the size of the NMOS stage. The excess current can be used by the 1.0V digital processing block, provided that voltage transients are adequately filtered. The *Vhalf* node DC potential is regulated with an off-chip power supply. A 100pF on-chip bypass capacitor supplies high-frequency current from the *VHV* node. Similar bypassing is placed on the *Vhalf* node.

The output stage is sized for maximum efficiency at 100mW output power (20dBm) with balanced switching and conduction loss for 2.4GHz operation. The output stage is hard switched to maintain accurate control of the pulse-density modulation waveform. Hard switching is performed by inverter drivers, which are scaled with approximate fanout of three. Shown in Figure 99, each cascode device was built to share the diffusion region of the switching device in order to reduce parasitic junction capacitance at the cascode node. The finger width for both cascode and switch was 5µm to minimize gate resistance.

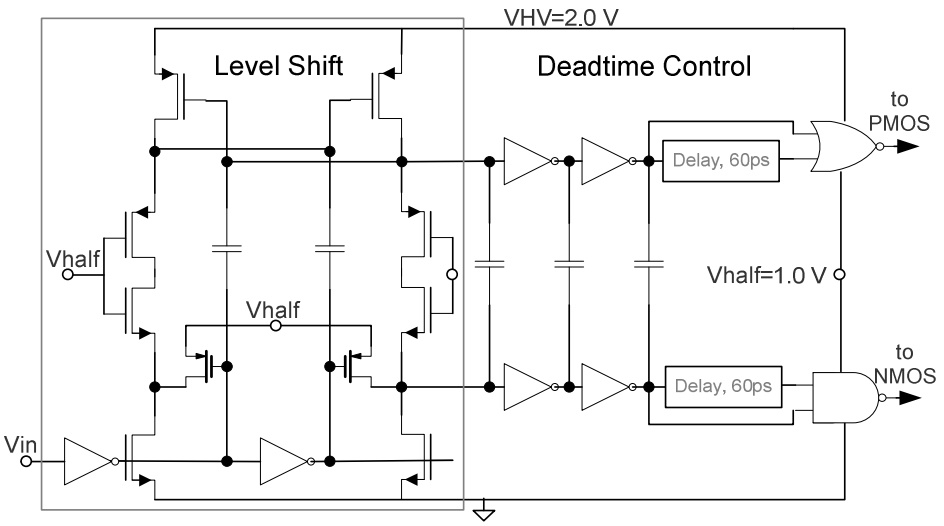


Figure 100. Level shift and deadtime control

The level shift block, shown in Figure 100, is used to interface the nominal 1.0V digital processing block to the PA output devices. The architecture is similar to that proposed in [109]. Latching structures were used to restore signal swing on intermediate nodes. Coupling capacitors increase frequency response of the digital signals. Deadtime control is implemented with fixed delay of 60ps in the high-side and low-side signal paths. The deadtime circuit prevents shoot-through current and synchronizes the output stage voltage waveforms. The 60ps deadtime optimizes power efficiency while providing a reasonable buffer for process and temperature variation. In the deadtime circuit, capacitors are placed between the high-side and low-side signals to assure proper time-alignment.

6.5.8 System Implementation

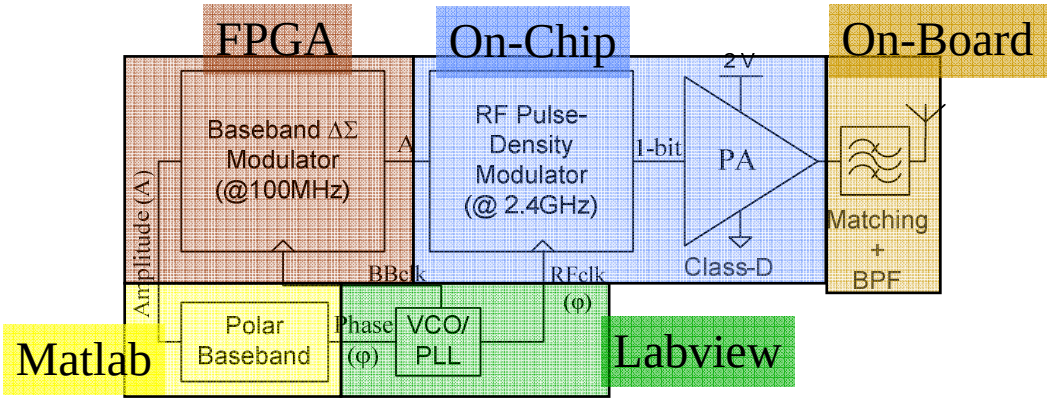


Figure 101. System-level implementation of Bluetooth transmitter

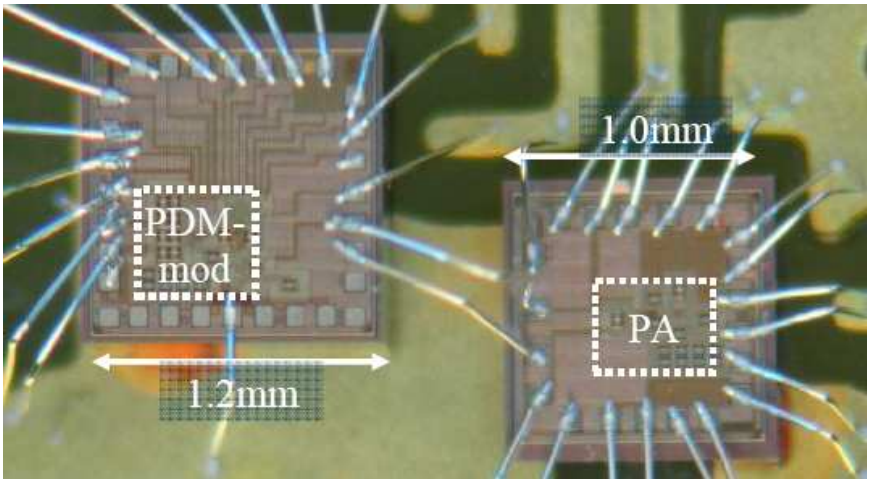


Figure 102. Die Photo of CMOS class D PA and RF pulse-density modulator circuits

The system is implemented with two test chips in 90nm CMOS. A first chip contains the class-D PA and drivers (active area 0.15mm^2). A second chip contains the PDM structure, synchronization, clock recovery and ROM (active area 0.2mm^2). A die photo is shown in Figure 102. The baseband and ΔΣ modulator are implemented in an FPGA.

The system is tested with a Labview PXI setup with RF upconverter and downconverter. The labview system and FPGA use a synchronous clock to perform time-alignment of the amplitude and phase signals. The output filter is implemented off-chip and consists of a traditional L-matching network and an additional bandpass filter component. The bandpass filter is a Johanson 2450BP41D100B component for the 2.45GHz band with 1.3dB maximum insertion loss.

6.5.9 Experimental results

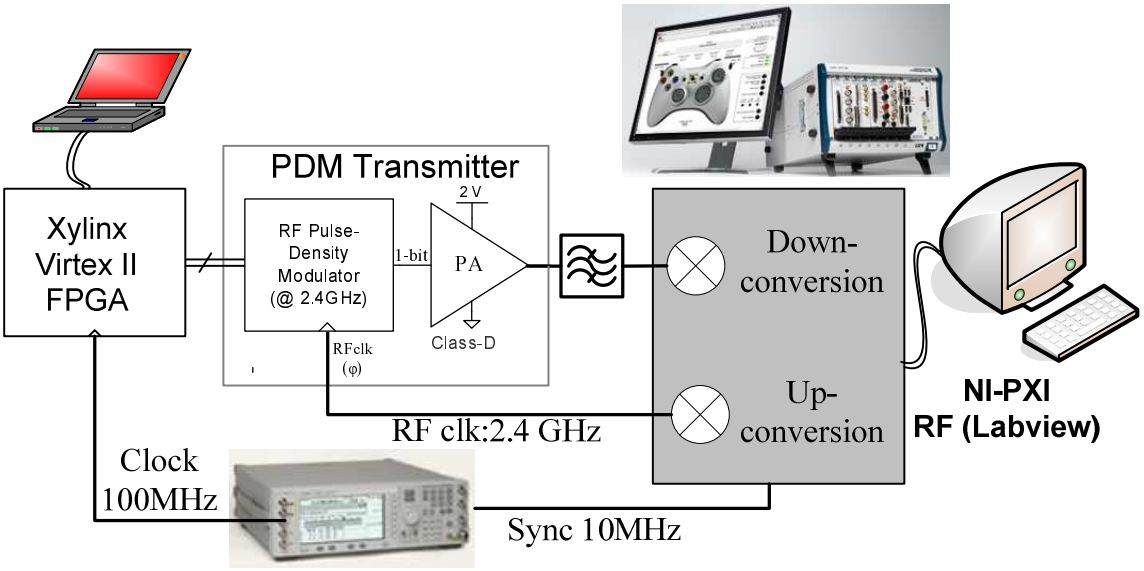
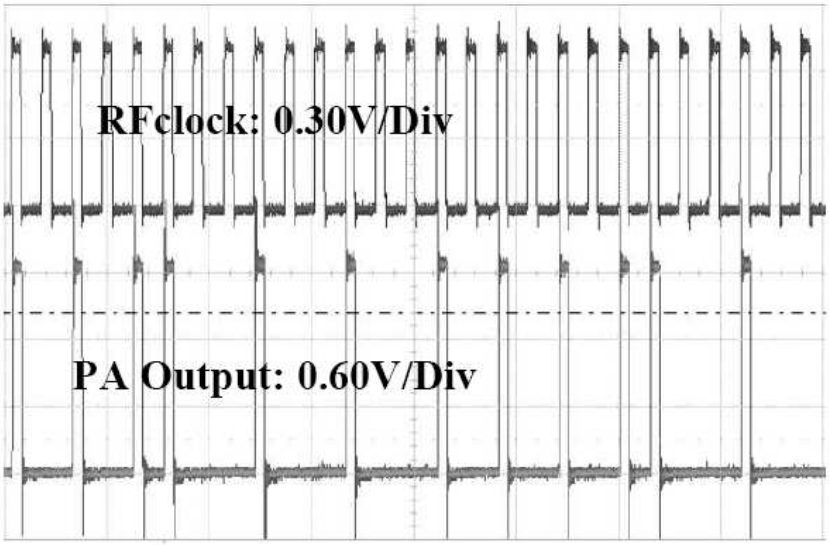


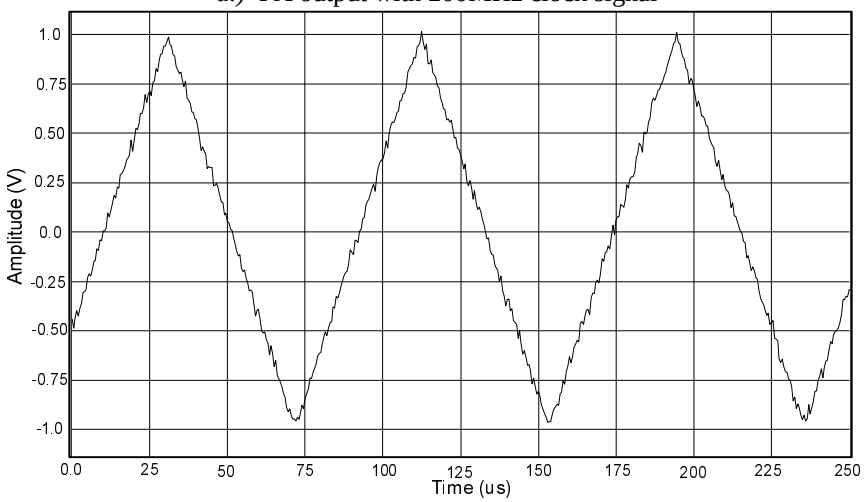
Figure 103. Block diagram of the experimental setup

The experimental setup is shown in Figure 103. The amplitude path of the digital polar transmitter is controlled by a Xylinx FPGA. The RF clock containing phase information is implemented in Labview and supplied directly to the chip. The Labview upconverter is synchronized to the FPGA with an external agilent RF source. The RF source is also used to synchronize the amplitude and phase paths in the polar system.

The phase of the RF clock is adjusted until the system reaches maximum EVM performance.



a.) PA output with 200MHz clock signal



b.) Downconverted transmitter output with 2.4GHz clock, linear ramp signal programmed into amplitude path

Figure 104. Time-domain waveforms at transmitter output

Figure 104 shows time domain waveforms at the output of the system. Figure 104-a shows the screen capture of an oscilloscope waveform at the output of the PA during PDM operation. The system clock is slowed to 200MHz to enable the oscilloscope to

capture the RF waveform. The PA output is shown to skip pulses to create the amplitude-modulated output of the system.

Figure 104-b shows the output of the polar transmitter after the Labview downconverter with 2.4GHz carrier frequency. The amplitude signal is programmed to be a full-scale linear ramp signal with polarity. After the downconverter, the linear ramp matches the desired pattern without deviation or noticeable distortion. The polarity of the envelope signal changes at zero amplitude demonstrating operation at ± full scale.

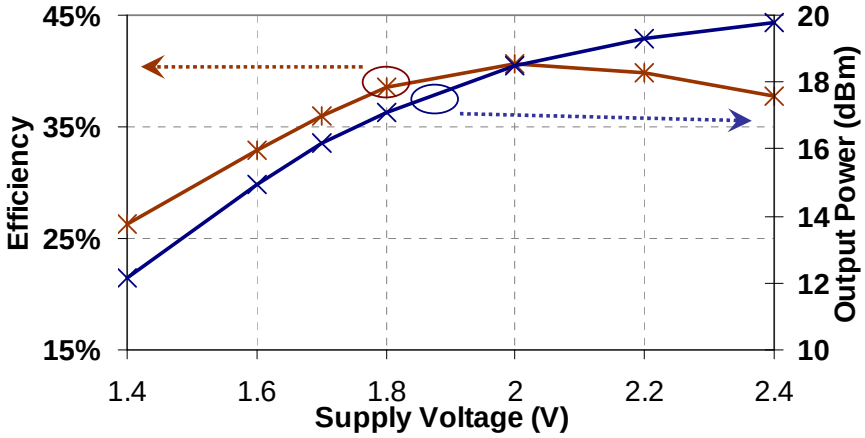


Figure 105. Efficiency and output power vs supply voltage

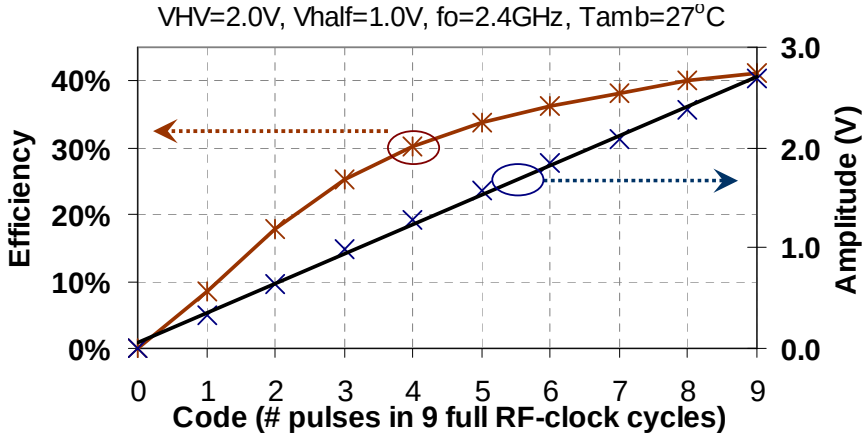


Figure 106. Efficiency and linearity vs pulse-density

Figure 105 shows the total output power and efficiency of the class-D PA across supply voltage with full modulation (peak power). Here, efficiency includes power of the PA drivers and loss in the matching network, but does not include insertion loss of the bandpass filter. The peak output power of 20dBm occurs for the maximum supply voltage of 2.4V (maximum oxide stress of 1.2V). The peak efficiency of 40.7% occurs for a supply voltage of 2.0V. With the bandpass filter included, peak efficiency was measured at 38.5%. Figure 106 shows linearity and efficiency at each of the 10-levels of amplitude quantization. Linearity for the PA is high with pulse-density modulation. Importantly, efficiency stays higher at lower power levels than with typical class A/AB power amplifiers. Efficiency of the PA, including driver power, stays above 25% for 10dB power backoff.

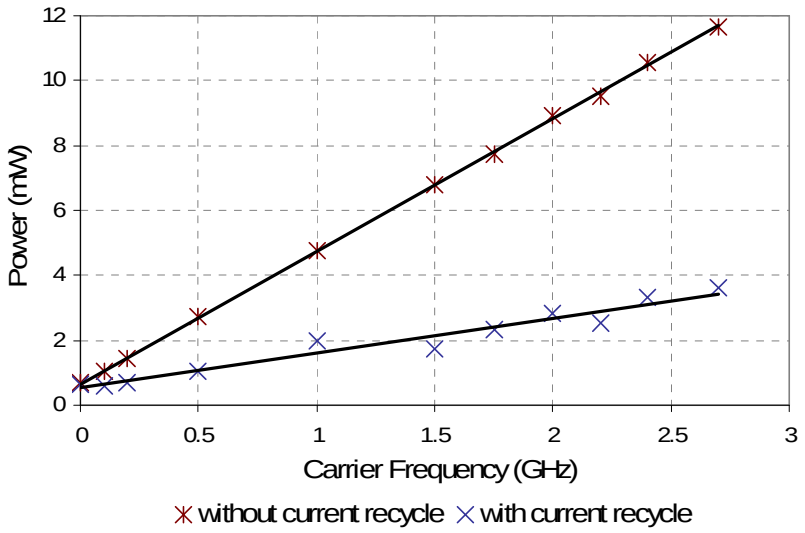
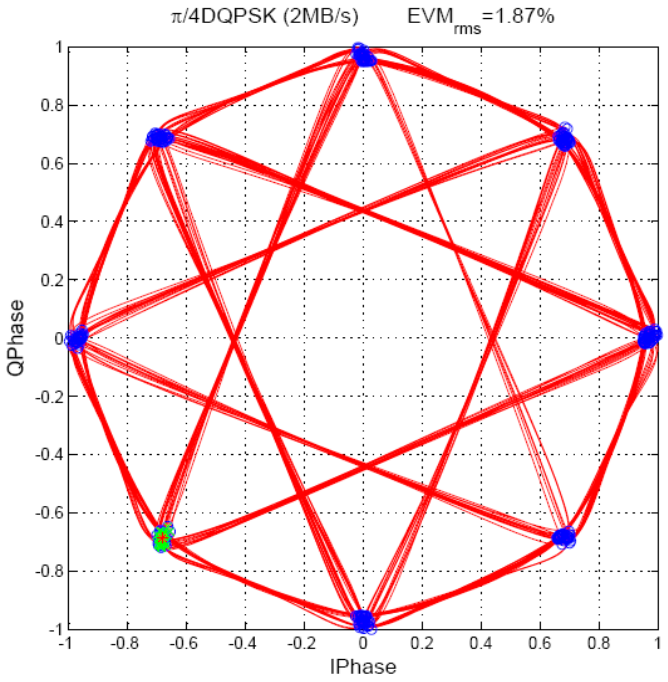


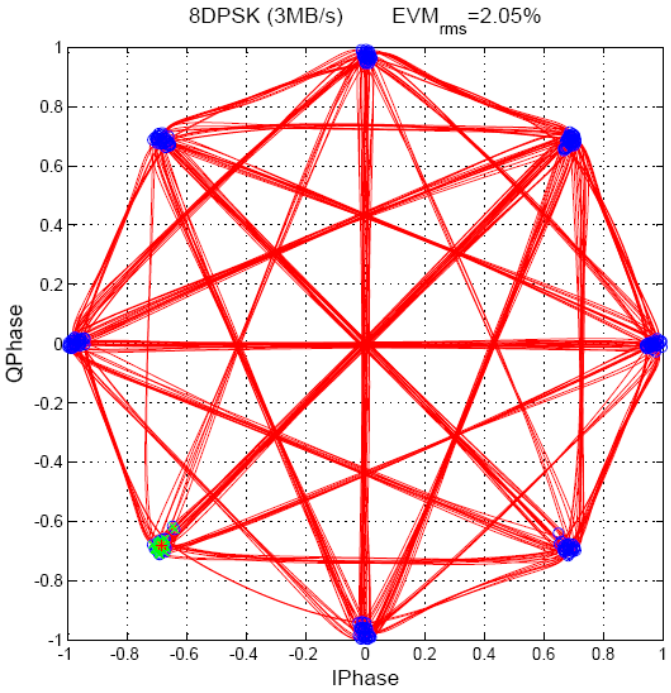
Figure 107. Power of digital processing (pulse-density modulation, clock recovery, sampling and synchronization) with and without current recycling scheme. Measured as power drawn from Vhalf regulator

The average efficiency of the system is further improved with a current recycling scheme. Shown in Figure 98, since the *Vhalf* node in the PA operates at 1.0V, this node can be shared with the 1.0V V_{DD} node. This allows excess current from driving the PMOS power device in the PA is used to power the remaining 1.0V circuitry. At 2.4GHz this reduces the current drawn from the 1.0V supply from 11.7mA to 3.7mA. The current recycling scheme allows the entire system to operate with 30% average efficiency for π/4DQPSK and 8DPSK modulated signals with approximately 3dB PAPR.

Low digital processing power and high average efficiency make this scheme amenable to low-power portable wireless standards, such as Bluetooth. Comparable work published in the literature achieves higher spectral fidelity at the tradeoff of significantly higher power consumption. Reference [106] demonstrates a system with $\Delta\Sigma$ DACs operating at 5.4GHz that meets cellular coexistence requirements for 802.11b/g and 802.16e. Digital processing power is in excess of 100mW for rms output power of 2.6dBm. The solution presented here requires between 2-5mW for the digital PDM block for 12-14dBm rms power levels.



a.) π/4DQPSK (2MBPS)



b.) 8DPSK (3MBPS)

Figure 108. Measured constellation diagrams

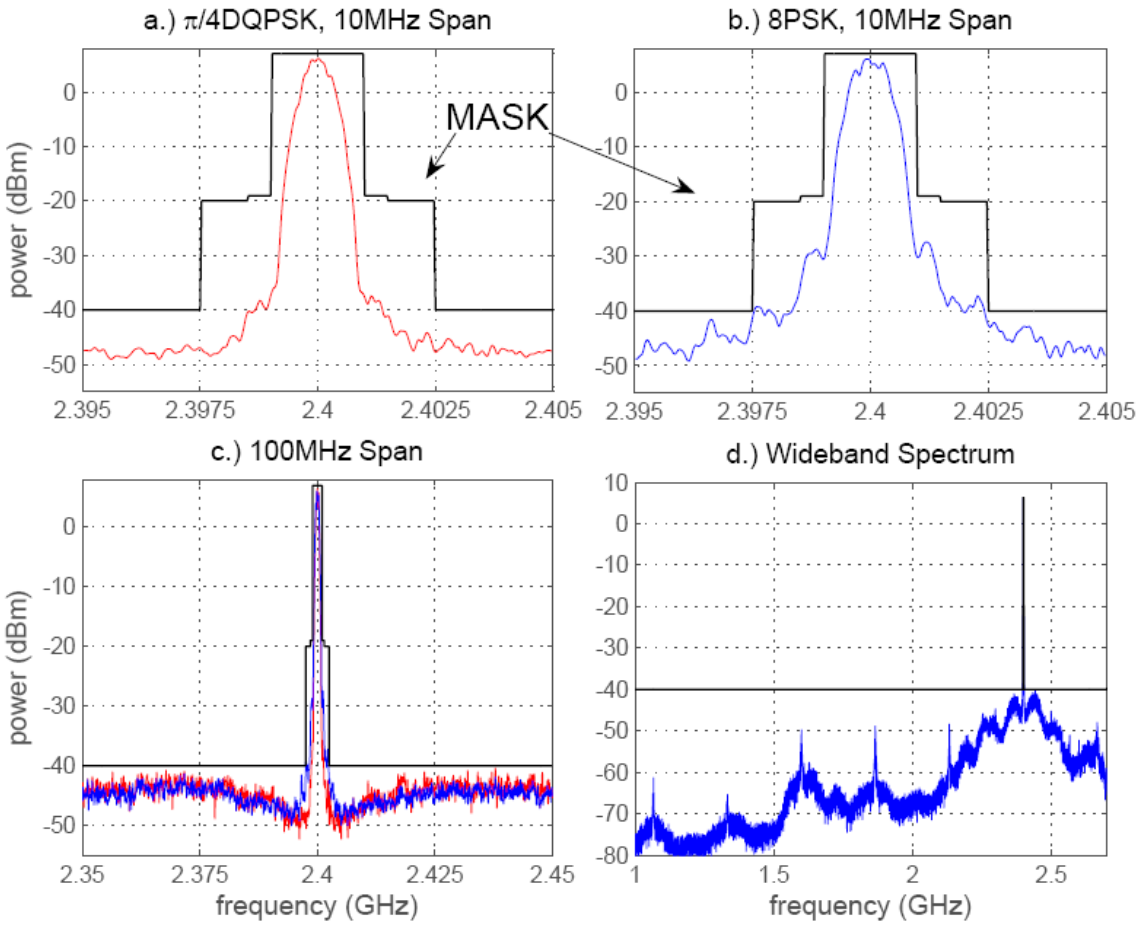


Figure 109. Efficiency and output power vs supply voltage

Figure 108 shows the measured constellation diagram for π/4DQPSK and 8DPSK test vectors. These test signals meet the requirements of the Bluetooth 2.1+EDR standard for the 2MBPS and 3MBPS datarates [9]. Measured EVM for π/4DQPSK is $EVM_{rms} = 1.8\%$ and $EVM_{peak} = 2.8\%$. For 8DPSK, $EVM_{rms} = 2.1\%$ and $EVM_{peak} = 2.9\%$. As seen for the 8DPSK data in Figure 108-b, the transmitter is capable of generating constellation trajectories that pass through the origin (infinite peak-minimum ratio). The system remains linear near zero amplitude, minimizing low amplitude distortion by synchronizing polarity

shifts with the digital polarity bit in the amplitude path. This significantly reduces the bandwidth requirements of the phase modulator and improves performance for high PAPR signals.

Quantization noise of the digital modulator is a limiting factor for spectral performance. Figure 109 a-d.) shows that the nearband spectral requirements for Bluetooth 2.1+EDR are satisfied for both π/4DQPSK and 8DPSK test signals. Average power levels at the spectrum analyzer are between 11-14dBm. The wideband spectral mask is satisfied due to the addition of the bandpass filter at the output. However, it should be noted that in peak-hold mode, which is required for the Bluetooth standard, there is little margin for the -40dBm power limit (100kHz RBW). Shown in Figure 109 c.), the lowest margin occurs near peaks in the quantization noise spectrum 50MHz from the center frequency. Low margin in the spectral mask could make the system susceptible to load pull, power supply variation, or other scenarios which cause wideband noise levels to increase. This can be improved by operating the ΔΣ process at higher clock frequencies, or reducing transmitter power level. In a fully-integrated version, it may be practical to operate the ΔΣ modulator at 250MHz or more, reducing the peak noise by 3-10dB. Due to limited margin in meeting the spectral-mask, we do not present this as a fully-functional Bluetooth transmitter, but rather a demonstration of a new and interesting topology worthy of further investigation. The high efficiency and excellent linearity show that this is a promising alternative to traditional Cartesian and polar transmitters.

Chapter 7 Conclusion and Future Work

Digital radio architectures show tremendous promise for future generations of wireless communications devices, but further research is needed to be directly competitive with the spectral performance of existing hardware. Our research demonstrates a solution that is significantly more energy efficient than existing transmitter topologies and meets the requirements of a high-datarate digital wireless standard. We achieve average (energy) efficiency in excess of 30% with EVM just over 2% for the π/4DQPSK and 8DPSK Bluetooth constellation. The limiting factor for our solution is spectral compliance. Artifacts from the quantized, discrete-time representation of the RF vector signal result in quantization noise and sampling images that are difficult to filter. To extend this technology to other wireless standards including cellular, WiFi, and WiMax it is necessary to further improve the wideband spectral performance.

Fortunately, scaling trends are in the favor of this type of solution. By operating the sampling process at higher frequencies, quantization noise is reduced both in and out of band. Also, filtering at the output is more successful in removing noise power. Additional circuit techniques will also have success in improving performance. A promising direction combines this work with the work presented in [38], [105], and [106]. Specifically, this would combine techniques presented here in Chapter 6 with a

multi-bit power amplifier. With voltage-mode power combining, the outputs of multiple power amplifiers can be combined to create a multi-bit RF DAC. Each additional bit will reduce out-of-band noise relative to peak power. Power combining also helps the PA achieve higher power for a given supply voltage [39]. Both outcomes may be necessary for future all-CMOS transmitters.

Regarding the work in Chapter 5 on hybrid voltage regulators, we propose a new operating strategy that promises substantially higher efficiency for supply modulated polar systems. However, more work is required to fully implement this concept in a hardware solution. There are significant research components remaining in this area, including how to determine the DC-DC current trajectory for rapid variation in the envelope signal. We see opportunities for feedforward control in this area. With an accurate model of the load, the current trajectory could be pre-computed on-line. This could maximize efficiency for the available switching regulator bandwidth.

Here we have presented several pieces of research that add to the body of knowledge of transmitter technology. The overall theme is connected through improving the performance and, ultimately, energy efficiency of wireless transmitter blocks. While these are only small steps in the broader goal of fully-integrated low power digital radio systems, they should provide a solid basis for further academic and commercial research in this area.

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