mm-Wave Quadrature Spatial Power Combinig: A Proposal

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1 Introduction

Traditional PA design involves a trade-off between efficiency, linearity, and output power. When transistors are operated in class A/AB, good linearity results, whereas when transistors are operated as switches, such as Class C/D/E, the linearity suffers. The normalized output power (relative to transistor stress) of switching mode amplifiers is lower, but larger devices are tolerable if the switch parasitics can be absorbed into the load tuning network (Class E). In recent years a great deal of research has focused on breaking this trade-off by employing transmitter architectures (Polar Loops, LINC, Cartesian feedback) that can utilize non-linear switching amplifiers while restoring signal linearity through feedback or through feedforward load supply modulation. While these techniques have been moderately successful at RF frequencies, extension of these techniques to mm-wave frequencies presents many challenges.

To begin with, relatively little work has been done on switching PAs at mm-wave frequencies, with the majority of demonstrations (especially in Si) utilizing class A operation. Moreover, any transmitter topology that utilizes load supply modulation will have a limited bandwidth in the DC-DC converter in order to achieve reasonable efficiency. Modulation bandwidths over 10 MHz are particularly challenging even for RF applications. High f_T transistors have lower breakdown voltages, requiring proportionally higher currents to reach the same output power, which requires larger devices (higher parasitics) and in turn limits the maximum frequency of operation. Moreover, low breakdown voltages require larger transformation ratios in the matching networks to realize hight output power, which again leads to higher losses.

For these reasons, the performance of mm-wave PAs have fallen short of RF PAs in both output power capability and efficiency. The output power is limited since the device width cannot be arbitrarily large due to the capacitive parasitics. The power is also limited by the quality factor of components, especially in silicon, which ultimately limits the achievable impedance transformation ratio (due to the losses in the matching networks). The efficiency is poor because of a multitude of loss mechanisms, including resistive losses in the metal lines, losses in matching/tuning networks, and low device power gain when operating close to the activity limits, which degrades the PAE of the PA due to increased input power drive.

2 Digital PA Architectures

In a digital PA, a discrete number of sub-PAs are switched in and out of the the circuit in order to provide amplitude modulation, replacing the supply modulation used in a polar transmitter [1][2]. Each individual PA is a non-linear switching mode PA which can relay constant envelope phase information. It is important to realize that the core PA is not "digital", but is an analog PA operating at the carrier frequency. The digital process is introduced by switching the PAs into and out of the circuit. This process is not done at the carrier frequency, but rather at the rate of the envelope of the signal, which is usually at least an order of magnitude slower (100 MHz - 1 GHz in this proposal).

The resolution of the digital PA is determined by the required EVM and spectral mask. For instance, a 2.5% EVM requires only about 6-bits. The resolution is usually constrained by the nearby out of band emissions, which is difficult to filter. Often the modulation bandwidth is much

lower than the carrier frequency, in which case oversampling can be used to lower the quantization noise. While the digital PA is "linear" in theory (in quantized steps), in practice the input/output AM-AM characteristics exhibits compression due to the code dependent output impedance. There is also AM-PM distortion arising from the change in the effective output capacitance as a function of code word. In practice the digital PA is easily linearized by employing two static AM-AM and AM-PM pre-distortion tables. Since each input signal is digital, this predistortion is easily implemented. The difficulty in the digital polar PA is the phase path, which experiences bandwidth expansion due to the $\tan^{-1}$ non-linearity (roughly a 7X increase). For this reason, we are proposing a new spatial Cartesian architecture.

3 Quadrature Spatial Power Combining

To realize both efficient and linear operation, we propose quadrature spatial combining. In this architecture the quantized amplitude is reconstructed at the output of the PA by modulating the number of "on" non-linear cores, thereby efficiently conveying linear amplitude information onto the RF carrier. The phase is conveyed by adding the in-phase (I) and quadrature phases (Q) of the signals together using two separate PAs. This signal is summed spatially as shown in Fig. 1.

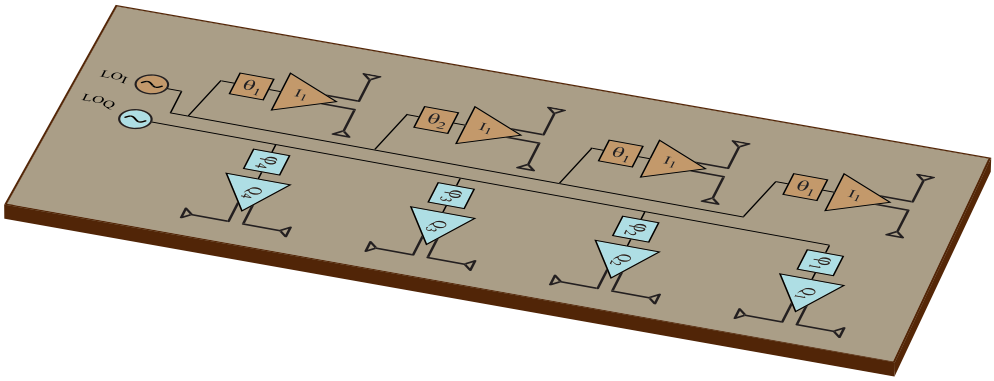


Figure 1: Conceptual diagram of digital quadrature spatial combining using an on-chip antenna array.

This architecture is motivated by the requirement to linearly amplify high bandwidth (100 MHz - 1 GHz) signals at high frequencies (45 GHz - 138 GHz). A distributed approach to the device layout and design is used to realize highly efficient mm-wave switches and power combiners. In contrast to traditional PA design, mixed-signal and mm-wave approaches are used synergistically to realize power and performance levels outside the realm of traditional mm-wave PAs. Transformer power combining [3][6] and the Distributed Active Transformer (DAT) [4] have helped CMOS PAs to deliver over 1W below 10 GHz. Extending these structures to higher frequencies is not trivial. By splitting the cores into discrete sub-cells, we can digitally control the output power in fine steps in order to convey amplitude and phase modulation onto the signal. This is very important because it allows each sub-cell to be operated in optimal efficiency non-linear and switching class of amplification (class D^{-1}, class E/F).

While in theory a digital PA is linear (within an LSB), we will show that a practical implementation introduces non-linearity which must be compensated through pre-distortion. The pre-distortion algorithms for a digital PA are simpler than an analog PA. The key realization is that the non-linearity is due to well-known DNL/INL mechanism arising from a transistor operating in on/off condition, as opposed to detailed dynamic device behavior, which arises from the varying output impedance of the RF DAC as a function of input code. We believe that the digital PA will exhibit less memory effects which is key requirement in simplifying the digital predistortion algorithm.

By employing signals in the digital domain all the way up to the PA, we essentially realize the entire transmitter chain without mixers and other analog/RF building blocks, greatly reducing the complexity and power of the system. Powerful signal processing can condition the signal for optimal performance with minimal power penalty. In many applications, the digital part of the chip can be over-sampled to reduce quantization noise.

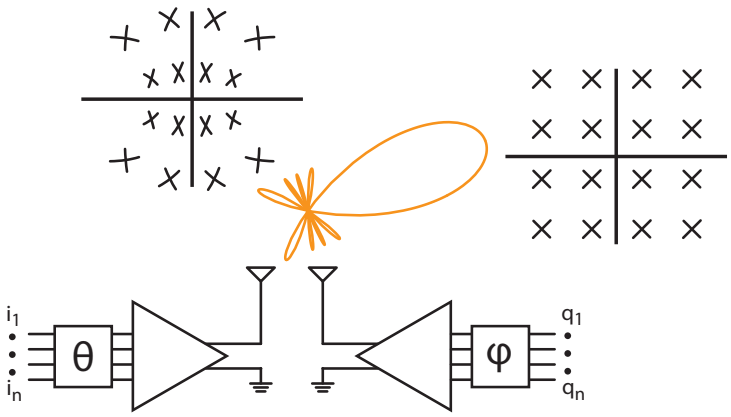


Figure 2: Quadrature Digital Spatial Combining is used to create a QAM signal in the desired direction. Other directions will experience a QAM distortion, making it harder to eavesdrop on the communication link.

Spatial power combining is an attractive solution for the realization of extremely high power levels, especially at mm-wave frequencies. The problem with spatial power combining is that signals need to be routed off the chip and into a separate substrate where the antennas reside. Low loss packaging above 100 GHz is non-trivial if we are targeting an efficiency greater than 50%. Assuming that signals can be routed off chip with an insertion loss of about 1 dB, or 80% efficiency, requires the core PA to have more than 65% efficiency (assuming the antenna has 100% efficiency for simplicity), a difficult challenge, even at 1 GHz. To solve this problem, we propose on-chip antennas and spatial power combining. For example, as shown in Fig. 2, several bits of I and Q signals can be combined in space to provide a QAM signal in the desired direction. Similar to the work presented by [5], the constellation is distorted for other undesired directions, making it harder to eavesdrop on the transmission. Even though on-chip antennas today are inefficient, due to surface waves and substrate losses, our research shows that wafer thinning and highly resistive substrates can greatly enhance the antenna radiation efficiency, which may allow a phased-array solution to provide high power levels and high efficiencies.

Spatial quadrature combining, conceptually shown in Fig. 1, has the potential to greatly simplify the design of the digital PA, perhaps even eliminating the need to do substantial power combining on-chip. Each in-phase and quadrature-phase signal is first oversampled and filtered digitally (to eliminate spectral lines and meet ACPR specifications). A group of the least significant bits are then combined on-chip while the remaining bits are thermometer coded and drive an array of antennas, each antenna driven by a single bit. These thermometer bits then gate highly efficient non-linear class E/F core PA's driving the antennas directly. By co-designing the antennas and PAs appropriately we minimize the need for impedance matching, thus improving the efficiency of the transmitter. Phase shifters delay the carrier driving the non-linear cores in such a manner to produce two antenna patterns in space. The digital bits from the I and Q are in essence combined in space. For example, assume that 10-bits are required to meet the EVM/ACPR specifications. Then if 4-bits are binary coded and the rest are thermometer coded, the array size for each I and Q path consists of 65 antennas. Since the phased-array has a spatial (directive) gain, only the receiver in the desired position will receive the I and Q pattern of bits coherently and thus the spatial quadrature combiner also has the extra benefit of preventing eavesdropping. These benefits together make this approach attractive. The key missing component is an efficient on-chip antenna, which we discuss next.

3.1 Example of Antenna Design

The main challenge facing integrated antennas on silicon substrates is low radiation efficiency, which has been shown to be less than 10% [7] for moderately conductive substrates. Conduction loss owing to the low resistivity of the silicon substrate and surface wave mode excitations caused by thick silicon substrates with high permittivity [8] account for most of this loss. From 3D EM simulation, wafer thinning techniques and the application of highly resistive substrates can greatly enhance the antenna radiation efficiency, which may allow a phased-array solution to provide high power levels and high efficiencies. High resistive (HR) silicon substrates, such as the SOI substrate, makes it possible to achieve a fully integrated transceiver with on-chip antennas having relatively high radiation efficiency [9][10].

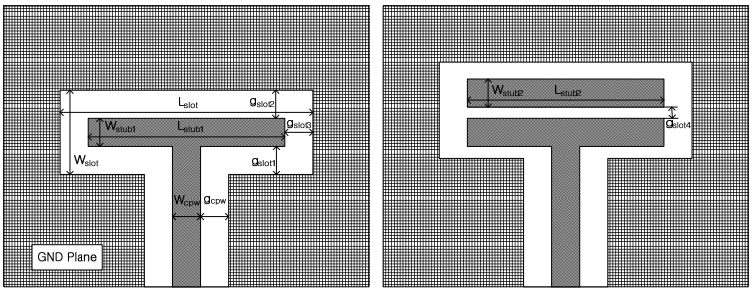
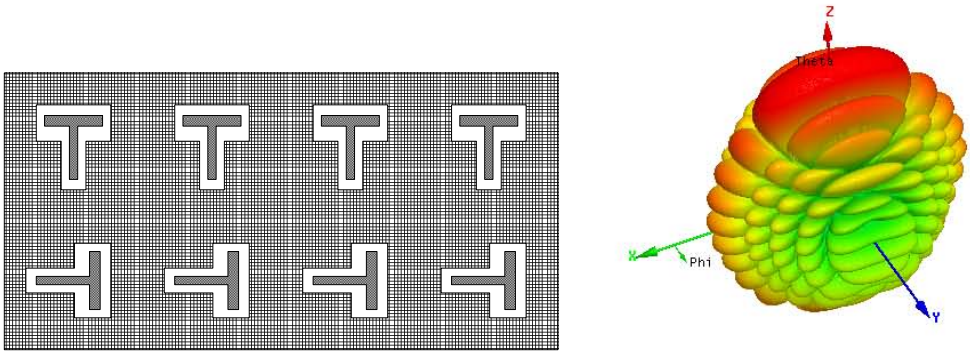


Figure 3: Folded slot antenna with single and double stub.

To test the validity of these assumptions, we have done some early stage research on feasibility of on-chip antenna structures. Fig. 3 presents a designed folded slot antenna with single stub at

45 GHz in a commercial 130nm SiGe process.[1] The input impedance of the folded slot antenna is well matched to 50Ω. The radiation efficiency is 90 % when the resistivity of the silicon substrate is assumed to be 1000 Ω-cm.

The radiation efficiency degrades to 76 % under the infinite array condition, possibly due to surface-wave mode excitation. Fig. 4a presents an array example for I and Q antennas. By using different polarization, one array is set to be collinear and another is linear to achieve better isolation between I and Q antennas. For the unit cell element, the isolation between vertically polarized and horizontally polarized antenna was -41 dB at 45 GHz. Fig. 4b shows the radiation pattern of the 16×16 array with master-slave boundary condition in HFSS. The resulting maximum antenna gain is 19 dBi.



(a) (b)

Figure 4: (a) Simulation setup for an I / Q spatial array using the folded slot antenna. (b) Radiation pattern of 16 by 16 antenna array using master-slave boundary condition.

[1] $L_{slot} = 1480\mu$m, $W_{slot} = 35\mu$m , $L_{stub1} = 1210\mu$m, $W_{stub1} = 20\mu$m, $W_{cpw} = 10\mu$m, $g_{slot1} = 7.5\mu$m, $g_{slot2} = 7.5\mu$m, $g_{slot3} = 135\mu$m. For double folded slot antenna, $L_{stub2} = L_{stub1} = 1210\mu$ m, $W_{stub2} = W_{stub1} = 10\mu$m,$g_{slot4} = 7.5\mu$m.

References

[1] A. M. Niknejad and R. G. Meyer, "Integrated RF Power Amplifiers for Wireless Applications: Integrated EER Proposal," presetned at Lucent, Auguet 1997.

[2] P. Cruise, Chih-Ming Hung, R.B. Staszewski, O. Eliezer, S. Rezeq, K. Maggio, D. Leipold, " A digital-to-RF-amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," *RFIC Digest of Papers*, 2005, pp. 21-24.

[3] G. Liu, T-J. King, A. M. Niknejad, "A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement," *Proceedings of CICC*, 2006, pp. 141-144.

[4] I. Aoki, S. D. Kee, D. B. Rutledge, A. Hajimiri, "Distributed Active Transformer-A New Power-Combining and Impedance-Transformation Technique," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, Jan 2002, pp. 316-331.

[5] A. Babakhani, D. B. Rutledge, A. Hajimiri, "A Near-Field Modulation Technique Using Antenna Reflector Switching," *IEEE International Solid-State Circuits Conference*, pp. 188-189, Feb. 2008.

[6] P. Haldi, D. Chowdhury, G. Liu, A.M. Niknejad, "A 5.8 GHz Linear Power Amplifier in a Standard 90nm CMOS Process using a 1V Power Supply," *RFIC Digest of Papers*, 2007, pp. 431-434.

[7] A. Shamim, P. Popplewell, V. Karam, L. Roy, J. Rogers, C. Plett, "5.2 GHz On-Chip Antenna/Inductor for Short Range Wireless Communication Applications," *2006 IEEE International Workshop on Antenna Technology Small Antennas and Novel Metamaterials*, pp. 213-216, 2006.

[8] D. Pozar, "Considerations for millimeter wave printed antennas," *IEEE Transactions on antennas and propagation*, vol. 31, pp. 740-747, 1983.

[9] M. H. Barakat, F. Ndagijimana, C. Delaveaud, "On the design of 60 GHz integrated antennas on 0.13μm SOI technology," *2007 IEEE International SOI Conference*, pp. 117-118, 2007.

[10] S. Montusclat, F. Gianesello, D. Gloria, "Silicon full integrated LNA, filter and antenna system beyond 40 GHz for MMW wireless communication links in advanced CMOS technologies," *2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*.

[11] T.M. Weller, L. Katehi, G. Rebeiz, "Single and double folded-slot antennas on semi-infinite substrates," *IEEE Transactions on Antennas and Propagation*, vol. 43, pp. 1423-1428, 1995.