Millimeter-Wave Circuits for 60GHz and Beyond

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Technical Report No. UCB/EECS-2010-113
http://www.eecs.berkeley.edu/Pubs/TechRpts/2010/EECS-2010-113.html

August 12, 2010

Acknowledgement

First and foremost I wish to express my deepest gratitude to my research advisor Professor Ali M. Niknejad. This work would not be possible without his continuous support and guidance. I would also like to thank my other thesis and qualifying exam committee members, Professor Jan Rabaey, Professor Paul Wright and Professor Seth Sanders. I would like to thank Professor Haideh Khorramabadi for her continuous support during my PhD at Berkeley. My especial thanks go to my colleagues, Ehsan Adabi, Amin Arbabian, Babak Heydari and Mounir Bohsali. I would also like to thank other members of the 60GHz and TUSI team, especially Cristian Marcu, Maryam Tabesh, Jun-chau Chien, Shinwon Kang and Steven Callender. Most importantly, I would like to thank my dear parents and my brothers, Babak and Arash.

Millimeter-Wave Circuits for 60GHz and Beyond

by

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B.S. (Sharif University of Technology) 2004
M.S. (University of California at Berkeley) 2007

A dissertation submitted in partial satisfaction of the
requirements for the degree of
Doctor of Philosophy

in

Engineering–Electrical Engineering and Computer Science

in the

GRADUATE DIVISION
of the
UNIVERSITY of CALIFORNIA at BERKELEY

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Spring 2010

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University of California at Berkeley

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Abstract

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Doctor of Philosophy in Engineering–Electrical Engineering and Computer Science

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Professor Ali M. Niknejad, Chair

Research in the mm-wave band using CMOS and SiGe technologies has gained momentum over the past few years. Millimeter-wave circuits are expected to enter consumer electronics in the near future. 60GHz circuits have the potential to be used in high definition wireless video transmission and high data-rate point-to-point communication. 77GHz has been explored for automotive radar and is expected to become more ubiquitous in coming years. 90GHz has been investigated for imaging and remote sensing applications.

Raw silicon transistor performance has improved dramatically in the past decade, which has spurred much of the research. The potential low cost of silicon ICs, especially CMOS, is great motivation to design mm-wave circuits for volume production.

This dissertation is divided into two parts. In the first part, the design of a 60GHz CMOS receiver is presented. Design methodologies for robust operation at 60GHz are introduced at device and circuit levels. Key building blocks of a 60GHz receiver are

investigated and several design techniques are proposed to increase the performance of the 60GHz circuits.

Second part explores the potential of mm-wave design for imaging applications. Performance requirements and challenges of a 90GHz power amplifier for imaging applications are explored. Circuit and system level design details of a pulsed power amplifier are provided and methodologies for enhancing the performance of those designs are introduced. In the end, A prototype of this power amplifier and its integrated version in an ultra wideband pulsed transmitter are presented.

This thesis is expected to provide a design framework for achieving predictable and desired performance at mm-wave band.

Professor Ali M. Niknejad
Dissertation Committee Chair

To My Parents, Farideh and Mohammad

Acknowledgements

I would like to thank many people who made my life at Berkeley a great and memorable one. First and foremost, I wish to express my deepest gratitude to my research advisor Professor Ali M. Niknejad. This work would not be possible without his continuous support and guidance during the years of my education at Berkeley. His deep knowledge in the field and his creative ideas helped me a lot during my PhD research. His pleasant personality made me always feel very lucky for having him as my research advisor. I would also like to thank my other thesis committee members, Professor Jan Rabaey and Professor Paul Wright who I benefited a lot form their interesting talks and lectures especially at Berkeley BWRC research retreats. I would also like to thank Professor Seth Sanders for being in my qualifying exam committee. I would like to thank Professor Haideh Khorramabadi for her continuous support during my PhD at Berkeley. I would like to thank Dr. Osama Shana'a for teaching advanced IC circuit class, EE290c. His deep knowledge and interesting teaching style made his class, one of the best classes I have ever taken at Berkeley.

Many thanks go to my colleagues, Babak Heydari and Mounir Bohsali who sincerely shared their knowledge and experience on 60GHz device modeling with me. My special thanks go to my research colleagues, Ehsan Adabi and Amin Arbabian from whom I received great support and with whom I had great research discussions and team work. It was really great to have them as my research colleagues at Berkeley. I would also like to thank other members of the 60GHz team and THz imaging (TUSI) team, especially Cristian Marcu, Maryam Tabesh, Jun-chau Chien, Shinwon Kang and Steven Callender with whom I had great team work and had interesting research discussions.

I would like to thank Berkeley Wireless Research Center (BWRC) and Electrical Engineering and Computer Science (EECS) administrative staff for their support during my PhD at Berkeley. Most importantly, I would like to thank my dear parents and my brothers, Babak and Arash for their support and encouragement. This work would not be done without them.

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Chapter 1

Introduction

1.1 Introduction to mm-Wave Designs: 60GHz

Research in SiGe and CMOS circuits in the mm-wave band, particularly the 60 GHz band, is an active topic [37]-[18]. Operation in the 60 GHz band has many potential advantages compared to other unlicensed frequency bands including the availability of large bandwidth (7 GHz) and high-transmission power levels. Standardization activity (IEEE 802.15.3c) is underway to enable many new applications of this technology including short-range high data rate communication, automotive radar (Fig. 1.1), point-to-point wireless links, and wireless HD video transmission (Fig. 1.2).

Raw silicon transistor performance has improved dramatically in the past decade, which has spurred much of the current research. The potential low costs of silicon ICs, especially CMOS, is a great motivation to design 60 GHz circuits for volume production. As transceivers with high levels of integration are realized in silicon [2], the cost of testing can be reduced significantly using Built-In Self-Test (BIST). Thus, 60 GHz radios can complement

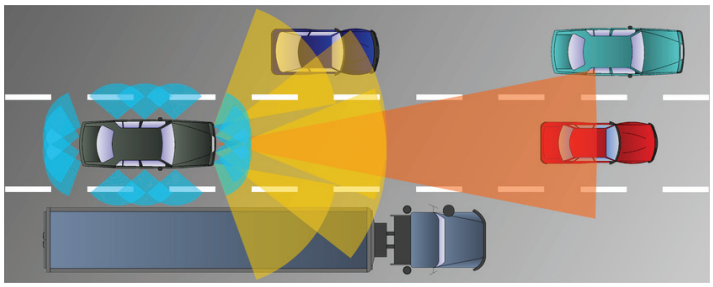


Figure 1.1: mm-wave application in car radar[80].

Figure 1.2: mm-wave application for wireless high definition video transmission [81].

existing WLAN radios by providing 10-100× bandwidth for short-range communication.

In order to enable high data rate communication in the 60 GHz band, particularly in battery operated mobile devices, it is necessary to reduce the power consumption of key building blocks in the receiver. In this chapter, we demonstrate a very lower power receiver core that can be realized in modern CMOS technology while maintaining sufficient noise figure and linearity for most envisioned applications.

This chapter is organized as follows: Section 2 highlights the features of the used technology including active and passive structures to implement the receiver core. Section 3 presents system-level calculations for a 60GHz communication system. Sections 4-6 review the detailed design of the receiver building blocks such as low noise amplifier, down conversion mixer and LO distribution network. Measurement results of the prototype receiver are presented in section 7.

Chapter 2

Analysis of Active and Passive Components for mm-Wave Design

2.1 CMOS Technology for 60GHz

The performance of active and passive components is largely determined by the substrate doping, the oxide and metal stacks, and the raw transistor f_t/f_{max}. It is important to note that the performance of transistors operating in circuits is largely affected by the interconnect at the transistor terminals, lowering the device f_t significantly from reported values for an intrinsic device.

In theory, the metal/oxide stack can be simulated to arrive at models of passive elements whereas in practice, we are hampered by practical and technical issues. First, the exact geometry of the stack is often unknown to the designer, and most foundries are reluctant to provide this information. Furthermore, the material parameters, such as the

permittivity and loss tangent of the layers, is also not known exactly, especially at mm-wave frequencies. The technical difficulty lies in the complexity of a modern IC process stack up, which consists of a sandwich of many dielectric layers (such as a low-K material to reduce interconnect parasitics), thick metal layers (not easy to simulate with most electromagnetic solvers), and passivation layers. Layout complexity arises due to process design rules created to maximize the yield and planarity of the process. For instance, wide metal lines must be slotted and extra 'dummy' layers litter the layouts. Most electromagnetic solvers have difficulty simulating such actual physical structures.

An alternative approach, which we have followed, is to use simplified cross sections of oxide/metal stack to simplify the simulations. In order to calibrate our setup, we fabricate and measure a test chip containing a library of active and passive devices. Based on the knowledge of measuring these test structures, we came up with models for active and passive devices for mm-wave design.

2.2 Previous Research

Research on active and passive device modeling for the mm-wave design in CMOS technology is mostly based on the work of previous members of the Berkeley Wireless Research Center (BWRC) 60GHz team. Sohrab Emami and Chinh Doan started the work on device modeling for 60GHz design and have done extensive work to characterize active and passive structures. They have done several test chips to develop libraries of active and passive devices for mm-wave design. Sohrab Emami also developed large signal 60GHz transistor model in CMOS for non-linear circuits such as mixers and power amplifiers. Babak

Heydari continued the effort on 60 GHz active device modeling by developing noise model for 60GHz and extended the work on small signal and large signal transistor modeling. Mounir Bohsali did extensive research on passive device modeling and substrate characterization to develop models for passive structures such as transmission lines. The author of this thesis applied these passive device modeling techniques to characterize lumped structures such as transformers for the 60GHz design. Here, we will review the work of the 60GHz team members at Berkeley Wireless Research Center (BWRC) on active and passive device modeling. The author of this thesis applied these techniques and methodologies to the design of a low power 60GHz receiver in 90nm CMOS technology.

2.2.1 Active Device Modeling for mm-Wave Design

The layout and optimization of active devices has been discussed previously [3] [5]. Unlike the transistors that are used for lower frequency applications, active devices do not have high gain at mm-wave frequencies like 60 GHz. This requires a 60 GHz designer to optimize the layout for maximum performance at the frequency of interest. The device maximum stable gain and maximum available gain could be shown to be: [31]

$$MSG = \frac{S_{21}}{S_{12}} \tag{2.1}$$

and

$$MAG = \frac{S_{21}}{S_{12}} \cdot (K - \sqrt{1 - K^2}) \tag{2.2}$$

in which K is the stability factor of the device

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{2.3}$$

and Δ is the auxiliary stability condition

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \tag{2.4}$$

If $K > 1$ and $\Delta < 1$ the device is unconditionally stable, otherwise the device is potentially unstable. Stability factor below one means that the device can oscillate if certain impedances are seen at load or source terminals. To summarize K factor and Δ into one parameter, μ factor is usually defined for amplifier design.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \tag{2.5}$$

If $\mu > 1$, the device or amplifier is unconditionally stable. The bigger the μ, the more stable the design. By looking into Eqn. 2.1, it could be seen that S_{21} is proportional to g_m of the device and S_{12} is proportional to C_{gd}. Therefore, in order to increase the performance of the device, we need to reduce the source resistance R_s to increase effective g_m. Reducing the parasitic capacitance C_{gd} will also increase the device performance. This is shown in the following equations:

$$MSG = \frac{S_{21}}{S_{12}} \propto \frac{G_m}{C_{gd}} \tag{2.6}$$

$$G_m = \frac{g_m}{1 + g_m \cdot R_s} \tag{2.7}$$

The conceptual layout of a common source and cascode devices are shown in Fig. 2.1 and Fig. 2.2. For the cascode and common source devices, source connection

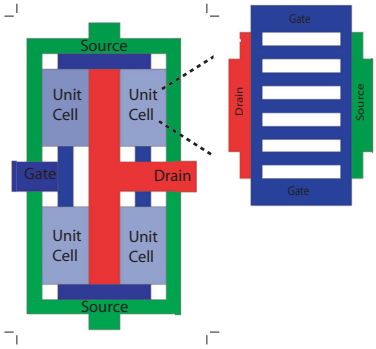


Figure 2.1: Simplified layout of common source transistor.

surrounds the device to reduce the source resistance and increase the g_m of the device. Gate and drain routings are separated and distant from each other to reduce the parasitic gate drain capacitance. Reducing this capacitance increases device stability and also increases its available gain. For the cascode transistor, shared junction architecture is used to reduce the capacitance at the junction node and to increase device gain. The increase in MAG due to shared junction architecture was more than 4dB in the used technology. In general, by multi-path and rounded structure for gate, drain and source connections, it is pursued to increase the performance of the active device for 60 GHz design.

As shown in [3], [5], the small signal and large signal model was produced based on the measurement data. De-embedding structures are used to characterize a transistor. In our calibration approach, we have used open-short de-embedding structures [28]. This method of de-embedding is usually good up to 40 GHz. For the 60GHz band, this method results in noisy and less accurate data. Therefore, a small signal model was generated based on de-embedded data up to 40GHz and the model was extrapolated to generate data for

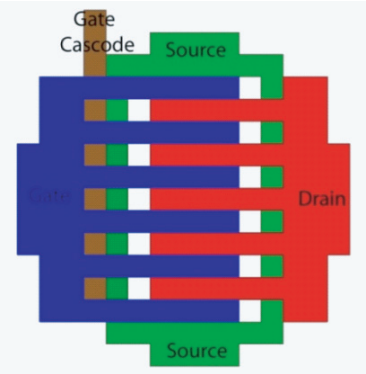


Figure 2.2: Simplified layout of cascode transistor.

the 60GHz band.

In order to generate a small signal model, not only parasitic capacitance and resistances are added to the junction nodes, which is mostly a low-frequency approach, but also parasitic inductances are added to the base and drain and source nodes to capture high-frequency behavior of the active device. Since available parasitic extraction tools do not capture these parasitic inductances for 60GHz, these parasitic inductances could be found either from a measurement-based approach or from accurate modeling using 3-D electro magnetic (EM) simulation software. Adding these elements plays an important role for a predictable design at 60 GHz band. However, an inductance should always be defined in a closed loop. This means the active device should be used in the final design with the exact layout and surrounding ground and return current loops as it was laid out in the test structure for modeling purposes. A simplified large signal model of a common source device is shown in Fig. 2.3.

The performance of the custom-designed common source and cascode devices are

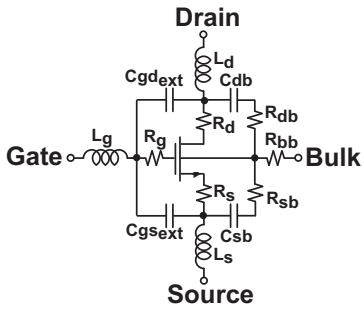


Figure 2.3: Simplified large signal model of the common source transistor with added parasitics.(Courtesy of Sohrab Emami)

shown in Fig. 7.6 and Fig. 2.5. It is interesting to note that cascode device provides substantially higher gain at low frequencies but experiences a drop in maximum available gain sooner, at around 40 GHz. This occurs due to the parasitic pole at the cascode junction of the transistor, even though the device uses a shared-junction layout. The cascode device becomes unconditionally stable after 40GHz as the stability factor goes above 1. While there is little difference in gain between the two devices at 60 GHz[1], the cascode device is unconditionally stable beyond 40 GHz (Fig. 2.5), which leads to more robust performance due to process variations. Due to higher isolation and smaller feedback loop (smaller S_{12}), input and output matching networks in an amplifier design are less affected by each other. This means that input and output matching networks can be designed more independently from each other.

2.2.2 Passive Devices for mm-Wave Design

Passive structures play an important role in mm-wave design and they occupy most of the area in a mm-wave chip. Unfortunately, passive device dimension does not

[1]The peaking in the gain of the device is explained in [6].

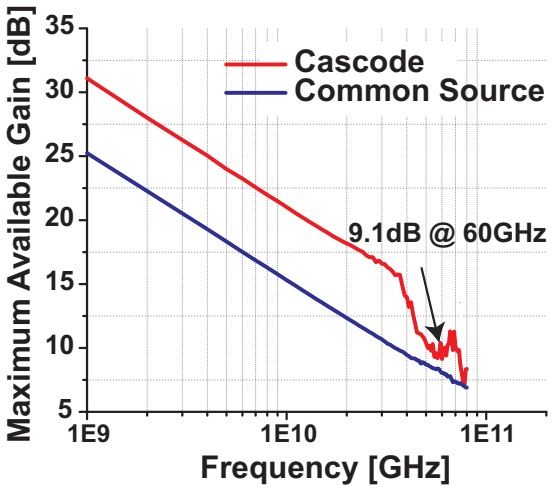


Figure 2.4: Measured NMOS common-source and cascode device performance: Maximum available gain.

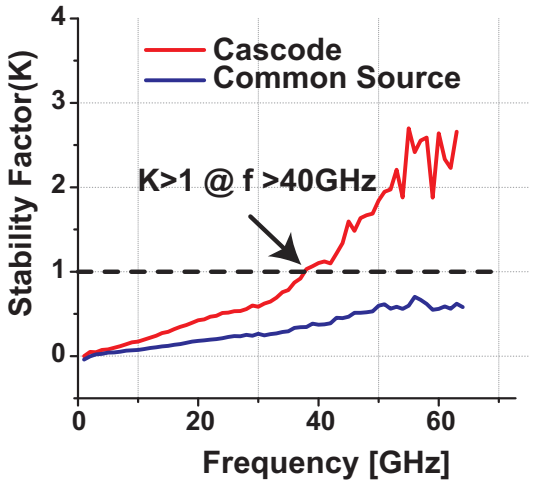


Figure 2.5: Measured NMOS common-source and cascode device performance: stability factor (K).

scale with technology scaling unless the frequency of operation is increased as well. On the other hand, passive performance usually worsens by technology scaling since metal stacks are getting closer to the substrate. In the absence of special process features like ultra thick top metal, passive device performance is usually degraded from one technology node to the next with smaller gate length.

Since the silicon substrate resistivity is relatively low ($\sim 10\Omega/cm$), the high-frequency signal leaks into the lossy substrate and increases the passive loss at mm-wave frequencies. Besides electric loss, magnetic loss is another factor in degrading the performance of passive devices and is mostly attributed to inducing eddy current into the substrate. Special layers like pwell blocker in the process mask can be used to decrease the doping of silicon substrate. This will help reduce the passive loss at mm-wave. Passive conductive loss is also due to finite conductivity factor and skin-depth effect. Skin depth is a frequency-dependant loss mechanism and causes the conductor loss to go up by increasing the frequency of operation

$$\delta_s = \frac{1}{\alpha} = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.8}$$

in which δ_s is the skin depth, μ is the magnetic permeability and σ is the metal conductivity. For copper with $\sigma = 5.8 \times 10^7$, we have $\delta_s = 0.25\mu m$ at 60 GHz.

In order to use passive structures for mm-wave design, they have to be characterized for desired frequency band. 3D electromagnetic simulation software like HFSS could be used to simulate passive structures. However to build a reliable stack profile in these EM software, a few passive structures need to be fabricated as test structures. Based on the

mm-wave measurement of these test structures, stack profile could be generated or adjusted to match the simulation results with measurement data.

Transmission Line Modeling Methodology

Transmission lines are usually used for mm-wave design since they provide well-defined return current loops. They are usually less sensitive to the modeling inaccuracy compared to their lumped counterparts. However, as a trade-off, they usually occupy more area as their dimensions are typically related to the wavelength. For example, at 60GHz, a quarter wavelength transmission line is about $600\mu m$. Due to their bigger size, they are also usually lossier compared to the lumped components. Challenges for a lumped design approach will be investigated in the next section.

For the mm-wave design, different types of transmission lines can be used. A transmission line could be realized in the form of microstrip or coplanar waveguide transmission line (CPW) or CPW line with underground connection. The choice of transmission line type usually depends on the process and design specifications. For example, if we are to realize certain line characteristic impedance (Z_0), one structure could be favorable to the other to realize a lower loss and achieve certain characteristic impedance. Another factor could be the amount of isolation requirement between lines. Usually, if we want more isolation between lines routed in the design, we go for the CPW line since it has ground lines on the sides of the signal line. This factor effectively shields adjacent signal lines from each other. On the other hand, the microstrip line is very easy to be routed and usually results in more compact layout compared to CPW.

A transmission line can be modeled with small signal R,L,G,C parameters. R and

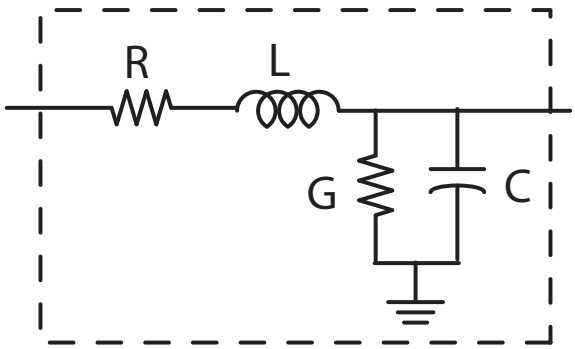


Figure 2.6: Small signal parameters of unit length transmission line.

L are series components and G and C are shunt parameters. R is mostly attributed to the conductor loss and G is mostly due to substrate loss. For technologies that have high-resistivity substrate like Silicon On Insulator (SOI), G is big and its associated substrate loss is negligible.

The small signal model of the transmission line for unit length is shown in Fig. 2.6. In order to model transmission line, several parameters like characteristic impedance (Z_0)) loss factor (α) and line quality factor (Q) could be used to match measurement versus simulations. Line characteristic impedance could be shown to be equal to: [31]

$$Z_0 = \sqrt{\frac{R + L\omega}{G + C\omega}} \tag{2.9}$$

If Loss factors, R and G are small then the Z_0 simplifies to:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.10}$$

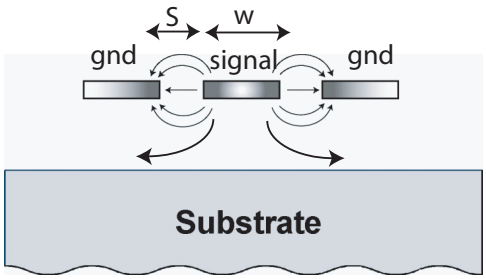


Figure 2.7: Conceptual view of a coplanar waveguide transmission line (CPW).

Also line loss factor α could be shown to be approximately equal to:

$$\alpha \cong \frac{1}{2}(\frac{R}{Z_0} + GZ_0) \tag{2.11}$$

Coplanar waveguide transmission line is shown in Fig. 2.7. The center metal is the signal line and the two side metal lines are ground paths. The current concentration in the line is shown by a darker color and is at the edges of the signal and ground lines. Current crowding comes from the fact that mm-wave signal prefers to flow on the minimum inductive path in the mm-wave band like 60GHz.

To change the Z_0 of the line, we can change the signal metal width (W) or metal spacing between signal and ground lines (S). By decreasing W or increasing S, line characteristic impedance goes up, however, decreasing W can increase conductive loss, and increasing W can increase substrate loss. By increasing S, more electric field will leak into the substrate instead of being confined between signal and ground lines. This will lead to increasing the substrate loss. Thus, there is obviously an optimum point for W and S parameters to realize certain line characteristics. From Eqn. 2.9 the increase in Z_0 could be explained by increasing L and reducing C in the above scenario.

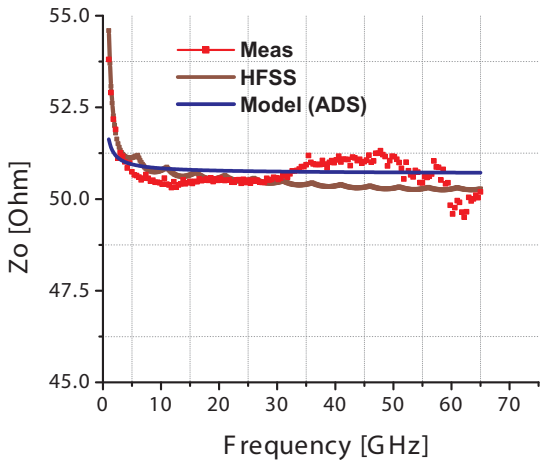


Figure 2.8: Measured, simulated, and modeled transmission line Z_0.

In order to build a length scalable model for the CPW line for the design phase, for example, a coplanar waveguide (CPW) line with a metal width W =10μm and a gap spacing of S =4μm has been fabricated, measured, simulated, and modeled. The simulation is performed with Ansoft HFSS, and a physical transmission line model in Agilent ADS is used to fit the measurements. Fig. 2.8 and 2.9 show a good match between measurement and simulations/model of the line characteristic impedance Z_0 and loss factor α. Several transmission lines with different gap spacing S were used to calibrate the process parameters.

Transformer Modeling Methodology

Transformers can be used for mm-wave design [42][43]. Transformers have a very well-defined return current loops, which means they have more predictable performance for 60GHz design. Unlike passive structures like inductors, most of the magnetic flux in the transformer is confined between the primary and secondary windings. Therefore, the

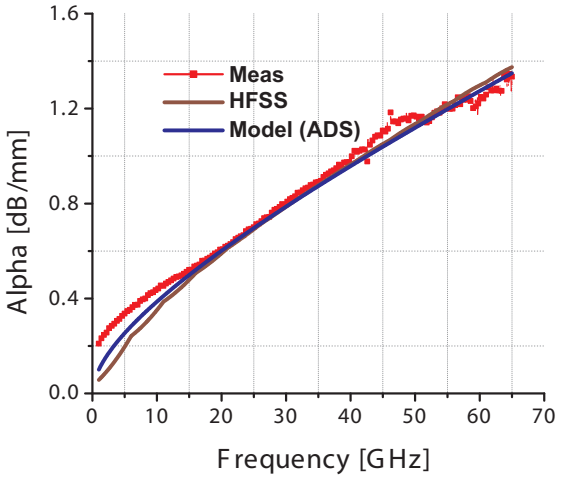


Figure 2.9: Measured, simulated, and modeled transmission line propagation loss α.

transformer is less affected by the surrounding grounds. In order to have a well-modeled transformer, it is preferable to simulate the structure with its surrounding ground. Fig. 2.10 shows an overlaid transformer structure with its surrounding ground inside the HFSS setup.

A transformer is usually characterized by its winding inductance (L_1,L_2), windings quality factor (Q_1,Q_2), transformer coupling factor (K) and its self-resonance (SRF). A transformer can be modeled in the form of two coupled inductors:

$$V_1 = j\omega L_1 I_1 + j\omega M I_2 \tag{2.12}$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2 \tag{2.13}$$

where M is the mutual inductance

$$M = k\sqrt{L_1 L_2} \tag{2.14}$$

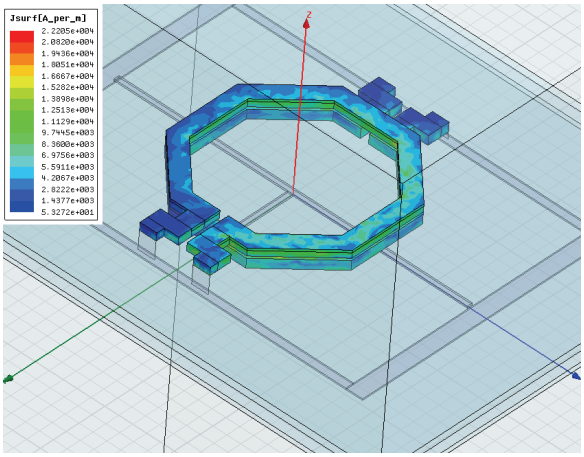


Figure 2.10: Overlaid transformer in HFSS setup.

So from Eqn. 2.12-2.14 we have:

$$V_1 = j\omega(L_1 - \frac{M^2}{L_2})I_1 + \frac{M}{L_2}V_2 = j\omega L_1(1-k^2)I_1 + k\sqrt{\frac{L_1}{L_2}}V_2 \tag{2.15}$$

Where the second term in above equation is used for transformer main functionality and the first term is undesired. Transformer turn ration is defined as:

$$N = k\sqrt{\frac{L_1}{L_2}} \tag{2.16}$$

If we assume that primary and secondary windings have resistance r_1 and r_2, then Egn. 2.12-2.18 could be written as:

$$V_1 = j\omega L_1 I_1 + r_1 I_1 + j\omega M I_2 \tag{2.17}$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2 + r_2 I_2 \tag{2.18}$$

so transformer parameters could be found as:

$$L_1 = \frac{imag(Z_{11})}{\omega} \tag{2.19}$$

$$L_2 = \frac{imag(Z_{22})}{\omega} \tag{2.20}$$

$$r_1 = real(Z_{11}) \tag{2.21}$$

$$r_2 = real(Z_{22}) \tag{2.22}$$

$$Q_1 = \frac{imag(Z_{11})}{real(Z_{11})} \tag{2.23}$$

$$Q_1 = \frac{imag(Z_{11})}{real(Z_{11})} \tag{2.24}$$

$$M = \frac{imag(Z_{12})}{\omega} \tag{2.25}$$

where Q_1 and Q_2 are primary and secondary winding quality factor.

Fig. 2.11 shows a simplified model for a transformer and includes winding parasitic resistance and capacitance to the substrate. Capacitor C_c is added to capture interwinding capacitance. These capacitors can be used to model transformer self-resonance. This simplified model is fairly accurate and can predict the transformer behavior over a wide frequency band of operation. More complete model for the transformer could be found in [44] [34].

To realize a transformer with maximum winding quality factor, a single turn transformer is preferable. Multi-turn transformers have lower quality factor and lower self-resonance. However if a certain impedance transformation ratio is required, multi-turn transformers may be used. Transformers could be realized in overlaid or lateral configura-

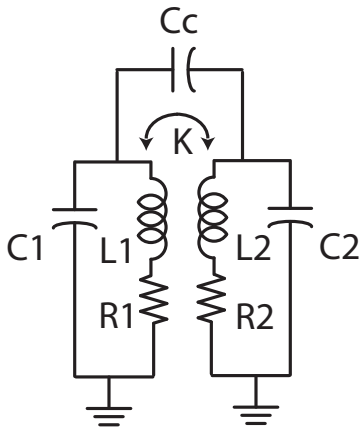


Figure 2.11: Simplified transformer model.

tions. Based on the metal stack profile and self-resonance concerns, impedance transformation requirement and area, one configuration may be superior to the other.

By increasing the winding width of a transformer, its conductive loss decreases and the winding quality factor increases to a point where capacitive coupling of the winding to the substrate increases the substrate loss and quality factor drops. The skin-depth effect should also be considered in finding the optimum metal width of the windings. The other important factor is transformer self-resonance, which goes down by increasing the winding width.

Fig. 2.12 and 2.13 show the quality factor of a single-turn overlaid transformer versus winding width and winding diameter.

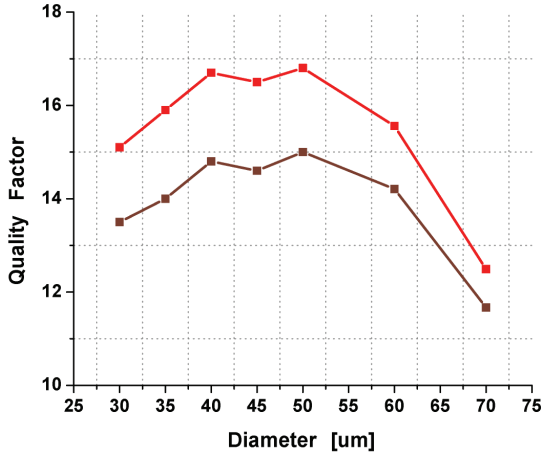


Figure 2.12: Quality factor versus internal diameter of the single-turn overlaid transformer with metal width=6μm.

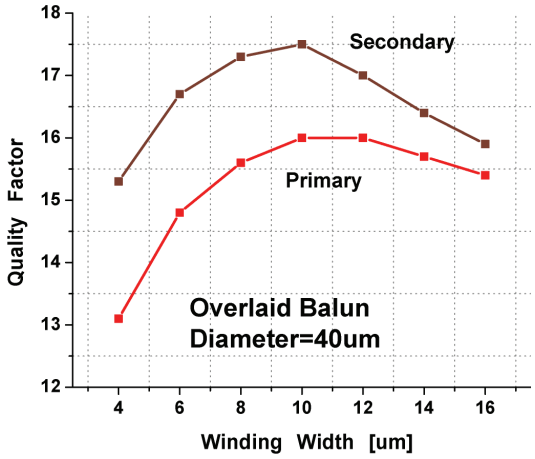


Figure 2.13: Quality factor versus metal width of single-turn overlaid transformer with internal diameter=40μm.

Chapter 3

60 GHz Receiver Design

3.1 60 GHz Link Budget

In order to establish a 60GHz wireless communication over a communication distance, we should first calculate the system link budget for the specific application. Here we calculate the link budget for 1Gb/s uncompressed 60 GHz wireless communication over 1m communication distance. One of the metrics that needs to be defined is the signal-to-noise (SNR)requirement. For different modulation schemes, we need different SNR level requirements. First, we will calculate the total noise power of the receiver at its input. Background noise at room temperature is given by:

$$background\ noise = KT = -174\ dBm \tag{3.1}$$

where K is the Boltzmann constant and T is room temperature

$$K = 1.38 \times 10^{-23} \frac{J}{K} \tag{3.2}$$

So the total receiver noise power at its input will be:

$$Noise\ Power = P_{noise} = KTBF \tag{3.3}$$

where B is the noise bandwidth and F is the receiver total noise figure. For 1Gb/s wireless communication with 10dB receiver noise figure, from Eqn. 3.3 we will have:

$$Noise\ Power = P_{noise} = KTBF = -174dbm + \ 90dB \ + \ 10 = -74dBm \tag{3.4}$$

To calculate signal power at the input of the receiver, we can use the friis transmission equation:

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} \tag{3.5}$$

where P_r is the received power, P_t is the transmit power, G_t is the transmit antenna gain, G_r is the receive antenna gain, λ is the wavelength and R is the distance between transmitter and receiver. Let's assume the transmitter can transmit a signal with power of $P_t = 10dBm$ at its P_{-1dB} and G_t and G_r are 2dB. P_r over $R = 1m$ communication distance from Eqn. 3.5 will be:

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} = -54dBm \tag{3.6}$$

If we consider 10dB margin for fading and shadowing loss over 60GHz channel we will have

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} - loss\ (fading/shadowing) = -64dBm \tag{3.7}$$

From Eqn. 3.4 and Eqn. 3.7 we have:

$$SNR = \frac{P_{sig}}{P_{noise}} = 10dB \tag{3.8}$$

this amount of SNR is enough for many simple modulation schemes like FSK.

However, to realize more complex modulation schemes with high bit rate such as 16QAM and 64QAM, we need more system SNR. To increase the system SNR, we can increase the transmitter power, but there is a limit on the amount of power that a power amplifier can generate in silicon technology, and usually this number is less than 20dBm. Phased array architecture is another viable alternative for SNR improvement. It could be shown that [32] by using antenna array for the transmit path we have:

$$SNR\ improvement = 20 \log N \tag{3.9}$$

where N is the number of antenna. Intuitively, SNR improvement comes from having N power amplifier multiplied by array gain of N. In other words, signals of all the transmitters (N) will be added in phase to generate the final transmitted power at a specific point in the space. The selection of the target point in the space is based on the amount of phase shift that is applied to each transmit path. For the receive path, the SNR improvement will be:

$$SNR\ improvement = 10 \log N \tag{3.10}$$

Intuitively, SNR improvement comes because for the signal path, applying the required phased shift in each received path makes the received signal paths signals in phase and so they are added in voltage, but noise from different receiver paths are added in power. If we assume we have array size N=16 for both receiver and transmitter, total SNR improvement be:

$$SNR_{added} = 10 \log N_{rx} + 20 \log N_{tx} = 12dB + 24dB = 36dB \tag{3.11}$$

Therefore, the overall system SNR for 16-element phased array transceiver for 1Gb/s communication over R=10m communication distance will be:

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} - loss\ (fading/shadowing) + SNR_{added} = 26dB \tag{3.12}$$

3.2 60 GHz Front-End Design

The choice of IF frequency is very important in mm-wave systems because this choice is closely tied to the LO frequency. While zero-IF or direct downconversion is popular at RF frequencies (Fig. 3.1), it requires the generation of an I/Q signal. Operation at twice the LO is costly because frequency dividers are very power hungry when operated at a significant fraction of the device f_t, and quadrature oscillators require double the power in the VCO. Accurate quadrature generation through on-chip hybrid couplers is a good option [4], and this can be used in the RF or LO path. Usually, the LO path is chosen to mitigate the losses in the signal path (and hence input-referred noise). In our work, we focused on the core of the I/Q downconversion receiver, shown in Fig. 3.2, which includes the LNA, mixer, and a multi-stage VGA. The bandwidth of the LO, RF, and IF ports are maximized to allow reception of wideband modulation signals.

In the next chapters, building blocks of a highly integrated 60 GHz front-end receiver in 90nm digital CMOS technology are presented. The front-end receiver has a wide gain tuning range of 60dB and an average noise figure of 6.2dB while consuming a record low power of 24mW from a 1V supply. An RF to IF conversion gain of 18dB is achieved while using an LO power of -2.5dBm. The design methodology is robust and features excellent agreement between measured and simulated performance. We first review and discuss the

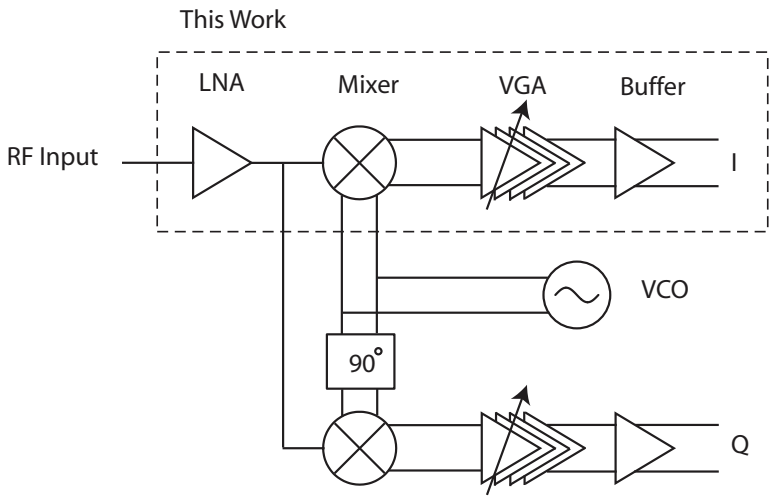


Figure 3.1: Block diagram of a direct-conversion receiver using I/Q paths.

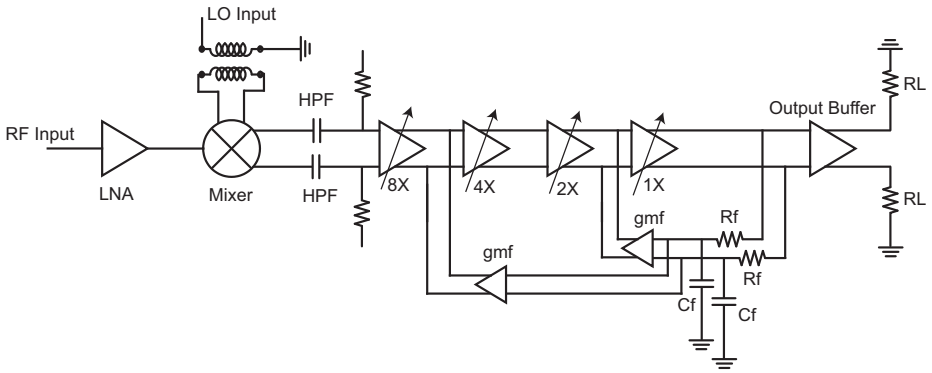


Figure 3.2: The core I or Q path implemented in this work.

design of low noise amplifier, down-conversion mixer and LO distribution network. Then measurement results of the 60GHz receiver design will be presented [14]. The LO for the 60GHz receiver was provided off-chip and was converted to differential signal by using on-chip transformer. The LO distribution network mentioned above was integrated in a 60GHz transceiver chip [35]. Interested readers are encouraged to review the Reference [36] for a detailed discussion on variable gain amplifier design.

Chapter 4

60GHz Low Noise Amplifier Design

4.1 Microwave Amplifier Design

Amplifiers are one of the most important building blocks in an mm-wave circuit. Since we have generated a two-port model for our active transistor test structures, most of the microwave amplifier design techniques could be used here. [31] [33]

In an amplifier design, we are usually concerned with metrics such as input and output matching networks, power gain, linearity, noise figure and stability. Consider an active transistor as a two-port block as shown in Fig. 4.1. The following metrics could be defined using its S-parameter.

A transistor power gain is a ratio of the power dissipated in the load Z_L to the power delivered to the input of the two-port network.

$$G_p = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-s_{22}\Gamma_L|^2} \tag{4.1}$$

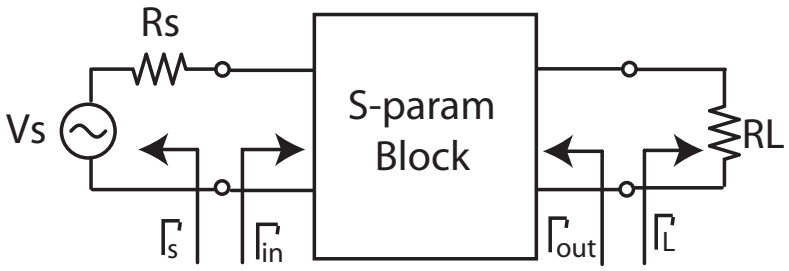


Figure 4.1: Two port S-parameter representation of active transistor.

where Γ_{in} is the input reflection coefficient and Γ_L is the load reflection coefficient.

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.2}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.3}$$

Z_0 is the reference port characteristic impedance and is usually 50Ω. The power available from the source is the maximum power that can be delivered to the network and happens when the input impedance of the terminated network is conjugately matched to the source impedance Γ_s.

$$P_{avs} = P_{in}|_{\Gamma_{in}=\Gamma_s^*} = \frac{|V_s|^2|1-\Gamma_s|^2}{8Z_0(1-|\Gamma_s|^2)} \tag{4.4}$$

Also the power available from the network, P_{avn} is the maximum power that can be delivered to the load.

$$P_{avn} = P_L|_{\Gamma_L=\Gamma_{out}^*} = \frac{|V_s|^2|S_{21}|^2|1-\Gamma_s|^2(1-|\Gamma_{out}|^2)}{8Z_0|1-S_{22}\Gamma_{out}^*|^2|1-\Gamma_s\Gamma_{in}|^2}|_{\Gamma_L=\Gamma_{out}^*} \tag{4.5}$$

$$P_{avn} = \frac{|V_s|^2|S_{21}|^2|1-\Gamma_s|^2}{8Z_0(1-|\Gamma_{out}|^2)|1-S_{11}\Gamma_s|^2} \tag{4.6}$$

Using Eqn. 4.4-4.6 we can define available power gain as:

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)}{(1-|\Gamma_{out}|^2)|1-s_{11}\Gamma_S|^2} \tag{4.7}$$

The amplifier transducer gain could be defined as:

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_s\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \tag{4.8}$$

let's assume that we use $Z_0 = 50\Omega$ and we have $Z_s = Z_L = Z_0 = 50\Omega$ or equivalently $\Gamma_s = \Gamma_L = 0$, then:

$$G_T = |S_{21}|^2 \tag{4.9}$$

Unilateral transducer gain is defined when S_{12}=0 and is equal to:

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|1-S_{11}\Gamma_s|^2|1-S_{22}\Gamma_L|^2} \tag{4.10}$$

If a circuit is unconditionally stable, the input and output ports could be conjugately matched. In that case we will have:

$$G_{T_{max}} = \frac{1}{1-|\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.11}$$

In the next chapter, we can use these metrics for the 60GHz amplifier design.

4.1.1 Cascode Transistor Design in the mm-Wave Band

As shown in the modeling section, the cascode transistor is unconditionally stable at 60GHz band. This means that the cascode amplifier can be designed for bi-conjugate match condition to get the maximum power gain out of each amplifier stage with its input and output matching network. Furthermore, since the cascode device offers more isolation

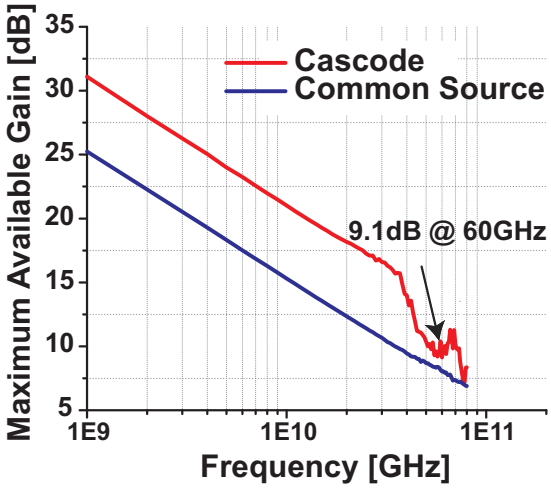


Figure 4.2: Maximum available gain of cascode and common source devices.

from output to input port (smaller S_{12}), designing a matching network for each amplifier stage will become much easier compared to the common source case. Due to high isolation, input and output matching networks become relatively independent of each other. As another reason for choosing the cascode transistor instead of a common source device in the design of 60GHz amplifier in this work, we can notice in Fig. 4.2 that cascode offers 1dB more MAG compared to common source transistor in 90nm CMOS process in our mm-wave optimized test structures.

Cascode transistor layout is optimized for the mm-wave design. Shared junction transistors are used to reduce the junction parasitic capacitance and increase the device MAG. If shared junction transistors are not used, a big portion of high-frequency 60GHz signal will be lost into the substrate through the parasitic capacitance at the junction of top and bottom transistors in the cascode configuration. This parasitic junction capacitance

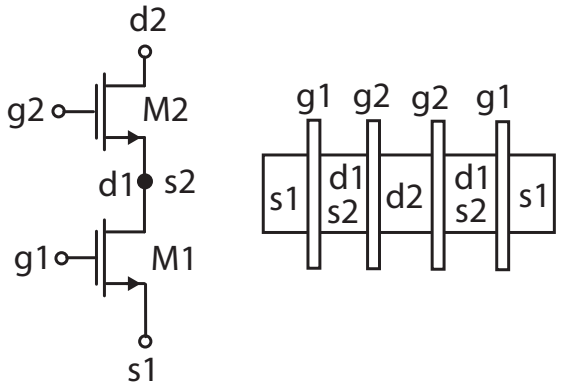


Figure 4.3: Layout of unit cell shared junction cascode transistor.

will substantially reduce the device maximum available gain (MAG). The configuration for the shared junction transistor is shown in Fig. 4.3

At the shared junction of source of transistor M_2 (s_2) and drain of transistor M_1 (d_1), contacts are removed to reduce the parasitic capacitance.

4.1.2 Stability Analysis of Cascode Amplifier Stage for 60GHz

Even though a cascode device provides more stability at high frequencies, certain considerations have to be taken into account in the layout of the cascode amplifier. It can be shown that the cascode gate terminal can exhibit negative resistance when the common source devices presents capacitive degeneration. In the cascode transistor shown in Fig. 4.4, if we replace the bottom transistor M_1 and replace it with a capacitor (which is a fare assumption for the 60GHz band), the real part of impedance that is seen through the gate of the cascode transistor M_2 will be:

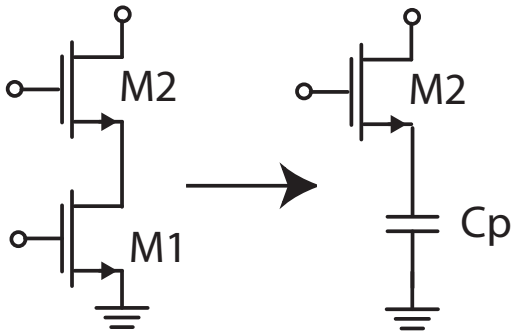
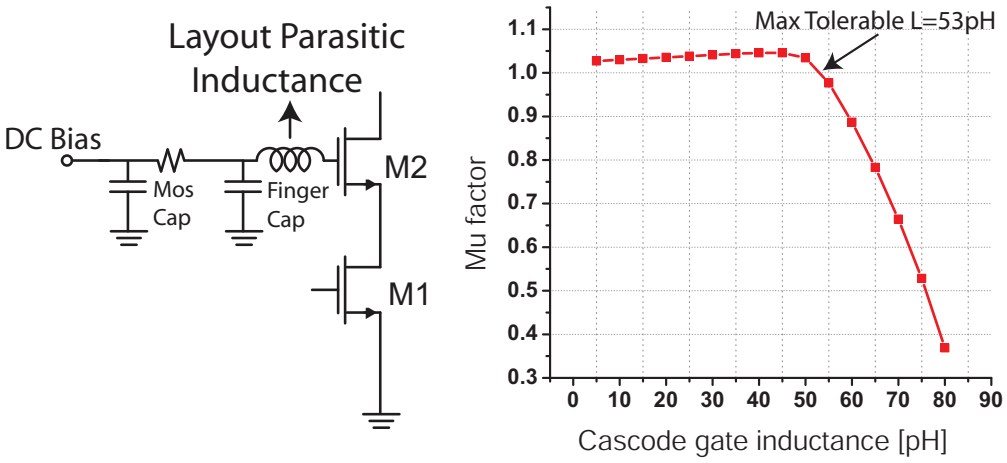


Figure 4.4: Simplified model of the cascode device for cascode gate stability analysis at the mm-wave band.

$$Real(Z_{in}) = \frac{-g_m}{C_p C_{gs} \omega^2} \tag{4.12}$$

Since the gate of the cascode device (M_2) is grounded as shown in Fig. 4.5 through bias capacitors, one must ensure that the inductance of this path is small so that the frequency of equivalent LC tank falls above the f_{max} of the device. As shown in Fig. 4.5b, only 53 pH is required for the device to become potentially unstable. Fig. 9.5 shows amplifier stability metric (μ)as a function of cascode gate parasitic inductance. The cascode bias circuit uses a C-R-C network to prevent low- and high-frequency instability. To minimize the inductance of the gate grounding network, a moderately sized bypass capacitor (900 fF) is placed close to the gate, and a second MOS-Capacitor device bypasses low frequencies. For low frequency stability, a series resistor is added between the capacitors to de-Q the network. This resistor should be big enough to de-Q the path and prevent the low frequency oscillation, but should still be small enough to provide a low impedance path to ground at low frequencies.



(a) (b)

Figure 4.5: (a) The parasitic inductance at the gate of the cascode and (b) the impact on the cascode device stability.

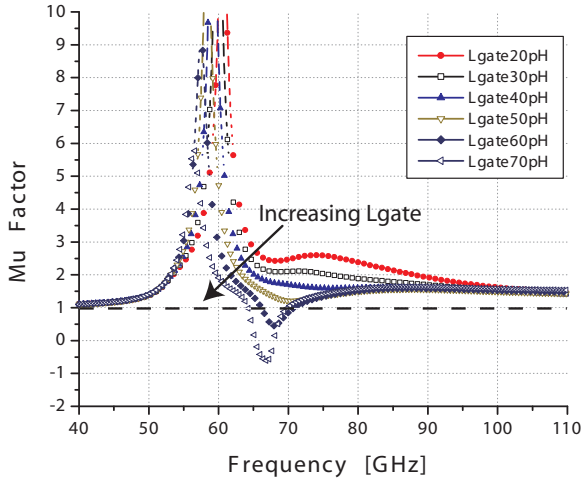


Figure 4.6: μ factor as a function of parasitic inductance at cascode gate node.

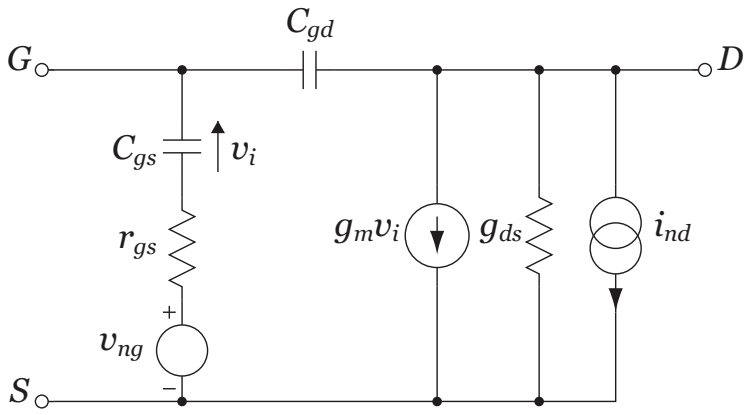


Figure 4.7: The Pospieszalski noise model assumes two uncorrelated noise sources, r_{gs} at T_g and r_{ds} at T_d.

4.2 Design for Low Noise

The pospieszalsky noise model is shown in Fig. 4.7. Pospieszalsky noise model assumes two uncorrelated noise sources. One is due to r_{gs} and the other to g_{ds} [7]. Each of these two resistors are assigned with a temperature T_g and T_d to represent MOSFET channel thermal noise. T_g is close to the ambient temperature and T_d is around several thousand degrees. Ignoring the effect of C_{gd}, the optimal noise source impedance of the device, (R_{opt} and X_{opt}) can be shown to be: [28].

$$R_{opt} = \sqrt{\left(\frac{f_t}{f}\right)^2 \frac{r_{ds} T_g (R_g + r_{gs})}{T_d} + (r_{gs} + R_g)^2} \tag{4.13}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} \tag{4.14}$$

where f is the operating frequency and f_t is the frequency at unity current gain of the device. Since f is much smaller than f_t at low frequencies, the second term in the R_{opt}

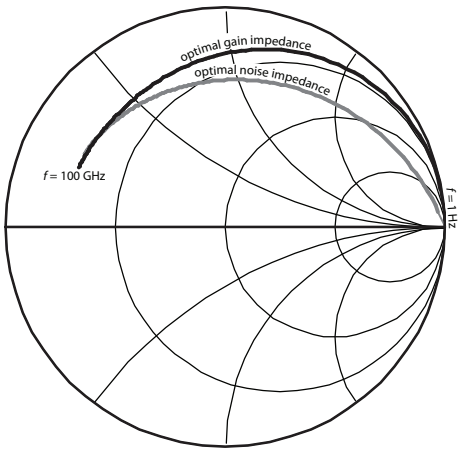


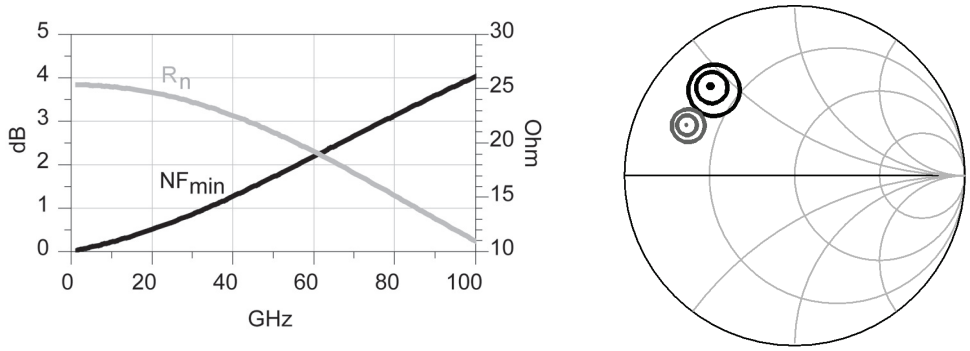
Figure 4.8: Optimal noise and power gain impedances for a 40 μm device for f= 1 GHz to 100 GHz.

equation is negligible so the equation for R_{opt} will be:

$$R_{opt}^{low\,f} = \frac{f_t}{f}\sqrt{\frac{(R_g + r_{gs})r_{ds}T_g}{T_d}} \tag{4.15}$$

As it could be seen from the Eqn. 4.15, the optimal resistance value is much larger than $R_g + r_{gs}$, since $R_g + r_{gs}$ is the optimal power gain resistance. This means that without simultaneous noise and gain optimization techniques, there will be a big penalty in achievable power gain or noise figure in the design. A typical technique at RF frequencies to meet simultaneous noise/power match requirement is inductive source degeneration.[11]

However, by increasing the frequency of operation f and getting it closer to f_t of the device, this approximation will not be valid anymore and the two terms become comparable. [28]. Furthermore, it could be shown that at high frequencies, the imaginary part of optimal noise and gain sources are also equal. These two factors together make the



(a) (b)

Figure 4.9: (a) Simulated NF_{min} and R_n for a 40μ common-source round-table device (b) noise and gain circles for optimal, optimal-0.25dB and optimal-0.5dB at 60 GHz. (Courtesy of Babak Heydari) [28]

optimal impedance for noise match and optimal impedance for power match to be close to each other Fig. 4.8. Since at mm-wave frequencies the device power gain is small and we can not afford to sacrifice on power match, the above analysis indicates that it is possible to design for power match with negligible penalty on noise figure. For cascode devices, the R_n moderately increases with the frequency in the mm-wave region. This scenario is verified both in simulation and measurements. Fig. 4.10 shows the simulated R_n and F_{min} for a cascode device.

4.2.1 Design Example of a 60GHz Low Noise Amplifier

The LNA is obviously one of the most important blocks in a front-end receiver as it directly sets the noise factor of the entire system. To realize high gain, a two-stage LNA is chosen using two cascode gain stages. LNA schematic is shown in Fig. 4.11. Each stage uses 40μm/0.1μm NMOS transistors biased at 7 mA. The device size and bias point were chosen so that the optimum noise/power match occur together. CPW lines with

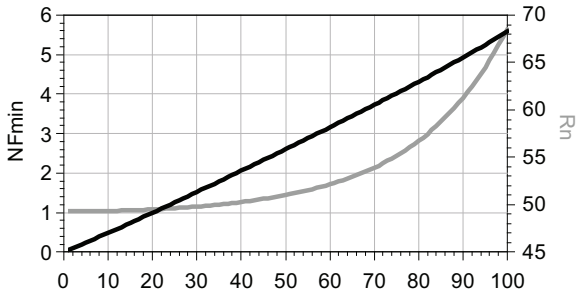


Figure 4.10: NF_{min} and R_n for a 40 μm cascode device.(Courtesy of Babak Heydari)[28]

$Z_0 = 50.8\Omega$ were used throughout the design. Using CPW lines, low Q multi-stage matching networks were used between cascode gain stages and also between the LNA and mixer blocks to provide higher signal bandwidth. This provides more robustness at face of process variation or modeling inaccuracies. The output of LNA was matched to 50Ω for standalone characterization of the LNA, even though this condition is not necessary at the interface of internal blocks.

Considering the analysis for low noise design at 60GHz, simulated noise figure of the two-stage cascode amplifier is shown in Fig. 4.12.

Simulation Results of Two-Stage Cascode Amplifier

The two-stage cascode LNA consumes 15.2mA of current from a 1V supply. The simulation data is noisy since measured transistor data is used for LNA simulation. Fig. 4.13 shows LNA S-parameters as well as amplifier stability factor.

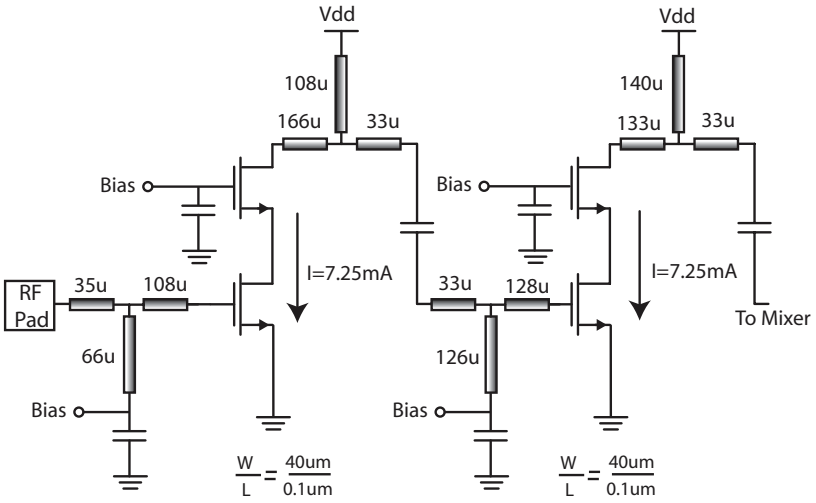


Figure 4.11: Schematic of the two-stage cascode LNA.

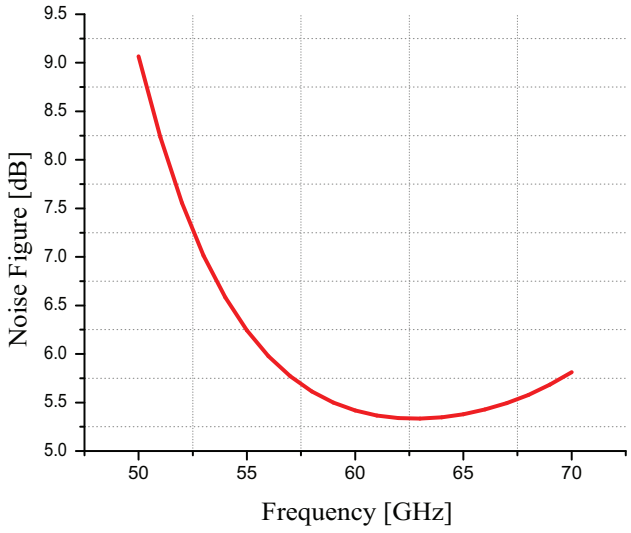


Figure 4.12: Simulated noise figure of the LNA.

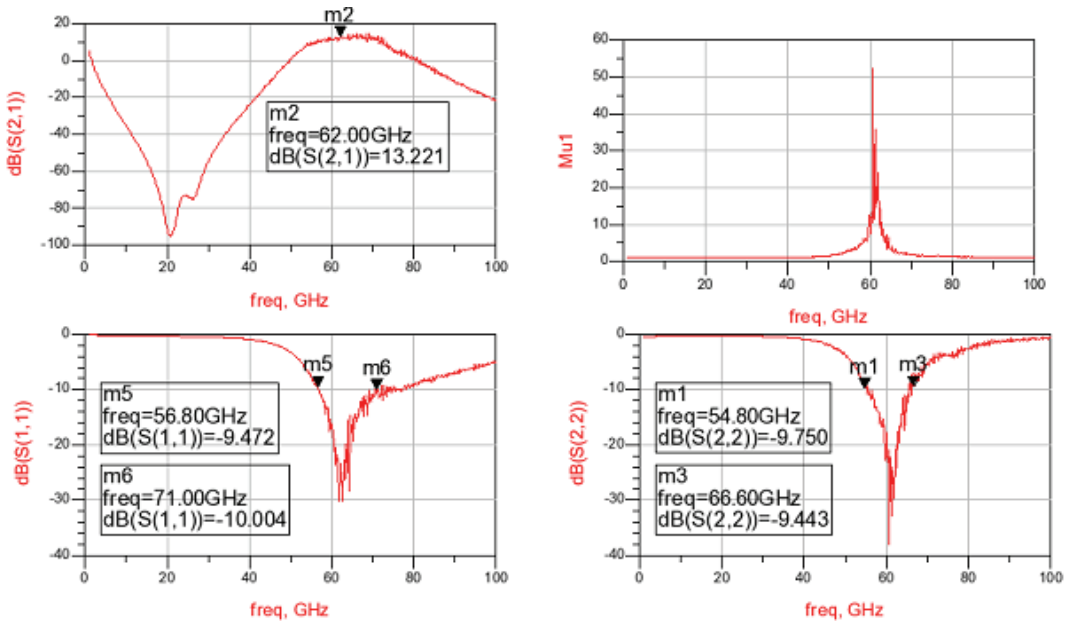


Figure 4.13: Simulated performance of the two-stage cascode low noise amplifier.

Chapter 5

60 GHz Down-Converting Mixer

5.1 Introduction to mm-Wave Mixer

Mixers are used to transfer a communication signal from one frequency band to another. Mixers are periodically time-varying circuits since the operating point of the switching stage changes through frequency conversion. They can be used on the transmitter side to modulate and translate the baseband signal to RF or up-convert the signal from a lower frequency band to a higher one. On the receive side, they can be used to down-convert the RF signal to based-band or lower frequencies.

5.2 CMOS Mixer Topologies

Mixers are divided into active and passive categories based on their ability to provide gain. Active mixers provide gain and passive mixers always present loss to the input RF signal. Having an active mixer is favorable in the sense that it provides some gain

in system-level design and relaxes the noise requirement slightly for the following blocks in the system. On the other hand, passive mixers usually provide higher linearity performance. Here, we briefly review different mixer topologies used for mm-wave design.

5.2.1 Current Commutating Active Mixer

The most common active mixers are current commutating mixers (Fig. 5.4). They can be single balanced [14] or double balanced [76]. Single-balanced mixers remove the RF feed-through to the output but present LO leakage to the output due to the dc term of the gm stage. Doubly balanced mixers prevent RF and LO leakage to the output, but require higher power consumption compared to single-balanced mixers. Modeling is also a concern for a differential RF gm-stage especially for high-frequency application like 60GHz since transistors are often characterized as two port devices, rather than three-terminal devices.

5.2.2 Single Transistor Active Mixer

The single transistor active mixer is the simplest active mixer Fig. 5.1. In this configuration, LO and RF are fed to the gate of the transistor. 60 GHz mixer was reported with this architecture in [77]. The combination of LO and RF was done by using a 90 branch-line hybrid made by coplanar waveguide T-lines.

5.2.3 Dual Gate Mixer

In a dual gate mixer Fig. 5.2, LO signal drives the upper transistor and RF signal is fed to the lower transistor. The LO signal modulates the trans-conductance of the lower transistor and converts the high frequency RF signal to the output IF signal [78]. The

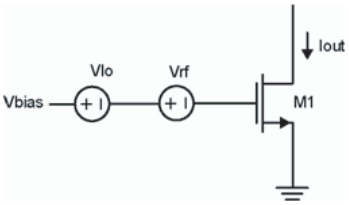


Figure 5.1: Single transistor active mixer.

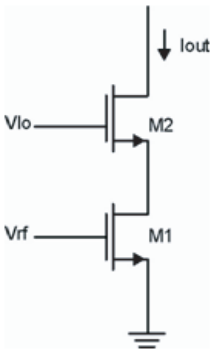


Figure 5.2: Double gate mixer.

source of the upper transistor and drain of lower transistor could be shared to minimize the parasitic capacitance to ground. This is very important in a high-frequency design like 60GHz as the conversion gain of the mixer is very sensitive to this parasitic capacitance.

5.2.4 Passive Mixer

The most commonly used passive mixer is shown in Fig. 5.3. Transistors are in the triode region while conducting and they act like switches. Passive mixers could be realized in doubly balanced, single balanced or unbalanced architectures. High-linearity performance is the most favorable advantage of the passive mixer while the conversion loss

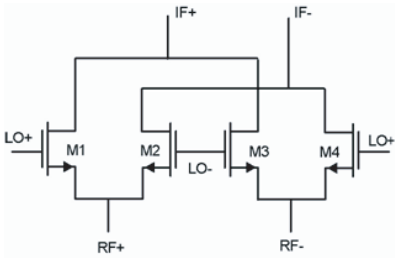


Figure 5.3: Passive mixer.

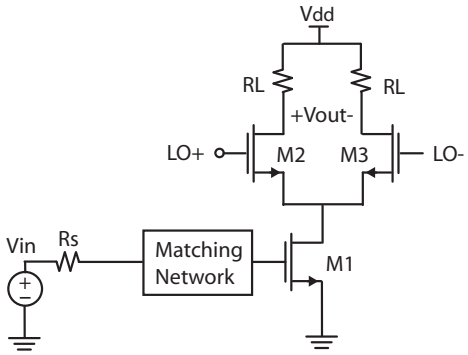


Figure 5.4: Single balanced active mixer.

could be its disadvantage [79]. Passive mixers usually need higher LO power compared to their active counterparts. Passive mixers are usually followed by amplifying the stage to compensate the loss.

5.3 Implementation of 60GHz Down-Converting Mixer

Fig. 5.4 shows a single-balanced active mixer that can be used in a direct conversion receiver. The input matching network at the input of the g_m stage is used to match the

mixer to the required input impedance. R_L is the load resistance at the mixer output. If we assume that the LO signal at the switching stage is large enough to provide perfect switching operation (ideal square wave), the mixer low-frequency conversion gain could be derived as shown below:

$$v_{out}(t) \simeq I_{RF}(t) \times s(t) \times R_L \tag{5.1}$$

$$s(t) \simeq \frac{4}{\pi}(\cos(\omega_{LO}(t)) + \frac{1}{3}\cos(3\omega_{LO}(t)) + \frac{1}{5}\cos(5\omega_{LO}(t)) + ...) \tag{5.2}$$

$$I_{RF}(t) \simeq g_m \times Q \times v_{in}\cos(\omega_{RF}(t)) \tag{5.3}$$

$$v_{out}(t) \simeq \frac{2}{\pi}(g_m Q R_L)(\cos((\omega_{RF}-\omega_{LO})(t))+\cos((\omega_{RF}+\omega_{LO})(t))+\cos((\omega_{RF}-3\omega_{LO})(t))+....) \tag{5.4}$$

Since we will have a lowpass RC filter at the mixer output, the final output signal after filtering will be:

$$v_{out}(t) \simeq \frac{2}{\pi}(g_m Q R_L)(\cos((\omega_{RF} - \omega_{LO})(t))) \tag{5.5}$$

So the mixer conversion will be:

$$CG \simeq \frac{2}{\pi}(g_m Q R_L) \tag{5.6}$$

where Q is the input matching quality factor.

$$Q \simeq \frac{1}{2R_s C_{gs}} \tag{5.7}$$

But for mm-wave design, none of the above assumptions are quite valid due to the non-ideal switching stage, loss in the matching network, modeling challenges of the transistors, significance of parasitic capacitance at the junction nodes, etc. These factors in unison make active mixer architectures not common for mm-wave designs [19].

Typically, a standard Gilbert cell at 60GHz does not provide substantial gain. Since the capacitance at the drain of the input transconductor stage is greater than $2C_{gs}$, and the conductance is g_m (assuming the switching devices and transconductor have equal area), the parasitic pole is $< f_t/2$, which limits the gain considerably. Moreover, accurate modeling of a Gilbert cell is more challenging since transistors are often characterized as two-port devices with the source grounded.

A Gilbert-cell type active single-balanced mixer that was used in this work to down-convert the high frequency 60 GHz signal to an IF from DC-2 GH is shown in Fig. 5.5. To increase the conversion gain of the mixer, the parasitic capacitance at the junction node between g_m-stage and switching stage should be tuned out using a small inductor or transmission line (similar to the way this was done for a cascode transistor in [11]). Alternatively, this capacitor can be split using a series inductor or transmission as shown in Fig. 5.6. The *C*-*L*-*C* network forms an artificial transmission line, and the cutoff frequency is determined by the LC product. The shunt line added to the junction node is a narrowband solution and also requires an AC coupling capacitor. In our design, the required length of transmission line was relatively short which makes the modeling of the junction node very sensitive to the parasitics of the coupling capacitor and the return current path through ground. The series transmission line, on the other hand, is longer and easier to model. The

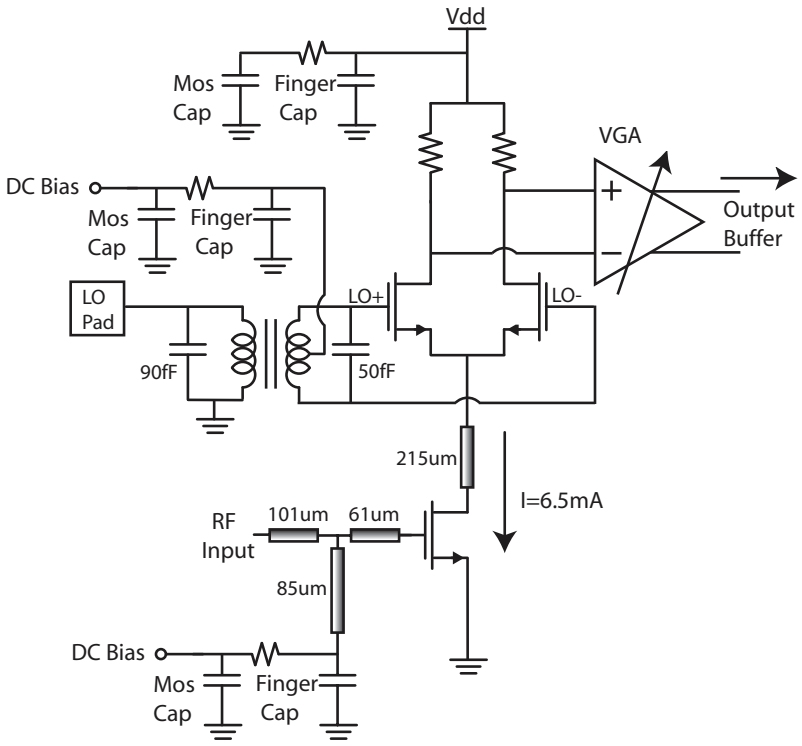


Figure 5.5: Circuit-level schematic of the mixer.

simulated conversion gain of the mixer versus the length of the tuning transmission line for the series and shunt versions are compared in Fig. 5.7. It should be noted that the actual length of the line is very well defined in a modern IC process, but the electrical length can vary due to layout (junctions of transmission lines) or difficult-to-model ground return paths.

5.3.1 LO Port Transformer

The LO signal is provided by using an on-chip balun that converts the single-ended LO port to differential signal. The balun is tuned to the 60 GHz band to minimize

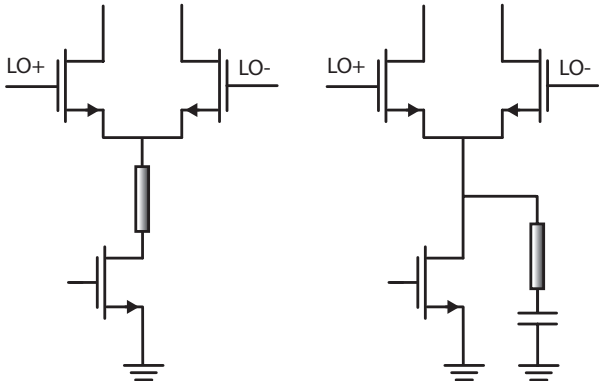


Figure 5.6: Mixer tuning options.

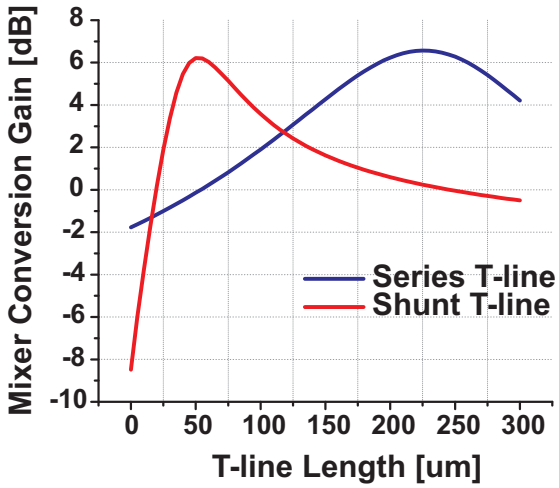


Figure 5.7: Simulated mixer conversion gain for series and shunt tuning options.

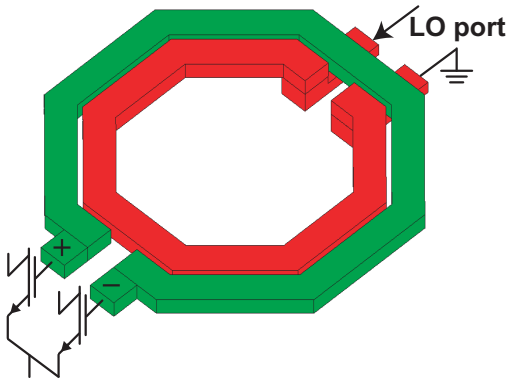


Figure 5.8: LO port balun structure.

the insertion loss of the balun. The center tap node of the balun provides a convenient biasing node for the switching stage. In addition to providing single-ended to differential conversion, tuned transformers can be used for impedance matching and biasing. The balun is inherently a two-port device and thus it is easy to employ in mm-wave circuits. This is not true of inductors and capacitors, which require careful modeling of ground currents in single-ended circuits. Furthermore, the magnetic field of a transformer is more confined as the primary and secondary currents are out of phase. This results in more compact layouts and lower losses, as transformers can be placed in closer proximity and magnetically induced currents in the substrate are lower due to the decrease in field strength.

The balun structure used in this design is shown in Fig. 5.8. A single turn baluns has a higher quality factor compared to multi-turn designs. The metal width of each winding was optimized to provide the highest-quality factor at the desired frequency band. By increasing the metal width, the winding quality factor increases to a point after which

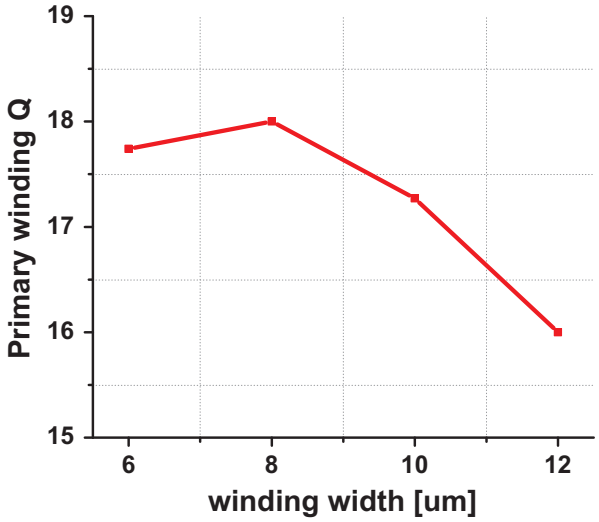


Figure 5.9: Balun quality factor(Q) versus metal width(W).

the substrate loss becomes the dominant factor and the quality factor drops (Fig. 5.9). In designing a balun for the switching stage, two factors are taken into consideration. First we maximized the LO voltage swing on secondary winding where the switching transistors are connected. Second we need to provide an impedance match on the primary winding to 50Ω as the LO signal was provided from the off-chip signal generator. This can be done by sizing the inductor windings appropriately and choosing optimal tuning capacitors to realize the minimum insertion loss.

5.3.2 LO Distribution Network

In the previous section, LO signal is provided off-chip from an external signal generator. However, it is usually required to distribute the LO signal from on-chip VCO. In this section, a sample of such LO distribution network in presented. The presented LO

distribution network was used to integrate the previously presented low noise amplifier and down-conversion mixer into a bigger 60GHz system.

LO Distribution Network Requirements and Implementation

LO distribution network is needed to distribute the VCO signal on chip. Usually, the LO distribution network for mm-wave is power hungry. Unlike lower frequency signal routing and LO distribution, any kind of signal division and signal routing at frequencies comparable to the device f_t has to be fully simulated and modeled. For example, diving a signal path into two paths cannot be simply done by routing two separate lines from the junction points (current domain division); instead, a Wilkinson power divider has to be used (power domain division). These blocks such as power dividers and interconnects are relatively lossy at these high frequencies [1]. This brings the need for additional active gain stages on the path to compensate for the loss. These active stages are realized in the form of amplifier stages. Design of the amplifier stage that can be used on the LO distribution path is discussed in the previous chapters. Here, the main goal of these amplifier stages are to compensate the loss on the path of the local oscillator signal due to power dividers and interconnects and to provide adequate signal power to the LO port of the transmit and receive path mixers. Adequate LO power at the mixer LO port is crucial for optimum performance of the mixer and acceptable conversion gain.

We have used transmission line based single-stage cascode amplifiers for the LO distribution network. Each amplifier has nominal power gain of more than 7dB over the 60GHz band and consumes 7.6mA of current from a 1.2V power supply. We used a 50Ω input match,

[1] The loss of a Wilkinson power divider was about 2dB at 60GHz in 90nm CMOS process.

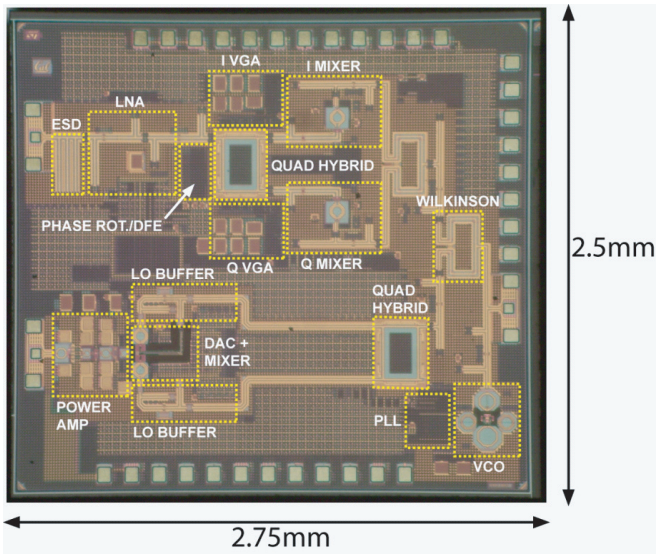


Figure 5.10: Die photo of the 60GHz transceiver chip [35].

50Ω output match design to make integration of these amplifier stages easy on the LO path. The transmission line based design also makes routing easy since the layout can be easily adjusted or modified to bring LO signal to different points on the chip where the mixers are present. The LO distribution network that was used in BWRC 60GHz transceiver (Fig. 5.10) is shown in Fig. 5.11. The LO distribution network is also shown in the block level schematic if the BWRC 60GHz transceiver chip Fig. 5.12 [35].

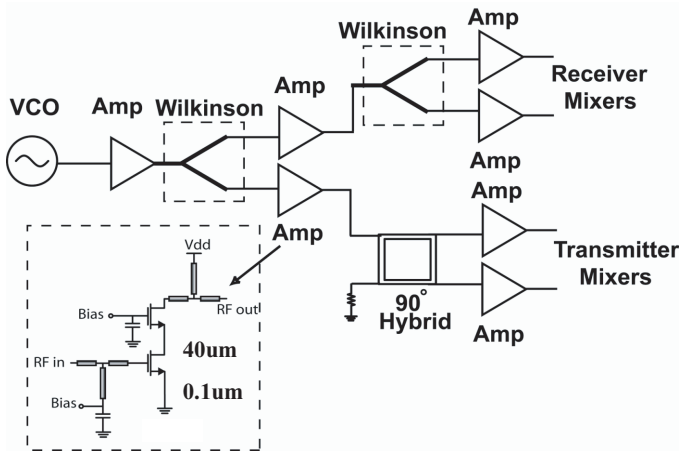


Figure 5.11: Block level schematic of LO distribution network for the 60GHz transceiver chip.

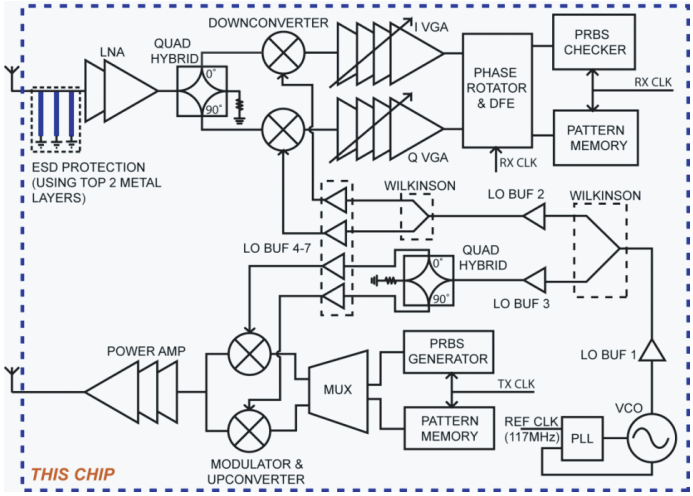


Figure 5.12: Block level schematic of the 60GHz transceiver chip [35].

Chapter 6

Variable Gain Amplifier

6.1 VGA Design for the 60GHz Receiver

Gain tuning range in the 60GHz receiver was provided by using a variable gain amplifier shown in Fig. 6.1. In a communication system, based on the strength of the received signal, the receiver should operate at a specific gain setting. If the receiver is receiving a weak signal, then usually the receiver is operating at its maximum power gain and its lowest noise figure. If the receiver is receiving a strong signal or there are strong blockers in band, then the receiver can reduce its gain by means of a variable gain amplifier. This gain reduction prevents the receiver from saturation by the strong received signal. At this mode, the receiver usually should satisfy a high-linearity specification [20]-[23].

The baseband VGA that was used in the 60GHz front-end receiver amplifies the signal through several stages of modified Cherry Hooper amplifier cells. Cherry Hooper cells provide a high bandwidth of operation. The VGA gain range can be adjusted through a single control voltage monotonically up to 60 dB. Several bandwidth enhancement techniques

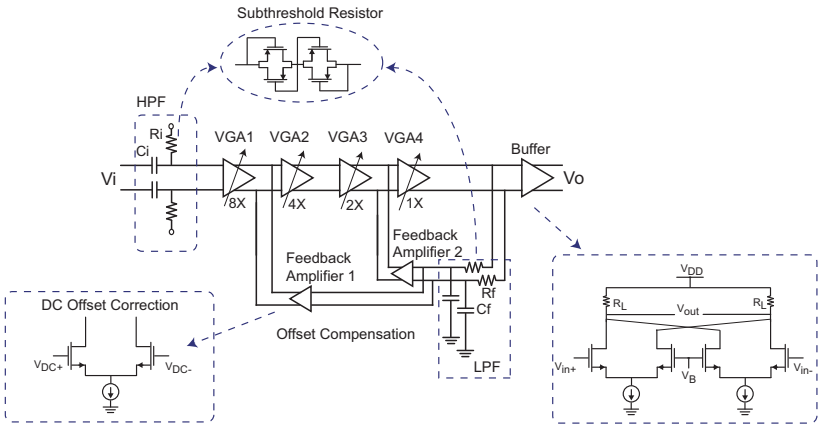


Figure 6.1: Block level schematic of the variable gain amplifier (VGA).

were used in the VGA to maintain more than 2.2GHz bandwidth at low power consumption. Inversely scaled transistors from input to output were used to increase the bandwidth of the overall amplifier. This approach reduces the power consumption considerably without degrading the noise figure. A novel dual feedback amplifier was used in the design of the VGA, which provides DC offset cancelation and bandwidth enhancement for the receiver. A high-pass filter at the input of the receiver cancels the dc offset coming from the previous stages. High resistor values (MΩ range) for the high-pass filter are realized by cascading PMOS transistor in the triode region. An RC low-pass filter at the output of the VGA will extract the dc offset component of the VGA output signal and feed it back to the input of the VGA by means of two negative feedback amplifiers. The VGA drives an output buffer for measurement purposes only. The VGA and output buffer consume 3mW and 8.5mW from a 1V power supply.

The detail of this VGA is discussed in [36] and interested readers are encouraged to review this reference.

Chapter 7

Measurement Results

7.1 Measurement Results of the 60GHz Receiver Core

The block-level schematic of the 60GHz front-end receiver is shown in Fig. 7.1 and its die photo is shown in Fig. 7.2. The chip was fabricated in a digital 90nm CMOS process (f_T =100GHz) and tested using on-chip GSG probes. The die area is $1.6mm^2$ including RF and DC pads. The RF signal is fed from the left to the input LNA and then feeds the down-converting mixer. The LO signal is provided off-chip through a GSG probe. The down-converted IF signal goes through several stages of variable gain amplifier. The IF signal is eventually fed to an output buffer for measurement purposes. The measurement of the IF signal is done differentially using the GSSG probe. Metal exclude layers are used on the critical 60GHz path to avoid the performance degradation by density dummy filling.

The entire receiver consumes a low power of 24 mW from a 1 V supply. The RF/DC pads are part of the design and are not de-embedded. The power breakdown is 14 mW for the LNA, 6.5 mW for the mixer, and 3.5 mW for the VGA. The LO power used

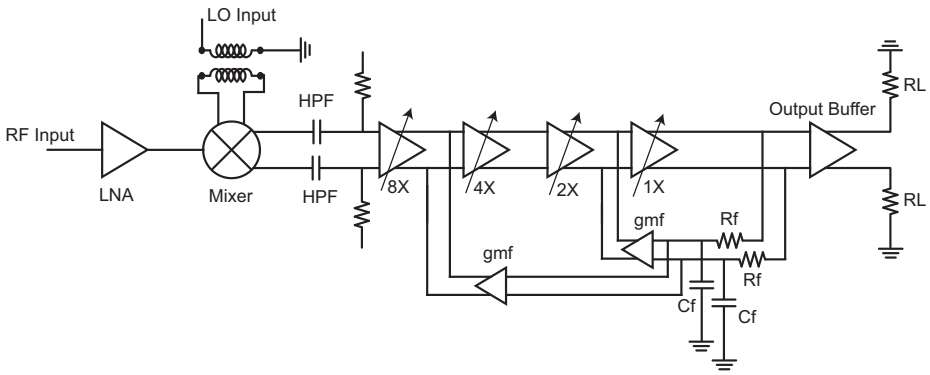


Figure 7.1: The core I or Q path implemented in this work.

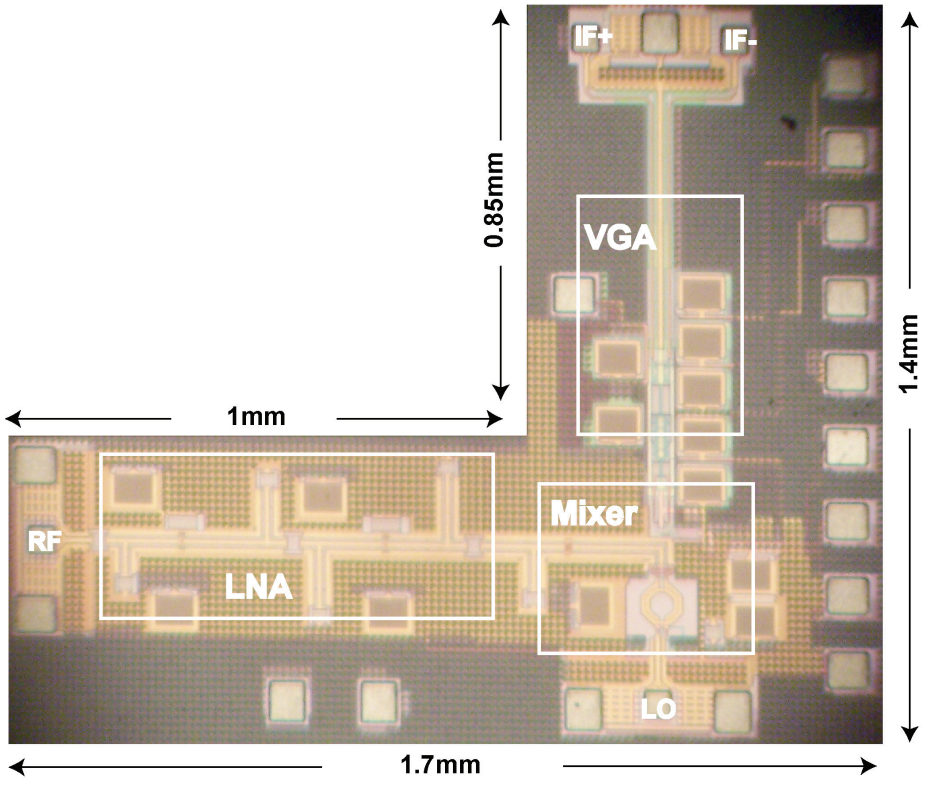


Figure 7.2: Die photograph of the front-end receiver.

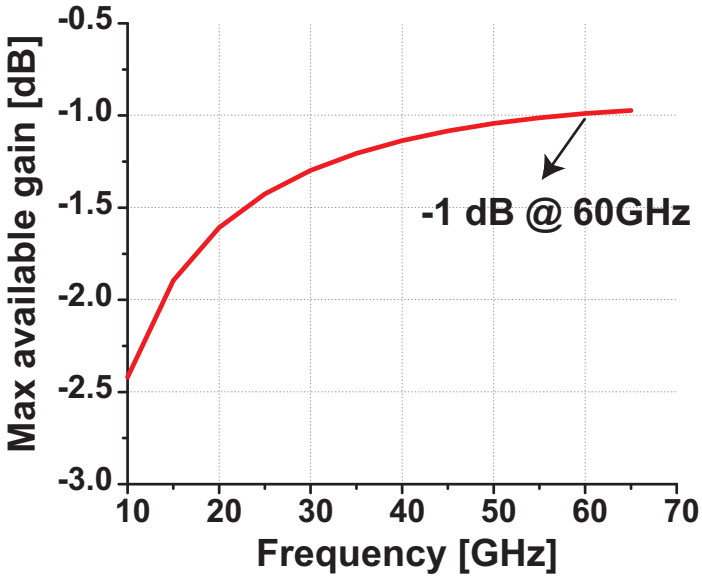


Figure 7.3: Measured balun maximum available gain.

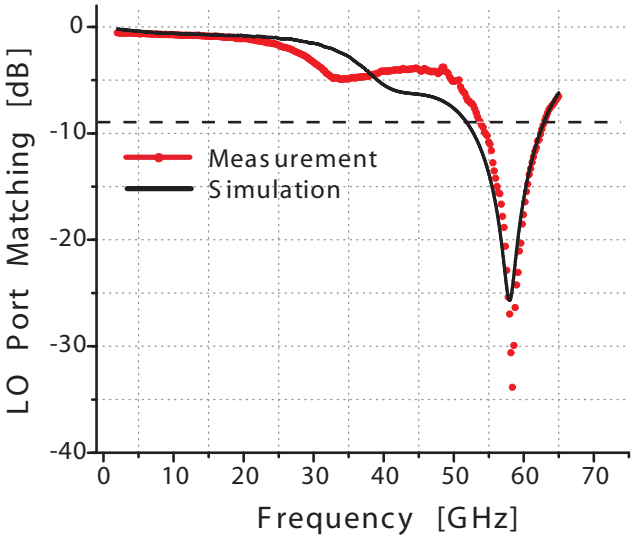


Figure 7.4: Measured return loss at the LO port.

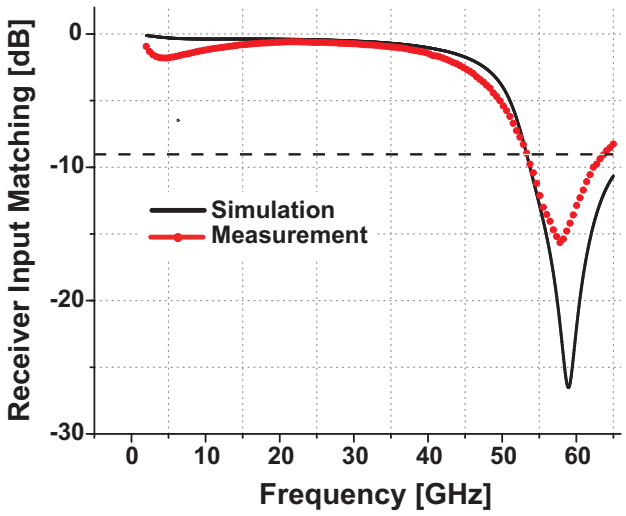


Figure 7.5: Measured return loss at the RF ports.

in the measurements is −2.5 dBm. An excellent LO port return loss has been measured as shown in Fig. 7.4. As it is shown in Fig. 7.3, the measured two-port balun insertion loss is about -1 dB at 60 GHz.

The RF port input match of the receiver is shown in Fig. 7.5 and is approximately below −9 dB over the entire 7 GHz of the 60 GHz band. The overall receiver gain is shown in Fig. 7.6. The receiver has a wide gain tuning range of 60 dB, which allows the system to operate with a wide dynamic range of input signals. The receiver -3 dB bandwidth is shown in Fig. 7.7 for various gain settings. The -3 dB bandwidth of the receiver varies from 3.2 GHz to 2.2 GHz when switching from low gain mode to high gain mode. The change in -3 dB bandwidth is because the output pole of the VGA changes during gain tuning. The VGA was also characterized separately so that the performance of the RF front-end could be determined. Measurements show that the RF front-end has a fixed gain of 18dB, very

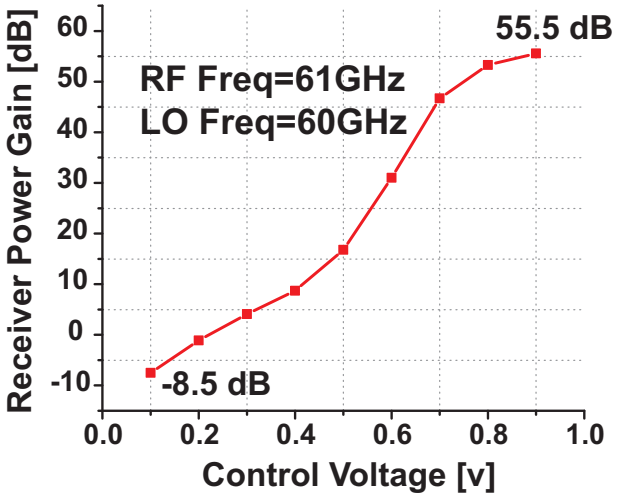


Figure 7.6: The measured receiver power gain as a function of control voltage.

closely matching our simulated performance. The large-signal performance of the receiver at the center band and its noise figure as a function of control voltage are shown in Fig. 7.8. Large signal operation and receiver linearity performance are characterized by single tone measurement and 60GHz power sensor and meter. The noise figure measurement was done using a 50-75 GHz noise source. Using noise source for the 6OGHz band is more accurate compared to the gain method for noise figure calculation. The noise figure is relatively constant over the band of interest, as shown in Fig. 7.9, and an average DSB noise figure of 6.2 dB is observed. Table I compares this receiver to several 60 GHz CMOS front-ends published in 2008 or before. The performance is very favorable, particularly with respect to the predictability, noise figure and the low power consumption.

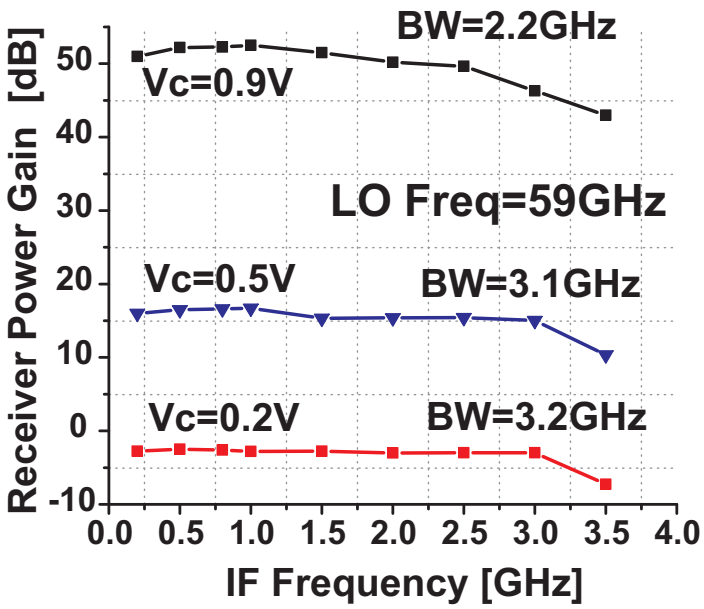


Figure 7.7: The measured receiver IF bandwidth as a function of control voltage.

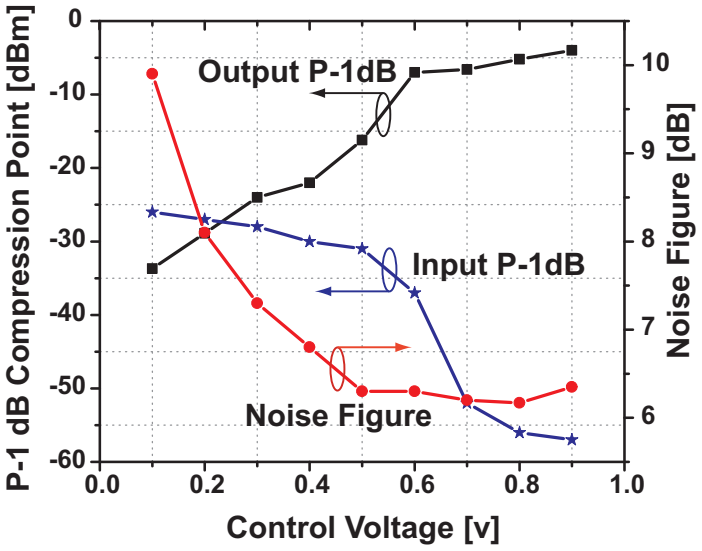


Figure 7.8: The measured receiver noise figure and linearity performance versus control voltage.

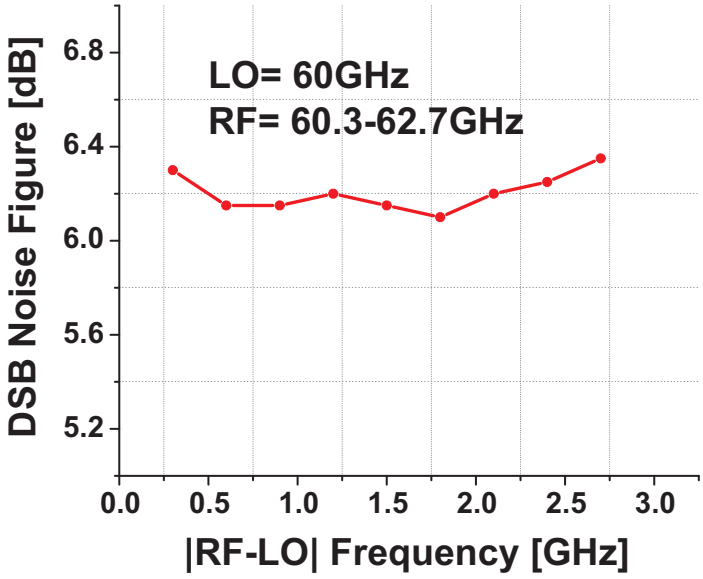


Figure 7.9: The measured receiver noise figure noise figure over the band.

	[13]	[15]	[29]	[30]	This Work
Frequency Range(GHz)	57-61	49-53	50-56	61.34-63.4	57-63
Noise Figure (dB)	5.7-8.8	6.9-8.3	7	8.4	6.1-6.35
Gain (dB)	18.3-22	26-31.5	16**	21.8-22.5	-8.5-55.5
P_{1dB} (dBm)	-27.5	-25.5	-21	NA	-26
LO Leakage to Input (dBm)	-65	-47	< -90	NA	< -77
LO Phase Noise (dBc/Hz @ 1-MHz offset)	-90	-95	off-chip	-90	off-chip
Power Consumption	32	65.6*	60	60*	24
Supply Voltage (V)	1.2	1.8	1.2	1.2	1
Chip Area (mm^2)	0.19	0.15	0.285	2.64	1.55
Technology CMOS	90-nm	90-nm	90-nm	90-nm	90-nm

$*$ Oscillator and synthesizer power consumptions are excluded.

$**$ Peak gain at 53GHz is 21.5dB.

Table 7.1: Comparison of several 60GHz receivers.

7.2 Conclusion

A low-power CMOS 60 GHz front-end receiver compatible with a direct-conversion I/Q architecture has been presented. A cascode LNA, Gilbert cell mixer, and an inductorless VGA comprise the receiver front-end. Accurate gain and noise measurements on component devices results in a robust and predictable design. We have shown that mm-wave design can differ significantly when operating a device close to the transition frequency f_t. Furthermore, the design of cascode amplifiers and Gilbert cell mixers requires careful considerations to maximize the gain and maintain stability over a wide frequency range. Careful layout and electromagnetic co-simulation were used extensively to realize the presented design.

Part II

Ultra Wide-band Pulsed Transmitter

Chapter 8

Introduction to Medical Imaging

8.1 mm-Wave for Medical Imaging

Medical imaging devices are playing an important role in medical screening, diagnosis and treatment. However, the cost of medical modalities are pretty high and they are mostly limited to hospitals and health care facilities. On the other hand, consumer electronics is becoming cheaper or more widely available due to technology scaling and heavy investments. Therefore, it would be very exciting and valuable to use the techniques that are used in consumer electronics and apply it to medical imaging market. By new innovations, it is possible to realize non-invasive, portable, battery-operated medical-imaging devices that are based on electronic circuitry.

With technology scaling, transistors become faster and smaller and realizing electronic circuitry at high frequencies are possible. Currently, most of the electronic circuits are operating at frequencies below 10GHz. However, it is expected that the frequency limit for transistors go up to 400GHz, entering the THz region. Microwave medical imaging of

biological material for frequencies beyond 30GHz is relatively unexplored and few works can be found for material characterization beyond 30GHz. However, for frequencies in the range of 10GHz, extensive research has been done on using electronics for medical imaging. For example, a confocal medical-imaging module was developed by Hagness [53] that could be used for breast cancer detection and screening. Traditional medical-imaging modalities for breast cancer detection like X-ray are invasive due to ionizing radiation and have high false positive rate and poor contrast. The approach proposed by Hagness is non-invasive and non-ionizing. The detection is based on the difference in permittivity and conductivity of the cancerous cells and healthy cells. Fig. 8.1 from [38] shows the contrast between cancerous and healthy breast cells in terms of conductivity and dielectric constant difference. Besides breast cancer detection [54] [55], microwave medical imaging can also be used for early detection of Melanoma [56] and non-invasive glucose monitoring [57] [58] [59].

To evaluate an imaging modality, metrics such as depth and lateral resolution, SNR and contrast are usually used. In the following sections, we will discuss system requirements for a power amplifier that can be used in a microwave medical imager.

8.2 Design Requirements for Power Amplifier in an Imager

8.2.1 Carrierless vs. Carrier-Modulated Pulse Transmission

In order to transmit and receive a pulsed signal, we have two options:

1. Carrierless pulse transmission

2. Carrier-modulated pulse transmission

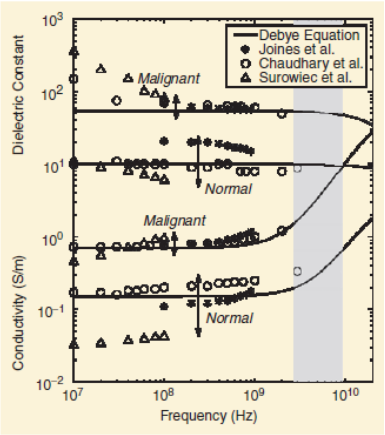


Figure 8.1: Conductivity and dielectric constant for normal and malignant breast cells [38].

Carrierless Pulse Transmission

A pulse can be transmitted without carrier by directly connecting the pulse generator circuitry to the antenna. On the receiver side, a detector circuitry (like a square law detector or diode) can be used to extract the information from the received pulse signal. This method of transmission and detection is simple, but has several disadvantages. In a carrierless narrow pulse transmission, the baseband pulse occupies a wide bandwidth that is stretched to DC. This means the antenna not only provides a very wide bandwidth, but also its bandwidth should cover very low frequencies. This makes the design of a wideband antenna challenging. A carrierless system also has a low sensitivity or SNR on the receiver side when diode or square law detection method is applied.

Carrier-Modulated Pulse Transmission

A sample of a carrier-modulated pulse transmitter is shown in Fig. 8.2. In this setup, the pulse will be modulated by the carrier frequency and will occupy the frequencies

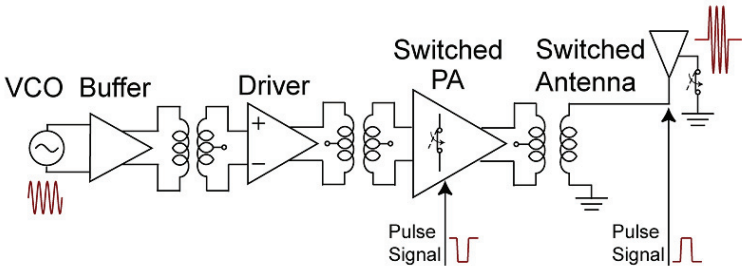


Figure 8.2: Sample of a simplified coherent pulsed transmitter [60].

around the carrier. This will relatively relax the design of a high bandwidth antenna. For a fixed fractional bandwidth, the antenna provides a wider absolute bandwidth if the center frequency of the antenna is higher.

$$fractional\ bandwidth = \frac{BW}{f_0} \tag{8.1}$$

In a carrier-modulated pulsed system, the local oscillator can be used in transmitting and receiving paths to extract the data from the carrier. This method has higher sensitivity compared to the diode or square law detection method mentioned in carrierless pulse transmission.

8.2.2 Frequency of Operation and Lateral Resolution

Radar lateral resolution is equal to: [61]

$$r_z = r \cdot \theta_z \tag{8.2}$$

$$\theta_z = \frac{\lambda}{D} \tag{8.3}$$

$$r_z = r \cdot \theta_z = r \cdot \frac{\lambda}{D} \tag{8.4}$$

in which r is the distance from the antenna, θ_z is the radar angular resolution, λ is the wavelength and D is the radar aperture. D could be physical or synthetic radar aperture. A synthetic aperture is formed through a phased array or pulsed array system. The wavelength is

$$\lambda = \frac{v}{f} \tag{8.5}$$

in which v is the speed of light in medium and f is the frequency.

$$v = \frac{c}{\sqrt{\varepsilon_r}} \tag{8.6}$$

in which c is the speed if light in vacuum and ε_r is the permittivity of the medium.

$$c = 3 \times 10^8 \frac{m}{s} \tag{8.7}$$

with $f_0 = 90\ GHz$ and $\varepsilon_r \simeq 4$ for human tissue at mm-wave frequencies we have

$$\lambda = \frac{v}{f} = \frac{3 \times 10^8}{\sqrt{4} \times 90 \times 10^9} = 1.66mm \tag{8.8}$$

So assuming that the object distance from antenna array is in the far field of antenna

$$R = \frac{2D^2}{\lambda} \tag{8.9}$$

The array synthetic aperture (D) could be calculated from the following equation

$$D = N.d \tag{8.10}$$

$$d = \frac{\lambda}{2} \tag{8.11}$$

where d is the antenna spacing. For N=10 antenna in each direction of the array, aperture size will be:

$$D = N.d = \frac{\lambda}{2} \cong 8.3mm \tag{8.12}$$

where N is the number of the antennas in each direction.

So lateral resolution will be:

$$r_z = r \cdot \theta_z = r \cdot \frac{\lambda}{D} = 1cm \cdot \frac{1.66mm}{8.3mm} = 2mm \tag{8.13}$$

Integration of Antenna on Chip

One of the main advantages of operation at mm-wave frequencies is the possibility of integration of the antenna on the chip. Antenna dimension is proportional to the wavelength $\lambda/2$ and the wavelength is inversely proportional to operating frequency. The silicon area is extremely expensive, especially in deep sub-micron technologies like 65 and 40nm. This prohibits the integration of the antenna on the chip at low frequencies due to the large footprint of the antenna. However, at mm-wave frequencies, the wavelength is small in the range of several millimeters (ex. 1.66mm at 90GHz), which opens up the possibility of antenna integration on silicon.

High Fractional Bandwidth Requirement for Imager

In order to realize a short pulse, the system requires a wide bandwidth. As shown before, a high bandwidth is easier to realize at high frequencies.

8.2.3 Depth Resolution and Pulse Width

If we assume that a pulse is sent in the form of a square wave and we don't do any additional processing on the received signal to increase the depth resolution, the following equation could be used to provide a first-hand estimate on the depth resolution of a pulsed radar system[61].

$$r_d = \frac{1}{2}\frac{c\tau}{\sqrt{\varepsilon_r}} = \frac{1}{2}\frac{c}{B\sqrt{\varepsilon_r}} \tag{8.14}$$

where r_d is the radar depth resolution, τ is the pulse width, c is the speed of light in vacuum, B is the radar bandwidth and ε_r is the medium permittivity. If we assume that the pulse width is 40ps and ε_r is 4 for biological material at microwave frequencies, the depth resolution will be:

$$r_d = \frac{1}{2}\frac{c\tau}{\sqrt{\varepsilon_r}} = \frac{3\times 10^8 \times 40 \times 10^{-12}}{2\sqrt{4}} = 3mm \tag{8.15}$$

Chapter 9

Design Considerations for a Wideband 90 GHz Power Amplifier in Silicon

9.1 Introduction

The millimeter wave band (mm-wave) has the potential for various wireless applications. The available 7 GHz bandwidth of the 60 GHz band has been explored for high-speed, short-range wireless communication including applications like high-definition video transmission, wireless Gigabit Ethernet and point to multi-point desktop connection. 77 GHz band offers opportunities for automotive radar and 90 GHz band is used for passive imaging. The 90 GHz band can also be used for active imaging with potential applications in medical screening and diagnosis.

mm-Wave systems that are realized in III-V technologies like GaAs and InP, offer superior performance in comparison with silicon-based technologies like CMOS and SiGe. For example, power amplifiers have been implemented in III-V technologies with 28dBm of power and 20-40 percent PAE [62][63]. However, these III-V technologies do not provide acceptable integration capabilities. They are considerably more expensive compared to silicon-based technologies with a low yield of manufacturing. Due to these shortcomings, these technologies could not find their way to the consumer market.

The main advantage of silicon-based technologies are their integration capabilities with high levels of system complexity as well as their relative low cost and high yield of integration. Technology scaling increased the frequency range of operation for these silicon-based technologies by increasing the device f_T and f_{max}.

Power amplifiers (PAs) are still one of the most challenging blocks in mm-wave systems. Limited breakdown voltage of transistors in silicon technologies, low resistivity substrate and lossy interconnects, low transistor gain at mm-wave and lossy matching networks bring significant challenges to the design of a power amplifier in terms of delivered output power and power-added efficiency (PAE).

To overcome some of the challenges of standard silicon technology and to increase the achievable performance of mm-wave circuits, several approaches have been investigated in academia and industry. Substrate resistivity in a standard silicon technology is low and is typically in the range of $10\Omega - cm$. Low resistivity substrate increases the loss of passive structures that are used in the mm-wave design. SOI technology could be used to improve the performance of mm-wave blocks since it has a high resistivity substrate. Using ultra-

thick top metals and increasing their distance from the substrate can also lower the loss of passive structures. However, these approaches add to the overall cost of the mm-wave chip and make the final product more difficult to compete in the consumer market. As the consumer market is price sensitive, the cheapest technology and methodology that can offer the same performance will prevail.

The importance of high-output power and efficient PAs with high PAE comes to the picture when we are dealing with portable applications. As mm-wave is finding its way into the portable consumer applications and the battery life is limited, high PAE PA are very desirable since they consume lower dc power. Most of the mm-wave PAs that are reported in the literature have very low reported PAEs [48] [39] [40]; however, few PAs also reported to have PAEs above 10% at 60GHz and 77GHz [34][51].

As we move toward sub-micron technologies, transistor sizes shrink and the digital portion of the chip becomes smaller and smaller; however, if we are to realize a single chip solution for the mm-wave system, RF part has to scale down too. However, passive structures do not scale with technology nodes. For example, a microwave approach for mm-wave design incorporates the use of many transmission lines for matching networks, interconnects, power combiners, dividers and couplers. Transmission line length is usually a factor of the wavelength. Since wavelength at 60 GHz is 2.5 mm on silicon, a big portion of the expensive die area is occupied by passive devices [64][65][66][67]. There have been some reported designs for mm-wave to take advantage of on-chip transformers for matching networks and power combining on silicon [42][68].

This chapter is organized as follows. Section 9.2 reviews the previous work on

mm-wave power amplifiers in SiGe technology. Section 9.3 will show the architecture for a wideband 90 GHz power amplifier. In sections 9.4 and 9.5, measurement setup and results of the 90GHz power amplifier are presented.

9.2 Previous Work on mm-Wave Power Amplifiers in SiGe Technology

Several recent publications have reported mm-wave PAs in SiGe $0.180/0.13\mu m$. Floyd et al. [39] demonstrated a class AB power amplifier in 0.13um SiGe process as part of a 60GHz transceiver chip. This power amplifier uses a two-stage balanced architecture to feed a differential antenna directly. The PA achieves 10.8dB of gain, 11.2dBm of P_{-1dB} and 16.2dBm of P_{sat} at 61.5GHz, using a 2.5V supply. In [49] a fully integrated 60GHz SiGe power amplifier with automatic level control is demonstrated. The design consisted of a single stage push-pull cascode amplifier in differential mode. It uses microstrip lines for input and output matching and biasing. At 60GHz, the design has a peak power gain of 18dB, P_{-1dB} of 13.1dBm and peak power added efficiency of 12.7%, using a 4V supply. Among other power amplifiers at 60GHz, a design by Wang [41] generates 15.8dBm of power with 16.8% power added efficiency. To achieve higher efficiency at 60GHz a class-E design is reported by Valdes-Garcia et al. [52], demonstrating 11.5dBm of output power with 20.9% PAE.

In order to generate higher output power at 60GHz, several power-combining techniques have been reported in the literature. In [50] a distributed active transformer is used to combine the power of eight cascode amplifiers into a differential 100Ω load. It generates

23dBm of saturated power at 60GHz. The transformer utilizes stacked coupled wires with high coupling factor of 0.8 at 60GHz. The two-stage amplifier has 13dB of compressed gain (at P_{sat}) and 6.3% of PAE using a 4V supply. Afshari [47] exploited the idea of electrical funnel as a broadband power combiner. Four distributed power amplifiers drive this power combiner to generate 21dBm of power at 85GHz. Each of the four distributed power amplifiers consists of eight cascode stages. The design has 8dB of power gain and 4% of PAE in 0.13um SiGe process. A 77GHz class-AB power amplifier has been demonstrated by Komijani [51] which uses on-chip power combining to generate 17.5dBm of saturated output power. The design has 12dB gain at saturation, P_{-1dB} of 14.5dBm and 12.8% PAE. Li et al. [40] also demonstrated high output power of 18.5dBm without power combining in differential mode at 77GHz.

9.3 Transformer-Coupled Power Amplifier

The power amplifier is designed as two stages of pseudo differential cascode amplifiers. Its block level schematic is shown in Fig. 9.1. Circuit-level schematics of this design is also shown in Fig. 9.2. Input and output ports use GSG single-ended probe pads for measurement purposes only. At the time of this design, a fully differential 110GHz 4-port VNA was not available so the measurements were done using 2-port 110GHz Anritsu vector network analyzer. Single-turn overlaid transformers are used for the input and inter-stage matching networks as well as output stage power combining. Differential transistors are biased at their peak f_T current density, which is about $1.2\frac{mA}{\mu m}$ (current per emitter finger length). Each transistor uses five fingers to maximize the maximum available

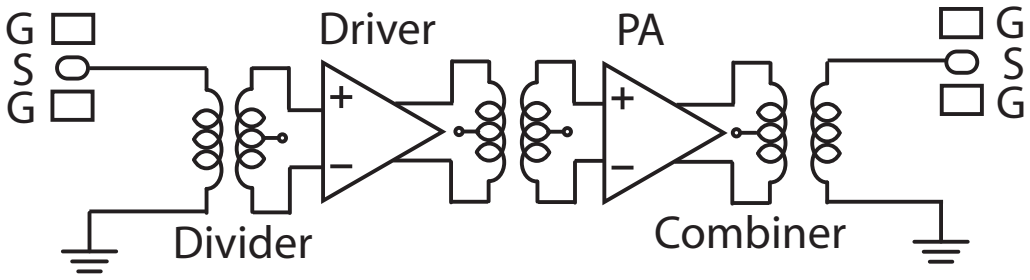


Figure 9.1: Block level schematic of the transformer coupled 90GHz power amplifier.

gain (G_{max}) of the device by reducing transistor parasitic inductance. The first stage uses $5(finger) * (2\mu m)$ transistors and the second stage uses $5(finger) * (4\mu m)$ transistors. The design consumes about 72mA of current from a 4V power supply. The details of the design of 90GHz transformer coupled power amplifier will be reviewed in the following sections.

There are several advantages in using a differential architecture for the mm-wave design and we will review some of these advantages here. Differential architecture makes the design less sensitive to its surroundings and removes the need for proximity of bypass capacitors. Since the size of the bypass capacitors are limited to their self-resonance, there is an upper bound on how big a bypass capacitor can be. The performance of the single-ended design can suffer from this limited bypass capacitor. However, a differential design is relatively independent of this requirement by providing a virtual ground at the symmetry points. But it should be emphasized that bypass capacitors are still needed in the differential design to provide short impedance path to ground for possible common mode excitation. However, the requirement on these common mode bypass capacitors are relaxed in a differential design. Also, a differential design offers more predictable performance by

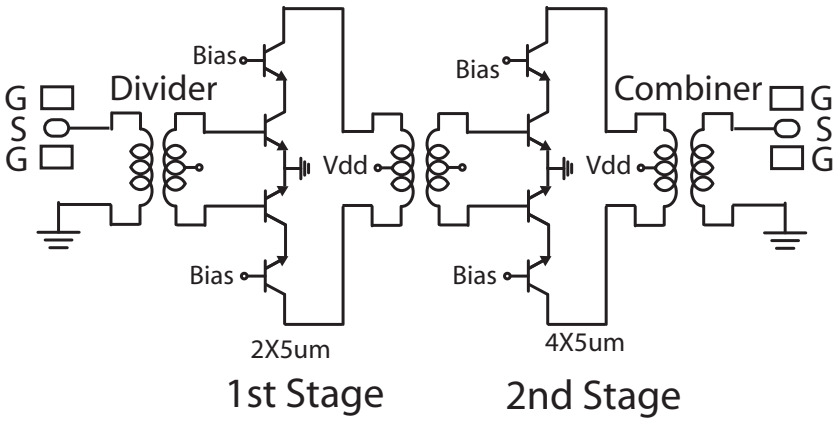


Figure 9.2: Circuit level schematic of the transformer coupled 90GHz power amplifier.

confining high-frequency signal loops. As the performance of an mm-wave design is highly dependant to its layout, a more confined and well-defined signal loop helps in predicting the performance of circuits at these frequencies. Since transformers have a very confined signal loop due to their structures, they have been used in this design for input, interstage and output-matching networks. Close proximity of the differential path and its transistors along with using differential transformers help to get a performance closer to the simulations at 90GHz. Of course, mm-wave modeling of the transistors should also be done accurately to give us the desired results. Modeling of active and passive structures for the mm-wave band has been discussed extensively in the first part. Fig. 9.3 shows how the differential signal loop is well defined in a differential PA and the values of the inductances that are used for matching networks could be estimated accordingly. The transistors' layout is shown as rectangles with node connections (e),(b),(c) for emitter, base and collector. Differential signal path at the transistors input and output are shown by the dotted red line. The direction

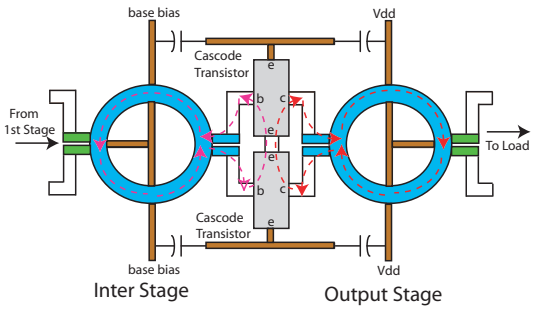


Figure 9.3: Differential signal loop

of the loop is shown by an arrowhead sign on the dotted line.

9.3.1 Bipolar Transistor Voltage Swing

Technology breakdown voltages for the bipolar device in 0.13um SiGe process are: $BV_{CEO} = 1.6V$ and $BV_{CBO} = 5.5V$. BV_{CEO} is the collector to emitter breakdown voltage when the base node is open Fig. 9.4. As long as the seen impedance that is driving the base node is small, we can have a voltage swing between collector and emitter that is considerably higher than BV_{CEO}. If this requirement is satisfied, we will be possibly limited to BV_{CER}, which is about 4.5V in this technology. To ensure high-voltage swing V_{CE}, the impedance seen at the base of the cascode transistors should be small in DC and AC operation mode. At DC, the bias circuitry that is connected to the base of the cascode transistor provides a low impedance of 50Ω. For AC operation, we take advantage of the differential nature of the design and close proximity of the differential transistors in layout. Since the base of the cascode transistors are connected together, differential signal loop at the base of the cascode transistors provides a very small external AC impedance (close to zero).

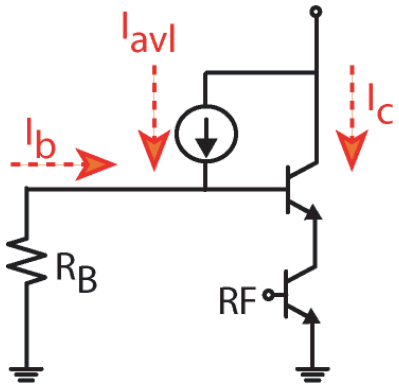


Figure 9.4: Avalanche current in bipolar transistor due to external impedance at the base junction.

9.3.2 Large Signal Stability

Stability analysis is very important in the power amplifier design. Since antenna impedance can be a function of its environment, the load impedance of the power amplifier can effectively change. This means that even if the PA is stable for the nominal load, it can potentially oscillate for other load values. It is preferable to design a power amplifier to be unconditionally stable to prevent any possible oscillation. Since power amplifiers are normally operating in large signal mode, not only small signal stability factors such as K and μ are important, but also large signal stability factors should be considered. Large signal stability is simulated by driving the PA with the large signal input to have PA output voltage swing close to its normal or peak value. Then the same stability metrics like μ and $\mu^{'}$ can be generated while the large signal input is present. The PA stability curves for the 90GHz transformer coupled design in this work is plotted in Fig. 9.5,Fig. 9.6. As can be seen, these values always stay above one across all the frequencies indicating the design is unconditionally stable.

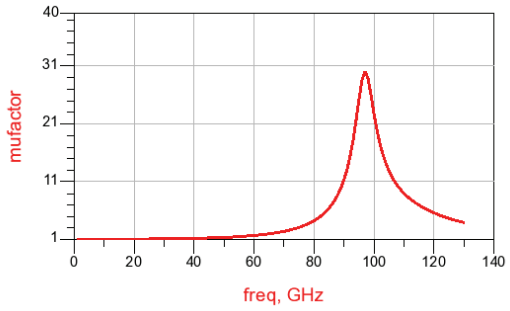


Figure 9.5: Large signal μ of the two-stage power amplifier.

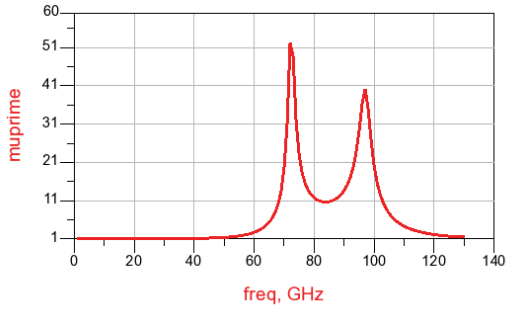


Figure 9.6: Large signal $\mu^{'}$ of the two-stage power amplifier.

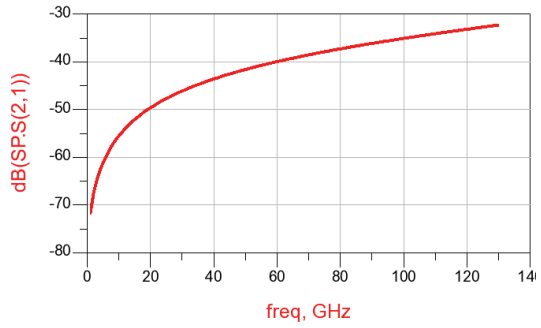


Figure 9.7: Common mode attenuation of the transformer without surrounding ground.

9.3.3 Common Mode Stability

When we are dealing with the design of a differential power amplifier, not only does differential stability have to be considered, but common mode stability is an important factor as well. Baluns suppress the common mode signal by nature. However, the amount of suppression on common mode is usually a function of frequency. Common mode suppression can be affected by the ground path surrounding the balun and interwinding capacitance between transformer windings. The common mode suppression of the balun for the two cases of with and without ground surrounding is plotted in Fig. 9.7 and Fig. 9.8.

As can be seen, common mode attenuation degrades by about 8dB when we have ground path surrounding the transformers. However, having ground path surrounding the transformer is preferable since it makes transformer modeling more predictable.

In order to calculate the amount of common-mode suppression and common-mode impedance load of the amplifier, we first try to model the common mode path of the signal in a transformer-coupled power amplifier for the input, interstage and output stages. Fig. 9.9 shows the common mode loop on the conceptual layout of the cascode transistors. Fig. 9.10

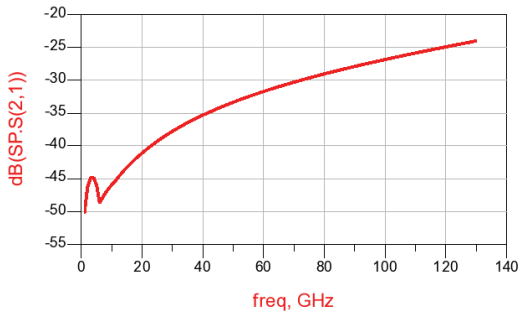


Figure 9.8: Common mode attenuation of the transformer with surrounding ground.

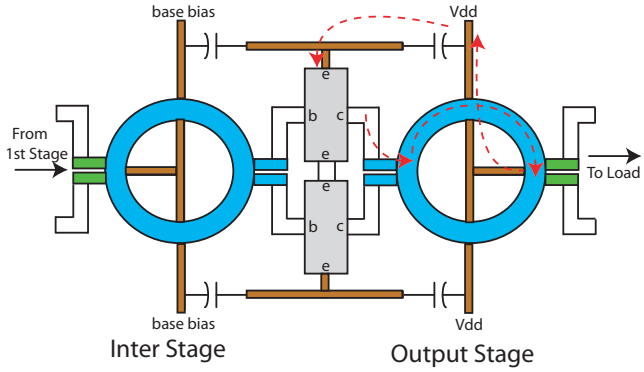


Figure 9.9: Common mode loop for interstage cascode transistors

shows the small signal half circuit for the common mode loop for the interstage transistors. These effects can be simulated by driving the PA in common mode of operation and knowing the common mode attenuation of the signal path.

To ensure common-mode stability, the common-mode load should fall inside the common-mode stability region of the PA. Since in our design, the input port is single-ended driven, it has a considerable common-mode signal. As shown above, with ground surrounding the transformers, the common-mode attenuation through balun is in the range

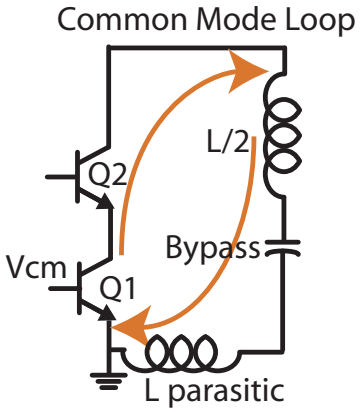


Figure 9.10: Small signal half circuit for the Common mode path for the interstage transistors

of -25dB at 90GHz. To improve the common-mode attenuation, a resistor can be added to the base of the bottom transistor (Q_1) on the center tap path. This resistor only will take part in common-mode analysis and increases the common-mode attenuation. It effectively breaks the common-mode loop open from the center tap point. This resistor will not affect the differential operation of the circuit. Adding a resistor to the base of the cascode transistor (Q_2) can help too. However, the resistor value cannot be too high since it may limit the transistor voltage swing V_{CE} as mentioned previously and can also add additional stability concern to the design.

Bias Network in Transformer-based Design

A balun structure provides a convenient biasing point at its center tap. The center tap is a virtual electrical ground, which in a symmetric balun coincides with the physical center of the balun layout. Fig. 9.11 shows the center tap connection for the transformer.

In this approach, the dc signal is brought to the center tap from the two sides,

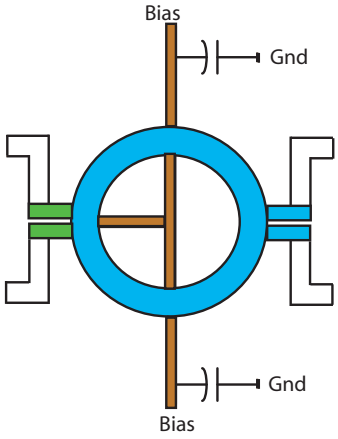


Figure 9.11: Transformer center tap connection for biasing.

perpendicular to the primary and secondary routings, which minimizes the magnetic interference of the DC routing on the primary and the secondary windings. Also, by using the lower metal layers for this dc connection, self-resonance will not be affected much. Another advantage of this approach is that the common mode loop is formed by two parallel paths, which minimizes the common mode loading. By decreasing the common mode load impedance, common mode stability will be improved in our design.

9.3.4 Power Combining Technique

Transistor Maximum Delivered Output Power

In order to achieve a high level of output power, power amplifiers are designed to deliver a maximum amount of output power. This approach is usually done by choosing the maximum allowable transistor size at the frequency of operation. Usually, the load impedance that each transistor drives is optimized to simultaneously consider the trade-

off between maximum delivered output power and acceptable output stage power gain. However, there are some other limitations on the impedance that each transistor can drive. By decreasing the real part of the load impedance that each transistor can drive, not only the power gain of the transistor drops but also the transistor becomes more prone to oscillation. Since stability is a major concern in designing high-output power PAs, optimum load selection has to be carefully considered in mm-wave PA design. The maximum output voltage swing is also limited to the junction breakdown voltages. So the maximum current that a transistor can deliver will be limited by the following equation in an optimum PA design.

$$V_{max} = R_{load} \times I_{peak} \tag{9.1}$$

In a class AB push-pull differential design, this current I_{peak} is equal to the dc current of the transistor. So if we assume that the maximum dc current of the transistor is fixed, then we have the next constraint for the current density for maximum f_T. In the SiGe $0.13\mu m$ process, this optimum current density is about $\frac{0.12mA-0.13mA}{1\mu m\ fingerlength}$. Therefore, the optimum device size can be determined. However, we have to be careful that this device size still provides acceptable power gain. At mm-wave frequencies, a transistor size cannot be arbitrarily increased. Since a big device leads to a huge layout with a lot of parasitics (specially parasitic inductances). These parasitic inductances are usually difficult to capture in simulation unless some measured data is available. These parasitic inductances will severely degrade the power gain of the transistors at mm-wave frequencies. For example, we can think of parasitic inductance at the emitter as emitter degeneration, which effectively

reduces the g_m of the transistor. The gain factor will be:

$$Gain\ factor = \frac{1}{1 + g_m \cdot L_s \cdot \omega \cdot j} \tag{9.2}$$

where L_s is the parasitic inductance at the emitter junction.

The parasitic inductance at the base and drain junctions could be reduced by using multi-finger structures. In our design, we have used a maximum number of fingers that was modeled by the foundry for the mentioned reason. However, by increasing the number of fingers beyond a certain limit, the high-frequency current distribution to all the fingers at base and collectors may not be symmetric anymore. In a big layout with many fingers, transistors in the center will not get the same portion of the ac current as the transistors at the two ends of the layout and will not deliver the same power gain or output power. Thus, the overall expected power gain and output power of a big transistor could be smaller compared to simulations at mm-wave frequencies. Therefore, special care has to be taken in working with big device sizes at mm-wave frequencies. Having measured the result of such big transistor layout and modeling the parasitic inductance at the gate/base, drain/collector and source/emitter will be beneficial for achieving more predictable performance at mm-wave frequencies like 60GHz and beyond.

Output Stage Power Combining

Since the maximum output power of each active transistor is limited, other techniques could be used to increase overall delivered output power. For example, several power-combining techniques could be used such as on-chip power combining or spatial power combining. On-chip power combining could be done using passive devices like Wilkinson

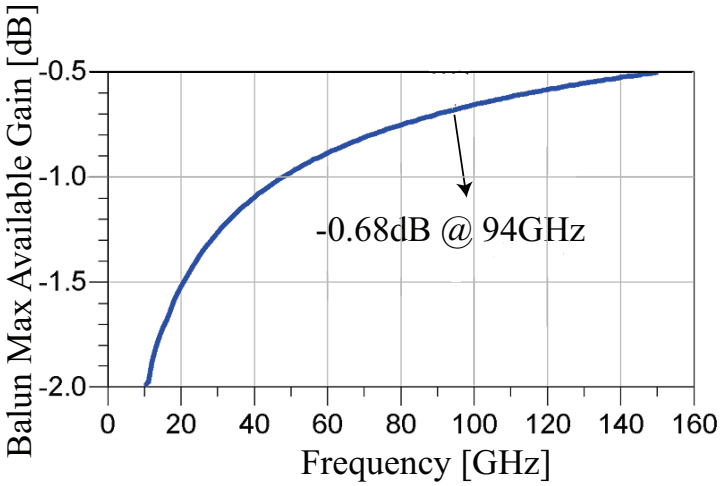


Figure 9.12: Simulated maximum available gain of power combining balun.

power combiner or transformer. Spatial power combining is done through phased-array or timed-array transmitters. In theory, the total output power in a phased-array transmitter can go up by $20 \cdot \log N$ where N is the number of antennas. Here we focus on on-chip power combining and have used the output stage transformer as a power combiner. We have chosen transformers over the Wilkinson power combiner since Wilkinson power combiners usually take more die area and add more loss to the signal compared to transformers.

In theory, power combing through the transformer should increase the total output power by 3dB. However, the balun adds additional combining loss and this number is less than 3dB in practice. A transformer is characterized by its maximum available gain or equivalently by its minimum insertion loss. The simulated result of the maximum available gain of the transformer that was used for the power combining is plotted in Fig. 9.12

At 94GHz, the balun minimum insertion loss is 0.68dB. It has to be emphasized

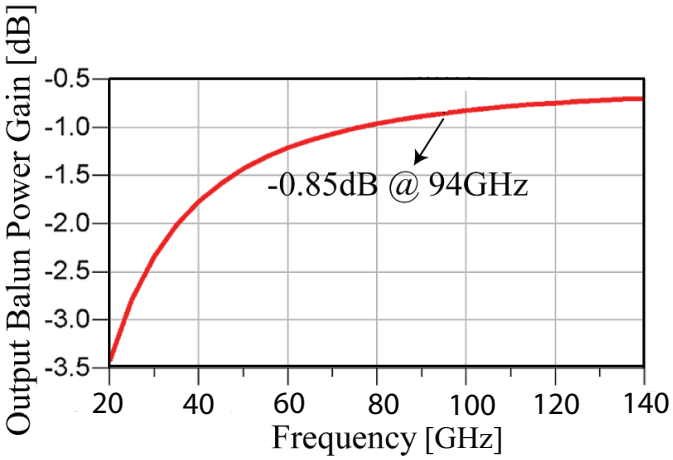


Figure 9.13: Power gain of the combining output transformer.

that this insertion loss is the best that we can get if we terminate the balun to the conjugate match impedances at the input and output ports. In practice, the output stage balun is designed to transform the 50Ω output port optimum load for maximum power delivery. So on one side of the termination, the balun sees the 50Ω load, and on the other end, it sees the output impedance of the transistor. The balun size is chosen in a way that its inductance tunes out the device parasitic capacitance. The power gain circles could be drawn for the balun to see how each choice of impedance at the input and output port will change the combining efficiency of the transformers. The simulated power gain of the transformer that was used in our design for the used impedances in the design of this power amplifier is shown in Fig. 9.13. The power gain at 94GHz is -0.85dB, which is about 0.2dB less than its best optimum value.

9.3.5 Multi-Stage PA Design Methodology

In the design of a two-stage PA, the ratio between transistor sizes is a function of the power gain of those two stages. Since the last stage is designed for maximum output power, the stage preceding the last stage (first stage) should be sized appropriately to be able to supply the required power to the input of the last stage. If the driver is oversized, it will hurt the PA efficiency (PAE). If this stage is undersized, it will never supply enough power to the last stage to reach maximum output power delivery. A small size driver will have low P_{-1dB}, which may not be sufficient for the last stage requirement. Assuming that transistor output power is proportional to its size, if each stage has a power gain of 5 or 7dB (including input and output matching network loss), then the ratio between last stage and driver stage could be 5:1. This method is mostly for P_{-1dB} calculation.

In a two-stage power amplifier, power gain, output power and efficiency of each stage will have an impact on the overall PA performance. These parameters can be optimized to get the best overall performance for the design. The overall PAE of a two-stage PA is a function of power gain and PAE of each of those two stages. The overall PAE is equal to:

$$PAE \approx \frac{1}{\frac{1}{PAE_2} + \frac{1}{G_2 \cdot PAE_1}} \tag{9.3}$$

where PAE_1 and PAE_2 are first- and second-stage power added efficiency and G_1 and G_2 are first-stage and last-stage power gain. In the above equation, it is assumed that $G_1 - 1 \approx G_1$ and $G_2 - 1 \approx G_2$. From Eqn. 9.3 it could be seen that if last stage power gain G_2 is high enough, the impact of the first stage on overall PAE is minimal.

Considering the above factors, we have used much bigger transistor size for the driver stage because of the following reasons:

1. We wanted to guarantee that we will be able to drive the output stage PA into saturation. In the saturation region, the power gain of the last stage drops significantly. So the driver stage has to supply a high amount of power to the final stage for P_{sat} measurement. This means that the driver size should be bigger compared to the case that output stage only has to reach to its -1dB compression point.

2. In case of any large signal modeling inaccuracy of the BJT transistors, the driver still maintains some margin for maximum output power measurement.

3. Since the last stage has about 10dB of power gain, based on Eqn. 9.3, the penalty on overall PAE is minimal.

In this design, the two differential transistors in the last stage are sized as $(5*4\mu m)$ and the driver stage are sized as $(5*2\mu m)$. Each of these transistors are biased at the current density for peak f_T.

9.4 Measurement Setup of the Power Amplifier

Measurement of the W-band power amplifier was done using Anritsu vector network analyzer (VNA) 37397C with extended W-band module 3742A-EW [70]. The setup could be used for measurements up to 110GHz. S-parameter measurement was done with on-wafer probing using Cascade 12000 Probe Station. Cascade Microtech 110GHz 100um pitch infinity probes were used for on-wafer measurement [72]. The whole measurement

setup was calibrated up to the tip of the RF probes using W-band calibration substrate 104-783 with 75-150μm pitch [73].

Measurement setup of the W-band power amplifier is shown in Fig. 9.14. W-band signal up to 110GHz is generated using the above VNA with extended W-band module 3742A-EW. 3742A-EW module can deliver power up to -4dBm in the W-band. Delivered power of the 3742A-EW module versus frequency is shown in Fig. 9.15. W-band external power amplifier was used to brig up the signal power level for P_{-1dB} and P_{sat} measurements. The external PA had P_{-1dB} of better than 10dBm with small signal power gain of 14dB for the W band (75GHz-110GHz). An additional PA driver may be necessary to provide enough signal gain to bring the power level high enough for DUT measurement. Since these external modules have WR10 waveguide interface, several additional WR10 to 1mm W band connectors were required for DUT measurement. Each of those 1mm W band to WR10 waveguide adapters has an insertion loss of better than 1dB for a frequency range of 75-110GHz [69]. Gore 132-458 110GHz cable was used at the input section for bringing W-band signal from the external PA to the W-band infinity probe and was used at the output section to connect the infinity probe to the power sensor [71]. 132-458 Gore cable has insertion loss of better than 3dB at max frequency 110GHz.

Power measurement is done using W8486A W-band power sensor [74] and E4418B power meter [75]. Cables and RF probes losses are de-embedded from subsequent power measurements of the DUT.

The DUT is the PA with input and output RF pad of 100μm pitch. DC biases are brought from outside to the DUT using DC probe card. PA measurement result will be

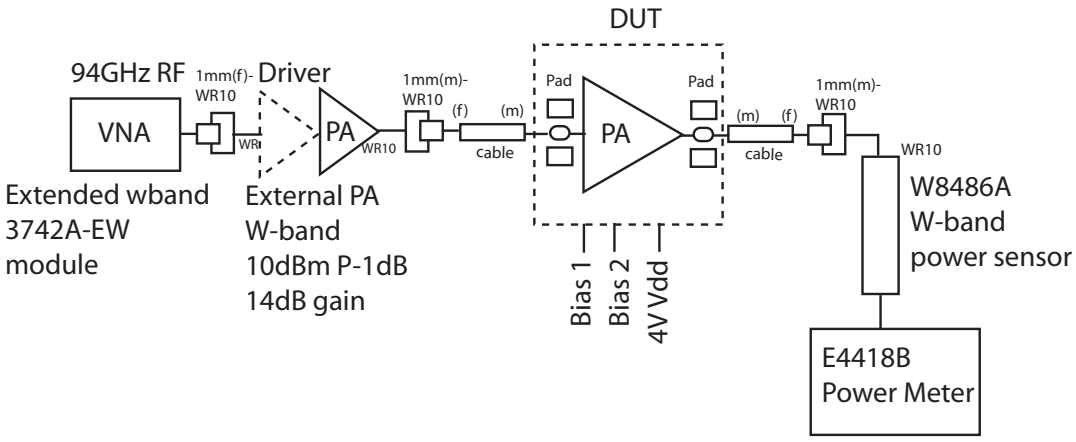


Figure 9.14: Measurement setup of W-band power amplifier.

Extended W Band (WR-10) Waveguide (3742A-EW Modules)

Frequency (GHz)	Max Signal into Port 2 (dBm)	Port 1 Power, Typical (dBm)	Noise Floor (dBm)	System Dynamic Range (dB)	Receiver Dynamic Range (dB)
65	+8	–6	–85	79	93
75	+8	–4	–94	90	102
85	+8	–6	–96	90	104
100	+8	–5	–92	87	100
110	+8	–7	–89	82	97

Figure 9.15: Extended 3742A-EW W-band module, Source: Anritsu documentation, ME7808B Broadband and Millimeter Wave VNA.

discussed in the next section.

9.5 Measurement Results of the Power Amplifier

The differential transformer coupled 90GHz power amplifier is implemented in $0.13\mu m$ SiGe BICMOS process with f_T=230GHz. The die photo of the power amplifier is shown in Fig. 9.16. PA occupies die area of $450 \times 329\mu m^2$ (including pads) and consumes 86mA of dc current (small signal input) from a 4V power supply. PA S-parameter S_{11}

and S_{22} are shown in Fig. 9.21. Input return loss of the PA is better than -10dB for frequencies from 60GHz to 108GHz. PA small signal power gain is $\sim 15dB$ at 89GHz with f_{-3dB} bandwidth of 53GHz. Power amplifier measured and simulated power-added efficiency curves are plotted in Fig. 9.17 and Fig. 9.18. The PA has a measured peak PAE of 9.25% at 89GHz. The main reason for the difference between measured and simulated PAE in a high output power PA could be due to the difficulty of accurate modeling of the bipolar device in high-current mode of operation. The PA simulated and measured power gain and output power are shown in Fig. 9.20 and Fig. 9.19. The PA P_{1-dB} and P_{sat} are relatively predicted well by simulations. However the power gain is smaller in measurement which could be due the fact that the transistors were not specifically modeled for 90GHz band operation. In this process, we relied on the transistor models, provided by the foundry and no additional modeling was done on transistors at the design phase. Fig. 9.22 shows PA saturated output power for several frequencies in the W-band.

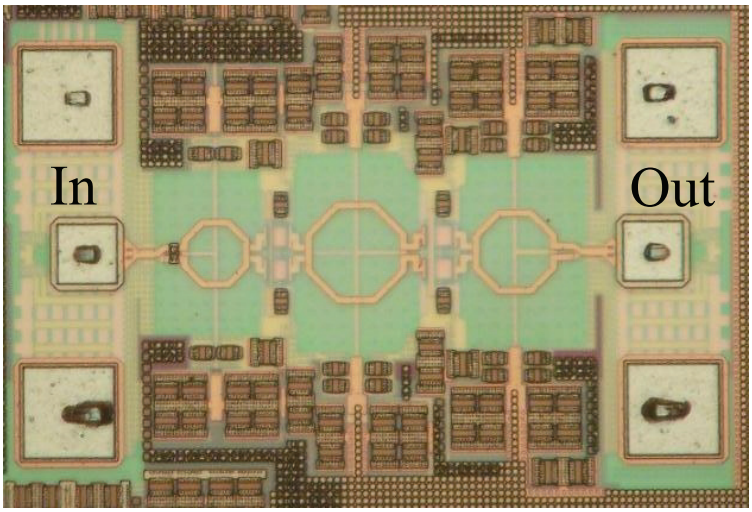


Figure 9.16: Die photo of the transformer coupled 90GHz power amplifier.

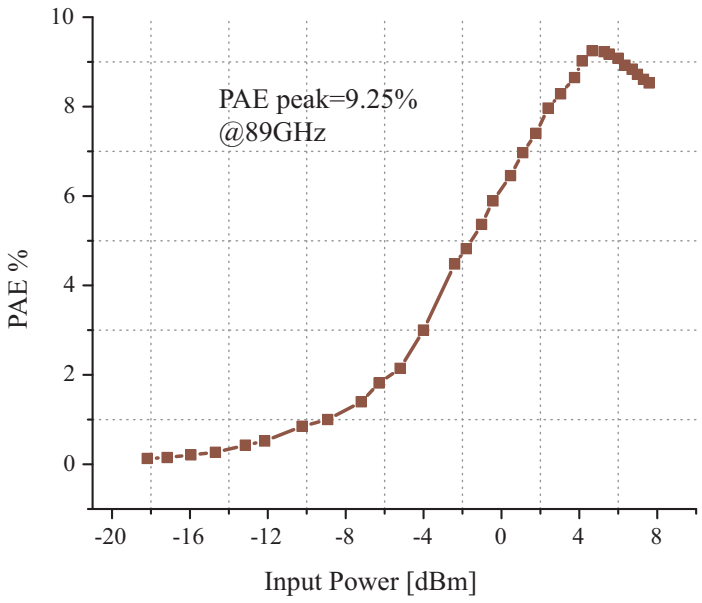


Figure 9.17: Measured power added efficiency of the 90GHz power amplifier.

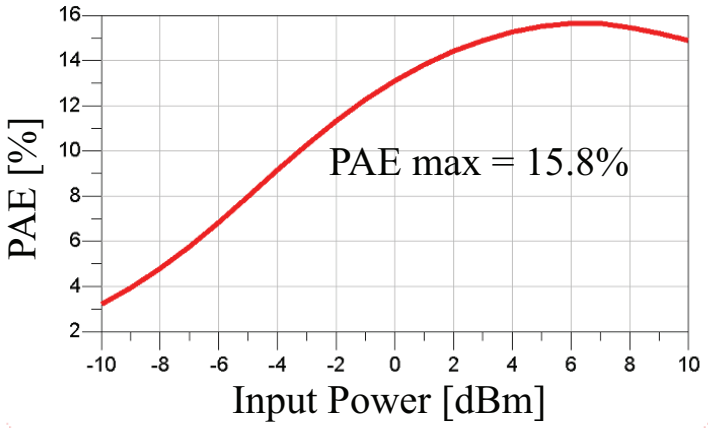


Figure 9.18: Simulated power added efficiency of the 90GHz power amplifier.

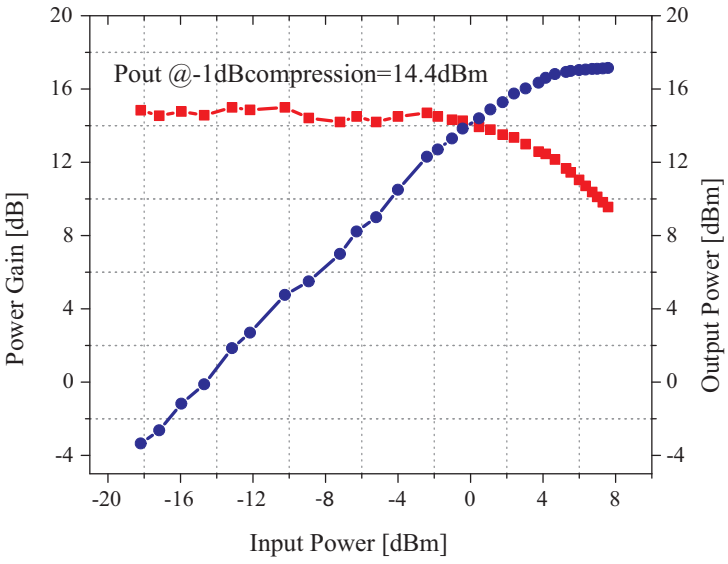


Figure 9.19: Measured PA power gain and output power curves at f=89GHz.

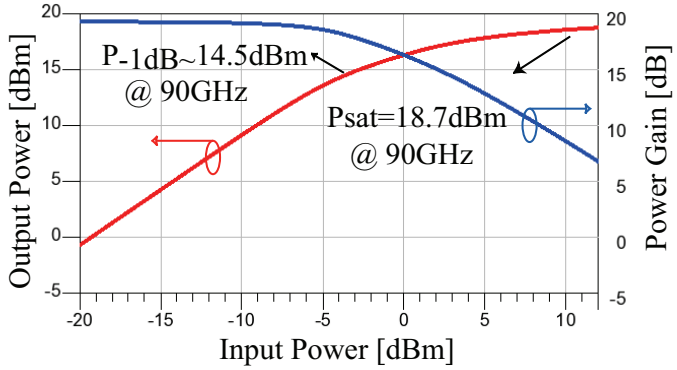


Figure 9.20: Simulated PA power gain and output power curves at f=89GHz.

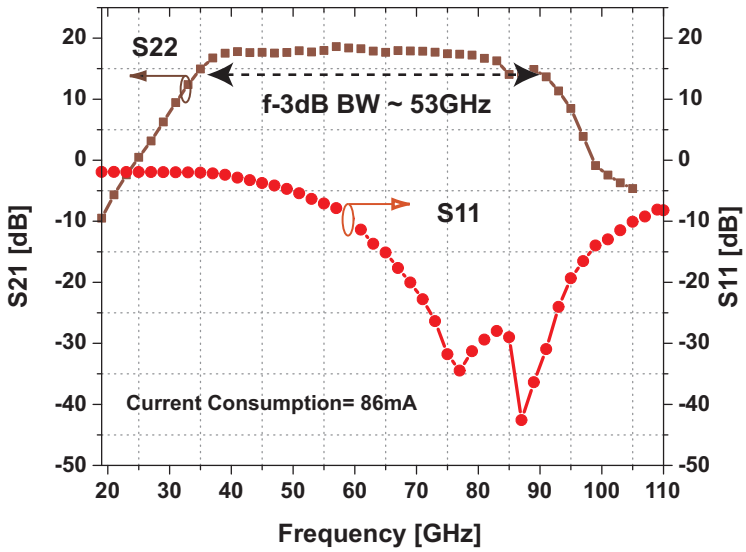


Figure 9.21: Measured PA S-parameters S_{21} and S_{11}.

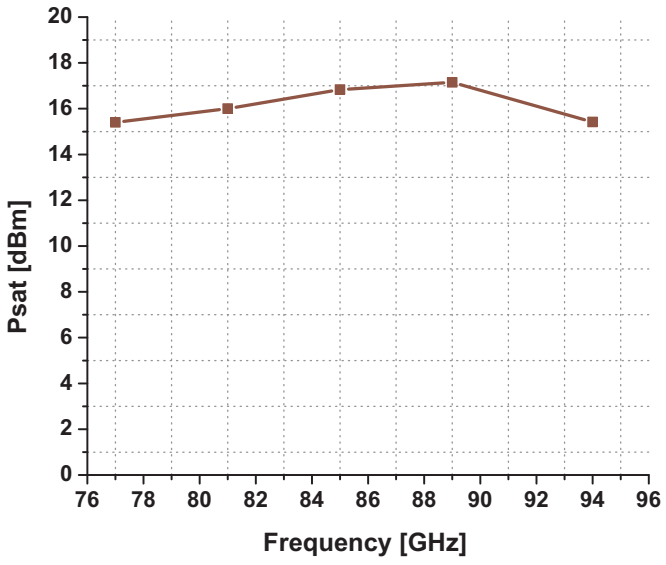


Figure 9.22: Measured PA saturated output power versus frequency

Chapter 10

Design Considerations for a Wideband 90 GHz Switched Power Amplifier in SiGe Technology

In this chapter, design considerations of a wideband 90GHz switched power amplifier in 0.13μm SiGe technology are investigated. The chapter is organized as follows. Section 10.1 discusses the concepts of switching to realize a pulse modulated signal at mm-wave frequency band. Section 10.2 explains the architecture of the switched PA. Measurement setup and measurement results of a prototype switched power amplifier and carrier modulated pulsed transmitter are presented in sections 10.3 and 10.4.

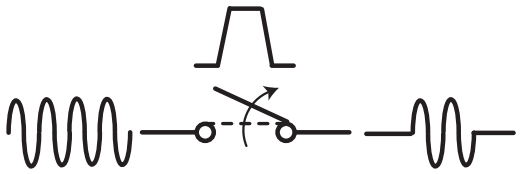


Figure 10.1: Conceptual Switching function

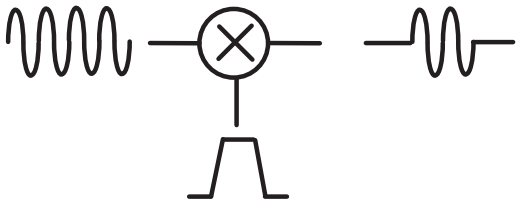


Figure 10.2: Conceptual Mixing functionality to generate carrier modulated pulsed signal

10.1 Switching Concept

Conceptual switching function for generating a carrier-modulated pulse signal is shown in Fig. 10.1. In other words, in order to switch the high-frequency carrier signal, we need to multiply the carrier signal with a baseband pulse signal. Fig. 10.2.

If x(t) is RF carrier signal and s(t) is the rectangular pulse signal with pulse width (2a), then the switching operation in time domain could be shown as:

$$y(t) = x(t) \times s(t) \tag{10.1}$$

where

$$x(t) = A_0 \cos(\omega_0 t) \tag{10.2}$$

$$s(t) = rect_a(t) = u(t+a) - u(t-a) = \tag{10.3}$$

$$\begin{pmatrix} 1 & -a \leq t \leq a \\ 0 & Otherwise \end{pmatrix}$$

Since the two signals are multiplied in time domain, their frequency response will be convolved in frequency domain.

$$\mathcal{F}[y(t)] = \mathcal{F}[x(t)] * \mathcal{F}[s(t)] \tag{10.4}$$

$$\mathcal{F}[x(t)] = \frac{\pi A_0}{2}[\delta(\omega - \omega_0) + \delta(\omega + \omega_0)] \tag{10.5}$$

$$\mathcal{F}[s(t)] = \mathcal{F}[rect_a(t)] = \mathcal{F}[u(t+a)] - \mathcal{F}[u(t-a)] \tag{10.6}$$

$$\begin{aligned} &= \frac{1}{j\omega}e^{ja\omega} - \frac{1}{j\omega}e^{-ja\omega} \\ &= \frac{2}{\omega}\frac{e^{ja\omega} - e^{-ja\omega}}{2j} \\ &= \frac{2}{\omega}\sin(a\omega) \end{aligned}$$

So the zero bandwidth for the baseband pulse will be:

$$\sin(a\omega) = 0 \tag{10.7}$$

$$a\omega = n\pi \tag{10.8}$$

$$f = n\frac{1}{2a} \quad n = \pm 1, \pm 2, \ldots \tag{10.9}$$

so the baseband zero bandwidth of the pulse will be $\frac{1}{2a}$

$$Baseband\ Zero\ BW = \frac{1}{2a} = \frac{1}{T} \tag{10.10}$$

where T is the pulse width.

Since the pulse in convolved with $\cos(\omega_0 t)$, then the frequency spectrum will occupy frequencies around ω_0. This means that the zero-zero bandwidth requirement for the carrier-modulated pulse will be:

$$Zero - Zero\ BW = \frac{1}{a} = \frac{2}{T} \tag{10.11}$$

where T is the pulse width.

If the pulse s(t) has a time delay of t_0, then its fourier transform will have an additional phase shift of $e^{-j\omega t_0}$, so it will not change our calculation for the bandwidth requirement of the pulsed carrier signal.

$$\mathcal{F}[s(t - t_0)] = e^{-j\omega t_0}\mathcal{F}[s(t)] \tag{10.12}$$

If we have a pulse width of 40ps, then the baseband bandwidth requirement for such system is 25GHz (10.10) and the RF zero-zero bandwidth requirement is 50GHz (10.11).

Since in real-circuit implementation, the pulse shape won't be as sharp as a rectangle, the bandwidth requirement of the system will be reduced and what is shown here is the worst case scenario. Based on what was shown above, the Fourier transform result of this switching functionality will occupy the spectrum around the center frequency. Thus, a system with flat gain and flat group delay variation is required for minimal degradation of the pulsed signal.

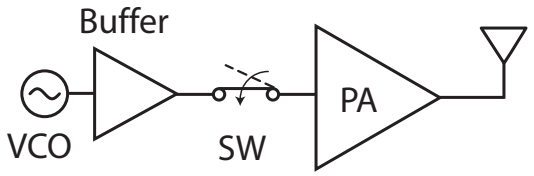


Figure 10.3: Switching before the power amplifier

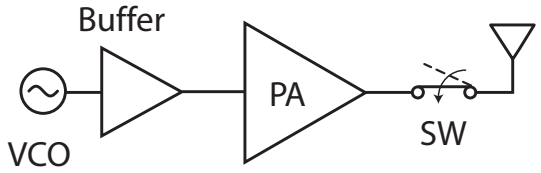


Figure 10.4: Switching after the power amplifier

10.1.1 Switch Location in Transmitter Architecture

For generating a carrier modulated pulse signal, the switch should be placed somewhere on the transmitter path. In this section, we will review the trade-offs on the location of the switch in the transmitter path. The switch can be placed before the power amplifier Fig. 10.3, after the power amplifier Fig. 10.4 or inside the power amplifier Fig. 10.5.

If we place the switch before the power amplifier (Fig. 10.3), the PA has to be

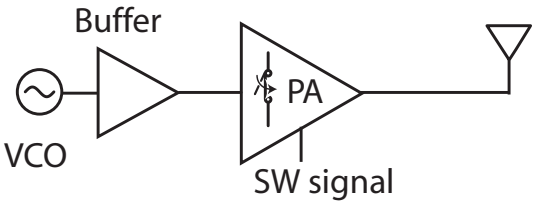


Figure 10.5: Switching inside the power amplifier

wideband for handling a narrow pulse. As it was shown in Eqn. 10.11, a narrow pulse requires a wide bandwidth. In this configuration, for a 40ps pulse, the PA has to offer (50GHz bandwidth zero to zero). Usually designing this PA has to be in distributed fashion (DA). DAs in general don't provide enough power gain while providing high-output power. Also, since the carrier frequency is 90GHz for our system, it would be very difficult to maintain flat group delay across such high bandwidth around 90GHz. For frequencies close to the DA upper corner frequency, the group delay variation increases considerably.

If we place the switch after the PA (Fig. 10.4), the PA can be designed narrow-band since it only has to deal with continuous LO signal from VCO. However, the switch loss will affect the maximum output power of the PA. Also, since the switch will be designed using active components, it may not handle the big voltage swing of power amplifier output.

If the switch is embedded inside the PA, (Fig. 10.5) only the circuitry that comes after the PA has to be wideband and the switch loss won't affect the maximum output power. In our design for the switched PA, we have embedded the switches inside the second stage of the PA and the switching operation was done in the current mode. The switch architecture will be discussed in the coming sections.

10.2 Transformer-Coupled 90 GHz Switched Power Amplifier

The schematic of the pulsed-based power amplifier is shown if Fig. 10.6. Since we are using a process with high f_T of 230GHz, switching is done in the current mode by applying a control voltage signal to the base of the cascode transistors in the switching stage.

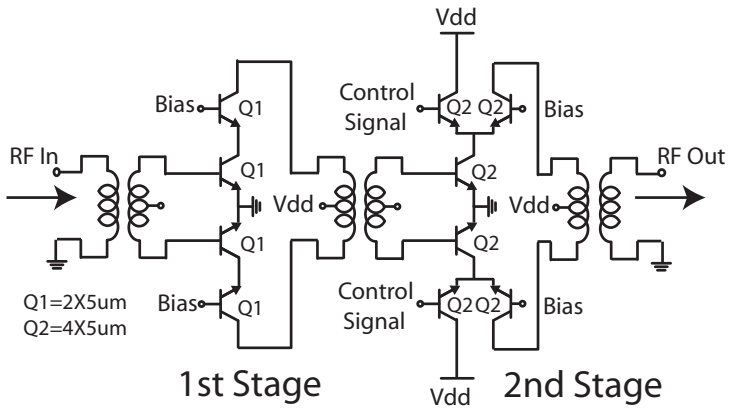


Figure 10.6: Circuit level schematic of the switched PA in pulsed transmitter.

In ON mode, the RF signal is directed toward the output antenna as shown in Fig. 10.7 and in OFF mode, the current is diverted away from the antenna toward the dummy path as shown in Fig. 10.8. The dummy path is bypassed to ground at its output to minimize the unwanted voltage swing.

In the following sections, design challenges and different aspects of the switched power amplifier will be investigated.

10.2.1 Switching Stage Driver Requirement

In order to realize a carrier modulated pulsed signal in the switched PA, the RF signal is gated by means of directing 90GHz RF current signal towards or away from the output. This switching operation happens by generating a narrow pulse as control signal and applying it to the base of the switching stage transistors.

Here the pulse-control implementation and constraints on the driver stage of the switching stage will be discussed.

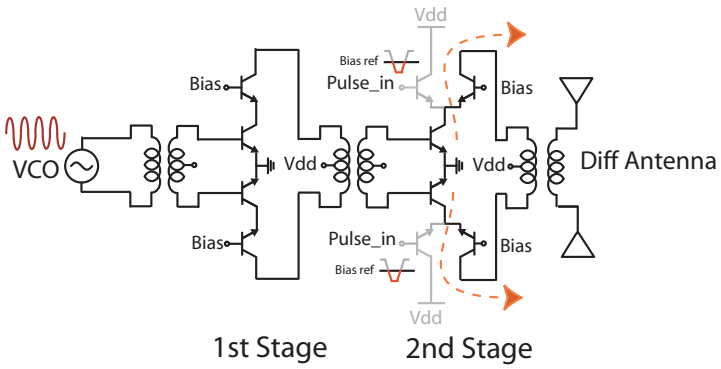


Figure 10.7: Switched PA in ON mode.

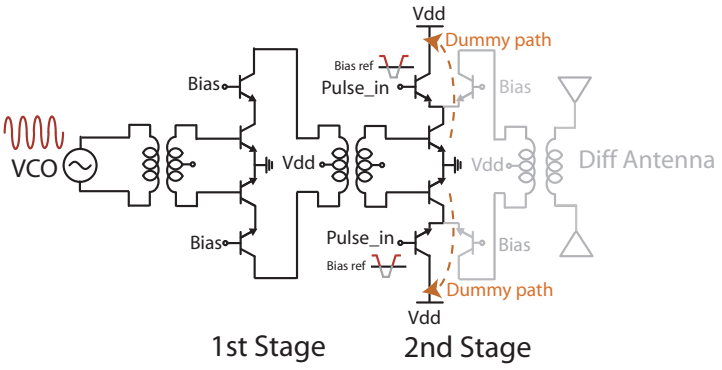


Figure 10.8: Switched PA in OFF mode.

For generating the narrow pulse, a low-frequency clock signal is delayed by the time amount equal to the desired pulse width and then the original signal and its delayed version go though an AND gate to generate the pulse. This pulse is sharpened through several stages of CML driver stages to finally drive the base of the switching transistors in the PA. The last stage of this chain has to drive a huge load at the base of the switching transistors. The input capacitance looking into the base of this switching stage in our design is about 200fF. In order to get a pulse rise and fall time within 20ps, we investigate the slew rate of the switching stage as well as RC time constant of the switching circuit to see which one will become the limiting factor.

Fig. 10.9 shows the amount of voltage swing that is required to completely divert the current from one side of the differential pair to the other. As can be seen for better than 40dB difference between ON and OFF mode, we need a voltage swing of 450mV. If we apply the control pulse to one side of the differential pair, we need to generate the full 0.45V voltage swing there. A better alternative would be to generate the control pulse differentially and apply the differential control pulse to the two bases of the switching stage then we need a peak-to-peak voltage swing of 0.225V on each end, which will be easier to generate (considering the huge capacitance that the driver has to drive at the base of the switching stage nodes).

However, in this work, we have generated the required swing only on one side of the differential pair and fixed the DC level on the other side. Let's say we would like to generate 0.6V swing (adding margin to the above required value of 0.45V). The main path cascode base voltage is biased at 2.4V. The dummy path cascode base voltage will have

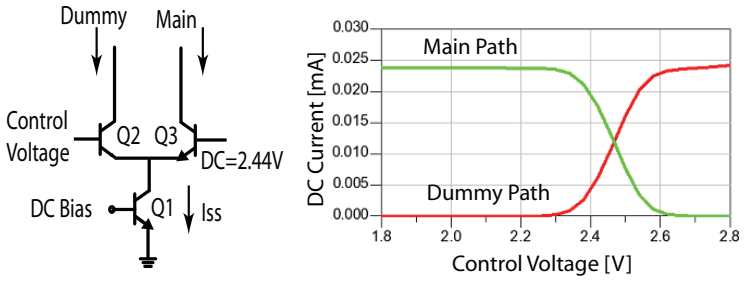


Figure 10.9: Current in main path and dummy path as a function of the control voltage.

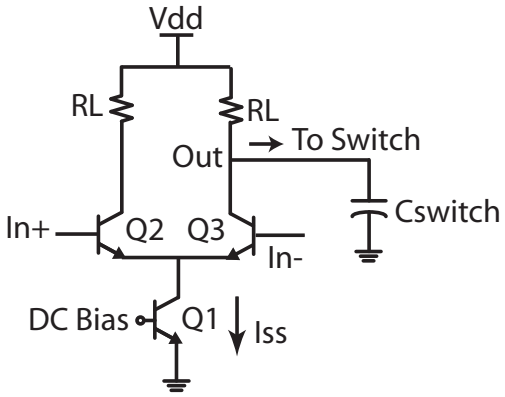


Figure 10.10: Schematic of the last stage of the switch driver.

2.7V in PA OFF mode and 2.1V in PA ON mode.

We will analyze the design of the last stage of the driver here. The simplified driver schematic is shown in Fig. 10.10. The drive stage is a fully differential common emitter with tail current source. The load of this differential stage is passive resistor connected to the power supply. This stage has to drive a load of 200fF of the switching stage.

Considering the slew rate limited scenario in the driver stage, we can calculate the amount of required DC current I_{ss} in this stage. When the control pulse coming from the

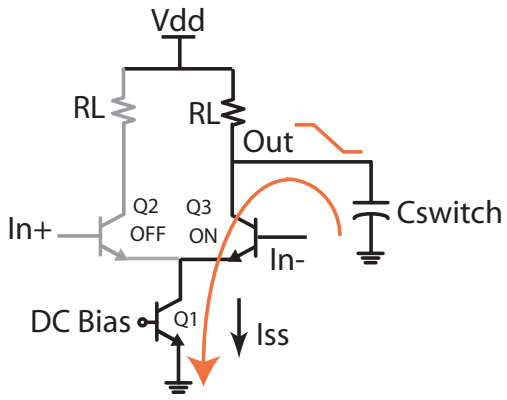


Figure 10.11: Current direction in falling edge of the pulse control signal.

driver stage at the output node is in the falling mode (generating falling ramp), the circuit will be slew rate limited. This scenario is shown in Fig. 10.11. The voltage swing needs to be 0.6V based on previous calculations. Equation. 10.13 shows the slew rate dependence on current and capacitance.

$$Slew\ Rate = \frac{I_{ss}}{C_T} \tag{10.13}$$

I_{ss} is the total dc current of the current source and C_T is the total capacitance at the driver output. C_T consists of the load capacitance of the switching stage ($C_{switch} = 200fF$) plus the portion of parasitic capacitance at the collector node of the driver stage. For simplicity, let's assume that C_T and is dominated by the load capacitance at the base of the switches. ($C_T \approx C_{switch} = 200fF$)

Since slew rate is the rate of voltage change in a circuit, Eqn. 10.13 could be written as Eqn. 10.14

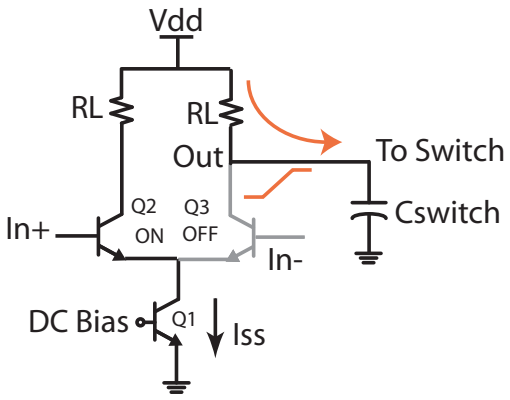


Figure 10.12: Current direction in rising edge of the pulse control signal.

$$Slew\ Rate = \frac{\Delta v}{\Delta t} = \frac{I_{ss}}{C_{switch}} \tag{10.14}$$

where Δv is the voltage swing and Δt is the time required for the voltage swing to happen. If we want to have a pulse falling time of 20ps for 0.6V voltage swing and 200fF load capacitance, the required dc current in the driver stage will be:

$$I = \frac{\Delta v \cdot C_{switch}}{\Delta t} = 6mA \tag{10.15}$$

which is acceptable and within our budget.

On the rising edge of the pulse control signal at output node (generating rising ramp), transistor Q_3 is OFF and the C_{switch} charges through the load resistance of the driver stage. This scenario is shown in Fig. 10.12. Charging capacitor time constant is:

$$\tau = R_L \times C_{switch} \tag{10.16}$$

where R_L is the load resistance and C_{switch} is the total capacitance at the input of the switching stage (200fF). The time required for the rising edge of the pulse will be

$$t \simeq 4\tau \tag{10.17}$$

In order to generate 0.6V voltage swing with 6mA current, we need R_L of 100Ω so the rising time of the pulse will be:

$$t \simeq 4\tau = 4 \times 100 \times 200f = 40ps \tag{10.18}$$

Since this is the limiting factor we can increase the dc current by a factor of two and reduce the R_L by half to keep the overall voltage swing requirement intact. In this case, the dc current consumption will be 12mA and the rising time of the pulse will be 20ps. Using the differential architecture, we would be able to reduce the dc current consumption by half since we only had to generate half of the voltage swing on each of the driver outputs. So in summary, a 40ps pulse could be realized with this switch driver.

The circuitry that can generate the narrow pulse for the drive stage is discussed in [60].

10.2.2 Stability of the Switching Stage

Since we are applying the control switching pulse to the base of the cascode transistors, stability of this node has to be carefully investigated. If the circuit has some potential instability at some frequencies, especially switching operation and applying the control pulse to the base of the cascode can lead to oscillation.

In order to analyze the stability of the base of the cascode, we can write the input impedance at that node and find its real and imaginary part. The simplified cascode model

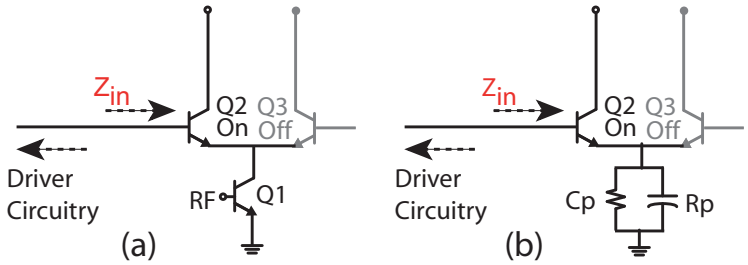


Figure 10.13: Simplified half circuit model for the impedance looking into the base of the cascode transistor, g_m stage replaced with lumped components

used in this analysis is shown in Fig. 10.13. Transistor Q_1 is replaced with capacitor C_p in parallel with R_p. Eqn. 10.19 shows the analytical input impedance seen at the base of the cascode device:

$$Z_{in} = \frac{(C_p + C_\pi)j\omega + (g_\pi + g_m)}{g_\pi C_p j\omega - C_p C_\pi \omega^2} \tag{10.19}$$

in which it is assumed that $\frac{1}{C_p s} \ll R_p$ for the bipolar device at the frequency range of interest.

The real part of Eqn. 10.19 is shown in Eq. 10.20:

$$R_{in} = \frac{C_p \omega^2 (g_\pi C_p - g_m C_\pi)}{(C_p C_\pi \omega^2)^2 + (g_\pi C_p \omega)^2} \tag{10.20}$$

So for mid-band frequencies, the real part of input impedance can become negative if

$$g_\pi C_p < g_m C_\pi \tag{10.21}$$

The driver circuitry will add some parasitic inductance to the base of the cascode transistors during the layout routing. This parasitic inductance can resonate with the overall capacitance at the base of the cascode. Since the real part of the impedance can

be negative if Condition 10.21 is satisfied, the circuit can potentially oscillate. Thus, we have to make sure this resonance happens beyond the frequencies that the device has any gain. To mitigate this problem, the last stage of the driver circuitry can be laid out as close as possible to the base of the cascode transistors. This will effectively reduce the parasitic inductance added by layout routing. Another method to mitigate this problem is adding additional resistance to the base of the cascode transistors. Even though this approach may increase the pulse rising time and decrease the gain of the switching stage, it may be necessary to guarantee safe and oscillation-free operation at the face of process variation and modeling inaccuracy.

In our design, even though the real part of the input impedance at the base of the cascode is positive for all the frequencies, however for extra safety and avoiding any oscillation possibility, $10 - 20\Omega$ could be added in series to this node with negligible degradation to pulse rise time and PA performance.

10.2.3 Output Stage Ringing

In this section, we will analyze the system on the falling edge of the pulse to see if the system exhibits some ringing behavior. Since the switches are placed in the output stage, we will model this staging for ringing analysis. Any kind of ringing at the output stage after the falling edge of the pulse can effectively limit the dynamic range of the system and is undesirable. Fig. 10.14 shows the small signal model of the output stage. For simplicity, the falling edge of the pulse is assumed to be sharp enough to be estimated by a step signal. Since the output pulse is generated in current mode, the input source in this analysis is a current source. C_{out} and R_{out} are device parasitic output capacitance and resistance. L_p

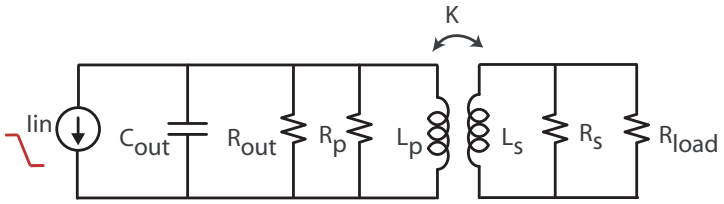


Figure 10.14: Simplified small signal model for the PA output stage

and L_s are inductances of the primary and secondary windings. R_p and R_s are parasitic resistors associated with the primary and secondary windings due to their finite quality factor Q. R_{load} is the output load, which is 50Ω in this case. Winding parasitic parallel resistance can be estimated by the following equation:

$$R_p = L_p \cdot \omega \cdot Q \tag{10.22}$$

$$\omega = 2 \cdot \pi \cdot f \tag{10.23}$$

where f is the frequency of operation and Q is the winding quality factor.

For simplifying the equations, let's assume that the interwinding capacitance of the transformer is negligible. We transfer the load from the secondary to the primary, which is shown in Fig. 10.15.

$$n = K\sqrt{\frac{L_s}{L_p}} \tag{10.24}$$

$$R_{L_{eq}} = \frac{R_L}{n^2} \tag{10.25}$$

Since R_{out} is the output resistance of bipolar cascode device, it's considerably bigger than

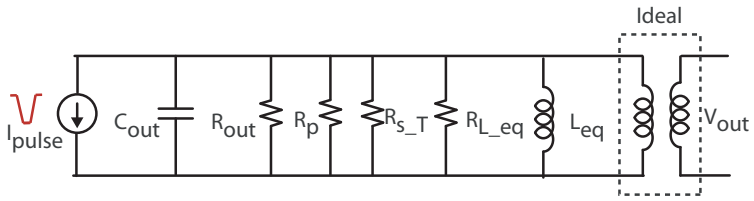


Figure 10.15: Simplified small signal model for the PA output stage with components transferred to the primary.

the rest of the parallel resistors on the primary side and its effect becomes negligible. Also, since the balun Q factor is in the range of 20 at 90GHz and the balun primary and secondary inductance is about 100pH so the R_p and R_s are about 1200Ω from Eqn 10.22. This will also be considerably bigger than the R_{Leq} and becomes negligible.

$$R_{Leq} \approx R_{Leq} \parallel R_{out} \parallel R_p \parallel R_{s_T} \tag{10.26}$$

Since L_1 and L_2 are almost equal due to the overlaid structure of the balun and K factor is in the range of 0.7 to 0.8, then R_{Leq} will be:

$$R_{Leq} = \frac{R_L}{n^2} \simeq \frac{50}{0.8^2 \times 1} \simeq 78\Omega \tag{10.27}$$

The balun size is chosen in such a way that its effective inductance at the primary is resonating with C_{out} at carrier frequency 94GHz.

$$L_{eq} \cdot C_{out} \cdot \omega^2 = 1 \tag{10.28}$$

$$\omega = 2\pi \times 90 \times 10^9 \tag{10.29}$$

The simplified model for the primary side of output stage will be (Fig. 10.16).

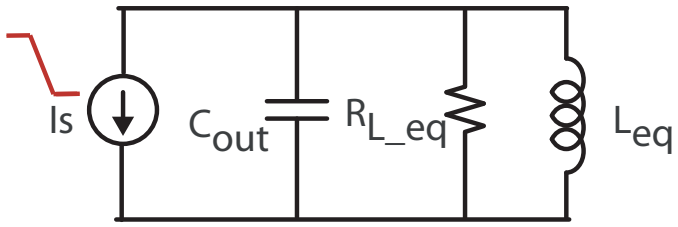


Figure 10.16: Simplified small signal model for the primary side as a second order system.

Here, assuming the interwinding capacitance is small between primary and secondary windings, on the primary side of the transformer we can assume a second order system with step input. The response of this system to the step input is shown below:

$$V(s) = I_s(\frac{1}{R_{Leq}} + \frac{1}{L_{eq}s} + C_{out}s) \tag{10.30}$$

$$V(s) = \frac{\frac{1}{C_{out}}}{\frac{1}{L_{eq}C_{out}} + \frac{1}{R_{Leq}C_{out}s} + s^2} \tag{10.31}$$

The general response of the second order system to the step input is shown below:

$$G(s) = \frac{K\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{10.32}$$

in which ω_n is the natural frequency of the system and ξ is the damping factor.

$$\begin{pmatrix} \xi > 1 & overdamped \\ \xi = 1 & critically\ damped \\ \xi < 1 & underdamped \end{pmatrix}$$

Comparing Eqn. 10.31 with Eq. 10.32 we will have:

$$\omega_n = \frac{1}{\sqrt{L_{eq}C_{out}}} \tag{10.33}$$

$$\xi = \frac{1}{2R_{Leq}}\sqrt{\frac{L_{eq}}{C_{out}}} \tag{10.34}$$

In our designs, the above values are:

$$\omega_n = \frac{1}{\sqrt{L_{eq}C_{out}}} = 2\pi \times 90 \times 10^9 \tag{10.35}$$

$$\xi = \frac{1}{2R_{Leq}}\sqrt{\frac{L_{eq}}{C_{out}}} = 0.36 \tag{10.36}$$

Since $\xi < 1$ the response is underdamped. This means the system will ring before dying out. The resonance frequency for the under-damped system is:

$$\omega_r = \omega_n\sqrt{1-\xi^2} \tag{10.37}$$

which in this design will be:

$$\omega_r = 2\pi \times 90 \times 10^9 * 0.87 \approx 2\pi \times 78 \times 10^9 \tag{10.38}$$

The settling time for a second order underdamped system responding to an step input is:

$$T_s = -\frac{\ln(K)}{\xi\omega_n} \tag{10.39}$$

where K is the tolerance fraction of the final settled value relative to the original value. So the settling time for the above system settling to 2% of original value will be:

$$T_s = -\frac{\ln(0.02)}{\xi\omega_n} \approx -\frac{3.9}{\xi\omega_n} \approx 18.3ps \tag{10.40}$$

So 18.3ps after the switch turns off, the signal level at the output node will be 34dB below its original value. Depending on the required dynamic range for the system, the requirement on settling time may change.

As it could be seen from Eq. 10.40, in order to keep the ringing time small, we would prefer to have smaller R_{eq}. L_{eq} is usually constrained to the tank resonance frequency. Since the power amplifier usually prefers smaller load values to deliver maximum output power, this requirement will be in line with the requirement on small ringing time.

10.2.4 Output Stage Pulse Reflection

In a pulse-based system, the distance of the target could be determined by the time of flight. Time of flight is the time it takes for the pulse to reach the target and come back. If the generated pulse in the transmitter has some reflections, then we can end up with a scenario that we transmit several pulses by each pulse command instead of sending only one clean pulse. This will make the detection in the receiver difficult since the received signal can come from actual pulse or its reflections hitting targets at different locations. This makes the system dynamic range requirement more challenging. To avoid pulse reflection, the PA should be matched to antenna input. Since the antenna is implemented on-chip, its input impedance does not have to be the general 50Ω impedance that is generally used in RF modular design approach. However, since the on-chip antenna in our design was a folded slot antenna with input impedance of 50Ω, a modified version of this PA was also designed with matched output impedance to 50Ω.(Fig. 10.18)

10.2.5 Output Stage Leakage

In a pulsed-based system, we would like to have maximum ratio between ON and OFF mode. ON mode is the time that the transmitter is transmitting the pulse. OFF mode is the time that the pulse is not transmitted to the antenna. In OFF mode, the RF signal

can be directed toward a dummy path or the transmitter can stop generating the pulse by turning itself off. When the pulse is not transmitted, we do not want to send any residual carrier signal since that signal directly reduces the overall system dynamic range and reduces the range of target detection. But unfortunately, there is always some residual leakage of the carrier to the antenna. Taking advantage of a high f_T process in this design, we generate the pulse in the current mode and use a differential pair Gilbert cell-type structure for pulse generation. As shown previously in Fig. 10.9, the current division between main path and dummy path is a function of control voltage. For a simulated rejection ration of 40dB, we need a voltage swing of 0.45V at the base of the cascode switching transistors.

To reduce the leakage, we are assuming that the dummy path is bypassed adequately to directly short circuit the dummy path output to ground. Also, the bypass capacitors on the base of the cascode transistors on the main path are big enough to prevent carrier signal from leaking to the output through the main path capacitances C_{BE} and C_{BC}. If we assume that the main path transistors are completely off, then C_{BE} of that transistor will be significantly reduced since base to collector capacitance, C_{BE} is a strong function of the g_m of the device.

$$C_{BE} = g_m \cdot \tau_f + 2C_{BE_0} \tag{10.41}$$

The small signal half-circuit schematic of the switching stage for leakage scenario is shown in Fig. 10.17 and the equation governing the output leakage is shown below.

$$OFF\ mode\ leakage = I_{RF} \times \frac{1}{g_{m_{dummy}}} \times \frac{Z_L}{Z_L \cdot C_{ce} \cdot s + 1} \tag{10.42}$$

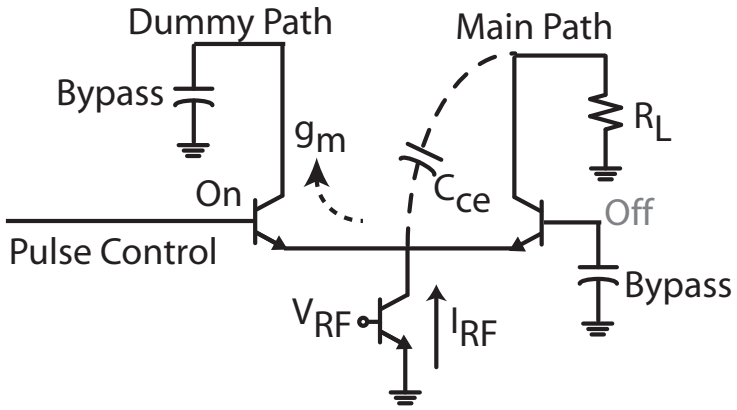


Figure 10.17: Small signal half circuit schematic of the switching stage and carrier leakage.

where $g_{m_{dummy}}$ is the g_m of the transistor on the dummy path. Since the output tank is tuned to carrier frequency and the leakage happens at carrier frequency we will have :

$$off\ mode\ leakage = I_{RF} \times \frac{1}{g_{m_{dummy}}} \times \frac{R_L}{R_L \cdot C_{ce} \cdot s + 1} \tag{10.43}$$

where R_L is the load impedance at resonance frequency and C_{ce} is the collector to emitter capacitance.

Since in OFF mode, the main path will be slightly on, we will have some small $g_{m_{main}}$, which translates into more carrier leakage signal at the output. To further reduce the leakage signal, we can stack more devices on the main path. The switched PA with stacked transistors in the main path is shown in Fig. 10.18. In the shown schematic, the pulse control signal is used differentially and a resistor is added to the output stage for output-matching purposes. By stacking more transistors in the main path, we are sacrificing output power for more isolation. By stacking more devices in the output, we will have less voltage headroom. Less voltage headroom translates to lower-delivered output power.

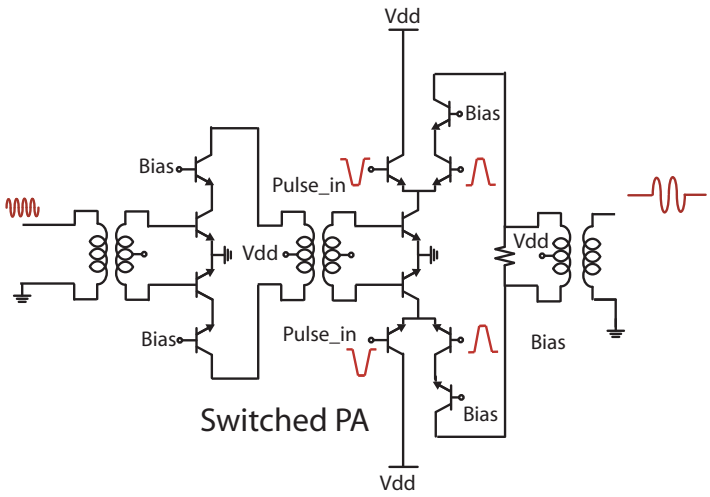


Figure 10.18: Schematic of the switched power amplifier with stacked transistors in the main path.

10.3 Measurement Setup of the Pulse Power Amplifier

The measurement setup of the Pulsed PA is shown in Fig. 10.19 and Fig. 10.20. The DUT consists of pulsed power amplifier with the integrated VCO and antenna. Fig. 10.19 shows the DUT with internal pulse control mechanism using high-speed timing circuitry and Fig. 10.20 shows the DUT without integrated high-speed timing circuitry. In this case, the pulse control signal is brought to the chip using LO port. Since the antenna is integrated on the die, no RF signal is routed to the chip except the 750MHz clock signal for the high-speed circuitry of Fig. 10.19 or LO signal for the pulse control of Fig. 10.20. 90GHz signal coming from the VNA is optional if we want to bypass the VCO and its buffer and drive the PA directly with external 90GHz RF signal. Since the main functionality of the system can be measured without the need for any RF high-frequency signal, the chip is mounted on a two-layer PCB board using COB technology. Using chip onboard, the

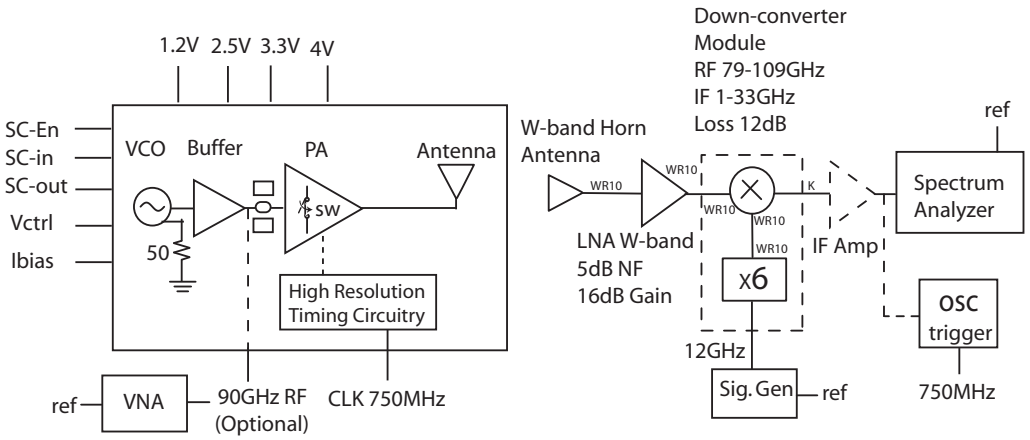


Figure 10.19: Block level schematic of the measurement setup of pulsed PA with internal pulse control.

chip could be tested without the electromagnetic field interference of the RF probes on the antenna pattern of the on-chip antenna. Fig. 10.21 shows the measurement board with the chip area highlighted. To analyze the transmitted signal from the transmitter chip, we used W-band horn antenna with about 20dBi antenna gain in the external receiver. The received signal goes through an external W-band low noise amplifier (LNA) with 5dB noise figure and 16dB small signal gain and then is down-converted to the IF. The IF frequency range coverage for the down-converter is about 1GHz to 30GHz. The LO signal for the external down-converter was provided through an external multiplier ($\times 6$). The IF output signal from the receiver could be either connected to an spectrum analyzer for spectrum analysis or could be connected to an oscilloscope for time-domain analysis.

The picture of the measurement setup of the pulsed TX is shown in Fig. 10.22.

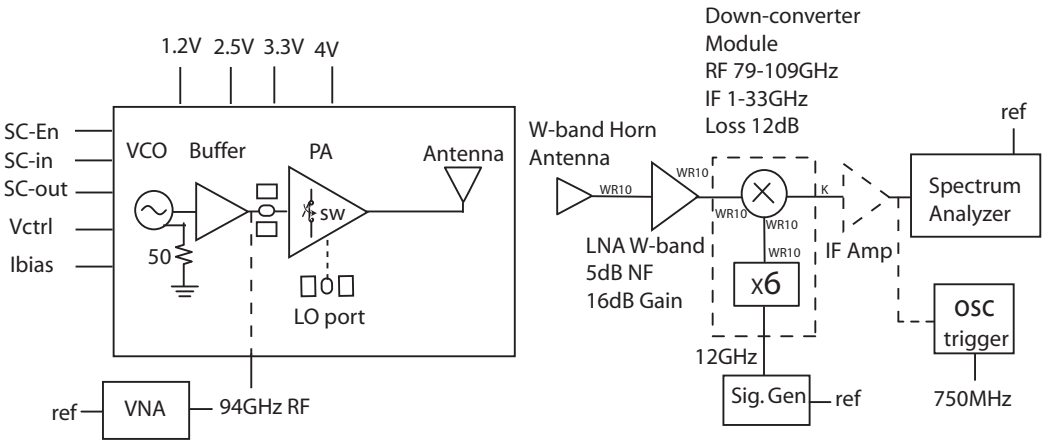


Figure 10.20: Block level schematic of the measurement setup of pulsed PA with external pulse control.

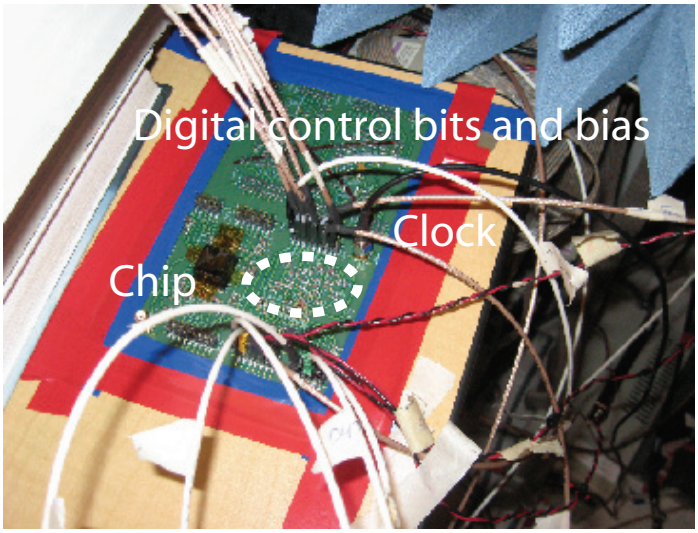


Figure 10.21: Chip on board measurement setup.

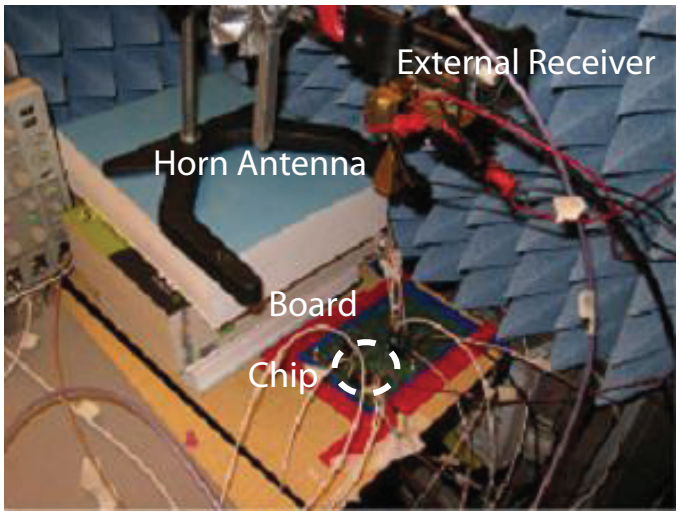


Figure 10.22: Picture of the pulsed transmitter measurement setup.

10.4 Measurement Results of the Pulsed PA/Pulsed TX

The switched PA is measured as part of a fully integrated 90GHz carrier time domain pulsed transmitter with on-chip antenna. This integration was done as a collaboration with the Berkeley Wireless Research Center T-Hz Ultra wideband Synthetic Imaging (TUSI) team.

Schematic of the transmitter with high-speed timing circuitry is shown in Fig. 10.23. This transmitter integrates a transformer-coupled power amplifier, Quadrature VCO, on-chip folded slot antenna and high-speed timing circuitry. The timing circuitry is used for several functions including pulse generation, pulse width control and selection of mode of operation. This transmitter can operate in several different modes. It can be used in PA-independent switching mode, antenna-independent switching mode or in hybrid switching mode. In hybrid switching mode, the output pulse is generated by mutual operation of PA

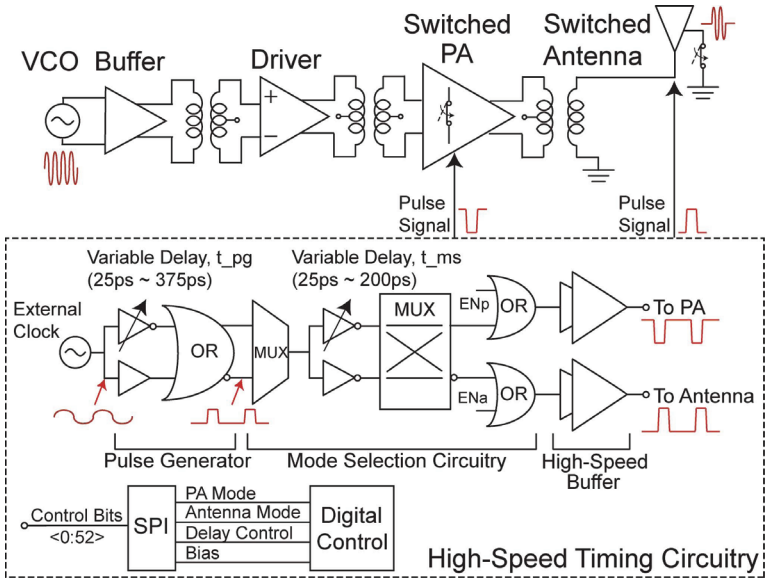


Figure 10.23: 90GHz Hybrid switching transmitter with integrated antenna. [60].

and antenna. Pulse generation circuitry is an OR gate with programmable inverter delay cells at one of its inputs. Variable delay is generated by using a bank of switched capacitors at the output of delay cells (inverters). Pulse repetition frequency (PRF) is determined by external 750MHz clock that drives both of the inputs of the OR gate in pulse-generation circuitry.

The details of the design of this transmitter is beyond the scope of this thesis. However, interested readers are encouraged to [60] for further discussions on the design of different blocks in this transmitter. In this section, we mostly mention measurement results that are directly related to the switched power amplifier, which is the work of the author.

The transmitter is realized in a $0.13\mu m$ SiGe BiCMOS process with ft=230GHz. Die photo of the Pulsed TX with integrated timing circuitry is shown in Fig. 10.24. The chip occupies a small footprint of $1mm \times 1.2mm$ (including on-chip antenna) while consum-

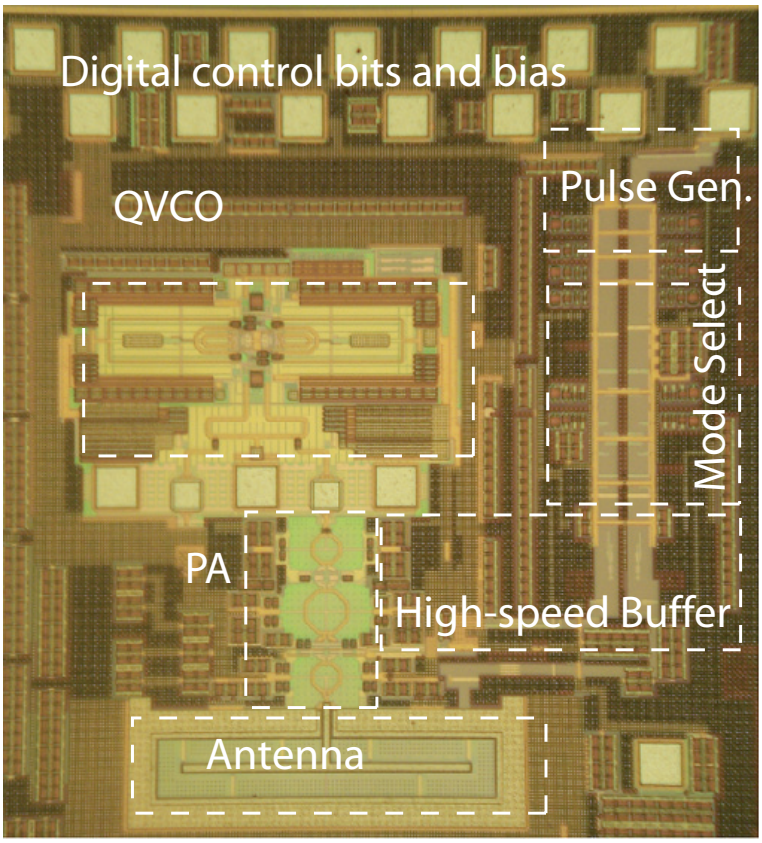


Figure 10.24: Die photo of pulsed TX with integrated timing circuitry.

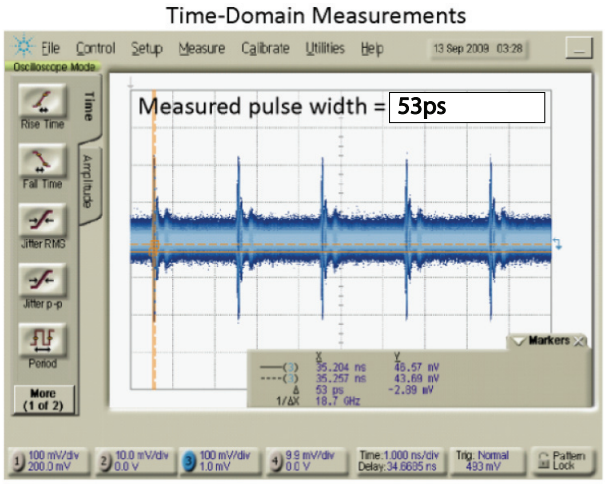


Figure 10.25: Time-domain pulse measurement in pulsed transmitter.

ing 700mW of power. There are several challenges in measuring an mm-wave chip, which generates extreme narrow pulses. Limited bandwidth of the external down-converter, noise floor of the oscilloscope and free running VCO on-chip all contribute to the measurement non-ideal setup condition. Time domain measurement result of the transmitter in independent PA switching mode is shown in Fig. 10.25. In this graph, the PA achieves a pulse width (50%-50%) of 53ps. Measurement spectrum of the switched PA generating a 115ps pulse is shown in Fig. 10.26.

Fig. 10.27 summarizes measured different pulse width in transmitter as a function of the control bits in timing control circuitry. As it could be seen from Fig. 10.27, pulse with down to 35ps (50%-%50) was measured which corresponds to $BW > 30GHz$.

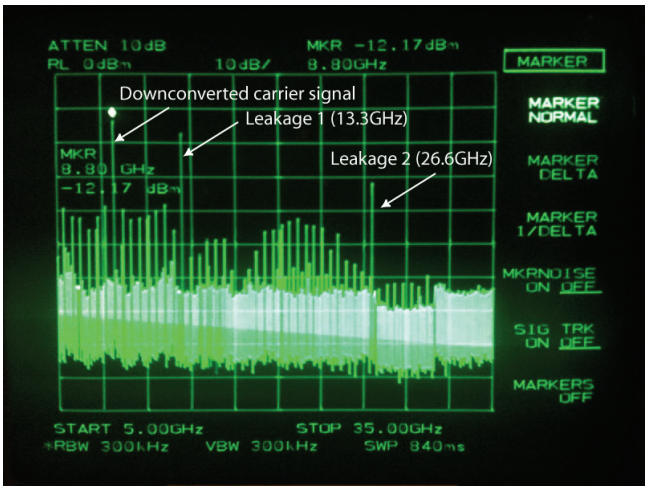


Figure 10.26: Spectrum of 115ps output pulse (external down-converter uses LO signal of 13.3GHz with a X6 multiplier factor).

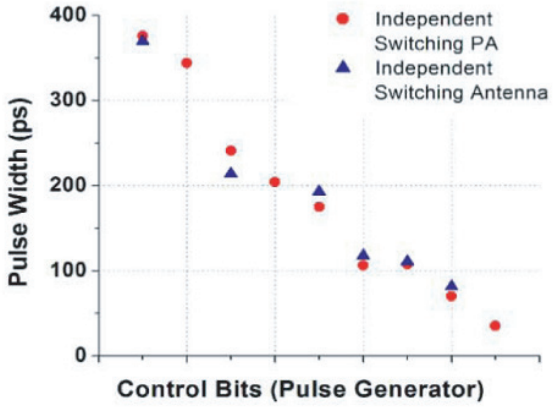


Figure 10.27: Measured several pulse width generation based on pulse generator control bits.

Chapter 11

Conclusion

Millimeter-wave circuits are expected to enter the realm of consumer electronics in the very near future. As there is an increasing demand in wireless content and data transmission, 60GHz band will continue to gain momentum and soon will be part of every portable device like cellular phone, PDA and digital camera. The mm-wave circuits will be also more available in car radars especially mainstream cars to increase the safety of the drivers and passengers and reduce the number of accidents. By technology scaling and reduction of transistor minimum feature sizes, the operation boundary of transistors will be increased. Electronic operation up to 200GHz is realized in today's advanced technologies and it is expected to go beyond 400GHz entering the THz region in the near future. This will further enable new and exciting applications in several fields such as in medicine. Materials can have certain signatures in THz region based on their ionic or molecular resonances which could be used for identifying material based on their chemical composition. Medical Sub-THz millimeter-wave imaging can help in medical screening and diagnosis. The contract

mechanism of mm-wave imaging is different from conventional imaging modalities and could be used as a complimentary assistance to the current imaging modalities like X-ray and MRI. Early breast cancer detection using non-ionizing electromagnetic radiations and non-invasive blood glucose monitoring are among the foreseeable applications of Sub-THz millimeter-wave imaging.

This dissertation has explored mm-wave band design using CMOS and SiGe Technologies. It addressed many of the challenges that are faced in the mm-wave band design. Issues related to the modeling of active and passive components for the mm-wave band along with circuit implementation of key building blocks of the mm-wave transceiver were discussed. Part 1 presented a very low power and low noise 60GHz receiver in 90nm CMOS digital process. Low noise, high gain and high gain tuning range were demonstrated with very low power consumption. These factors in unison made this front-end suitable for small footprint mobile devices such as cell phones, PDAs, or laptop computers. In chapter 1, potentials and applications of the 60GHz band were discussed. Chapter 2 discussed modeling methodologies of active and passive components for the mm-wave band to increase achievable performance of the mm-wave design in a power-constrained system. Chapter 3 discussed the system level link budget for a 60GHz wireless communication system. Details of the design of key building blocks of a 60GHz receiver were the topic of the following chapters. The first part of this thesis was concluded by measurement results of the 60GHz receiver prototype in 90nm CMOS technology. Accurate mm-wave device characterization resulted in a robust and predictable design. We have shown that mm-wave design can differ significantly when operating a device close to the transition frequency f_t. Furthermore,

the design of cascode amplifiers and Gilbert cell mixers requires careful considerations to maximize the gain and maintain stability over a wide frequency range. Several techniques were proposed in the design of low noise amplifier and down converting mixer to increase the performance of these blocks for the 60GHz band. Careful layout engineering and extensive electromagnetic co-simulation were used to realize the presented design. Considering the increasing demand for high data-rate wireless communication, realization of a phased-array 60GHz transceiver would be the next step for this project. A 60GHz phased-array transceiver can offer higher data-rate and more communication range. However, power consumption can be the challenging part in that system especially if it is to be deployed in a portable device.

Part 2, discussed the design of an ultra wide-band pulsed power amplifier for an imaging transmitter. During the chapters of this part, system level requirements of an imaging transmitter were developed and design considerations for a 90GHz transformer-coupled power amplifier in SiGe technologies were discussed. A prototype of a switched power amplifier in an integrated time-domain pulsed transmitter was presented at the end of this part. In this work, very narrow pulses with a very high carrier frequency were generated which can potentially increase the depth resolution and lateral resolution of the imaging transmitter. Details of the design of the switched power amplifier for an imaging system were discussed here. This work could be further improved by integrating the receiver part of the imaging system to build an ultra-wideband mm-wave imaging transceiver. In the end, to increase the system dynamic range, detection range and resolution, a timed-array transceiver has to be developed consisting of several on-chip imaging transceivers as well

as picosecond-range precision timing circuitry to synchronize the full array. This work was the beginning of an interesting and exciting path towards the realization of a portable low-cost mm-wave medical imaging device which can be widely used in ambulances, healthcare facilities and hospitals. The module is expected to enhance the performance of the current imaging modalities or even replace them for some specific medical imaging applications.

Research in the mm-wave band will follow the two following paths. On one path, the direction will go over reducing the power consumption of the mm-wave design to make it suitable for portable applications. Since portable devices like cell-phones are expected to continue offering more functionality from one generation to the next, It is extremely important to reduce the power consumption of the mm-wave portion of the chip to save battery life of the device and make it practical for the 60GHz integration. In this way, While taking advantage of the available wide bandwidth of the 60GHz band for establishing a multi-Gigabit per second wireless communication. To minimize the power consumption of the mm-wave chip, it is extremely important to fully characterize the active devices for the mm-wave band operation. Even though technology scaling will continue to enhance the performance of the active transistors for the 60GHz operation, accurate modeling of the devices will still be necessary for reducing the design overhead and lowering the overall power consumption. It should be also mentioned that dealing with a wide bandwidth baseband signal in a 60GHz chip could be quite challenging. There is definitely a need for innovation in this field to bring down the power consumption of the 60GHz front-end and baseband portions of the chip. The mm-wave power consumption of the chip will become more important if the 60GHz chip is used in phased-array configuration for increasing range

and data-rate. Smart division of the array elements between RF and baseband can lead to the optimum solution for the overall system in terms of power consumption and system performance. In the coming future, we should expect to see more phased-array architectures using deep sub-micron CMOS technologies operating in the 60GHz band.

On the next research direction, there will be a great emphasis on pushing the frequency boundaries of electronic circuitries using CMOS and SiGe technologies for commercialized applications. By going towards higher frequencies, new opportunities will rise and new applications will be envisioned. Taking advantage of these new potential high frequency applications requires extensive research and innovation in all levels of device modeling and circuit blocks and system architectures. New modeling methodologies has to be developed and new system trade-offs have to be investigated. For example, Sub-THz medical imaging is among these future potential applications. There has not been much research on microwave imaging of biological material above 30 GHz and this field is relatively unexplored. Realizing a sub-THz or THz medical imaging modality which is low-cost, portable and non-ionizing can lead to a breakthrough in the field of medical imaging and requires extensive research and innovation.

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