Capacitive Power Transfer

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by Mitchell Herman Kline

Research Project

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Approval for the Report and Comprehensive Examination:

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Abstract

The simplicity and low cost of capacitive interfaces makes them very attractive for wireless charging stations and galvanically isolated power supplies. Major benefits include low electromagnetic radiation and the amenability of combined power and data transfer over the same interface.

We present a capacitive power transfer circuit using series resonance that enables efficient high frequency, moderate voltage operation through soft-switching. An included analysis predicts fundamental limitations on the maximum achievable efficiency for a given amount of coupling capacitance and is used to find the optimum circuit component values and operating point.

A prototype capacitive charger achieves near 80% efficiency at 3.7 W with only 63 pF of coupling capacitance. An automatic tuning loop adjusts the frequency from 4.2 MHz down to 4 MHz to allow for 25% variation in the nominal coupling capacitance. The duty cycle is also automatically adjusted to maintain over 70% efficiency for light loads down to 0.3 W.

Simulation results from a galvanically isolated LED driver (work in progress) indicate that efficiencies over 90% at 12.6 W output power are possible using only 500 pF of capacitance. Regulation of LED current is accomplished by tuning the frequency of the series resonant circuit, eliminating the need for secondary-side current sense and regulation electronics.

1 Introduction

Contactless power transfer is gaining increasing attention for powering and charging portable devices including smart phones, cameras, and laptop computers. The predominant solution today uses an inductive [1, 2] interface between a charging station, acting as the transmitter, and a receiver, typically a portable device. Both the transmitter and receiver are fitted with electrical coils. When brought into physical proximity, power flows from the transmitter to the receiver. Here we examine an alternative approach that uses a capacitive, rather

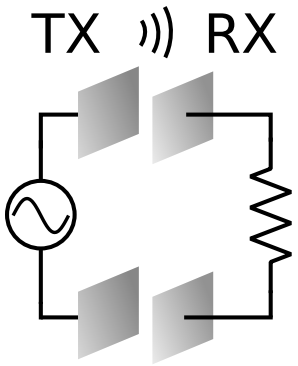

Figure 1: Power is transferred from an AC source to a load through capacitors formed by parallel plates on a transmitter and a receiver.

than inductive interface to deliver power—Fig. 1. In the capacitive interface the field is confined between conductive plates, alleviating the need for magnetic flux guiding and shielding components that add bulk and cost to inductive solutions [3].

The realizable amount of coupling capacitance is limited by the available area of the device, imposing a challenging design constraint on contactless power delivery. For example, the parallel plate capacitance across a 1/4 mm air gap is only $3.5\,\mathrm{pF/cm^2}$, limiting typical interface capacitance to a few tens of picofarads, and the required charging power is upwards of 2.5 W (USB-specification). Existing capacitive power transfer (CPT) solutions either use much larger capacitors [4] or are targeted at lower power applications, such as coupling of power and data between integrated circuits [5] or transmitting power and data to biosignal instrumentation systems [6,7]. To improve the performance of the reported results, we devote substantial effort into circuit design and optimization.

Contactless power transfer techniques are also applicable to galvanically isolated offline power supplies [8]. The traditional approach is to use a transformer, composed of coupled primary and secondary coils that share a magnetic core. Ideally, the signal applied to the primary coil, typically $120\,\mathrm{V_{rms}}$ across the hot and neutral conductors, appears at the secondary coil, scaled by the turns ratio of the transformer. The galvanic isolation property of the transformer is due to the rejection of common-mode signals, which are earth-referenced signals present on both hot and neutral input lines. Electrically, the body can be considered

as a load to earth ground, thus these common-mode signals are dangerous, and one should never directly touch either of the hot or neutral conductors. The transformer rejects these signals, i.e., the secondary side terminals of the transformer have a very high common-mode source impedance, which restricts the current that could, for instance, flow through your body to earth ground. The common-mode impedance is high enough that one terminal can be connected to earth potential (this would form a short circuit if the transformer were not present), which can be further connected to a metal shield which encloses the hazardous terminals. To emphasize, one should never touch the terminals of the secondary coil as there are still potentially dangerous voltages present.

Similarly, capacitors can be used for isolation, but the mechanism for the common-mode rejection is fundamentally different. The transformer rejects the common-mode signal simply because it does not lead to generation of flux in the core. In fact, an ideal transformer has infinite common-mode rejection. In practice, finite capacitive coupling from the primary to secondary leads to common-mode feedthrough. This statement implies that capacitive coupling does the opposite of what is desired: it causes common-mode feedthrough. But, the situation is not hopeless. The key is that the common-mode signal is typically limited to low frequencies—the line frequency and its harmonics. The impedance of a capacitor at low frequencies is very high, thus the common-mode current that can pass through the interface is limited. Therefore, capacitors can be used to give the isolation property, and power can be transferred at a much higher frequency. The amount of coupling capacitance is limited by the common-mode rejection requirement to no more than a few nanofarads.

The concept of high frequency power transfer has been in practice with magnetic solutions for decades; it allows reduction of the size and cost of the transformer. Here we argue that because of the poor scaling properties of magnetics, that at some power level, the cost and size of the galvanic isolation components are minimized with a capacitive, rather than inductive, interface.

Section 2 presents the analysis of the CPT circuit, including an efficiency expression that accounts for all relevant loss mechanisms. Section 3 discusses how to design a circuit given

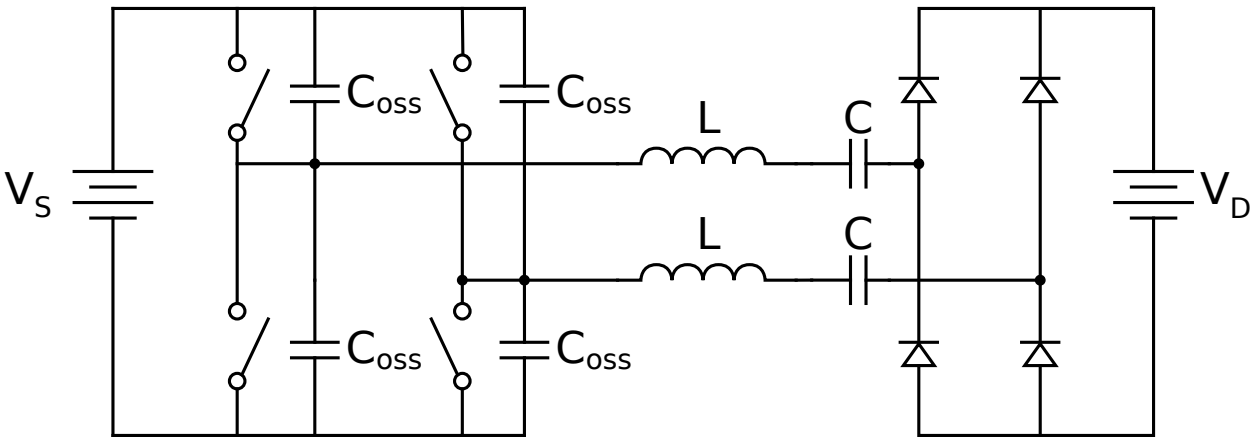

Figure 2: Schematic of a series resonant converter circuit constructed around the coupling capacitors C.

the results of the analysis. Section 4 presents experimental results from an example design suitable for USB-level power delivery in a smartphone sized package. Section 5 presents work in progress on a capacitively isolated LED driver.

2 Analysis

The analysis is based on a series resonant architecture, presented in Fig. 2. Power is transferred from V_S to V_D through the two coupling capacitors C. These two capacitors are in series, so the effective capacitance between transmitter and receiver is $C/2$. An H-bridge driver converts V_S into an AC voltage to enable current flow through the capacitors. Inductors L are placed in series with the coupling capacitance to enable soft-switching. A diode rectifier converts the AC voltage back to DC. A voltage source models the load, which is equivalent to a resistive load in parallel with a sufficiently large hold-up capacitor.

Similar architectures appear in [9] and [10] with the differences being unbalanced operation and use of an additional frequency selective tank. A differential driver reduces EMI by suppressing the common-mode signal on the receiver. Eliminating the additional tank permits dynamically tuning the frequency to adapt to a variable coupling capacitance.

The switches used in the H-bridge have three relevant parasitics: the on-resistance R_{on}, the drain capacitance C_{oss}, and the gate capacitance C_g. The technology-dependent parameter τ_{sw} is used to model the sizing trade-off between on-resistance and drain capacitance as $R_{on} = \tau_{sw}/C_{oss}$. If hard-switched, the parasitic C_{oss} capacitors cause $4C_{oss}V_S^2 f$ switching loss, where f is the operating frequency. This loss can be eliminated by operating the circuit in a zero voltage switching (ZVS) regime, where the inductor recovers the charge on the C_{oss} capacitors, and no current impulses are drawn through the switches. Similarly, the loss from driving the gates is $4C_g V_G^2 f$, where V_G is the gate drive voltage. In practical CPT designs for contactless charging, V_D is much greater than V_G, so the drain capacitance loss term dominates. The gate loss is not considered in the analysis for clarity, but it is not conceptually difficult to include.

The series resonant architecture has been extensively analyzed in [11–13]. The following analysis differs in that the coupling capacitance, C, is treated as the scarce parameter. The goal is to determine a circuit design that uses the available C as efficiently as possible. The input parameters are the output power, P_{out}, the source voltage, V_S, and the technology-dependent parameters Q and τ_{sw}. The analysis determines the relationship between the available coupling capacitance and the *maximum* achievable efficiency. From this, we can design a circuit that requires the least amount of coupling capacitance to achieve the efficiency η. The switch size parameter is captured by C_{oss}. It is convenient to require Q as an input, as it accurately models the inductor loss and is generally well-known for a particular inductor technology.

2.1 Efficiency

The efficiency of the converter considering the conduction losses only is given by

$$\eta = 1 - \underbrace{\frac{1}{2}\frac{||i_t||^2 R_S}{P_{out}}}_{\text{Conduction loss}}, \tag{1}$$

where $||i_t||$ is the magnitude of the tank current and R_S is the effective parasitic series resistance due to the inductor, capacitor, and switch. The tank current, i_t, is assumed to

be sinusoidal due to the frequency selectivity of the tank; thus, the standard definitions of magnitude and phase apply. The conduction loss is simply the multiplication of the RMS current squared by the total series resistance. Typically, the inductor will have a much lower Q than the capacitor, so R_S can be approximated by

$$R_S \approx 2\left(\underbrace{R_{on}}_{\text{switch}} + \underbrace{\frac{\omega L}{Q}}_{\text{inductor}}\right), \tag{2}$$

where $\omega = 2\pi f$ and the factor of 2 is from the series combination of switches and inductors. Considering only conduction losses for a fixed P_{out}, (1) and (2) indicate that we should try to minimize $||i_t||$, R_{on}, and the inductor equivalent series resistance (ESR). This can be done by using high voltages, increasing the size of the switch, and reducing the size of the inductor, respectively. However, high voltages and large switches (high C_{oss}) inevitably lead to high switching losses, which are proportional to $C_{oss}V_S^2$. These losses will be eliminated with ZVS, but this is enabled only when the inductor stores enough energy to commutate the switch output capacitance (a necessary but not sufficient condition). The inductor energy is given by $L||i_t||^2/2$, which indicates that the current and inductor size cannot be made arbitrarily small. In other words, we must tolerate some conduction loss in order to satisfy the ZVS condition. This analysis determines the minimum conduction loss that enables ZVS.

The current efficiency expression (1) is under-constrained, as it does not consider ZVS. In the following sections, we enforce the ZVS condition on this expression to expose optimum designs that use the available coupling capacitance as efficiently as possible.

2.2 Tank Current

The circuit in Fig. 3 is used to derive the tank current, i_t, using phasor analysis and neglecting harmonics. The voltage sources $v_s = V_S\angle 0$ and $v_d = V_D\angle\phi$ are applied to the series resonant circuit. In order to achieve ZVS, the impedance of the tank must be inductive, thus ϕ is negative and the operating frequency is above the resonant frequency. Since the (ideal) rectifier in Fig. 2 can only consume power, i_t is restricted to be in phase with v_d. This is

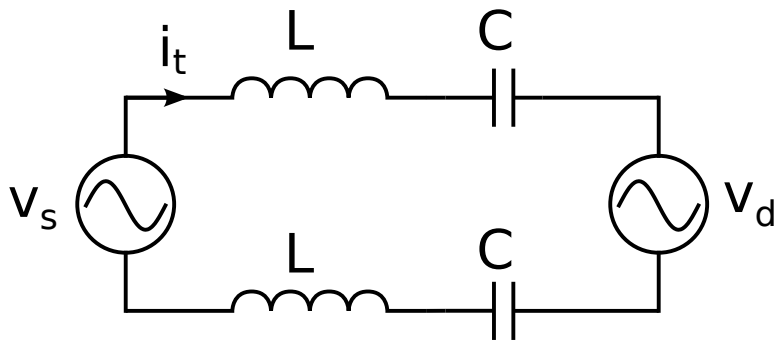

Figure 3: Circuit used for calculating the tank current as a function of the applied phasor voltages.

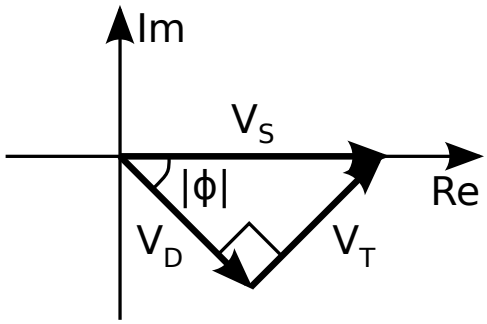

Figure 4: Phasor diagram used to calculate phase and amplitude of tank current, with V_T representing the total voltage drop across the reactive components.

equivalent to assuming that the diodes have no parasitic capacitance. The operation of the circuit can be best understood by a phasor diagram—Fig. 4. The voltage across the reactive components, $v_t = V_T \angle \phi_t$, is orthogonal to v_d because the current is in phase with v_d and the tank has an inductive impedance. Then the phase shift is given by

$$\phi = \angle \left(\frac{i_t}{v_s} \right) = - \arccos \left(\frac{V_D}{V_S} \right). \tag{3}$$

The magnitude of the current, including the effect of finite component Q, is given by

$$||i_t|| = \frac{Q\omega_0 C/2}{Q(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}) + 1} \sqrt{V_S^2 - V_D^2}, \tag{4}$$

where $\omega_0 = 1/\sqrt{LC}$ is the resonant frequency and ω is the applied frequency. For high

component (unloaded) Q, this can be approximated by

$$||i_t|| \approx \underbrace{\frac{\omega C/2}{\omega^2 LC - 1}}_{\text{conduction of tank}} \times \underbrace{\sqrt{V_S^2 - V_D^2}}_{\text{magnitude of tank voltage}} . \tag{5}$$

The factor of 2 is from the series combination of the two coupling capacitors. The current can also be expressed as a function of the output power. The DC output current is the average value of a rectified sine wave and is given by

$$I_{OUT} = 0.64||i_t||. \tag{6}$$

The output power is

$$P_{out} = I_{OUT} V_D = 0.64||i_t||V_D, \tag{7}$$

thus the tank current is

$$||i_t|| = \frac{P_{out}}{0.64 V_D}. \tag{8}$$

By setting (5) equal to (8), we can solve for the L that gives the appropriate output voltage with the specified output power,

$$L = \underbrace{\frac{1}{\omega^2 C}}_{\text{resonance}} \times \left(\underbrace{\frac{\omega C}{2}\sqrt{V_S^2 - V_D^2}\frac{0.64 V_D}{P_{out}}}_{\text{fraction above resonance}} + 1 \right), \tag{9}$$

which will later be substituted into (2) to eliminate the inductance from the efficiency expression. The factor marked *resonance* would be all that is required if $\omega = \omega_0$; in this case $V_S = V_D$. The additional term pushes the frequency above resonance, and depends on the capacitance, frequency, output power, and voltages.

2.3 Zero Voltage Switching Condition

Since the efficiency expression considers only conduction losses due to switch and inductor resistance, a ZVS condition should be enforced to validate the analysis. ZVS occurs when the tank current fully commutates the C_{oss} capacitors during the time when all switches in the H-bridge are open. This time interval is known as the dead-time of the driver. The

initial and desired final states of the C_{oss} capacitors are known; two start at V_S and must be discharged to zero volts, and two are initially at zero volts and must be charged to V_S.

Consider the C_{oss} capacitors initially charged to V_S; together they store

$$q_{sw} = 2C_{oss}V_S \tag{10}$$

charge. This is the amount of charge that the tank current must displace during the dead-time interval to satisfy ZVS. Since the magnitude of i_t is known, the maximum possible charge that the tank can remove from the capacitor can be calculated by integrating the portion of i_t corresponding to discharging C_{oss}. The time interval to be integrated is from the falling edge of the H-bridge output voltage to the zero crossing of the tank current. Immediately before this time interval, the H-bridge is still driving the output, so the tank current is sourced from V_S, not C_{oss}. After this time interval, the current changes direction, thus is flowing in a direction to charge, rather than discharge C_{oss}. Fig. 6 represents this graphically.

The time interval just described simply corresponds to the phase shift between the H-bridge output voltage and the tank current, which has already been calculated as ϕ above. Using a cosine reference for the phasor i_t,

$$i_t = ||i_t|| \cos(\omega t + \phi), \tag{11}$$

the integral that gives the average value of the current is

$$I_{avg} = -\frac{1}{\phi}\int_{\pi/2+\phi}^{\pi/2} ||i_t|| \cos\theta d\theta = -\frac{||i_t||}{\phi}(1-\cos\phi), \tag{12}$$

where ϕ is negative (current lags voltage), making the result positive. Multiplying by the integration time $-\phi/\omega$ gives

$$q_t = \frac{||i_t||}{\omega}(1-\cos\phi), \tag{13}$$

where q_t represents the maximum amount of charge that the tank can displace. The ZVS condition is then $q_t \geq q_{sw}$ or

$$\omega \leq \frac{||i_t||}{V_S 2C_{oss}}(1-\cos\phi). \tag{14}$$

Using (3) and (8), (14) can be refactored as

$$\omega \leq \frac{P_{out}}{0.64 V_D V_S 2 C_{oss}} (1 - \frac{V_D}{V_S}) = \omega_{max}. \tag{15}$$

This result predicts that there is a maximum frequency beyond which ZVS does not occur.

2.4 Maximum Efficiency

We now return to the efficiency expression and enforce the ZVS condition. The goal will be to maximize the efficiency for a given coupling capacitance, which is equivalent to minimizing the required capacitance for a given efficiency. Substituting (9) into (2) gives

$$R_S = 2 \left(\underbrace{R_{on}}_{\text{switch}} + \underbrace{\frac{1}{\omega C Q} \times \left(\frac{\omega C}{2} \sqrt{V_S^2 - V_D^2} \frac{0.64 V_D}{P_{out}} + 1 \right)}_{\text{inductor}} \right). \tag{16}$$

This can now be substituted into (1), giving

$$\eta = 1 - \frac{P_{out} R_{on}}{(0.64 V_D)^2} - \frac{1}{0.64 Q} \times \left(\frac{1}{2} \sqrt{\frac{V_S^2}{V_D^2} - 1} + \underbrace{\frac{P_{out}}{0.64 V_D^2 \omega C}}_{\text{enforce ZVS}} \right), \tag{17}$$

where (8) was used to eliminate $||i_t||$. Upon examination, we see that the far right term is minimized for large ω. The ZVS condition (15) places an upper bound on ω, so the logical choice is $\omega = \omega_{max}$. Substituting this into (17), the expression becomes

$$\eta = 1 - \underbrace{\frac{P_{out} \tau_{sw}}{(0.64 A_V V_S)^2 C_{oss}}}_{\text{switch}} - \underbrace{\frac{1}{0.64 Q} \times \left(\frac{1}{2} \sqrt{\frac{1}{A_V^2} - 1} + \frac{2 C_{oss}}{C} \frac{1}{A_V (1 - A_V)} \right)}_{\text{inductor}}, \tag{18}$$

where $A_V = V_D / V_S$ and the relationship $R_{on} = \tau_{sw} / C_{oss}$ was used. Note that C_{oss} is proportional to switch size. This efficiency expression is now representative of the global efficiency of the converter, as switching losses have been eliminated with ZVS. The next section discusses further optimization of this equation as well as practical design considerations.

3 Design

The expression (18) contains two loss terms. The first is due to the switch on-resistance and the second to the inductor ESR. Assume the goal is to maximize the efficiency for a given coupling capacitance, C. If only the first term is considered, the switch size (C_{oss}), V_S, and A_V should be as large as possible. If only the second term is considered, Q should be maximized, the switch size minimized, and there is an optimum value for A_V. Since the two loss terms predict opposite impacts of C_{oss}, both should be considered to find the optimum switch size. It is always desirable to choose a switch with low τ_{sw} and an inductor with high Q since this corresponds to a better switch or inductor, respectively. A high source voltage V_S is desirable to reduce conduction losses but is often limited by practical constraints such as safety or compatibility with available step-down converters. The following example design demonstrates the utility of this equation.

3.1 Example Design Process

A capacitive power transfer circuit is to be designed to meet USB-level power specifications, 2.5 W at 5 V. To meet these specifications, we first choose $V_S = 35\,\mathrm{V}$, $P_{out} = 4\,\mathrm{W}$, and $\tau_{sw} = 44\,\mathrm{ps}$. The choice of V_S is based on the decision to use a 60 V family of Siliconix switches as well as the convenience of a single-stage step-down to 5 V. P_{out} is chosen conservatively to allow for some inefficiency of this final step-down. The τ_{sw} parameter is representative of the same family of Siliconix switches.

Fig. 5 is a plot of the maximum achievable efficiency as a function of the available coupling capacitance. Several values of the unloaded Q are plotted to show the effect of the inductor loss. This plot was generated by substituting the above parameters into (18) and using numerical methods to find the maximum η at each C. This maximum η value corresponds to optimum values of A_V and switch size (C_{oss}).

An alternative way to interpret this plot is that a target efficiency corresponds to a

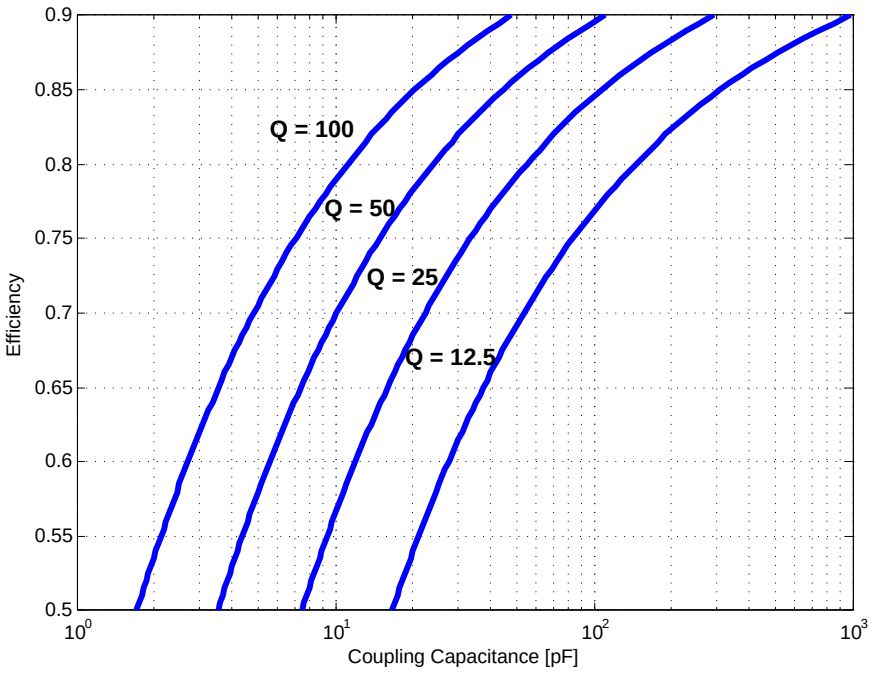

Figure 5: Maximum achievable efficiency vs. available capacitance for several unloaded Q values with $P_{out} = 4\,\mathrm{W}$, $V_S = 35\,\mathrm{V}$, and $\tau_{sw} = 44\,\mathrm{ps}$.

minimum required coupling capacitance. The capacitance must increase by nearly two orders of magnitude to increase the efficiency from 50% to 90%. Also, increasing the unloaded Q by a factor of 2 reduces the required capacitance by approximately half.

As an example, we chose an operating point corresponding to $\eta = 0.9$ and $Q = 40$. The minimum C is 147 pF, corresponding to A_V and C_{oss} (switch size) equal to 0.8 and 13 pF, respectively. Using these parameters and the results of the above analysis, the circuit design is complete. See Table 1 for all design equations and final component values. The parameters R_L, Q_L, and I_{OUT} are the effective load resistance, the loaded Q, and the DC output current, respectively. This design is optimum in that it uses the smallest coupling capacitance possible to achieve the target specifications (equivalently, the maximum efficiency for this particular value of coupling capacitance).

Equation	Example Value
$\omega = \frac{P_{out}}{0.64 A_V V_S^2 2 C_{oss}}(1 - A_V)$	$2\pi 7.8\,\mathrm{Mrad/s}$
$L = \frac{1}{\omega^2 C} \times \left(\frac{\omega C}{2} \sqrt{V_S^2 - V_D^2} \frac{0.64 V_D}{P_{out}} + 1 \right)$	$3.8\,\mu\mathrm{H}$
$R_{on} = \frac{\tau_{sw}}{C_{oss}}$	$3.4\,\Omega$
$V_D = A_V V_S$	$28\,\mathrm{V}$
$\omega_0 = \frac{1}{\sqrt{LC}}$	$2\pi 6.7\,\mathrm{Mrad/s}$
$R_L = \frac{2 \times 0.64^2 V_D^2}{P_{out}}$	$161\,\Omega$
$Q_L = \frac{2}{R_L}\sqrt{\frac{L}{C}}$	1.9
$\|\|i_t\|\| = \frac{P_{out}}{(0.64 V_D)}$	$223\,\mathrm{mA}$
$\phi = -\arccos\left(V_D / V_S\right)$	-37°
$I_{OUT} = \frac{P_{out}}{V_D}$	$143\,\mathrm{mA}$

Table 1: Design equations with example design values.

Parameter	Design	Simulation
P_{out}	4 W	3.75 W
η	0.9	0.9
$\|\|i_t\|\|$	223 mA	196 mA
I_{OUT}	143 mA	133 mA

Table 2: Simulation results.

3.2 Simulation Results

The above design was simulated in Spectre. The results are summarized in Table 2. Fig. 6 shows the waveforms of the H-bridge output voltage and tank current, along with the gate voltages which drive the H-bridge. The voltage is commutated by the tank current during the dead-time of the H-bridge, indicating that the design meets the ZVS condition. The next section presents experimental results that verify this design methodology.

4 USB-level Capacitive Power Transfer System

This section presents the design and experimental verification of a 3.7 W, near 80% efficient CPT system requiring only 63 pF of series coupling capacitance, suitable for USB-level power delivery to a smartphone sized package. The design procedure in Section 3 is used to guide the design of the series resonant circuit. Techniques are presented that allow the circuit to remain near the optimum operating point as long as C is larger than the minimum required coupling capacitance and P_{out} is less than or equal to the design value. That is, the system is made tolerant to changes in alignment and load conditions. This is accomplished by automatically tuning the operating frequency and adjusting the duty cycle, respectively.

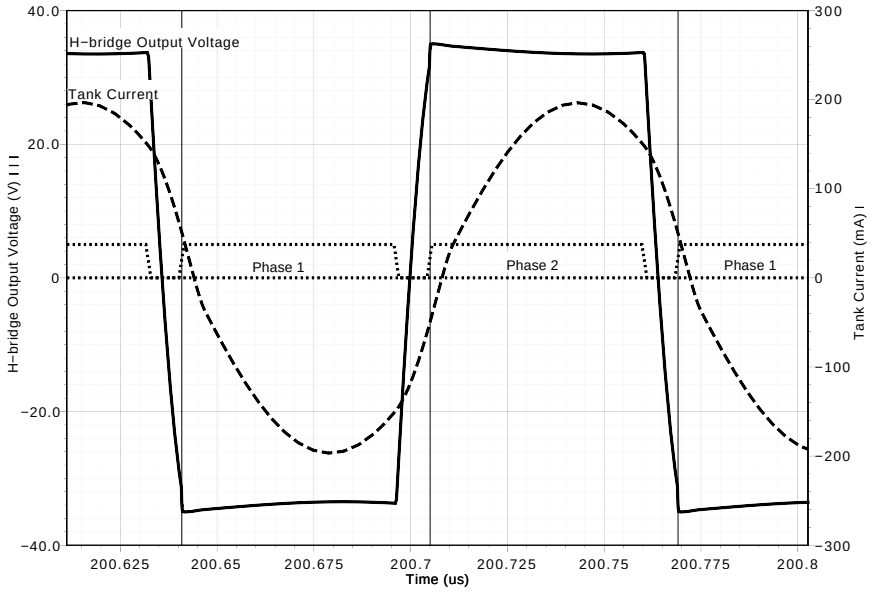

Figure 6: Simulation results of example design showing ZVS. Solid: H-bridge output voltage. Dashed: Tank current. Dotted: Gate drive voltages.

4.1 Series Resonant Circuit Design

A slight modification to the methodology presented in Section 3 is made to account for the rectifier non-ideality. The rectifier has two parasitics: conduction loss and parasitic capacitance. Assume that parasitics are the same as those of the H-bridge by design. The conduction loss can be modeled with either a voltage drop or equivalent on-resistance. This on-resistance has the same impact on the design equations as R_{on}. Parameter τ_{sw} is multiplied by 2 to account for this parasitic.

The parasitic capacitance creates an LCC resonant circuit that acts as an impedance transformation between the series tank and the rectifier input. The impedance seen by the tank is reduced, and there is voltage gain to the input of the rectifier. This implies that the voltage v_d in Fig. 3 is increased, thus i_t is reduced. The ZVS condition then becomes more strict according to (14). An exact analysis is not provided for the new condition, but this effect is mitigated by multiplying τ_{sw} by an additional factor of 2. This increases the C_{oss} parameter in (14) and works well in practice.

Parameter	Design	Simulation	Experimental
P_{out}	4 W	4 W	3.72 W
η	0.8	0.81	0.77
$\|\|i_t\|\|$	223 mA	222 mA	—
I_{OUT}	143 mA	142 mA	133 mA
$\angle(v_d/v_s)$	$-37°$	$-32°$	$-48°$

Table 3: Designed, simulated, and experimental results.

The design presented in Section 3 was redone with $\tau_{sw} = 4 \times 44\,\text{ps}$ to account for the rectifier capacitance and conduction loss. We relaxed η to 0.8 to reduce the required amount of capacitance. Using the above methods, the minimum C is 125 pF, corresponding to $A_V = 0.8$, $L = 13.1\,\mu\text{H}$, $C_{oss} = (2)12\,\text{pF}$, $R_{on} = (2)3.5\,\Omega$, and $f = 4.2\,\text{MHz}$. Note that half of both C_{oss} and R_{on} is contributed by the H-bridge switch and half by the rectifier switch (diode).

The circuit was implemented with discrete components on a printed circuit board (PCB). The components were chosen to match the above design as closely as possible. The Siliconix 1029X Complementary N- and P-channel MOSFETs are chosen as the H-bridge switches. The specifications are $R_{on} = 5.5\,\Omega$ and $C_{oss} = 8\,\text{pF}$, so $\tau_{sw} = 44\,\text{ps}$, which is no coincidence. To be clear, the optimization done above would suggest that we increase the size of the switch such that $R_{on} = 3.5\,\Omega$ and $C_{oss} = 12\,\text{pF}$.

The rectifier is composed of NXP PMEG6002EJ Schottky diodes which have approximately the same capacitance and conduction loss as the switches. The inductor is a Coilcraft 1812LS, which is a surface-mount, ferrite-core part with $L = 12\,\mu\text{H}$ and $Q = 42$. The capacitive interface is implemented with PCB capacitors separated by a Kapton film dielectric and two layers of soldermask. The PCBs were clamped together to minimize capacitance variation due to imperfect flatness. The total gap is about 0.13 mm with a dielectric constant of 3. The plate area required is then calculated as $6\,\text{cm}^2$. The capacitance was adjusted through

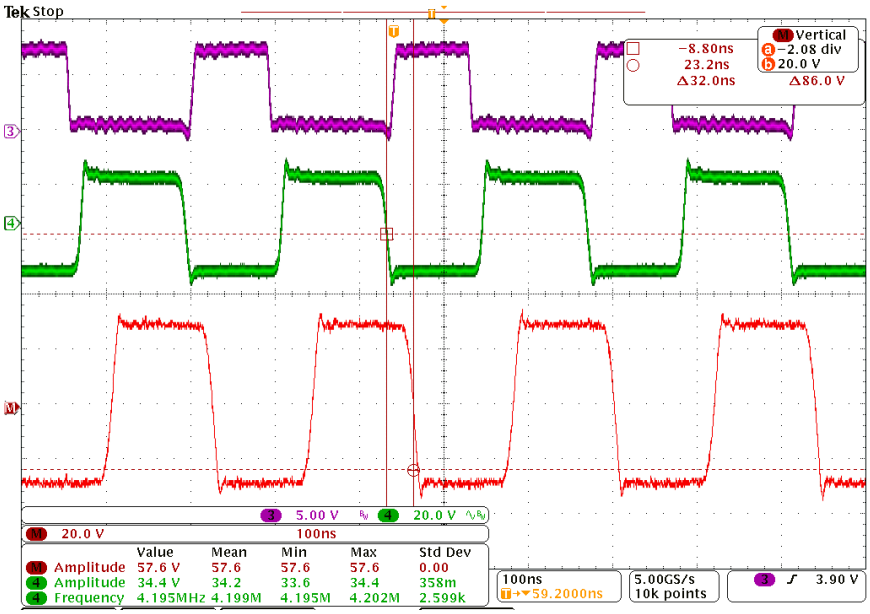

Figure 7: Experimental results showing ZVS. Top: 1 phase of gate drive voltage (5 V/div). Middle: 1 phase of H-bridge output voltage (20 V/div). Bottom: Differential input voltage to rectifier (20 V/div). Time scale is 100 ns/div.

alignment to be 125 pF to make an accurate comparison between calculated, simulated, and experimental results.

The experimental setup is essentially identical to Fig. 2. The switching frequency was set to 4.2 MHz with 15 ns of dead-time between the clock phases. The load voltage was set to 28 V. The input and output currents were measured to calculate the output power and efficiency. The results are included in Table 3. An oscilloscope capture of the H-bridge drive waveform showing ZVS is given in Fig. 7. This figure also shows the differential input voltage to the rectifier, which lags the H-bridge voltage by 32 ns or 48°. The increase in phase shift from simulated to experimental results can be attributed to parasitic loading from the oscilloscope probes.

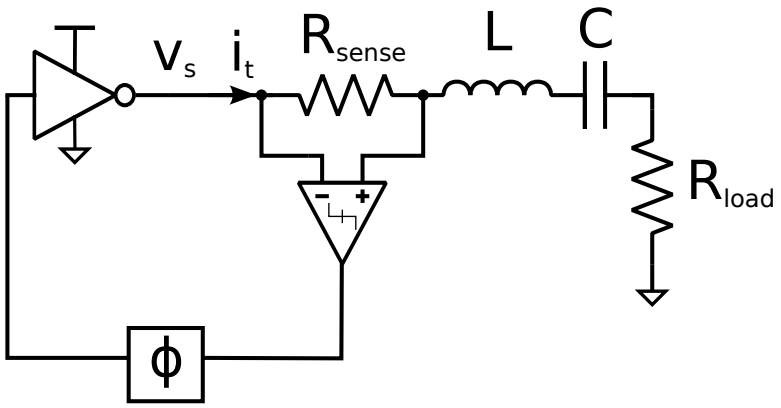

Figure 8: Simplified schematic of automatic frequency tuning loop.

4.2 Automatic Frequency Tuning

In order to make the performance of the powertrain insensitive to the exact amount of coupling capacitance, an oscillator is constructed that uses the primary LC tank as the frequency selective element [14]. A simplified schematic is presented in Fig. 8.

To understand the operation of the circuit, first assume that $\phi = 0$. Then the oscillation frequency is set to the point where the loop formed by the inverter, R_{sense}, and the comparator has 0 degrees of phase shift. Since the inverter and comparator each contribute 180°, their effects cancel. This forces the condition that v_s is in phase with i_t, so the frequency must be the resonance of the tank, $f = 1/(2\pi\sqrt{LC})$.

If $\phi \neq 0$, then the effect will be to force an equal and opposite phase shift between the tank current and input voltage, $\angle(i_t/v_s)$. This is illustrated in Fig. 9, which is a plot of $\angle(i_t/v_s)$ versus normalized frequency. For $\phi > 0$, the plot indicates that the oscillation frequency will shift up.

By setting ϕ equal and opposite to the phase shift calculated in the example design, the circuit is forced to run at the correct operating point. This also has the effect of regulating the output voltage because of the relationship derived in (3).

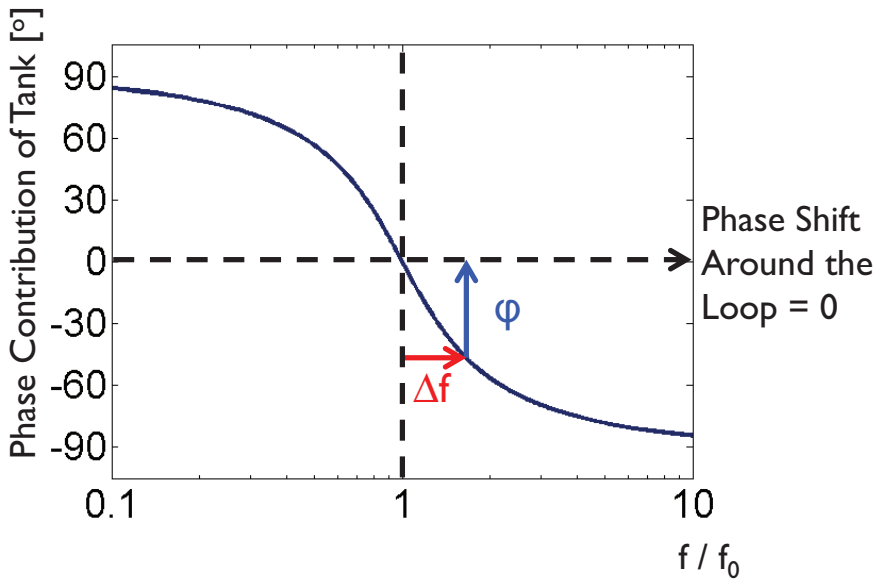

Figure 9: Effect of introducing extra phase shift into the frequency control loop.

4.3 Automatic Duty Cycle Control

In Section 2, the ZVS condition was derived assuming a constant output power. In particular, (15) shows the specific relationship, which clearly does not hold for all P_{out}. This will cause the light load efficiency of the powertrain to suffer, as ZVS will not occur. Multi-period pulse-width modulation (MPWM) is used to solve this problem.

In MPWM, the transmitter is switched on and off, with a duty cycle scaled proportionately with the output power. The desired operation under a light load condition is presented in Fig. 10. The top trace is the `SHUTDOWN` signal; when high, the transmitter is off. The middle trace is the DC component of the current drawn from V_S and the bottom trace is the DC output voltage.

The complementary duty cycle of `SHUTDOWN` is adjusted to the portion of full power that the load is drawing, in this case about 75%. When the transmitter is off, the load draws power from a hold-up capacitor, slightly discharging it. When turned back on, the supply current drawn will be the sum of the current required to recharge the hold-up capacitor and the load current. In this way, the average current drawn while the transmitter is running is

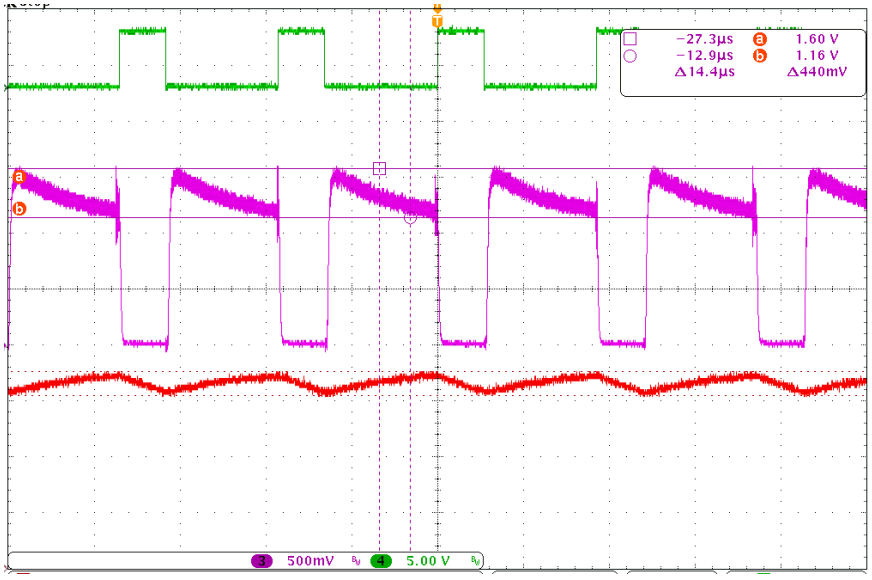

Figure 10: Experimental results showing operation of multiperiod PWM loop. Top: `SHUTDOWN` signal. Middle: DC Component of supply current (40 mA/div). Bottom: DC output voltage (10 V/div). Timescale is 40 μs/div.

always high enough to satisfy the ZVS condition, regardless of the load current.

As the hold-up capacitor is recharged, the supply current will decrease. This can be detected, and the transmitter can be shutdown until the beginning of the next MPWM cycle. This will result in the duty cycle being automatically adjusted to the load condition.

The the hold-up capacitor should be sized based on the allowable amount of ripple on the DC output voltage. The relationship between voltage ripple, power, frequency, and capacitance is given in [15].

4.4 Experimental Results

Fig. 11 presents a block diagram of the designed system, composed of the pieces described above. Automatic frequency tuning was implemented by measuring the zero crossing of the inductor voltage rather than the tank current. Because the current is nearly sinusoidal, this

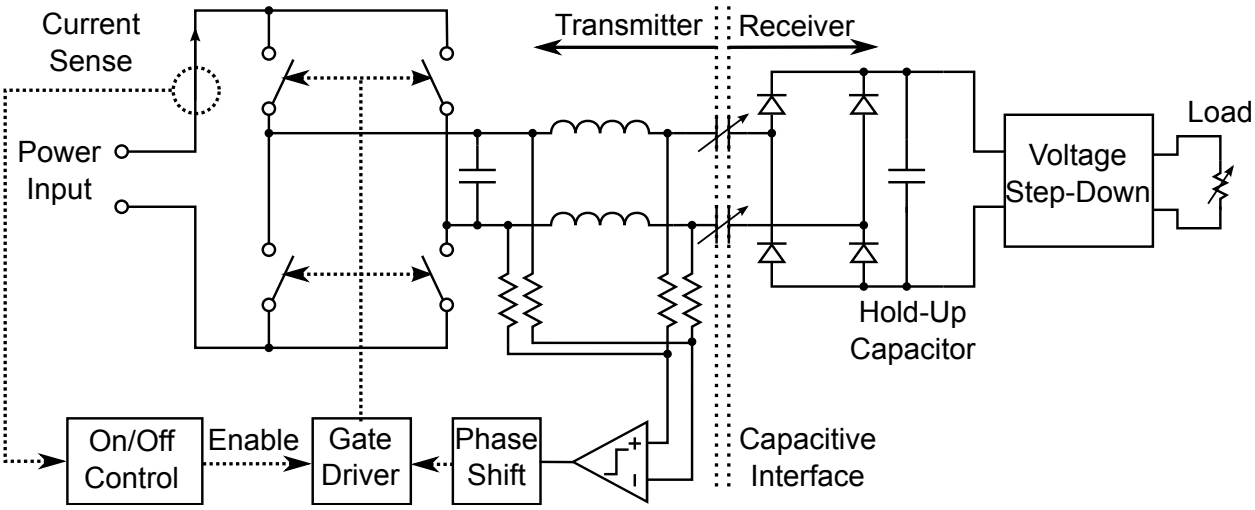

Figure 11: Block diagram of CPT system including series resonant converter, automatic frequency control, and automatic duty cycle control.

simply results in 90° of phase lead, which is compensated for in the phase shift block. A relaxation oscillator embedded in the loop starts the circuit up then locks to the correct frequency.

MPWM is implemented with the on-off controller, which senses the average value of the supply current with a second-order low-pass filter. The filter is designed to attenuate the current component at twice the operating frequency while responding quickly to changes in the DC component. This current is compared with a reference. If it is less than the reference value, the gate drive circuit is disabled, and the powertrain is turned off. A 38.8 kHz clock forces the powertrain on for a minimum of 3.5 μs every cycle, which is enough time for the series resonant circuit to reach steady state. A 1 μF capacitor is sufficient to hold-up the output voltage under worst-case conditions. A limiter clamps the supply current to a safe value in case of a short circuit or cold-start condition.

The efficiency was measured for a range of output power with $C = 156$ pF (no added misalignment). The results are presented in Fig. 12; the loss of the final step-down is not included. The switching frequency was measured to be 4 MHz. To first order, the efficiency should remain constant across the range of output power, but because of the dynamics in-

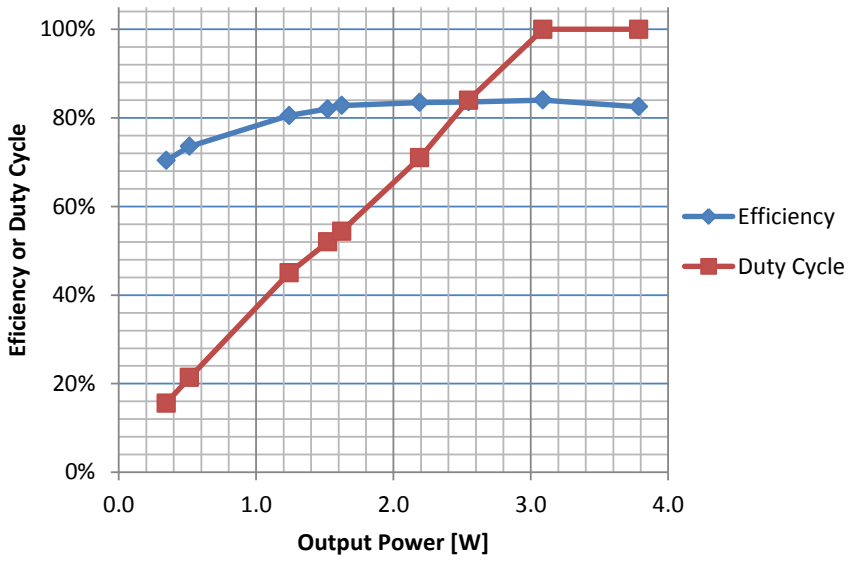

Figure 12: Experimental data showing efficiency and duty cycle vs. output power for designed CPT system.

volved in turning the transmitter on and off, the efficiency slightly drops off at light loads. The peak efficiency is 84% at 3.2 W of output power. The duty cycle is also plotted in Fig. 12. The transmitter is always on until the output power drops below 3.2 W; this threshold is determined by the reference tank current. The duty cycle scales linearly with the output power below this point, as expected. Fig. 10, described above, was captured from this particular system running at 75% duty cycle.

4.5 Alignment Sensitivity Reduction

It is worth mentioning some techniques to reduce the alignment sensitivity of CPT. This problem is unique to the charging application and arrises because there is potential to misalign the transmitter and receiver, reducing the available amount of capacitance. The adaptive frequency control reduces the sensitivity to the exact value of coupling capacitance. However, this does not solve the problem addressed in [16], when one of the receiver plates overlaps both phases of transmitter plates. The effect is that the current injected into the

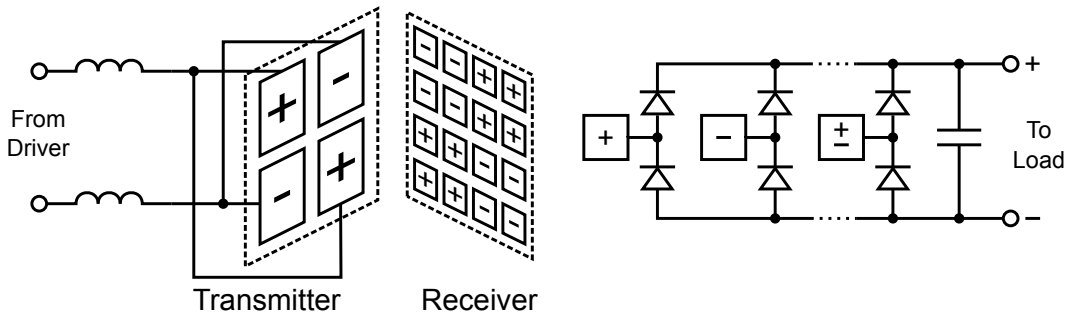

Figure 13: Pixelated electrodes concept.

receiver by one side of the transmitter will be partially canceled by the other side. Clearly, this is an undesirable effect, and this situation should be avoided through intelligent design of the geometry, i.e., making it impossible for receiver plates to bridge transmitter plates, or through electronic alignment control, i.e., turning off those transmitter plates being bridged by a receiver plate [17].

The latter option has the disadvantage of requiring many separate drivers, thus many wires that connect the plates to the half-bridge drivers. A more attractive option may be to pixelate the receiver, and design the pixel size so that two transmitter plates cannot be shorted by one pixel. A schematic representation is shown in Figure 13. Each pixel is connected to its own rectifying half-bridge. The advantage is that the rectifiers are all self-configuring; they force current to flow in the correct direction. Disadvantages are the large number of rectifiers needed and increased amount of parasitic capacitance. Further disadvantages with both of these options are that the fill factor will be reduced, due to the finite gap spacings required between plates, and the capacitors could easily become mismatched, leading to high-frequency common mode signals present on the receiver.

Considering all of this, the best solution for contactless charging applications may be to use some reasonable mechanical limits to prevent severe misalignment and to rely on the adaptive frequency control to allow for variations in the coupling capacitance. Other applications reqiring less power and more freedom of movement, such as cordless mice, can benefit from pixelation of either the transmitter or receiver electrodes.

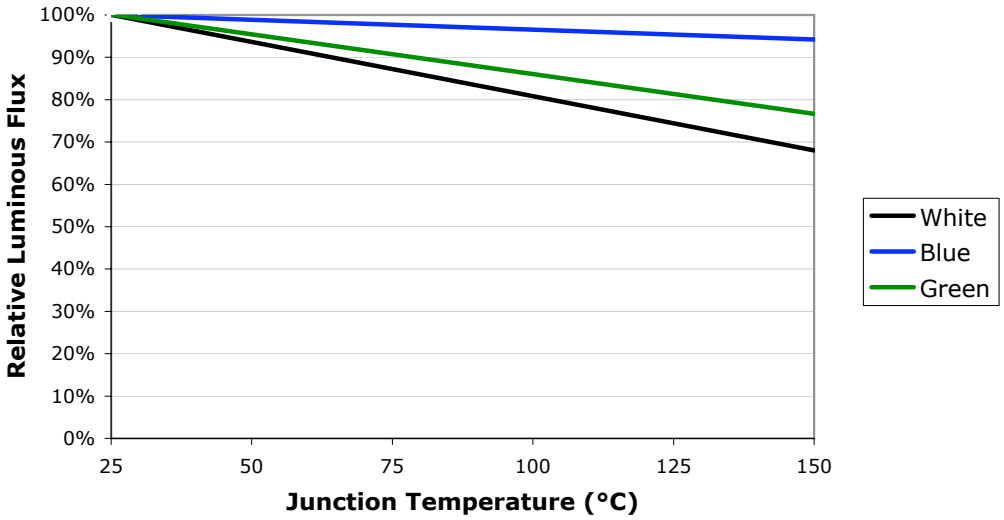

Figure 14: Typical light output versus junction temperature characteristics from a Cree XR-E series LED [18].

5 Galvanically Isolated Capacitive LED Driver

Residential LED lighting is an emerging market, with several manufacturers producing screw-in retrofit LED lamps designed to be used in standard $120\,\mathrm{V_{rms}}$ Edison sockets. There are many unique challenges to LED lighting circuits, the paramount of which is thermal management. Unlike incandescent lamps, which work well at filament temperatures up to 2500 °C, LED junctions are limited to cool temperatures, typically less than 100 °C. Figure 14 is a plot of luminous flux (light output) versus junction temperature from a Cree XR-E series LED. The heat produced by an LED is not directly convected but must be conducted through the back-side of the chip. The heat transfer path is typically from junction to solder point to board to atmosphere. It is critical to minimize the total thermal resistance from junction to ambient to provide adequate cooling of the LED.

Ideally, the LED would be directly bonded to a large, atmosphere-exposed metal heat sink to minimize the total thermal resistance. In this configuration, the heat sink would become a shock hazard, as standard Edison sockets have no earth connection. To overcome this problem, ceramics acting as electrical insulators have been proposed as heat sink materials [19].

This solution is attractive because no additional electronic isolation component is needed. This component is normally a transformer, which is bulky, expensive, and takes up valuable space inside the volume-constrained lamp housing. However, the thermal conductivity of the proposed ceramic Rubalit is an order of magnitude less than that of aluminum, 24 W/(Km) versus 210 W/(Km) [20]. To take advantage of the high thermal conductivity and low cost of aluminum while not requiring a bulky transformer, we propose using a capacitive isolation barrier.

The same techniques and circuit—Figure 2—described in Sections 2 and 3 are applicable to the design of efficient capacitively isolated LED drivers. In particular, we are concerned with maximizing the efficiency for a particular power output and coupling capacitance. As described in Section 1, the amount of coupling capacitance is limited by galvanic isolation constraints. Typical safety rated isolation capacitors are constrained to values below 10 nF.

In addition to presenting a powertrain design, we also discuss using the series resonant circuit as a current regulator, which eliminates the need for any additional electronics on the isolated side of the power converter. Work is still on progress on the experimental prototype LED driver. Only simulation results are provided in the following sections.

5.1 12.6 W LED Driver Design

In this example design, we investigate the circuit design for a screw-in LED lamp that produces light equivalent to a 60 W incandescent. The chosen white Cree XR-E LED (`XREWHT-L1-0000-00D01`) has a luminous efficiency of about 85 lm/W. One LED consumes 1.26 W at 350 mA, thus 10 LEDs would consume 12.6 W and produce 1070 lm. As a comparison, a typical 60 W incandescent produces 870 lm, giving 14.5 lm/W.

The nominal output voltage of 10 LEDs in series is 36 V. Using the equations of Section 2, we calculate that 1 nF of capacitance is sufficient to achieve efficiencies above 90%. For reference, a suitable capacitor could be the 3 kV ceramic C0G part from AVX (`2220HA102K`). An operating point corresponding to 93% efficiency is given in Table 4. Note that the factors

Operating Point
$\eta_{max} = 0.93$
$C_{oss,opt} = 2 \times 43\,\text{pF}$ (optimum switch size)
$A_{V,opt} = 0.69$
$V_S = 56\,\text{V}$
$\omega = 2\pi 3.02\,\text{Mrad/s}$
$L = 4.6\,\mu\text{H}$
$R_{on} = 2 \times 0.53\,\Omega$
$\omega_0 = 2\pi 2.35\,\text{Mrad/s}$
$R_L = 84\,\Omega$
$Q_L = 1.6$
$\|\|i_t\|\| = 547\,\text{mA}$
$\phi = -46^\circ$
$I_{OUT} = 350\,\text{mA}$

Table 4: LED circuit operating point corresponding to $P_{out} = 12.6\,\text{W}$, $V_D = 36\,\text{V}$, $\tau_{sw} = 4 \times 22.5\,\text{ps}$, $Q = 50$, and $C = 1\,\text{nF}$.

of 2 and 4 are due to accounting for rectifier loss.

The circuit was simulated in Spectre, and the results are summarized in Table 5. The discrepancy in the voltage V_S is due to the rectifier non-ideality. Suggested components are listed in Table 6.

5.2 Regulation

Unlike incandescent lamps, LEDs require regulated, low-ripple DC current. It is important to control the current precisely, as the luminous efficiency is maximized at a particular current density. Additionally, control of the current is necessary to enable lamp dimming.

Parameter	Design	Simulation
P_{out}	12.6 W	12.4 W
η	0.93	0.93
$\|\|i_t\|\|$	547 mA	513 mA
I_{OUT}	350 mA	344 mA
V_S	56 V	44 V

Table 5: LED driver simulation results.

Component	Manufacturer	Part Number	Attributes
Switch	Siliconix	`Si2308BDS`	$R_{on} = 0.192\,\Omega$, $C_{oss} = 26\,\text{pF}$
Inductor	Coilcraft	`1812FS-472`	$L = 4.7\,\mu\text{H}$, $Q = 84\,@\,3\,\text{MHz}$
Capacitor	AVX	`2220HA102K`	$C = 1\,\text{nF}$, $V_{max} = 3\,\text{kV}$
Rectifier Diode	Diodes Inc.	`PD3S160`	$C = 38\,\text{pF}$, $V_F = 0.58\,\text{V}\,@\,0.7\,\text{A}$

Table 6: Suggested LED driver components.

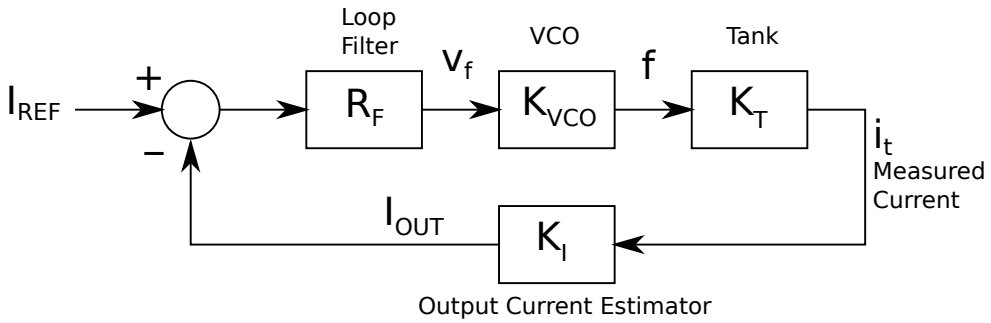

Figure 15: Block diagram of LED current regulator, with I_{OUT} being estimated from the measured tank current i_t.

In Section 2 we derived an expression for the tank current,

$$||i_t|| \approx \underbrace{\frac{\omega C/2}{\omega^2 LC - 1}}_{\text{conduction of tank}} \times \underbrace{\sqrt{V_S^2 - V_D^2}}_{\text{magnitude of tank voltage}} ,$$

repeated here for convenience. The output current is directly related to the tank current as in (8) and can be controlled by adjusting the *conduction of the tank* term above. The most straightforward way of doing this is by adjusting the operating frequency. The relationship between $||i_t||$ and ω is nonlinear but it is monotonic so long as $\omega > \omega_0$.

Using negative feedback, a controller is formed to regulate the output current. The block diagram in presented in Figure 15. A voltage controlled oscillator (VCO) with gain K_{VCO} in Hertz per volt is used to synthesize the frequency f ($\omega = 2\pi f$) that controls the tank current. To avoid having current sense electronics on the isolated side of the power converter, the tank current is directly measured, and the output current is estimated with the K_I block. The estimated output current is subtracted from a reference, and the error is amplified and filtered by the loop compensator R_F. The loop gain,

$$\mathcal{R} = R_F K_{VCO} K_T K_I, \tag{19}$$

determines the steady state error,

$$\epsilon = \frac{1}{1 + \mathcal{R}}. \tag{20}$$

The allowed steady state error, along with stability issues due to the dynamics of K_T, K_{VCO},

and K_I, influence the design of the loop filter R_F. Here we consider analytically only the steady state error and confirm through simulation the loop stability.

The K_T block models the transfer function from operating frequency to tank current, described by the nonlinear function (5) above. This function can be linearized around the nominal operating point ω_n, giving

$$K_T \approx -\frac{C}{2}\frac{\omega_n^2 LC + 1}{(\omega_n^2 LC - 1)^2} \times \sqrt{V_S^2 - V_D^2}. \tag{21}$$

Using the sign convention in Figure 15, the loop gain $\mathcal{R}$ is positive for negative feedback. Since K_T is negative, an additional inversion in the loop is necessary to correct the sign of the loop gain.

Using the powertrain design above, K_T is calculated to be $-140\,\mathrm{mA/MHz}$. Using (6), $K_I = 0.64$. For a steady state error of 10%, the loop gain should be about 10, giving

$$R_F K_{VCO} = \frac{\mathcal{R}}{K_T K_I} = -0.11\,\mathrm{MHz/mA}. \tag{22}$$

The loop was simulated in Spectre using the specifications above. The output current estimator K_I is implemented with a rectifier followed by low pass filter. This has the desired effect of calculating the average value of the rectified tank current and does not rely on the current waveform being purely sinusoidal. Dominant pole compensation was implemented with the R_F block. The pole was placed at 160 Hz; the closed-loop rise-time is then calculated to be $230\,\mu$s.

Figure 16 is a plot of the simulated output current and error signals of the closed loop system. The rise-time of the error signal is approximately $50\,\mu$s. The simulated loop gain is 60. The simulated VCO frequency is 3.3 MHz. The discrepancy between the reported error signal and the actual error in the output current is due to the slight inaccuracy of the current approximation block K_I.

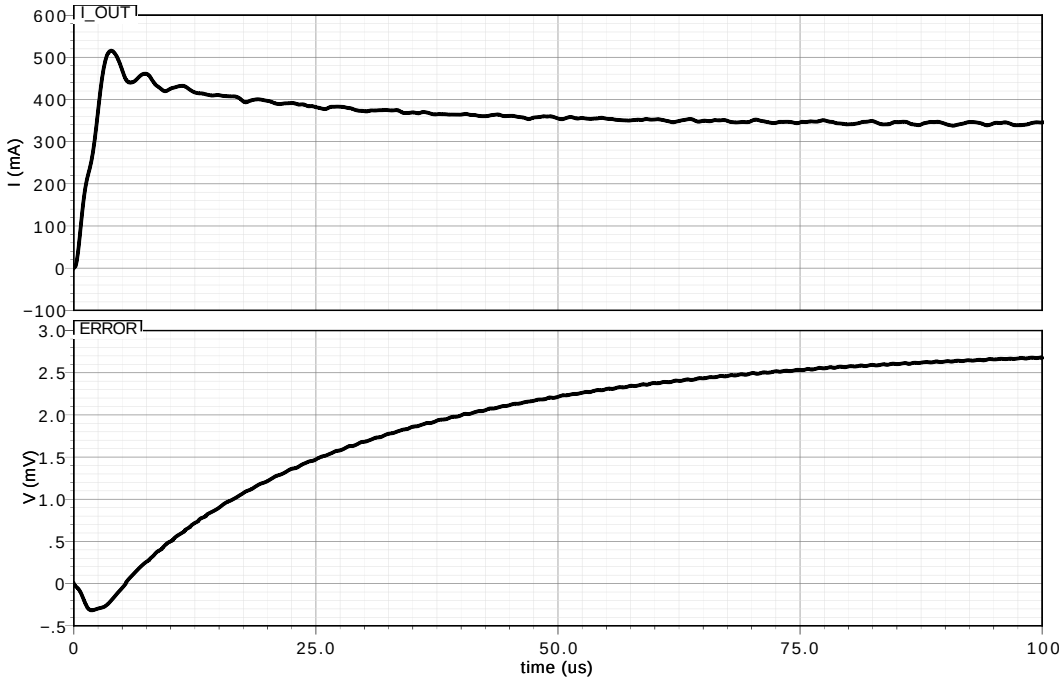

Figure 16: Simulation of current regulation demonstrating loop stability. Top: Output current, I_{OUT}. The final value is 343 mA. Bottom: Error signal; final value 2.8 mA (1 A/V).

6 Conclusion

Small air gap capacitors enable high efficiency contactless power transfer. Their simplicity, small size, and low EMI makes them a very attractive solution for efficient charging of battery powered appliances such as smartphones. The key to high efficiency is series resonant operation using small and moderate Q ferrite core inductors, enabling soft-switching and high frequencies. Dynamically adjusting the operating frequency and duty cycle ensures high efficiency over a wide range of load conditions and accommodates large capacitance variations resulting, for example, from variations of alignment of the capacitor plates on the primary and secondary. This tuning is accomplished continuously in the background at the primary only, thus alleviating the need for a feedback loop from the load side back to the controller. Capacitive powering can be easily combined with high speed data transfer, enabling both charging and data synchronization over a single interface.

The same techniques described for capacitive contactless power transfer are applicable to galvanically isolated power supplies. A series resonant circuit serves a dual purpose as an isolation barrier and current regulator. Capacitive isolation in LED lighting circuits is attractive due to the reduced size compared to transformer-based solutions and low-cost enabled by allowing heat-sinks to be made of electrically conductive materials, such as aluminum. The proposed circuit can be combined with well-known [21, 22] switched capacitor step-down converters to enable a fully functional offline LED driver.

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