Solution Processed Silver Sulfide Thin Films for Filament Memory Applications

Shong Yin
Vivek Subramanian, Ed.

Electrical Engineering and Computer Sciences
University of California at Berkeley

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by

Shong Yin

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Committee in Charge:

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Professor Tsu-Jae King Liu

Professor Ronald Gronsky

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Abstract

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Filament Memories based on resistive switching have been attracting attention in recent years as a potential replacement for flash memory in CMOS technology and as a potential candidate memory for low-cost, large-area electronics. These memories operate at low voltages with fast switching speeds. These devices are based on ionic conduction through an electrolyte layer and differ fundamentally in operation from conventional flash memory, which is based on the field effect transistor. To facilitate development of this technology, effects of film structure on ionic and electronic conducting properties and the filament formation processes must be studied.

In this work, silver sulfide, a mixed ionic-electronic conductor, is used as a model material for studying the solution processing of filament memories, and to study the impact of film structure on conducting and switching properties. Three different solution processing methods are investigated for depositing silver sulfide: sulfidation of elemental silver films, and sintering of two types of silver sulfide nanoparticles. Effects of nanoparticle sintering conditions on electrolyte structured and mixed conducting properties are investigated by a combination of X-ray diffraction, electrical impedance spectroscopy and thermo-gravimetric analysis. Impact of forming voltage and time on filament morphology is examined to provide an overall view of the impact of electrical and material parameters on device operation.

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Acknowledgements

The Ph D is a long sojourn of learning and discovery. It is similar to finding a new path through an unknown forest, starting out with only a spoon in hand. Along this journey, new skills are learned, new tools are found for use, and new friends and colleagues are met. There are many people that have made this journey worthwhile and possible. I thank my advisor Vivek Subramanian for providing the freedom and encouragement to explore new and novel topics. My father, mother, sisters: Siejen and Sue, and brother-in-law Pete have always provided their support. Steve Volkman has provided invaluable assistance and instruction in brainstorming new research ideas. Mike Toney of SSRL and Kanan Puntambekar assisted in learning X-ray diffraction analysis. I gratefully acknowledge my colleagues in the Organic Electronics Group. Daniel Huang provided firm and useful reminders about the utility of the scientific method. Alejandro De La Fuente Vornbrock always provided genuine motivation. Feng Pan provided the modeling verification of the filament formation studies in the work. Jaewon Jang is thanked for providing the aqueous Ag_2S nanoparticle synthesis which was essential to this work. Tim Bakishev and Ben Weil are thanked for assistance with projects. The NSF, JSPS and NRF, and Dr. Kazuya Terabe and Professor Chan Siew Hwa are thanked for providing the opportunity work at NIMS and NTU. Delia Milliron, Robert Wang, and Ravi Tangirala of the Molecular Foundry at the Lawrence Berkeley National Laboratory are thanked for helpful discussions and assistance with the ODA Ag_2S nanoparticle synthesis. The Balsara Laboratory provided access to the Solartron tools used in impedance measurements. The Alivisatos Group provided access to the TGA and DSC tools. Many thanks are extended to my qualifying exam and dissertation committee members: Professors Tsu-Jae King Liu, Ronald Gronsky and Nathan Cheung.

Chapter 1: Introduction

1.1: Non-Volatile Memory Background

Nonvolatile memory (NVM) is an essential component of electronics. The abilities to store information in solid state devices and furthermore scale these devices to smaller dimensions have enabled various industries ranging from automotive to consumer electronics. Requirements of these memories vary by application. Engine control units in automobiles require memories having very high data integrity, but can tolerate high voltage operation (5V), high power consumption and low cycle life [1]. Inversely in consumer electronics, portable devices like smartphones require memories having low voltage operation (3.6V), low power consumption and high cycle life.

The scaling of non-volatile flash memories has enabled the enormous growth of low-cost portable consumer products in the last decade. An 8 gigabyte (GB) thumb drive as small as a keychain, and costing less than $10 can store the entire contents of 10 compact discs (CDs). iPhone devices once fathomable only in science fiction movies are now used by over 14 million people worldwide. Emerging challenges to the scaling of flash memory threatens to slow the development of this product market. In response to these scaling challenges, novel non-volatile memory device technologies are being actively researched as possible replacements to flash memory.

In addition to the need for a flash memory replacement, there is an emerging need for a non-volatile rewriteable memory in printed electronics. This field targets novel low-cost, large device area applications such as flexible displays and smart radio frequency identification (RFID) tags. A portable tablet personal computer (PC) using a touch screen display that can be rolled up like a newspaper is one exciting new product that could arise from this field. Plastic organic polymer substrates and solution processing are used to facilitate the low-cost manufacturing of these products. Thus, primary requirements for a printed non-volatile memory technology are compatibility with processing constraints of plastic organic polymer substrates, and solution processing.

Resistive Switching Random Access Memory (RRAM) is a class of NVM technology that can potentially satisfy the requirements of a flash memory replacement, and a printable NVM. These devices are two-terminal switches that can occupy a smaller device area compared to three-terminal flash devices. Furthermore, the active switching materials of RRAMs can be processed at low temperatures (<200C). This allows vertical stacking in CMOS integration to increase effective areal device density, and is compatible with plastic substrates. This chapter will review flash memory and its scaling challenges, provide an overview of printable electronics, and describe RRAM technology in further detail.

1.1.1: Flash Memory Background and Scaling Challenges

Current solid state rewritable non-volatile Flash memory is based on the floating gate transistor illustrated in FIG 1-1A. These are fabricated from single crystal silicon substrates and are n-type. The higher mobility of electrons relative to holes in silicon facilitates higher current

and faster programming. A cross-sectional band diagram of the gate-stack in FIG 1-1B illustrates how the floating gate serves as a potential well for electronic carriers. Data is stored by injecting electrons from the transistor channel through the bottom oxide into the storage element. This charge injection changes the electrostatics by shifting the threshold voltage (V_t) positive for an n-type metal oxide semiconductor (NMOS) field effect transistor (FET) as illustrated in FIG 1-2. The memory state is detected by reading current through the channel under a voltage bias on the gate. Although this type of device has served as the standard non-volatile memory for over twenty years, there are now many challenges to scale it towards lower voltages and smaller geometries. These scaling issues are related to the fundamental operation and design of the devices.

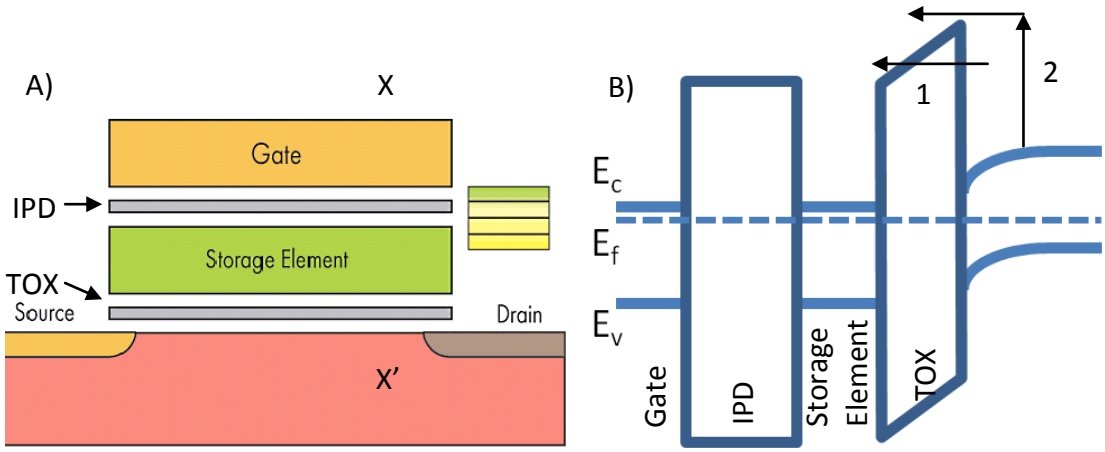


FIG 1-1: Sample Cross-section A) Floating Gate Transistor B) Band Diagram Through Gate Stack XX'. Two programming mechanisms are illustrated: 1) Fowler-Nordheim Tunneling, 2) Hot Carrier Injection

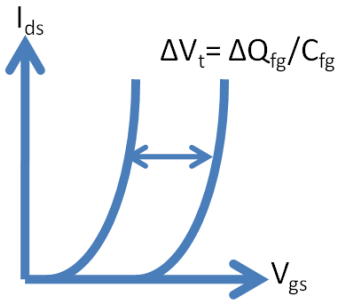


FIG 1-2: Drain Current vs Gate Bias; V_t shift caused by change in electronic charge on storage element

NOR and NAND are the two broad classes of Flash Memory used today, named for the implemented logic function. These differ by programming mechanism and circuit layout. NOR flash is implemented as the pull-down circuit network of a NOR logic gate. Each memory cell has a dedicated bitline (BL) and ground (GND). These dedicated connections allow fast random access of each cell for reliable read and write operations. However, because one bit line per cell must be contacted by metal lines, the minimum array areal density is limited. The contact hole adds $4F^2$ to each cell (where F is the minimum feature size of the fabrication technology) resulting in a large cell feature area of $8F^2$.

NOR flash is programmed by hot carrier injection which consumes significant power. This process is illustrated briefly in FIG 1-1B2. The lucky electron model explains this mechanism as a series of three requisite events. First, under high electric field at the drain, electrons attain sufficient kinetic energy to become "hot" enough to surmount the potential barrier between the channel and floating gate. Second, a fraction of these hot electrons will be redirected towards the floating gate by a positive gate bias. Finally, the diverted electrons must not encounter any energy losing collisions before settling into the potential well. In this mechanism, only a fraction of the drain current directly programs the gate, resulting in high power write operations [2]. Because of its high data integrity and fast read speed, NOR flash has traditionally been used for code storage in portable devices.

NAND flash is implemented as the pull-down circuit network of a NAND logic gate. Memory cells are connected in chains of 32 transistors or more [3]. There are two contacts per transistor chain, reducing the cell feature area to a minimum of nearly $4F^2$, resulting in high cell density. However, because data must be accessed through a series of pass transistors and associated resistive voltage drops, the data integrity and random access speed to bits in NAND is lower than NOR. Bit errors during read are handled by error correction codes.

NAND is programmed by Fowler-Nordheim tunneling, illustrated in FIG 1-1B1. Under high electric field, the tunneling distance of the dielectric is thinned at the top of the energy barrier, facilitating electron tunneling into the storage gate. This requires significantly less power per cell than the hot-electron injection method used by NOR. Because of high cell density and low power, NAND has been used for mass data storage applications in consumer electronics such as digital cameras and media players.

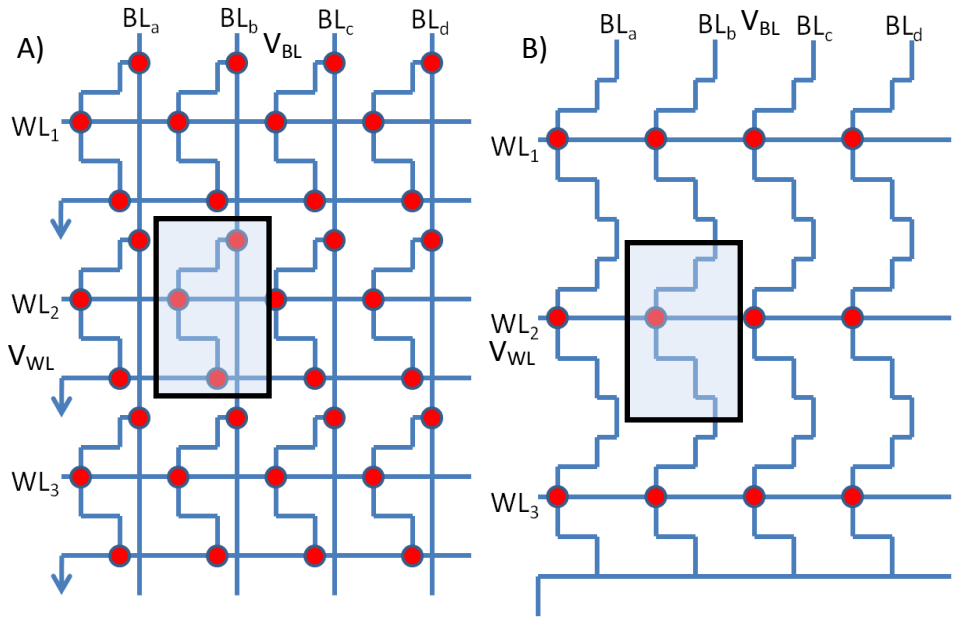


FIG 1-3: Flash Circuit Schematics A) NOR B) NAND. Red dots indicate contact point. Box indicates selected cell during program/read operation.

During operation of floating gate transistors in NAND and NOR arrays, non-ideal voltages applied to unselected cells cause disturb effects [4][5]. These are classified as Word Line (WL) and Bit Line (BL) disturbs. FIG 1-3 illustrates these effects for a cell in row 2, column b in a NOR and NAND array. For simplicity, only DC effects are considered in this section. When programming cell 2b in a NOR array, voltage is applied to WL_2 and BL_b, while other WL and BL are grounded. Unselected cells in row 2 are affected by the high gate bias. If the unselected cell is initially erased, electrons may tunnel through the tunnel oxide, resulting in a programming effect. If the cell is initially programmed, electrons may tunnel through the IPD, resulting in an erase effect. In unselected cells along the biased BL column b, high field between the drain and unbiased control gate may cause tunneling of electrons from the floating gate to the drain, resulting in an erase effect. During read operation in the NOR array, a low bias is applied to the BL, and moderate bias is applied to the WL. This may cause electronic tunneling from the substrate to the floating gate, causing unwanted programming.

During programming in a NAND array, the WL_2 and BL_b of the selected cell are set to V_{WL} and GND respectively. The WL and BL of the unselected cells are all set to $V_{WL}/2$. Ideally, only the selected cell 2b will have a gate-source/drain bias of V_{WL} and be programmed. However, all adjacent cells: 2a, 2c, 1b, 3b, will experience a gate-substrate bias of $V_{WL}/2$ and be partially programmed. During a read operation in a NAND array, all unselected WL are biased above the programmed V_t to act as fully turned-on pass transistors. The selected WL is biased at a voltage between the programmed and erased V_t. All of the unselected WLs receive elevated voltage stress that can cause undesirable programming disturbs.

Various static disturb effects for NAND and NOR have been described. In real programming and read operations, pulsed voltage is used instead of DC voltage. This creates dynamic disturb effects. As the pitch between poly WL is reduced, capacitive coupling between adjacent rows increases. This coupling can cause program disturb of unselected cells. Referring back to FIG 1-3, pulsing high voltage on WL_2 during programming will also pull WL_1 and WL_3 high, causing program disturb of cells in those rows. Such effects from capacitive coupling become more severe with scaling.

Worsening of disturb effects is one of many scaling challenges that both NAND and NOR flash face going forward. According to the 2009 ITRS, the demonstrated minimum feature size (defined as the half pitch between poly lines) is 38nm for NAND flash and 50nm for NOR flash. Some of the scaling challenges arise from the common floating gate transistor structure, while others are unique to the implementations of NAND and NOR.

The tunnel oxide thickness of the FG cell is set by limits on tunneling current leakage that degrades the data retention. The minimum thickness of the IPD is also limited because it is tied to the tunnel oxide thickness by constraints on the gate coupling ratio (GCR). This GCR is the ratio of the IPD capacitance to the total capacitance of the floating gate. The higher this value is, the higher the fraction of control gate-substrate voltage that will drop across the tunnel oxide. For modern floating gate devices, the minimum GCR is 0.6 [3][2]. This prevents tunneling of electrons through the IPD under high gate bias, and ensures that the bulk of

voltage drop will be across the tunnel oxide. The derivation of the GCR may be illustrated using FIG 1-4.

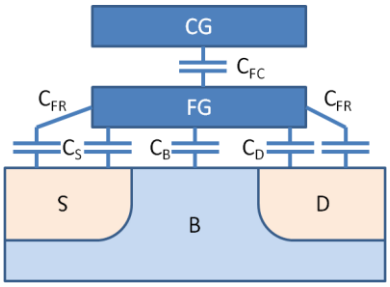


FIG 1-4: Capacitances with respect to floating gate in a floating gate transistor

Independent electrode voltages are the control gate (V_G), source (V_S), drain (V_D) and bulk (V_B). These may be related to total charge and capacitance.

$$Q_{FG} = C_{FC}(V_{FG}-V_{CG}) + C_D(V_{FG}-V_D) + C_S(V_{FG}-V_S) + C_B(V_{FG}-V_B)$$

Equation 1-1: Total Charge on Floating Gate neglecting fringing capacitance

By assuming zero charge on the gate, using the source as the voltage reference, and tying the source and bulk together, an expression can be derived that relates the floating gate voltage to a ratio of electrode capacitances as shown in Equation 1-2. α_G is the GCR. The ratio α_D/α_G is small because the floating gate-drain overlap is small relative to the control gate-floating gate overlap [2].

$$V_{FG} = \alpha_G(V_{GS} + \alpha_D/\alpha_G * V_{DS})$$

Equation 1-2: Relation between floating gate, control gate, and drain voltages. A represents the ratio of the associated capacitance to total capacitance.

Current NAND devices use control gates wrapped around the floating gate to increase the GCR. As devices are scaled laterally, this geometry is difficult to maintain. Fringing capacitance also becomes a larger fraction of total FG capacitance, reducing the effective GCR. Because of all these factors, the minimum required GCR is difficult to sustain with continued scaling.

Reduction of electronic charge capacity of the floating gate is another problem that arises with the scaling of FG cells. As the number of stored electrons decreases, the total charge and shift in V_t become more sensitive to fluctuations in the number of electrons. This makes management of bit statistics across an array difficult. In flash memory, common reference threshold voltages are defined for groups of cells to specify the programmed and erased states. Wide and overlapping distributions of programmed and erased V_t impedes selection of these levels. Despite the physical issues of scaling, innovations in architecture have enabled virtual enhancement of bit density in multi-level cells. By encoding 4 V_t levels, 2 bits are effectively stored per cell. However, increasing bit density using this method becomes exponentially more difficult as 2^N distributions of V_t levels are required to encode N bits per cell.

Although FG transistor cells are becoming harder to scale in general, the NOR flash implementation has been more difficult to scale than NAND flash. The requisite contact hole per cell bit line has restricted minimum cell area due to necessary buffers for contact hole to active layer, and metal to contact hole alignment. NAND flash eliminates these extra alignment steps and layout margins by using a self aligned process to fabricate the array. The hot-electron programming method requires high lateral electric fields at the drain. Heavy doping can increase these fields, but lowers the junction breakdown voltage and aggravates short channel effect. The minimum thickness of the NOR tunnel oxide is more limited than NAND by stringent requirements on NOR data integrity. Because a lower tunneling loss is required, a thicker tunnel oxide must be used that further aggravates short channel effect. In addition to these NOR scaling challenges, NAND flash is steadily displacing the market for NOR. New caching architecture and efficient compilation of program code allows NAND flash to emulate the read performance of NOR flash. NAND flash is now the driver and benchmark for FG based non-volatile memory scaling. The difficult outlook for FG based memory scaling has facilitated new research efforts into novel and alternative memory technology.

1.1.2: Printable Non-Volatile Memory Background

In addition to conventional CMOS electronics, the emerging field of printable electronics needs a non-FG based non-volatile memory technology. This field has generated large interest in recent years with promises of low-cost ubiquitous displays, e-textiles, RFID tags and various types of sensors. PDAs like iPads that can be rolled up and stored away as newspapers and smart soldier uniforms that can diagnose wounds for medical treatment are just two exciting applications. Smart inventory control of food items in a supermarket is one pragmatic application for the general populace. RFID price tags that do not require line of site for scanning would enable high throughput at checkout. Grocery purchasing could become as fast as driving through the electronic tollbooth on a highway, instead of having to manually unload and repack items from a checkout conveyor belt. Integrated sensors on the tags that can accurately detect food spoilage would facilitate smart pricing to automatically discount products near expiration. Furthermore, accurate detection of food spoilage would reduce premature disposal of food items by following an arbitrary expiration date that was assigned at the time of packing.

The common traits of these applications are low-cost, low transistor count, large device area applications. The main goal is not to compete directly with silicon applications, but to fill a new market space enabled by low-cost manufacturing. This is similar to the creation of the smart tablet market by the introduction of Apple's iPad. The key components of low-cost manufacturing are low-cost materials and process technology. These components limit process parameters, such as maximum temperature and thermal budget, which affect resultant film quality and ultimately device performance. Conventional CMOS electronics use single crystal silicon wafers as the starting substrate. These silicon wafers have high thermal stability, able to endure temperatures above 1000C, but are relatively expensive compared to glass and plastic. A 6" diameter doped prime wafer costs about $30, equivalent to a cost per area of $1.05/in^2 [6]. In stark contrast, a 3"x1" soda lime glass slide costs $0.40, or $0.13/in^2, but is stable only up to 550C [7]. Furthermore, PET plastic substrates, stable up to 150C, costs $0.02/in^2, nearly

1.5 orders of magnitude less than Silicon [8]. PEN plastic substrates, stable up to 220C do exist and presumably cost more than PET, but commercial prices could not be found publicly [9]. There exists a clear trade-off between maximum processing temperature of the substrate and cost per area of the substrate. By lowering the process temperature and thermal budget, substrate cost is drastically lowered.

Inexpensive starting substrate is only part of low-cost manufacturing; Low-cost process technology is the other essential piece. For example, it would be nonsensical to pattern cheap plastic substrates by expensive photolithography. High cost of processing would erode the cost benefit of using inexpensive substrates. Solution processing and printing are the enabling methods of low-cost process technology. Solution processing here-in refers to the methods of materials preparation and processing, whereas printing refers to the delivery and patterning of said materials to substrates. Solution processing encompasses use of polymer, small molecule precursor, or nanoparticle solutions to form continuous functional thin films on the substrate. This avoids costly high vacuum and high temperature steps such as evaporated deposition of films, chemical vapour deposition of thin films, and thermal annealing of deposited films. All of the described solutions can be cast and dried into continuous films. Small molecule precursors and nanoparticle solutions will require a thermal annealing step to convert the material into an active state. However, these annealing temperatures (<400C) are usually much lower than those used in CMOS processing (500C-1050C). In fact, nanoparticle films exploit the phenomena of melting point depression to lower the sintering temperature at which discrete particles fuse into thin films. This has been demonstrated in Gold and Silver nanoparticle thin films, where the conversion temperatures are significantly lower (<250C) than the bulk melting temperatures of the elements (1000C) [10][11].

The use of low-cost solution processing techniques does not imply the use of low-cost patterning techniques such as printing. To illustrate this difference between solution processing and printing, consider the photolithographic patterning of a sintered nanoparticle film. The layer was deposited via inexpensive solution processing, but patterning was done by costly lithography. The attractive benefits of printing are use of arbitrary substrates, all-additive processing, obviation of photolithography, and roll-to-roll processing.

Conventional CMOS processing requires the use of high quality single crystal silicon as starting material, because the wafer serves as the mechanical substrate and the active material of devices. In printing, the active materials are dispensed from prepared inks, and ideally can be deposited onto any arbitrary substrate, such as inexpensive glass or plastic. The all-additive processing reduces waste of precious materials that is requisite in photolithographic patterning of blanket deposited layers. For example, when patterning gold metal lines with a bright-field mask, a large fraction (>50%) of the blanket layer will be etched away into chemical waste. In printing, inks are deposited only where needed. Obviation of photolithography avoids the associated high costs of resist materials, waste abatement and mask manufacturing. Roll-to-roll processing ideally provides very high throughput. To illustrate this, one possible embodiment of an ink-jet printed system is shown in FIG 1-5. The continuous flow process line begins from an initial roll and terminates in a final roll. Various functional layers are dispensed at different points in the process through printing.

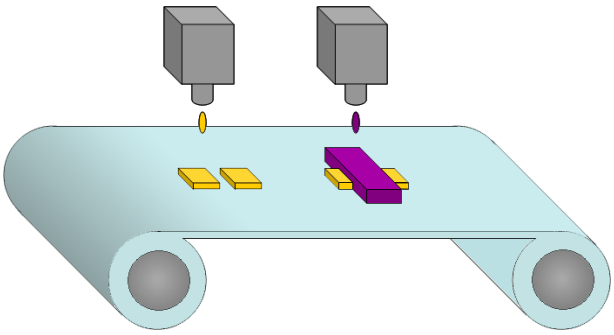


FIG 1-5: Ink-jet Printing System

Inkjet printing and gravure printing are the two methods proposed for patterned deposition of solution processed material inks. Gravure transfers inks from patterned rolls onto the substrate, whereas inkjet dispenses inks from nozzles onto the substrate. Gravure is similar to the roll-based process used to print newspapers and magazines. The use of rolls facilitates very fast throughput, but requires the fabrication of a roll per printed pattern. This is similar to the fabrication of a chrome mask per pattern in photolithography. In contrast, inkjet printing has slower throughput than gravure, but more patterning flexibility. Ideally, any type of pattern can be printed by translating an inkjet head across a substrate. Because of these differences, gravure is better suited for high volume manufacturing while inkjet is better suited for rapid prototyping.

The use of plastic substrates and solution processing constrains the process parameters and types of materials that can be used in printed electronics. Maximum process temperature is about 150C for polyethylene terephthalate (PET) plastic substrates. This temperature cap and the solution processing requirement necessitate the formation of polycrystalline and amorphous layers. The majority of printed electronics research has focused on the development of printable passive components such as inductors and capacitors, and active transistor devices under such process constraints. For example, loop inductors and capacitors have been fabricated by printing polyimide and sintered gold nanoparticle layers [12]. All-printed transistors have been fabricated using pentacene as the active layer, poly(4-vinylphenol) polymer as the gate dielectric, and sintered nanoparticles as the source/drains [13][14]. To support this device research, there have many efforts to develop better solution processable semiconductors [15][16][17].

There have been fewer numbers of studies on printable non-volatile memory devices. The constraint of using polycrystalline and amorphous semiconducting films excludes flash memories. Flash requires high mobility single crystal materials to facilitate hot carrier injection and tunneling of electrons for programming. This has motivated exploration of alternative memory technologies to flash in the literature for printable electronics. Mattis fabricated a stacked organic anti-fuse programmable read only memory (PROM) array on plastic [18]. The pentacene semiconductor and poly(4-vinylphenol) (PVP) dielectric layers were spun-cast. While this demonstrated a solution processed memory, the anti-fuse cells were one time programmable and could not be erased. Ng et al have demonstrated a rewriteable solution processed Ferroelectric Field Effect Transistors (FeFETs) as non-volatile memory cells [19]. The

ferroelectric and semiconductor layers were deposited by spin-casting. However, these devices suffer from poor data retention and large cell size as a fully printed FET. Hackett et al have recently used a sol-gel method to deposit TiO_2 as the electrolyte layer in a rewriteable resistive-switching memory [20]. Remarkably, all processing was conducted at room temperature on plastic. Although the geometric feature sizes of devices were large at about 2 mm, the devices showed good switching and retention characteristics. This resistive switching type of memory appears to be very promising for printed electronics.

1.2: Resistive Switching Random Access Memory Background

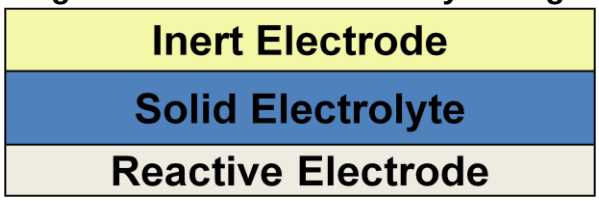


FIG 1-6: Sample Cross-section of Resistive Switching Random Access Memory

The needs and constraints for a replacement to flash memory and for a printable rewriteable non-volatile memory have been described in the previous sections. RRAMs have been attracting attention to fulfill both roles. This technology encompasses a broad array of switching materials and mechanisms. These RRAMs are all implemented as two-terminal vertical devices that show resistance change depending on the voltage bias. An archetypal device is illustrated in FIG 1-6. General attractive features of RRAMs are high scalability and low voltage operation. Scalability facilitates high cell density and storage capacity. The current market drivers for non-volatile memory are portable electronic devices such as smartphones and netbooks that require high storage capacity and low voltage and low power operation. In printed electronics applications such as RFID tags powered by inductive coupling, voltage and power supply are also limited. The characteristics of RRAMs match well to the requirements of these portable electronics and low-cost printed electronics applications.

RRAMs provide some benefits and complements with conventional CMOS processing and printed electronics. The scaling of RRAMs, as current driven devices, instead of field effect devices, is constrained by a different set of principles than flash. The cell geometry is simpler as a two terminal device, instead of a three terminal device. The overall scaling geometry is not limited by the tunnel oxide thickness. As vertical devices, these RRAMS can be fabricated as minimal feature size contact plugs in a cross-bar array. Most of the RRAM technologies use polycrystalline materials and can be fabricated in CMOS backend processes under 500C. This allows stacking over the first silicon layer, and increases device density in 3D volume, not just 2D area. Although 3D integration has been proposed for NAND flash, the high temperatures required to epitaxially grow single crystal silicon and activate dopants severely constrains the thermal budget of cell layers formed on top of the first silicon layer. Using solution processing techniques, process temperatures may be reduced below 200C, which is compatible with both CMOS backend processes and plastic substrates for printing. The operating voltages of these RRAMs depend on the particular switching mechanism.

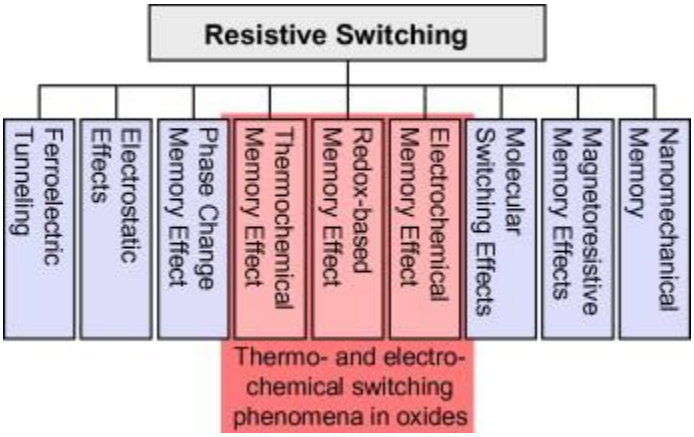


FIG 1-7: Resistive Switching Mechanisms [21]

There are many different classes of RRAMs that use different physical phenomena for switching. Waser has classified these into nine broad categories [21]. These devices are further classified into unipolar and bipolar switches based on their operation. The SET or program operation is defined as transitioning the cell from a high to low resistance state. The RESET or erase operation is defined as transitioning the cell from a low to high resistance state. Additionally, some devices use a filamentary switching mechanism and require an initial forming step to grow the first filament. Unipolar devices SET and RESET under voltage biases of the same polarity. Bipolar devices SET and RESET under opposite polarities. These differences are illustrated in FIG 1-8.

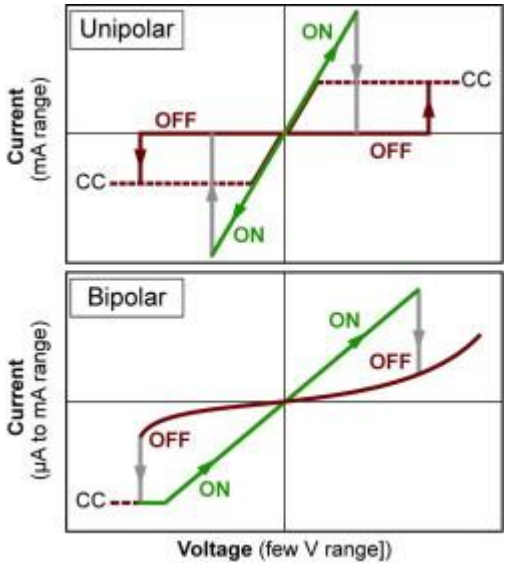


FIG 1-8: Unipolar vs Bipolar switching. Reproduced from reference [21]

Phase change (PC) memories are among the most popular type of RRAMs, currently being commercialized by Intel and Samsung. The resistance change results from transitioning the storage element between a crystalline and amorphous state. The cell has a lower resistance in the crystalline state than the amorphous state. A typical phase change cell will resemble the

device in FIG 1-6, but with a resistive heater in series with the storage element. The cell is RESET from a conductive to resistive state by heating the PC material above the melting temperature (T_m) and then rapidly quenching before the material can crystallize. The device is SET to a conductive state by heating and dwelling above the glass transition temperature (T_g), but below the melt temperature (T_m).

The crystallization kinetics of the material, which is related to mobility of compound elements, affects the retention, reliability and switching speed of the PC RAM. Large kinetic barriers that correspond to long crystallization times would result in slow switching speeds, but high retention of the amorphous state. Lower kinect barriers and shorter switching times would result in faster switching, but higher susceptibility to spontaneous crystallization and false SETs. The crystallization time must also not be so short that the temperature of the cell cannot be quenched rapidly enough to lock in the amorphous state.

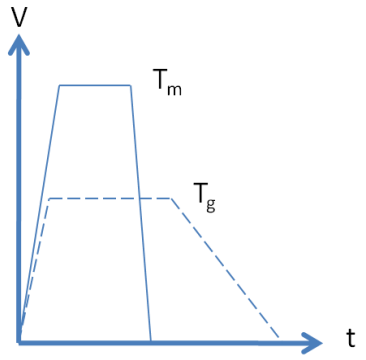


FIG 1-9: SET (solid) and RESET (dash) Voltage profile

A critical enabling characteristic of these devices is the presence of threshold switching during the SET operation, illustrated in the IV curves in FIG 1-8. Without this abrupt reduction in resistance, very high voltage would be required to deliver enough power to heat the highly resistive amorphous PC material. The source of this threshold switching may be crystallization by filamentary instabilities, or higher current that results from avalanching breakdown [22]. Uttecht et al observed these crystalline filaments forming optically from the amorphous material as early as 1970 [23]. The filaments were formed between two Tungsten Carbide electrodes and were initiated at the anode. The precise mechanism of this filamentary crystallization is still under investigation.

Commonly used PC RRAM materials include ternary chalcogens, composed of elements from groups V and VI of the periodic table. Germanium Antimony Telluride (GST) is one of the commonly explored PC materials, well-known from use in (compact disc-rewritable) CD-RWs. The operating principle of CD-RWs is similar to PC RRAM, whereby data is recorded as amorphous and crystalline domains on the CD surface. However, in a CD-RW, the state is read optically by measuring reflectivity, rather than electrically by measuring resistance. Although both technologies exploit differences between amorphous and crystalline states, features that facilitate optical differences may not be suitable for solid state memory. For example, optical contrast between the amorphous and crystalline states results from a large difference in mass

density (7-8%) [24]. Such a volume change during switching may cause de-lamination and cracking of the PC material in a solid state RRAM cell.

PC RRAMs have been considered as a possible replacement for NOR flash memory but not NAND flash due to high power consumption during switching. The temperature-based mechanism requires high current and power, comparable to the hot-electron injection mechanism used in NOR flash. Despite comparable power consumption, PC RRAMs can offer some advantages over NOR flash. For example, when implemented in a cross-bar array, each cell can be individually programmed and erased, unlike NOR flash cells which must be erased in blocks. This can simplify memory management as controllers can write and erase data as needed, instead of waiting for the latency of a block erase procedure. Furthermore, Intel has recently demonstrated multi-bit operation in PC RAM which increases effective bit density, just like multi-bit operation in NOR and NAND flash memory.

The scaling of PC RRAM is affected by different physical mechanisms than Flash. Studies show that as the PC material volume is scaled down, T_m decreases while T_g increases [25]. The melting point depression as a function of domain size is well-known and has been applied to sinter gold nanoparticles far below the bulk melting temperature [10]. This reduces the necessary RESET voltage, and increases the stability of the amorphous RESET state. The increase in glass transition temperature may be caused by lower entropy of a smaller volume, and would stabilize the RESET state. These scaling effects could increase stability of individual cells. However, thermal disturb between cells during SET and RESET operations will limit the scaling of PC RRAM devices in an array. Heat generated during those operations may cause adjacent cells to spontaneously crystallize. Current simulations show that this thermal disturb issue becomes important around 65 nm, well behind the current NAND pitch, which calls into question the viability of this technology as an eventual NAND replacement [26].

1.3: Cationic Electrochemical Resistive Switching Random Access Memory

The cationic electrochemical metallization (ECM) RRAM is a memory that can avoid the thermal disturb issues of PC RRAMs. This is the type of memory technology studied in this dissertation. In the literature, it has also been named as Programmable Metallization Cells (PMC), and Conductive Bridging RAM (CB RAM). The switching mechanism is the controlled formation and dissolution of a metal filament. A schematic of the cell and operation is illustrated in FIG 1-10. A device consists of three layers, an inert electrode, solid electrolyte and reactive electrode. The inert electrode is usually a high work function metal like platinum or gold. The solid electrolyte is ideally a pure cationic conductor with no electrical conductivity. The reactive electrode serves as a cation source. In this dissertation, Ag_2S is the solid electrolyte, silver is the reactive electrode, and gold, platinum or tungsten is the inert electrode.

As a filament memory, an initial forming step is required to form the first filament that serves as the template for subsequent switching. Subsequently, in order to SET from a resistive to conductive state, the inert electrode is biased as the cathode, and the reactive electrode as the anode. Metal will oxidize from the reactive electrode forming cations, and the resultant cations will migrate through the electrolyte, reducing and depositing on the inert electrode.

Due to non-uniform deposition, a metal filament will form, providing a low resistance path for the current between the electrodes. To RESET to a high resistance state, the inert electrode is biased as the anode and the reactive electrode as the cathode. The metal filament will oxidize and re-dissolve, depositing on the reactive electrode.

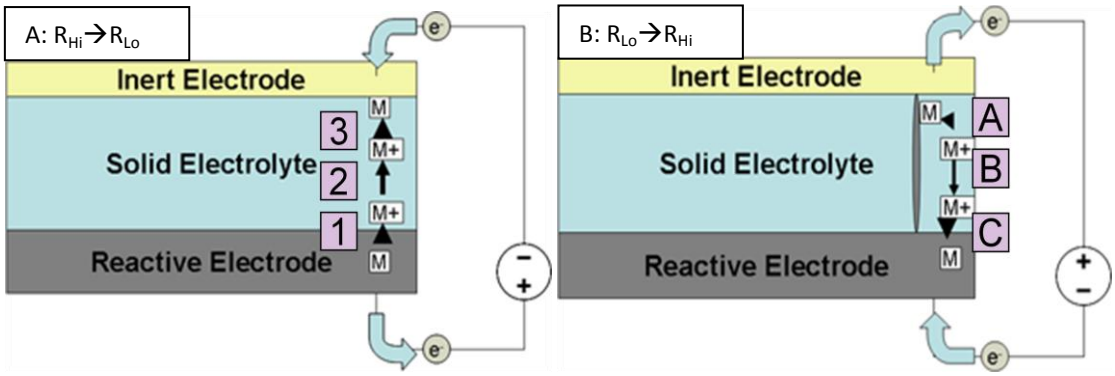


FIG 1-10: ECM Cell Operation A) Program B) Erase

There are several potential benefits offered by ECM RRAM over flash and PC RRAM: scalability, low power operation, reduced disturb, and fast read speed. The physical limits for floating gate NAND scaling are set by the minimum tunnel oxide thickness to maintain data retention, minimize capacitive cross-talk between adjacent rows of cells, and maintain the gate coupling ratio. These are all related to the field effect nature of NAND flash transistors. The physical limits for PC RRAM scaling are related to thermal disturb, which arise from its temperature based operation. In contrast to NAND and PC RRAM, ECM RRAMs are current driven devices. DC ionic current must flow to form metallic filaments that cause the resistive switching. Lateral scaling of the electrolyte dimension will be limited by the number of metal atoms needed to form a conductive metal path. Terabe et al have demonstrated this limit in a quantized conductance atomic switch which resolved conduction from contributions of single atoms across a vacuum gap [27]. When the cells are implemented as contact plugs in an array, the minimum pitch between cells is limited by electronic tunneling current through the interlevel dielectric (ILD), not capacitive cross-talk. Formation of the filaments requires flow of DC ionic and electronic current, not virtual capacitive current. Additionally, ECM RRAMs may be 3D stacked to further increase bit density.

The low power operation of ECM RRAMs arises from the electrochemical nature of the device. Switching is caused by a series of 3 processes: electrochemical oxidation of the anode generating metal cations, migration of resultant cations through the electrolyte, and reduction on the cathode. An initial forming step bridges the two electrodes. Subsequent growth and dissolution occurs near the tip of the filament. This switching requires less energy and is faster than the initial forming. The electrochemical reactions that facilitate filament formation are driven by voltages on the order of volts. Chapter 6 will describe filament forming experiments in further detail and show how filament forming time and morphology depend on the method and magnitude of applied bias (step input versus sweep input).

The metal filament of the SET state facilitates fast read speed of the cell. The latency of data access in memory chips consists of address decoding delay, word line activation delay, bit line sensing delay and output driving delay. The word line activation and bit sensing delays are related to the memory core which is the array of cells. The address decoding and output driving delays are related to the peripheral circuitry which drive input and sense output from the core. Address decoding delay is the time required to transmit addresses and data from input/output (IO) pins of a chip package to the memory core. Conversely, output driving delay is the time needed to detect and propagate data from sense amps at the periphery to the IO pads on the package. Address decoding delay is independent of the core and neglected, but output driving delay will depend on the effective R_{off}/R_{on} ratio of the selected core cell. This delay will be further discussed after first considering delays intrinsic to the core memory array.

The word line activation delay and the bit line sensing delay are respectively the time required to drive the word line to a certain voltage, and the time required to propagate the cell data to the sense amplifier input. These two delays are intrinsic to the core and as RC delays, will depend on the type of memory cell. A layout and circuit schematic illustrating the components of these core delays is shown in FIG 1-11. 'r' is an incremental resistance, 'c' is an incremental capacitance, and 'R' is the variable resistance of the RRAM. The voltage driver must charge the parasitic capacitances of the word line and bit line of the selected cell. The elmore delay of this circuit, described in Equation 1-3, will set the read speed of a cell. Further note that the delay of a cell will depend on its position relative to the voltage driver and sense-amp.

$$\tau = x^2 \cdot rc + (L - x)^2 \cdot rc + (R + y \cdot r) \cdot yc$$

Equation 1-3: Elmore Delay of Memory Core

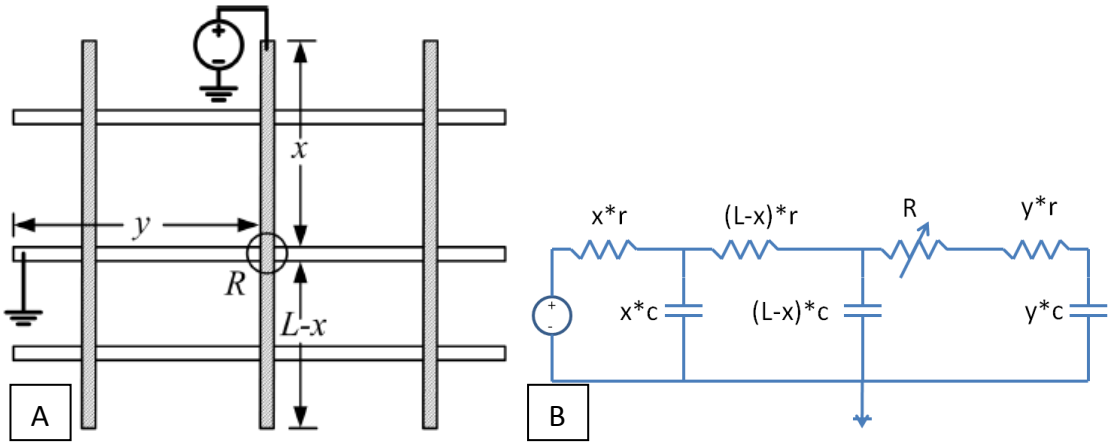


FIG 1-11: (A) Layout of crossbar core with one selected cell (B) Circuit Schematic of path from driver (voltage source) through selected cell to sense amp (ground) [28]

The cell located furthest from the driver and sense amp (x=L, y=L) will have the worst case delay. Although the longest possible delay occurs when this cell is RESET to R_{off}, the limiting delay of a single level cell occurs when it is SET to R_{on}. Because of the binary data, the memory

core needs only be read long enough to identify whether it is in the SET state. Otherwise, it must be in the RESET state. A similar shortcut exists for multi-bit cells. The limiting delay of the cell is not set by the largest R_{off} state, but the second largest R_{off} state.

Material	Resistivity (Ω*m)
Copper	1.67E-8
Silver	1.54E-8
Tungsten	5.28E-8
GST [29]	1E-4
Silicon (single crystal)	
*P-doped [1E18]	2E-4
*P-doped [1E19]	5.4E-5
Polysilicon	
*P-doped [1E18]	2E-3
*P-doped [1E19]	5.4E-4

Table 1-1: Resistivity of Various Materials. Due to lower electron mobility, resistivity of polysilicon is estimated to be 10 times higher than that of single crystal.

This limiting core delay can be separated into two components: the memory cell, and array of the WL and BL. Given resistivity values, such as those in Table 1-1, it is possible to estimate limiting delays for ECM RRAM, PC RRAM and flash memory. The estimated delays for each of these technologies will depend on the geometry and materials used. For example, ECM RRAM uses metallic WL and BL, while PC RRAM uses one metallic WL and one polycrystalline BL. To standardize comparison across these technologies, the line length of the WL and BL are considered in 60 nm increments. The nominal dimensions of the BL and WL are 60 nm line width and 40 nm thickness. To estimate the cell delay, the effective filament and phase change volume of ECM RRAM and PC RRAM is estimated as a cylinder of 10 nm diameter and 40 nm height.

The cell delay of a flash memory is modeled as an 'rc' delay of the channel resistance driving the WL capacitance of a single gate stack. Channel resistance is approximated as the resistance of a 60 nm wide x 60 nm long x 10 nm thick doped silicon layer. The gate stack of the cell is estimated as a series capacitor pair, representing the IPD and T_{ox} capacitances. IPD and T_{ox} thicknesses are set to 30nm and 20nm respectively to maintain a gate coupling ratio (GCR) of 0.6. Estimated values for line and cell delay are computed and displayed in the table below.

Parameter	***ECM RRAM***	***PC RRAM***	***Flash Memory***
WL material	Silver	Tungsten	Polysilicon (1E-19 P Dope)
BL material	Tungsten	Polysilicon (1E-19 P Dope)	Silicon (1E-19 P Dope)
WL Delay per 60 nm (s)	1.19594E-18	4.1E-18	3.35486E-14
BL Delay per 60 nm (s)	4.10038E-18	4.19E-15	5.03229E-15
Cell Delay (s)	2.43636E-17	1.58E-13	5.03229E-15

Table 1-2: Estimated cell and WL, BL delays

Immediately observable from the table is that cell delay of the ECM RRAM is much shorter than either PC RRAM or flash due to very low resistance of the on-state. The line delays of silicon can be significantly longer due to the higher resistivity. Thus, the lower resistance enables fast reads by reducing RC delay through the memory core.

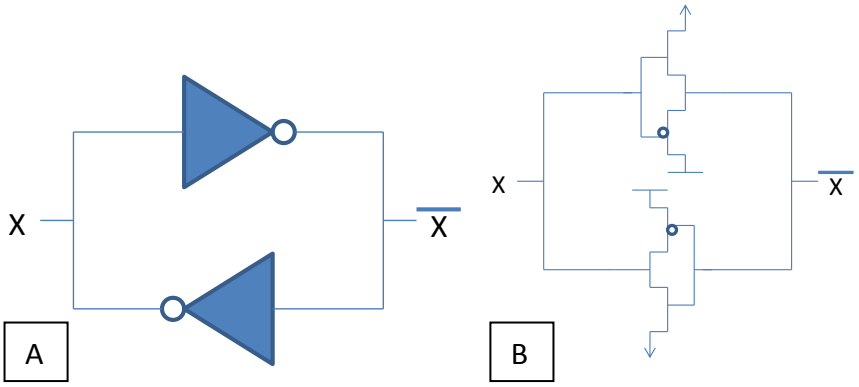


FIG 1-12: Cross-coupled inverter pair used in Sense Amplifiers
(a) Schematic using components (b) Schematic using circuit elements

An additional component of the delay is the time required by the sense amplifiers to detect the data state of the core memory cell. These sense amps are usually differential amplifiers that operate through a regenerative feedback mechanism describable by a pair of cross-coupled inverters, shown in FIG 1-12. This regenerative feedback is a positive feedback loop that amplifies a difference in voltage applied at the inverting inputs. For example, consider a small voltage difference initially applied between x and x-inv. If x > x-inv, it turns on the NMOS in the top inverter which pulls down x-inv. This further turns on the PMOS in the bottom inverter which pulls up the initial x. The process iterates again by pulling down x-inv at a faster rate since the overdrive voltage ($V_{gs} - V_t$) of the top pull down NMOS is now higher. As the process iterates around the inverter loop, this feedback accelerates until the inputs rail at the supply and ground voltages. Larger initial voltage differences across the inputs will cause the outputs to hit the rails at a faster rate due to higher current driving the pull-up and pull-down transistors of the cross-coupled inverters. The use of larger initial voltage differences therefore result in faster read times.

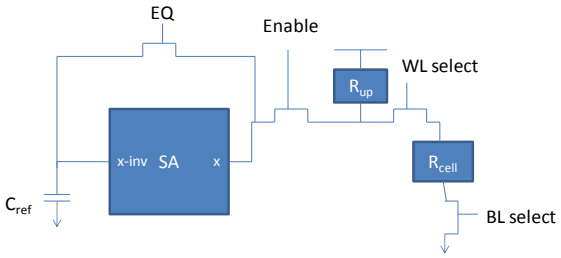


FIG 1-13: Sample implementation of read circuit

In a non-volatile memory array, there is no inverting output pair to feed into the inverting and non-inverting input. Thus, the sense-amps must be used in a single-ended configuration whereby one input is connected to the bit line, and the other input is connected to a reference

value. This is illustrated in FIG 1-13. In standard operation, the WL and a reference capacitor is pre-charged and equalized to the reference voltage at the sense amp inputs. The sense amp input is then connected to the selected cell and pull up network. The WL will discharge through the cell if it is conducting, generating a voltage difference with the reference value that will be amplified by the sense-amp. ECM RRAMs which have highly conducting ON states can quickly discharge the WLs to generate this voltage difference.

1.4: Limitations of Leakage Sneak Paths in Crossbar Arrays

As described previously, larger initial voltage differences across the sense amp inputs cause faster read operation. The maximum voltage difference in RRAMs is set by the R_{off}/R_{on} ratio. Ideally, the ratio detected from the core array is equal to the ratio of the cell. Realistically, parasitic sneak paths drastically reduce the effective R_{off}/R_{on} ratio that is detected from the array. These effects not only reduce read speed, but can also constrain the array size of the core.

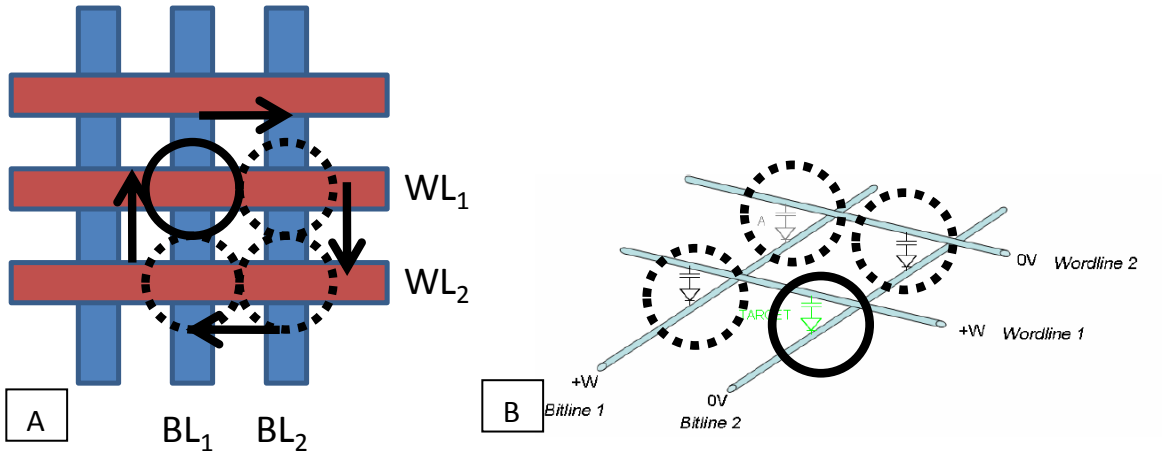


FIG 1-14: Sneak Path Illustration. Selected cell is solid circle. Unselected by programmed cells are dotted circle. (A) Parasitic sneak-path circumvents selected cell without steering elements. (B) Steering elements prevent flow of current through sneak-path [30].

The concept of the sneak path is illustrated in the simple cross-bar structure in FIG 1-14A. In this example, 3 SET cells form a parasitic current path to circumvent the selected cell. This may result in a false read of a RESET cell as a SET cell. To avoid this problem, a steering element such as a diode must be placed in series with each element of the array as shown in FIG 1-14B. The diode breaks the path by preventing reverse current flow from BL_1 to WL_2. Although conventional diodes work well as steering elements for unipolar devices, the ECM RRAM is a bipolar device. A more complicated steering element such as a Zener diode is required to facilitate bipolar functionality.

Alternatively, Linn has proposed a pair of back-to-back ECM RRAMs that act as self-steering elements (FIG ***1-15***). This complementary resistive switch (CRS) may be analyzed by treating the series RRAMs as a voltage divider. Initially the top device is SET, and the bottom device is RESET. The majority of applied bias will fall across the highly resistive bottom device. As applied voltage is increased, a filament will form in the bottom device transitioning it to the SET

state ($V_{th,1}$). As the voltage is increased further, the top device will be RESET ($V_{th,2}$). The devices may then be similarly switched by reversing the bias.

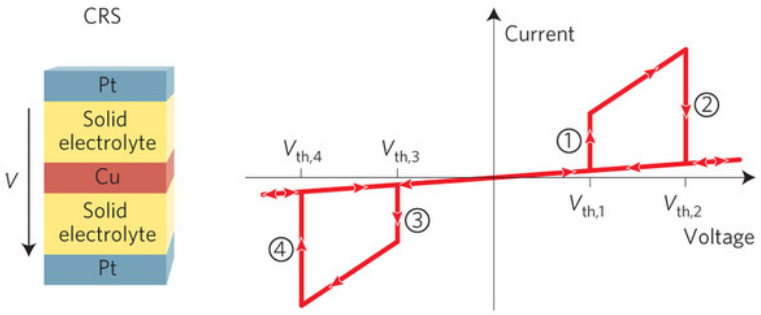


FIG* 1-15*: Complementary Resistive Switch [31]

Although steering elements reduce current through sneak paths, there still exists finite leakage current through the cell. As arrays are scaled up, the cumulative effect of all this leakage will affect operation. The total number of sneak paths through programmed bits can be calculated, given a distribution of programmed bits [30]. For example referring to FIG 1-14, 3 additional programmed bits are needed to complete a sneak path in an array of x word lines and y bit lines. Starting from the selected word line, there are $(x-1)*P_x$ programmed bits, where P is the probably of that a bit along the word line is programmed. For each bit line, there are $(y-1)*P_y$ programmed bits. To complete the circuit, the last bit will have a probability P_b of being programmed. The total number of leakage paths is then: $(x-1)*P_x*(y-1)*P_y*P_b$. The total fraction of leakage paths relative to array size is: $(x-1)*(y-1)/(x*y)*P_x*P_y*P_b$. In the limit of large arrays, this fraction will be $P_x*P_y*P_b$. If all these probabilities are uniformly 50%, then the fraction of leakage paths will be 12.5%. This number increases with a higher density of programmed bits. The limit of array size is then a function of number of programmed bits, leakage current per cell, and the ON current of a cell. When the product of the number of sneak paths and leakage current exceeds the ON current threshold, then read errors will occur. Without the use of steering elements, the array size would be severely constrained since the leakage current equals the ON state current. Although they are not the focus of this dissertation, research into novel steering elements and schemes will be necessary to facilitate the development of cross-bar RRAMs.

1.5: Oxide Based RRAMs

The benefits of scalability and low power operation ascribed to ECM RRAMs also apply to a broad class of oxide-based RRAMs. The switching material of these devices is a solid transition metal oxide such as $SrTiO_3$, TiO_2, NiO, Ta_2O_5 and ZnO. Instead of lumping all of these RRAMs into one oxide-based category, they should be further classified by the switching mechanism, which depends on the switching material and contact materials. For example, ZnO can operate either as a unipolar switch when using two inert contacts, or bipolar switch, when using at least one silver contact. Additionally, the mechanism affects the form of the conducting state. This state may show pad-size dependence indicating an area switching effect, or pad-size independence indicating a filamentary switching effect. Waser has reviewed three main switching mechanisms of oxide-based RRAMs that use redox chemical effects: electrochemical

metallization (ECM), valency change mechanism (VCM), and thermo-chemical mechanism (TCM) [21][32].

The electrochemical metallization effect has already been described previously. It requires the use of two asymmetric contacts: one inert metal such as platinum and one reactive metal of either silver or copper. These two reactive metals are typically used because their cations are unique in being highly polarizable, and able to deform under stress. This facilitates migration through interstitial sites of the solid electrolyte [33]. This transport is analogous to squeezing a soft rubber ball versus a hard metal ball through the small spaces between interstitial sites. During the SET operation, the reactive metal is oxidized from the anode into cations. These are injected into the electrolyte and migrate towards the cathode where they are reduced, growing a metal filament that that bridges the two electrodes. During the RESET operation, the polarity of the voltage is reversed and the reactive metal becomes the cathode, and the inert metal becomes the anode. The metal filament electrochemically dissolves returning the device to a resistive state. This results in bi-polar filamentary switching. The combination of silver or copper electrodes and bipolar switching is a strong indicator of this ECM mechanism. Solid oxides that can operate this way include ZnO, Al_2O_3, and SiO_2 [32].

The valency change mechanism (VCM) is based on modifying the valence state of the transition metal cations in a material. It is similar to ECM whereby redox reactions at the electrodes and ionic migration through the bulk facilitate resistive switching. However in VCM, oxygen vacancies instead of metal cations are the mobile species. This mechanism results in bipolar switching behavior that may be filamentary or areal in nature. The oxygen exchange reaction in Equation 1-4 describes how oxygen within the material interacts with the surrounding environment.

$$O_O = {}^{1}\!/_{2}\, O_{2(g)} + V_O^{\cdot\cdot} + 2e'$$

Equation 1-4: Oxygen Exchange Reaction

The filamentary bipolar switching is very similar to the ECM. To form the initial SET filament, one electrode is biased as the cathode, and one electrode is biased as the anode. The cathode attracts oxygen vacancies and partially blocks the oxygen exchange reaction, causing accumulation of cationic vacancies. The transition metal cations in this region will trap electrons from the cathode, increasing the local conductivity and forming a conductive virtual cathode. As time proceeds, the vacancy rich region grows towards the anode as a filament (similar to the the metal filament growth in ECM). When this filament connects with the anode the, device becomes conductive. At the anode, the partial oxygen exchange causes evolution of oxygen gas and injection of vacancies into the electrolyte to compensate the cathodic reaction. During the RESET operation, the polarity of the electrode biases is reversed, causing dissolution of the vacancy rich filament. This vacancy based filament mechanism has been verified in $SrTiO_3$ by conductive AFM studies, and in TiO_2 by X-ray and TEM studies [32][34]. Furthermore in TiO_2, the collection of oxygen vacancies causes the formation of a conducting oxygen deficient compound Ti_4O_7 that comprises the conductive filament. Strong indicators of

filamentary VCM are pad-size independent on-state resistance, and bipolar switching using two inert contacts.

In addition to filamentary switching, some devices exhibit areal switching in which ON-state resistance depends on the electrode area. Although the migration of oxygen vacancies also drives this switching, it is limited to a narrow spatial region near the electrode contacts. The change of oxygen concentration modifies the injection barrier at the contact, resulting in resistance change. Meyer et al have fabricated such a device by using a bi-layer oxide switching element consisting of a thin tunnel oxide and thick conducting oxide, as shown in FIG 1-16 [35]. The specific materials were withheld from the publication. FIG 1-16B illustrates operation of the device. To RESET the device into a resistive state, oxygen anions are injected into the tunnel oxide under high bias. This creates an electrostatic barrier to electron flow. To SET the device to a conductive state, the oxygen anions are extracted, reducing the barrier. There are fewer systems that exhibit this type of switching. At the biases used to switch RRAM devices, inherent instabilities favor the formation of filaments. Additionally, more engineering and precision is needed in the fabrication of the types of multi-layer switching materials illustrated in FIG 1-16A, than for single layer devices.

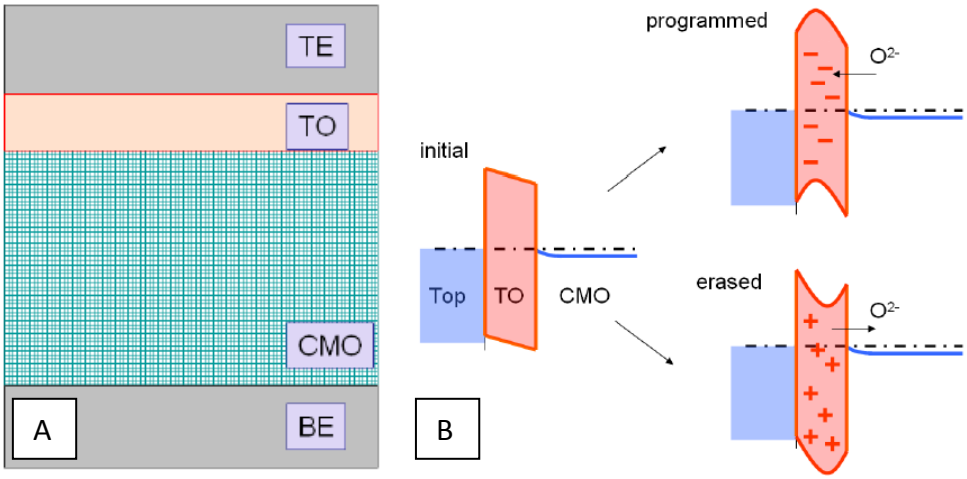


FIG 1-16: A) Bi Layer Areal Switching Device B) Proposed Switching Mechanism [35]

The ECM and VCM both use ionic migration and filamentary formation to facilitate bipolar switching. In contrast, the thermo-chemical mechanism (TCM) uses partial dielectric breakdown and joule heating to facilitate unipolar switching. Its operation closely resembles fuse-antifuse memories, whereby filaments are formed under low current, and annihilated under high current. A sample IV curve of a unipolar RRAM is illustrated in FIG 1-17. As a filament memory, a forming step is required to create the first filament. The conductivity of this initial filament is set by the current compliance. This filament may be composed of the electrode metal or the decomposed oxide. The oxygen vacancy mechanism described for VCM can cause formation of the decomposed oxide filament. A joule heating mechanism can cause the formation of the electrode metal filament [30]. The filament formation by the joule heating mechanism occurs in several phases [30][36]. During Phase I, electronic current flows via a

percolation path grain boundaries. In Phase II, as current flow increases, joule heating causes thermal expansion of this region. In Phase III, the high temperature causes melting of the electrode metal and draws in material forming a conductive filament partly composed of electrode metal thermally decomposed oxide material.

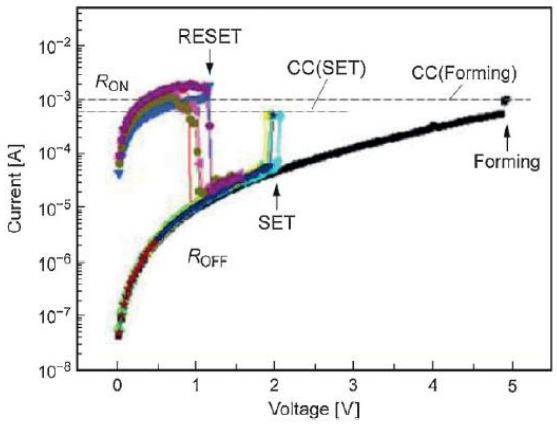


FIG 1-17: Unipolar Switching Characteristic of Pt/NiO/Pt RRAM [32]

After this initial forming step, the device can be RESET by applying a lower voltage bias without enabling current compliance. Higher current will flow through the conductive filament, and subsequent joule heating will rupture the filament resetting the device to a resistive state. It may be SET to a conductive state again at a voltage higher than the RESET voltage, but lower than the forming voltage. This suggests that the conductive path is reformed along the previous filament instead of along a new filament.

Three main switching mechanisms for oxide-based RRAMs have been reviewed. Although these have been described in isolation, a combination of these effects may occur during switching. For example, in an Ag/ZnO/Au device, resistive switching may occur by ECM (injection of silver), and VCM (decomposition of ZnO). To carefully de-convolute these mechanisms, switching materials and contact materials, along with bias conditions should be carefully selected.

1.6: Application of ECM RRAMs to Reconfigurable Logic

Having distinguished oxide-based RRAMs and the subclass of ECM RRAMs, an additional application specific to ECM RRAMs will be discussed. While all RRAMs are generally scalable with minimum cell area ($4F^2$ cell), the ECM RRAM cell in particular has fast read speed because of its metallic SET state. The combination of this highly conductive SET state and small cell size makes ECM RRAMs attractive for use in Reconfigurable Logic. The prototypical embodiment of this application is the Field Programmable Gate Array (FPGA), an integrated circuit that can be reconfigured by the end-user, independent of the manufacturing setting. This enables end-users to implement various logic applications using the same chip, without having to invest time and money in designing and fabricating a new Application Specific Integrated Circuit (ASIC) per application. For example, a video decoder and display controller can be implemented using the

same type of FPGA chip. This is especially attractive for prototyping of ASICs and making products that sell in low-volumes or require high customization.

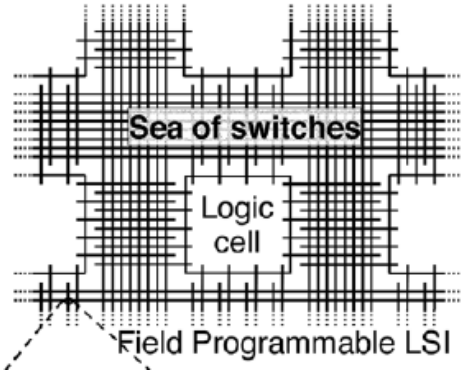


FIG 1-18: Field Programmable Circuit: Logic Cells surrounded by reprogrammable arrays of interconnects [37]

The typical Reconfigurable Logic chip consists of several logic blocks joined by a reconfigurable array of interconnects as illustrated in FIG 1-18. The logic block may either be fine grained or coarse grained. Fine grained blocks offer the highest resolution of control by manipulating operations on the bit-level, but require more area, power and delay to implement. In contrast, coarse grained blocks offer less control by manipulation of standard operations such as addition of groups of bits, but require less area, power and delay. The selection of logic block granularity depends on the available chip area, power and resolution of control desired. The switches of the interconnect array usually consist of an SRAM array controlled by pass transistors. These types of devices occupy large feature area (~$100F^2$) and long RC delay resulting from high on-state resistance [37]. Because of the large foot print of the switch, the switching array consumes a large fraction of the chip area, limiting the remaining area for logic blocks and therefore reducing their resolution or number. Furthermore, the RC delay of the switching interconnect matrix is greater than the RC delay of the logic blocks. The replacement of the SRAM/pass transistor switch by a steered ECM RRAM could greatly enhance the abilities of the reconfigurable logic chip. It would free chip area for the logic blocks, reduce delay and potentially reduce power consumption. The non-volatility of the ECM RRAM facilitates the reduced power consumption. Once programmed, no applied voltages are necessary to maintain the state. Although the SRAM ideally consumes no static power, realistically there will be some finite leakage current that causes static power consumption.

In addition to the speed and size advantage, the filamentary SET mechanism of the ECM RRAM is well suited for interconnect switches. In the reconfigurable array, these switches are reprogrammed a few times, but read many times. The read must be fast (requiring low on-state resistance), but the reprogramming step can be slow. As will be described in Chapter 6, a slow SET operation at low voltage forms a thick filament in ECM RRAMs, in contrast to high voltage which rapidly forms a thin filament. The slow forming produces a more stable and conductive ON-state, but requires a longer time, which is acceptable for this reconfigurable logic application.

Several benefits and applications of using ECM RRAMs have been discussed, however further research on the materials design and understanding of the switching are required. It is the goal of this dissertation to study the interplay between materials processing and microstructure on the operation of ECM RRAMs.

1.7: Objectives

As a device based on ionic transport and electrochemical reactions, the ECM RRAM is fundamentally different than the flash transistor, which is a field effect device. The metrics for nonvolatile memory and limiting factors for flash and ECM RRAMs are listed in Table 1-3. This section aims to compare the different attributes of flash memories and ECM RRAMs.

	Field Effect Device	**Electrochemical Device**
Metrics	**Flash Attribute**	**Ionic Attribute**
Scalability	Cross-talk/tunnel oxide thickness	Limit of Dendrite Formation
Read Time	R-C Elements	R-C Elements
Read Margin	Vt-Window	Filament/Bulk Electrolyte Electrical Resistance
W/E Time	Tunneling/Hot Carrier Injection	Ionic Diffusion/Electrode Reactions
Write Voltage	Cell Geometry	Ionic Diffusion/Electrode Reactions
Retention	Oxide Integrity	Ion Diffusion
Endurance	Oxide Integrity	Electrolyte Composition

Table 1-3: Comparison of Metrics and Limiting Factors for Flash and ECM RRAMs

Scalability of the respective devices has been discussed previously. Read time of devices is limited by RC delay from the cell to the sense amplifiers at the edge of the array. This consists of the time required to charge up the WL and BL to propagate a signal. This will likely be shorter for ECM RRAMs. In flash, the capacitance of all the floating gate transistors connected to the WL must be charged. In ECM RRAM, parasitic capacitance along the WL must be charged. This parasitic capacitance may be less than the gate capacitance of several FG transistors. Additionally, the metallic SET state of ECM RRAM is likely to have lower resistance compared to channel resistance of an ON state FG transistor. The combined lower resistance and capacitance of a SET ECM RRAM should make its minimum RC delay shorter than flash. The peripheral circuitry can poll for this shorter interval, enabling faster read operation in ECM RRAMs.

Read margin of flash devices is determined by the amount of charge that can be stored on the floating gate. This charge affects the threshold voltage of the transistor and is read out via the transistor current. The read margin is defined as the difference in current for a programmed transistor (with charge stored on the floating gate) vs. an erased transistor. As flash devices are scaled down, the amount of charge stored decreases so that they are more sensitive to charge loss (i.e. retention time is degraded). Also, short-channel effects (degraded sub-threshold swing) reduce the read margin. The read margin of ECM RRAM devices is set by

the On/Off resistance ratio. The maximum OFF state resistance is limited by the bulk electronic resistance of the electrolyte. The minimum ON state resistance is set by the maximum size of metal filament formation. The superior technology for this metric has not yet been determined.

The write/erase times of each memory device depend upon the programming/erase mechanisms. Floating gate transistors are programmed and erased through FN tunneling and hot carrier injection of electronic charge. The programming and erase current will set the speed. In ECM RRAMs, the SET/RESET speeds are determined by the rates of ionic diffusion and electrochemical electrode reactions during filament formation and dissolution. Given these different mechanisms, the two types of devices can be implemented differently in arrays. For example, in flash memory, entire blocks of cells are erased in parallel by biasing the channel of all the cells through the substrate. This reduces total erase time and avoids disturb effects that arise from selectively biasing individual cells under high voltages. In ECM RRAMs, implementation of this parallel erase feature will depend on whether the filament dissolution process is self-limiting, or would result in undesirable parasitic electrochemical reactions after the dissolution is complete. However unlike flash, cells may be individually SET/RESET in ECM RRAMs with few disturb effects. The selection of parallel vs bit-wise erase will depend on the application of the memory. For code storage in NOR flash, bit-wise operation is preferred, while for mass data storage in NAND flash, parallel operation is preferred. The operation speeds for both Flash and ECM RRAMs will depend on the applied voltage. A comparison of the sensitivities of write/erase speed versus voltage and power could provide a good metric for the two technologies, but has yet to be quantified and reported.

The write voltage for flash depends on the device geometry and design. For example, high field is required in hot carrier injection programming. Doping profiles can be engineering to produce these fields. The GCR that determines the fraction of gate voltage drop across the tunnel oxide can also be controlled through geometry. This voltage across the tunnel oxide directs hot carrier current into the floating gate during NOR flash programming, and facilitates FN tunneling during NAND flash programming. In NAND devices, a wrap-around gate and high K interpoly dielectric can be implemented to increase the GCR. In ECM RRAMs, the filament formation depends on the applied voltage, ionic conductance of the electrolyte, and rates of electrode electrochemical reactions. Chapter 6 will explore this filament formation mechanism and the trade-offs between the speed and voltage for ECM RRAMs.

Retention and endurance cycling of memory devices depends on the kinetics and thermodynamics of the system. In flash devices, cycling and endurance depend on the integrity of the tunnel oxide, which maintains the potential well for the electronic charge. As the oxide degrades, the ability to retain charge decreases as defects develop. These facilitate trap-assisted tunneling leakage. The endurance of the flash device depends on the degradation rate of the oxide with successive program/erase operations. In ECM RRAMs, the retention of the SET state is dependent on the rate of spontaneous filament dissolution into the electrolyte, assuming that the SET state is the thermodynamically unstable state. The rate of filament dissolution will depend on the diffusion rate and solubility of the metal atoms in the surrounding electrolyte.

1.8: Silver Sulfide as a Model Material

Having discussed various metrics for ECM RRAMs, a test material must be selected to evaluate some of these characteristics. This dissertation uses silver sulfide as a model material to explore the effect of microstructure on mixed ionic-electronic conducting materials, and the filament formation process through these materials. The goal is to develop a framework for evaluating and engineering ionic materials for memory applications with an emphasis on solution processing.

Many solid electrolytes have been implemented in cationic ECM RRAMs. FIG 1-19, reproduced from reference [38] lists several of these. Silver sulfide has been selected as a convenient model material for testing. It was one of the first materials used to develop RRAMs. Terabe et al demonstrated a cross bar switching device consisting of an Ag/Ag_2S/Air Gap/Pt stack [27]. This device showed fast switching and good cycling endurance, indicating the utility of Ag_2S as an ECM RRAM material.

Ag_2S has several desirable traits which include solution processability for printed electronics applications, relative simplicity and stability of composition and structure, and an understood ionic conduction mechanism. It belongs to the class of silver halides and chalcogenides that are among the best known binary solid electrolytes. For example, Silver Iodide is often used as a pure ionic conductor at high temperatures, when it transitions into a superionic conducting state. However, silver halides are also highly photosensitive. Early photographic technology exploited this photosensitivity. The daguerreotype was the first publicly available photographic processes, and used silver iodide as the photosensitive component [39][40]. Compared to the silver halides, Ag_2S has lower photosensitivity. As a binary compound, its composition is simpler than ternary and quaternary compounds such as AgGeS. It has a single stable oxidation state, and exists only as the monoclinic acanthite phase below 179C. Above this temperature, it transforms into the BCC argentite phase until about 600C, at which another phase transition occurs. The simple stoichiometry and phase makes Ag2S easier to process than other materials such as copper (I) sulfide (Cu_2S). That compound is desirable for CMOS compatibility, due to the use of copper interconnects but is vastly more complicated by the two stable oxidation states of copper. At least three compounds (Chalcocite, Roxybyite, and Covelitte) span the stoichiometric range between CuS and $Cu_{2-x}S$. These compounds have different crystal structures and conducting properties that are stoichiometry dependent [41]. Using Ag_2S removes these aspects of variability.

For integration into printed electronics, convenient solution processing methods for Ag_2S via sulfidation and nanoparticles already exist [42][43][44][45]. These existing methods can help reduce process development time. Additionally, a number of previous studies provide basic information on the physical and mixed ionic-electronic conducting properties of the bulk material [46][47][48]. Silver is the only mobile species in the compound; Sulfur sits on a fixed anion sub-lattice. This contrasts with ECM RRAMs that use metal oxide electrolytes. In those materials, the metal cation and oxygen anion can both be mobile, presenting a complicated system for analysis. For further reading, literature on metal corrosion and oxidation provides some tabulated information about the mobile species of various metal oxide materials [49][50].

Using Ag2S also provides an additional benefit because silver is already present in the electrolyte. There will be no parasitic reduction or introduction of oxygen at the cathode during the transient between initial oxidation of silver at the anode and migration to the cathode. Waser et al have demonstrated that oxygen evolution is a failure mechanism in $SrTiO_3$ RRAMs [32]. In that study, the cycling endurance of RRAMs using Pt contacts and W contacts was compared. Endurance of devices fabricated with W pads was higher than Pt pads. When using Pt contacts, discrete bubbles were observed at the surface, suggesting evolution of oxygen gas. No such defects were observed when using W contact pads. It was hypothesized that WO_3 forming on the W pads served as an oxygen reservoir. The use of Ag_2S avoids convolution of other electrochemical reactions during switching studies, and the failure mode of oxygen evolution from decomposition of the electrolyte. Besides, sulfur is a solid that will not evolve from the film should decomposition occur.

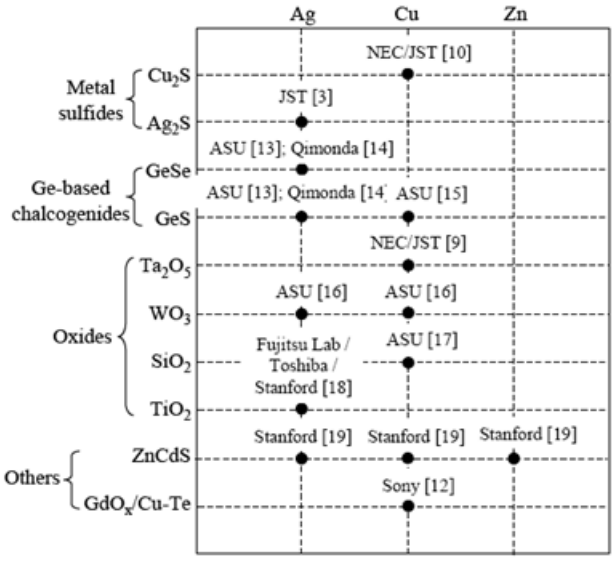


FIG 1-19: Cationic Resitive Switching Materials [38]

1.9: Organization

1.9.1: Independent Contributions

The independent contributions of this dissertation are outlined below.

- Exploration of Solution Processing Methods for depositing Ag_2S
  - Sulfidation of elemental silver films
  - Sintering of octadecylamine (ODA) encapsulated Ag_2S Nanoparticles
  - Sintering of thioglycerol (THG) encapsulated Ag_2S Nanoparticles
- Demonstrating use of sintered nanoparticle thin films to control mixed conducting properties
  - Correlation of materials analysis (XRD, TGA) with Mixed Conductivity (EIS)
  - Understanding effect of encapsulant and synthetic methods
    - ODA-Ag_2S films: Steric hindrance and high boiling point requires high temperature (350C) to cause onset of mixed conduction

        - THG-Ag_2S films: Use of rapid heating forms different grain sizes and affects the mixed conduction.
- Study of Filament Forming Process in Lateral Structures:
    - Effects of operating voltage and stimulus conditions on filament formation are explored.
    - Effects of sintering on mixed conductance and filament formation rate are studied.

1.9.2: Overview

The topics in this dissertation span many different fields from nanoparticle synthesis to oxidation of materials, and defect chemistry. For a good introduction to the solid ionic conductors, one should consult Maier's "Physical Chemistry of Ionic Materials [51]." For understanding nanoparticle synthesis, there are several resources depending on the particular type of material desired. Murray's work provides a concise introduction to the hot-injection method [52]. For impedance spectroscopy, Macdonald's book serves as a useful guide [53].

Chapter 2 provides an overview to ionic conduction in the solid state. Defect chemistry, which quantifies the generation of point defects that serve as ionic charge carriers, is reviewed. A framework that uses Fermi levels to quantify ionic carriers, similar to electronic carriers, is introduced. Interfacial effects on carrier concentration are discussed. This provides basic understanding for interpreting later results.

Chapter 3 covers experimental work on sulfidized silver films. While this method does produce silver sulfide thin films that show resistive switching, high porosity and surface roughness preclude integration into vertical cross bar structures.

Chapter 4 describes sintering studies of ODA-Ag_2S nanoparticle thin films. The theory of nanoparticle synthesis is reviewed. The high boiling point of the ODA encapsulant limits the onset of conduction to 350C. The films proceed through several different stages as a function of sinter temperature, first insulating, then pure electronic conducting and finally mixed conducting.

Chapter 5 describes sintering studies of THG-Ag_2S nanoparticle thin films. The temperature of conductivity onset is reduced by using a lower boiling point encapsulant. Sinter temperature is correlated to the grain size. Mixed ionic electronic conduction is found to be grain boundary limited in this system.

Chapter 6 covers filament formation studies using sintered THG-Ag_2S nanoparticle thin films. Effect of voltage on filament formation rate and morphology is studied. Consequences for developing programming algorithms for RRAMs are discussed.

Chapter 7 provides conclusions and future outlook on the development of RRAM materials and devices.

Chapter 2: Solid State Ionic Conduction and Characterization

The basic principles of solid state ionic conduction are reviewed in this section. First, defect chemistry is presented which describes the types of carriers that are generated in the bulk of ionic solids. Mass action laws are formulated for calculating equilibrium concentrations of these defects. Schottky and Kroeger-Vink notation are reviewed to provide clear and standard language for describing reaction equations. This is emphasized because various publications encountered use different notation that can result in apparently inconsistent expressions for mass action laws. Next, the notion of the electrochemical potential, or Fermi level, is reviewed for holes and electrons in semiconductors. A similar analysis is presented for ionic carriers, showing the ability to use effective band diagrams to rationalize ionic interfaces. Basic transport equations can be used to model the conduction of these defects. The concepts here are covered extensively in the literature [54-61][62-64][65]. Approximations of dilute solution are used to simplify the analysis by using Boltzmann statistics and by neglecting particle interactions. Although Silver Sulfide is not strictly a dilute solution, the analysis is still a useful framework for understanding ionic transport [66]. Finally, characterization of mixed ionic-electronic conduction by impedance spectroscopy is described along with discussion of possible grain boundary effects.

2.1: Defect Chemistry

Point defects in materials form the basis of conduction in the solid state. Thermally generated electrons and holes in semiconductors are a well known defect type in electronic devices. These differ from defects in ionic solids because electronic carriers are delocalized from lattice atoms and exist in continuous bands. In ionic solids, defects such as interstitials and vacancies move by hopping transport instead of band-like transport. Phenomena resulting from point defects have broad utility ranging from industrial applications in film photography and fuel cells, to cosmetic applications in the coloring of gemstones. In film, exposure of silver halide grains causes nucleation of silver, which provide catalytic sites for reduction in developer solution. The photo-sensitivity of film can be increased by using interfacial effects to generate surface fields to separate photo-generated charge. In solid oxide fuel cells, homogenous doping of ceramics such as Yttria-Stabilized Zirconia (YSZ), improve oxygen conductivity by increasing the concentration of oxygen vacancies. In gemstones, colour is caused by homogenous doping that creates charged schottky defects.

In this section, point defect chemistry will be reviewed for the framework of ionic conduction. Schottky and kroeger-vink notation for describing the generation of these point defects is first reviewed. Subtle differences between the two will be discussed. Different types of point defects, such as Frenkel and Schottky defects will then be explained in terms of formation conditions. Finally, mass action laws that describe the equilibrium concentration of these defect species will be derived from the defect reaction equations.

2.1.1: Schottky Notation and Kroeger-Vink Notation

In this section, the difference between Schottky and Kroeger-vink notation is reviewed. During a survey of literature, it was observed that notations were used interchangeably and

mixed at times in various sources. This eventually led to apparently inconsistent expressions and missing terms in mass action laws that were derived from reaction equations. A presentation of a consistent framework is described, drawing from Maier and Smyth [33][51].

There are two types of notation to describe defect reactions: Schottky and Kroeger-Vink [33]. Sample notation is shown in Table 2-1. M is the species of interest indicated by the atomic symbol. S is the lattice site in the crystal indicated also by the atomic symbol. Charge is denoted by a superscript in both notations. '$^{\cdot}$' refers to a positive charge, and '$^{\prime}$' refers to a negative charge. Multiple charges on the same element are indicated by repeating the charge symbol as needed.

	Lattice	Interstitial	Vacancy
Schottky "Building Elements"	$M\|S\|$	M^{c}	$\|M\|^{c}$
Kroeger-Vink "Structural Elements"	M_s^{c}	M_i^{c}	V_s^{c}
Building Element/Structural Element Equivalence	$M1_{s1}^{c}$- $M2_{s2}^{c}$	M_i^{c}- V_i^{c}	V_s^{c}- M_s^{c}

Table 2-1: Schottky Notation for building elements. Kroeger-Vink Notation for structural elements: species 'M', on lattice point 's', having charge 'c'. Equivalence of notations.

In schottky notation, ***building elements*** describe defects and charges relative to the perfect crystal. A vacancy is described with brackets around the main species. Interstitials are denoted as a species symbol with charge. Lattice atoms are written as an interstitial-vacancy pair. Charges are indicated by the superscript '$^{\cdot}$' for positive charges, or '$^{\prime}$' for negative charges. Neutral charges are indicated by the omission of charge symbol.

In kroeger-vink notation, ***structural elements*** describe defects and charges relative to free space. This notation is more methodic compared to schottky notation. The species of interest is represented by the main character M, which is also the atomic symbol. Lattice sites are denoted by the subscript 'S'. Interstitials are indicated by occupation of the site 'i.' Vacancies are represented by the absence of a main species on a site by main character 'V'. For example, $Ag_i^{\cdot}$ describes a positively charged Ag atom at an interstitial site. Neutral charges are denoted by an 'x', unlike schottky notation which omits neutral charge symbols.

The difference between these notations is best demonstrated by examining reaction equations. The same reaction can be represented in both schottky and kroeger-vink notation as shown in Table 2-2. Schottky notation is simple and concise, but does not emphasize location of lattice sites in building elements. For complicated reactions involving multiple species, kroeger-vink notation provides clear though verbose accounting through structural elements. The specific transitions of species across multiple lattice sites can be tracked, which is not possible when using Schottky notation.

Schottky notation can be converted into kroeger-vink notation and vice versa. The kroeger-vink structural elements can be combined into expressions that are equivalent to schottky building elements. All reactants are moved from the left hand side to the right hand side and summed in separate groups by species, and pair-wise by interstitial sites. Both notations can be

translated into mass action laws as shown later in this chapter. As demonstrated by this conversion method, the structural elements of kroeger-vink are necessarily coupled. The structural elements should not be directly converted to mass action laws of the chemical potential due to this dependence. The derivation of the free enthalpy requires that the activities of individual species can be independently varied by introduction of those species into the system [65]. It is this difference between the notations that can lead to apparently inconsistent expressions for mass action laws. However, because Kroeger-Vink notation provides more information about the mechanics of defect generation, it will be the standard notation for defect reactions used throughout this work.

Schottky-Notation	$Nil \leftrightarrow Ag^{\cdot} + \lvert Ag \rvert'$
Kroeger-Vink Notation	$Ag_{Ag}^{x} + V_I^{x} \leftrightarrow Ag_I^{\cdot} + V_{Ag}'$
Schottky Kroeger-Vink Equivalence	$Nil \leftrightarrow (Ag_I^{\cdot} - Ag_{Ag}^{x}) + (V_{Ag}' - V_I^{x})$

Table 2-2: Schottky and Kroeger-Vink Notation for Interstitial Creation Reaction

2.1.2: Point Defect Types

Having reviewed notation for describing point defects, different types of point defects will now be reviewed. Schottky and frenkel defects are two types of defects that can be generated, and can be either intrinsic or extrinsic. Intrinsic defects are generated in a pure stoichiometric material, while extrinsic defects are generated in an impure or non-stoichiometric material. There are several inter-related principles that must be maintained in any type of defect formation. These are: conservation of charge, conservation of structure, conservation of mass and conservation of electronic states. The first two principles state that within a volume of crystal, the total number of atoms and net charge must remain the same before and after defect formation. For example, after hole-electron generation, net charge is still 0. The next two principles are related to the total capacity of crystal volume. For example, the total number of electron-hole pairs generated within a crystal cannot exceed the total number of initial bonds in the crystal. The ionic defect analogue is conservation of mass. The total number of cation-anion defect pairs within a crystal volume cannot exceed the number of starting atoms.

Intrinsic Disorder

Intrinsic defects occur in undoped stoichiometric compounds. Schottky and Frenkel defects are two main types of point defects found in these ionic crystals [33]. A schottky defect is formed when an anion-cation pair is displaced from the regular crystal to the surface forming a corresponding pair of vacancies. The reaction for this is expressed in Equation 2-1. The reactants may be any neighboring anion-cation pair in the crystal. Schottky defects are likely to form in crystals with close-packed structures having rigid cation and anion sub-lattices. Displacement of either ion to an interstitial site would cause too much deformation in the crystal. NaCl is one example of a material in which schottky defect formation dominates.

$$Na_{Na} + Cl_{Cl} \leftrightarrow V_{Na}' + V_{Cl}^{\cdot} + NaCl$$

Equation 2-1: Schottky Defect Formation

Frenkel defects are formed by the displacement of either the anion or cation from the lattice site to an interstitial site. Displacement of a cation to the interstitial site is called a Frenkel Defect. Displacement of an anion to the interstitial site is called an Anti-Frenkel Defect. The type of ion displacement in a crystal depends on the relative sizes of the cations, anions and interstitial sites. Frenkel defects are more likely to form in compounds that have different cationic and anionic radii, and in which one of the species has a volume comparable to the size of the interstitial site. A sample reaction for cationic frenkel defect formation is expressed in Equation 2-2. A silver atom is displaced from the lattice site into an interstitial site forming a cationic interstitial silver, and anionic vacancy. This type of defect is most common in the silver halides and chalcogenides. The silver cation has the unique property of not acting like a rigid sphere, allowing it to deform and move through interstitial sites in a crystal [62].

$$Ag_{Ag}^{x} + V_{I}^{x} \leftrightarrow Ag_{I}^{\cdot} + V_{Ag}^{'}$$

Equation 2-2: Frenkel Defect Formation

Extrinsic Disorder

Extrinsic defects arise from non-stoichiometry and impurities in compounds. These can cause doping effects that modify carrier concentrations. These doping effects can be classified as either homogeneous or heterogeneous. Homogenous doping effects occur by the uniform dispersion of impurities throughout a single phase. Heterogeneous doping effects occur at the interfaces of two phases. Further description of this heterogeneous doping will be delayed until after discussion of interfacial effects.

$$O_O^x \leftrightarrow 0.5O_{2(g)} + V_o^{\cdot\cdot} + 2e^{'}$$

Equation 2-3: Vacancy-Electron Generation

Homogeneous doping is further subdivided into substitutional doping and defect doping. A well-known example of electronic substitutional doping is the substitution of donor phosphorous impurities on silicon lattice sites to enrich electron concentration. An example of defect doping is zinc oxide, an n-type semiconducting oxide whose conductivity depends on the non-stoichiometry [51]. The composition can be controlled by the partial pressure of oxygen in the atmosphere during high temperature sintering in order to tune conductivity. A deficiency of oxygen generates oxygen vacancies and excess electrons as described in Equation 2-3. Although two defects are generated in this case, at room temperature the defects contribute primarily to electronic conduction because vacancy diffusion is very slow. This type of defect doping is further classified as vacancy doping, because the presence of oxygen vacancies enriches the electronic carrier concentration.

$$CdCl_2 + 2V_{Ag}^{'} + 2V_{Cl}^{\cdot} \leftrightarrow Cd_{Ag}^{\cdot} + V_{Ag}^{'} + 2Cl_{Cl}^{x}$$

Equation 2-4: Vacancy-Electron Generation

Ionic compounds can also be homogeneously doped to vary ionic defect concentrations, just as silicon may be doped to vary electronic concentration. For example, incorporation of a

small amount of $CdCl_2$ into AgCl enhances the ionic conductivity by enriching the concentration of silver vacancies, as shown in Equation 2-4 [62].

Given these mechanisms of defect generation, a method for quantifying equilibrium concentrations of these defects will be needed. Mass action laws are the method for this quantification and will be subsequently discussed.

2.1.3: Mass Action Laws for Intrinsic Disorder

The equilibrium formation of defects is governed by mass action laws and the energy of defect formation. For example, for generation of an electron-hole pair in a semiconductor, the energy of formation is the bandgap. For the silver halide frenkel defect in Equation 2-2, the formation energy is the amount needed to displace the silver cation into an interstitial site from a lattice site. The formation of defects by excitation across energy levels is illustrated qualitatively in FIG 2-1. The left hand side illustrates the formation of a Frenkel defect, and the right hand side illustrates the formation of an electronic defect. The formation energy for the frenkel defect is the difference between the interstitial and regular levels, and for the electronic defect is the difference between the valence band and conduction band.

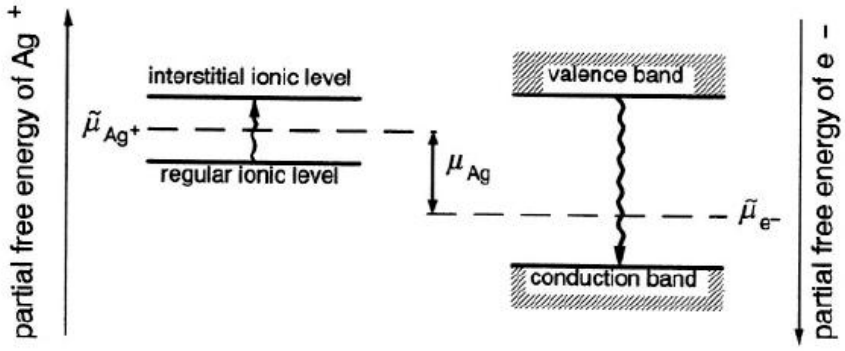


FIG 2-1: Diagram Showing Energy Levels for Defect Formation [58]

The equilibrium reaction in Equation 2-2 can be re-expressed as an equilibrium constant, a quotient of the forward (k_f) and reverse (k_r) rate constants, noted in Equation 2-5. The right hand side expresses the relation of the equilibrium concentrations to the formation energy of the defect. Although volumetric concentrations are commonly used, dimensionless concentrations that represent the thermodynamic activity of the species should be used. The particular form of this activity depends on the thermodynamic reference state, as will be further discussed in the next section. Here, the value in brackets is the ratio of the equilibrium volumetric concentration to total maximum volumetric concentration of the species. For example, $Ag_I^{\cdot}$ denotes the ratio of equilibrium interstitials per volume, to the total number of interstitial sites per volume.

$$K = \frac{k_f}{k_r} = \frac{[Ag_I^{\cdot}][V_{Ag}^{'}]}{[Ag_{Ag}^{x}][V_I^{x}]} = e^{-(\Delta Go/kT)} \xrightarrow[\text{Dilute Solution}]{} [Ag_I^{\cdot}][V_{Ag}^{'}]$$

Equation 2-5: Equilibrium Constant Expression for Mass Action

If the free enthalpy of formation ΔG is greater than multiples of thermal energy kT, the equilibrium constant is very small. In this dilute solution regime, the concentration of interstitial and vacancy defects will be very small, leading to negligible change in the starting silver lattice and vacant interstitial sites. The bottom two terms of Equation 2-5 may be approximated to 1, and eliminated from the equation. Although according to strict principles of thermodynamics, Kroeger-Vink notation cannot be used to generate proper mass-action expressions, it is still applicable in the dilute-solution.

$$\frac{n}{Nc}\frac{p}{Nv} = e^{-(Eg/kT)}$$

Equation 2-6: Equilibrium Constant Expression for Mass Action

This functional form for calculating carrier concentrations is analogous to the mass action law for electrons and holes under Boltzmann statistics, listed in Equation 2-6. n/N_c and p/N_v are the ratio of equilibrium carriers to the total capacity or effective density of states and correspond to the thermodynamic activities of electrons and holes.

2.2: Expression of Electrochemical Potential for Defects

In the previous section, mass actions laws were derived from reaction equations to describe equilibrium concentrations of defects. In this section, to further complement these values, electrochemical potentials will be derived for use in band diagrams to describe the spatial concentration of defects and effects of electric fields. Following the framework derived by Maier, the free enthalpy of formation for defect generation, $\Delta_d G$, is expressed as the difference between the total enthalpy of the perfect solid material, and real solid material [51]. The chemical potential is then the derivative of this free enthalpy $\Delta_d G$ with respect to the number of moles of defect n_d. The free enthalpy of formation consists of bonding enthalpy, vibrational entropy, and configurational entropy.

$$\Delta_d G = \Delta_d G_{bdg} + \Delta_d G_{vib} + \Delta_d G_{cfg}$$

Equation 2-7: Components of Enthalpy of Defect Formation

Bonding enthalpy includes the energy required to break lattice bonds to generate the defect and the energy released from relaxation and polarization of the remaining lattice atoms around the defect site. This value will always be positive, requiring net input of enthalpy. Generation of defects perturb the vibrational frequencies of the nearest neighbours in the lattice. This tends to increase when vacancies are formed and decrease when interstitials are formed. Near room temperature, this effect is usually negligible. The final term, configurational entropy, quantifies the number of microstates that exist given a number of defects formed. The number of microstates given N_d and N lattice positions is the number of combinations: ${}_N C_{Nd}$. Applying stirling's approximation for large numbers, the configurational enthalpy is expressed below [62]. This term will always be negative because the number of defects generated cannot exceed the total number of atoms or free states. Consequently, increase in configurational entropy drives defect formation at temperatures above absolute zero. This is analogous to the broadening of the Fermi-dirac or Maxwell-boltzmann distributions with increasing temperature that facilitate statistical excitation of electrons across a bandgap.

$$\Delta_d \boldsymbol{G}_{cfg} = \boldsymbol{kBTN}_{\boldsymbol{d}} \boldsymbol{ln}\,(\frac{\boldsymbol{N_d}}{\boldsymbol{N}})$$

Equation 2-8: Configurational Enthalpy

The total free enthalpy of formation can then be expressed as a function of the defect concentration. Differentiating with respect to the moles of defect n_d, yields the chemical potential of the defect species: μ_d. The reference state denoted by μ_d^* corresponds to bonding and vibrational enthalpy. N_A is avogadro's number.

$$\Delta_d G = N_d(\Delta_d g_{bdg} + \Delta_d g_{vib} + RTln\left(\frac{N_d}{N}\right)) \xrightarrow{N_A * \frac{d}{dN_d}} \mu_d = \mu_d^* + RTln(\frac{N_d}{N})$$

Equation 2-9: Derivation of Chemical Potential of Species, N_A is Avogadro's number

Adding the electric potential to the chemical potential yields the electrochemical potential that accounts for effects of electric field on carrier movement.

$$\tilde{\mu}_d = \mu_d + z\emptyset = \mu_d^* + RTln\left(\frac{N_d}{N}\right) + z\emptyset$$

Equation 2-10: Electrochemical Potential, z is charge number of defect species

The expression for electrochemical potential in Equation 2-10 can be compared to the functional expressions of electron and hole concentrations in semiconductors using Boltzmann statistics, listed in Table 2-3. The direct equivalence of the Fermi level and electrochemical potential can clearly be observed. The reference states: μ_e^*/N_A and $-\mu_h^*/N_A$ correspond to the conduction band and valence band edge respectively. The potentials are divided by N_A, avogadro's number to relate to the energy values. This scales the energy values to per particle from per mole.

$n = Nc * \exp\,(\frac{-(Ec - Ef)}{kT})$	$p = Nv * \exp\,(\frac{-(Ef - Ev)}{kT})$
$Ef = Ec + kT * \ln\,(\frac{n}{Nc}) = \frac{\widetilde{\mu_e}}{N_A} = \frac{\mu_e^*}{N_A} + kT * \ln\,(\frac{n}{Nc})$	$Ef = Ev - kT * \ln\left(\frac{p}{Nv}\right) = \frac{-\tilde{\mu}_h}{N_A} = \frac{-\mu_h^*}{N_A} - kT * \ln\left(\frac{p}{Nv}\right)$

Table 2-3: Equivalent Expression for Chemical Potential and Fermi Level

The reference states denoted '*' are specific to each defect species. Each configurational entropy term for a different species, $RTln(N_d/N_s)$, has a different maximum concentration N_s. For vacancies, this value is the total number of lattice atoms. For electrons, it would be the effective density of states, N_c. For convenience, all configurational entropies can be normalized such that N_s is replaced by N_m, the atomic density of the crystal, by subtracting RTln(N/Nd) from μ^*, the current reference state. The new temperature dependent reference state would be μ^o.

The vacuum level is the common reference state for both electrons and holes, representing an unbound electron and fully bound hole. At levels below vacuum, the free energy of electrons decrease, while the free energy of holes increase. The different sign of charge causes the opposite reaction of these carriers. FIG 2-2 summarizes this framework for defect carrier

generation. The ionic and electronic carrier concentrations of a material will depend on the bandgap and defect formation enthalpy.

Maier has stated that the ionic and electronic Fermi levels are related by the chemical potential of the neutral species as illustrated in FIG 2-1 [51]. In Ag_2S, the two relevant species are silver cation interstitials and conduction band electrons, shown in Equation 2-11.

$$Ag \leftrightarrow Ag^+ + e^- \;\; ; \;\; \mu_{Ag} = \mu_{e-} + \mu_{Ag+}$$

Equation 2-11: Silver / Electron Coupling

This statement is significant because it couples the ionic and electronic concentrations to the activity of neutral silver. This may be explained as follows. The chemical potential of silver can be written as the sum of a reference state and activity term.

$$\mu_{Ag} = \mu^*_{Ag} + RTln(a_{Ag})$$

Equation 2-12: Expression of Chemical Potential

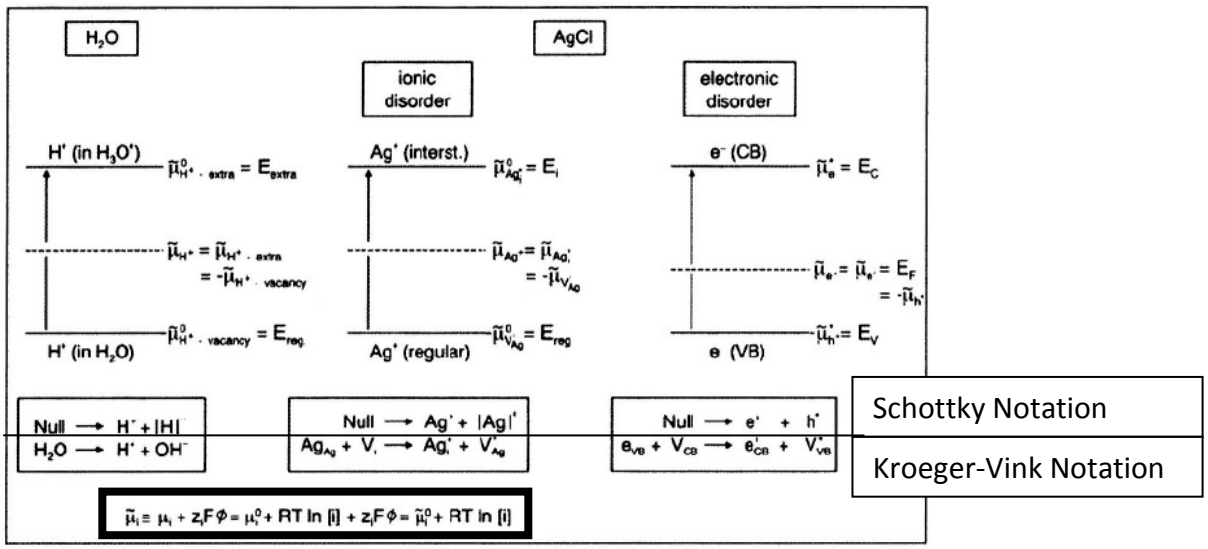


Figure 2. Electronic and ionic disorder in ionic solids and in water in "physical" (top) and "chemical" language (bottom).[20] The coupling of the ionic and electronic Fermi levels takes place via the chemical potential of the neutral components (here: $\tilde{\mu}_{Ag^+} + \tilde{\mu}_{e^-} = \mu_{Ag}$) (see Fig. 3). A further relevant example could be the breaking-up of an ion pair in a polymer.

FIG 2-2: Band Diagram Equivalents reproduced from [58] (The lower band has '-' preceding each value)

For convenience, the only constraint placed on the reference state is that the activity at the stoichiometric composition of Ag_2S is equal to zero. As neutral silver is incorporated into the Ag_2S, the activity of silver and thus the chemical potential of silver will increase. This will generate more Ag_i and e^-, and is reflected by a lengthening of μ_{Ag} in FIG 2-1. Since the reference states, μ_{Agi}^* and μ_e^*, for the interstitial ionic level and conduction band are fixed, the electrochemical potentials and $\tilde{\mu}_{Ag}$ and $\tilde{\mu}_e$ must shift closer to the interstitial ionic level and electronic level respectively. The magnitude of each shift depends on the ratio of change in

silver activity to the intrinsic interstitial and electron concentration. It is significant only if the change is larger than the intrinsic carrier concentration.

2.3: Ionic Conduction

Having reviewed the mechanisms behind ionic and electronic carrier generation in solids, transport mechanisms of these carriers through the solid will be described next. Conductivity is the product of carrier concentration and carrier mobility. Electronic conduction typically takes place by band-like transport in well ordered solids, or by a hopping mechanism in disordered solids with significant numbers of trap states. On the other hand, ionic conduction takes place by one of three possible mechanisms: movement by 1) vacancy, 2) interstitial or 3) interstitialcy. These are thermally activated hopping mechanisms, because the ionic species must surmount energetic barriers to traverse different lattice and interstitial sites in the solid. The vacancy and interstitial conduction are analogous to hole and electron conduction respectively.

Reaction equations in Kroeger-Vink notation describe these three mechanisms in Table 2-4 [62]. In the vacancy mechanism, neighboring lattice atoms jump into the lattice vacancy, exchanging positions. Movement of this vacany can be tracked, just like a hole. In the interstitial mechanism, interstitial atoms jump into neighboring vacant interstitial sites. In the interstitialcy mechanism, an interstitial atom displaces a lattice atom into a neighboring interstitial site. This last process takes place in solids with large cations in close-packed structures. The indirect movement by displacement of a lattice atom has a lower energetic barrier than direct hopping. This takes place in silver halides and chalcogenides such as Ag_2S.

Vacancy	$Ag_{Ag}^{x}(x) + V_{Ag}^{'}(x') \leftrightarrow V_{Ag}^{'}(x) + Ag_{Ag}^{x}(x')$
Interstitial	$Ag_{i}^{\cdot}(x) + V_{I}^{x}(x') \leftrightarrow V_{I}^{x}(x) + Ag_{i}^{\cdot}(x')$
Interstitialcy	$Ag_{i}^{\cdot}(x) + Ag'_{Ag}^{x}(x^*) + V_{I}^{x}(x') \leftrightarrow V_{I}^{x}(x) + Ag_{Ag}^{x}(x^*) + Ag'_{I}^{\cdot}(x')$

Table 2-4: Ionic Conduction Mechanisms

The relative levels of ionic and electronic conduction in a solid are thus dependent upon the thermodynamics of carrier formation and the kinetics of carrier movement. In cubic α-AgI, the prototypical pure ionic conductor, the ionic carrier concentration is significantly higher than the electronic concentration, and the electron mobility is low [67][66]. In monoclinic β-Ag_2S, a mixed ionic-electronic conductor, the concentration of ionic carriers is higher than the electronic carriers, but the electron mobility is higher, leading to higher electronic conduction.

2.4: Interfacial Effects on Ionic Conductors

In the previous sections, formal notation for describing point defect generation and mass action laws has been reviewed, and the electrochemical potential or Fermi level of these defects has been derived. Using these principles enables quantification and examination of interfacial effects of these materials. In this section, quantification of interfacial space charge in semiconductors will be reviewed. Two different charge profile models are described, along with application of interfacial effects for heterogeneous doping of ionic materials.

The Fermi level is a powerful tool for visualizing carrier migration and interfacial effects on carrier concentration in semiconductors and solid electrolytes. At thermal equilibrium within a

semiconductor and across junctions of semiconductors, the Fermi level is a uniform value. A non-zero gradient would drive carrier migration. Although the gradient of the electrochemical potential is zero at thermal equilibrium, the gradients of the chemical and electric potential may be non-zero but exactly balance. This is often the case at interfaces, where carrier concentrations may differ from the bulk.

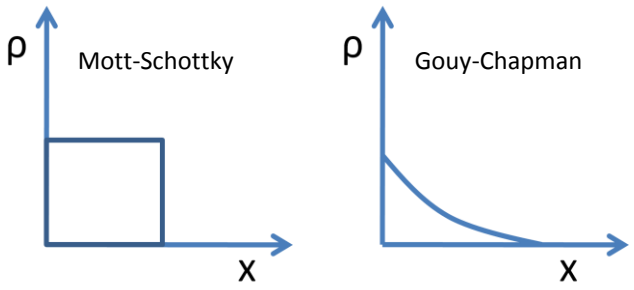


FIG 2-3: Sample Mott-Schottky and Gouy-Chapman Space Charge Profiles

Equilibration of the Fermi levels in adjacent phases allows calculation of interfacial space charge. This is similar to analysis of p-n junctions in semiconductors. However, the models for spatial distribution of this charge depend on the doping profile of the material and the mobility of the space charge in the material. The Mott-Schottky and Gouy-Chapman profiles are two such models for space charge distribution and are illustrated in FIG 2-3. In intrinsic semiconductors the majority of space charge is mobile, and a gouy-chapman profile is used [68]. In contrast, in substitutionally doped semiconductors, the majority of space charge is immobile, corresponding to ionized dopants, and a mott-schottky profile must be used. This mott-schottky profile facilitates the well-known depletion approximation that is used in basic analysis of p-n junctions. In the depletion approximation, semiconductors on either side of the junction are extrinsically doped with a uniform dopant profile. Because the profile of this fixed charge is independent of spatial voltage and fields within the device, the space charge may be approximated as a fixed rectangular depletion region.

Although the solution of the mott-schottky profile for doped materials is presented in many device texts, the solution of the gouy-chapman profile for intrinsic materials is covered in few if any such works [69][70]. Derivation of this gouy-chapman profile for the semi-infinite case will be reviewed briefly following the framework presented by Maier [55]. At an interface, shifts of carrier concentrations from equilibrium can be driven either by interaction with a neighboring phase, or by an intrinsic enthalpy when terminating in free space. The interaction of two phases is treated as an equilibration of Fermi levels, where a built-in potential results from the difference of the isolated Fermi levels. In the absence of a neighboring phase, intrinsic interfacial disorder occurs. This sets a fixed surface potential as a boundary value in the solution, instead of a built-in potential difference. These values will become clearer in the following derivation of the solution. The objective is to solve for a relation between electric potential and carrier concentration within an intrinsic material, subject to either a surface boundary value.

Within a given material of interest, by setting the Fermi levels of the bulk and interface equal to one another, a dimensionless carrier concentration for the surface can be expressed.

$$\tilde{\mu}_o = \tilde{\mu}_\infty \rightarrow [\left(\frac{c_s}{c_\infty}\right)\left(e^{(\mu_o - \mu_\infty)}\right)]^{-z_k} = e^{-\frac{F}{RT}(\emptyset_o - \emptyset_\infty)} \xrightarrow[\mu_o = \mu_\infty]{} \zeta_k^{z_k} = \left(\frac{c_s}{c_\infty}\right)^{-z_k} = e^{-\frac{F}{RT}(\emptyset_o - \emptyset_\infty)}$$

Equation 2-13: Dimensionless Carrier Concentration: o-interface, ∞-bulk, k-species index

The poisson-boltzmann equation then relates the carrier concentration to electric potential. The specific cases of a monovalent cationic and anionic species is considered for simplicity.

$$\frac{d^2 ln\zeta_{i,v}}{d\xi^2} = \frac{1}{2}\left(\zeta_{i,v} - \zeta_{v,i}^{-1}\right)$$

Equation 2-14: Poisson Boltzmann Distribution: $\xi = x/\lambda_d$, dimensionless length scaled by debye length

The analytical solution to the poisson-boltzmann is parameterized by a degree of influence ϑ. This parameter ranges from -1 to 1 corresponding to maximum carrier depletion to enrichment.

$$\zeta_{+,-} = \left(\frac{1 + \vartheta_{+,-}e^{-\xi}}{1 - \vartheta_{+,-}e^{-\xi}}\right)^2$$

Equation 2-15: Analytical Solution to Poisson-Boltzmann Equation

$$\vartheta_{+,-} = \frac{\zeta_{o+,-}^{0.5} - 1}{\zeta_{o+,-}^{0.5} + 1}$$

Equation 2-16: Degree of Influence

When equilibrating the Fermi levels, the carrier concentration is solved by setting the built-in potential (Φ_o-Φ_∞) in the poisson-boltzmann equation and the dimensionless carrier concentration in Equation 2-13 and Equation 2-14. In the case of intrinsic surface disorder, the surface carrier concentration c_o, may be calculated given an interfacial formation enthalpy set as a constraint in the degree of influence in Equation 2-16.

These interfacial carrier effects are significant within two debye lengths of the surface. Beyond that length from the interface, the carrier concentration is not significantly perturbed from the bulk value. Several sample cases are calculated and plotted in FIG 2-4. At a domain length of $4\lambda_d$ (debye lengths), the interfacial effects completely penetrate the bulk. Perturbations to carrier concentration throughout the length of material are completely dominated by the surface. The enhancement and depletion of ionic carriers at this length scale is also known as the “true size effect” of nanoionics.

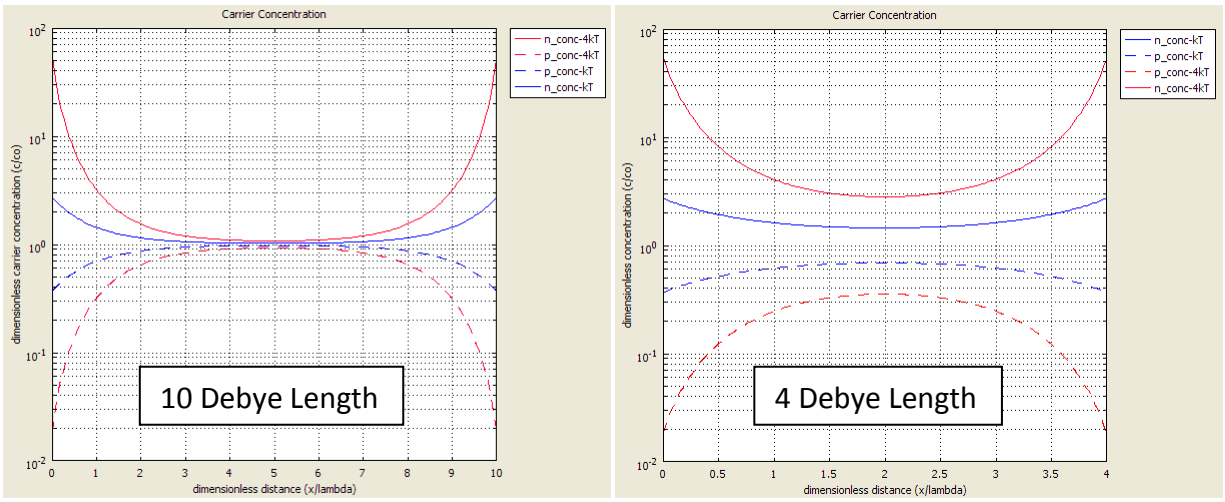


FIG 2-4: Dimensionless carrier enrichment and depletion: varying dimensionless length of material in debye lengths, and setting built-in potential to either 4 kT or 1 kT.

2.4.1: Heterogeneous Doping

The doping of materials to enrich specific types of carriers has been previously described when introducing point defects. The homogeneous doping of materials was discussed. This occurred from substitution and non-stoichiometric effects within the bulk. Here, the heterogeneous-doping of compounds is described, that result from interfacial effects between distinct material phases. Mixtures of these material phases show enhanced ionic conductivity relative to components. These effects have been demonstrated in Ag_2S/Al_2O_3 and for nearly all of the silver halide/Al_2O_3 composites [71][72]. Mixed powders of AgCl and Al_2O_3 show higher ionic conductivity than pure AgCl [51][55][71]. In these cases, the binding of silver interstitials at the grain boundaries enhances mobile vacancy concentration in a space charge region near the surface, thereby enhancing conductivity of these interfacial space charge regions. This contrasts with semiconductor interfaces for which interfacial space charge is usually immobile and does not contribute to conductivity.

These interfacial phenomena are modeled by the core-space charge model, whereby the bound silver cations at the surface form the core, and adjacent depletion region forms in response to that surface charge. The excerpted FIG 2-5, illustrates these interactions between the bulk mixed conductor and a second phase. In these cases, the second phase is not another solid, but a monolayer of gas. At the surface of a sample metal oxide, chemisorption of oxygen generates a negative surface charge, which depletes electrons and enhances holes within the interfacial space charge region. At the surface of a silver halide, nucleophilic ammonia binds silver interstitial cations with its lone pair of electrons. This generates a positive surface charge, and induces an adjacent negative space charge layer by depleting interstitials and enriching vacancies. These interfacial effects have been use to develop composite materials with enhanced conductivity, and in sensor applications. These interfacial effects play a role in Chapter 4, which uses Ag_2S nanoparticles stabilized by an amine-ligand.

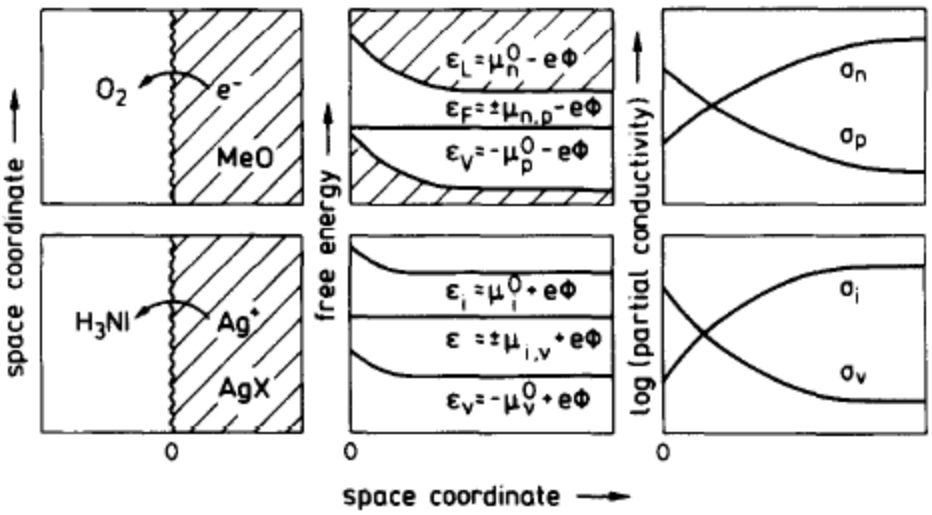


FIG 2-5: Modification of surface carrier concentration due to interfaial interaction with gases [72]

2.5: Characterization Method: Electrical Impedance Spectroscopy

Having described a basic framework of ionic and electronic conduction in solids, Electrical Impedance Spectroscopy is introduced as a technique for measuring the ionic and electronic conductivities in mixed conductors. To separate the mixed conductivity, ion or electron blocking contacts are used. Platinum is typically used as an ion blocking electrode due to low reactivity with other compounds. For electron-blocking contacts, an Ag/pure ionic conductor bilayer is often used to contact silver conducting electrolytes. The pure ionic conductor is typically AgI, used only for measurements higher than 150C, when it acts as a superionic conductor. At lower temperatures, $RbAg_4I_5$ may be used instead. In this work, Pt blocking contacts are used due to ease of processing, compared to the pure ionic conducting silver halide compounds.

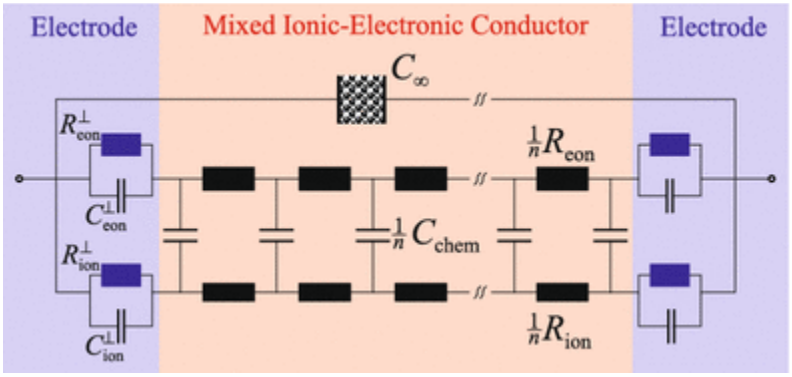


FIG 2-6: Equivalent Circuit for Bulked Mixed Conductor [76]

Impedance spectroscopy resolves processes that occur at different time constants. These processes and time constants can be modeled as resistive and capacitive elements. The equivalent circuit for a bulk mixed conductor is an infinite series transmission line with terminal elements depending on the nature of the contacts. The derivation of this model from thermodynamics has been covered by Jamnik, Maier and Lai in the literature [73][74][75]. The

core assumptions of this model are local electroneutrality and dilute solution. The contact resistance and capacitance are denoted with the ⊥ symbol, and correspond to the small signal model for a schottky contact.

A dielectric capacitance represents a bulk parallel plate capacitance. When measured across large electrode gaps, this value tends to be very small, corresponding to a short time constant well separated from other processes. Ionic and electronic conduction are represented by two parallel paths. These are coupled together by a chemical capacitance that represents polarization of the ions in the material. At high frequency, all capacitances except the bulk dielectric are shorted and the circuit reduces to the ionic and electronic resistance in parallel. Contact effects are bypassed in this regime. At low frequency, all capacitors open and the circuit reduces to a parallel ionic and electronic conduction path that includes the contact resistances. By using ion blocking contacts, the electronic resistance can be resolved in the low frequency measurement. Measurement data is represented in a nyquist plot of negative imaginary versus real impedance. This convention is selected so that capacitance loops appear in the first quadrant.

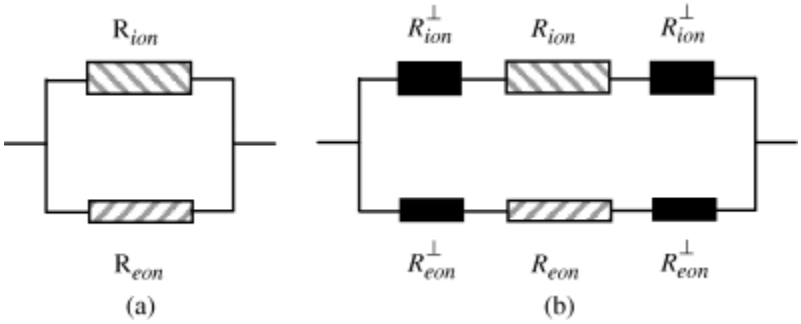


FIG 2-7: a) high frequency limit equivalent circuit b) low frequency limit equivalent circuit. When contacts blocking for either ions or electrons are used, one of the two resistances can be resolved. [73]

An ideal nyquist plot for a mixed conductor is shown in FIG 2-8, assuming clear separation of the time constants. The high frequency bulk dielectric loop and low frequency mixed conduction loop are both shown. Figures of merit extracted from these plots are the real-intercepts of the mixed conduction loop. The values of contact resistance have been neglected in the plot. The high frequency dielectric loop corresponds to the time constant of the small bulk capacitance, denoted C_{∞} in FIG 2-6, and ($Z_{ion}||Z_{eon}$) in FIG 2-7a. This bulk capacitance is similar to the bulk capacitance between electrodes in a battery. In the high frequency limit, all of the current is shunted through the bulk capacitance leading to very low real-impedance. At intermediate frequencies, current is shunted through the chemical capacitance and contact capacitances, yielding the value of ($Z_{ion}||Z_{eon}$) in FIG 2-7a. The low-frequency loop exhibits a half-tear drop shape, characteristic of mixed conducting materials with blocking contacts. Referring to FIG 2-7b, when ionic blocking contacts are used, only R_{eon} and $R_{\perp eon}$ are measured in the low frequency limit. The specific shape of the mixed conductance loop arises from the solution of the ladder circuit illustrated in FIG 2-6. This is a hyperbolic tangent relation between the complex impedance and frequency, and has been derived from basic thermodynamic principles by Lai et al [73].

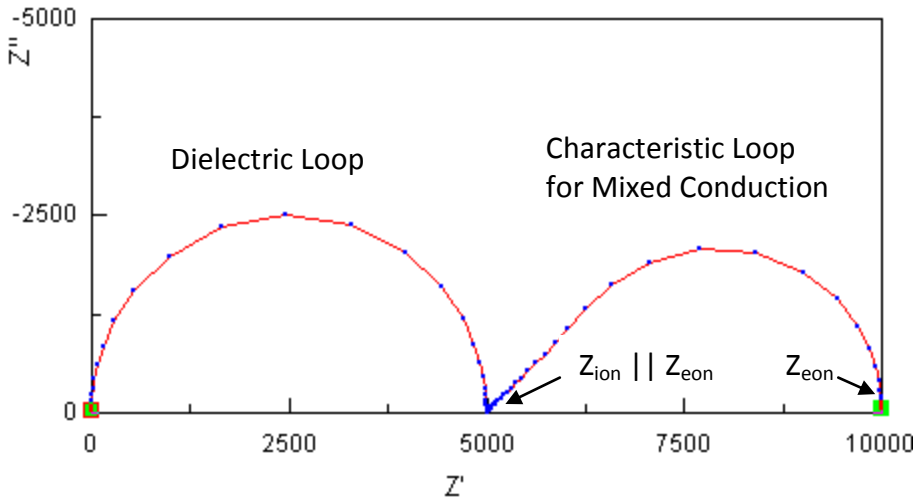


FIG 2-8: Sample nyquist plot using ion blocking contacts.

The impedance data in this dissertation were measured using a Solartron 1260 Frequency Response Analyzer connected to a Solartron 1296A Dielectric Interface. The frequency range of the tool is 10 µHz to 32 MHz. The 1296A add-on allowed measurements up to the TeraOhm range. Samples were placed inside a small probe station in a faraday cage to eliminate noise from ambient light and equipment. Data were collected using the Solartron Materials and Research Test (SMaRT) software, and processed using ZVIEW software from scribner associates.

2.6: Grain Boundary Models

Impedance spectra of polycrystalline materials may differ from bulk materials depending on the relative conductivities of the grain interior and grain boundary. The brick-layer and easy path models are used to describe the impedance data for these microstructures. In the brick layer model, all grains are assumed to be cubic and of uniform size, completely surrounded on by a boundary layer. This case applies to certain high temperature ceramics in which impurities segregate to form continuous boundary layers. For example, SiO_2 impurities in yttria stabilized zirconia (YSZ) are known to degrade the performance of YSZ based solid oxide fuel cells [77]. This degradation results from segregation of SiO_2 to the grain boundaries of YSZ, forming an insulating layer around grains that impedes current flow of oxygen anions. When there is imperfect coverage of this boundary phase, easy-paths for current flow through thin or non-existing regions of the boundary phase between grains exist.

The physical representations of the models are illustrated in FIG 2-9A, B for the brick layer and easy-path modified model. The equivalent circuits are shown in FIG 2-9C, D. In the ideal brick layer model, each grain is completely surrounded by a boundary layer. The basic unit of this repeating matrix of grains is a single cubic grain surrounded on three sides by a boundary layer. Thus, when considering current flow vertically through this matrix from the base to the top, there exist three current paths through each grain unit: one through the vertical boundary layer and grain (2+C in FIG 2-9A), and two through the lateral boundary layers (1+3 in FIG 2-9A). Each of these paths is modeled by a parallel resistor and capacitor in the equilvalent circuit

shown in FIG 2-9C. Three parallel paths are modeled: Two are for the side boundaries 1 and 3, and one is for the series connection of the core and boundary 2.

The easy-path modification of the brick-layer model is illustrated in FIG 2-9B. A set of four grain cores is surrounded by a boundary phase. g_b refers to the grain boundary, and g_i refers to the grain interior. At defective regions of the grain boundary, "easy-paths" to current flow exist. These manifest as a shunt resistance in the equivalent circuit in FIG 2-9D. The circuit for boundary layer 2 which is in series with the core, has been modified to include a shunt resistance for the easy-path (R-Easy Path). The circuits for boundary layers 1 and 3 are unmodified because the easy-path mainly affects current flowing normal through grain surfaces, not along grain boundaries.

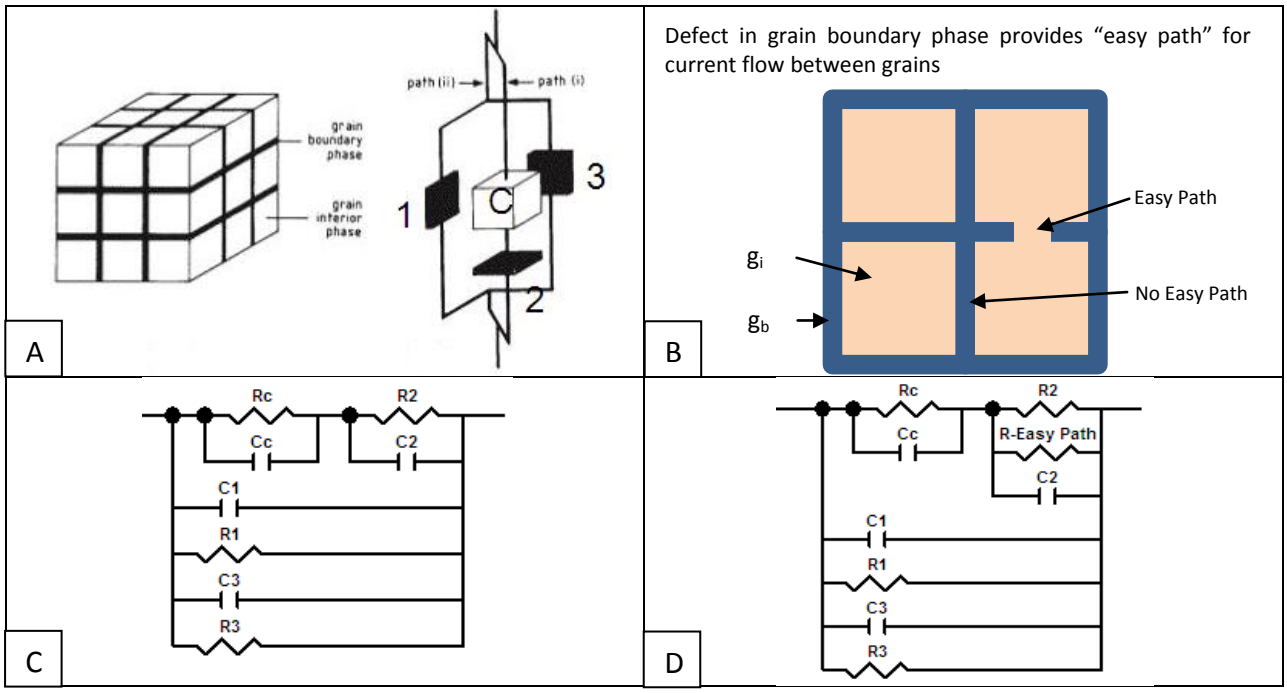


FIG 2-9: A) Brick Layer Model B) Easy Path Illustration [78] C) Equivalent Circuit of Brick Layer Model D) Easy path Modified Circuit

Simulated EIS data of the brick-layer model is illustrated in FIG 2-10 assuming pure ionic or electronic conduction. Four corner cases are shown. When small highly conductive cores are surrounded by a vast insulating boundary matrix, two time constants exist in the form of two nyquist loops (FIG 2-10A). However, the large impedance of the boundary phase overshadows the core impedance which is not easily observed. If the structure consists of large cores surrounded by a thin insulating phase, the two nyquist loops are more clearly resolved (FIG 2-10B). For this case, the presence of an easy path shunt resistance through the thin insulating layer is observed as reduced resistance of the boundary phase (FIG 2-10E). This easy-path is clearly illustrated by difference between equivalent circuit models for the ideal brick layer model and easy path-modification in FIG 2-9C and FIG 2-9D. In the last cases, when the boundary phases are highly conducting, then the current path bypasses the cores, showing little frequency dependence (FIG 2-10C,D), or a single loop.

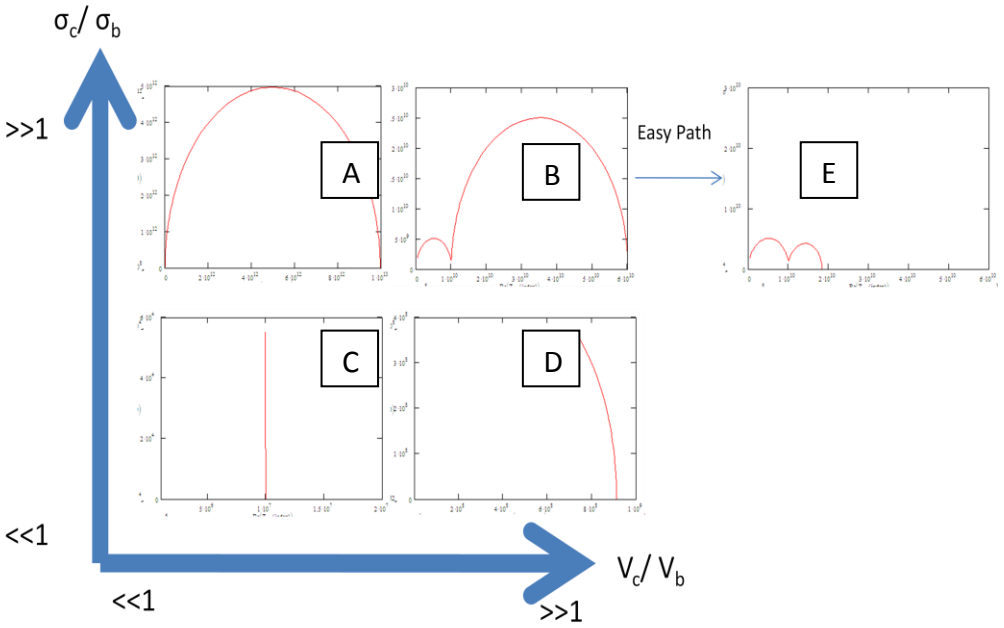


FIG 2-10: Simulated Brick layer model for limiting cases, varying core/boundary conductivity and volume.

2.7: Summary

The relation of defect chemistry to mass action and equilibrium carrier concentrations has been reviewed. The standard analysis of electron-hole carriers in doped semiconductors is shown to be a specific case of defect chemistry. Dilute solution approximations are made to simplify analysis. More accurate modeling will require use of concentrated solution theory, including stefan-maxwell diffusion models. Interfacial effects are shown to modify surface carrier concentrations, similar to surface effects in schottky barriers at metal-semiconductor interfaces. A method for measuring and resolving ionic and electronic impedances has been reviewed, along with an equivalent circuit model for bulk mixed conductors and discussion of possible grain boundary effects. This provides a basic framework for understanding solid state mixed ionic-electronic conduction and characterization.

Chapter 3: Sulfidation of Elemental Silver Films

3.1: Background

3.1.1: Blanket Thin Film Deposition Methods

In conventional microelectronic fabrication, thin films are sequentially deposited and lithographically patterned on a substrate to form electronic devices and mechanical structures. Integration of novel materials into a CMOS process flow requires a blanket thin film deposition method, etch method, and material compatibility with the photoresist and developer chemistry for lithography. Thermal evaporation, chemical vapor deposition, chemical bath deposition and sulfidation have been explored in literature as thin film deposition methods for silver sulfide (Ag_2S) [79][80][81-83][41]. Only the last two methods are solution processable, and can avoid costly high-vacuum and high-temperature steps required in the first two methods.

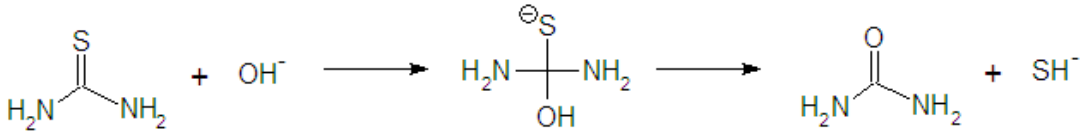
Chemical bath deposition (CBD) is analogous to chemical vapour deposition (CVD) but done in liquid phase. Desire for low-cost, high-throughput deposition of blanket layers for solar cells motivated early CBD research in the 1980s. A large number of published CBDs use aqueous chemistries for low cost and simplicity [84][85]. The obviation of hazardous organic solvents and reagents reduces the cost of waste abatement. The wider range of abundant water soluble metal salts than organic soluble salts increases the synthetic diversity of aqueous CBDs. The use of aqueous baths also facilitates patterned deposition through selective de-wetting. Redinger has demonstrated such selective CBD of zinc oxide on a patterned fluorinated octadecyltrichlorosilane (FOTS) monolayer [86]. This selective patterning can avoid an expensive photolithography step, reducing cost and avoiding compatibility issues between the material and photoresist chemistry.

In CBDs, there are typically two competing processes: heterogeneous nucleation at the solid-liquid interface between the substrate and solution, and homogeneous nucleation in the bulk of the solution, followed by growth of the nuclei. In the heterogeneous process, ions adsorb onto the substrate surface and react to form the desired material, resulting in a dense film. In the homogenous process, colloids form in solution that adsorb onto the substrate surface, resulting in a porous film. The heterogeneous process is preferred for metal-insulator-metal (MIM) structures, necessary for cross-bar memories.

The solubility product (K_{sp}) of a compound represents an upper limit for its bulk dissolved concentration, beyond which the material will precipitate from solution. In an aqueous CBD, the concentrations of the compound's component ions are controlled around the solubility limit to cause deposition.

In a sample Ag_2S-CBD process, silver nitrate, ethylenediamine tetraacetic acid (EDTA), and thiourea are mixed together in deionized (DI) water [87][82]. Silver nitrate is the metal source; thiourea is the sulfur source; EDTA is a chelating agent to control equilibrium concentration of Ag^+ cations in solution. The chelating agent acts as a chemical buffer of the metal ion source to maintain a stable concentration during the deposition reaction. It is similar to a buffering agent, which maintains a stable pH against small perturbations of acid or base. Concentrated aqueous ammonia is added to raise pH of the solution and hydrolyze the thiourea to produce

hydrosulfide ions (HS^-). These react with free Ag^+ cations in solution to form Ag_2S, shown in Equation 3-1. Once the concentrations of the reactants exceed the K_{sp} of Ag_2S in water, deposition will occur. The onset of precipitation depends on the coupling of pH and relative concentrations of the reactants. The pH affects the concentration of free SH^- produced from hydrolysis of thiourea, and free Ag^+ by modifying the strength of the chelating agent. Meherzi quantified these precipitation conditions by calculating the equilibrium SH^- and Ag^+ concentration as a function of pH [82].



Equation 3-1: Reaction of Thiourea with OH- to form SH-

Although there are a plethora of publications describing CBDs, few of these explicitly address stability of the chemical bath. In the ideal CBD, heterogeneous deposition forms a dense layer on the substrate. In real cases, uncontrolled homogeneous nucleation also occurs, forming a porous layer. A quantitative thermodynamic analysis described in the literature, has determined that solubility is a key parameter for stability [88]. Materials having a higher aqueous solubility are more likely to have a stable chemical bath. Zinc Oxide has a solubility of 1.6E-3g/mL in water and has a stable CBD process [86][88]. Inversely, Silver sulfide has a very low solubility of 8.5E-18g/mL in water, and to the knowledge of this author, does not have any stable CBD process. Several published Ag_2S CBD processes were run in the lab, all resulting in uncontrolled homogeneous nucleation of Ag_2S [81-83], [87], [89]. Electrical testing of these films did show resistance switching, thereby affirming filament formation, but the instability of the process affected reproducibility.

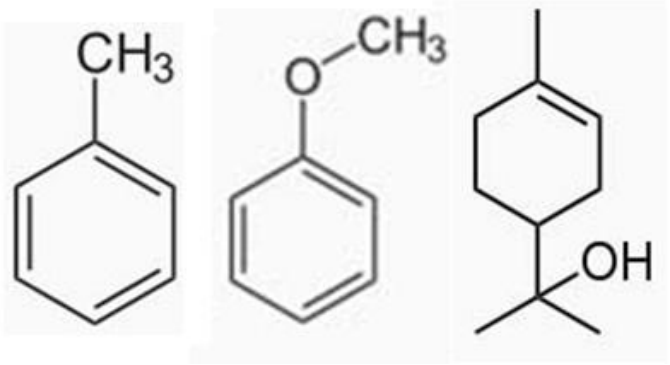
3.1.2: Sulfidation Method

Given the stability problems with Ag_2S CBDs, solution-based sulfidation of silver was investigated as an alternative method to form silver sulfide thin films. Sulfidation is defined here as the conversion of elemental silver films to silver sulfide by reaction with molecular sulfur. This process is similar to solid synthesis of metal chalcogenide compounds through high temperature reaction of components in a furnace crucible. Although sulfidation may superficially resemble silicon oxidation in conventional CMOS processing, the study presented here shows significant differences in the diffusing species and resulting film quality.

The use of various vapor sulfidation methods to produce functional films and devices has been demonstrated in the literature. Terabe et al fabricated a 100 nm x 150 nm cross bar structure by using thermally-cracked sulfur vapor [27]. The device was a silver/silver sulfide/air gap/platinum stack. Silver filaments were reversibly formed and dissolved across the 1 nm air gap. The devices were program/erased to 1E5 cycles and switched as fast as 1 µs. Thomson et al replicated the device by using SF_6 in a reactive ion-etching (RIE) tool to produce sulfur species for sulfidation [90]. Analogously, Liang used H_2S gas to sulfidize evaporated copper films to fabricate Cu_2S switching devices [91]. Although vapor sulfidation has been applied to both

copper and silver films, detailed studies show that a single crystal phase results for Ag_2S, but multiple phases result for Cu_XS that depend on stoichiometry [41], [92], [91]. This difference in the number of crystal phases arises from the multiple oxidation states of copper compared to the single oxidation state of silver. Although Cu_2S may be preferable for CMOS integration, Ag_2S is simpler to process and study.

The sulfidation methods discussed previously were all vapor based. In order to conduct solution based sulfidation, a solution based reaction medium is needed. Sulfur is soluble in aromatic organic solvents such as toluene, anisole and technical grade α-terpineol, but insoluble in aliphatic solvents such as hexanes and tetradecane. The molecular structures of the stabilizing solvents and solubilities are provided in FIG 3-1. Toluene-sulfur solutions are selected for study because of low solvent cost.



Solvent Name	Toluene	Anisole	α-Terpineol
Sulfur Solubility	~15mg/mL	~15mg/mL	<15mg/mL

FIG 3-1: Sulfur Solubilities in various aromatic solvents

The sulfidation is done by immersing silver films into the sulfur solutions. Benefits of this method include plastic compatible process temperature (<150C), high process throughput, easy bath replenishment, and self-alignment to previously formed silver patterns. The procedure is also safer than vapor sulfidation by corrosive H_2S gas. Because the bath solvent is toluene, process temperatures are limited below the 110C boiling point and compatible with plastic substrates. This process can even be done at room temperature, but with a long reaction time as described later in a sulfidation rate study. The bath can be used in reel-to-reel fabrication, whereby silver patterns on plastic sheets are passed through a sulfur bath for a fixed dwell time to convert the silver film. Because the sulfidation occurs at the metal solution interface, there should be no homogeneous reaction in the bulk solution. Because there are no byproducts of the sulfidation released into the bath, sulfur only needs to be added into the solution to replenish the bath. The sulfidation can also be used as a self-aligned process to fabricate dense arrays of devices with a simple process flow. The initial silver layer may be patterned by lithography of silver deposited via vapour techniques such as evaporation, or direct printing of nanoparticles. Sulfidation of this layer would produce a self-aligned silver/silver sulfide stack. Deposition of a top inert metal contact would complete the memory cell. This self-alignment aspect of sulfidation avoids an additional patterning step for the Ag_2S.

To understand how the film evolves during sulfidation, quantification of sulfidation rates is necessary. Therefore, a sulfidation rate study is first conducted, followed by characterization by X-ray Photoelectron Spectroscopy (XPS), X-ray diffraction (XRD), Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) to explore stoichiometry, crystal phase, and surface roughness during the process.

3.2: Sulfidation Rate Study

Silver sulfide has two dominant crystal phases below 500C: the low temperature acanthite phase stable below 179C, and high temperature argentite phase stable above 179C [93]. The acanthite phase has an optical bandgap of about 1 eV, while silver has no bandgap and is opaque to light [94]. The rate of sulfidation is measured by quantifying transmission of sulfidized silver films at various bath temperatures, concentrations and time points.

Experimental:

Sublimed sulfur powder (99.98% trace metals basis) and Toluene were purchased from fisher scientific and used without further modification. Sulfur solutions were prepared by dissolving sulfur powder in toluene at various concentrations (0.26M, 0.82M, 1.2M) and temperatures, stirring at 150 RPM in a 100 mL beaker, heated by a mineral oil bath. Sulfur's solubility limit in toluene was approximately 0.46M at 25C but increased to 1.2M at 80C. This set the upper bound on concentration at various temperatures.

Sample substrates were prepared as follows. 1mm thick glass slides were piranha cleaned, then rinsed with acetone and isopropanol (IPA). 23Å of chrome adhesion layer and 620Å of silver were thermally evaporated onto the glass. The chrome adhesion layer was necessary to prevent de-lamination of the silver film from the SiO_2 that would occur under long sulfidation times. These films were sulfidized under various bath temperatures and times. The wait time between evaporation and sulfidation was limited to less than 1 week to prevent formation of surface layers that could impede sulfidation. Silver films that had been left out in ambient air for several months, or exposed to UV-Ozone treatment did not sulfidize at the same rates as freshly prepared films. Transmission was measured on a shimadzu UV-VIS spectrophotometer. Upon removal from the bath, samples were rinsed with toluene to wash off the sulfur solution, then rinsed with acetone and IPA, and dried with compressed air.

Results:

Representative transmission spectra of sulfidized films are illustrated in FIG 3-2 and FIG 3-3. In FIG 3-2, the progression of the transmission spectra versus sulfidation is shown. A cut-off of UV transmission around 280nm (4.4eV) is observed on the glass slide, but does not affect the transmission spectra in the region of interest around the acanthite bandgap at 1.13um (1.1eV). The film turns from opaque to transmissive as the silver converts to silver sulfide, eventually saturating at a maximum value. A silver plasmon peak observed at 320nm rapidly disappears with conversion corroborating the reaction of silver.

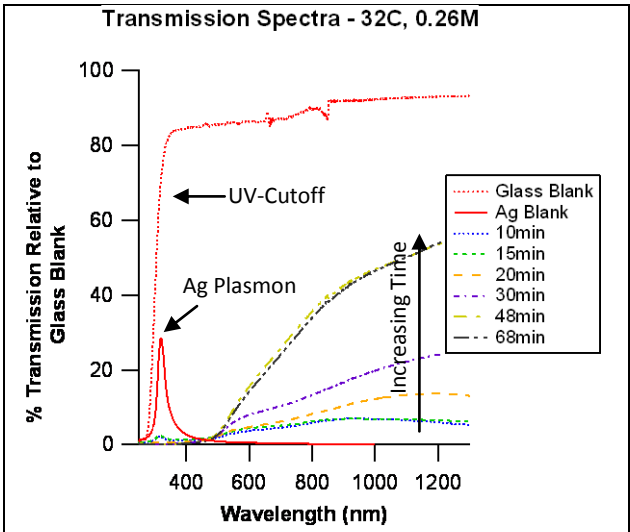


FIG 3-2 Transmission Spectra versus Time

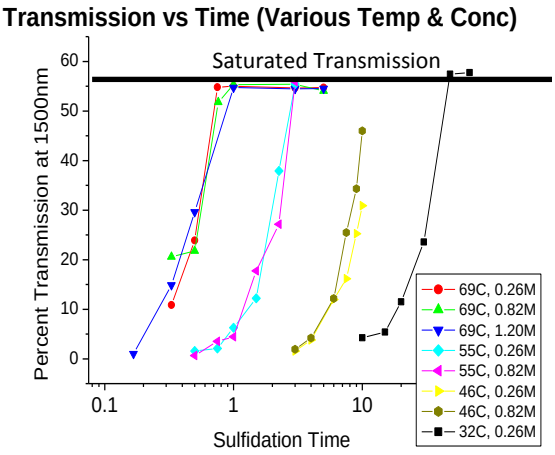


FIG 3-3 Transmission versus Time, Various Baths

FIG 3-3 shows transmission measured at 1500 nm (0.83 eV), a value below the acanthite bandgap, as a function of various bath temperatures and concentrations. Transmission for the samples all saturate around 56%. In order to quantify the extent of sulfidation, a sulfidation threshold time is defined as the least sulfidation time needed to saturate transmission at a particular bath temperature and concentration for a 23Å Cr/620Å Ag film. Dependence of sulfidation threshold time on silver film thickness has not been explicitly tested in this study. The independence of sulfidation threshold time from concentration as shown in FIG 3-3, combined with the single activation energy dependence illustrated in FIG 3-4 suggests that the process is limited by surface reaction.

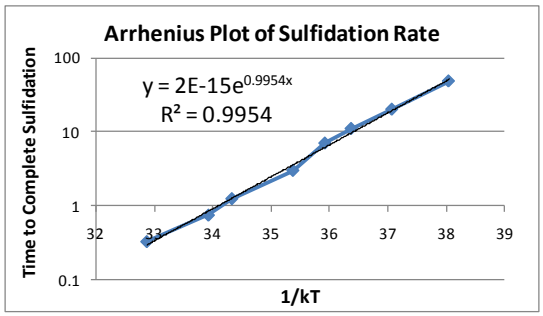


FIG 3-4: Arrhenius Plot of Sulfidation Times

Given information about the sulfidation rates, further materials characterization was performed. Table 3-1: lists test conditions that span temperature, and times before and after the sulfidation threshold. The τ in the table are the sulfidation time normalized to the sulfidation threshold time. τ = 1 corresponds to the first onset of saturated transmission measured by UV-VIS.

Sulfidation Times (min)			
τ	**40C**	**65C**	**80C**
0.3	6	0.375	
0.5	10	0.600	0.16
1	20	1.250	0.33
2	40	2.500	0.66
5	100	6.250	1.50
10			3.00

Table 3-1: Sulfidation Times, τ =1 is the normalized time to onset of saturated transmission by UV-VIS

3.3: Materials Characterization

Experimental:

The silver sulfide samples used for materials characterization were prepared on 1000Å of thermal oxide on silicon instead of glass to provide a smooth starting surface for AFM measurements, and facilitate easy cleaving into smaller test pieces. A subset of the samples were split and annealed at 190C for 15 minutes in nitrogen to evaluate the impact of heating beyond the phase transition temperature on the film structure.

3.3.1: X-Ray Photoelectron Spectroscopy (XPS)

XPS was measured on a PHI VersaProbe Scanning XPS Microprobe. The spectral peak intensities were baseline subtracted, integrated, and scaled by relative strength factors. The stoichiometric composition as extracted from XPS is illustrated in FIG 3-5. At longer normalized sulfidation times, the relative sulfur content of the film increases. Post-sulfidation heat treatment increases silver content within the surface film. These observations are consistent with previously reported results on vapour sulfidized films [41]. More sulfur is incorporated into the film with longer reaction time. Annealing the samples is hypothesized to cause silver diffusion to the surface from the bottom layers, thereby raising surface silver content.

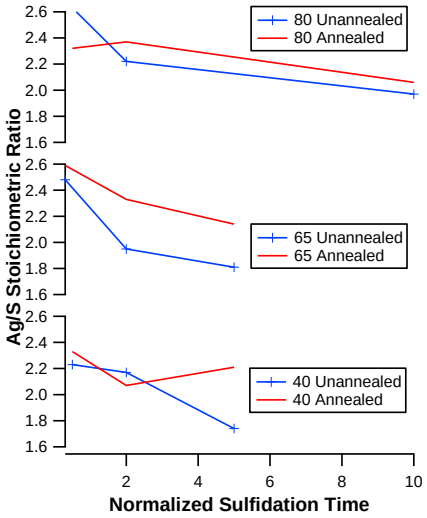


FIG 3-5: Silver Sulfide Stoichiometric Ratio

3.3.2: X-Ray Diffraction (XRD)

Specular 1D diffraction was measured on the films using a Siemens D5000 powder diffractometer at a wavelength of 1.54 Å. To further elucidate observations in the 1D data, grazing incidence x-ray diffraction (GIXD) was used to measure 2D areal data. GIXD was done at Stanford Synchrotron Radiation Light Source (SSRL) on beamline 11-3, at a detector distance of 200 mm, a wavelength of 0.97 Å and a grazing angle of 0.3°. Grazing geometry increased the diffracted signal by providing a long path for the x-ray beam through the film, and provided a complete record of reciprocal space. Collecting areal diffraction data in specular mode cut off some information as parts of the diffracted beam are physically blocked at the bragg angle by the sample [95]. In-situ heating GIXD measurements were also done to examine the effect of temperature on the texture and phase of the films. The sample was heated in 10 degree increments, dwelling at each temperature for about 25 minutes for each measurement.

FIG 3-6 shows the measured 1D diffraction pattern for samples sulfidized to 5 normalized times at 40C and 65C, and 10 normalized times at 80C. The peaks are indexed to the low-temperature acanthite phase as listed in the JCPDF card file 14-72. An intense peak at 33.18° is attributed to crystalline coesite from the wet oxide substrate [96]. The presence of the high temperature phase, argentite, cannot be definitively confirmed by X-ray measurements due to close proximity to the acanthite peaks. However, argentite and acanthite have different bandgaps, 0.4 eV versus 1 eV [94][97]. Measured transmission of silver sulfide before and after heat treatment did not show any change suggesting that no high temperature phase remains.

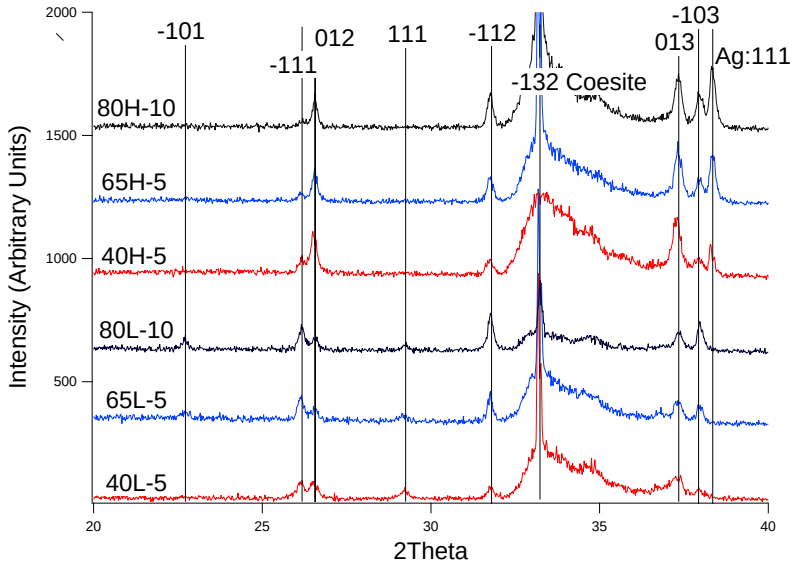


FIG 3-6: Diffraction Patterns for Long Sulfidation Time Samples, Pre Heating (L) and Post Heating (H)

The films that underwent the post sulfidation anneal show a strong Ag 111 peak, and change in several relative peak intensities at the -111/012 and 013/-103 indices. The areal diffraction data in FIG 3-7 corroborate the 1D data. A vertical slice along the Qz axis in the 2D plots in FIG 3-7 corresponds to the 1D specular diffraction data in FIG 3-6. FIG 3-7A,C,E show the sulfidized films before annealing and, FIG 3-7B,D,F show the sulfidized films post annealing, in the 40C, 65C and 80C baths respectively. In all post annealed samples, granular untextured

silver is observed. In-situ heating measurements show that this granulation of silver begins around 150C and continues through the phase transition at 178C. Although several arcs that are close in proximity cannot be individually resolved in the 2D data, the change in texture is still observed as changes in intensity versus radial angle along the -101, 111 and 031 arcs.

The debye-scherrer crystallite sizes are extracted from the -112 peak of FIG 3-6, and plotted in FIG 3-8. The -112 peak was selected since because it appears in all samples with clear intensity. It is located far from other peaks, allowing clear extraction of the full-width at half-max (FWHM). The crystallite size uniformly increases at higher bath temperatures and is reduced by post annealing.

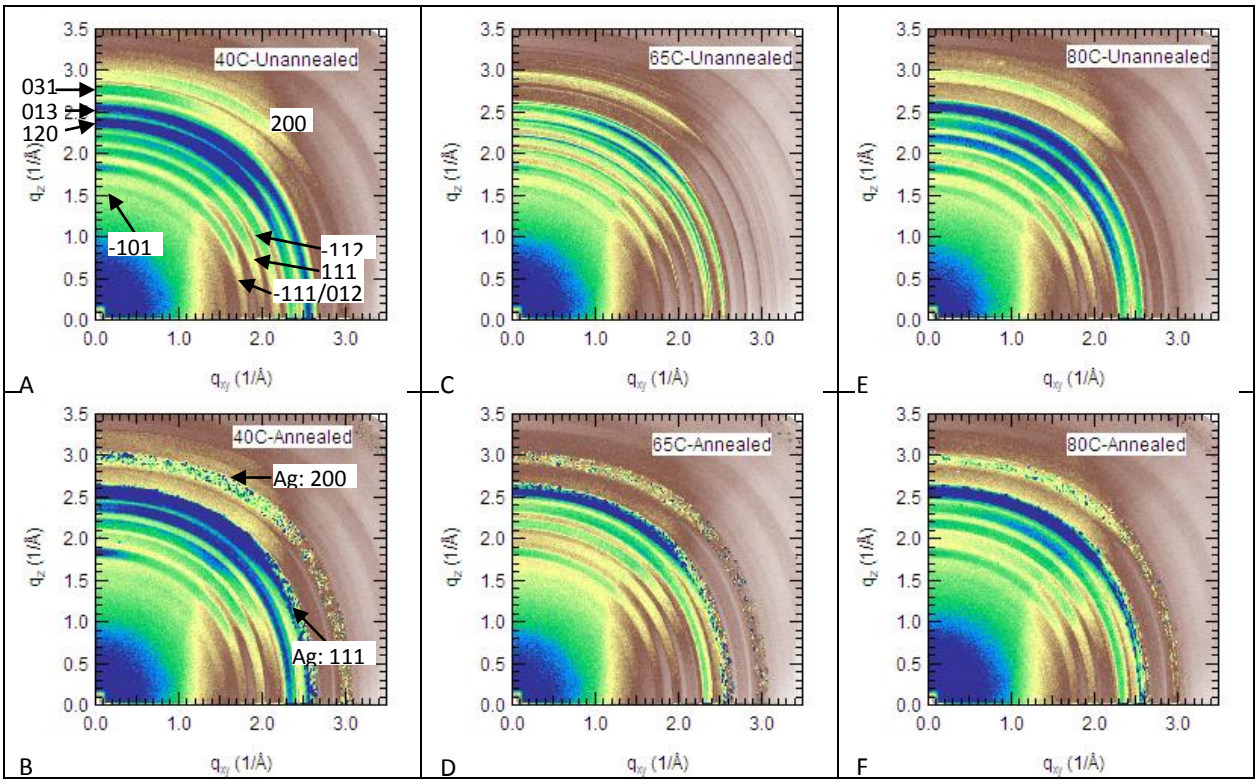


FIG 3-7: Areal Diffraction Patterns Before & After Annealing, Long Sulfidation Time

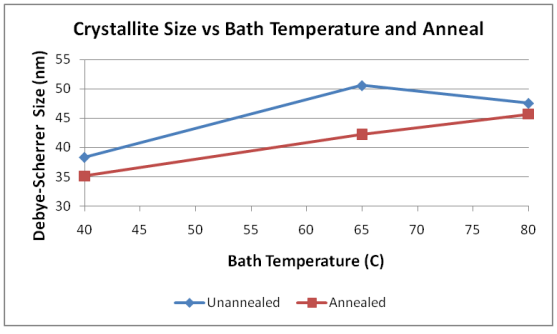


FIG 3-8: Debye-Scherrer Crystalite Size of -112 Peak

3.3.3: Atomic Force Microscopy & Scanning Electron Microscopy

Evolution of film surface roughness with time is measured across a 5 um x 5 um area. Low surface roughness of the electrolyte layer is critical to fabricating functional vertical devices in compact crossbar-array memories. FIG 3-9 illustrates the surface morphology of films sulfidized for 1 normalized time. Results are shown for different bath temperatures, before and after anneal. The reduction in surface roughness is apparent in the fewer number of intensity oscillations across the surface.

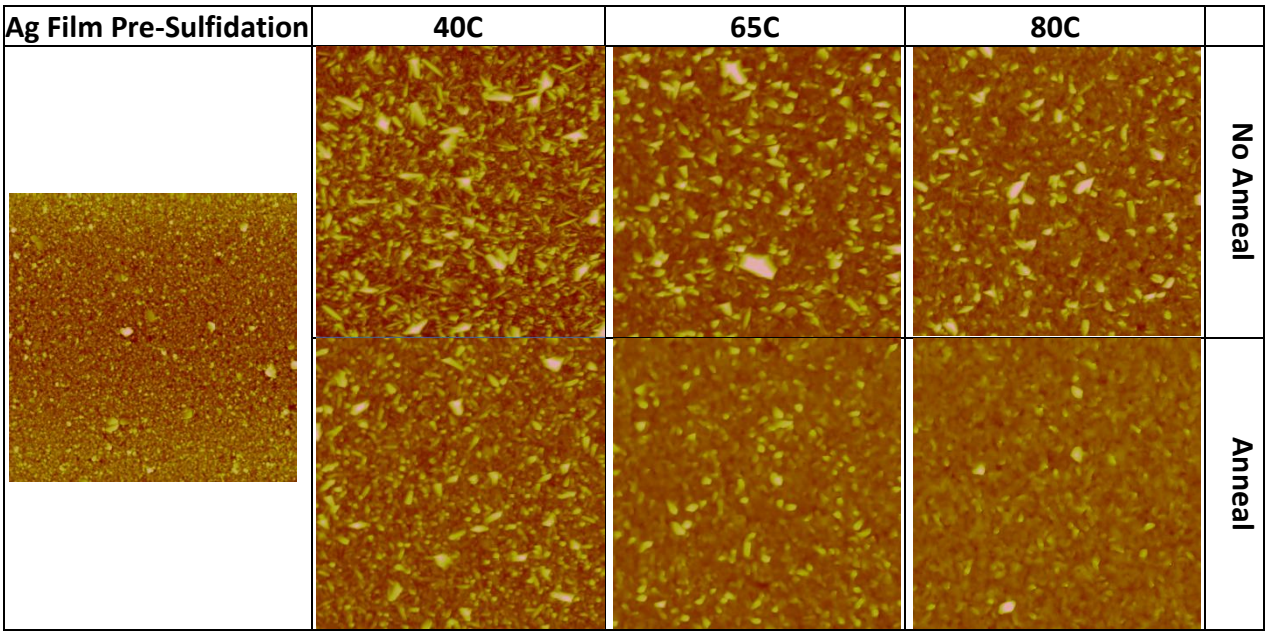


FIG 3-9: 5um x 5um AFM of film pre and post anneal after 1 normalized sulfidation time at various bath temp

The extracted rms roughness is plotted versus sulfidation time and temperature in FIG 3-10. Surface roughness increases with sulfidation time under all conditions. Higher temperature baths have lower surface roughness, and post-annealing slightly reduces roughness at time constants less than 1, in silver rich films.

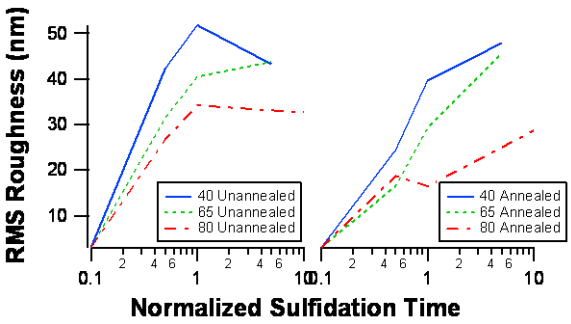


FIG 3-10: Roughness of Films Before and After Anneal

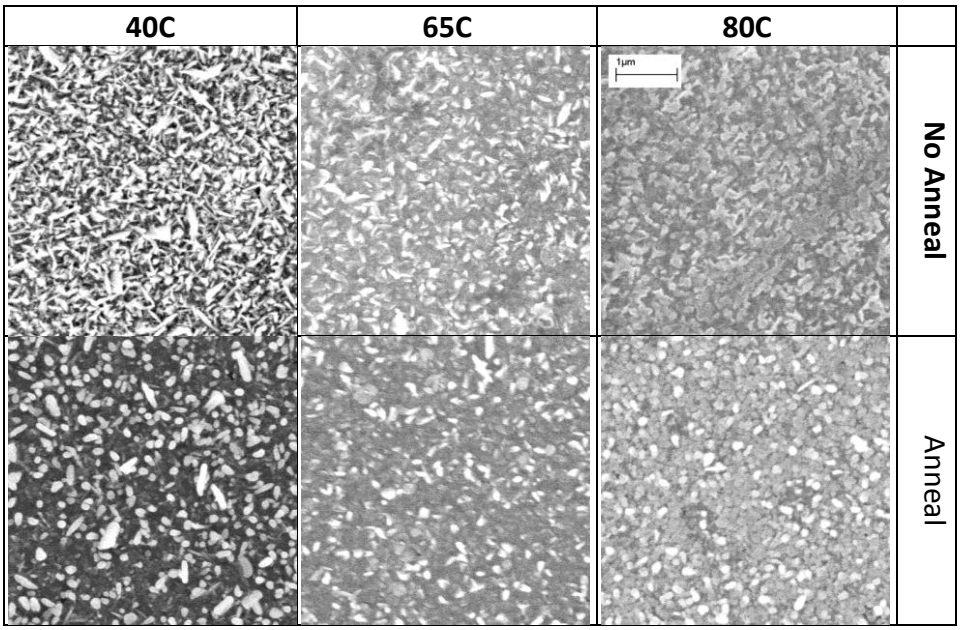


FIG 3-11: SEM of film surface after long sulfidation time at various bath temperatures

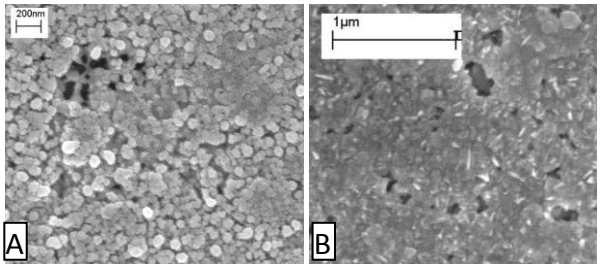


FIG 3-12: Close up SEM of Film Sulfidized in 80C Bath (A) 0.3 Normalized Time (B) 10 Normalized Time

SEM images of the Ag_2S surface are shown in FIG 3-11 after long sulfidation times: 5 normalized times for 40C and 65C, and 10 normalized times for 80C. Corresponding to the AFM images, lower temperature sulfidation results in rougher films. Close-up SEM images of the 80C sulfidation in FIG 3-12 reveal that significant pinholes and porosity develop during the conversion.

3.3.4: Discussion

The sulfidation rate study shows that the process is surface reaction limited through the range of tested conditions with a single dominant mechanism, indicated by the single activation energy. AFM and SEM show that the resultant films are highly porous. These observations contrast with oxidation of silicon wafers which produces a dense adherent oxide layer. Although this studied process is a sulfidation, it may be understood through mechanisms for oxidation of materials. The next sections will review the Deal-Grove model for silicon oxidation, Pilling Bedworth Ratio qualification of oxides, and the generic model for transition metal oxidation. The objective of this review is to compare the assumptions of these models, and understand their applicability to the experimental results from the sulfidation study.

The Deal-Grove model can accurately account for results from oxidation of single crystalline wafers. It makes the following assumptions: 1) oxygen is the diffusive species while Si remains fixed, 2) the oxidant goes through 3 steps in the process: transport across a stagnant boundary layer, transport across a growing oxide layer and reaction at the Si-SiO_x interface[98]. Initial oxidation is surface reaction limited due to fast oxidant transport across a thin oxide layer. The thickness is linearly dependent on oxidation time in this regime. Subsequent oxidation is transport limited by diffusion of oxidant species through the growing oxide layer. The thickness shows a parabolic dependence on oxidation time in this regime.

Although the Deal-Grove model accurately predicts results for single crystal silicon, the model breaks down for polycrystalline films. Different crystal planes with varying surface atom densities will oxidize at different rates in the linear regime, resulting in uneven growth across the film surface. In the transport limited regime, oxidant species diffuse significantly faster at grain boundaries resulting in higher oxidation rates.

The Deal Grove model was developed specifically for oxidation of single crystalline silicon which produces a dense adherent layer, and only has the oxidant as the mobile species. However, these results are a very specific case. The oxidation of transition metals produces vastly diverse empirical results. Some metals such as aluminum and chrome form protective dense adherent oxides similar to silicon oxide, while others such as iron form inadhesive oxides.

$$\mathrm{R_{PB}} = \frac{\mathrm{V_{oxide}}}{\mathrm{V_{metal}}} = \frac{\mathrm{M_{oxide}} \cdot \rho_{\mathrm{metal}}}{\mathrm{n} \cdot \mathrm{M_{metal}} \cdot \rho_{\mathrm{oxide}}}$$

Equation 3-2: Pilling-Bedworth Ratio

The Pilling-Bedworth ratio provided in Equation 3-2 is often used to qualify the morphology of oxidized metal layers, and can be applied to sulfidized metal layers [99]. It qualifies stress between the oxide and metal by comparing the molar volumes of the metal and corresponding oxide/sulfide. M is the molar mass, ρ is the mass density, and n is the number of metal atoms per oxide molecule. When the molar volume of the oxide is much smaller than the metal (R_{pb} < 1), the oxide layer is cracked and porous from tensile stress. When the molar volume of the oxide is much larger than the metal (R_{pb} > 2), the oxide layer will break off from the surface in segments from compressive stress. When R_{pb} lies between 1 and 2, the oxide should be a dense, adherent and passivating layer. Examples of adherent oxides and corresponding ratios are SiO_2 (2.15), Alumina (1.28) and Titania (1.73). Magnesium oxide (0.81) is an example of a poor oxide that cracks from contraction, and vanadium oxide (3.25) is an example of an oxide that breaks off due to expansion. The pilling-bedworth ratio for Ag_2S/Ag is 1.66, indicating that considering only film stress, a dense passivating layer should be formed, contrary to experimental observations. A key assumption common to both pilling-bedworth analysis and the deal-grove model is that only the oxidizing species diffuses through the forming oxide. As shall be discussed in the next section, this assumption does not hold for the Ag/Ag_2S system.

The most generic model for transition metal oxidation is similar to the deal-grove model, but includes diffusion of both the metal and oxidant species through the oxide [49][50]. In

Ag_2S, silver, not sulfur is the dominant diffusive species [100]. As Ag diffuses into the growing sulfide layer, the metal boundary recedes causing the formation of pores in the film. This mechanism is illustrated in FIG 3-13B, and contrasted to oxidation of single crystal silicon shown in FIG 3-13A. The silver reacts at the Ag_2S/S solution interface, not the Ag_2S/Ag interface. Channels through the porous film facilitate direct transport of sulfur species to the silver surface, instead of diffusion through a boundary layer, explaining why the sulfidation process was surface reaction limited as observed in the rate study. The silver diffusion is not unique to processes using bulky molecular sulfur. Both silver and copper ions are highly mobile in the respective metal sulfides. Liang visually observed void formation in cross-sectional TEMs on copper films sulfidized with sulfur vapor and H_2S gas [91].

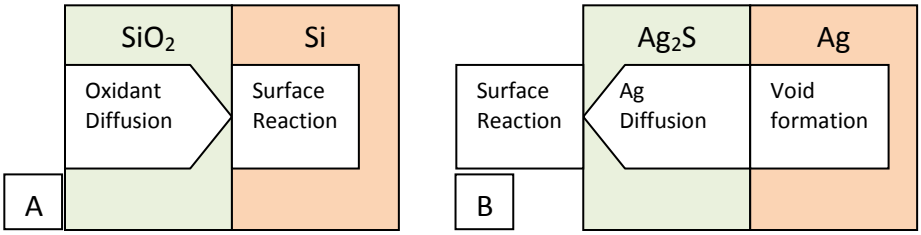


FIG 3-13: (A) Oxidation by Diffusing Oxidant (B) Sulfidation by Diffusing Metal Species

The sulfidation process likely results in a gradient of silver with high concentration near the bottom of the film and low concentration near the surface. XPS and XRD results provided in the previous section support this. XPS has shown that the surface silver content decreases relative to sulfur with increasing sulfidation time. XRD has shown that the post-annealing treatment causes precipitation of silver from the Ag_2S and reduces grain size of the Ag_2S. In-situ heating XRD shows that the precipitation starts around 150C. Some of these results may be explained by referring to the phase diagram of Ag2S, shown in FIG 3-14. The next sections will briefly review phase diagrams, then examine the phase diagram of Ag_2S.

Phase diagrams represent conditions of thermodynamic equilibrium, but materials may exist in different kinetic states. Different methods of preparation result in the materials having the same composition, but different microstructures and physical properties. A microstructure is defined as a spatial configuration of component species in a material [101]. The iron-carbon system provides an example of various microstructures and effects on material properties. Slow cooling from a melt results in large precipitates near grain boundaries and a brittle bulk material, and fast cooling results in fine precipitates dispersed throughout iron grains and a ductile bulk material. Tempering through subsequent heat treatment can further change the microstructure by formation of precipitates. As temperature increases, the diffusivity of species in a material increases. This facilitates higher rates of species transport to form precipitates and second phases in a material that would otherwise not form on observable time scales at low temperatures. The precipitates are likely to form at interfaces such as grain boundaries that reduce the overall surface energy.

Given the phase diagram of Ag_2S and basic understanding of phase transitions some of the experimental results can be interpreted. According to FIG 3-14, Ag_2S is stable across a narrow

stoichiometric range in the α–phase (acanthite), and slightly wider range in the β-phase (argentite). The silver precipitation observed by XRD is likely occurring near grain boundaries in silver rich regions of the film. The silver precipitation near grain boundaries reduces the observed grain size after heating and phase-transition, shown in FIG 3-8.

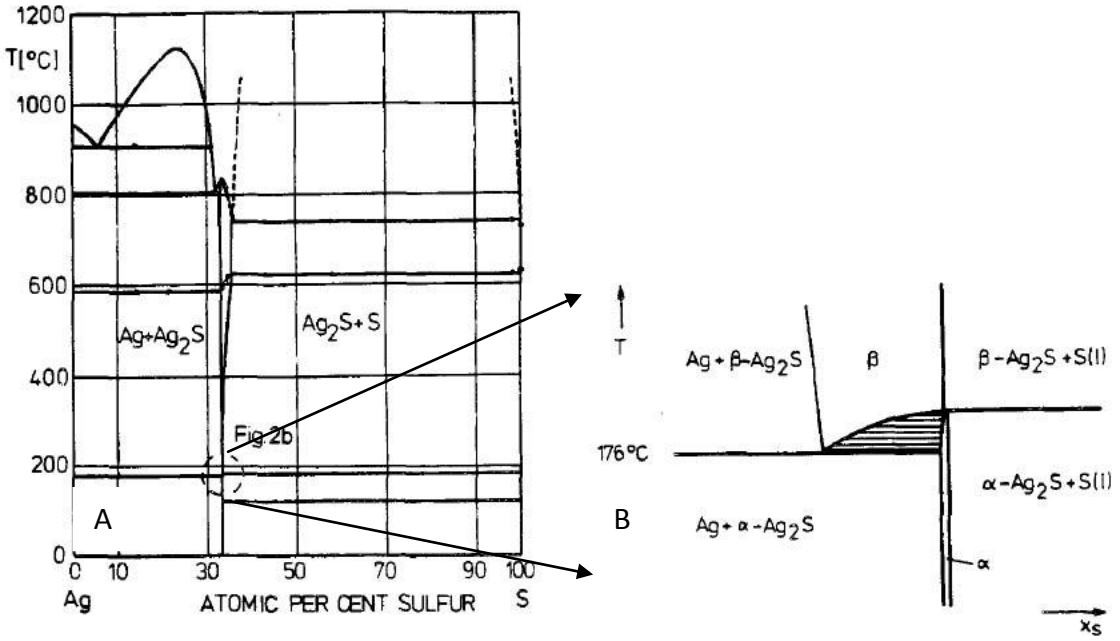


FIG 3-14: (A) Phase Diagram for Ag2S (B) Expansion around stoichiometric composition and phase transition [48]

A reduction in surface roughness is also observed by AFM, shown in FIG 3-10 and FIG 3-11. Previous studies on Ag_2S films produced by sequential thermal evaporation have yielded morphologies similar to those formed by the solution based sulfidation [102]. Densification of the porous film is used to explain the reduction in surface roughness. FIG 3-5 and FIG 3-10 show that excess silver is correlated with this smoothing effect.

3.4: Electrical Characterization

After completing materials characterization, electrical testing was done on the sulfidized films to examine switchability via filament formation through the films. Due to high surface roughness and porosity, as shown by AFM and SEM, vertical MIM devices with top contacts could not be successfully fabricated. Tested vertical devices were all shorted through pinholes. To circumvent this issue, devices were fabricated in a vertical stack with a blanket gold electrode as a bottom contact, and tungsten probe as a top contact as shown in FIG 3-15. Pulse testing was employed to control time of applied voltages. An HP4156C parametric analyzer was used for measurements.

Experimental:

500 Å of gold on 23 Å of chrome adhesion layer are first thermally evaporated onto 1000 Å of thermal oxide on silicon. 620 Å of silver is then evaporated on top of the blanket gold contact and sulfidized at various normalized times and temperatures. Post sulfidation

annealing is not explicitly tested. Effect of film thickness on switching is investigated by sulfidizing a thicker 1400 Å silver layer on a blanket gold bottom contact. The sulfidation condition was 80C-1.2M for 1 minute, about 1 normalized sulfidation time when scaled for thickness.

FIG 3-16 shows the I-V curve of a typical device that is tested through a forming and erase cycle. To form a filament, the top tungsten contact is double swept from 0V to -1V to 0V in 10 ms pulses with 1ms duty cycle. To break the filament, the top contact is double swept from 0V to 0.6V to 0V. On-state resistance is measured from the forward positive sweep, and off-state resistance is measured from the backward positive sweep.

Results and Discussion:

All tested films across the various sulfidation times and temperatures demonstrated resistive switching behavior. On-state resistance through the formed filaments was approximately 5-8 ohms in all cases, with a tight distribution as shown in FIG 3-17. There was higher variation in the off-state resistance ranging from 50-300 ohms. The tight distribution of the on-states is caused by limiting the current during formation. The variability of the off-state is attributed to uncertainty of penetration height from using a probe tip contact.

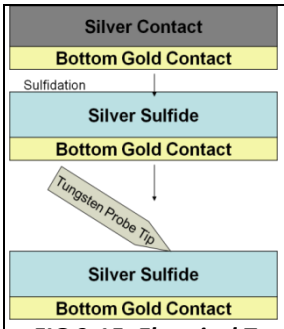


FIG 3-15: Electrical Test Setup

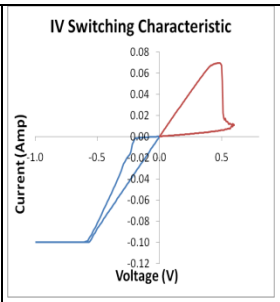


FIG 3-16: IV Switching from a sample sulfidized at 80C for 10 time constants

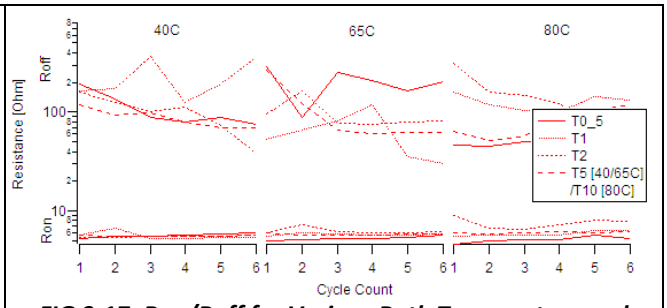


FIG 3-17: Ron/Roff for Various Bath Temperature and Normalized Sulfidation Time

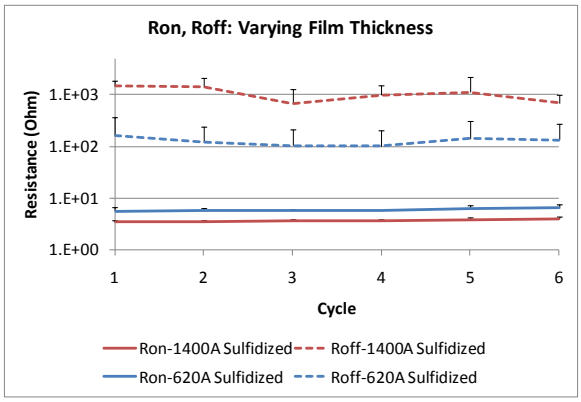


FIG 3-18: Ron, Roff for varying Film Thickness. The 1400A sulfidized film shows higher off-state resistance compared to the 620A sulfidized film.

R_{off} values for the 1 minute sulfidized sample are higher, around 1 kΩ as illustrated in FIG FIG 3-18. This shows that off-state resistance is highly dependent on bulk film properties [103]. Previous studies on Cu_2S films prepared by solution based anodization of copper have shown similar thickness dependence of R_{off} [103]. Given constant on-state resistance, the R_{on}/R_{off} ratio of devices can be tailored by adjusting thickness to vary R_{off}.

3.5: Conclusions

Solution processed silver sulfide films have been formed by sulfidizing evaporated silver films in toluene-sulfur solutions. The sulfidation process occurs by diffusion of silver through the forming sulfide layer, instead of sulfur diffusion. This is inherently different from silicon oxidation in which the O_2 or H_2O gaseous oxidant diffuses through the forming layer. Consequently, sulfidation results in a rough porous film instead of a dense adherent one. Post sulfidation anneal raises surface silver content, causes silver precipitation, and lowers surface roughness. This sulfidation process produces films that exhibit bi-polar switching, but are too rough to use with deposited contacts.

The diffusion of metal species during sulfidation places an upper limit on sulfidized thickness before significant porosity results in shorted devices. Although device yields have not been reported for Ag_2S devices formed by vapour sulfidation, one paper reported an optimal sulfidized layer thickness of 20 nm [90]. Further optimization will be required to reduce surface roughness to facilitate integration into metal-insulator-metal (MIM) vertical devices. However, if the sulfidation process proceeds via silver diffusion rather than sulfur diffusion through the growing sulfide layer, the utility of the process may be limited to very thin sulfide layers because of pore formation.

Chapter 4: Sintered Octadecylamine Capped Ag_2S Nanoparticle Films

The sulfidation process presented in the previous chapter has several inherent problems including porosity and variable stoichiometry. Diffusion of silver into silver sulfide creates voids and pores as the silver film is sulfidized. The interfacial conversion of silver forms non-stoichiometric films with a gradient spanning the thickness of the sulfidized film. To circumvent these issues, sintering of Ag_2S nanoparticles is studied as another method of forming films for resistive switching devices.

Sintered nanoparticle films are attractive because of printability, and control over stoichiometry and grain size. Nanoparticles of gold, silver, and copper have been printed and sintered to form passive devices such as inductors and source-drain electrodes for thin film transistors (TFTs) [16][11][104]. Semiconducting nanoparticles of ZnO have also been used to form the active layer in TFTs [105]. Through inkjet printing, silver sulfide nanoparticle inks may be directly deposited onto electrodes to fabricate memory cells.

Nanoparticles of thermodynamically stable compounds ideally can be synthesized. Thin films formed by deposition of nanoparticles should be more homogenous in composition than sulfidized films which have a silver gradient. Through different heat treatments, the particles can be sintered into continuous films with controllable grain size [106]. Thus sintered nanoparticle thin films provide a good test bench for exploring the effect of grain size on mixed ionic-electronic conducting properties. In this chapter, effect of sinter temperature on the structure of sintered octadecylamine (ODA) encapsulated silver sulfide films are studied by ex-situ X-ray diffraction (XRD), thermogravimetric analysis (TGA) and differential scanning calorimetry (DSC) and correlated to the mixed ionic-electronic properties measured by electrical impedance spectroscopy (EIS).

4.1: Nanoparticle Synthesis

4.1.1: Background on Nanoparticle Synthetic Methods

Various strategies exist for forming nanoparticles through either a top-down or bottom-up approach. Top-down methods are generally variations of mechanical milling, which is a process to form nano-size powders but has poor control over size distribution and shape of nanoparticles. Bottom up approaches include gas-phase synthesis and liquid-phase colloidal synthesis, and can form nanoparticles as small as 5 nm. Colloidal synthesis is defined as a wet chemical process that produces a disperse solution of nanoparticles. Liquid phase synthesis is preferred because of the relative ease of working with liquids compared to gases. Synthetic conditions such as temperature and starting reagent concentrations control the shape, size and solubility of nanoparticles. The basic mechanism behind colloidal synthesis is the controlled precipitation of the desired material from bulk solution. Surfactants are used as capping materials on the nanoparticles to control their growth and disperse them to prevent agglomeration.

There are two generic approaches to colloidal synthesis: high temperature thermolysis of organic precursors by the “hot-injection” method, and low temperature precipitation from

aqueous solutions. The high-temperature organic method forms nanoparticles that have higher monodispersity and contain fewer defects as measured by photo-luminescence [107]. However, the low-temperature aqueous method is easier to scale to larger batches of nanoparticles. The synthesis used in this chapter is a variant of the high-temperature organic synthesis, and will be reviewed subsequently. In the following chapter, an aqueous synthesis method is used and described in further detail.

The key to forming monodisperse nanoparticles is to temporally separate the nucleation and growth phases. La Mer and Dinegar demonstrated that formation of colloidal sulfur sols was dependent on a fast initial nucleation event termed "burst nucleation," followed by growth on existing nuclei [108]. Murray et al is credited with first applying this principle to semiconductor nanoparticle synthesis and setting the foundation for the hot-injection method [109][52]. The specific compounds synthesized were CdS, CdTe, and CdSe. A mixture of metal and chalcogen organic precursors at room temperature was rapidly injected into a flask of hot (~300C), vigorously stirring solvent and surfactant. Rapid thermal decomposition of the precursors caused the "burst nucleation" of metal chalcogenide. Rapid undercooling of the reacting solution caused by addition of the room temperature solution arrested nucleation and facilitated growth of the initial nuclei at a lower temperature.

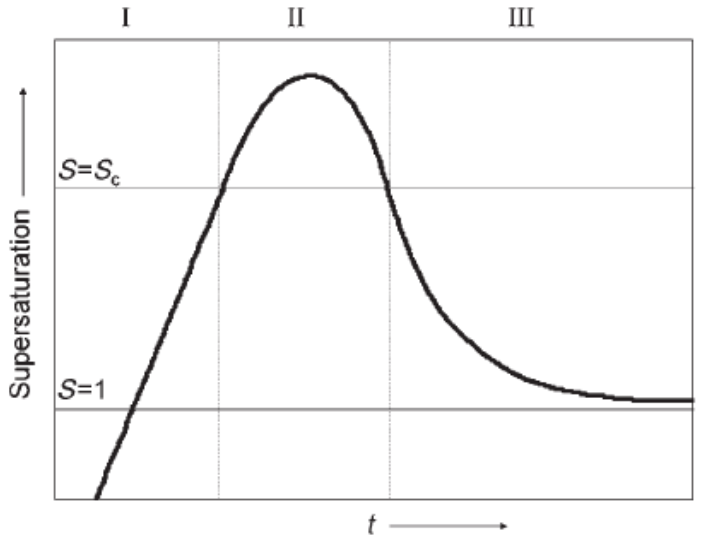


FIG 4-1: La Mer Plot. S=1 is equilibrium solubility. S=Sc is critical supersaturation. [110]

Mechanistic studies have used classical nucleation theory to explain the kinetics of the nanoparticle formation [110][111]. Homogeneous nucleation models synthesis of nanoparticles directly from precursors. Heterogeneous nucleation models seed-nucleated growth whereby core-shell nanoparticles are formed by growth of material around pre-synthesized nanoparticle nuclei. The La-Mer plot illustrated in FIG 4-1 qualitatively illustrates the different periods of nanoparticle synthesis. It neglects effects of surfactants on the surface energy of the nanoparticles. In Region I, the concentration of monomer increases beyond the equilibrium solubility resulting in supersaturation. A monomer is defined as the minimum

subunit of the bulk material. Homogeneous nucleation does not occur due to a high kinetic barrier. This monomer concentration increases until the critical supersaturation level is reached in Region II when homogeneous nucleation of the monomer begins. In Region II, nucleation and growth of existing nuclei occurs consuming monomer until the concentration falls below critical supersaturation. In Region III, homogenous nucleation stops and the nanoparticle nuclei grow by incorporation of monomer from the bulk solution.

The controlled precipitation of nanoparticles can be considered as a phase transition. The thermodynamics and kinetics may be further illustrated by a phase diagram and temperature-time transition (TTT) diagram. FIG 4-2a illustrates a sample phase diagram for solubility of a material in a solvent, and FIG 4-2b illustrates a sample TTT diagram showing kinetics of the precipitate nucleation. The phase diagram represents a two component system, solvent A, and solute B. α is the solid form of A, and β is the solid form of B which is the nanoparticle material.

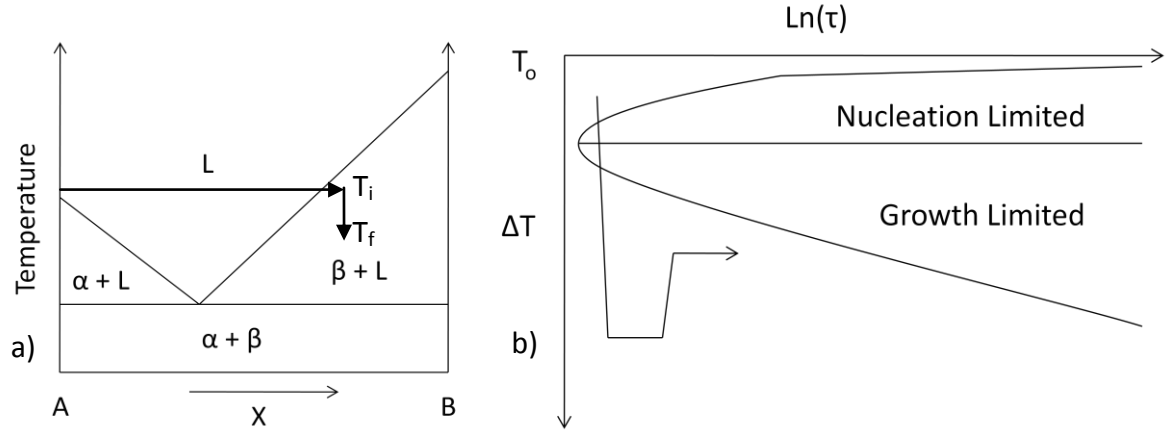


FIG 4-2: a) Sample equilibrium phase diagram b) Sample TTT Diagram. τ is the time to nucleation.

The change in free energy (ΔG) of nuclei formation is the sum of the changes in volume and interfacial free energies [101]. Forming a volume of the stable product phase reduces the volume free energy, but forming the interface between the parent and product phase raises the surface energy. The competition between these two competing effects is summarized in Equation 4-1a.

a) $\Delta G = \frac{4}{3}\pi r^3 \Delta G_v + 4\pi r^2 \sigma$	b) $\Delta G_v = -RTln(S)/V_m$	c) $\Delta G_v = -\Delta H_v \Delta T / T_m$
d) $r_c = \frac{-2\sigma}{\Delta G_v}$	e) $r_c = \frac{2\sigma V_m}{RTln(S)}$	f) $r_c = \frac{2\sigma T_m}{\Delta H_v \Delta T}$
g) $\Delta G_c = \frac{16\pi\sigma^3}{3(G_v)^2}$	h) $\Delta G_c = \frac{16\pi\sigma^3 (V_m)^2}{3(RTln(S))^2}$	i) $\Delta G_c = \frac{16\pi\sigma^3 (T_m)^2}{3(\Delta H_v \Delta T)^2}$
Equation 4-1: a) Free Energy of Nucleus Formation b) Volume Free Energy d) Critical Radius [110][112] ***ΔG_v: free energy change per volume, σ: interfacial energy per surface area, Vm molar volume of product phase, S: super saturation, T: temperature, R = Gas constant, ΔH_v: enthalpy of formation, ΔT = T_o-T: Undercooling***		

The volume term is negative and varies as r^3, and the interfacial surface area term is positive and varies as r^2. A critical radius (Equation 4-1d) can be defined that corresponds to ΔG_c

(Equation 4-1g),or activation energy for nucleation. Particles formed larger than this radius will be stable, while ones formed smaller will dissolve. Equation 4-1b, e, h and c, f, i show the volume free energy, critical radius, and activation energy of nucleation derived for isothermal conditions with variable supersaturation, and isotonic conditions with variable temperature respectively. Under isothermal conditions, supersaturation drives nucleation and lowers the kinetic barrier. Under isotonic conditions, undercooling drives nucleation and also lowers the kinetic barrier . At large undercoolings, ΔG_c becomes small enough that the formation of nuclei is limited by the diffusive transport and incorporation of monomer into the particle. These two competing effects under isotonic conditions are shown as the nucleation and growth limited regions in FIG 4-2b.

Under ideal synthetic conditions, Region I and II of the La Mer plot FIG 4-1 would be completed at high temperature in the nucleation limited region of FIG 4-2b. After relieving the critical supersaturation, and assuming insensitivity of solubility to temperature, a quench of the solution would then arrest the growth of nanoparticles. Paths of a possible hot injection synthesis are illustrated in FIG 4-2a, b. Injection of the precursor solution instantaneously increases the solute concentration generating a supersaturated solution. Depending on specific reaction kinetics, the solution should be quenched just after relief of the supersaturation. Contingent on residual supersaturation, the solution may be heated to grow the nanoparticles consuming the excess monomer and focusing the size distribution. Continued heating upon depletion of the supersaturation will cause ostwaldt-ripening which will defocus the size distribution resulting in poly-disperse nanoparticles [113][110][114].

4.1.2: Synthesis of Octadecylamine Encapsulated Ag_2S Nanoparticles

Octadecylamine encapsulated Ag_2S nanoparticles (ODA-Ag_2S NP) are synthesized using a type of high temperature organic synthesis reported by Li et al [114]. The nanoparticles are monodisperse with 10 nm diameter. A representative TEM illustrates the particle size and distribution in FIG 4-3. This synthesis forms and thermolyzes silver amine complexes to produce silver nanoparticles, which are then sulfidized into silver sulfide nanoparticles.

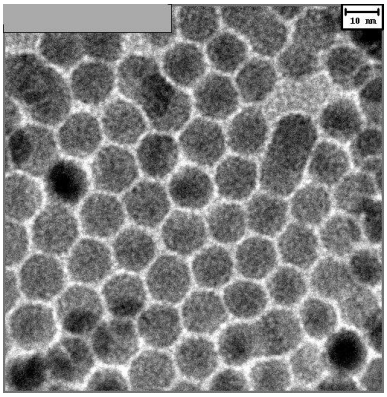


FIG 4-3: Ag2S Nanoparticles at 200KX

The required reagents were octadecylamine (ODA), silver nitrate ($AgNO_3$) and sulfur powder. Required solvents were toluene, ethanol, and chloroform. Suggested laboratory equipment were a heating mantle, 50 mL 3-neck round bottom flask, magnetic stir plate, stir

bar, neck clamp and ring stand. An NMR-tube inserted through a rubber septum served as a temperature finger to hold the thermocouple. The reaction is completed in ambient air.

8.6 g (~10mL) of ODA is heated to 185C over 10 minutes and dwelled at 185C for 10 minutes to stabilize temperature. After the solid ODA melts at 55C into a clear solution, the stir plate is turned on. A heat gun is used to melt ODA adhering to the sides of the flask. 0.5 g of silver nitrate powder is added to the heated ODA and allowed to react for 10 minutes. The solution colour changes from clear to brown and then silvery blue almost immediately indicating the formation and thermolysis of the silver-amine complex. 0.07g Sulfur powder is added at 10 minutes, and allowed to sulfidize for an additional 10 minutes. The reaction mixture colour changes from silvery blue to black immediately. At the end of the 10 minute sulfidation, the flask is raised from the heating mantle and allowed to cool to room temperature. At 100C, 30 mL of toluene is added to the mixture to solvate the ODA to prevent solidification while cooling to room temperature.

The precipitation method is used to wash ODA and other reactant by-products, and extract the nanoparticle solution. There are three wash steps including the initial precipitation. TGA measurements on powders dried from solutions washed a different number of times are illustrated in FIG 4-4. After two washes, the mass loss saturates. An additional wash is used to reduce remaining impurities. More washes should ideally help, but may strip the ODA encapsulant from the nanoparticle.

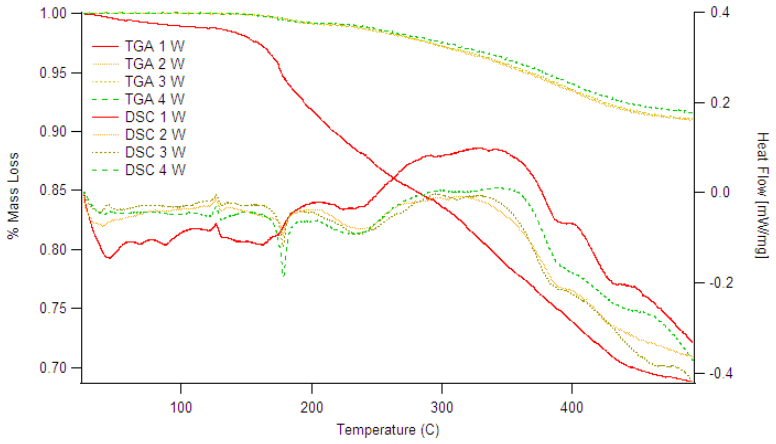


FIG 4-4: TGA and DSC heating curves of ODA-Ag_2S Nanoparticles washed various times before extraction

The solution is distributed evenly into four 50-ml centrifuge tubes. Ethanol is added to each tube with agitation until the particles begin to precipitate. This typically requires an ethanol volume equal to twice the nanoparticle solution volume. The solutions are centrifuged at 9000 RPM for 2 minutes to settle the precipitate. The supernatant is decanted, and the precipitate resolvated by sonication and vortex mixing in 0.5mL chloroform and 1.5 mL of toluene. 10 mL of Ethanol is added to each tube to re-precipitate the nanoparticles. The four tubes are combined into one tube to raise yield of nanoparticles. The solution is centrifuged and decanted. The precipitate is resolvated again in 0.5 mL chloroform and 1.5mL toluene and then precipitated by 10mL ethanol for the third wash. To extract the nanoparticles, the precipitate is

resolvated in 5 mL of toluene and centrifuged. The supernatant containing the nanoparticles is collected. The final mass loading ranges from 20-40 mg/mL.

4.1: Sintering Study: Materials Characterization

Experimental Description

Silver sulfide nanoparticle solutions in toluene were prepared according to the procedure described in the previous section. For TGA/DSC measurements, the solution was dried to a powder under nitrogen, and tested in an aluminum boat. Temperature was swept from 25C to 500C at 5C/minute in Argon. Blank measurements were conducted on both reference and sample boats prior to testing the nanoparticle powder to provide a background for subtraction from the DSC measurement.

Films were prepared by spincasting nanoparticle solutions. The starting substrates were 4" undoped test grade silicon wafers. An insulating oxide layer was grown by wet thermal oxidation at 900C to 1000A of thickness. 40 mg/mL of nanoparticle solution was dispensed through a 0.25 um PTFE filter and spuncast at 1000 RPM for 60 seconds onto the substrates. The nanoparticles could not be successfully redispersed after drying into powder. FIG 4-5 illustrates agglomeration caused by drying the nanoparticles. The sample in FIG 4-5A, prepared from a nanoparticle solution extracted after wash shows dispersed particles assembled into a close packed structure. The sample in FIG 4-5B, prepared by re-dispersing dried nanoparticle powder, shows 3D agglomeration of particles. To adjust concentration to 40 mg/mL, the solutions were partially dried under nitrogen and diluted, while maintaining the nanoparticles wet in solution at all times.

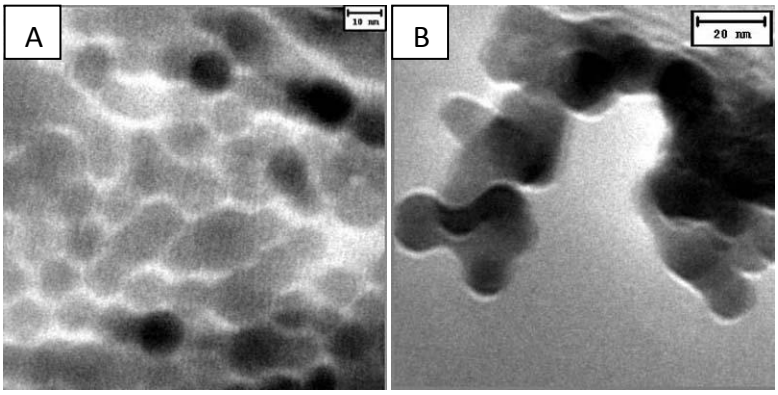


FIG 4-5: Nanoparticles A) Before Drying B) After Drying, significant agglomeration in dried sample

Based on the TGA/DSC data, several sinter temperatures were selected for further materials and electrical characterization. Nanoparticle thin films were sintered in a furnace under Argon for 1 hour at the following temperatures: 120C, 200C, 300C, 350C, 400C, 500C and 600C. The ramp rate for the furnace chamber was about 10C/minute.

Areal x-ray diffraction was measured on ex-situ and in-situ annealed samples on beamline 11-3 at Stanford synchrotron radiation lightsource in grazing and specular configuration to qualify the effect of sinter temperature on texture and grain size. In-situ heating was done in a

helium atmosphere in increments of 10C, dwelling at each temperature for about 20 minutes to collect diffraction data. The detector distance was 300 mm, and wavelength was 0.976Å. Ex-situ high-resolution x-ray diffraction was measured on beamline 2-1 in a symmetric geometry to quantify grain size within the films. The wavelength was 1.24Å. To extract grain size, the debye-scherrer equation was applied to the -112 peak, which was observed across all temperature measurements.

Results

4.1.1: TGA/DSC

TGA means Thermogravimetric Analysis, and DSC means Differential Scanning Calorimetry. These are powerful techniques for analyzing the transformation of materials. TGA measures the mass versus temperature of a material loaded in a sample pan. Measurements are done by sweeping temperature of the sample at a fixed rate and measuring the mass change. This indicates decompositions or phase transformations of materials by mass loss at various temperatures. Data is typically presented as percentage mass loss relative to initial mass, or absolute mass versus temperature.

DSC measures the heat flow of a material versus temperature. As a differential measurement, DSC compares the heat flow of a sample crucible loaded with a material and a reference crucible. Prior to the sample measurement, a blank measurement may be taken on the empty sample and reference crucibles. This establishes a baseline for the different heat flows for each crucible, which depend on heat capacity and therefore mass and purity of the crucibles. To improve accuracy of measurement data, this baseline may be subtracted from data of the sample measurement. Data is usually presented as heat flow normalized to mass in the units: mW/mg. Heat flow is positive into the sample, and negative out of the sample by convention.

The combined TGA and DSC data can distinguish between decomposition and phase transformations. For example, sharp endotherms upon heating, and exotherms upon cooling, without a corresponding change in mass, indicate a phase transition is occurring. Heat flows with weight loss suggest decomposition. This data can be very useful in evaluating the sintering process of nanoparticles.

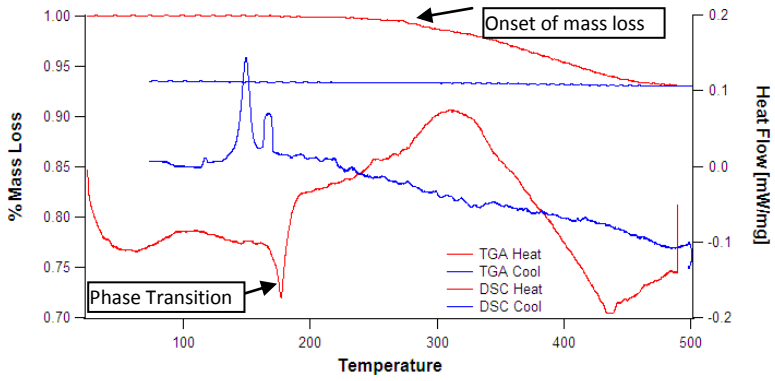


FIG 4-6: Typical TGA/DSC curve

FIG 4-6 illustrates a typical set of TGA/DSC curves for the ODA-Ag_2S nanoparticles. The key parameter from the TGA is the onset of mass loss around 280C. This corresponds to desorption of the stabilizing ligand from the film. From the DSC data, the phase transition of silver sulfide from acanthite to argentite is observed at 179C in the heating curve, affirming that the nanoparticle compound is Ag_2S. Upon cooling, there is some hysteresis observed in the phase transition. Reasons for this hysteresis are currently unknown but can be investigated in the future.

4.1.2: XRD

FIG 4-7 shows the high-resolution 1D diffraction patterns for ex-situ annealed samples. Particle coarsening begins between 120C and 200C. Granular silver appears around 500C and a predominantly silver film remains at 600C. Texturing of the film is observed between 120C and 200C and is attributed to the phase transition temperature. 2D areal diffraction measured on the same samples corroborates the 1D data. FIG 4-8 shows 2D data for samples sintered at 25C, 300C and 500C. The texturing is observed as change of isotropic intensity versus radial angle along the -111/012 peak and the 111 arcs. Silver nucleation, also observed in sulfidized films in the previous chapter, begins at 400C in the 2D data. The reduction in intensity of silver sulfide peaks at 600C suggests that the film is decomposing as the silver nucleation occurs. Although the silver sulfide should nominally decompose at 800C, the lower decomposition temperature observed at 600C may be facilitated by the reducing amines [115].

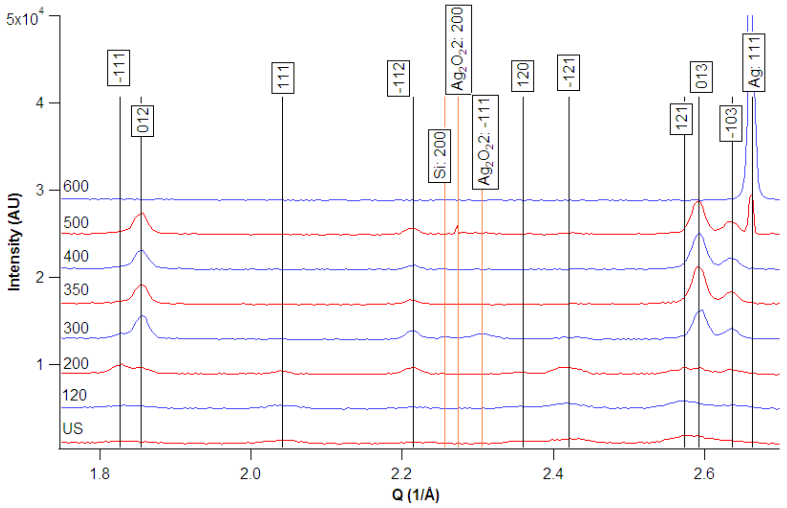


FIG 4-7: High-resolution XRD collected in specular geometry measured on sintered samples

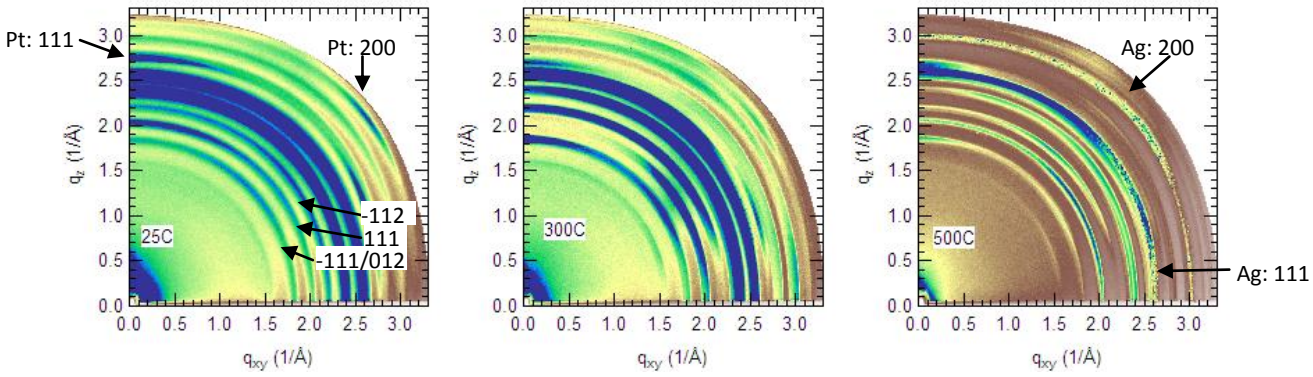


FIG 4-8: Areal Diffraction Patterns measured on ex-situ sintered-samples

Crystallite sizes extracted from the 1D data of the ex-situ heated samples, and 2D data of the in-situ heated sample are plotted in FIG 4-9. The onset of grain growth for in-situ heated samples occurs at ~85C, lower than 120C for ex-situ. Energy from the synchrotron beam is hypothesized to weaken the ligand-surface bond and lower the sinter temperature. The coarsening of the particles saturates shortly after the onset of growth.

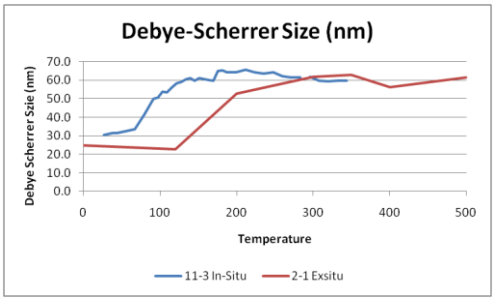


FIG 4-9: Debye Scherrer size extracted from in-situ areal and ex-situ 1D diffraction

4.1.3: AFM

AFM was used to measure the surface roughness and thickness, and qualify morphology of ex-situ sintered films. The thickness decreases from 50 nm to 34 nm during heating from room temperature to 400C, until increasing to58 nm and 323 nm at 500C and 600C. Roughness of the film does not change significantly until 600C. The AFM images in FIG 4-11 are measured across a 5 um x 5 um area and show the change in surface morphology with heating. Clear grain growth can be observed from FIG 4-11A to B, but large disconnected segments are observed after sintering at 600C.

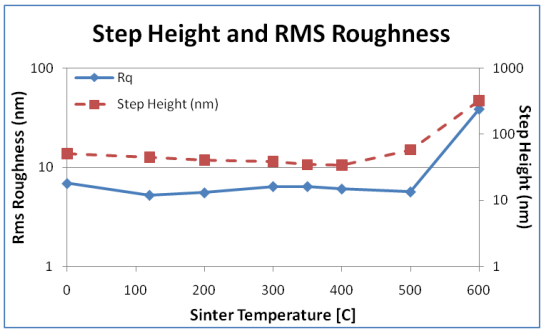


FIG 4-10: Step Height and Surface Roughness of Film

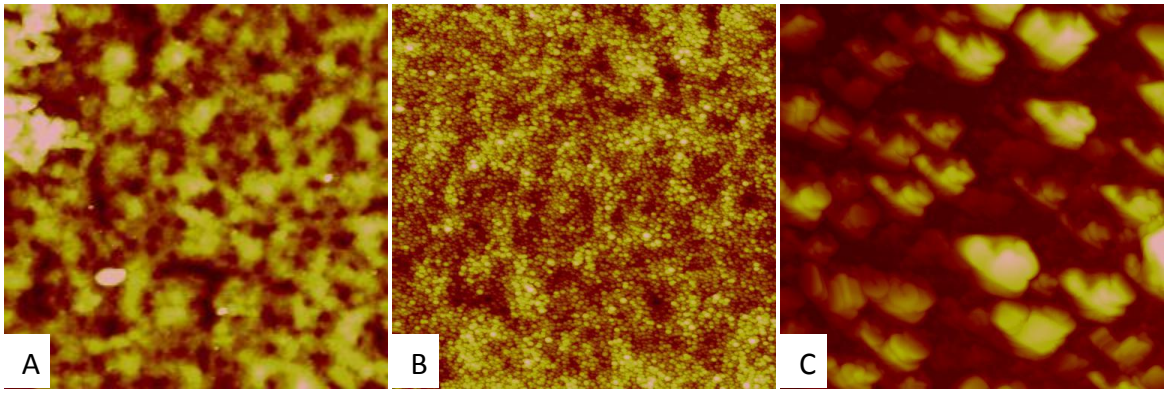


FIG 4-11: AFM of surface morphology: A) Unsintered, B) Sintered at 350C, C) Sintered at 600C

4.2: Sintering Study: Electrical Characterization

Experimental Description

There were two parts of the electrical characterization: 1) Electrical Impedance Spectroscopy (EIS) to separate ionic and electronic impedances, and 2) Potentiostatic measurements to examine filament formation. Lateral test structures were used to avoid pinholes that caused shorts in vertical structures. Additionally, the lateral tests allowed time resolved study of the filament growth across large gaps, which could be visualized optically.

To measure EIS, rectangular platinum contacts were sputtered onto the oxide substrates through a shadow mask. The tested pads' dimensions were 400um x 100um, and the separation gap was 40um. The EIS test conditions were 0V DC bias and 10mV AC Bias, sweeping from 1 MHz to 1 mHz. Data is only displayed up to 10 KHz because wire inductance effects became significant above that frequency. Samples were prepared by spincasting of nanoparticle solution and sintering as described in the materials characterization section. In this study, EIS measurements were only conducted at room temperature post sintering due to limitations of test equipment, and to avoid potential sintering disturb effects. The use of the solartron 1296A dielectric interface was critical in these measurements because sample impedance regularly exceeded Gigaohms. Without the interface, the Solartron 1260A frequency response analyzer (FRA) can only measure up to 100 Megaohm. Other tools such as the Gamry Potentiostats and HP4194A are also limited to a measure a maximum impedance of 100 Megaohms.

Samples used for filament studies were prepared as follows. Nanoparticle thin films were spuncast as described in the materials characterization section and sintered at 350C and 400C for 1 hour in an Argon environment. These temperatures were selected based on data from the EIS measurements. Silver was sputtered through a shadow mask onto the sintered nanoparticle films forming large circular electrodes that were 1000A thick. The silver served as the anode and cation source. A 25 um diameter tungsten probe tip was used as the cathode to enable rapid testing and induce high electric field for filament forming. The forming gap was set to 40 um. Forming tests were conducted at 4V and 10V. Ex-situ optical micrographs and current response curves during filament forming were measured under potentiostatic bias.

Results

4.2.1: Electrical Impedance Spectroscopy

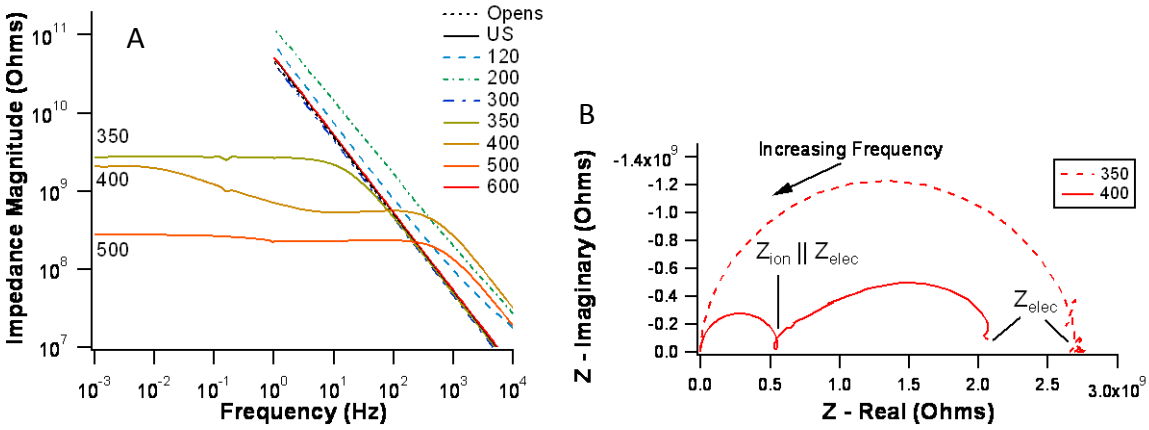


FIG 4-12: A) Magnitude Bode Plot of Impedance B) Nyquist plot of 350C and 400C Sintered films

FIG 4-12A illustrates the frequency dependence of the impedance magnitude obtained from EIS. Samples sintered at 300C and below, and at 600C show purely capacitive behavior. Between 350C and 500C, finite conduction is observed. The Nyquist plots for the 350C and 400C sintered samples are illustrated in FIG 4-12B. At 350C, only one time constant is observed, whereas two are observed at 400C. In the absence of grain boundary effects and using blocking electrodes for one of the two carriers, two time constants are expected in the mixed conduction regime [73]. A high frequency time constant corresponds to the bulk dielectric capacitance of the material, and a lower frequency time constant corresponds to a chemical capacitance from polarization of the blocked carrier. The chemical capacitance is stored energy in a chemical potential gradient, similar to electric capacitance as stored energy in a charge gradient. Pt is used to block silver cations, and the electronic conduction is measured at the low frequency limit (labeled Zelec in FIG 4-12B). The intermediate frequency intercept corresponds to the parallel conduction of the ions and electrons. The reason for the single nyquist loop at 350C will be discussed later.

4.2.2: Filament Formation Tests

Given the information on the ionic and electronic conductivities from the EIS data, filament formation was tested in lateral structures on films sintered at 350C and 400C. These temperatures were selected because they correspond to the first onset of electronic conductivity, and mixed conductivity. The number of testable samples was limited by functional yield of nanoparticles. Certain test batches showed catastrophic dewetting upon sintering. The root cause of this variability was not determined.

Filament formation was not observed at all in the 350C sintered film up to 10V testing, but was observed in the 400C sintered film. Ex-situ optical micrographs and current response curves of filaments grown at 4V and 10V are illustrated in FIG 4-13. At 4V a filament bridges the electrode in 85 seconds, while at 10V a filament bridges the electrodes in 7 seconds. The shorter formation time at higher voltage is consistent with the exponential dependence of electrochemical reaction rates on voltage. As the filament forms in both cases, the silver anode is consumed as shown by the receding white silver electrode. In electrical measurements, initial current is low until sharply increasing upon bridging of contacts. This indicates that despite low current, silver ions are still being transported and reduced to form the filament.

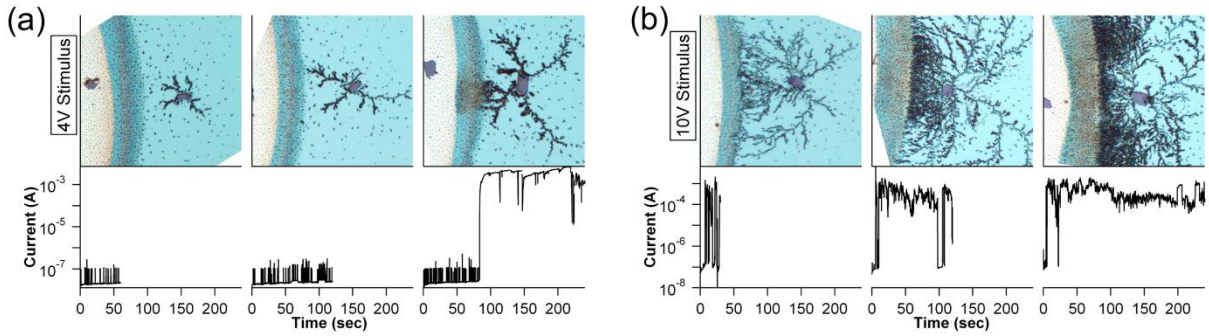


FIG 4-13: Filament Formation at 4V for Various Times (a) 10V for Various Times (b)

In the 10V case, as the bias is held constant past the bridging of the two electrodes, new dendrites continue to form in addition to ripening of existing dendrites. This indicates that the current is not completely shunted through the metallic dendrite. Consequently, in RRAM memory cells, the initial filament formation should be controlled to reduce overgrowth, which could affect cycling reliability.

4.3: Discussion

The materials and electrical data show that there is a window of sintering temperatures between 400C and 500C that is optimal for mixed conduction in ODA-Ag_2S nanoparticle films. FIG 4-14 concisely illustrates this by comparing the extracted impedances from EIS, the debye-scherrer grain size from XRD, and the mass loss curve from TGA. Four Regions are identified. In Region A, from about 120C to 200C, there is significant coarsening of the nanoparticles, but without any measurable change in the film impedance. In Region B, between 200C and 350C, ligand starts to evolve from the film. At 350C, there is onset of electronic conduction through Region C, followed by mixed conduction from 400C to 500C in Region D. Across this temperature range, the electronic impedance is reduced at a faster rate relative to the ionic

impedance. At 600C, the measured impedance is purely capacitative, and a predominantly silver film remains, as illustrated by 1D XRD in FIG 4-7.

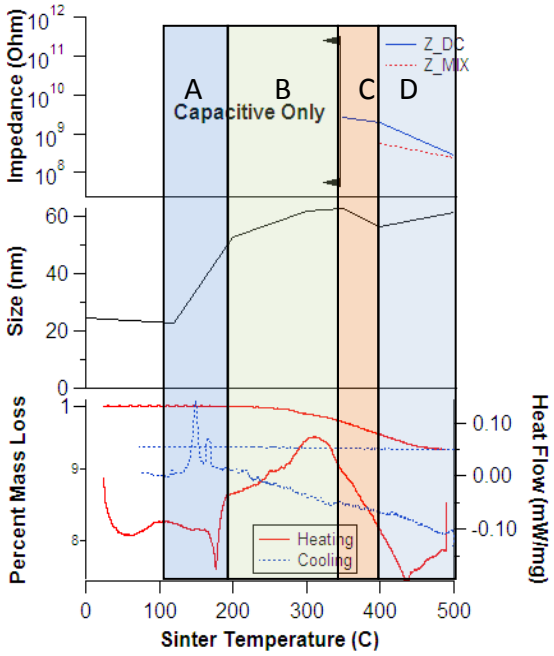


FIG 4-14: Impedance Data Separated in Mixed Conduction and Electronic Conduction (Top) Crystallite Size as calculated from Debye-Scherrer Equation (Middle) TGA/DSC Data (Bottom)

The sintering mechanism of nanoparticles has been studied by Volkman using thiol encapsulated silver nanoparticles as a test vehicle [106]. Three distinct transformations are identified. These are 1) dissociation of surfactant from the nanoparticle surface, 2) growth of crystallites through coalescence and 3) formation of an electrically conductive polycrystalline film through densification. The dissociation of thiol surfactant was identified by an endotherm in the DSC data. In ODA-Ag_2S nanoparticles, no abrupt endotherm is observed. Amines bind silver more weakly than thiols. This is corroborated by an alkyl-length dependence of sinter temperature in amine encapsulated silver nanoparticles, but independence in thiol encapsulated silver nanoparticles [11][116]. The strong thiol-silver interaction limits ligand removal, not the boiling point of ligand. The weaker binding of ODA may explain why no endotherm is observed, as there is no strong interaction between the ligand and nanoparticle surface that must be broken with thermal energy. This weak binding also suggests that using a lower boiling point ligand with a shorter alkyl chain length can reduce the onset temperature of conduction. The growth of crystallites in occurs mostly in Region A where encapsulant still remains in the film. In Region B, densification begins as ligand is evolved from the film.

In Region C, the onset of electronic conduction without ionic conduction may be rationalized by a combination of interfacial effects and connectivity between grains. Interfacial effects reviewed in Chapter 2, modify the surface carrier concentration. This is similar to the enhancement or depletion of electronic carriers at a metal semiconductor junction. It is the

mechanism of heterogeneous doping of ionic compounds, where conductivity enhancement occurs in fine grain composites of two distinct phases of different compounds.

The encapsulant of the Ag_2S nanoparticles is octadecylamine ($C_{18}H_{37}NH_2$), which shares the nucleophilic properties of ammonia (NH_3). This would be expected to generate an electron enhanced surface region as described in FIG 2-5 in Chapter 2. The penetration depth of the space charge layer is expected to be, twice the debye length of the material. Using Equation 4-2, the debye length of Ag2S is estimated to be 36nm. The value used for the relative permittivity ϵ_r was 8 [117]. The maximum stoichiometry range δ of Ag_2S, 4.89E15 cm^{-3} was used [47]. From the plot of extracted grain sizes in FIG 4-9, final scherrer debye size is 60nm. The penetration depth of the space charge is 2 λ_d from a surface. Because the grain size is smaller than 4 λ_d, the bulk of the grain is expected to exhibit enhanced electron carrier concentration and depressed silver interstitial carrier concentration while the amine encapsulants are still bound to the surface.

$$\lambda_d = \sqrt{\frac{\epsilon_r \epsilon_o k_b T}{q^2 (\sum_i \ z_i{}^2 \, c_i)}}$$

Equation 4-2: Debye Length. q: elementary charge, ϵ_r: relative dielectric constant, ϵ_o: permittivity of free space, k_b: boltzmann's constant, T: temperature (K), z_i: charge number, c_i: carrier concentration

However, while the amines are still bound, the particles are dispersed and maintained as separate domains. As ligand is removed, the particles can come into contact and can begin conducting through contacted surfaces. The transition from a pure electronic conducting film with high impedance, to a mixed conducting film of lower impedance suggests that there is a trade-off of grain surface area between carrier enrichment and physical with adjacent grains. When the maximum number of amines is bound to a grain occupying the entire surface area, electronic enhancement is greatest, but there is no net conduction through the film because all grains are separated. As the amine encapsulant is removed, the enhancement decreases, but contact between grains is increased increasing conductivity.

Within Region D, XRD data in FIG 4-7 and FIG 4-8 show that silver nucleation in the film begins. Assuming that the initially synthesized nanoparticles are stoichiometric, the film is decomposing, and effective silver content is increasing. This may decrease the electronic impedance by one of two mechanisms. In one case, percolation paths through the phase segregated silver may form, facilitating a parasitic easy path of conduction. Alternatively, the increased silver content could be electrically doping the film. The framework of point defect chemistry presented in chapter 2 can help explain this doping effect.

The total conductivity of Ag_2S is known to vary by as much as two orders of magnitude depending on stoichiometry [47]. As a mixed ionic-electronic conductor, there are two defect generation processes in Ag_2S, described in Equation 4-3a,b. Electron-hole pairs, and silver frenkel defect pairs are thermally generated. The specific carrier concentrations will depend on the defect formation energies and stoichiometry.

a) $e_{VB}^{x} + h_{CB}^{x} \leftrightarrow h_{VB} + e'_{CB}$	b) $Ag_{Ag}^{x} + V_{i}^{x} \leftrightarrow Ag_{i} + V'_{Ag}$

Equation 4-3: Reaction Equations: a) electron-hole generation b) Ag interstitial-lattice vacancy generation

According to the phase diagram in chapter 3, $Ag_{2+\delta}S$ has a very narrow phase width δ in the low temperature acanthite phase [71]. The phase width is defined as the stoichiometric domain of a compound over which phase segregation does not occur. Measurements by Wagner indicate this stoichiometric variability is on the order of 2.7E-7 mol, or 4.89E15 cm^{-3}.

$$\boldsymbol{Ag^{x} \leftrightarrow Ag_{i} + e'_{cb}}$$

Equation 4-4: Silver Ionization Reaction

Excess silver is known to dope Ag_2S n-type by forming silver cations and electrons according to Equation 4-4. Assuming full ionization of this excess silver δ, the total carrier concentrations of interstitial silver cations and conduction band electrons will only change if δ is greater than the respective intrinsic carrier concentrations. Reports in the literature indicate that the intrinsic silver cation concentration is higher than electronic concentration [71][48]. This is supported through high temperature impedance measurements (~160C) that showed that electronic conductivity was sensitive to silver activity, while ionic conductivity was not [76].

The published values of intrinsic carrier concentration in the literature are all measured at high temperature: ~100-200C. These studies took measurements at elevated temperatures to reduce impedance of films to measurable range of test equipment, because the AgI contacts in test structures must be operated in the super-ionic phase (>150C). Using published values of intrinsic carrier concentration and formation energies at these elevated temperatures, the intrinsic carrier concentrations at room temperature can be estimated. The frenkel defect formation energy and intrinsic carrier concentration used were 138 kJ/mol and 5e-4 mol/mol Ag_2S at 450K [71][48]. These were correspond to 1.43eV and 8.78E18 cm^{-3}. The electronic carrier concentration used was 3e-7 mol/mol Ag_2S at 168C, corresponding to 5.25e15 cm^{-3}[71]. The electronic formation energy used was a bandgap of 0.9eV [67]. The extrapolated carrier concentrations at room temperature would be 2.02E13 cm^{-3} for electrons, and 8.55e14 cm^{-3} for Ag interstitial cations. The electronic concentration is 2 orders of magnitude below δ, while the ionic carrier concentration is on the order of δ. Assuming that mobility remains fairly constant, electronic conductivity is expected to change more than the ionic conductivity versus δ at room temperature, as shown in FIG 4-14.

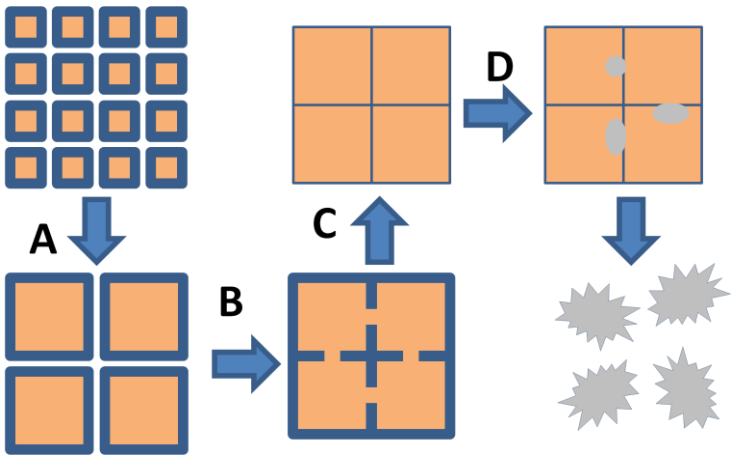


FIG 4-15: Schematic of Sintering Process of the Nanoparticles

The sintering process of the ODA-Ag_2S Nanoparticles is summarized in FIG 4-15. In Region A, discrete nanoparticles coalesce into larger ones. The ODA ligand is still bound to the surface, maintaining separate domains of Ag_2S. EIS data confirms this by showing that the films are purely capacitive similar to unsintered films. In Region B, upon further heating to the boiling point of ODA at 350C, the ligand begins to evolve from the film while grain growth has saturated. As ligand is removed, the film thickness decreases suggesting densification. As densification and ligand removal continue, percolation paths begin to form that facilitate electronic conduction. In Region C, the ligand removal continues, reducing the electronic carrier enhancement and facilitating larger contact between grains. Onset of mass transport is observed. In Region D, upon further heating and ligand evolution, silver nucleation in the film begins, as shown in the 2D XRD data in FIG 4-7 and FIG 4-8. Electronic conduction also increases. Further heating beyond 500C to 600C causes further decomposition until a porous and disconnected silver film remains, as shown in the 1D data in FIG 4-7 and AFM of the film surface in FIG 4-11C. The filament formation studies corrobate the sintered nanoparticle data. Films tested at 350C did not show any clear filament formation, indicating that there was little mass transport through the film. At 400C, when there was both ionic and electronic transport observed in the impedance data, filament formation was observed. Further detailed discussion of filament formation will be reserved until chapter 6.

4.4: Conclusions

The effect of sintering temperature on mixed ionic-electronic conductivity of ODA encapsulated Ag_2S nanoparticle films has been studied. A process window has been identified in which ligand binding to the surface limits the lower sinter temperature, but thermal decomposition of Ag_2S limits the upper sinter temperature. Sintering of the particles follows a mechanism similar to the one proposed by Volkman for silver nanoparticles [118]. In order to further reduce the sintering temperature of silver sulfide nanoparticles, a lower boiling point ligand should be used.

Chapter 5: Sintered Thioglycerol Encapsulated Ag_2S Nanoparticle Films

In the previous chapter, effects of sintering conditions on mixed ionic electronic conductivity of octadecylamine encapsulated silver sulfide nanoparticles (ODA-Ag_2S NP) were explored. Upon heating, the film transitioned through insulating, pure electronic conducting, then mixed ionic electronic conducting states, before decomposing at high temperature. Removal of ligand from the film was required before onset of conductivity. The high boiling point of octadecylamine limited this onset to 350C, much higher than the plastic compatible temperatures for printing applications. Additionally, yield issues with the organic synthesis limited the quantity of functional nanoparticles that could be produced for testing. In this chapter, an aqueous method is used to synthesize water-soluble thioglycerol encapsulated silver sulfide (THG-Ag_2S) nanoparticles as the starting material for forming thin films. The lower boiling point of THG (120C) compared to ODA (350C), reduced the onset temperature of mixed conduction. The aqueous synthesis was easily scaled up to increase yield [119]. Issues associated with using the aqueous synthesis are discussed and compared with the organic synthesis. Effect of sintering conditions on the structure THG-Ag_2S nanoparticle thin films are explored by XRD, TGA, and AFM, and correlated to mixed ionic-electronic conducting properties, determined by electrical impedance spectroscopy.

5.1: Nanoparticle Synthesis

The basic concepts of colloidal nanoparticle synthesis have been reviewed in chapter 4. The two generic classes of methods are high temperature organic synthesis and low temperature aqueous synthesis. The organic methods use thermolysis of organic precursors to cause a sudden burst of nucleation that facilitates formation of monodisperse nanoparticles. These methods are difficult to scale up to large batches due to the high temperatures required (>150C). Low temperature aqueous methods use chemical reactions to precipitate materials in the presence of surfactants. The term aqueous is interpreted broadly in this context to include reactions that use polar protic solvents such as alcohols, not just water. Metals are usually formed by reduction of metal salts. Metal oxides are formed by hydrolysis and condensation reactions. Semiconductors such as metal chalcogenides are formed by co-precipitation of metal salts with chalcogen compounds such as thiourea or Na_2S.

Aqueous processing of silver compounds has been historically studied in the context of film photography. Composites of micron-sized AgCl, AgBr, and β-AgI grains dispersed in gelatin are the fundamental photosensitive component of black and white film [21]. AgF was not used because its water solubility was too high, precluding precipitation. The silver halide composites were formed by the co-precipitation of silver and halide salts in gelatin.

Aqueous synthesis methods tend to result in broad nanoparticle size distributions because the nucleation occurs over a wide range of time, resulting in crystallites with different growth histories. The LaMer plot presented in chapter 4 provides the conceptual framework for understanding effect. A long nucleation time corresponds to a long Region II. Particles formed later have less growth time and will be smaller. Size selective precipitation can reduce polydispersity of nanoparticle solutions [107][120]. This exploits the condition that larger

particles are more easily flocculated from solution than smaller particles by addition of a non-solvent. The flocculate can be collected by centrifugation. Successive iterations of this process result in several nanoparticle extractions of narrowed size distribution, with mean particle size decreasing per iteration. The mean size of the nanoparticles can also be controlled through the synthesis. For example, in the reverse-micellar method, increasing water content increases reverse micelle size and the mean radius of synthesized Cu and CdS nanoparticles [121].

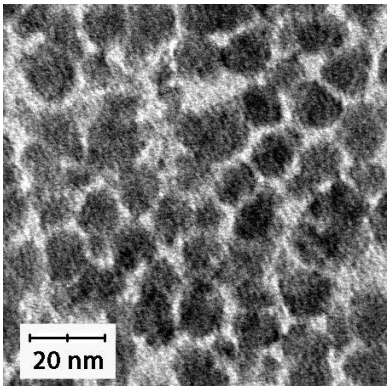


FIG 5-1: Thioglycerol Encapsulated Nanoparticles ~8nm

Polydisperse THG-Ag_2S nanoparticles of ~8nm diameter were synthesized according to the method by Jang [119]. A representative TEM illustrates the particle size and distribution in FIG 5-1. The synthesis was a controlled co-precipitation of silver nitrate ($AgNO_3$) and sodium sulfide (Na_2S) in presence of THG encapsulant.

	$AgNO_3$		***Thioglycerol***		***NaOH***		***Na_2S***
Solvent	**H_20**		**H_20**		**H_20**		**H_20**
Solvent Volume (mL)	50		50		10		50
Reactant Mass (g)	0.45		1.25		0.4		0.1
Reactant Volume (mL)	N/A		1				N/A
Reactant Density (g/mL)	N/A		1.25		2.13		N/A
Reactant MW (g/mol)	169.87		108.16		40		78.0452
Reactant mmol	2.65		11.56		10.00		1.28
Molarity mM	52.98		0.23		1000.00		25.63
Initial pH	4.9		1.7		11		

Table 5-1: Aqueous Nanoparticle Synthesis Reagents

The required reagents were $AgNO_3$, Na_2S, NaOH, and DI-water. The ratio of starting materials and solutions is listed in Table 5-1. The silver and sulfur were reacted in a stoichiometric ratio, and encapsulant was added in strong excess. First, all four solutions were prepared separately. The starting pH of the THG solution is 1.7, and was raised to 11 by addition of the NaOH solution. This drove the deprotonation of the thiol forming thiolate ions that would complex with silver cations. The $AgNO_3$ solution was added to the THG solution under vigorous stirring. The solution looked cloudy upon initial mixing, and turned clear with stirring as the Ag-thiolate complex was formed and dissolved. Without raising the pH, the

$AgNO_3$/THG solution remained cloudy until a yellowish-white precipitate settled from solution. Final appearance of the $AgNO_3$/THG solution was transparent pale yellow. The Na_2S solution was added to the $AgNO_3$/THG solution, resulting in a specular black solution. This was mixed for an additional 1 hour.

The precipitation method was used to extract and wash the nanoparticles from solution. 2 wash steps are used including the initial precipitation. Further washes were not done, because the solubility of the nanoparticles was so high in water that they could not be precipitated and recovered. 20mL of the reacted solution was poured into a 50 mL centrifuge tube and mixed with 20 mL of isopropanol (IPA) to induce precipitation. The tubes were centrifuged at 4000RPM for 10 minutes. Supernatant was decanted and discarded. Remaining precipitate was dispersed with 5 mL of acetone for washing, and centrifuged and decanted. 2 mL of DI-water was used to disperse the precipitate with sonication and vortex mixing. 4 sets of the re-dispersed 2 mL solution were combined into a single tube to raise recovered yield, and precipitated with 20 mL of IPA. The remaining precipitate was dispersed with 5 mL of acetone and centrifuged and decanted. The final precipitate was dried under vacuum into a powder. Unlike the ODA particles, the aqueous nanoparticles could still be successfully re-dissolved from a powder. The stronger bond of the thiol to Ag, relative to the amine is the likely cause of this improved stability.

Residual NaOH from the aqueous synthesis was detected in some batches by measuring pH of final solutions. These solutions could be further washed with DI-water through a cellulose membrane. Centrifugal filter units rated for 10,000 Nominal Molecular Weight Limit (NMWL) manufactured by Millipore were used. A NMWL with a smaller value would retain smaller particle sizes. The centrifugal filter unit consists of a filter cartridge mounted in a centrifuge tube. A small volume of the nanoparticle solution is placed inside the filter unit, and rinsed with DI-H2O under centrifuge until the pH of the filtrate solution is about 7.

5.2: Sintering Study: Materials Characterization

Experimental:

THG-Ag_2S NP were synthesized and prepared according to the method described in the previous section 5.1:. TGA/DSC test conditions were the same as those for ODA-Ag_2S NP. The sample powder was heated from 25C to 500C at 5 C/minute in Argon in an aluminum test boat. Blank measurements were conducted on the reference and sample boat prior to the test measurement to obtain a background for DSC subtraction.

Based on the TGA/DSC data, a sinter temperature range for thin film samples was selected for further characterization. Starting substrates were 4” undoped test grade silicon wafers, on which a wet thermal oxide layer was grown. For XRD measurements, a 1000A oxide was used, and for EIS testing, a 1 um oxide layer was used. Films were prepared by spincasting a solution [50 mg/mL] filtered through a 0.2 um PVDF filter at 1000 RPM for 60 seconds onto the substrates. To improve wetting of the aqueous solution, substrates were first treated with UV ozone for 10 minutes immediately prior to spinning. Samples were cleaved into 1 cm^2 pieces and sintered in nitrogen for 1 hour at 50C, 100C, 150C, 200C, 250C, 300C and 350C. The

samples were heated instantaneously by direct placement onto a hot plate at the sinter temperature, and quickly cooled by placement onto a cool silicon wafer.

AFM was measured across a 5 um x 5um sample area to evaluate surface morphology and roughness of the film. Extracted metrics were the thickness, rms roughness and peak to peak height range.

Areal 2D and high resolution 1D X-ray diffraction was measured on beamline 11-3 and 2-1 respectively at Stanford Synchrotron Radiation Light Source. The areal data qualified texture and silver impurities, and the 1D data quantified grain size. Areal data was collected at a detector distance of 300 mm, and a wavelength of 0.976 Å. Two sets of 1D data were measured. Full scans were measured in an asymmetric geometry to reduce background peaks from the substrate, with a wavelength of 1.24 Å. The step size was 0.0339^{o} in theta, and 0.003 Å^{-1} in q. To quantify grain size, high resolution measurements of the -112 peak were conducted in symmetric mode. The step size was 0.002 Å^{-1} in q. The debye-scherrer equation was applied to the -112 peak to calculate grain size, because it was measurable in all samples.

Results:

5.2.1: TGA/DSC

The TGA/DSC curve for the THG-Ag2S NP is shown in FIG 5-2. The TGA curve shows two mass loss temperatures. The first one at 100C corresponds to loss of water moisture from the powder, retained in the hygroscopic THG encapsulant. The second mass loss at 190C is the evolution of the THG ligand from the film. This temperature is significantly lower than 350C for ODA, but higher than the 120C boiling point of THG. The smaller molecular weight of THG results in the lower ligand evolution temperature compared to ODA. The higher ligand removal temperature, relative to the THG boiling point results from the thiolate-silver bond that must first be broken.

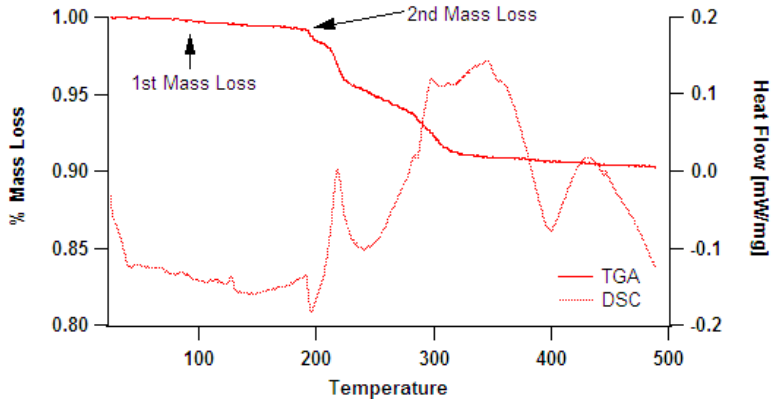


FIG 5-2: TGA/DSC curve for THG-Ag_2S Nanoparticles

5.2.2: XRD

The high-resolution 1D diffraction data in FIG 5-3 shows that significant crystallization occurs between 100C-150C and that silver exists in sintered films. The peaks have been assigned to the acanthite phase of Ag_2S, fcc Ag, and a substrate peak from the oxide. The

debye-scherrer size of the -112 peak, in FIG 5-4, shows an optimum at 250C. Reasons for this will be discussed later.

The strong 111 silver peak starting from 150C shows that silver crystallites grow within the film during sintering. In 2D areal diffraction shown in FIG 5-5, granular spots along the 111 and 200 arcs indicate that silver crystallites exist within the film even before sintering. This contrasts with the ODA-Ag_2S films, in which silver crystallized as the film decomposed after sintering around 500C. The presence of silver in the initial nanoparticle film suggests that the aqueous synthesis method is the source of contamination. Mechanisms of this contamination will be considered in the discussion section.

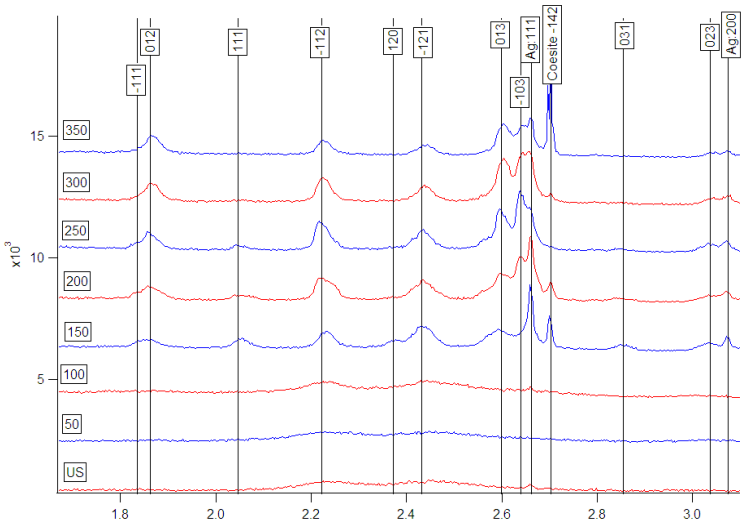


FIG 5-3: 1D High-resolution XRD in asymmetric geometry

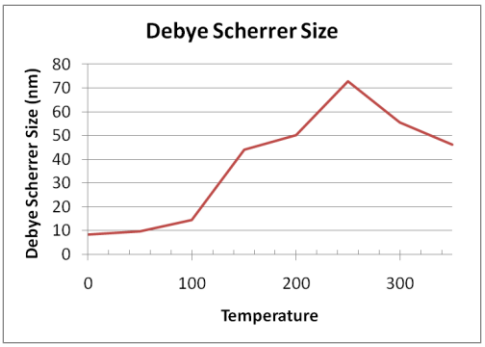


FIG 5-4: Debye Scherrer Crystallite Size. On set of crystallization occurs at 100C. Optimal grain size is observed around 250C.

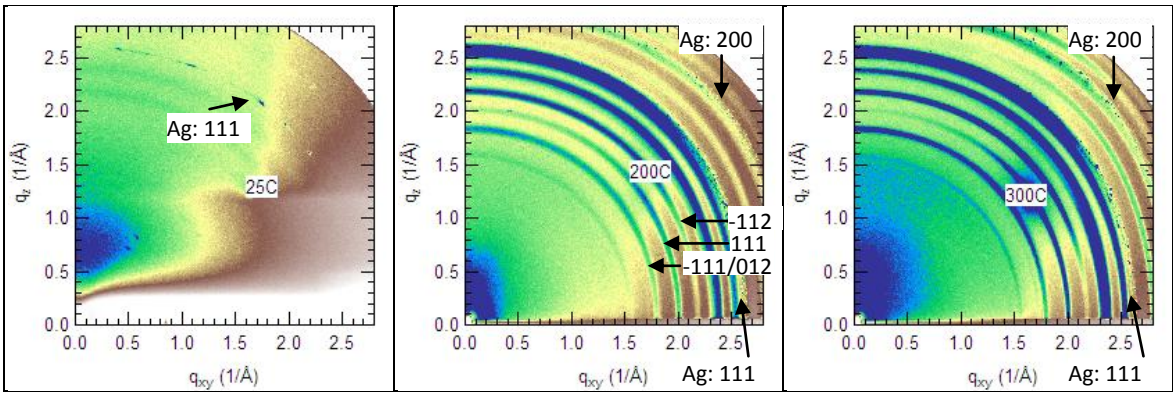


FIG 5-5: Areal Diffraction Data for sintered particles. Silver crystallites exist in pre-sintered films. Granular silver begins to grow around 200C, increasing in intensity at 300C.

5.2.3: AFM

The surface morphology of films is shown in FIG 5-6 before sintering, and after sintering at 150C and 300C. Coarsening of the Ag_2S NPs can be observed in the underlying film in the 150C image. At 300C, there are significant voids observed as large dark spots. These voids are not as prominent at lower sinter temperatures. FIG 5-7 plots the thickness, rms roughness, and peak-valley range of the film, versus sinter temperature. As sinter temperature increases, the thin film compacts as water and then THG ligand evolves, as indicated by the decrease in thickness. Surface roughness increases as the Ag_2S and Ag grains grow and voids form.

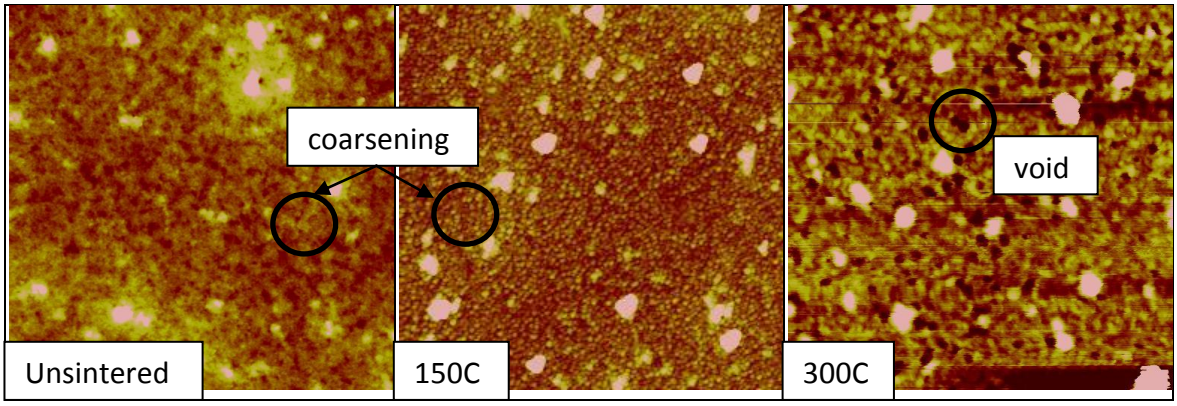


FIG 5-6: AFM Image illustrating surface topology

Across all temperatures, there are large nodules observed on the surface. These are hypothesized to be silver crystallites that have grown on the surface during the sintering, as observed in XRD.

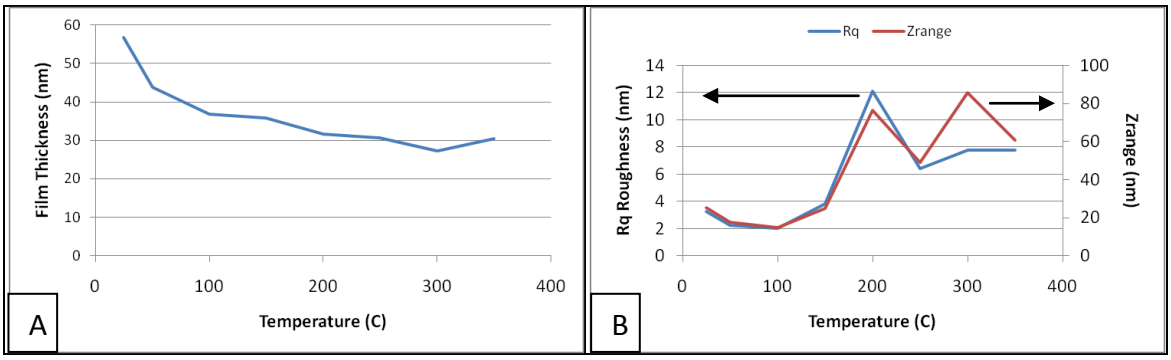


FIG 5-7: (A) Film thickness vs sintering temperature (B) Roughness and Z-Range vs Sintering Temperature

5.3: Sintering Study: Electrical Impedance Spectroscopy

Impedance spectroscopy is used to quantify the mixed ionic-electronic conductivity of the films. Two sets of contact metals were used for EIS testing. 18Å/400 Å of Ti/Pt and 18 Å/390 Å of Cr/Au were evaporated on separate 1 um thick oxide on silicon before spin-casting of the nanoparticles. The Ti/Pt layers were e-beam evaporated and the Cr/Au layers were thermally evaporated. Frequency was swept from 1MHz to 10 mHz to measure the DC electrical impedance. Lower frequencies were not tested due to time constraints (a 1 mHz cycle would require 1000s or 30 minutes).

At low frequency, the Cr/Au contact pads showed an open circuit condition extending into the complex plane, while the Ti/Pt pads showed a closed-circuit condition terminating on the real axis. Selected spectra are shown in FIG 5-8A,B. The measured impedance for the gold pads was an order of magnitude higher at low frequency, as shown in the bode plot: FIG 5-8C.

This discrepancy may arise from gold diffusion through silver sulfide, which has been observed in Ag_2S/Au/Pt core-shell nanoparticles [122]. A charge transfer mechanism of diffusion was proposed based on the Au work function (-5.1 eV), and Ag_2S valence band edge (-5.32 eV). This Au diffusion may have modified the contacts resulting in the higher measured impedance. The high work function (-5.65eV) of Pt would prevent this charge transfer and diffusion through Ag_2S. Pt is known as an inert metal due to its high work function and is the standard electrode metal for electrochemistry. For these reasons, the Ti/Pt EIS data is selected for further analysis.

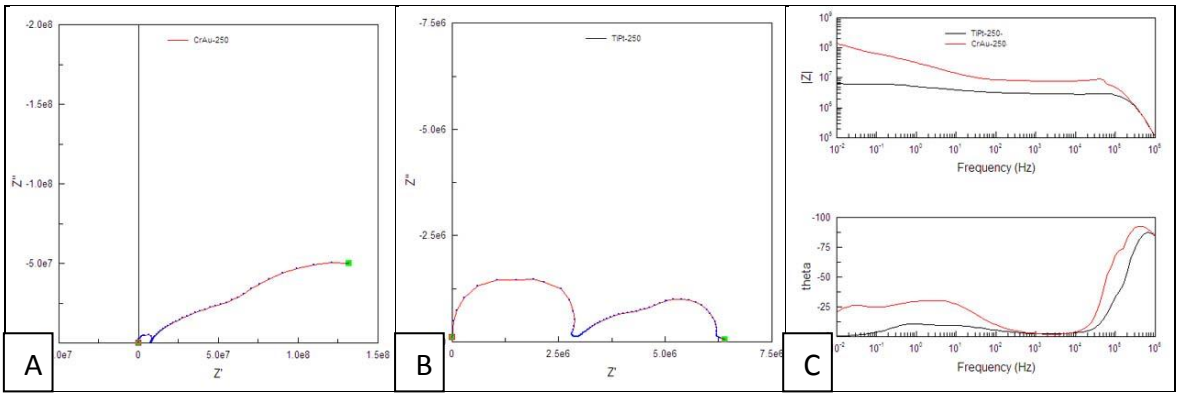


FIG 5-8: (A) Nyquist Plot for Cr/Au Contact (B) Nyquist Plot for Ti/Pt Contact (C) Bode Plot

FIG 5-9A illustrates the reduced EIS data for the Ti/Pt contacts after extraction of the ionic and electronic conductivity, as described in the previous chapter on ODA-Ag_2S NPs. Impedance of the mixed conduction point increases between 0C-100C. In the TGA data (FIG 5-2) there is slight mass loss observed at this range attributed to water loss. Ionic impurities in water may be the source of this conduction. As moisture is removed from the film, the ionic impurities become immobile. At 150C, there is an onset of crystallization along with mixed conductivity. All impedances are minimal at 250C sintering.

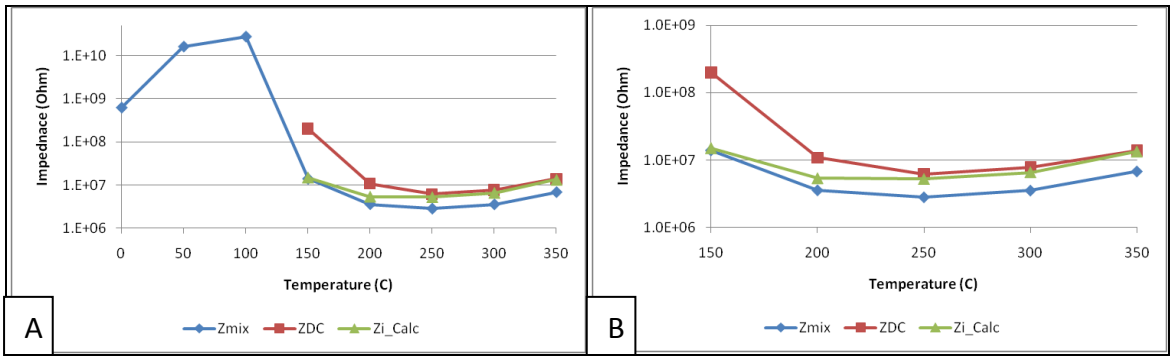


FIG 5-9: Ti/Pt Contact (A) Ionic, Electronic Conductivity versus sinter temperature (B) Close of 150C-350C

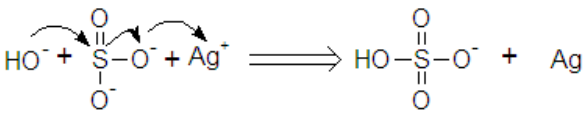
5.4: Discussion

The THG-Ag_2S and ODA-Ag_2S nanoparticles and sintered thin films showed differences in materials and electrical properties. These arise from differences in the synthesis and sintering conditions. The THG-Ag_2S nanoparticles are more polydisperse than the ODA-Ag2S nanoparticles. This is an inherent result of using the low-temperature co-precipitation in which the nucleation step spans a longer duration. Nuclei form at different times, with later nuclei growing for shorter times to a smaller size than earlier nuclei.

Crystalline silver was also observed in the initial THG-Ag_2S nanoparticles as indicated by the areal XRD data in FIG 5-5. Motte and Urban have observed similar contamination in aqueous synthesis of Ag_2S nanoparticles [123]. In their reverse micellar method, sodium bis(2-ethyl-hexyl) sulfosuccinate (NaAOT) was used as micelle surfactant, dodecanethiol (DDT) was used as encapsulant, and $AgNO_3$ and Na_2S were used as silver and sulfur sources. The proposed mechanism was the reduction of silver cations in solution by the sulfite (SO_3^-) group of the AOT surfactant, catalyzed by the Ag_2S nanoparticles [124]. Although the aqueous synthesis employed in this chapter did not use NaAOT, the reaction of Na_2S and H_2O could have produced the sulfite (Na_2SO_3) in situ according to the net reaction in Equation 5-1.

$$Na_2S + 2(H_2O) \rightarrow H_2S + 2(NaOH)$$
$$2(H_2S) + 3O_2 \rightarrow 2(SO_2) + 2(H_20)$$
$$SO_2 + 2NaOH \rightarrow Na_2SO_3 + H_2O$$
Net Reaction:
$$Na_2S + 3/2(O_2) \rightarrow Na_2SO_3$$

Equation 5-1: Net Reaction of Sodium Sulfite Production



Equation 5-2: Reaction of Na_2S and H_2O to produce Na_2SO_3

The sodium sulfite could then reduce silver cations by the mechanism illustrated in Equation 5-2. This is catalyzed by Ag_2S, which provides a surface for the adsorption and reduction of silver cations, and subsequent nucleation of elemental silver. This process is similar to the chemical development of silver halides done in photographic processes. In those cases, electron transfer of reducing agents is catalyzed by latent formation of elemental silver clusters [125].

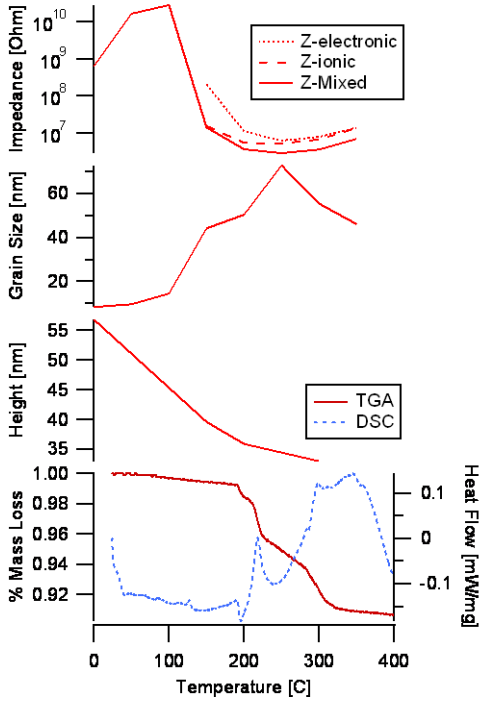


FIG 5-10: Combined Plot of Mixed Conductivities, Grain Size, Film Thickness and Mass Loss

There are several trends in the sinter process that are illustrated when combining data from the various materials characterization and EIS, illustrated in FIG 5-10.

XRD data shows a peak grain size versus sintering temperature for THG-Ag_2S NP films, but shows a saturated grain size versus sintering temperature for ODA-Ag_2S films. The sintering method of the films causes this difference. The ODA-Ag_2S films were heated at a finite ramp rate of 10C/minute from room temperature to the sinter temperature in a furnace, while the THG-Ag_2S films were instantaneously heated by placement onto a hot plate at the sinter temperature.

Volkman observed a similar trend of peak grain size in the study of sintered silver nanoparticle thin films in which samples were instantaneously heated [106]. This trend was

explained as a competition between encapsulant moderated grain growth, and densification of the film. The proposed mechanism of encapsulant moderated grain growth was coalescence of particles. After dissociation of encapsulant from the particle surface, the encapsulant acted as a solvent for nanoparticles to reorganize and bind at similar crystal faces, forming larger particles. The effective size of particles could be expressed as the product of ligand residence time in the films, and particle growth rate. Ligand residence time decreases with increasing temperature as the ligand removal rate is faster. Particle growth rate increases with temperature as a thermally activated process. The peak grain size results at the optimal trade-off between these two effects.

The same framework may be applied to the THG-Ag_2S particles. Between 100C and 250C, the encapsulant has not yet evolved from the film, but is facilitating coalescence and grain growth. As temperature increases, the rate of growth increases resulting in larger grain size. This trend continues until the rate of encapsulant evolution from the film begins to limit the encapsulant residence time and therefore growth time. This occurs between 250C and 350C. Instantaneous heating causes rapid removal of ligand that locks particles in place and arrests grain growth. The optimum grain size occurs in the middle of the mass loss temperature domain in FIG 5-10. This peak size was not observed in the ODA-Ag2S NP XRD data presented in the previous chapter, due to the gradual heating used in the sample preparation. The nanoparticle films proceeded through the low-temperature coalescence phase until ligand evolution. The rate of heating was slow enough such that the particles could grow to a saturated size before ligand was completely removed.

The TGA and EIS data show that for sintered THG-Ag_2S NP films, the onset of mixed conductivity and grain growth occurs at the same temperature, 150C, before ligand evolution from the film. This contrasts with the ODA-Ag_2S NP films, for which grain growth begins before ligand evolution, but conductivity onset was observed after ligand removal, transitioning between a pure electronic and mixed ionic-electronic conducting state. The different steric properties and chemical properties of the encapsulants can explain this. ODA is a bulkier ligand than THG, as illustrated in FIG 5-11. It maintains a large steric separation between adjacent particles during the coalescence phase, preventing flow of electrons and ions. As the ODA is removed from the film, the crystallites come into contact. THG is a smaller ligand, about $1/10^{th}$ the length of ODA. The THG-Ag_2S NPs are also more polydisperse than the ODA-Ag_2S NPs. During the coalescence phase, instead of forming discrete particles separated by the THG, a network of connected particles may be formed that facilities conduction through the entire film. In this way, onset of conduction and crystallite growth would occur at the same temperature in the THG-Ag_2S NP films.

In the THG-Ag_2S films, there was no pure electronic conducting regime observed, unlike the ODA-Ag_2S films. The different nature of the amine silver and thiolate-silver bonds may explain this. In ODA-Ag_2S, formation of a positive surface charge of silver cations was proposed to enhance electron concentration. The source of the positive surface charge was the binding of silver cations by neutral amines through the lone pair of electrons. Thiols are known to bind to silver and other metals as a thiolate anion [126]. In this case, there would be no net surface charge to modify carrier concentration and change the conducting properties.

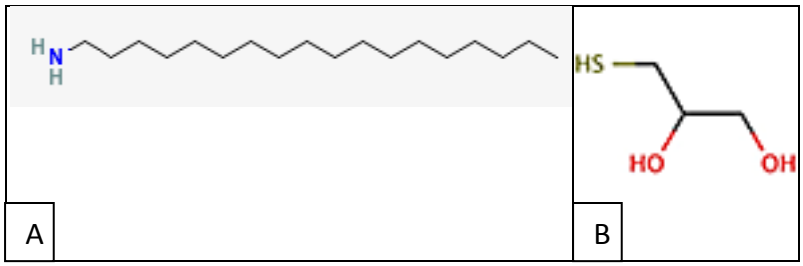


FIG 5-11: (A) octadecylamine(B) thioglycerol

A dependence of mixed conductivity on the grain size was observed in the THG-Ag_2S NP films as show in FIG 5-10. This was not observed in the ODA-Ag_2S NP films because there was no peak grain size dependence, due to the gradual heating method used during sintering. Instead, in ODA-Ag_2S films, the conductivity was correlated to ligand content in the film. The electronic and ionic resistances are both inversely related to grain size. This suggests the conduction mechanisms are grain boundary limited. As grain size increases, the ratio of grain boundary surface area to grain volume decreases. Between the two electrodes, fewer grain boundaries exist in a current path.

There have been several studies in the literature examining the effect of grain boundaries on either electronic or ionic conduction in semiconductors and solid electrolytes[127-132]. One common model is the treatment of the grain boundary as a double-schottky barrier. Interfacial states occupied by ions or electrons create a core surface charge. This induces a surrounding space charge of opposite sign and the potential barrier as illustrated in FIG 5-12. The nature of the core surface charge for pure ionic conductors depends on the relative interstitial and vacancy formation energies. The defect with lower formation energy will dominate in the space charge layer of the bulk, while the core charge will compensate. This has been demonstrated with silver halides where the space charge consists of cation interstitials [131], [133]. The core charge of pure electronic conductors depends on the doping profile and density of trap states [134]. In mixed ionic-electronic conductors, the net surface charge will be a superposition of these two effects. The free surface potential of silver sulfide has been determined to be negative, indicating that there will be an excess of cation interstitials and deficiency of electrons in the space charge region [135]. This condition is illustrated in FIG 5-12.

Although a potential barrier is created, it can only impede one of the two charge carriers. In treatments of pure ionic or electronic conductors, this blocked carrier is usually the majority carrier. In mixed ionic-electronic conductors, the majority ionic and electronic carriers are necessarily of different sign. Thus the electric potential barrier will only impede one of the two carriers depending on the sign of the charge carried. In Ag2S, the electrons would be impeded by the electric potential barrier, while the silver interstitials should be unaffected. However, impedance data shows that both the ionic and electronic conductivity vary with grain size. The grain boundary dependent ionic impedance is hypothesized to arise from some form of chemical barrier.

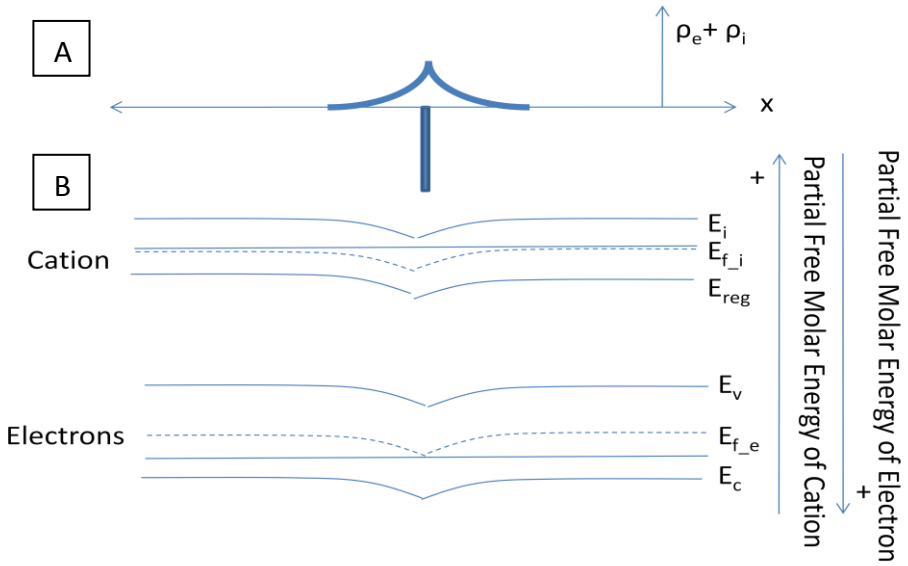


FIG 5-12: A) Charge Density versus Spatial Coordinate. Core charge is negative. Space Charge Region is positive. B) Energy level schematic for cation and electron carriers. Potential barrier exists for one of two carriers.

5.5: Conclusions

The impact of sintering conditions on the mixed ionic-electronic conducting properties of THG-Ag_2S nanoparticle thin films has been studied and contrasted to ODA-Ag_2S NP thin films. A threshold temperature for onset of mixed conductivity exists for both systems, but is lower for THG-Ag_2S because of the lower boiling point of THG. While mixed conducting properties are affected by film ligand content in the ODA-Ag_2S system, they are affected by grain size in the THG-Ag_2S system. The physical-chemical properties of ODA and THG, and film sintering methods explain these differences. Gradual heating versus rapid heating results in either a peak grain size, or a saturated grain size versus sintering temperature. The bulky ODA ligand was able to maintain separate grains, while the small THG ligand facilitated formation of a mixed conducting network at low temperatures. This shows that not only can mixed conducting properties be adjusted through sinter conditions, but also through the selected encapsulant and synthetic method of the starting nanoparticles.

Chapter 6: Filament Formation Studies

The prior chapters presented methods of depositing and controlling microstructure of silver sulfide thin films to tailor mixed ionic-electronic conducting properties. In this chapter, using sintered THG-Ag_2S nanoparticle films, vertical and lateral devices were fabricated and tested. Mechanistic studies on filament formation were conducted in lateral test structures, and corroborated by simulated results. Challenges of using sintered silver sulfide nanoparticles to fabricate vertical structures are discussed.

6.1: Vertical Device Testing

In the majority of publications on RRAMs, the electrolyte layer is deposited by vapor and vacuum techniques such as sputtering and chemical vapour deposition (CVD). These methods usually form high quality dense films and functional devices, but are expensive relative to solution processing. Several research groups have demonstrated functional devices using sol-gel methods to deposit metal oxide electrolyte layers [136-138]. Remarkably, researchers at NIST produced an amorphous TiO_2 layer that showed resistive switching without any required thermal annealing [139]. However, impact of processing conditions on microstructure and device performance has not been investigated in those studies. Recently, Bakishev fabricated a filament memory using sintered ZnO nanoparticle films [140]. The required sinter temperature to produce functional devices was 350C. Whether ligand evolution or kinetic barrier to crystallization is the limiting factor was not explicitly determined. In this section, vertical test devices have been fabricated to explore the feasibility of using sintered Ag_2S nanoparticle thin films to form electrochemical metallization RRAMs.

6.1.1: Device Fabrication

Crossbar structures were fabricated by using thermally evaporated metal electrodes patterned by a shadow mask. Starting substrates were 4” undoped silicon wafers, coated with a 1000Å silicon dioxide layer grown by wet thermal oxidation. THG-Ag_2S nanoparticles were synthesized according to the procedure described in Chapter 5. A bi-layer of 170Å gold on 20Å chrome adhesion was evaporated through a shadow mask onto the wafer substrates. The line width was 100um. The substrates were first rinsed with acetone and isopropanol then blown dry with N_2. These were then exposed to UV-Ozone for 5 minutes immediately prior to spincasting to improve wettability. A THG-Ag_2S nanoparticle solution [50 mg/ml] was pushed through a 0.2 um PVDF syringe filter and then spuncast onto the patterned lines. The spuncast sample was then cleaved into 4 pieces, and sintered at 100C, 150C, 200C and 300C for 1 hour. A 1000Å thick silver electrode was thermally evaporated through a shadow mask onto the substrates forming cross bar structures.

6.1.2: Electrical Testing & Results

The cross bar structures were tested with an Agilent 4155C Parametric Analyzer. In all test cases, the bottom gold cathode was biased to induce resistive switching, while the top silver anode was grounded. Of the 4 samples prepared, only the 100C sintered sample yielded any functional devices. The devices sintered at 150C, 200C, and 300C were all shorted. AFM data from chapter 5 showed that surface roughness of sintered films became significantly larger

after grain growth started to occur in the films. This roughness is likely the source of shorting in the films.

Sample switching data for two functional devices from 100C films are shown in FIG 6-1 operated under two test conditions and plotted in log and linear scales. The testing sequence is enumerated in FIG 6-1A. The forming step was a double voltage sweep from 0 to -0.5V in both cases. The reset step was a double voltage sweep from 0 to 1V in one case, and 0 to -0.6V in the other case. The device that was reset under the 1V sweep showed reverse filament formation. This is affirmed by filament formation studies in lateral test structures that will be described in a latter section. On-Off ratio for the devices was about 10^2. Cycle lifetime for these devices was poor, switching only about 10 cycles before failing as shorted devices.

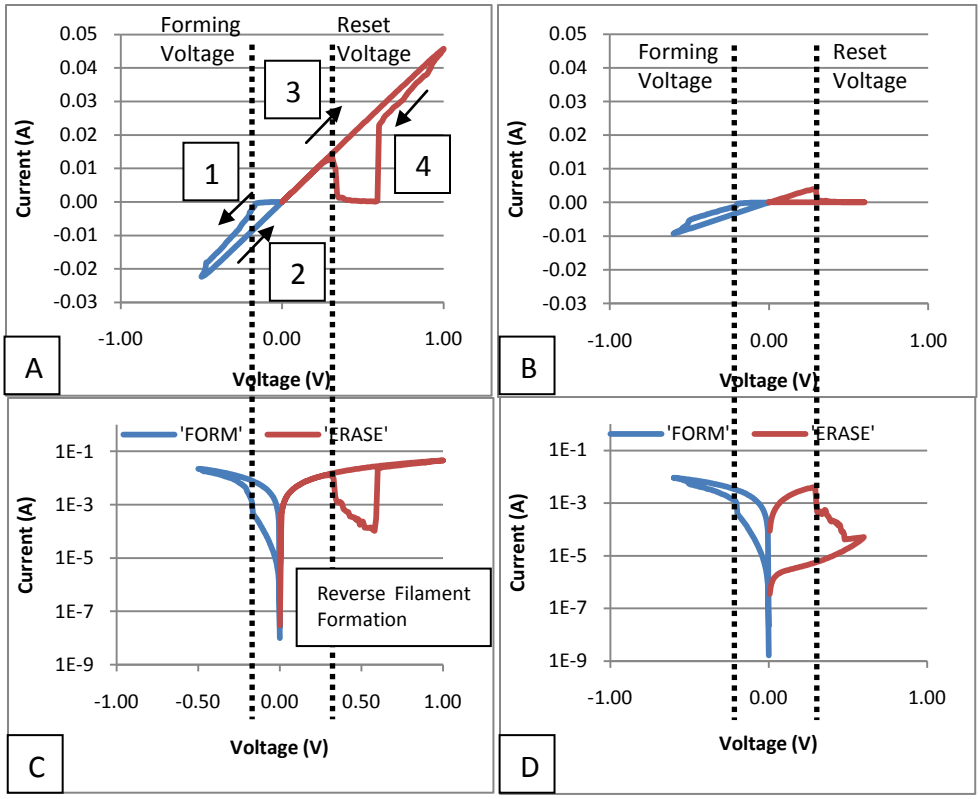


FIG 6-1: IV Switching Characteristic of 100C Sintered Samples. A) Device biased between -0.5V and 1V. B) Device biased between -0.5V and 0.6V. C) Same as plot A, in log scale. D) Same as plot B, in log scale

6.1.3: Discussion

Although functional devices were only yielded on the 100C film due to surface roughness issues, according to EIS measurements in chapter 5, total impedance is highest at 100C. Clear onset of mixed conduction does not occur until 150C. High electric field may explain this discrepancy. In these devices, the electrode gap is about 40 nm, defined by film thickness, compared to the 40 um gap used in the EIS measurements Consequently, the electric field is 3 orders of magnitude higher in the crossbar structures. This may be high enough to cause dielectric breakdown through the film, forming the filament.

The poor program-erase cycling endurance of these devices contrasts with published studies on Ag_2S devices which can be repeatedly program-erased until at least 100 cycles. The test structure may explain this. In the quantized conductance atomic switch fabricated by Terabe, an air gap existed between the Ag_2S electrolyte and Pt cathode [27]. Quantized conductance was achieved only by bridging the air gap at a single point. The silver filament grew from the surface of the Ag_2S, reduced by tunneling electrons across the gap [141]. In the cycle studies by Pi et al on an Ag_2S thin film, a tungsten probe contact was used as the cathode [142]. In both cases, filamentary contact occurred in a narrow region. In the crossbar structures used here, large area electrodes (100 um x 100 um) were used. The high concentration of silver cations initially in the film may have facilitated formation of multiple filaments forming across the electrode surface. Instead of forming and breaking at a single location, multiple filaments may have connected across the surface causing eventual failure into a conductive state.

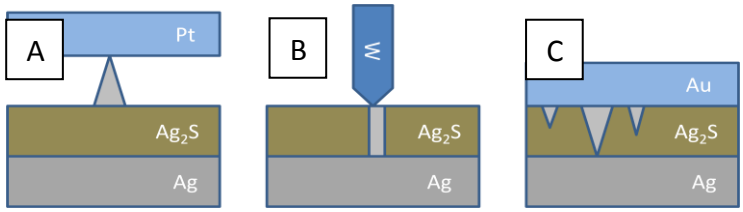


FIG 6-2: Possible Filament Formation Schemes A) Air Gap B) Tungsten Probe Tip C) Contacted Film

6.2: Lateral Device Testing

The impact of material properties and electrical test conditions on the filament forming process is examined in lateral test structures. Direct observation of the filament formation through optical microscopy is possible in lateral structures, but not vertical structures. The formation of silver filaments from silver bromide was reported as early as 1950 by Berry. The silver diffusion was driven by a gradient of silver chemical potential generated by a temperature gradient [143]. A subsequent study by Ohachi explored this same thermally driven chemical diffusion, but across a broad range of silver chalcogenides and silver halides [144]. The earliest reference currently found describing electric potential driven formation of silver filaments in the context of memory was by Hirose in 1975 [145]. More recently, Guo et al have used the SEM to visually observe ex-situ dendrite formation across a 650 nm between Pt and Ag, using DI water as the electrolyte. Hsu et al recently reported in-situ observation of silver filaments forming on the surface of an Ag_2S film by using a conductive AFM tip as the cathode [146]. In that study, a highly direction filament formed, but did not show a morphological dependence on the forming voltage or time. In this section, we explore the impact of forming voltage and microstructure on filament formation rate and morphology. Sintered THG-Ag_2S nanoparticle films were used as a test vehicle for controlling mixed ionic-electronic conducting properties through grain size, as described in Chapter 5. Two regimes of filament formation are observed under potentiostatic test conditions: surface reaction limited and transport limited. Under surface reaction limited conditions at low voltage, near isotropic metal deposition produces low aspect ratio filaments. Under mass transport limited conditions at high voltage, anisotropic diffusion limited aggregation produces high aspect ratio filaments. By varying forming voltage, mixed dendrite morphologies are demonstrated. The forming voltage not only impacts

formation rate and aspect ratio, but also filament stability. Differences between the potentiostatic and potentiodynamic forming conditions are discussed.

6.2.1: Sample Preparation and Experimental Setup

Starting substrates were 4" undoped test grade silicon wafers that underwent wet themal oxidation to grow a 1000A thick SiO_2 layer. THG-Ag_2S nanoparticle solution [50 mg/ml] was filtered through a 0.2 um PVDF filter, and then spuncast at 1000 RPM for 60 seconds onto the wafer substrate. Samples sintered under the same conditions as chapter 5 at room temperature, 50C, 100C, 150C, 250C, 300C, and 350C for 1 hour in N_2. 1000 Å of silver were thermally evaporated through a shadow mask onto the sintered films to form the silver electrode. 100 um wide silver line patterns were formed.

Filament formation tests were conducted using a tungsten probe as the cathode. The lateral spacing between tungsten probe tip and silver electrode was set by using an eye piece graticule. An HP4155C was used to provide the electrical stimulus. Images were collected through a live video camera mounted onto the probe set up. An air table below the probe station reduced effect of vibrations. Testing is done with a series 1KΩ resistor to reduce discharge from stray capacitance in the test setup upon bridging of the electrodes. The current compliance and stop threshold was set such that voltage stimulus would end once the resistance exceed 2KΩ. Accounting for the 1KΩ series resistor, the filament would be 1KΩ.

Several types of forming tests were conducted: potentiostatic, potentiodynamic, and pulse testing. A step input voltage is used in potentiostatic tests, and can show the change in kinetics as a function of electric potential. A sweep input voltage is used in potentiodynamic tests. The sweep rate would be important if kinetics were a strong function of electric potential. Most publications on RRAMs use sweep tests to show transition voltages. To control sweep rate, auto-ranging was turned off on the HP4155C during testing, and sweep rate was controlled by setting pulse duration.

Pulse voltage testing was done to emulate operation in real memory devices. A series of voltage pulses would be sent by peripheral circuitry to the memory cell to program or erase it. Retention and reset tests were not conducted because the filaments showed very poor retention time on the order of tens of seconds.

Initial potentiodynamic, potentiostatic and pulse measurements were done on samples sintered at 150C. To investigate effect of mixed conducting properties on filament formation rate, samples were sintered at various temperatures: 50C, 100C, 150C, 200C, 250C, 300C, and 350C in nitrogen for one hour.

6.2.2: Potentiostatic/Step Voltage Input Tests

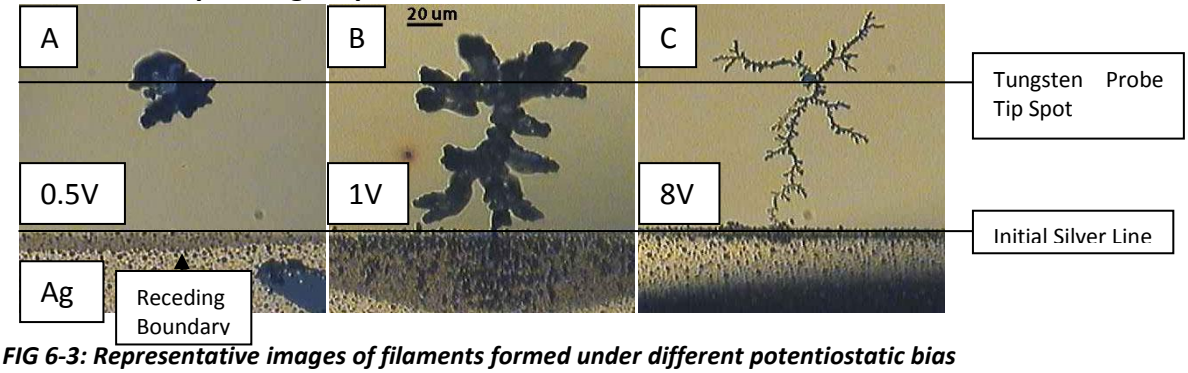


FIG 6-3: Representative images of filaments formed under different potentiostatic bias

Potentiotatic tests were conducted to examine the effect of forming voltage on switching time and morphology. Samples were stimulated by a step voltage of 0.5V, 1V, 2V, 4V, 6V, or 8V. Tests were conducted in time increments to track progress of filament growth. The time increment varied on the applied bias, ranging from 22s for 0.5V, to 50 ms for 8V. Representative micrographs of the filaments are illustrated in FIG 6-3. The silver anode dissolved as the filament formed, as shown by the receding silver boundary. The metrics from these measurements were aspect ratio of the filament and cumulative forming time. Aspect ratio was extracted from the longest filament that eventually contacted the silver anode in FIG 6-3. Forming time was extracted from potentiostatic data as the time the current exceeded the stop condition. FIG 6-4 plots the extracted metrics.

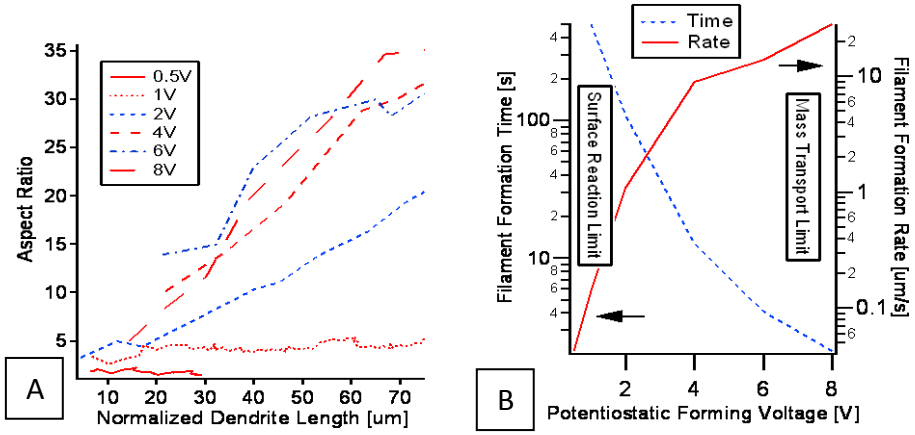


FIG 6-4: A) Filament aspect ratio versus forming voltage and length B) Filament formation time and rate

FIG 6-4A illustrates the progression of the filament growth while FIG 6-4B shows the cumulative switching times and rates. At low voltages, the filament grows isotropically. At higher voltages, the aspect ratio increases as the filament grows. The width remains fairly constant as the length increases. These trends are qualified by the images of the filaments. The forming times and rates show two regions ascribed to a surface reaction limit and mass transport limit. The filament grows isotropically in the surface reaction limit, and more anisotropically as it approaches the mass transport limit.

6.2.3: Potentiodynamic Tests from Ramp Input

Potentiodynamic tests are conducted, varying sweep rate from 0.33V/s to 10V/s and varying forming distance at a constant sweep rate of 0.33V/s. The devices were swept from 0 to 15V, with a current compliance and stop condition of 200uA to prevent filament overgrowth. The metrics from these tests are forming voltage, and forming time. The forming voltage is extracted as the discontinuous change in slope of the IV curve, and is illustrated in FIG 6-1. Extracted metrics are plotted in FIG 6-5.

Potentiodynamic Filament morphology and forming rate show similar trends to potentiostatic testing. FIG 6-5A shows the dependence of filament forming time and voltage on sweep rate. A cross-over point between forming voltage and time occurs. In the limit of fast sweep, the voltage increases at much higher rate than the filament growth leading to complete formation at a high final voltage. At low sweep rate, growth rate is comparable to the sweep rate resulting in lower effective growth voltage. At high sweep rates, the forming voltage is exponentially dependent on sweep rate, but begins to taper off to a constant value at lower sweep rates. As observed from the potentiostatic tests, at too low a voltage, slow isotropic growth occurs. The voltage must exceed some threshold to induce filament growth, otherwise the effective inter-electrode distance will never close. The morphology of filaments shown in FIG 6-5C and D reflect this. The thickness of filament is directly related to sweep rate and is graded as earlier segments are formed under lower effective voltage.

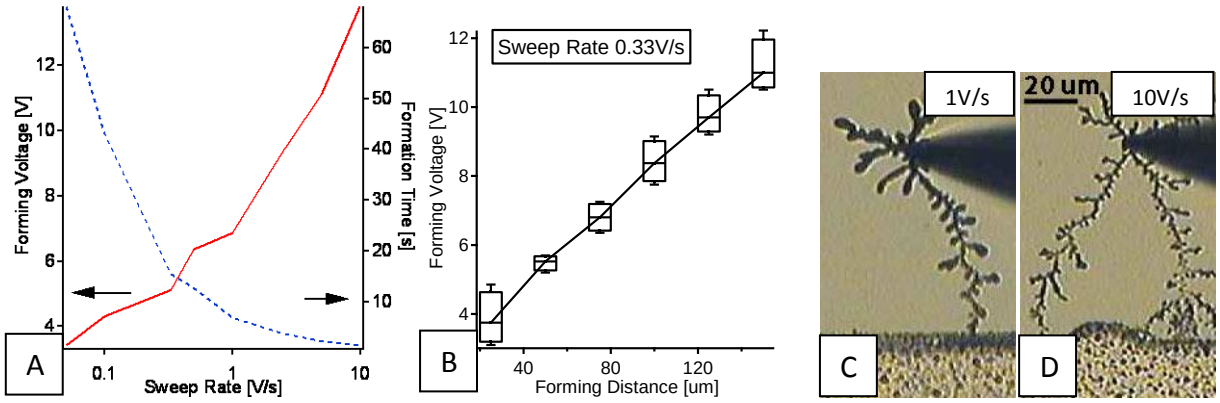


FIG 6-5: Potentiodynamic results: A) Forming voltage and time versus sweep rate. B) Forming voltage versus electrode gap C) Filament formed at 1V/s sweep rate across 75 um gap. D) Filament formed at 10V/s sweep rate across 75 um gap.

FIG 6-5B illustrates the linear dependence of initial forming voltage on electrode gap separation. The voltage intercept at zero forming gap however is non-zero at 2.48 V. This non-zero limit may be rationalized as the overpotential needed to drive electrochemical reactions at the contacts, even in the absence of a transport gap. The relation between forming voltage and gap may change as the gap length scales towards the debye length of the electrolyte when interfacial effects may affect carrier concentrations and surface potentials, as described in Chapter 2.

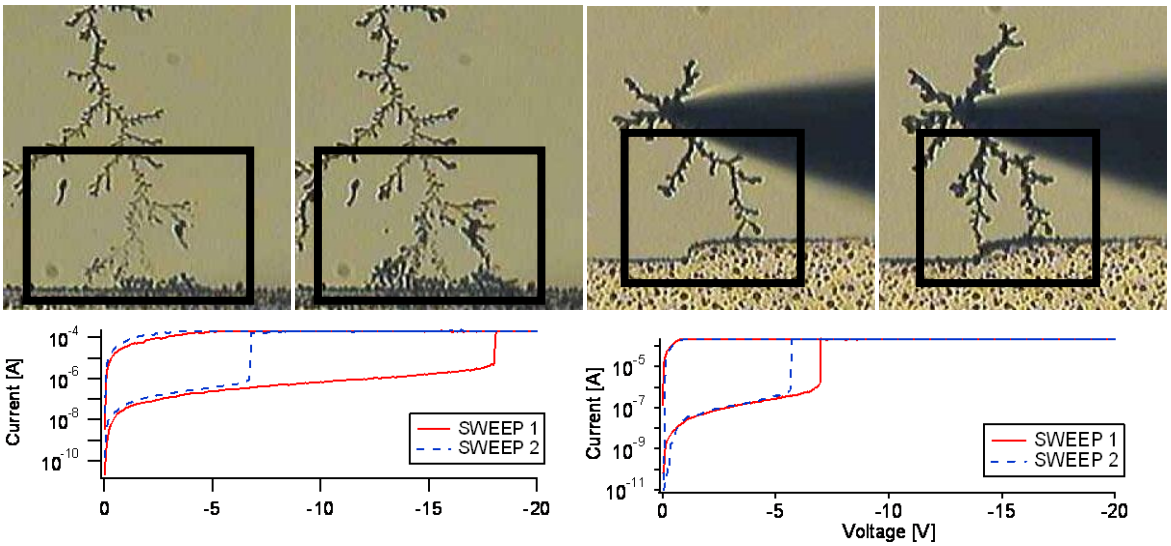


FIG 6-6: Filament Reforming: (Left) Easy Path (Right) New Path

Several devices were reset to a high resistance state by a applying a negative sweep from 0 to 20V at a sweep rate of 10V/s to break the filament. The filament was subsequently reformed by sweeping from 0 to -20V at a sweep rate of 0.33V/s. If the filament were broken and reformed in the same position near its tip, the reforming voltage should be significantly lower than the initial forming voltage. As illustrated in FIG 6-6, the reforming voltage is lower when reforming along the same path as the original filament, but comparable to the forming voltage if it creates a new path.

6.2.4: Pulse Programming: Mixed Filament Morphology and Stability

The potentiostatic tests showed that the filament morphology and growth rate depended on the forming voltage. Given this information, dendrites of mixed morphology and stability could be formed. Testing was done by applying a series of pulses. The pulse duration was 5 ms, and pulse width was 15 ms. 2000 pulses were applied for 2V segments while 100 pulses were applied for 8V segments. The electrode gap was 75 um. The results are illustrated in FIG 6-7. Alternating thick and thin regions are observed, depending on the applied bias.

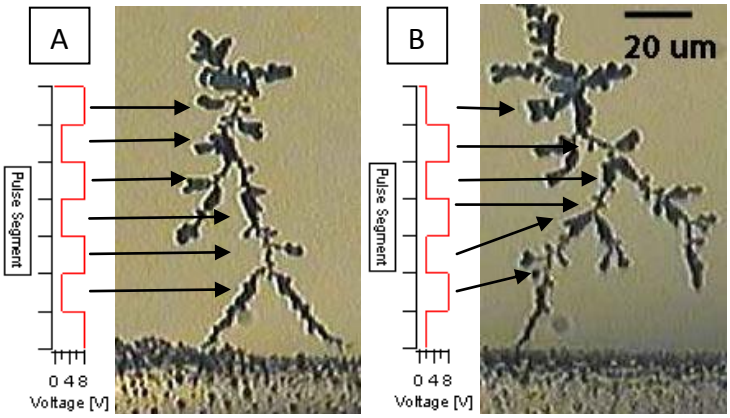


FIG 6-7: Mixed filament shape. Generated by alternating A) 8V and 2V pulses B) 2V and 8V pulses

Stability of the filaments depends on the forming voltage and filament thickness. This was observed in a series of forming experiments across a 75 um electrode gap. The filaments were grown at several different voltages (8V, 6V, 4V) across the initial 55 um, and then 2V for the final 20 um. Representative images of the growth regions are illustrated in FIG 6-8. In the 4V/2V case, growth at 2V completes, bridging the electrodes. However in the 8V/2V case, growth at 2V does not successfully. Instead, dissolution of the initial filament is observed.

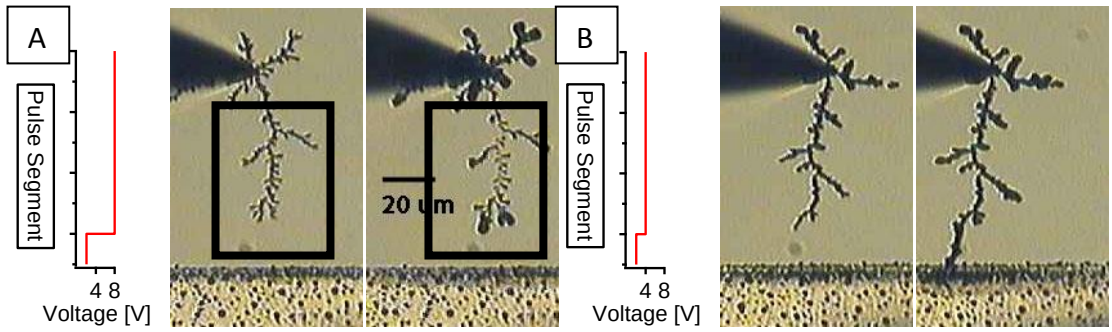


FIG 6-8: Filament Stability A) 8V/2V Forming B) 4V/2V Forming

6.2.5: Sinter Temperature Dependence of Forming

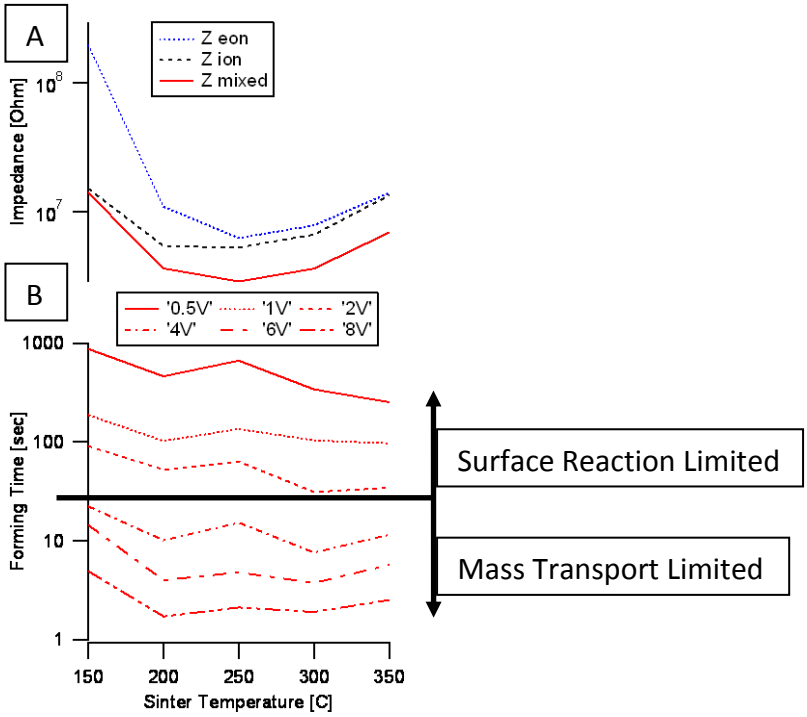


FIG 6-9: Dependence of Forming Time on Sinter Temperature: A)

Chapter 5 showed that mixed conducting properties of THG-Ag_2S nanoparticle thin films could be controlled by the sinter temperature and grain size. Effect of the grain size on filament formation rate was tested by measuring potentiostatic filament formation times on samples sintered at various temperatures. The results are shown in FIG 6-9, along with impedance data reproduced from Chapter 5. FIG 6-4B shows that the forming process

transitions between the surface reaction limit and mass transport limit between 2-4V. The mass transport limited regime is observed as a dependence of forming time on sinter temperature at higher potentiostatic forming voltages in FIG 6-9B. This dependence is less significant in the surface reaction limited regime. This illustrates that sintering conditions of nanoparticles will affect the switching properties. This becomes important during process integration, and will set a thermal budget on the sintered electrolyte, depending on desired switching properties.

6.2.6: Discussion

The experimental results observed in these filament formation studies are consistent with data from other publications. In particular, the voltage-dependent switching mechanisms, and filament morphology stability have been affirmed. A recent STM study by Nayak examines filament formation across a tunneling gap in vacuum between an Ag_2S surface and scanning tunneling microscope (STM) tip [147]. The use of an STM tip allowed rapid testing and avoided the challenges and issues associated with fabricating functional cross-bar devices. Two distinct regions of switching were observed in switching time as a function of applied voltage. Separate activation energies were also extracted from varying the measurement temperature within those switching regions, affirming that two different mechanisms were occurring.

Empirical evidence for the filament morphology stability has recently been published by Tsuruoka et al [148]. In that study, ECM RRAM devices were fabricated using a 15 nm sputtered Ta_2O_5 layer as a solid electrolyte. Voltage dependence of filament formation time was described, although dependence of the ON-state filament resistance on forming voltage was not explicitly mentioned. Several filaments of various resistances were formed and then subjected to read stress at various temperatures. The higher resistance filaments were found to be less stable than the low-resistance filaments, affirming the observations described in FIG 6-8, that showed filaments formed at 8V, were less stable under forward voltage stress than filaments formed at 4V.

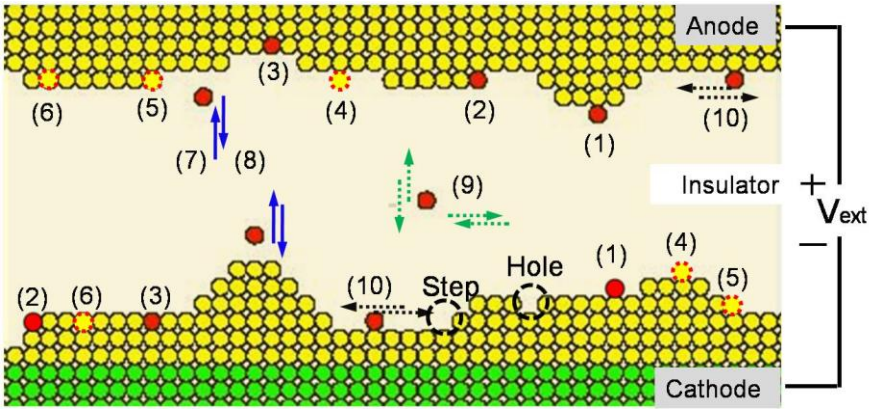


FIG 6-10: Simulated Processes for Filament Formation [149]

The difference in growth morphology of the filaments may be interpreted through a framework developed by Pan and simulated by the kinetic monte carlo (KMC) method

[149][150]. A schematic and table describing the different processes is provided in FIG 6-10 and Table 6-1.

No.	*Process Name:*	*No.*	*Process name:*
(1)	oxidation at adatom site	(6)	reduction at hole site
(2)	oxidation at step site	(7)	adsorption
(3)	oxidation at hole site	(8)	desorption
(4)	reduction at adatom site	(9)	bulk diffusion
(5)	reduction at step site	(10)	surface diffusion

Table 6-1: Summary of basic processes and their standard activation energies (E_a) symbols included in KMC simulation for the ECM cell.

The KMC method calculates transition rates for a set of particles in the system. The state of each particle depends on the activation energies of several possible transition processes. At the electrode three processes can take place: adsorption/desorption, oxidation/reduction, and surface diffusion. In the electrolyte bulk, only bulk ionic diffusion is considered. As a simplifying assumption, the electrolyte is assumed to be a pure ionic conductor. Transient effects of cathodic electrolyte decomposition during initial oxidation and migration of silver from the anode to cathode are ignored. An atom may start in either a hole, step or adatom site at the anode. It may then oxidize, or remain in the same state. Once oxidized, the ion may either desorb from the surface or diffuse across the surface of the anode. If desorbed from the surface, the ion either diffuses through the bulk or re-adsorbs to the surface. If the atom successfully diffuses through the electrolyte, to the cathode, it can repeat a similar set of steps as the anode, in reverse: adsorbing then reducing to an atomic metal again. Applied voltage is modeled as biasing transition rates, so that either oxidation or reduction, or migration in a certain direction is favored. Using this framework, forming times versus potentiostatic voltages are calculated and plotted in FIG 6-11. A threshold voltage is simulated at point (1). This represents the minimum overpotential needed to drive the anodic and catholic reactions for the redox and adsorption/desorption processes. This curve matches well to the experimental data in FIG 6-4B.

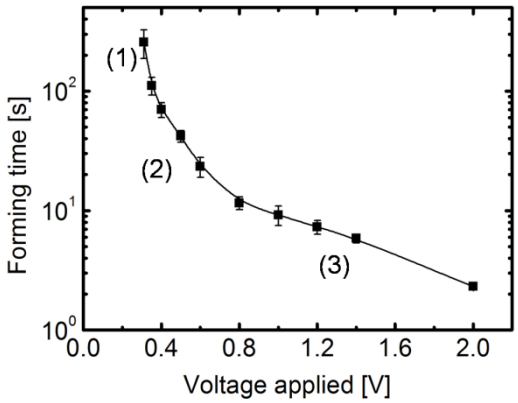


FIG 6-11: Simulated forming time versus potentiostatic forming voltage [149]

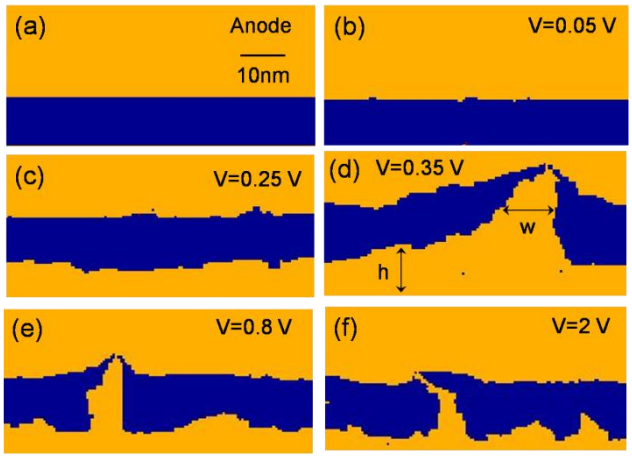


FIG 6-12: Simulated dendrite morphology versus forming voltage [149]

Simulated filament morphologies are also illustrated in FIG 6-12, that closely resemble the experimentally measured images in FIG 6-3. At low voltage bias, isotropic deposition occurs, because the cathodic reduction rate is slower than the surface diffusion rate. Adsorbed ions can migrate across the surface to reduce at more stable step and hole sites, instead of a surface adatom site. As potential increases, filaments start to form as the rate of cathodic reduction is higher than surface diffusion. Also, as the filament begins to grow, the distance between the tip and anode decreases, raising the electric field. Preferential growth will occur at this filament, until it bridges the two electrodes.

While the KMC framework does correspond well with experimental data, it does neglect some key aspects of silver sulfide. Initially, there is a uniform concentration of silver interstitials throughout the solid electrolyte. This facilitates abundant supply of cations to a slow surface reaction. In the model, the surface reaction rate is slower than the oxidation rate and supply of cations, and initially there are no silver cations in the electrolyte. Thus there exists for the model a transient period during which silver migrates from the anode to the electrode, which does not occur in Ag_2S. Despite this subtle difference, the model still simulates the forming process well.

In addition to results that show voltage dependent filament morphology, pulse testing showed that filament thickness could affect stability. In FIG 6-8, the thin filament formed at 8V dissolved, while the filament formed at 4V persisted under subsequent 2V bias. A similar effect has been observed by Peppler et al in their study of silver migration in silver bromide. They observed that an elemental silver deposit in silver bromide, located between two silver electrodes would move under bias from an electric field. This is illustrated in FIG 6-13. The left electrode is biased as the cathode, while the right is biased as the anode. Due to electric and chemical potential differences in the silver bromide, the left side of the silver cluster will act as an anode, while the right side will act as cathode. Thus silver will deposit on the right side of the cluster, and oxidize from the left, moving it through the electrolyte. A precondition of this migration is that the silver cluster is not directly attached to either electrode. In the 8V/2V forming in FIG 6-8B, the thin 8V segment likely breaks, facilitating the diffusion of the resultant silver clusters.

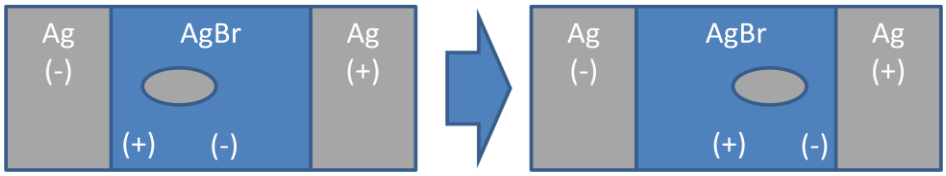


FIG 6-13: Illustration of silver cluster migration in silver bromide

Although these filament formation studies are across forming gaps that are significantly larger than the ~100nm range electrode gaps in vertical crossbar RRAMs, the information about filament growth and morphology can be very useful in developing forming and programming algorithms. In non-volatile memory, fast programming and erase times are desired. In flash, this is achieved by using higher voltages. This study shows that for electrochemical metallization (ECM) RRAMs, there will be a trade-off between retention, and programming speed. Additionally, filament resistance will be affected by geometry and therefore the forming conditions. Low voltage formation will produce a thick filament that is more stable and conductive than high voltage formation. It may also be possible to engineer burn-in protocols during testing of commercial devices. For example, devices may be initially programmed under low voltage to grow a thick filament and then high voltage to form a thin filament near the anode. This would localize the unstable segment of the filament that undergoes switching, potentially improving cycle lifetime.

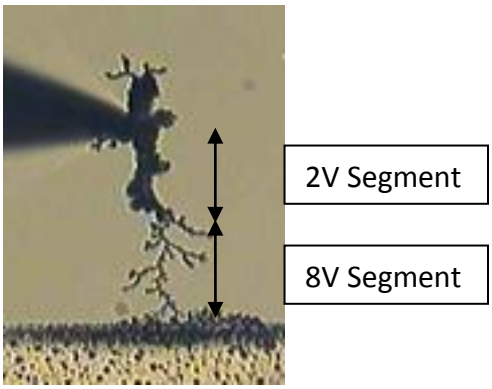


FIG 6-14: Filament grown at 2V/8V

6.3: Conclusions

The effect of forming conditions on filament morphology has been examined. Depending on the potentiostatic bias, there are two regimes, surface reaction limited and mass transport limited. As the voltage bias increases, aspect ratio of the filament increases. Consequently, the shape of filament can be controlled by varying the voltage during formation. This presents a trade-off between switching speed and reliability. Results have been confirmed by KMC simulation of filament forming. Measurements on sintered THG-Ag_2S nanoparticle films shows that the forming time is affected by the microstructure and mixed conducting properties of the electrolyte. Sintering of nanoparticle films has been demonstrated as a method for engineering solid electrolytes.

Chapter 7: Conclusions and Future Work

7.1: Conclusion

In this work, Ag_2S was used as a model material for studying solution processing techniques and engineering of the solid electrolyte layer in ECM RRAMs. Three methods of solution processing were explored: sulfidation and sintering of two types of nanoparticles. The challenges of each method were examined. Sulfidation provided a rapid method for producing Ag_2S films at low temperature but resulted in rough and porous films.

Two methods of sintering nanoparticles were examined. The high temperature organic method used could produce monodisperse ODA encapsulated nanoparticles, but at low yields. The low temperature aqueous synthesis produced polydisperse THG encapsulated nanoparticles in large quantities, but had issues with intrinsic silver contamination. Impact of sintering conditions on grain size and ligand content were correlated to mixed ionic-electronic conducting properties. In sintered ODA-Ag_2S NP films, the boiling point of ODA (350C) limited the minimum temperature of conductivity onset. The film transitioned through a pure electronic conducting phase into a mixed conducting phase as the ligand was removed from the film. In sintered THG-Ag_2S NP films, temperature of conductivity onset was significantly reduced to 190C. The ligand-surface bond now limited the onset of conductivity, not the boiling point of the ligand. Sinter temperature affected the grain size and mixed conducting properties of the film. The ionic and electronic conductivities were observed to be grain boundary limited.

Vertical devices were successfully fabricated only under one sinter condition. Surface roughness and film porosity of the films are still obstacles to realization of vertical cross-bars. Filament formation was studied in lateral test structures of sintered THG-Ag_2S NP films. Two regimes of growth were observed, surface reaction limited at low voltage and mass transported limited at high voltage. Growth was more isotropic at the lower voltages, resulting in thicker and more stable filaments, than those formed at high voltage. The control of filament morphology was demonstrated, and application to programming routines for memories was discussed. Grain size and mixed conducting properties were correlated to filament formation rate. Films with larger grain size and higher electronic and ionic conductivity showed faster filament formation rate. The sintering of nanoparticles to engineer microstructure and mixed conducting properties to affecting the device switching characteristics has been demonstrated.

7.2: Future Work and Outlook

Future development of RRAM technology will require research efforts in various components of the development queue. A sample of various research topics is listed in FIG 7-1 that span the materials-device levels. Higher abstraction levels such as integration with other circuit elements into a functional system are not considered here. This dissertation focused on materials processing and filament formation that is relevant to device characterization. Although Ag_2S was used as a model system, there are many other possible electrolytes, consisting of binary and ternary compounds. Selection of a compound will depend on the mechanism used for switching: cationic migration or oxygen migration. The important intrinsic

parameters for each material include bandgap, ionic defect formation energy, majority defect type and mobility of electronic and ionic carriers. The current selection process of materials is empirical. Electrolytes are selected either for process compatibility in CMOS integration (e.g. Cu_2S, NiO) or based on historically measured data (e.g. Ag_2S). There does exist a large body of information in metallurgy and corrosion literature that about various transition metal oxides and metal sulfides. These texts describe the mobile species during the corrosion process and some information about the diffusion coefficients. Although the measurements have typically been measured at high temperature > 500C, some inferences about room temperature behavior can be made, such as whether the film is likely to be an anionic or cationic conductor. Crystallographic data provides information about interstitial sizes that can guide selection of solid electrolytes.

The field of computation materials design (CMD) aims to streamline the materials selection process by identifying candidate bulk materials for time intensive materials characterization [151]. Although it may not accurately predict absolute values, it may predict trends in materials properties that can be correlated against reference points in the literature. Additionally, polymer electrolytes have been used in ECM RRAMs [152]. The synthetic and structural diversity of block co-polymers opens a whole new dimension of materials for RRAM applications.

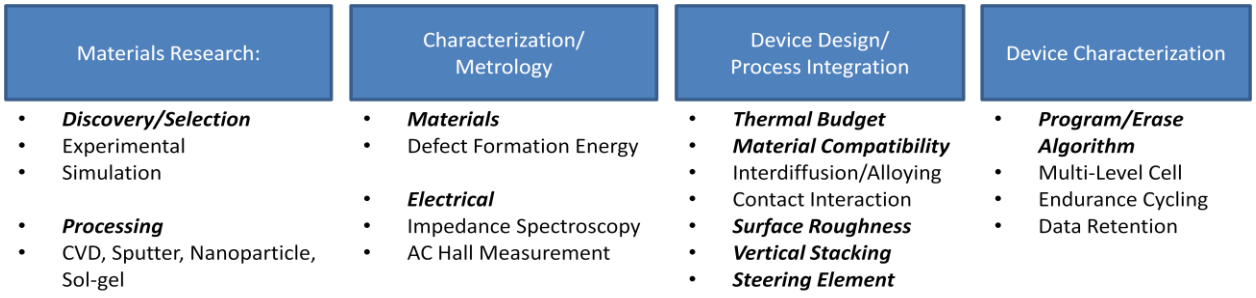


FIG 7-1: Research topics relevant to RRAM

Once candidate bulk materials are identified, processing techniques must be developed for deposition of thin films. Techniques that enable control of microstructure and composition are desirable for studying intrinsic structural effects such as grain size and boundaries, and extrinsic effects of combination with other compounds. Extrinsic effects include homogeneous doping and heterogeneous doping. An example of homogeneous doping is the introduction of dilute amounts impurity, such as the doping of AgCl by $CdCl_2$ to increase silver vacancy concentration. An example of heterogeneous doping by interfacial effects is the composite of AgCl and Al_2O_3 phases that facilitates enchancement of silver vacancies within 2 debye lengths of the surface. Milliron has been examining solution processing methods for producing nanosized composites, in which materials are dominated by the interfacial effects at the scale of the debye length [153]. Given controllable processing methods, combinatorial experimental methods can increase the efficiency of evaluating higher order materials such as ternary and quaternary compounds. The interaction of so many compounds can become incredibly convoluted as different phases interact homogenously or heterogeneously. The use of combinatorial

methods provides an efficient shotgun for empirically exploring the higher order materials space. Sohn has applied genetic algorithms to screen for optimal luminescent phosphors [154].

Characterization techniques and metrology are essential for measuring material properties for further development in application. Electrical impedance spectroscopy was the technique of choice used in this study to deconvolute ionic and electronic conductivity. However, there are still many ongoing research efforts to improve understanding of equivalent circuit modeling of data. The origin of the constant phase element is still being studied [155][156]. Other techniques such as AC hall measurement have not been applied in this study, but may serve as a complimentary method to verify EIS measurements.

Given stable and controllable methods of characterization, process integration and device design may be explored. Challenges include for thermal budgets for materials and exploring interactions between layers. For example, the sintering of nanoparticle electrolytes will place an upper limit on the processing and operating temperature. Just as interfaces are critical in semiconductors devices, in the formation of rectifying or ohmic contacts for example, interfaces will be important in ionic devices. As a cell is scaled towards the debye length of its electrolyte, interfacial effects with the surrounding dielectric isolation may influence the ionic and electronic carrier concentrations, and thus device switching performance. Integration into a functional cross bar array will also require some method to prevent signal bypass from cells in the on-state [157]. As described in the introduction, diode steering elements are commonly used to implement this. For a bipolar device like the ECM RRAMs, a zener diode would be needed to facilitate reversible switching. While zener diodes are commonly made in CMOS through control of silicon doping profiles, a low temperature process will be needed for plastic compatibility in printed electronics. Linn has proposed a stacked pair of ECM RRAM devices that may circumvent the need for a zener diode [31].

A critical requirement for the formation of vertical devices is low porosity and smooth films. Surface roughness and porosity was a consistent problem observed in sulfidized Ag films and sintered Ag_2S NP films. This problem may potentially be resolved either through different selection of material, processing method, or device design. Sintered ZnO films have shown excellent smoothness, at the expense of high temperature [140]. Currently unpublished XRD data shows that there is no grain growth during the sintering process. The grain growth in Ag2S nanoparticle films may be the source of roughness. Selecting a non-coarsening material may resolve the surface roughness problem, but would remove the ability to control electrolyte microstructure and conducting properties by sintering. This may be circumvented by controlling ZnO nanoparticle size pre-sintering, but at the expense of modifying solubility in inks. The use of thermal evaporated has been demonstrated to form smooth films, but is not a solution processable method conducive to printed electronics [79]. A resolution through device design could be integration of a polymer dielectric layer in the device illustrated in FIG 7-2.

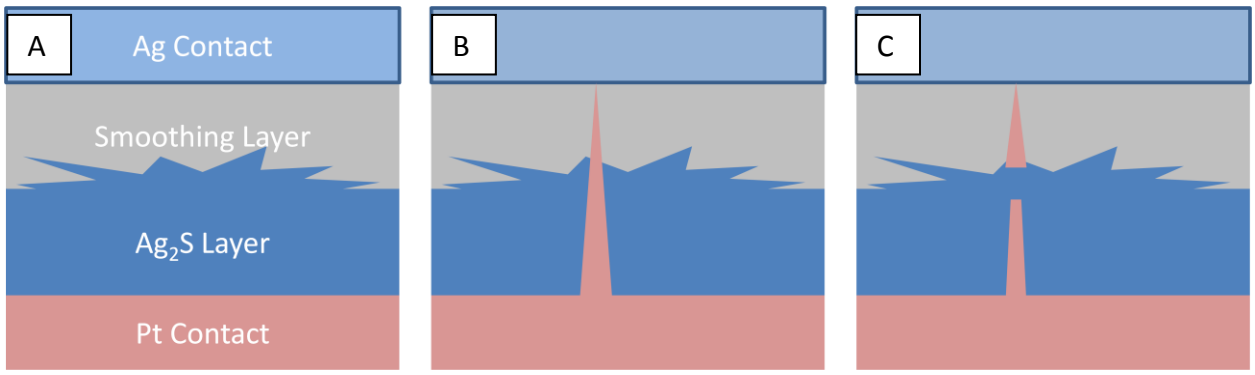


FIG 7-2: Use of smoothing Layer to resolve porosity and roughness (A) Pre-forming (B) Post-forming (C) Post-Reset

The polymer layer would reduce the surface roughness and fill in pinholes in the film. Forming would consist of filament formation and dielectric breakdown of the polymer film. Reset would involve oxidation of the filament in the Ag_2S layer only.

The highest level of abstraction considered here is characterization of device operation. In a memory array, operating parameters such as voltages and pulse times for programming, erase and read will affect the metrics of performance, endurance and retention of the device. Performance is defined as speed of program, erase and read operations. Endurance is defined as the cycle lifetime of the device before failure, and retention is defined as the period of time data can stored in the device without refresh. Chapter 6 explored the effect of filament forming voltages on morphology. A trade-off between filament stability and formation rate was observed. Such knowledge can be applied towards developing programming, erase and read routines for optimizing various metrics of memory cells.

RRAM development draws together many disciplines to engineer a functional device. The work of this dissertation focused on processing techniques for control of electrolyte structure, and study of the filament formation in a cationic mixed conducting material. The demonstration of structural control of conducting properties can be explored in other material systems. The filament formation studies provide guidance for cell operations. There are still many open opportunities and issues to explore in the various disciplines at each abstraction level. Collaborative efforts will inevitably be necessary to span and bridge all these fields.

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