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Technical Report No. UCB/EECS-2010-32

<http://www.eecs.berkeley.edu/Pubs/TechRpts/2010/EECS-2010-32.html>

March 18, 2010

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ABSTRACT

High-performance concurrent libraries, such as lock-free data structures and custom synchronization primitives, are notoriously difficult to write correctly. Such code is often implemented without locks, instead using plain loads and stores and low-level operations like atomic compare-and-swaps and explicit memory fences. Such code must run correctly despite the relaxed memory model of the underlying compiler, virtual machine, and/or hardware. These memory models may reorder the reads and writes issued by a thread, greatly complicating reasoning about parallel interaction and interference.

We propose RELAXER, a combination of a predictive dynamic analysis and software testing, to help programmers write correct, highly-concurrent programs. Our technique works in two phases. First, RELAXER examines a sequentially-consistent run of a program under test and dynamically detects potential data races. These races are used to predict possible violations of sequential consistency under alternate executions on a relaxed memory model. In the second phase, RELAXER re-executes the program with a biased random scheduler and with a conservative simulation of a relaxed memory model in order to create with high probability a predicted sequential consistency violation. These executions can be used to test whether or not a program works as expected when the underlying memory model is not sequentially consistent.

We have implemented RELAXER for C and have evaluated it on several synchronization algorithms and concurrent data structures. RELAXER generates many executions of these benchmarks with violations of sequential consistency, highlighting a number of bugs under relaxed memory models.

1. INTRODUCTION

In a multithreaded program, a *data race* occurs when two threads simultaneously access the same shared variable and at least one of the accesses is a write. Data races are the most common and notorious kind of concurrency bug. The conventional wisdom is that programmers should use synchronization mechanisms such as

```
Initially: x = y = 0;

thread1:      thread2:
1:  x = 1;    3:  y = 1;
2:  t1 = y;   4:  t2 = x;

assert(t1 == 1 || t2 == 1);
```

Figure 1: Program with error under relaxed memory model TSO, but correct with sequentially-consistent memory.

locks to ensure that their programs contain no data races, and a large body of research over the past thirty years has focused on detecting data races in parallel programs.

Yet software developers often write programs with intentional data races. Highly-concurrent libraries, such as lock-free data structures and custom synchronization operations, may contain explicit data races for performance. Such code uses compare-and-swap-like primitives or unsynchronized reads and writes to avoid the overhead of locks. Additionally, developers of large applications often introduce data races to avoid the cost of synchronization on certain frequent operations.

The presence of explicit data races, however, greatly increases the difficulties of writing correct parallel software. In addition to the normal challenges of reasoning about thread interleavings and of nondeterminism in testing and debugging, data races expose the programmer to the underlying *relaxed memory model* of the language and hardware. Under such relaxed memory models, a program can exhibit a wide range of counter-intuitive behaviors that can be quite difficult to reason about.

Consider the example program in Figure 1. The program has two data races—the write of x at Line 1 races with the read of x at Line 4, and the write of y at Line 3 races with the read of y at Line 2. Under sequential consistency, the final assertion will always hold. Either the statement at Line 2 or at Line 4 is the last to execute, so at least one of them must see an earlier write of 1. But, in the absence of any synchronization, most relaxed memory models permit the writes to x and y to be *delayed* or *reordered* so that they occur after the reads at Lines 2 and 4. Thus, the final values of $t1$ and $t2$ can both be 0. That is, these seemingly benign data races can lead to an error under a relaxed memory model.

Thus, there is a need for techniques and tools to aid developers in writing and testing high-performance parallel software with intentional data races. While there exist many tools to help programmers find and reproduce data races in their programs, few address the challenges of ensuring program correctness when these races expose violations of sequential consistency. Recently, there have been a number of efforts to verify and model check concurrent programs on relaxed memory models [4, 19, 8, 25, 2, 9, 3]. Some of these techniques [8, 25, 2] encode a program as well as the axiomatic semantics of the underlying memory model as a constraint system and use a constraint solver to find bugs. Other techniques [4, 19, 9] explicitly explore the state space of a program to find bugs. More recently, SOBER [3] has been proposed for run-time monitoring of sequentially consistent executions to find violations of sequential consistency on “nearby” executions. Although this technique scales and finds bugs, it must be driven by a model checker to encounter executions which come close to a violation of sequential consistency. Moreover, violations of sequential consistency are not

necessarily always bugs in, e.g., highly-concurrent data structures.

In this paper, we propose an *active testing* technique, RELAXER, to detect bugs under relaxed memory models. Active testing [21, 10] is a two-phase analysis and testing approach for predicting and confirming concurrency bugs. Active testing techniques have been developed for detecting real data races [21, 12], atomicity violations [18, 12], and deadlocks [11]. In the first phase of active testing, a static or dynamic analysis is used to predict *potential* concurrency bugs in a test program—e.g. pairs of statements that could be data races. In the second phase, for each potential concurrency bug, the test program is executed with the analysis actively controlling the thread schedule to cause the bug to occur. A concurrency bug is reported to the user only if it is observed in some execution during the second phase—e.g. if a pair of potentially-racing statements actually race in a created execution.

Applying active testing in RELAXER to find relaxed memory model bugs poses several challenges. For the first phase of RELAXER, we must devise an analysis to predict violations of sequential consistency in a test program. We use the existing notion of a *happens-before cycle* to characterize a violation of sequential consistency and formalize a *potential happens-before cycle* as a sequence of potential data races. We propose a simple dynamic analysis that, given a sequentially-consistent execution of a test program, predicts such cycles. In the second phase, RELAXER attempts to create each potential happens-before cycle by running the test program while actively controlling not only the thread scheduler but also the underlying memory model. This enables RELAXER to create feasible potential cycles with high probability and to test if the resulting sequential consistency violations lead to real bugs.

In order to control the underlying memory model, the second phase of RELAXER requires an operational implementation of each relaxed memory model under consideration. In this paper, we consider three memory models, *Total Store Order* (TSO) [22] and *Partial Store Order* (PSO) [22], and *Partial Store Load Order* (PSLO)[14]. TSO allows to delay a store relative to subsequent loads on a processor. The operational model of TSO uses a store buffer for each processor. This memory model is quite similar to that of the x86 architecture. PSO additionally allows to delay stores relative to other stores to different addresses on the same processor. The operational model of PSO is implemented by using a separate buffer for each address per processor. These write-write reorderings are present in many architectures, including Alpha, IA64, and POWER. PSLO captures some of the behaviors of SPARC’s *Relaxed Memory Order* (RMO) [22] and other very relaxed memory models like Alpha, IA64, and POWER. PSLO is like PSO, but additionally allows loads to be reordered to before previous loads and stores on the same processor. The operational model of PSLO is implemented by keeping a per-thread store history for each address.

RELAXER has several advantages:

- RELAXER provides conservative implementations of the operational semantics of various relaxed memory models. These operational models are often intuitive to understand and debug. With RELAXER, a programmer can plug-in an implementation of a relaxed memory model and observe the actual run-time behavior of a program under the model. This can be useful for testing and debugging.
- RELAXER can help distinguish harmful violations of sequential consistency from benign ones. RELAXER, after creating a happens-before cycle, completes the test execution to check for any crashes or functional errors. Further, it produces execution traces that can be used to help debug any errors found.
- RELAXER can quickly trigger memory model related bugs

even though such bugs often happen only under rare schedules and memory operation reorderings. RELAXER does this by predicting potential happens-before cycles and guiding the execution of the program to create the cycles with high probability.

We have implemented RELAXER for C programs and applied it to two mutual exclusion algorithms and several concurrent data structures. Our implementation intercepts all loads, stores, fences, and other memory operations, providing debuggable simulations of these operations under various relaxed memory models. RELAXER rapidly predicts and then creates many executions for these benchmarks in which sequential consistency is violated. Further, RELAXER creates many executions in which violations of sequential consistency lead to program errors, highlighting bugs in the benchmarks under relaxed memory models.

2. PRELIMINARIES

Before describing the RELAXER algorithm, we present some formal background on memory models. In particular, we give an axiomatic description of sequential consistency, along the lines of [3], to help motivate the RELAXER approach.

2.1 Execution Traces

The axiomatic semantics of various memory models are described in terms of an execution *trace* of a program, which is a sequence of events. The events of a *trace* are:

- $ld(l, p, a, v, i, c)$, denoting a load of the value v from memory address a by processor p . The load is the i^{th} instruction executed by processor p according to the program order and it returns the c^{th} value written to the address a . i is called the instruction index and c is called the commit index. l is the label of the instruction (same for below),
- $st(l, p, a, v, i, c)$, denoting a store of the value v at the memory address a by processor p . The store is the i^{th} instruction executed by processor p according to the program order and it is the c^{th} value written to the address a .

We use corresponding projection functions $l(e)$, $p(e)$, $a(e)$, $v(e)$, $i(e)$, $c(e)$ for an event e , and use $o(e)$ to denote the type of e —i.e. ld or st . A trace is generated from a concurrent program execution by logging all loads and stores. For a generated trace:

- For all p , if an event of the form $o(l, p, a, v, i, c)$ is present in the trace, then for all $1 \leq i' < i$, exactly one event of the form $o(l', p, a', v', i', c')$ must be present in the trace.
- For all a , if an event of the form $o(l, p, a, v, i, c)$ is present in the trace, then for all $1 \leq c' \leq c$, exactly one event of the form $st(l', p', a, v', i', c')$ must be present in the trace.

2.2 Sequential Consistency

In order to define a sequentially consistent execution, we define two relations on the set of events.

Events e and e' are related by the *program-order relation*, denoted by $e \rightarrow_p e'$, iff $t(e) = t(e')$ and $i(e) \leq i(e')$. That is, $e \rightarrow_p e'$ when either $e = e'$ or e and e' are events from the same thread and that thread issues e before e' .

Two events e, e' are related by the *conflict-order relation*, denoted by $e \rightarrow_c e'$, iff $a(e) = a(e')$ and either (1) $o(e') = st$ and $c(e) < c(e')$, or (2) $o(e) = st$ and $o(e') = ld$ and $c(e) \leq c(e')$. Informally, $e \rightarrow_c e'$ means that e and e' are operations on the same memory location and e happened first from the point of view of that memory location.

```

Initially: x = y = done = 0;

thread1 {
1:  x = 1;
2:  y = 1;
3:  done = 1;
}

thread2 {
4:  if (done) {
5:      if (x==0)
6:          ERROR;
7:      local = y;
8:  }
}

```

Figure 2: A program correct under sequential consistency, but with an error under relaxed memory model PSO.

The classic *happens-before relation* is defined as follows:

$$\rightarrow_{hb} = (\rightarrow_p \cup \rightarrow_c)$$

Then, we define a trace to be *sequentially consistent* in terms of the happens-before relation:

DEFINITION 1. A trace T is sequentially consistent if \rightarrow_{hb} is acyclic on the events in T .

Note that this condition is equivalent to requiring the existence of a total ordering on the events in T that is consistent with the happens-before relation.

Given Definition 1 above, we can say that a trace generated under a relaxed memory model violates sequential consistency iff the trace contains a cycle under the classic happens-before relation \rightarrow_{hb} . Thus, such a *happens-before cycle* is a witness to the violation of sequential consistency.

3. EXAMPLE

In this section, we give an informal overview of RELAXER on a simple example.

Consider the concurrent program in Figure 2. Under a sequentially-consistent memory model, this program cannot encounter the ERROR at line 6. The only sequentially-consistent thread interleaving in which the second thread reads a non-zero value for done is the interleaving where thread1 runs completely before thread2. In this case, the second thread will also read a non-zero value for x and no error occurs.

However, under many relaxed memory models provided by current multiprocessor systems, the ERROR can be encountered. For example, under the Partial Store Order (PSO) model, the store x=1 in thread1 can be *delayed* until after the store done=1. Thus, it is possible for the second thread to read a value of 1 for done but a value of 0 for x.

We now illustrate how RELAXER creates an execution exhibiting this error. RELAXER consists of two phases. In the first phase, RELAXER examines a sequentially-consistent run of the program to predict possible cycles of program events that would violate sequential consistency. In the second phase, for each predicted violation RELAXER executes the test program on a relaxed memory model with a biased random scheduler to generate an execution in which the violation actually occurs. RELAXER also checks if the violation could lead to a correctness error.

3.1 Phase I of RELAXER

In the first phase of RELAXER, we use a predictive dynamic analysis on a run of the program under test to detect *potential* violations of sequential consistency.

Given a sequentially consistent trace, a *potential happens-before cycle* is a cycle of events e_1, \dots, e_n, e_1 such that the pairs of successive events $(e_1, e_2), (e_2, e_3), \dots, (e_{n-1}, e_n), (e_n, e_1)$ alternate

between being in program order $e_1 \rightarrow_p e_2$ and being *potential data races*. Two events are potential data races if they are from different threads, both access the same memory address, and at least one is a write. That is, if the events would form a data race if run in parallel without any intervening synchronization.

Suppose that RELAXER observes the sequentially-consistent execution where thread1 runs completely and then thread2 runs. There are three potential data races:

- 1: x = 1 and 5: (x==0)
- 2: y = 1 and 7: local = y
- 3: done = 1 and 4: (done)

Thus, there are two *potential happens-before cycles*:

- (1, 3, 4, 5), and (2, 3, 4, 7)

The first because lines 1 and 3 are in program order, lines 3 and 4 are a potential data race on done, lines 4 and 5 are in program order, and lines 5 and 1 are a potential data race on x. The second because lines 2 and 3 are in program order, lines 3 and 4 are a potential data race on done, lines 4 and 7 are in program order, and lines 7 and 1 are a potential data race on y.

(There is no cycle involving just x and y because thread2 reads them in the same order that thread1 writes them.)

In the observed execution, the potential cycle e_1, \dots, e_n cannot form an actual happens-before cycle because the execution is sequentially consistent. But consider corresponding events e'_1, \dots, e'_n from the same statements in a new execution under relaxed memory model. If each potential data race (e_i, e_{i+1}) is resolved so that $e'_i \rightarrow_c e'_{i+1}$, and the other pairs are still in program order, then the corresponding events would be a witness to a violation of sequential consistency:

$$e'_1 \rightarrow_p e'_2 \rightarrow_c e'_3 \rightarrow_p e'_4 \rightarrow_c e'_1$$

3.2 Phase II of RELAXER

Given the two potential happens-before cycles from Phase I, we now give an overview of how RELAXER creates executions under the relaxed memory model PSO in which these cycles actually violate sequential consistency.

Under PSO, a thread is free to locally “buffer” writes to shared memory, deferring the actual write until after later instructions have executed. RELAXER uses this freedom, in combination with control over the thread scheduler, to create happens-before cycles.

Suppose RELAXER is given the first potential happens-before cycle, (1, 3, 4, 5), consisting of the statements at lines 1, 3, 4, and 5. RELAXER begins executing the test program on a single core—i.e. with only a single thread executing at a time.

Suppose thread2 is scheduled first. RELAXER sees that the statement at line 3 is supposed to execute before the statement at line 4, so it delays thread2. Then, when thread1 writes to x, RELAXER intercepts the write (through source instrumentation) and keeps it in a thread-local buffer. The next two statements in thread1 are allowed to execute normally. Before committing the buffered write to x at the end of thread1, RELAXER delays thread1 so that that thread2 will execute next. thread2 will then read 1 for variable done but 0 for variable x.

At this point, RELAXER has created a happens-before cycle—the value written to done at line 3 is read at line 4, while the read of x at line 5 reads a value from before the write at line 1. RELAXER then allows the program to continue executing to determine whether any errors occur. In this case, the execution soon encounters the ERROR at line 6.

RELAXER can then output this execution trace to a programmer as an execution possible under memory model PSO which not only violates sequential consistency, but leads to a program error.

RELAXER similarly creates a sequential consistency violation for potential cycle (2, 3, 4, 7) by delaying the write to x. This execution, however, does not lead to an error. If the test program is fully equipped with assertions to detect incorrect program behavior or output, then the programmer need not examine the execution traces when the assertions all pass. RELAXER can thus be used to test that programs behave as expected under various relaxed memory models.

4. ALGORITHM

In this section, we provide a full description of the RELAXER algorithm. We assume that we are given a concurrent test harness, a closed program with fixed inputs and assertions checking its output.

RELAXER works in two phases. In the first phase, described in Section 4.1, RELAXER runs the test harness on random schedules on the sequentially consistent memory model and observes the various memory load and store events. RELAXER analyzes these events to find sets of events such that the events in each set could form a cycle in the happens-before relation in some other potentially feasible schedule.

In the second phase, for each such set of events, RELAXER executes the program again and actively controls the schedule and memory operations so that the cycle in the happens-before relation gets created with reasonable probability. RELAXER also checks if the assertions in the harness could be violated in the controlled execution; if a violations happens, then RELAXER reports the error along with a concrete execution trace for the purpose of debugging.

The second phase of RELAXER is parameterized by the memory model on which we are testing. In particular, RELAXER requires an operational semantics for a memory model so that it can simulate the model during testing. RELAXER's strategy for controlling the schedule and the behavior of memory operations is then specific to each memory model.

Thus, we describe in Section 4.2 our operation models for three relaxed memory models: TSO, PSO, and PSLO. Then in Section 4.3 we describe Phase II of RELAXER on each model.

4.1 Phase I of RELAXER

In Phase I, RELAXER predicts set of events which could be involved in a potential cycle of the happens-before relation.

For prediction, RELAXER generates a trace of the concurrent program under test by running it on a random thread schedule and on a sequentially consistent memory. Note that we do not address here the problem of executing the test program on a random schedule. There exists much prior work on generating thread schedules for testing concurrent software, including noise making [5, 23], active random scheduling [21, 12], or model checking [24, 15].

We focus only on the problem of predicting potential cycles given an execution trace. For such a trace, RELAXER looks for a sequence of events, not necessarily adjacent in the trace, that form a potential \rightarrow_{hb} -cycle. We now formally define potential \rightarrow_{hb} -cycles.

DEFINITION 2. A sequence of events $e_1, e'_1, e_2, e'_2, \dots, e_n, e'_n$ is called a \rightarrow_{hb} -chain iff

- $\forall j \in [1, n], e_j \rightarrow_p e'_j,$
- $\forall j, k \in [1, n], p(e_j) \neq p(e_k),$
- $\forall j \in [1, n - 1], e'_j$ and e_{j+1} are in potential data race,

Algorithm 1 Phase I of RELAXER

```

1: INPUTS: a trace
2:  $i \leftarrow 1$ 
3:  $C^i \leftarrow \{e, e' \mid e \rightarrow_p e'\}$ 
4: while  $C^i \neq \emptyset$  do
5:   for each  $e$  in the trace and each  $c$  in  $C^i$  do
6:     if  $c, e$  is a chain then
7:       if  $i$  is even and  $c, e$  is a potential  $\rightarrow_{hb}$ -cycle then
8:         report  $l(c, e)$ 
9:       else
10:        add  $c, e$  to  $C^{i+1}$ 
11:      end if
12:    end if
13:  end for
14:   $i \leftarrow i + 1$ 
15: end while

```

i.e. $p(e'_j) \neq p(e_{j+1}), a(e'_j) = a(e_{j+1}),$ and $o(e'_j) = st \vee o(e_{j+1}) = st,$ and

DEFINITION 3. A sequence of events $e_1, e'_1, e_2, e'_2, \dots, e_n, e'_n$ is called a potential \rightarrow_{hb} -cycle iff it is a \rightarrow_{hb} -chain and e'_n and e_1 are in potential data race.

Note that in a potential \rightarrow_{hb} -cycle, for any $j \in [1, n - 1],$ either $e'_j \rightarrow_c e_{j+1}$ or $e_{j+1} \rightarrow_c e'_j$ in the trace. Similarly, either $e'_n \rightarrow_c e_1$ or $e_1 \rightarrow_c e'_n.$ Note that the potential \rightarrow_{hb} -cycle cannot be a real cycle on the happens-before relation of the current trace as the trace is being generated by running the program on a sequentially consistent memory model. However, since e'_n and e_1 are in potential data race and $\forall j \in [1, n - 1], e'_j$ and e_{j+1} are in potential data race, we could expect that one can execute the program in a controlled way on a relaxed memory model where $e'_n \rightarrow_c e_1$ and $\forall j \in [1, n - 1], e'_j \rightarrow_c e_{j+1}$ and thereby creating a real cycle over the happens-before relation. In Phase II, RELAXER tries to create such cycles by executing the program in a controlled way on a relaxed memory model.

For each sequence of events $c = e_1, e'_1, e_2, e'_2, \dots, e_n, e'_n$ that forms a potential \rightarrow_{hb} -cycle, RELAXER records the sequence $l(e_1), l(e'_1), l(e_2), l(e'_2), \dots, l(e_n), l(e'_n).$ Let us denote this sequence of events by $l(c).$ At the end of Phase I, RELAXER reports a set of sequences of instruction labels. RELAXER uses the reports from Phase I in Phase II to try to create those cycles and to check if there could be an error due to the created cycle.

Given a trace, RELAXER computes all potential \rightarrow_{hb} -cycles iteratively as follows. Let C_n be the set of all \rightarrow_{hb} -chains of length $n.$ RELAXER computes potential \rightarrow_{hb} -cycles by iteratively computing $C^1, C^2, C^3, C^4, \dots$ and finding potential \rightarrow_{hb} -cycles in those sets. The iterative algorithm for computing potential cycles is described in Algorithm 1.

Note that in the algorithm, we do not add a \rightarrow_{hb} -chain to C^{i+1} if it is a potential hb -cycle. This ensures that we do not report \rightarrow_{hb} -cycles that can be decomposed into simpler cycles. Moreover, in Algorithm 1, a potential \rightarrow_{hb} -cycle of length $2k$ gets reported k times. For example, if

$e_1, e'_1, e_2, e'_2, \dots, e_n, e'_n$
is reported as a potential \rightarrow_{hb} -cycle, then
 $e_2, e'_2, \dots, e_n, e'_n, e_1, e'_1$

is also reported as a cycle. We remove all such duplicates.

4.2 Operational Models

In this section, we describe our operational models for the three relaxed memory models, TSO, PSO, and PSLO, to which RELAXER has been applied. Note that our operational implementations are a conservative approximation of the full relaxed memory

models. Every behavior our operational semantics generate is allowed by the full memory model, so we report only true bugs and violations of sequential consistency.

In these models, a program consists of a set of parallel processes that issue memory operations such as loads, stores, atomic compare-and-swaps, and memory barriers. A memory model implements these operations, deciding what values are returned to a process whenever it performs a load.

Sequential Consistency (SC).

As a point of comparison, we present in Figure 3 a simple operational model for sequential consistency (SC). In SC, memory is modeled as an array m mapping addresses $a \in \mathbf{Adr}$ to data values $v \in \mathbb{V}$. $\text{store}_{SC}(p, a, v)$ stores value v at $m[a]$, $\text{load}_{SC}(p, a)$ returns the value stored at $m[a]$, and $\text{CAS}_{SC}(p, a, \text{oldv}, \text{newv})$ is an atomic compare-and-swap on $m[a]$. Each function in our operational model executes atomically.

Total Store Order (TSO).

The TSO memory model [22] allows stores to be reordered past later loads, but maintains a total order over stores. To maintain intra-thread consistency, when a store is reordered past a load of the same address, the load still sees the stored value.

Our operational model for TSO is given in Figure 4. To the global memory map from SC, we add a $\text{FIFOQueue } B[p]$ as a store buffer for each process. Instead of directly updating mem-

```

m : array[Adr] of V
l: storeSC(p, a, v) :
  m[a] = v
l: loadSC(p, a) :
  return m[a];
l: CASSC(p, a, oldv, newv) :
  if (m[a] == oldv)
    m[a] = newv

```

Figure 3: Operational Model of SC

```

m : array[Adr] of V
B : array[Proc] of FIFOQueue of Adr×V
l: storeTSO(p, a, v) :
  B[p].addLast((a, v))
storeTSOc(p) :
  (a, v) = B[p].removeFirst()
  m[a] = v
l: loadTSO(p, a) :
  if (B[p].contains((a, *)))
    (a, v) = last element (a, *) of B[p]
    return v
  else
    return m[a]
l: CASTSO(p, a, oldv, newv) :
  membarTSOsl(p)
  if (m[a] == oldv)
    m[a] = newv
l: membarTSOsl(p) :
  while (not B[p].empty())
    storeTSOc(p)

```

Figure 4: Operational Model of TSO

ory, $\text{store}_{TSO}(p, a, v)$ enqueues the pair (a, v) to the local buffer $B[p]$. $\text{store}_{TSO}^c(p)$ is an internal transition that commits to global memory the oldest buffered store for process p . The memory model can non-deterministically call $\text{store}_{TSO}^c(p)$ any number of times at any state of the execution. $\text{load}_{TSO}(p, a)$ reads from main memory unless there is a pending store to a , in which case it returns the value of the most recent pending store.

We implement store-load memory barrier $\text{membar}_{TSO}^{sl}(p)$ by committing all pending stores. Following the SPARC v9 description [22] of TSO, we do not allow compare-and-swaps to be reordered under TSO. We enforce this by including a store-load memory fence in $\text{CAS}_{TSO}(p, a)$.

Partial Store Order (PSO).

The PSO memory model [22] is similar to TSO, but further allows stores to be reordered past later stores to different addresses.

Our operational model for PSO is given in Figure 5. As in SC and TSO, PSO maintains a global memory m . PSO also maintains a store buffer $B_a[p][a]$ for each process p and address a . $\text{store}_{PSO}(p, a, v)$ enqueues v to the buffer $B_a[p][a]$. $\text{store}_{PSO}^c(p, a)$ is an internal transition that commits to global memory the oldest buffered store of process p to address a . The memory system can non-deterministically call $\text{store}_{PSO}^c(p, a)$ for any address a any number of times in any state of the execution. $\text{load}_{PSO}(p, a)$ returns the value from the oldest pending store in $B_a[p][a]$ or from main memory if no stores are buffered.

We conservatively implement both store-store and store-load memory barriers in TSO by committing all pending stores. This is too strict—these fences require only that pending stores commit before later stores commit or later loads are issued. Thus, our operational model does not quite capture all possible PSO behaviors.

Following the SPARC v9 description [22] of PSO, stores can be delayed past compare-and-swaps on different addresses. But pending stores to the same address are committed before the CAS in $\text{CAS}_{PSO}(p, a)$. Our operational model can be easily changed for instances of PSO in which CASs have stronger ordering properties.

```

m : array[Adr] of V
Ba : array[Proc][Adr] of FIFOQueue of V
l: storePSO(p, a, v) :
  Ba[p][a].addLast(v)
storePSOc(p, a) :
  if (not Ba[p][a].empty())
    m[a] = Ba[p][a].removeFirst()
l: loadPSO(p, a) :
  if (not Ba[p][a].empty())
    return Ba[p][a].getLast()
  else
    return m[a]
l: CASPSO(p, a, oldv, newv) :
  while (not Ba[p][a].empty())
    storePSOc(p, a)
  if (m[a] == oldv)
    m[a] = newv
l: membarPSOss(p) or l: membarPSOsl(p) :
  foreach a ∈ Adr
    while (not Ba[p][a].empty())
      storePSOc(p, a)

```

Figure 5: Operational Model of PSO

Partial Store Load Order (PSLO).

The PSLO memory model was proposed by [14] to capture some of the behaviors of RMO [22]. PSLO allows loads to be reordered to before stores and loads of different addresses. This models both speculative issuing of conditional loads (as in RMO) and speculative data-dependent loads (not allowed in RMO).

Our operational model for PSLO is given Figure 6. PSLO is very similar to PSO except that it also maintains a per-process, per-address set S , called *store history*, of past stores. Like in PSO, $\text{store}_{PSLO}(p, a, v)$ enqueues a write and $\text{load}_{PSLO}(p, a)$ returns the most recent pending store if one exists in the local write buffer. But when there is no pending store, $\text{load}_{PSLO}(p, a)$ returns a value chosen non-deterministically from the set $S[p][a]$ of past stores and removes all older stored values. (Intuitively, this models reordering the load back to just after that store committed.)

As in PSO, $\text{store}_{PSLO}^c(p, a)$ commits to the global memory the oldest pending store of process p to address a . In addition, it clears the set of past stores $S[p][a]$ —because no later read of a by p can be reordered before this store. Then for each process p' , it adds the newly-committed value $m[a]$ to the set $S[p'][a]$.

We conservatively implement store-store and load-load fences

```

m : array[Adr] of V
Ba : array[Proc][Adr] of FIFOQueue of V
S : Set[Proc][Adr] of V

l: storePSLO(p, a, v) :
    Ba[p][a].addLast(v)

storePSLOc(p, a) :
    if (not Ba[p][a].empty())
        m[a] = Ba[p][a].removeFirst()
        S[p][a].clear()
    foreach p' ∈ Proc
        S[p'][a].add(m[a])

l: loadPSLO(p, a) :
    if (not Ba[p][a].empty())
        return Ba[p][a].getLast()
    else
        v = a value from S[p][a]
        remove from S[p][a] values earlier
            than v
        return v

l: CASPSLO(p, a, oldv, newv) :
    while (not Ba[p][a].empty())
        storePSLOc(p, a)
    if (m[a] == oldv)
        m[a] = newv
    S[p][a].clear()
    foreach p' ∈ Proc
        S[p'][a].add(m[a])

l: membarPSLOss(p) :
    foreach a ∈ Adr
        while (not Ba[p][a].empty())
            storePSLOc(p, a)

l: membarPSLOll(p) :
    foreach a ∈ Adr:
        S[p][a] = singleton(m[a])

l: membarPSLOsl(p) :
    membarPSLOll(p)
    membarPSLOss(p)

```

Figure 6: Operational Model of PSLO

by committing all of p 's pending stores in $\text{membar}_{PSLO}^{ss}(p)$ and resetting all of p 's store histories in $\text{membar}_{PSLO}^{ll}(p)$. We conservatively implement a store-load fence by performing both of these actions. As in PSO, a compare-and-swap first commits pending stores to the same address and cannot be buffered.

4.3 Phase II of RELAXER

Given operational models for TSO, PSO, and PSLO, we can now describe the RELAXER Phase II algorithm on these models.

In Phase II, RELAXER is given a potential \rightarrow_{hb} -cycle predicted by Phase I. This cycle $c = l_1, l_2, \dots, l_n$ is a list of an even number n of statement labels l_i . Our goal in Phase II is to execute the test program in a controlled way so that its trace contains events e_1, \dots, e_n such that, for $1 \leq j \leq n$: (1) $l(e_j) = l_j$, (2) if j is odd, $e_j \rightarrow_p e_{j+1}$, and (3) if j is even, $e_j \rightarrow_c e_{(j+1)\%n}$.

If these conditions are satisfied, then the e_1, \dots, e_n form a happens-before cycle on the statements l_1, \dots, l_n .

RELAXER focuses on the third above requirement. That is, it bypasses the scheduling of the threads and controls each threads store buffers and store histories to try to create the conflict ordering $e_j \rightarrow_c e_{(j+1)\%n}$ for each even j .

Informally, we aim to cause $e_j \rightarrow_c e_{(j+1)\%n}$ for even j by:

(ODD) When RELAXER encounters an instruction labeled $l_{(j+1)\%n}$, such that $(j+1)\%n$ is odd, it aims to *delay* the instruction so that some other thread can first execute a racing statement l_j . This essentially means buffering $l_{(j+1)\%n}$ if it is a store or pausing the thread for some time before executing $l_{(j+1)\%n}$ if it is a load.

(EVEN) When RELAXER encounters an instruction labeled l_j , such that j is even, it aims to let l_j execute quickly, so that it completes before some other thread executes the racing statement $l_{(j+1)\%n} \in c_o$. In TSO or PSO, when l_j is a write this means immediately committing it (unless some other write is pending). In PSLO, when l_j is a load this means reading the earliest value from the store history (to make l_j happen as early as possible).

We now formally describe RELAXER's Phase II strategy for each memory model. Let c_o and c_e denote the sets of odd-numbered $\{l_i \mid i \in [1, n] \wedge i \text{ odd}\}$ and even- $\{l_i \mid i \in [1, n] \wedge i \text{ even}\}$ labels from the predicted cycle.

```

Bt : array[Proc] of FIFOQueue of N

l: before_storeTSO(p, a, v) :
    if (l ∈ co and rand() < P)
        Bt[p].addLast(time() + delay)
    else
        Bt[p].addLast(time())

l: before_membarTSOsl(p, a) :
    while (not Bt[p].empty())
        waitUntil(Bt[p].getFirst())
        Bt[p].removeFirst()

l: after_anyTSO(p) :
    while (not Bt[p].empty()
        and Bt[p].getFirst() < time())
        Bt[p].removeFirst()
    storeTSO(p)

```

Figure 7: Phase II for TSO

```

 $B_a^t$  : array [Proc] [Adr] of FIFOQueue of N

l: before_storePSO(p, a, v) :
  if (l ∈ co and rand() < P)
     $B_a^t$ [p][a].addLast(time() + delays)
  else
     $B_a^t$ [p][a].addLast(time())

l: before_loadPSO(p, a) :
  if (l ∈ co and rand() < P)
    waitUntil(time() + delayL)

l: before_CASPSO(p, a, oldv, newv) :
  if (l ∈ co and rand() < P)
    waitUntil(time() + delayL)

l: before_membarPSOss(p) :
l: before_membarPSOsl(p) :
  while (∃a such that not  $B_a^t$ [p][a].empty())
    waitUntil( $B_a^t$ [p][a].getFirst())
     $B_a^t$ [p][a].removeFirst()

l: after_anyPSO(p) :
  foreach a ∈ Adr
    while (not  $B_a^t$ [p][a].empty()
           and  $B_a^t$ [p][a].getFirst() < time())
       $B_a^t$ [p][a].removeFirst()
      storePSOc(p, a)

```

Figure 8: Phase II for PSO

Our Phase II algorithms are presented in Figures 7, 8, and 9. The algorithms are described as modifications to the operational memory models. Functions such as `before_load` and `before_store` are executed before each call by a test program to the corresponding memory model function (i.e. **load** or **store**). Similarly, `after_any` is called immediately after any call to a memory model operation. These functions execute atomically with the underlying memory model function, except where they explicitly call `waitUntil`. Further, the Phase II algorithm for PSLO completely replaces `loadPSLO`.

Note that the Phase II algorithms depend on both a notion of *time*—via the `time` function—and a way to pause a running thread until some later time—via the `waitUntil` function. The algorithms work with wall time or a logical time incremented with each executed instruction—we use wall time for simplicity.

Each Phase II algorithm maintains an extra buffer B^t or B_a^t , similar to the buffers the `B` and `Ba`, respectively. Whenever a store is buffered, a corresponding commit time is computed and queued in B^t or B_a^t to record when the store should be committed. The `after_any(p)` functions use these buffers to commit any oldest pending stores whose times have been reached. Thus `after_any` ensures that we immediately commit any pending store which is not explicitly delayed or is behind an earlier commit that was delayed.

Note that each decision to delay a store, pause a thread, or load an old value is gated by a condition: $(\text{rand}() < P)$. That is, we only perform the delay, etc., with probability P , which we set to $P = 0.5$ in our experiments. This helps RELAXER explore all possible dynamic occurrences of static predicted cycles.

Total Store Order.

For TSO, the statements in c_o will always be stores, so there is no need to pause before loads. In keeping with principle (ODD), we buffer stores in c_o for some small time `delay`. Further, we pause before store-load barriers until it is time to commit all pend-

```

 $B_a^t$  : array [Proc] [Adr] of FIFOQueue of N

l: before_storePSLO(p, a, v) :
  before_storePSO(p, a, v)

l: before_loadPSLO(p, a) :
  before_loadPSO(p, a)

l: before_CASPSLO(p, a, oldv, newv) :
  before_CASPSO(p, a)

l: before_membarPSLOss(p) :
l: before_membarPSLOsl(p) :
  foreach a ∈ Adr
     $B_a^t$ [p][a].clear()

l: after_anyPSLO(p) :
  after_anyPSO(p)

l: loadPSLO(p, a) :
  if (not  $B_a^t$ [p][a].empty())
    return  $B_a^t$ [p][a].getLast()
  else if (|S[p][a]| > 1 and l ∈ ce
           and rand() < P)
    return earliest value from S[p][a]
  else
    S[p][a] = singleton(m[a])
    return m[a]

```

Figure 9: Phase II for PSLO

ing stores, so that no purposely-delayed store is committed early.

Partial Store Order.

For PSO, a load or CAS could also be in c_o . So, in keeping with (ODD), we pause for `delayL` before such statements. As in TSO, we pause before forcibly committing any writes at a barrier. We select `delayL < delayS`—i.e. delay writes longer than pausing before stores—to ensure that a write in c_o from one thread does not commit while we are paused before a load in c_o in another thread.

Partial Load Store Order.

We treat PSLO the same as PSO except for two differences. First, when we encounter a load in c_e , as discussed in (EVEN), we read the earliest allowed value. Second, there is no need to pause at memory barriers—even if a store $l_{(j+1)\%n}$ has committed, a later load l_j can still read an earlier value from its thread’s store history.

5. EVALUATION

In evaluating RELAXER, we want to validate two hypotheses:

- (1) RELAXER can predict and create real sequential consistency violations. Further, for a predicted and feasible happens-before cycle, RELAXER creates the cycle with high probability.
- (2) RELAXER can create violations of sequential consistency leading to real bugs in our benchmarks.

5.1 Implementation

In order to evaluate our claims, we implemented RELAXER for C. RELAXER intercepts all of the loads and stores executed by a test program via source instrumentation with CIL [16]. We manually replace calls to synchronization primitives such as pthread locks, GCC atomic built-ins, etc., with calls to RELAXER stubs that translate the operations into loads, stores, CASs, and memory barriers. (Following [22] and [2], we treat lock acquires as load-load barriers

Benchmark	LOC	Average Runtime (seconds)			Cycles Predicted	Cycles Confirmed			# of Bugs			probability of confirming a cycle			
		phase 1	phase 2			TSO	PSO	PSLO	TSO	PSO	PSLO	TSO	PSO	PSLO	
dekker	39	1.133	1.904	2.004	2.477	112	47	45	69	39	38	65	0.69	0.81	0.84
bakery	31	2.285	4.346	3.554	5.409	222	36	75	100	33	68	96	0.85	0.84	0.82
msn	78	2.037	1.183	1.380	1.682	459	0	117	144	0	117	144	-	0.84	0.72
ms2	60	1.033	1.847	2.438	1.781	75	0	2	5	0	2	5	-	1.00	0.57
lazylis	116	1.936	2.675	2.945	3.122	192	0	8	10	0	8	9	-	0.96	0.62
harris	150	4.366	2.775	3.393	3.767	172	0	54	49	0	48	49	-	0.35	0.68
snark	143	6.260	1.664	0.989	1.180	1800	0	647	404	0	419	191	-	0.60	0.59

Table 1: Results of RELAXER experimental evaluation.

and lock releases as store-store barriers.) Together, this gives each memory operation a unique static label.

RELAXER then provides implementations for each memory operation for our four memory models: SC, TSO, PSO, and PSLO. In addition to simulating the desired memory model, these implementations generate a trace of an executing test program and perform the controlled scheduling of the Phase II algorithms. The cycle prediction of Phase I is run off-line on generated execution traces.

Column 2 of Table 1 reports the average running time in seconds of Phase I of RELAXER for each benchmark—i.e., the time to execute once the benchmark’s test script (defined below), predicting cycles via Algorithm 1. Columns 3 through 5 report average running times in seconds for Phase II for TSO, PSO, and PSLO—i.e., for one predicted cycle, the cost of one execution of the test script, guiding the thread schedule and memory model and including monitoring to determine whether or not the target happens-before cycle is created.

5.2 Benchmarks

We evaluate RELAXER on seven benchmarks, listed in Table 1. Benchmarks *dekker* and *bakery* are Dekker’s algorithm and Lamport’s bakery algorithm [13], both classic solutions to the mutual exclusion problem. The other five benchmarks are concurrent data structures—we use the implementations from [2], another study of correctness under relaxed memory models. The benchmarks are *msn*, a non-blocking queue, *ms2*, a two-lock queue, *lazylis*, a list-based concurrent set, *harris*, a non-blocking set, and *snark*, a non-blocking double-ended queue.

None of these benchmarks are closed programs. To apply RELAXER to them, we need test harnesses to exercise the benchmark code. Along the lines of [2], we manually constructed a handful of test harnesses for each benchmark. A test script for each benchmark executes its test harness 100 times. For *dekker* and *bakery*, our test harnesses contain two threads that use the provided mutex to protect a critical section. Each thread executes its critical section three times and assertions check that the two threads are never concurrently in their critical sections. For the concurrent data structures, each test harness runs multiple data structure operations in parallel and asserts that the results are correct. We check the result by comparing against a set of all possible results when the test harness is run with each data structure operation run atomically. These harnesses are a proxy for the kinds of parallel unit tests we expect a developer would use with RELAXER.

We report experimental results only for the largest test harnesses we tried for each data structure. The results are similar for the smaller harnesses, except that they have fewer predicted, confirmed, and buggy SC violations. These harnesses are:

- For queues *msn* and *ms2*, one thread performs two enqueues, two dequeues, then an enqueue while a second thread performs two dequeues, two enqueues, then a dequeue.
- For sets (sorted lists) *lazylis* and *harris*, insert 3 and then 7, and then in three parallel threads: (1) insert -1 then

remove 2, (2) remove 3, insert 1, then check membership of 7, and (3) check membership of 3 and then insert -5.

- For double-ended queue *snark*, two parallel threads both performing: push-right, push-left, pop-right, then pop-left.

5.3 Experimental Setup

We run each of the test scripts described in the previous section once under sequential consistency (SC) and record the execution traces. These schedules are generated via noise making [5, 23]—each SC memory operation contains a small, random sleep. These traces are fed to Phase I of RELAXER and we record all predicted happens-before cycles of length 4. We focus on length-4 cycles because they capture sequential consistency violations involving two threads and ordering of memory operations on two addresses.

For Phase II of RELAXER, for each predicted cycle, we run 30 trials of a benchmark’s test script under each of TSO, PSO, and PSLO. We record which cycles we are able to create in a real execution, and which of these confirmed sequential consistency violations leads to program errors—i.e. incorrect output, assertion failures, or memory errors.

5.4 Experimental Results

Table 1 summarizes the results of these experiments. For each benchmark listed in Column 1, the number of unique cycles predicted by Phase I is reported in Column 6. Columns 7, 8, and 9 report the number of these predicted cycles that RELAXER was able to create under each of the three memory models. That is, a predicted cycle is “confirmed” if, in at least one of the 30 trials, RELAXER produced a real violation of sequential consistency among the static statements in the cycle.

The number of predicted and confirmed cycles validates the first part of our Hypothesis (1): RELAXER can predict and then create many real violations of sequential consistency in our benchmarks.

In the last three columns of Table 1, we estimate the average probability, over all feasible, predicted cycles, with which RELAXER creates a cycle. As we cannot know which cycles are truly feasible, we assume a cycle is infeasible under a memory model if no RELAXER trial on that model ever creates it. For each cycle created at least once, we estimate its probability of being created by RELAXER as (# times created)/(# trials).

These probability estimates provide evidence for the second part of Hypothesis (1). RELAXER can reliably create most of these feasible cycles by running Phase II only a handful of times.

Columns 10, 11, and 12 of Table 1 report the number of confirmed sequential consistency violations from Columns 7-9 which lead in at least one trial to a program error. That is, RELAXER was able to cause a program error by forcing the statements in a given predicted happens-before cycle to actually witness a violation of sequential consistency.

The number of observed program errors provides evidence for Hypothesis (2): RELAXER can produce real bugs involving relaxed memory models. We examine some of these bugs in greater detail.

```

struct Q {
    lock H, T;
    node *hd, *tl;
}

enqueue(Q, data):
1: n = new_node();
2: n->data = data;
3: n->next = NULL;
4: lock(Q->T);
5: Q->tl->next = n;
6: Q->tl = n;
7: unlock(Q->T);

struct node {
    node* next;
    void* data;
}

dequeue(Q):
8: lock(Q->H);
9: n = Q->hd;
10: nhd = n->next;
11: if (nhd) {
12:   Q->hd = nhd;
13:   unlock(Q->H);
14:   return nhd->data
15: }
16: unlock(Q->H);
17: return NOT_FOUND;

```

Figure 10: Core of ms2 benchmark.

```

Initially flag0 = flag1 = 0.
thread0:
...
1: flag0 = 1;
2: while (flag1)
3:   if (turn) {
4:     flag0 = 0;
5:     while (turn)
6:       ;
7:     flag0 = 1;
8:   }
// Critical
// section
9: turn = 1;
10: flag0 = 0;

thread1:
...
11: flag1 = 1;
12: while (flag0)
13:   if (!turn) {
14:     flag1 = 0;
15:     while (!turn)
16:       ;
17:     flag1 = 1;
18:   }
// Critical
// section
19: turn = 0;
20: flag1 = 0;

```

Figure 11: Core of dekker benchmark.

Partial Initialization Bug(s).

Figure 10 lists simplified enqueue and dequeue methods from benchmark ms2. The queue is a linked list with different locks H and T for protecting the head and tail. When empty, the list contains a single, “dummy” element.

RELAXER reports two buggy cycles for this benchmark: (2, 5, 10 14) and (3, 5, 10, 10). In both cases, under PSO a write in dequeue to a field of a newly-allocated node can be delayed until after the node is added to the list at line 5. This allows an enqueue from another thread to read a random, uninitialized value for nhd->data or n->next, leading to an incorrect return value or a memory error.

RELAXER found cycles exhibiting this *partial initialization* bug in every data structure benchmark. To prevent such bugs, store-store memory fences are needed—e.g., before line 5 in ms2.

Under PSLO, many of these bugs are possible even with added store-store fences. A thread is permitted to read the out-of-date, uninitialized value of nhd->data at line 14 even after reading at line 10 the more recent value of n->next. This models a processor speculating n->next and loading n->next->data before the load of n->next completes. Load-load fences are needed to prevent such bugs. (Note that cycle (3, 5, 10, 10) is not in PSLO \ PSO because unlock is a load-load fence.)

Read-After-Delayed-Write Bug(s).

Figure 11 lists the core of the dekker benchmark. The intention is that only one thread at a time can pass through to its critical section. When RELAXER predicts and creates the cycle (1, 2, 11, 12) under the TSO memory model, it buffers the writes to flag0 and flag1. Thus, the reads at lines 2 and 12 see flag0 = 0 and flag1 = 0. This both violates sequential consistency and lets the

```

Initially flag0 = 1, turn = 0.
thread0:
...
9: turn = 1
10: flag0 = 0
...
1: flag0 = 1
2: read flag1 (1)
   -- SC violated --

thread1:
14: flag1 = 0 [delayed]
15: read turn (0)

```

Figure 12: Trace of dekker with a benign violation of sequential consistency: 14 →_p 15 →_c 9 →_p 2 →_c 14.

two threads erroneously enter the critical section at the same time.

This is a well know issue in Dekker’s algorithm—to function correctly on a relaxed memory model such as TSO, a store-load fence must be placed between between lines 1 and 2 and between lines 11 and 12. RELAXER similarly finds errors via cycles (1, 2, 17, 12) and (7, 2, 11, 12), showing that store-load fences are needed immediately after lines 7 and 17. RELAXER finds similar known issues in the Bakery algorithm, where mutual exclusion is violated if certain groups of stores are delayed past several later loads. No TSO bugs were found for the other benchmarks—we believe they are free of such read-after-delayed-write bugs.

5.5 Discussion

As RELAXER is a testing tool, it produces no false warnings. However, it can have false negatives—i.e., fail to report bugs. We next discuss some sources of this unsoundness.

First, RELAXER could fail to predict a feasible cycle. This could happen if the test harness provided is not sufficient to predict all program behaviors. The source of this unsoundness could perhaps be removed by using symbolic test generation [7]. In this paper we manually generated tests. Further, we used a very coarse predictive analysis to get better coverage of all feasible cycles.

Second, even if RELAXER predicts all feasible cycles, it may not be able to confirm all such cycles. There are a couple of reasons behind this. In order to create a difficult cycle: (1) a store may be required to remain buffered for a long time (unlikely in practice), and (2) a complex thread schedule may be required. For example, consider the predicted cycle (9, 10, 12, 15) for benchmark dekker. This cycle is feasible, but it requires thread0 to buffer a write to turn while thread1 enters, runs, and exits its critical section and then while both threads simultaneously try to enter their critical sections again. We were not able to confirm several predicted cycles in our benchmarks, both because our coarse predictive analysis reported many infeasible cycles and because we missed some difficult-to-create cycles.

Third, even if RELAXER confirms all feasible cycles, it may not be able to classify all cycles as buggy. A key reason behind this is that some of the cycles are benign and cannot lead to a bug under any circumstances. We analyzed dekker for benign cycles and we found that some confirmed cycles, which were not reported as buggy by RELAXER, were indeed benign. We discuss such a benign cycle in some detail below.

Benign dekker Cycle.

Consider potential happens-before cycle (9, 2, 14, 15) for benchmark dekker, listed in Figure 11. This happens-before cycle is created in the trace shown in Figure 12. Initially, thread0 is in its critical section, and thread1 is waiting to enter. thread0 exits its critical section then attempts to reenter. The write of 0 to

Initially: $x = y = 0$	
thread1	thread2
1: $x = 1;$	6: $f1();$
2: $r1 = y;$	7: $lock(L);$
3: $lock(L);$...
...	8: $unlock(L);$
4: $unlock(L);$	9: $y = 1;$
5: $f2();$	10: $r2 = x;$

Figure 13: Program with rare TSO sequential consistency violation ($r1 = r2 = 0$). $f1$ and $f2$ are long-running functions.

$flag1$ at line 14 is buffered, so that the read of $flag1$ at line 2 sees an old value. Note that this cycle is feasible even with all of the necessary store-load fences added to `dekker` (e.g., one between lines 1 and 2).

This violation is benign because `thread0` will wait for `thread1` to modify `turn` and `thread1` will eventually see the write of 1 to `turn` and enter its critical section. More generally, we can see that there is no need for any global ordering between lines 14 and 15 or, similarly, lines 4 and 5. (Along the same lines, it is safe for a processor, compiler, or run-time to reorder the writes at lines 9 and 10 or lines 19 and 20.)

By quickly confirming buggy cycles, RELAXER can help separate buggy cycles from benign cycles like the above example.

6. RELATED WORK

This work is related to a number of recent techniques that have been proposed to confirm potential bugs in concurrent programs using random testing. Havelund et al. [1] uses a directed scheduler to confirm that a potential deadlock cycle could lead to a real deadlock. Similarly, ConTest [17] uses the idea of introducing noise to increase the probability of the occurrence of a deadlock. Active random testing [21, 10] has been proposed to confirm data races and deadlocks by biasing a random model checker. CTrigger [20], instead of trying out all possible schedules, uses trace analysis to systematically identify (likely) feasible unserializable interleavings for the purpose of finding atomicity violations.

Recently, Flanagan and Freund proposed to use an adversarial memory to discover at run-time if a data race in a Java program could be harmful under Java's relaxed memory model [6]. For a read operation involved in a data race, the technique checks if there exists a different return value allowed by the Java Memory Model, that would cause the program to exhibit a bug.

As mentioned in Section 1, there have been a number of efforts to verify concurrent programs under relaxed memory models through explicit state model checking [4, 19, 9] or bounded model checking [8, 25, 2], by translating both a test program and an axiomatic specification of a memory model into SAT.

Run-time monitoring algorithms, such as SOBER [3], scale well in practice; however, they need to be driven by a model checker to find all violations of sequential consistency. For example, consider the program in Figure 13. If $f1()$ and $f2()$ are large, expensive functions, then the first thread will acquire lock L before the second thread in almost all executions. If SOBER sees only such runs, it cannot detect the potential violation of sequential consistency. But if RELAXER sees any run of this program, it will predict the cycle (1, 2, 9, 10) and can then direct the program's executions to create the sequential consistency violation. In addition, RELAXER is easily adapted to any memory model for which we can develop an operational approximation, such as PSO and PSLO, while SOBER can currently be applied only to TSO.

7. REFERENCES

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