Compositional Design of Analog Systems Using Contracts

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This work is dedicated to my supporting family and friends. I'd like to give a special thanks to my advisor Professor Alberto Sangiovanni-Vincentelli, as well as all my dissertation committee members.

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by

Xuening Sun

A dissertation submitted in partial satisfaction of the
requirements for the degree of
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in

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Committee in charge:

Professor Alberto Sangiovanni-Vincentelli, Chair
Professor Jan Rabaey
Professor David Brillinger

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Abstract

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Professor Alberto Sangiovanni-Vincentelli, Chair

This work addresses the problem of assembling analog integrated systems out of pre-designed IP components. Efficient system-level design is increasingly relying on hierarchical design-space exploration, as well as compositional methods, to shorten time-to-market, leverage design re-use, and achieve optimal performances. However, in analog electronic systems, circuit behaviors are so tightly dependent on their interface conditions that accurate system performance estimations based on characterizations of individual stand-alone circuits is a hard task. Since there is no general solution to this problem, analog system integration has traditionally used *ad-hoc* solutions heavily dependent on designers' experience and detailed knowledge of the target application.

A system composition method is proposed that build upon the *analog platform-based design* (APBD) methodology by exploiting assume-guarantee reasoning, *contracts*, to enforce *correct-by-construction* system-level composition. Contracts intuitively capture the thought process of a designer, who aims at *guaranteeing* circuit performance only under specific *assumptions* (e.g. interface loading or dynamic range). Contracts can be broadly classified into two categories: *horizontal* contracts between components of the same abstraction level and *vertical* contracts between a system at level $l + 1$ and the components that make up the system from level l. Horizontal contracts can be used to ensure that correct component behavior by constraining the external environment settings to be within the assumed range. Vertical contracts capture assumptions that system-level designers introduce by leveraging knowledge about the system architecture, which is not available at the component-level. *Contracts* can be naturally incorporated into the APBD design flow to ensure accurate design space explorations and correct design implementations.

The methodology is applied to several case studies to demonstrate the value of our approach. First, an ultra-wide band receiver front-end is composed using horizontal contracts to preserve the correct behavior of pre-designed IP components in composition and to allow design decisions to be reliably made at a higher abstraction level, both key factors to improve designer productivity. In another case study for composition of an analog feedback systems, the Sallen-Key cell, I show the application of both horizontal and vertical contracts so that the performance of a composition of circuit blocks not only preserves component behavior, but also satisfies system specifications

and requirements. Finally, the methodology is applied to the complete design study of the UWB receiver chain for the Intelligent Tire System to demonstrate hierarchical design space exploration using analog contracts. The study shows that given a library of components, an optimized system can be quickly realized through hierarchical construction of subsystems and propagation of contracts. The works featured are seminal to further advancements in bridging the gap between system-level and circuit-level design in the analog/mixed-signal domain.

To my supporting family and friends.

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support, I would not be the person that I am today. For this, I am grateful.

Chapter 1

Introduction

Electronic systems are an integral part of modern society. The global semiconductor market in 2010 reached an astonishing $300.3 Billion, after a 31.5% post-recession growth from 2009. [2] Indeed, industry demands remain strong, and as the pace of innovation continues to accelerate, semiconductor technology is pushed beyond the realm of computing and becomes pervasively applied across all industry sectors. In the energy sector, smart-meters pave the way for the next generation of efficient power distribution, load-balancing, and demand-response. [3] In transportations, micro-sensors help monitor and manage congested traffic. [4] In the automotive industry, X-by-wire systems have replaced traditionally mechanical control to improve handling, safety, and ergonomics for the driver. [5] In healthcare, brain-machine interfaces may, one day, enable paraplegic patients to walk again. [6] And in the military space, unmanned vehicles and robotics can replace humans in reconnaissance missions exploring uninhabitable terrain or dangerous unknown habitats through use of complex electro-mechanical sensor systems. [7]

The deep immersion of electronic systems is driven by a combination of innovations in sensor/actuator technology, shrinking devices, system integration, packaging, wireless communication, and embedded software. One key technology component is the set of analog, mixed-signal, and RF (AMS/RF) systems that lie at the interfaces, bridging the physical world with the digital processing cores. Without these systems, such rich physical interactions and novel applications would not be possible. However, the development process for AMS/RF systems still heavily relies on manual efforts in transistor-level design and physical layout and is one of the main bottlenecks in the design and implementation of new electronic applications.

1.1 Trends and Challenges

The development of the electronics industry over the past half-century have been largely fueled by advancements in digital CMOS technology and guided by Moore's Law. [8] Innovations from the electronic design automation (EDA) industry have allowed digital designers to handle the exponential increase in system design complexity by raising the level of abstraction from transistor-level to gate-level, register-transfer-level (RTL), and most recently, electronic-system-level (ESL). [9] Unfortunately, EDA counterparts for analog and mixed-signal systems have remained elusive, and systems still primarily rely on manual design and integration efforts.

As new applications become more complex, heterogeneous, and deeply immersed into the physical world, the lack of tools and design methods to effectively address the increasing design complexity of AMS/RF systems becomes a major hindrance. Traditionally stand-alone AMS/RF blocks, such as PLL or transceiver front-ends, are increasingly being integrated onto the same chips as the digital processing cores in order to minimize fabrication costs and to improve performances. As of 2009, 90% of all systems-on-chip (SoC) contain analog circuitry and take up 20% of the physical area.[10] And according to industry estimates, between 50-70% of SoC respins are due AMS issues, each of which incur an extra $5-10 million to the non-recurring-engineering (NRE) cost and six- to eight-week delay in product delivery. [11, 12] AMS issues are not only concerns for SoC designers, but also for historically digital-dominated microprocessor and graphic processor companies such as Intel and nVidia. As pointed out by Intel Fellow, Greg Taylor, at the 2010 VLSI Conference, more than 20 different types of analog components (ranging from I/O buses and clock generator to thermal sensors, power management units, and fuse control) exist on each Intel microprocessor for technology nodes at 90nm and below, with the number rapidly increasing for each new process generation.[13] Along with the increasing number of required AMS/RF components, the market demand for high-performance low-resource applications have further constrained these components to meet very stringent performance requirements, such as ultra-low-power, high dynamic-range, low-cost, or high-yield. However, AMS/RF designers are also severely constrained by the physical limitations of the underlying devices. Specifically, the desire to integrate AMS/RF functionalities onto the digital core introduces many complex physical-level issues such as voltage scaling, lower signal-to-noise-ratio, signal interference, and device mismatch.

Despite the increasing demand and complexity of AMS/RF systems, designer productivity in this domain have remained unchanged, relying mostly on manual design efforts. The need for new EDA tools and design methods is clear. Thus far, industry and academic efforts have mostly focused on automation of *circuit-level* design and *physical-level* layout; however, commercial adoption have been extremely limited. According to the 2010 Gartner Hype Report[14], analog automated synthesis and optimization tools introduced thus far have been under industry expectation. They are either not powerful enough to produce reliable designs that meet the demanding requirements of industrial applications or are too restrictive/complicated to use to foster mass adoption. The main reasons for the lack of adoption by design community can be broadly attributed to three types:

1. Limitation in scope of use: when the tool or method is only valid for specific types of topology, application, or technology. Either not generally applicable or lose significant accuracy or performance when wrongly applied. Rule-based systems are especially prone to this.

2. Loss of design insight: when the tool or method maps the design problem onto internal variables that are insignificant or incomprehensible to the designer, where designers lose valuable design insight and cannot understand or modify the output of the tool. Optimization tools that rely on numerical methods for manipulation and optimization are prone to this, which causes designer doubt when combined with lack of accuracy or generality from above.

3. More effort, minor gain: when the tool or method is significantly different from traditional electronic design training and tool flow used by the designer, significant retraining is required. However, when combine with the effects of 1 and 2, many designers and companies consider the return on investment for retraining to be of little or even negative value.

Instead of attempting to automate the low-level design processes, a compositional design methodology at the system-level can more efficiently overcome the complexity of modern AMS/RF integrated systems, without dramatically disrupting the current design practices of AMS/RF circuit designers, allowing smooth industry adoption. Specifically, a compositional design flow leverages design reuse, enables early-stage validation of design decisions, and reduces the number of design iterations, which minimizes overall NRE costs. Furthermore, as we reach the end of Moore's Law, the industry is transitioning to the "More than Moore" paradigm, which relies on innovative system integration and optimization techniques to meet performance demands. [15] Design methodologies that make decisions at the system-level would allow global tradeoffs to be evaluated among various system components, rather than focusing on localize optimizations of single components, achieving a greater degree of freedom during design space exploration.

However, integration and reuse of AMS/RF components at the system-level is non-trivial. In fact, analog intellectual-property (IP) components offered by most companies today are hard IP blocks, in GDS II format, where the physical sizing and placement of the transistors in the component are already pre-determined to a fixed parameter. Thus, the components are not configurable, and are very hard to reuse in most cases. Even in cases where these IP blocks can be used, their performances differ depending on different system environments and requires multiple design iterations between the IP vendors and the system architects to meet the system requirements. The problem stems from the fact that the functionality and performance of an analog component is closely tied to the physics of the underlying devices. Not only are they a function of the internal design parameters, such as transistor sizings and voltage biasing, but also a function of the interface conditions at the input and output ports. Even in the simple case of two cascaded analog circuits, performances of the composition cannot be generally obtained by directly cascading behavioral and performance models of the stand-alone components, since the behavior of the loading block substantially affects that of the driver. The problem of interface conditions during integration, under which hierarchical system compositions are legal, has not been rigorously addressed and mostly relies on the experience and manual efforts of the circuit designer. However, to overcome

the increasing complexity of modern AMS/RF design, a formalized approach must be introduced to enable fast and accurate performance estimation and validation of integrated AMS/RF systems based on pre-characterized component blocks. Furthermore, configurability of the component blocks must be retained at the system-level to ensure a high degree of flexibility during design space exploration, so that the optimal system can be reached to meet the demanding requirements of modern electronic applications.

1.2 Thesis Contributions and Organization

This dissertation introduces a compositional design methodology, which leverages the analog platform-based design (APBD) flow introduced in [16, 17] and assume-guarantee reasoning to guarantee correct system construction. The main contributions include:

- The definition of AMS/RF *contracts* for component composition and a set of necessary and sufficient conditions for composition *compatibility*, under which the functions and performances of the composed AMS/RF components in the integrated system are guaranteed to behave the same as those obtained from stand-alone characterization, within a specified error margin;
- A *design flow* for leveraging contracts in system construction using the APBD methodology is introduced;
- Application of the design flow for a *cascade* composition of a low-noise-amplifier with an integrated transmit/receive switch (TRLNA) and a down-converting mixer (MIXER) for UWB receiver applications;
- Application of the design flow for the *feedback* composition of an bi-quadratic low-pass Sallen-Key filter cell (SKCELL), consisting of a feed-forward differential-difference-amplifier (DDA) and a feedback second-order passive resistor-capacitor (RC) filter network;
- Application of the design flow for the specification, composition, and multi-level design-space exploration of the UWB receiver system for the Intelligent Tire application, consisting of subsystems (UWB RF-frontend and low-pass filter) constructed using previously characterized circuit components, to demonstrate hierarchical design refinement and application.

This dissertation is organized into six chapters. Chapter 2 provides the related background works for this dissertation, including an overview of the state-of-the-art analog EDA tools and methods, introduction to the the platform-based design framework, and history on the use of contracts for verification and design in other domains. In Chapter 3, contracts for analog composition will be formally defined, and incorporated into the APBD paradigm. The methodology is applied to the design and integration of an RF system, composed of a TR switch, LNA, and Mixer. In

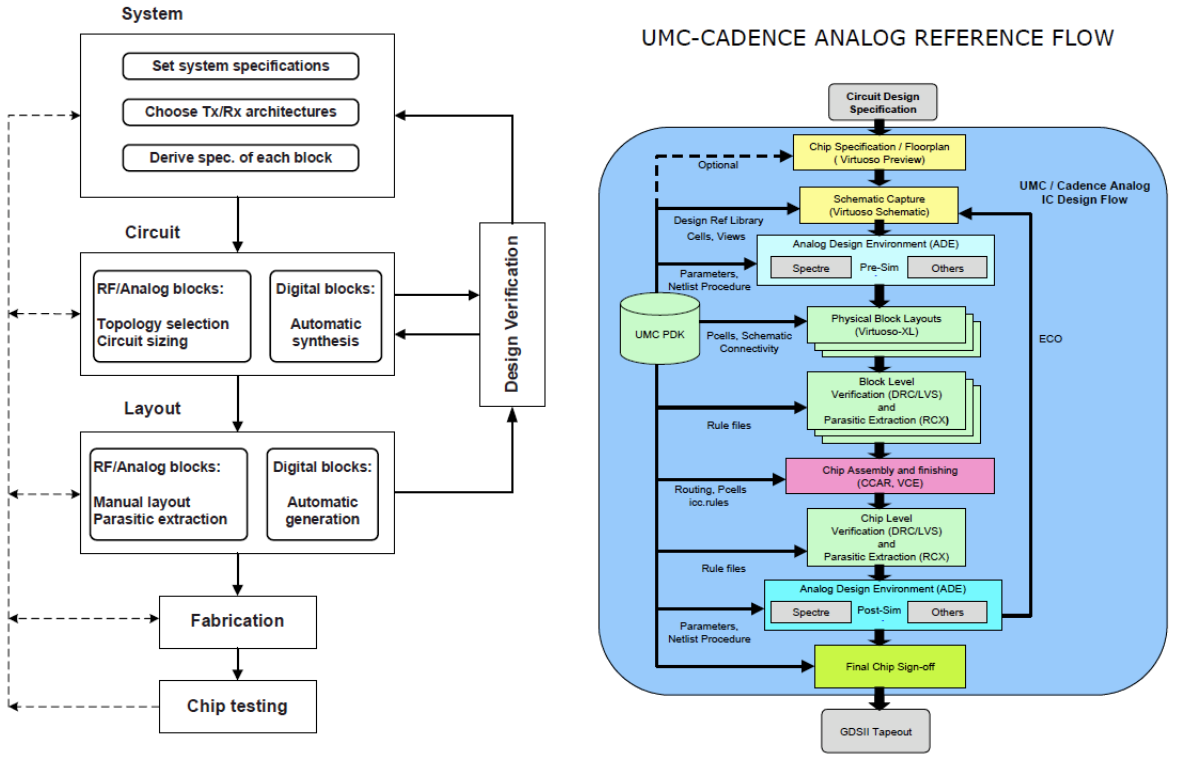
Chapter 4, a detailed study on the propagation of contracts across different abstraction layers is studied. Specifically, the concept of vertical contracts is discussed. Both horizontal and vertical contracts are demonstrated through a case study on the composition of an analog feedback network, the Sallen-Key bi-quadratic cell. In Chapter 5, a complete application of the design flow is demonstrated through the construction of the UWB receiver chain in the Intelligent Tire System, demonstrating multi-level hierarchical design exploration and composition. In Chapter 6, a summary and recommendations for future research directions is discussed.

Chapter 2

Background

Despite more than 25 years of active research and development in AMS EDA techniques and methods, analog design is still very much a knowledge-intensive and handcrafted process that require expert designers, supported only by a handful of commercial SPICE simulation tools and interactive transistor and layout-level design entry software. As illustrated in Figures 2.1a and 2.1b, modern analog design processes are mostly top-down, where each component is customly designed, optimized and verified locally based on a set system specifications and assumptions. There are many drawbacks to this approach:

- Difficult system-level tradeoffs and exploration: Components are individually designed based on pre-determined specifications. Since there is very little information about the physical performances of the components at the system-level, it is very difficult to fully explore the entire design space at the system-level and accurately perform tradeoffs among the performances of different components.
- Multiple design iterations among various design stages: Since specifications are determined with very little information of the available resources and performance feasibility of the components, considerable portion of the design cycle is devoted to iterating between specification engineering and design refinement at each stage of the design cycle.
- Difficult to simulate and validate the system pre-silicon: Since the abstraction of design is stagnated at the transistor-level, fully validating the system via pre-silicon simulation is extremely time consuming. Although there have been efforts [18, 19, 20] on abstracting mixed-signal simulation into a higher level of abstract, adoption have been slow.



(a) Traditional Transceiver Design Flow [21]

(b) UMC-Cadence Reference Analog Design Flow [22]

Figure 2.1: Reference State-of-the-Art Analog Design Flows

2.1 Design Tools

Majority of research efforts in analog EDA have been focused on automating specific stages in the traditional design flow, such as topology selection, circuit sizing, or automatic layout. In [1], a very comprehensive review of the major works in analog EDA over the past 25 years was presented, which is also illustrated in Figure 2.2. Here, the reviewed works were categorized into three abstraction levels: Physical, Electrical, Behavioral. Another way of interpreting this categorization is based on the tasks performed at each abstraction level, which can be drawn directly from Figure 2.1a, specifically:

1. Behavioral: Functional Partition, Architecture Selection, and Specification Derivation.
2. Electrical: Circuit Topology Selection and Sizing
3. Physical: Layout, Routing, and Parasitic Extraction

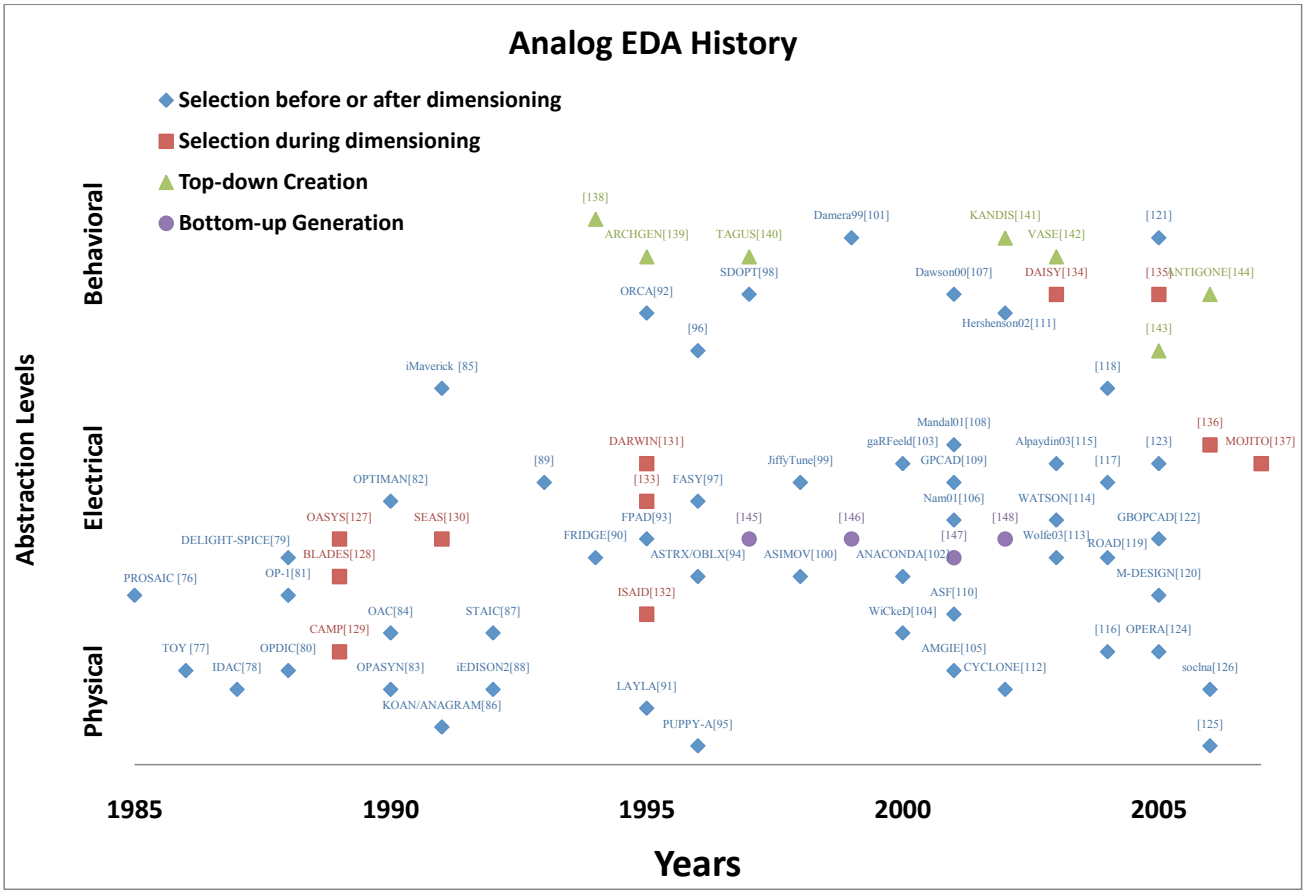


Figure 2.2: Review of analog EDA work in the past quarter-century by G. Gielen [1].

The design exploration strategies were classified into four types:

- *Architecture Selection before or after dimensioning*
  - Select topology or architecture first, then optimize paramters in selection, OR
  - Select multiple topologies or architectures, and optimize each of them. Select the best one.
- *Selection during dimensioning*
  - Design is incrementally modified based on a starting parameterized template, until optimal design is reached

- *Top-down creation*
  - Starting with a high-level description, the system is translated into internal representations and mapped onto basic architecture components. Components are then optimized, integrated, and validated.
- *Bottom-up generation*
  - Starting with a set of seed component, systems are modified, composed, and rearranged to meet given design specifications.,

Commercially, as observed in Figure 2.1b, the state-of-the-art analog design flow from [22] remains a heavily manual process. Recently, the use of parameterizable cells (PCells), which are pre-designed circuit or layout templates that may be parameterized, have been introduced to reduce designer effort and promote design reuse. However, the use of PCells in industry is still mostly limited to minor components and generally used only at the transistor and layout levels. Furthermore, PCells are only design templates and do not carry any information for circuit or system performance. They still need to be properly sized, simulated, and validated. Current commercially available PCell sizing tools include Cadence NeoCircuit and NeoCELL [23], which came out of research from CMU for stochastic simulation-based circuit sizing [24], as well as Titan ADX [25], which came out of research from Stanford for circuit sizing through geometric programming [26].

While many research works in analog EDA are quite powerful, their applicability and scope of use were limited, which prevented mass adoption of these tools in the designer community. Tools that leveraged the strategies of *selection before, during, or after dimensioning* require an initial set of template designs and rules which may not be widely available and must be created by designers from scratch, often in the context of the new tool, which are unfamiliar to designers. Tools that use the *top-down creation* strategy are generally limited to the technology-independent behavioral and macro-model levels, while the *bottom-up generation* tools were restricted to the electrical circuit level. There exists a clear gap between the system behavioral level and the electrical circuit level in analog design, which prevents the level of abstraction for AMS design from moving beyond the transistor level. Thus, many system-level issues discussed in Chapter 1 cannot be properly addressed within the current design flow. To address this gap in design, analog platform-based design (APBD) [16] was introduced as a recursive meet-in-the-middle design framework that can be applied to all levels of abstraction.

2.2 Analog Platform-based Design

Analog Platform-based Design (APBD) is a design methodology proposed in recent years [27, 21, 16, 28, 17, 29, 30] that adopts the platform-based design (PBD) paradigm [31, 32] into the analog domain. Fundamentally, platform-based design identifies design as a *meeting-in-the-middle* process (Figure 2.3), where successive top-down refinements of high-level specifications across

design layers are mapped onto bottom-up abstractions of potential implementations. The layers in design are supported by a set of *platforms*, which is a collection of abstracted views of low-level components and a set of composition rules. This library-based approach makes PBD is naturally amenable to design reuse.

The multi-view approach to design allows the problem to be partitioned and orthogonalized into concerns at various levels of abstraction and can incorporate all four types of design exploration strategy described in Section 2.1, while closing the gap between abstraction levels through appropriate mapping. Defining the proper levels of abstraction depends on the target application. Since PBD is a recursive process that can applied across many application levels [33, 34, 35, 36, 37, 38], it's not restricted to any single application, design-flow, or set of tools.

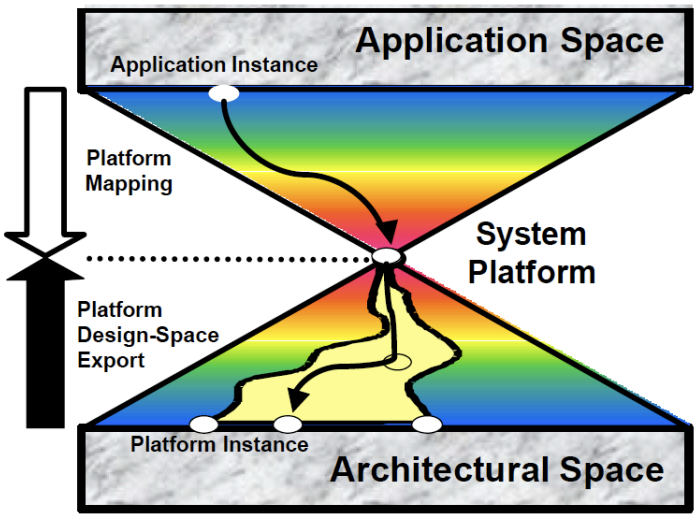


Figure 2.3: Each platform stack of PBD features a meeting-in-the-middle of system constraints and performance characterizations.

In APBD, each component is characterized by a behavioral model that represents the functionality of the component and a performance model that represent a set of feasible performances of the component and abstracts away unnecessary details. Through the use of machine learning techniques [28], continuous circuit-level performance feasibility regions can be extrapolated from a set of discrete transistor-level electrical simulation simulation samples. An m-dimensional support-vector machine is used as a classifier to tightly estimate the feasible performance space of interest for a circuit block (Figure 2.4), where m is the number of performance parameters for the circuit.

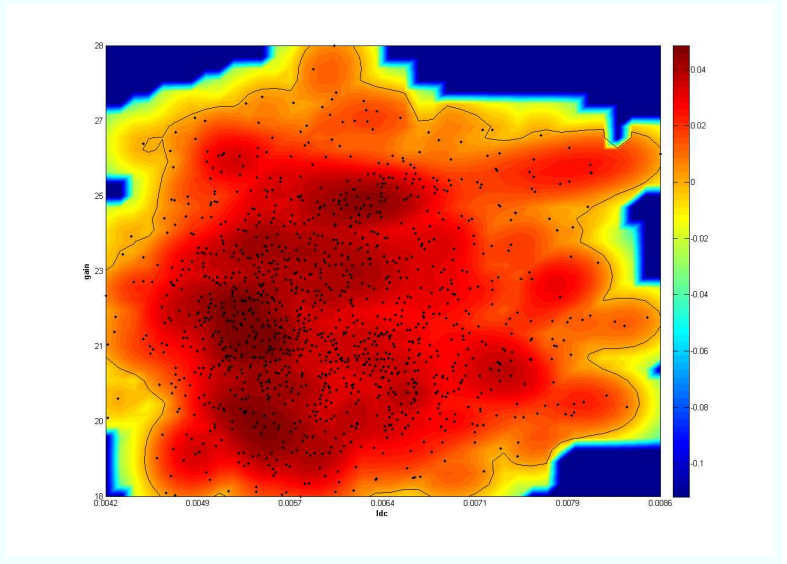


Figure 2.4: SVM classifiers help separate feasible and infeasible performance spaces of a component.

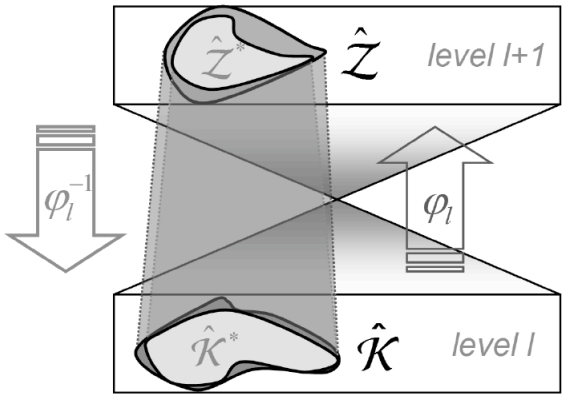


Figure 2.5: Platform abstraction process.

A design is obtained by composing components of the platform into a platform instance, as shown in Figure 2.5, where the outputs of level l (κ) are used as configurations to obtain system performances at level $l+1$ (ζ). In this framework, new designs can be assembled quickly from a library of pre-designed and pre-characterized components, giving the highest priority to design reuse, correct assembly of components, and an efficient flow from specification to implementation.

Since design decisions are made at the system level, APBD can locate globally optimal design solutions by evaluating system tradeoff across all components, instead of just using locally optimized designs of each individual component. In addition, platforms permits hierarchical design space exploration, which progressively reduce the number of design variables and separate design concerns.

However, the problem of defining correct composition rules for components of a platform library has not been rigorously addressed. Correct composition guarantees implementation feasibility and performance estimation accuracy. Indeed, performances of analog components are strongly dependent on interfaces with other components and loading conditions. In previous APBD case studies, the interface conditions were hand-tuned and fixed to constants during performance characterization. In [16] the introduction of ad-hoc interconnection blocks is suggested to accurately model interface effects in analog circuits. However, the provided guidelines can be hardly generalized, basically consisting in case-by-case topology-related heuristics which require non negligible effort for the designer to build the models. To formulate a more rigorous composition approach, this work proposes the use of contract-based compositional reasoning.

2.3 Contract-based Design

Contracts are fundamentally rooted in compositional *assume-guarantee* reasoning: if given a set of defined assumptions, a component or model can provide or guarantee a set of outputs, then the assume/guarantee sets form contracts. The essence of contracts is *divide-and-conquer*, where assume-guarantee (AG) reasoning reduces design and verification complexity by decomposing system-level tasks into manageable subproblems at the component-level under a set of assumptions. System properties are inferred or proved based on component properties that are guaranteed under the given assumptions. The first formal use of AG reasoning can be traced to [39], which leveraged assume-guarantee relations on input and output message traces of individual processes to prove correctness of the overall constructed communication network. In [40], a similar logic style is applied to infer system properties for concurrent software programs. In [41, 42, 43], contracts are applied to reduced complexity in formal verification of large systems, which would otherwise be intractable. More recently, contracts have been extended into the design digital and software systems, where component models are either inherently embedded or annotated with contracts and enforced during design such that the constructed system is *correct-by-construction*. In [44, 45], *assumption/guarantee* is used to model the interfaces of components, which can be used to support incremental refinement of systems and independent implementability.

The core of contract-based design (CBD) [46, 47] is a set of assume-guarantee relationships between the environment (e.g. interfaces) and the component (e.g. performances). In [47], a meta-theory of of contracts is presented which define the basic properties of contracts, including consistency and compatibility. In addition, contracts are casted both horizontally and vertically, depending on the source of the contract assumptions and abstraction level of the guaranteeing

components. During composition, a legal connection must satisfy the assumptions of all components involved to guarantee the correct system behavior. However, thus far, application of contracts have resided in the digital domain with discrete components that, in general, have a fixed number of static input/output requirements (e.g. legal states or timing constraint) and guarantees. In this dissertation, I apply the meta-theory of contracts from [47] to the analog domain to construct systems based on component composition, where assumption conditions (e.g. load impedance, input voltage level) are continuously variable within a specified range.

Unlike digital components, analog component models must capture a wide and continuous range of assumption values in order to provide rich models that can be used for multiple applications and system environments. Composition is only allowed if the contract assumptions of all interconnected components are simultaneously satisfied. In fact, assume-guarantee relationships have always been intuitively used by analog designers. However, in most cases, only a few fixed interface assumptions are considered in an ad-hoc manner and are rarely captured into an executable model. Within APBD, *validity laws* need to be defined for a component to be useful. However, thus far, *validity laws* have been defined on an ad-hoc basis that can hardly be applied to a general design flow. In contrast, contracts allow rigorous definitions and analysis of the validity of compositions. By considering a wide continuous range of assumptions, contracts allow each component to be reused in multiple application domains since it provides a rich feasibility space that the system designer can explore.

Chapter 3

Analog Composition Using Contracts

Efficient system design increasingly relies on hierarchical design-space exploration and compositional methods to shorten time-to-market, leverage design reuse, and minimize design costs. However, the hierarchical approach tend to lose in accuracy when propagating information across design levels. Consequently, component reuse and system integration are very difficult tasks in all domains: digital, analog, software, and hardware. Integration of analog components is even more cumbersome because circuit performances and behaviors are not only functions of internal design parameters, such as transistor sizings and voltage biasing, but also functions of the external environment, such as interface loading or common-mode input voltage. Even in the simple case of two analog circuits in cascade, performances of the composition cannot be generally obtained by directly cascading behavioral and performance models of the stand-alone components, since the behavior of the loading block substantially affects that of the driver, and vice versa. This tight coupling of circuit behaviors and their environment make component-reuse and performance estimation of the composite system an extremely hard task. Currently, there exists no general solution to this problem, so analog system integration commonly rely on *ad-hoc* solutions, heavily dependent on the designers' experiences and insights at both the circuit and the system levels.

3.1 Analog Contracts

As discussed in Chapter 2, Analog Platform-based Design (APBD) is a natural framework to adopt to promote design reuse. However, there lacks a mechanism to ensure the validity of composition. I build upon the APBD methodology by exploiting *contracts* to enforce *correct-by-construction* system composition. Contracts intuitively capture the thought process of a designer, who aims at *guaranteeing* circuit performance only under specific *assumptions* (e.g. loading and dynamic

range). By formally incorporating contracts into the design flow, this approach allows the detection and correct composition of compatible components in a given library, which ensures that the design decisions made at the system-level, based on a global objective, account for the compositional compatibility of the underlying components. Let's first begin by defining the *Analog Platforms*, which is used to represent components at all levels of abstraction in APBD.

Definition 1 *An Analog Platform (AP) consists of:*

- *a set of input variables $u \in \mathcal{U}$, a set of output (and performance) variables $y \in \mathcal{Y}$, a set of internal variables $x \in \mathcal{X}$ (including state variables), a set of configuration parameters $\kappa \in \mathcal{K}$;*
- *a behavioral model $\mathcal{F}(u, y, x, \kappa) = 0$, which implicitly represents the behavior of the component; in general, $\mathcal{F}(.) = 0$ is a set of integro- differential equations uniquely determining y and x given u and κ;*
- *a performance feasibility model:*

$$\mathcal{P}(y, x) = 1 \Leftrightarrow \exists \kappa, u, (y, x) = \phi_y(\kappa, u) \tag{3.1}$$

  Let $\phi_y(\kappa, u)$ denote the map that computes the performance y corresponding to particular values of u and κ by solving the behavioral model. The feasible performance set is then the set described by the relation (3.1). $\mathcal{P}(y, x)$ is an indicator function denoting the feasible performance space of the component. ϕ_y maybe be either a functional or electrical simulator such as Simulink® [48] or SPICE [49].
- *a set of assumptions: $\mathcal{A}(u, y, x, \kappa, \delta) \leq 0$, which is a set of constraints on the variables of the AP for which both behavioral and performance models are guaranteed to be* valid *within a set of tolerable margins $\delta \in \mathcal{D}$.*

Here, we replace *validity rules* in the original definition of AP from [16] with a set of *assumptions*, which is more aligned with the use of contracts. Assumptions of an AP may either be *static* or *dynamic*. Static assumptions are uniquely singular conditions on a set of AP variables, and generally denotes conditions (e.g. supply voltage) that do not change and must be satisfied for the AP to be instantiated, such as:

$$\begin{aligned} V_{DD} &= 1.5V \\ V_{SS} &= 0V \\ L_{min} &= 0.18\mu m \end{aligned}$$

Dynamic assumptions refer to conditions (e.g. loading impedance) that varies depending on the system architecture or external environments. Dynamic assumptions specifies a range of values for the assumed variable for which the AP may be used, such as:

$$R_{source} = r \quad \forall \ r \in [100, 10000]\Omega$$

In this example, R_{source} is assumed to be variable within a continuous range between 100 and 10000 Ω; however, dynamic assumptions may also be variable within a discrete set, such as in variable-mode components. Since dynamic assumptions are variable, the guaranteed performance of the AP should be able to vary with the assumption. For example, an amplifier may provide a gain of 10 dB if the loading impedance is 1000 Ω or a gain of 15 dB if the loading is 5000 Ω. The AP should capture both the varying range of the loading assumption, as well as the corresponding set of gain performances. Clearly, static assumptions are a special case of dynamic assumptions, and the decision for which variables to statically assume versus dynamically assume depends on the component designer and the degree of freedom allowed for the external user of the component. Dynamic assumptions allow greater flexibility for the system environment in which an AP component can be instantiated, which promotes component reuse. A completely statically-assumed component is essentially hard IP components with no flexibility, whereas a completely dynamically-assumed component is configurable, but would require more efforts during characterization to guarantee accurate model outputs. An AP model is *valid* when all static assumptions are satisfied, and for dynamic assumptions, there exists a value for the assumed variables that lies within the assumed range, while still satisfying the performance feasibility model of the AP. A valid AP guarantees that its behavioral and performance models correspond to the actual circuit implementation within a tolerance dictated by δ.

Given a set of AP components at level *l*, systems can be composed and represented as APs at level *l+1*, which themselves are components for a higher-level. *Contracts* ensure component validity during composition and are defined as follows.

Definition 2 *The contract* ***C*** *for an AP component is a set of assume/guarantee tuples* $\{c_i = (a_i^\delta, g_i) : i = 1, \ldots, N\}$ *where for each* i*,*

1. a_i^δ *is the set of vectors for the assumed variables of the AP,* $(u,y,x,\kappa) \in \mathcal{U}\times\mathcal{Y}\times\mathcal{X}\times\mathcal{K}$*, that satisfies all assumption conditions described in* $\mathcal{A}$ *of the AP within the margins* δ*.*
2. g_i *is the set of all* $(y,x) \in \mathcal{Y}\times\mathcal{X}$*, such that* $a_i^\delta \models \mathcal{A} \implies \mathcal{P}(g_i) = 1$*, that is, if* a_i^δ *satisfies* $\mathcal{A}$*, then* g_i *is contained in the AP performance feasibility model. Clearly,* g_i *can be also computed by directly executing the* behavioral model *under the condition dictated by* a_i^δ *if* $a_i^\delta \models \mathcal{A}$*.*

The role of the contract is to identify the correct performance regions guaranteed by each component during composition. As different assumptions are realized during composition, corresponding component performance guarantees are utilized to configure the system to meet the given specifications. This ensures that for various system configurations, the AP models correctly represent the true behavior of the circuit within the system environment. In particular, only *compatible* components can be composed to construct a higher level AP. More formally,

Definition 3 *Two AP components A and B, with contracts $\boldsymbol{C}_A$ and $\boldsymbol{C}_B$, are* compatible*, i.e. $A \bowtie B$,* iff *there exists ports $p_A \in \mathcal{U}_A \cup \mathcal{Y}_A$, $p_B \in \mathcal{U}_B \cup \mathcal{Y}_B$, and contract tuples $(a_A, g_A) \in \boldsymbol{C}_A$ and $(a_B, g_B) \in \boldsymbol{C}_B$ such that*

$$\mathscr{P}_{p_A}(a_A) \cap \mathscr{P}_{p_B}(g_B) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{p_B}(a_B) \cap \mathscr{P}_{p_A}(g_A) \neq \emptyset$$

where $\mathscr{P}_p(\mathcal{S})$ is the (orthogonal) projection of the set $\mathcal{S}$ onto the subspace of the variables related to port p.

Informally, two AP components are compatible if there exists a set of values for the variables on the shared ports that satisfy the assumptions of *both* components and obeys their behavioral and performance feasibility models. Two AP components are then *composable*, i.e. either the composition $A \otimes B$ or $B \otimes A$ forms a valid AP, when $A \bowtie B$ holds. There are no restrictions for the ports p_A and p_B in Definition 3 to be output and input ports, respectively.

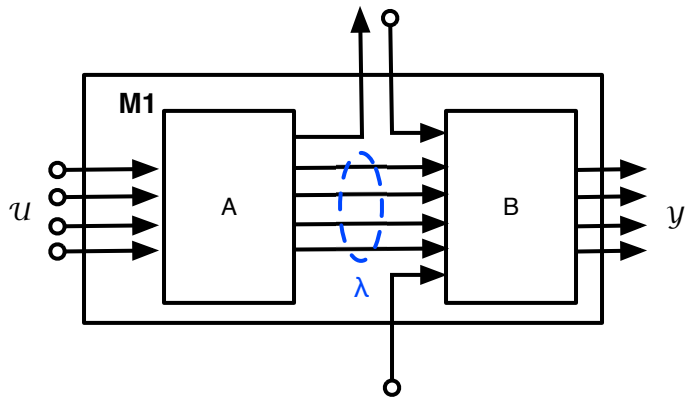


Figure 3.1: A compose B on shared variables λ.

The set of all compatible component configurations form the *compatible regions* for the APs during composition, which are the *valid* search spaces to explore while ensuring that APs remain valid after system construction. It should be noted that the compatible region is not a simple intersection of the assumption space of one component with the guarantee space of another for the interconnected variables. To see this, I introduce a simple toy example in Figure 3.1, where component A is composed with component B on the variables λ to form the system M1. Figure 3.1 shows the contract spaces of A and B, projected into the assumption and guarantee spaces on the shared λ variables, $\mathscr{P}_\lambda(a_A)$, $\mathscr{P}_\lambda(a_B)$ and $\mathscr{P}_\lambda(g_A)$, $\mathscr{P}_\lambda(g_B)$ respectively. In general, only a subset of the assumption space of A, $\mathscr{P}_\lambda(a_A)$, is satisfied by the performance space of B, $\mathscr{P}_\lambda(g_B)$, related to the variables λ. The reduced assumption space that is satisfied upon composition directly corresponds to a reduced performance space of A, denoted with $\mathcal{G}'_A$. Similarly for B, $\mathscr{P}_\lambda(g_B)$ is reduced to $\mathcal{G}'_B$,

due to the reduced assumption space of B. The reduced performances are recursively intersected and reduced with the reduced assumption spaces, until a set of fixed-point configuration is reached, which form the compatible regions between A and B. Thus, in general, a single intersection of the assumption and performance spaces of two composing elements do not form the compatible regions. In the example of Figure 3.1, the compatible region are the design spaces corresponding to the projections $\mathcal{G}''_B = \mathscr{P}_\lambda(a_A) \cap \mathcal{G}'_B$ and $\mathcal{G}''_A = \mathscr{P}_\lambda(a_B) \cap \mathcal{G}'_A$.

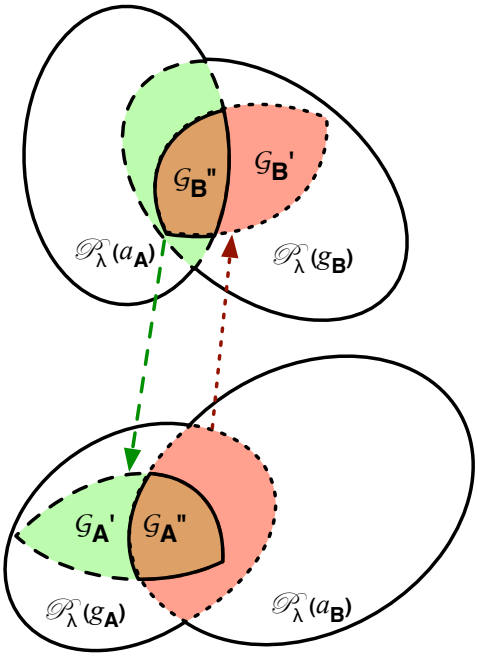


Figure 3.2: Projections of the contracts of A and B onto assumptions and performance guarantees of the shared variables λ during composition. Composition can only occur between design instances that simultaneously satisfy assumptions of both components involved, which is confined to the *compatible regions* $\mathcal{G}''_A$ and $\mathcal{G}''_B$.

3.1.1 Composition

Contracts allow AP components to be reliably composed, while preserving correct system behavior and performance estimation accuracy. Without loss of generality, this section formalizes the composition of compatible components *A* and *B* at platform level *l*, to generate *C* as an AP component at level *l*+*1*, i.e. $C = A \otimes B$. The variables of *C* are:

- a set of internal variables $x_C \in \mathcal{X}_C$,
- a set of input variables $u_C \in \mathcal{U}_C$,

- a set of output (and performances) $y_C \in \mathcal{Y}_C$,
- a set of configuration parameters $\kappa_C \in \mathcal{K}_C = \{\mathcal{G}_A; \mathcal{G}_B\}$, where $\mathcal{G}_A, \mathcal{G}_B$ are the set of guaranteed and compatible performance outputs of A and B in composition.

Some level *l* component variables may change roles in composition, e.g. an input variable may become an internal variable, depending on the application. Composition is allowed when components are *compatible*. A composition is characterized by the interconnect variables, which are shared variables when composing components, and the contracts that are defined when the composition is indeed possible. Formally, a connection is establishing a pairwise equality between variables and performances (e.g. $p_A = p_B$) of two components. Interconnect relations are generally a set of linear equalities. The set of interconnected (shared) variables between *A* and $Bisdenotedas\lambda_{AB}$.

The system-level behavioral model, $\mathcal{F}_C$ is $\mathcal{F}_A \times \mathcal{F}_B$ conjoined with the interconnect relations, similar to process behavior composition used in tagged-signal model [50], where variables are mapped onto an extended space containing variables of both components, and the behavioral models of the components are evaluated on the set of extended variables. The interested reader should refer to [47] for the complete formulation on the meta-theory of *contract-based design*. The output and internal variables of the system, $(y_C, x_C) \in \mathcal{Y}_C \times \mathcal{X}_C$, are obtained through a map $\phi_C(\kappa_C, u_C)$, where the configurations of the system κ_C are extracted from the set of guaranteed and compatible outputs of lower level components, $y_A \in \mathcal{G}_A, y_B \in \mathcal{G}_B$. ϕ_C is the performance map from platform *l* to platform *l+1*, which computes the values of (y_C, x_C) by solving the system-level behavioral model $\mathcal{F}_C$ for particular values of κ_C, u_C. The performance feasiblity model, $\mathcal{P}_C$, is defined afresh based on ϕ_C. The assumption set of the composed system, $\mathcal{A}_C$, include component-level assumptions, which remain open in composition (i.e. unrelated to the interconnected variables). More formally:

$$\begin{aligned} &\forall\, (a_{Ai}, g_{Ai}) \in \mathbf{C}_A, \forall\, (a_{Bj}, g_{Bj}) \in \mathbf{C}_B \;\; i = 1 \ldots n, j = 1 \ldots m \\ &a_{Cij} = \{a_{Ai} \;\; a_{Bj}\} \;\text{ if} \qquad (3.2) \\ &\quad \mathscr{P}_\lambda(a_{Ai}) \cap \mathscr{P}_\lambda(g_{Bj}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_\lambda(a_{Bj}) \cap \mathscr{P}_\lambda(g_{Ai}) \neq \emptyset \\ &g_{Cij} = \{\phi_C(g_{Ai}, g_{Bj})\}\; \forall g_{Ai} \in \mathcal{G}_A, g_{Bj} \in \mathcal{G}_B \qquad (3.3) \end{aligned}$$

where n and m are the total number of contract tuples for *A* and *B*, respectively. g_{Ai} and g_{Bj} are compatible and guaranteed performances of *A* and *B*, respectively. Together, (3.2) and (3.3) state that design instances of *A* and *B* can compose under the shared variables λ if they are compatible. The set of all (a_C, g_C) tuples form the contract of the composition, $\mathbf{C}_C$.

At the system-level (i.e. level $l + 1$), the behavioral model, $\mathcal{F}_C$, may also be defined anew by the system-level designer, configured using the outputs of underlying components, to either simplify the model (e.g. RF cascade equations) or to refine the model to isolate the behaviors of interest. Additionally, new assumptions may be introduced at the system-level, on both the outside environment, as well as internally, on the components that make up the system. System-level assumptions vary depending on application and are referred to as *vertical assumptions*. Their role

and how they are propagated top-down to constraints at the component-level is discussed more in detail in Chapter 4.

Contracts allow design decisions made at a raised level of abstraction to remain accurate with respect to physical implementation since feasibility and performance estimation accuracy are preserved in composition. The accuracy of the performance model of the composed system is only dependent on the accuracy of ϕ_C and the performance models of the components, and no additional errors are introduced due to false assumptions or miscommunication between design teams.

3.1.2 Properties of Composition

To deal with complex system construction, hierarchical design approaches must be leveraged. I list here some properties that contract-based analog composition exhibits in hierarchy. First, analog composition is not *commutative*. In fact, besides the trivial cases, where *A* and *B* perform different functions, which are not interchangeable, in [51], it is demonstrated that, even in cascaded filter designs, the order of cells is key in accurately estimating the total system noise figure and linearity. Contract-based analog composition does preserve the *associative* property, in the sense that the evaluation order of system composition, for the same set of interconnection relations, does not affect the final design space that is explored, if the behavior of the components are associative. This property enables extra degrees of freedom in hierarchical design exploration. The interconnection relations, are decided a priori by the system designers, and are independent of the order in which composition is evaluated, as shown in Figure 3.3 for the case of three components.

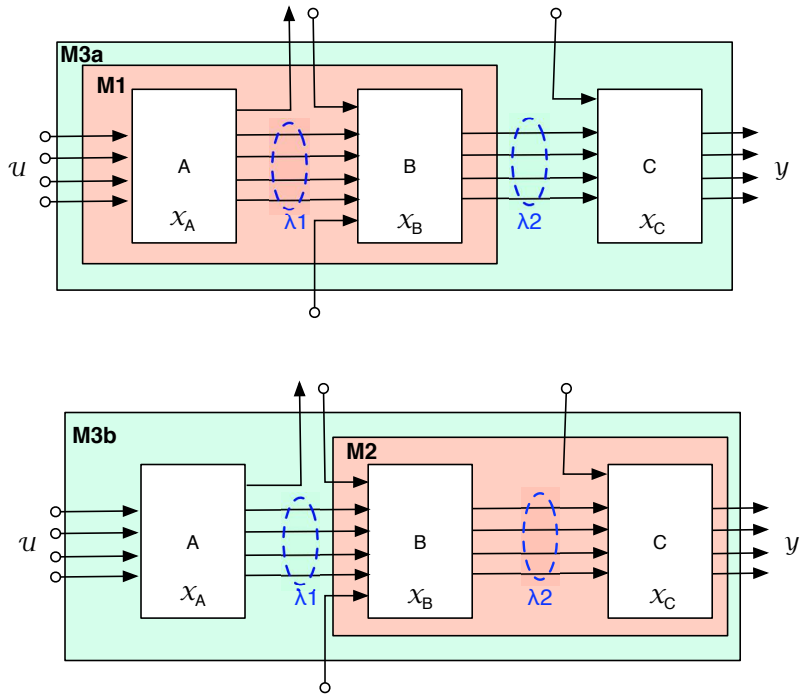


Figure 3.3: Composition Associativity

Theorem 1 *Analog composition using contracts preserves associativity: In hierarchical composition, the set of compatible component designs among all components, for a given set of interconnections, $\lambda = \{\lambda_1, \lambda_2 ... \lambda_n\}$, is independent of the evaluation order of system composition if the behavioral models of the components are associative.*

Proof 1 *Given components A, B, and C, as in Figure 3.3, the contract of M1 = A⊗B is given as:*

$$\begin{aligned} &\mathbf{C}_{M1}: \ \{a_{M1ij} = (a_{Ai} \ \ a_{Bj}), g_{M1ij} = \{\phi_{M1}(g_{Ai}, g_{Bj})\} \ \text{if} \\ &\mathscr{P}_{\lambda_1}(a_{Ai}) \cap \mathscr{P}_{\lambda_1}(g_{Bj}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_1}(a_{Bj}) \cap \mathscr{P}_{\lambda_1}(g_{Ai}) \neq \emptyset \\ &\forall \ (a_{Ai}, g_{Ai}) \in \mathbf{C}_A, \forall \ (a_{Bj}, g_{Bj}) \in \mathbf{C}_B \end{aligned} \tag{3.4}$$

where λ_1 is set of connections between A and B, and g_{Ai}, g_{Bj} are compatible component outputs of A and B, respectively, given λ_1. Similarly, the contract of M2 = B⊗C is

$$\begin{aligned} &\mathbf{C}_{M2}: \ \{a_{M2jk} = (a_{Bj} \ \ a_{Ck}), g_{M2jk} = \{\phi_{M2}(g_{Bj}, g_{Ck})\} \ \text{if} \\ &\mathscr{P}_{\lambda_2}(a_{Bj}) \cap \mathscr{P}_{\lambda_2}(g_{Ck}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_2}(a_{Ck}) \cap \mathscr{P}_{\lambda_2}(g_{Bj}) \neq \emptyset \\ &\forall \ (a_{Bj}, g_{Bj}) \in \mathbf{C}_B, \forall \ (a_{Ck}, g_{Ck}) \in \mathbf{C}_C \end{aligned} \tag{3.5}$$

where λ_2 is set of connections between B and C. The contract of M3a = M1⊗C is

$$\begin{aligned}&\mathbf{C}_{M3a}: \ \{a_{M3a_{mk}} = (a_{M1m} \ \ a_{Ck}), g_{M3a_{mk}} = \{\phi_{M3a}(g_{M1m}, g_{Ck})\} \text{ if}\\ &\mathscr{P}_{\lambda_2}(a_{M1m}) \cap \mathscr{P}_{\lambda_2}(g_{Ck}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_2}(a_{Ck}) \cap \mathscr{P}_{\lambda_2}(g_{M1m}) \neq \emptyset\\ &\forall\,(a_{M1m}, g_{M1m}) \in \mathbf{C}_{M1}, \forall\,(a_{Ck}, g_{Ck}) \in \mathbf{C}_C\end{aligned} \tag{3.6}$$

Substituting (3.4) into (3.6), I obtain

$$\begin{aligned}&\mathbf{C}_{M3a}: \ \{a_{M3a_{ijk}} = (a_{Ai} \ \ a_{Bj} \ \ a_{Ck}), g_{M3a_{ijk}} = \{\phi_{M3a}(\phi_{M1}(g_{Ai}, g_{Bj}), g_{Ck})\} \text{ if}\\ &\mathscr{P}_{\lambda_1}(a_{Ai}) \cap \mathscr{P}_{\lambda_1}(g_{Bj}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_1}(a_{Bj}) \cap \mathscr{P}_{\lambda_1}(g_{Ai}) \neq \emptyset \quad \text{and}\\ &\mathscr{P}_{\lambda_2}(a_{Bj}) \cap \mathscr{P}_{\lambda_2}(g_{Ck}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_2}(a_{Ck}) \cap \mathscr{P}_{\lambda_2}(g_{Bj}) \neq \emptyset\\ &\forall\,(a_{Ai}, g_{Ai}) \in \mathbf{C}_A, \forall\,(a_{Bj}, g_{Bj}) \in \mathbf{C}_B, \forall\,(a_{Ck}, g_{Ck}) \in \mathbf{C}_C\end{aligned} \tag{3.7}$$

Similarly, contract assumptions of M3b = A⊗ M2 is

$$\begin{aligned}&\mathbf{C}_{M3B}: \ \{a_{M3b_{il}} = (a_{Ai} \ \ a_{M2l}), g_{M3b_{il}} = \{\phi_{M3b}(g_{Ai}, g_{M2l})\} \text{ if}\\ &\mathscr{P}_{\lambda_1}(a_{Ai}) \cap \mathscr{P}_{\lambda_1}(g_{M2l}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_1}(a_{M2l}) \cap \mathscr{P}_{\lambda_1}(g_{Ai}) \neq \emptyset\\ &\forall\,(a_{Ai}, g_{Ai}) \in \mathbf{C}_A, \forall\,(a_{M2l}, g_{M2l}) \in \mathbf{C}_{M2}\end{aligned} \tag{3.8}$$

Substituting (3.5) into (3.8), I obtain

$$\begin{aligned}&\mathbf{C}_{M3b}: \ \{a_{M3b_{ijk}} = (a_{Ai} \ \ a_{Bj} \ \ a_{Ck}), g_{M3b_{ijk}} = \{\phi_{M3b}(g_{Ai}, \phi_{M2}(g_{Bj}, g_{Ck}))\} \text{ if}\\ &\mathscr{P}_{\lambda_1}(a_{Ai}) \cap \mathscr{P}_{\lambda_1}(g_{Bj}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_1}(a_{Bj}) \cap \mathscr{P}_{\lambda_1}(g_{Ai}) \neq \emptyset \quad \text{and}\\ &\mathscr{P}_{\lambda_2}(a_{Bj}) \cap \mathscr{P}_{\lambda_2}(g_{Ck}) \neq \emptyset \quad \text{and} \quad \mathscr{P}_{\lambda_2}(a_{Ck}) \cap \mathscr{P}_{\lambda_2}(g_{Bj}) \neq \emptyset\\ &\forall\,(a_{Ai}, g_{Ai}) \in \mathbf{C}_A, \forall\,(a_{Bj}, g_{Bj}) \in \mathbf{C}_B, \forall\,(a_{Ck}, g_{Ck}) \in \mathbf{C}_C\end{aligned} \tag{3.9}$$

Thus, contract (3.7) of $M3a$:(A⊗B)⊗C and contract (3.9) $M3b$:A⊗(B⊗C), are identical if the mapping of $\phi_{M1}, \phi_{M2}, \phi_{M3a}$ and ϕ_{M3b} (i.e. the behavioral model of the components) are associative. Therefore, contract-based analog composition preserves associativity. □

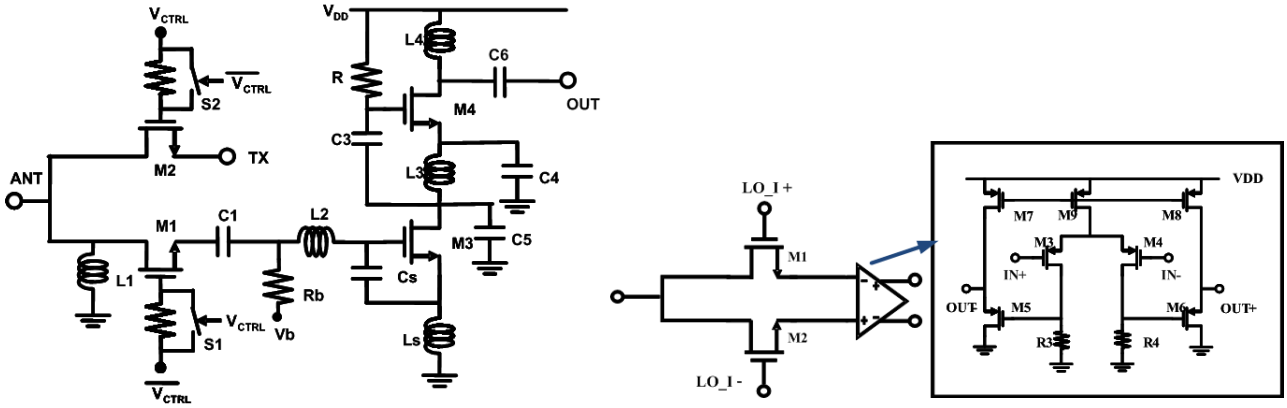
3.2 Case Study

To concretely illustrate contract-based analog composition, an ultra-wide band receiver RF front-end system, based on the architecture in [29], is composed bottom-up from two pre-designed RF blocks, characterized as circuit-level APs. Contracts are used to smoothly integrate the system. The compatible component performances are mapped to a simple system behavioral model (i.e. RF cascade equations) and optimized at the system-level to meet system specification constraints.

The authors of [29] showed that APBD can be used to automatically optimize RF system design; however, there was a lack of composition rules to account for different possible loading conditions on the components of the system. Thus, to produce accurate and reliable results, fixed interface conditions were enforced by adding an interface buffer to shield the components from the environment. However, this not only adds to the performance overhead of the system, but it also limits the design space of the components, making them inflexible and hard to reuse in different system settings. By using contracts, I can remove the interface buffer between the LNA and mixer and still enforce correct system composition.

3.2.1 UWB RF Components

As shown in Figure 3.4a, the RF front-end includes two main building blocks.



(a) TRLNA Schematic

(b) Mixer Schematic

Figure 3.4: Circuit Schematic

The first block, TRLNA, (Figure 3.4a) consists of the T/R switch (M_1 and M_2), the wideband (3.1 - 4.8 GHz) input matching network (L_1, L_2, L_S, and C_S), and the LNA, which features a stagger tuning technique to achieve gain flatness over the wide band. The second block, Mixer, (Figure 3.4b) includes a passive mixer (M_1 and M_2) and a low-noise buffer amplifier (M_3-M_8) to boost mixer gain.

3.2.2 Contracts

The process technology used for the TRLNA and mixer blocks was 0.13μm 1.2V technology. The input signals were assumed to have a bandwidth of 500MHz centered at 3.96 GHz. Thus, I define

the following static assumptions, $\mathcal{A}_s$, for both components on the system environment.

- Lmin = 0.13 μm
- Vdd = 1.2V
- BW = 500 MHz
- Fc = 3.96 GHz

I define interface assumptions, which are dynamic, for the output of the TRLNA and the input of the mixer. The interface assumptions, $\mathcal{A}^{\delta}_{TRLNA}$, of the TRLNA restricts the equivalent loading impedance as follows:

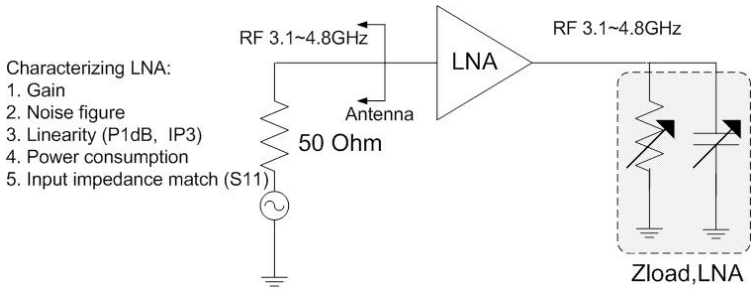
$$\begin{aligned} &\mathcal{A}_{TRLNA} = \{a^1_{TRLNA} : Rload = r, a^2_{TRLNA} : Cload = c\}; \\ &r \in [85, 520]\Omega, c \in [0.03, 0.25] \text{ pF} \end{aligned} \tag{3.10}$$

where $Rload$ and $Cload$ are the assumed loading resistance and capacitance at the output of the TRLNA. The mixer interface assumption on the source impedance is:

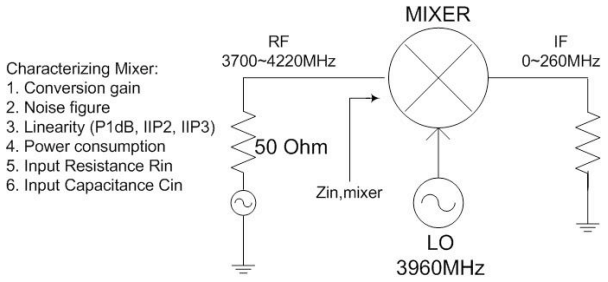
$$\mathcal{A}_{Mixer} = \{a^1_{Mixer} : 20\Omega \leq Rsource \leq 1000\Omega, a^2_{Mixer} : Csource \leq 1 \text{ nF}\} \tag{3.11}$$

where $Rsource$ and $Csource$ are the input source resistance and capacitance loadings. The interface assumptions of the TRLNA component are dynamic assumptions, in that the guaranteed performance of the TRLNA cell varies dynamically with different interface conditions. The mixer interface assumptions are singular conditions (i.e. only one assumption relation for each assumed variable), and therefore static. In this case, the source impedance of the mixer did not dramatically affect the output performance (e.g. noise figure), within the specified range, and the outputs were within the specified δ of 1%.

To characterize the feasible performance regions of each component, I first generate a sample set by running a series of batch simulation. Figure 3.5 shows the basic test bench for component characterization.



(a) TRLNA Schematic



(b) Mixer Schematic

Figure 3.5: Circuit Characterization Testbench

Then, SVM [28] is used to characterize the sample points into a continuous region, which forms the feasible performance space, $\mathcal{P}$, used in system-level optimization. 1338 configurations of the TRLNA were simulated, using uniformly randomized RC loads within the assumed range. 2132 configurations of the mixer were simulated, using a source impedance of 50Ω. Since the mixer block just had one set of dynamic assumptions, I do not need to vary the source impedance during characterization. On the contrary, dynamic assumptions of the TRLNA directly correspond to the guaranteed performance, that is varied loading conditions causes varied performances. During performance characterization, this phenomenon can be reflected by including dynamic assumptions as part of the performance vector. Appending dynamic assumptions increase the dimensions of the SVM by d, where d is the number of columns of the dynamic assumption. In the case of the TRLNA, d is 2 for *Rload* and *Cload*.

The contracts of the two components are:

$$\mathbf{C_{TRLNA}} = \{[\mathcal{A}_s;\ \ a^1_{TRLNA_i};\ \ a^2_{TRLNA_i})], \zeta_{TRLNA_i}\} \quad (3.12)$$
$$\text{s.t. } \mathcal{P}_{TRLNA}(\zeta_{TRLNA_i}) = 1;$$
$$\mathbf{C_{Mixer}} = \{[\mathcal{A}_s;\ \ a^1_{Mixer_i};\ \ a^1_{Mixer_i})], \zeta_{Mixer_i}\} \quad (3.13)$$
$$\text{s.t. } \mathcal{P}_{Mixer}(\zeta_{Mixer_i}) = 1$$

where ζs are the subsets of the characterized performance space that are guaranteed under the given assumptions. The elements of performance vectors of ζ_{TRLNA} and ζ_{Mixer}, are shown in Table 3.1 .

	1	2	3	4	5
ζ_{TRLNA}	NF	gain	S11	power	IIP3
ζ_{Mixer}	Rin	Cin	gain	power	NF
	6	7	8	9	10
ζ_{TRLNA}	IIP2	P1dB	Zout	Rload	Cload
ζ_{Mixer}	IIP3	IIP2	P1dB	Rsource	Csource

Table 3.1: Elements of performance vectors ζ_{TRLNA} and ζ_{Mixer}

3.2.3 Composition and Optimization

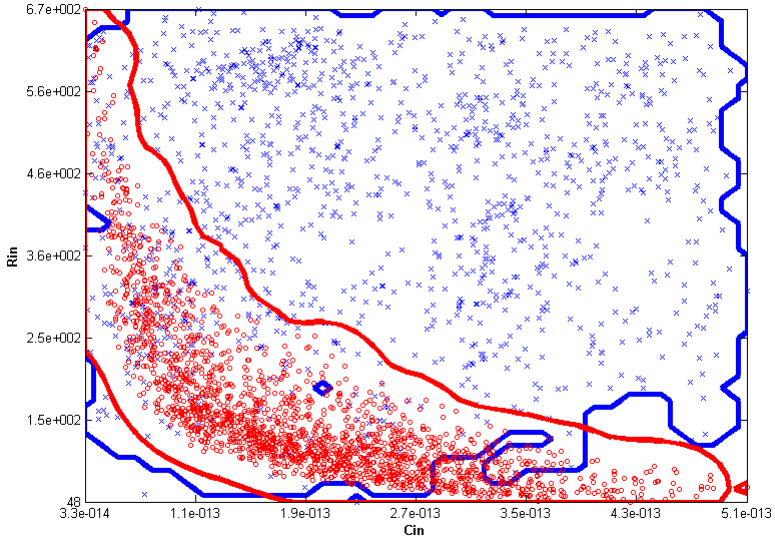


Figure 3.6: Intersection of TRLNA RC loading assumptions (blue) and mixer input RC performances (red).

Before composition, component compatibility conditions must be checked.

$$\mathscr{P}_\lambda(a_{TRLNA}) \cap \mathscr{P}_\lambda(\zeta_{Mixer}) \neq \emptyset \quad \text{and} \tag{3.14}$$

$$\mathscr{P}_\lambda(a_{Mixer}) \cap \mathscr{P}_\lambda(\zeta_{TRLNA}) \neq \emptyset \tag{3.15}$$

where λ is the interconnection between TRLNA and mixer. In addition, the static assumptions on the system environment from the two components must agree. In this case, the TRLNA and Mixer block had identical static system assumptions during characterization. However, the interface assumptions must be checked for compatibility during composition.

The mixer interface assumption, in this case, is a static condition and can be checked a-priori to isolate all TRLNA designs in the characterized design space that met the assumption. For this case, all of the characterized TRLNA performance space satisfied (3.11), so in this case, (3.15) is always true in this composition.

However, the interface assumptions of the TRLNA are dynamic and can not be evaluated prior to optimization. In general, when dynamic assumptions are involved, automatic construction of the

compatible region is computationally expensive, since it must be recursively constructed until a set of fixed-points are found. Thus, instead of explicitly constructing the compatible region, I enforce (3.14) in the optimization problem formulation as constraints. In this case, I constrain the search space, so that the interface assumptions of the TRLNA, $\zeta_{TRLNA}(9, 10)$, is equal to the actual input resistance and capacitance of the mixer, characterized by $\zeta_{mixer}(1, 2)$.

To avoid unnecessary calls to the optimization engine, I can prune the search space by first estimating the existence of a compatible region through checking for the bounding-box intersection between the assumptions of the TRLNA and the guarantees of the mixer, and vice versa. If this preliminary compatibility check passes, I frame the contract conditions as constraints in the system-level optimization problem, which will bound the search space to within the compatible regions. By inspection, Figure 3.6 shows that (3.14) indeed is true, similarly (3.15) also holds.

Now,the system-level optimization problem can be formulated. In this particular case, I aim to minimize power consumption and noise of the RF front-end while meeting system constraints on IIP3, Gain, and NF. The system level optimization problem is defined as:

$$
\begin{aligned}
& min_{\zeta_{TRLNA},\zeta_{Mixer}} \quad \omega_1 \cdot power + \omega_2 \cdot \Theta_1(NF) \qquad (3.16)\\
& \text{s.t.} \begin{cases}
\left.\begin{array}{l} IIP3 \geq -35dBm \\ Gain \geq 18dB \\ NF \leq 5dB \end{array}\right] & \text{System Specifications} \\
\left.\begin{array}{l} \mathcal{P}_{TRLNA}(\zeta_{TRLNA}) = 1 \\ \mathcal{P}_{mixer}(\zeta_{mixer}) = 1 \end{array}\right] & \text{Feasibility Constraints} \\
\zeta_{TRLNA}(9, 10) = \zeta_{mixer}(1, 2) & \text{Contract Constraints}
\end{cases}
\end{aligned}
$$

where ω_i are weight coefficients and Θ is a penalty function. System performances (power, NF, gain, and IIP3) are calculated from the ζ_{TRLNA} and ζ_{mixer} using simple cascade equations.

$\mathcal{P}_{TRLNA}$ and $\mathcal{P}_{mixer}$ are SVM classifiers to bound ζ_{TRLNA} and ζ_{mixer} in the feasible performance space. Furthermore, a legal composition must satisfy contract constraints between elements $\zeta_{TRLNA}(9, 10)$, representing the assumed loading resistance and capacitance of the TRLNA, and $\zeta_{Mixer}(1, 2)$, representing the actual input resistance and capacitance that loads the TRLNA during composition. As in [29], I employ adaptive simulated annealing [52] as the optimization engine, modified such that the stochastic search is within the feasibility regions given by $\mathcal{P}$, as well as compatible regions of composition.

3.3 Results

Optimization finished after evaluating 20730 design instances of the TRLNA and mixer, 7186 of which satisfied contract assumptions and formed *legal* compositions. The total optimization time took 21 minutes on a 3.16 GHz Intel Core2 Duo Workstation for the optimization formulation of (3.16). Since I used equality constraints for the TRLNA assumptions, extra optimization time were

required for the simulated annealing engine to find satisfactory points. Less stringent inequality constraints may also be used for assumptions to speed up optimization, but at the cost of less accurate performance estimations.

Optimization results are verified by comparing between estimated system performances and transistor-level simulations from SpectreRF. I use a nearest-neighbor (NN) search to map the optimization results onto a set of configuration vectors saved from the performance characterization phase.

Perf. @3.96 GHz	TRLNA Opt.	Mixer Opt.	TRLNA NN	Mixer NN	System Estimated	System Simulation	Ref. [29]
NF(dB)	3.49	13.3	3.49	13.2	3.67	3.89	4.36
Power Gain(dB)	23.5	-3.57	23.5	-3.34	19.9	18.74	17.2
IIP3(dBm)	-13.7	-7.37	-13.7	-7.26	-30.9	-27.96	-22.5
P1dB(dBm)	-21.2	-14.7	-21.2	-14.8	-38.3	-38.85	-34.6
Power(mW)	5.39	1.62	5.39	1.67	7.07	**7.07**	**10.8**

Table 3.2: Optimization and simulation results

Table 3.2 shows the optimized results, NN performance parameters, estimated system performance, and simulated results of the RF front-end, based on NN configurations. The estimated system performance, based on simple cascade equations, closely matched simulation results without any function fitting or adjustments, showing that contracts preserved model accuracy at the system level after composition. The quality of the optimized system is investigated by comparing with the reference system [29], which was optimized without using contracts and required an intermediate buffer to fix interface conditions. By removing the interface buffer, the system power consumption reduced by 34.5%, while improving system noise figure and gain performances. The linearity of our optimized system is slightly degraded in comparison. The main reason is because higher-order effects for the interface loading between the TRLNA and the Mixer were not accounted for by the first-order RC-pair assumptions. A more detailed assumption model can help improve the accuracy of the final system, but at the cost of more effort during component characterization stage. It should be noted that the reported voltage gain from [29] was 29.2 dB, based on a high-impedance output loading (1MΩ in parallel with 1pF) on the mixer during characterization. For a fair comparison, I normalized the mixer output load in [29] to 50Ω, which is the mixer output loading used in our characterization environment, and found that the equivalent power gain to be 17.2 dB.

To show flexibility of the methodology in design reuse, Table 3.3 shows the optimization results for various cost functions, and is compared with the absolute bounds of the given models, and the original reference design. Note that the bounds of the performances may not be realizable due to composition contract and feasiblity constraints, but they show how close the results were to the optimal bounds.

	Min Power	Min NF	Min f(Power, IIP3)	Min f(Power,NF)	Bounds	Ref. [29]
NF(dB)	4.2	**3.4**	4.8	3.7	3.23	5.05
Gain(dB)	**21.2**	**21.2**	16.8	19.9	28	17.2
IIP3(dBm)	-30	-33	**-25**	-30	-23	-22.5
Power(mW)	**6.8**	8.1	**6.8**	7.07	6.6	10.8

Table 3.3: Optimization results for different cost functions

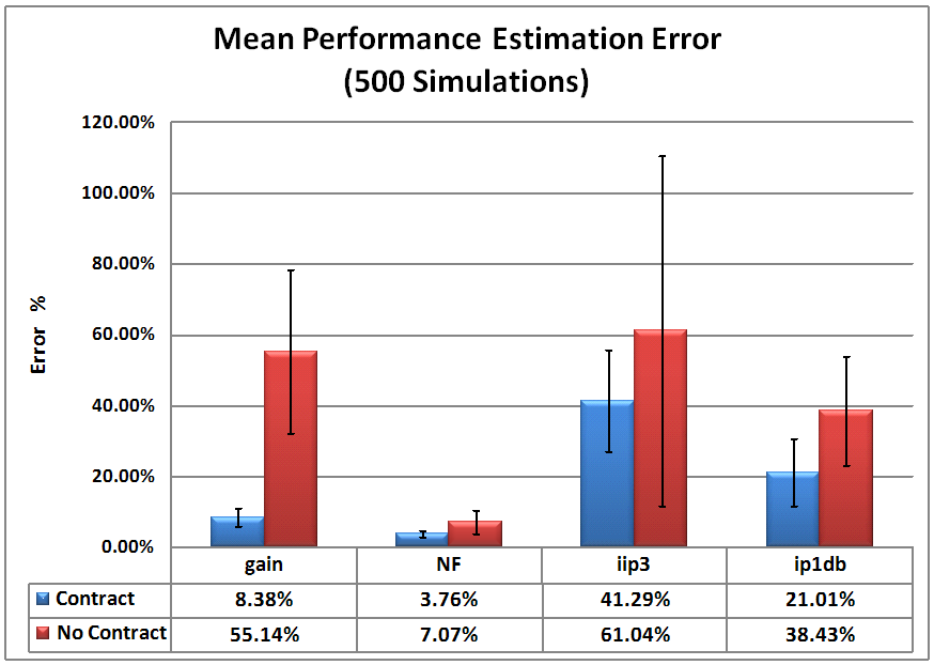


Figure 3.7: Contract-based composition yielded lower average estimation error for all performances, as well as a lower standard deviation, as represented by the error bars.

To further examine improvements in accuracy, I compare the errors between systems composed with and without contract conditions. Figure 3.7 shows the errors between estimated performances and simulation results, averaged over 500 individual system compositions, for both *contract* and *no contract* cases. For all performance parameters, contract-based composition resulted in significantly lower average estimation error, as well as lower standard deviation on the error. Errors on the linearity performance parameters remained relatively high because the interface models considered in this case study were linear RC models and may not reflect higher-order effects (e.g. parasitic capacitance) introduced at the mixer input. However, this linear approximation of the interface shows that contracts indeed help in maintain model accuracy at high abstraction levels.

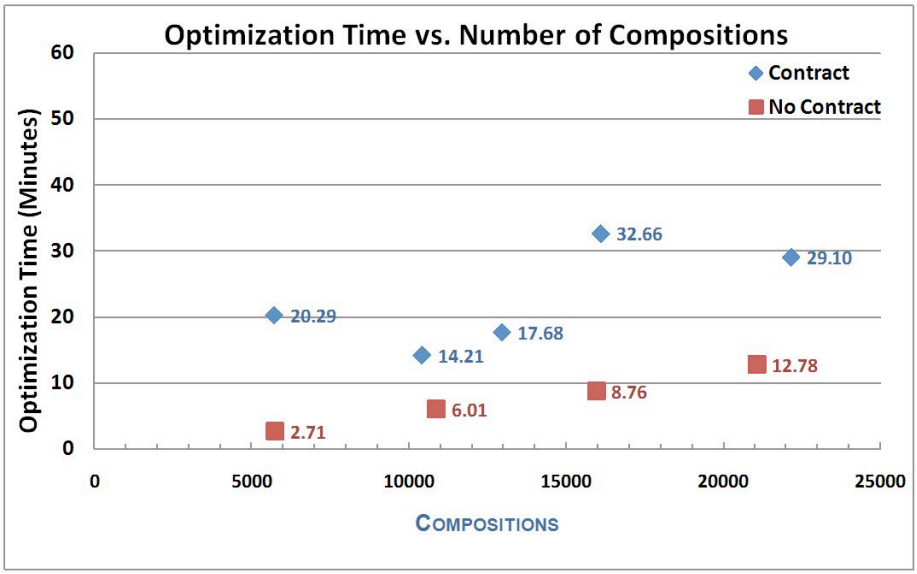


Figure 3.8: Optimization runtime comparison for composition with and without contracts.

The improved accuracy of optimization results does come at a cost in optimization runtime, since more constraints must be satisfied. Figure 3.8 shows some differences in runtime for different number of compositions evaluated. In general, the optimization runtime depends heavily on the structure of the characterized performance and whether the compatible regions can be easily located. For the AP components used in this study, the average increase in runtime for using contracts was about four times when compared with optimization without contract constraints. But this is still within reason, with a maximum of around 30 minutes, when compared with manual integration efforts.

Contract-based composition enables correct-by-construction systems in APBD through methodical characterization, detection, and integration of compatible components from a given library of circuit topologies. Without contracts, direct composition of pre-characterized components is highly unreliable, forcing designers to rely on either manual integration or extra circuitry/design cost to ”match” components. By leveraging assume/guarantee reasoning, independently characterized components account for loading effects introduced by the system environment, and help isolate the system-level optimization space within the valid implementation region (i.e. feasible and compatible). In this chapter, I examined the role of contracts when constructing systems in a bottom-up fashion, and showed how level l component contracts are propagated into contracts for components at level $l+1$. The work in this chapter is published in [53]. However, APBD is recursive design process featuring a meet-in-the-middle approach, where bottom-up characterizations meet with system specifications propagated in a top-down fashion. Similarly, in the top-down process, there exist assumptions by the system designers on the underlying components that make up the system. In the following chapter, the propagation of contracts and mapping of vertical contracts onto the underlying components as constraints is examined.

Chapter 4

Vertical Propagation of Contracts

In the previous chapter, contract-based composition enabled the correct behavior of analog IPs to be preserved after integration into the system; however, correct component behavior is not sufficient, in general, to guarantee correct system behavior. APBD is a meet-in-the-middle process, where systems are not only constructed bottom-up from a library of component, but are also subject to top-down constraint mapping. Designers often make assumptions by leveraging knowledge about the system architecture, which may not always be anticipated *a priori* or enforced at the component-level. Thus, *vertical assumptions* on the underlying components need to be accounted for and propagated onto the component level, as constraints, to drive the *refinement* of the desired specification into a correct implementation. The set of assume-guarantee tuples based are vertical assumptions are referred to as *vertical contracts*.

In this chapter, I complete the incorporation of contracts into the entire APBD flow, with a special focus on the introduction of *vertical contracts* and the contract propagation process. The final generated system are valid with respect to the compatibility conditions the components, as well as sufficiently satisfies the behavioral requirements of the system architect. Moreover, I introduce a projection-based optimization heuristic to efficiently explore the *system-level guarantee* space. *System-level guarantees* are generated by evaluating the system behavioral model, upon enforcing all horizontal and vertical contracts in the system. *System-level contracts* are formed from the set of system-level assume/guarantee tuples and can be used to correctly build systems by hierarchical composition. As an example, the composition of an analog feedback systems is studied and applied to the construction of a Sallen-Key biquadratic cell for UWB applications. Simulation results show that when filters are constructed by enforcing both horizontal and vertical contracts, they closely match the desired behaviors, with an average error reduction of 10% for the base-band gain and 60% for the filter bandwidth.

4.1 Contract Propagation

4.1.1 Design Flow

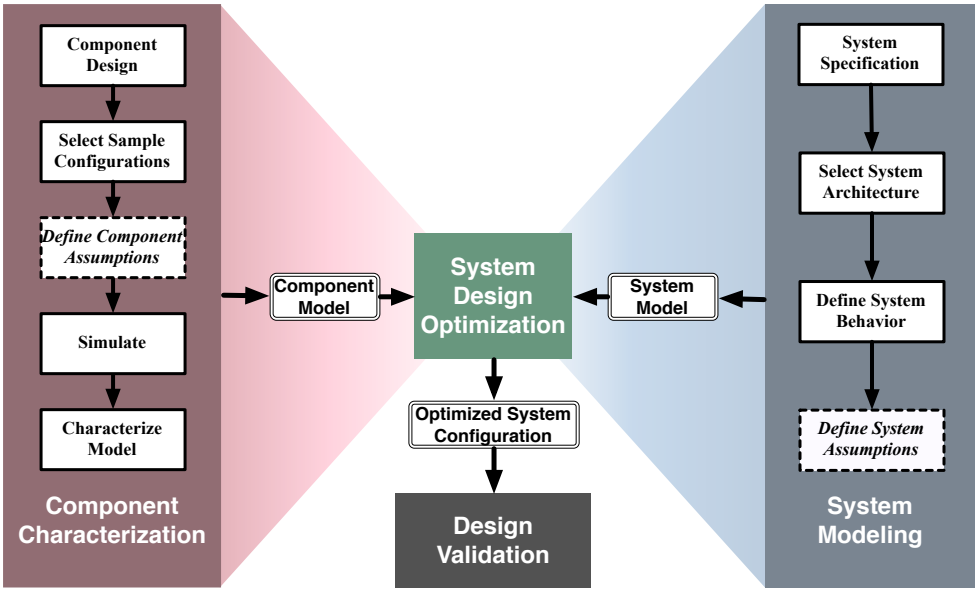


Figure 4.1: APBD Design Flow

Figure 4.1 illustrates the APBD flow with the incorporation of *assumption definition* used for *analog contracts*. Component design and characterization is completely orthogonalized from system specification and architectural design. AP components are built bottom-up to provide component models to the system-level optimization engine. On the other side, system constraints capturing the desired specification are propagated top-down, possibly associated with more abstract system-level behavioral models. The optimization phase leverages information from both the system and the component levels to evaluate global tradeoffs among components, while respecting the physical constraints dictated by the performance feasibility models of the AP components. The optimized results are then passed to a validation stage, where the design is verified against electrical simulations.

As introduced in Chapter 3, component contracts come into play when circuit designers make assumptions, from the bottom-up viewpoint, on the system environment when designing and characterizing a component. These interface contracts are *horizontally* enforced among components of the same abstraction level to ensure the compatibility of the contracts in composition. However, a valid composition alone is not sufficient to guarantee the desired system behavior. There may also exist a set of assumptions made by system designers from the top-down viewpoint. Correspondingly, the assume/guarantee tuple formed from this viewpoint are referred to as *vertical*

contracts.

4.1.2 Vertical Contracts

Similar to component assumptions made on the system environment, at the system-level, assumptions can be made, from the top-down viewpoint, on the underlying components that make up the system. These vertical assumptions may result from several modeling and architectural decisions made by system architects.

To begin, when an architecture is chosen for exploration, the system specification constraints are translated into constraints on the selected architecture and its underlying components. At this stage, the architect may make assumptions to bound the behavior of the chosen architecture to *capture the desired specifications*. These assumptions are not only on the external environment, but, more importantly, reflect the expected interaction between the components that make up the architecture. Secondly, although the performance feasibility information of the components may not be available at this point from bottom-up propagation, an experienced architect can already anticipate and account for possible undesired behaviors or non-dealities, such as unwanted signal paths or coupling. Thus, additional requirements can be made to *minimize* the impact of *undesired component behaviors* on the overall system. And as the system design is incrementally refined, more knowledge about the system architecture is gained, so additional assumptions are accumulated to bound the system behavior into the desired region. Lastly, non-ideal system behaviors in heterogeneous systems can be very difficult to model or computationally expensive to simulate. A clear tradeoff exists between the number of effects accounted for in a model and its computational complexity. Therefore, assumptions might also be needed to *reduce the complexity* of the system macro-model used for high-level simulation and design exploration, which otherwise may be too computationally expensive to evaluate or too complex to offer intuitive insights.

As a result, several assumptions are aggregated incrementally during the system-level specification refinement process. These assumptions are defined as *vertical assumptions*, and I represent them as a set A_S in Figure 4.2. A_S is the set of vectors $(u_S,y_S,x_S,\kappa_S) \in \mathcal{U}_S \times \mathcal{Y}_S \times \mathcal{X}_S \times \mathcal{K}_S$, that satisfies the vertical assumption relations within system margins δ_S, where u_S and y_S are the system input and output variables, x_S are the system internal variables and κ_S denotes the system configurations. The internal assumptions on the underlying components need to be propagated top-down onto the component-level as constraints, so that the final constructed system not only respect the expectations of the component designers, but also satisfies the required system behavior dictated by the system architects. Table 4.1 summarizes the four different types of *strong assumptions*, as defined in [47], which are assumptions that must be satisfied to complete valid system construction, that may occur in analog systems design. *Weak assumptions* may also exist in a system, where assumptions are not required to be satisfied and are simply discarded if not met. In analog system construction, we care most about strong assumptions.

Horizontal Static	***Horizontal Dynamic***
Vertical Static	***Vertical Dynamic***

Table 4.1: Types of Assumptions

4.1.3 Propagation

By propagating vertical assumptions down to the component level, I provide sufficient conditions for an implementation to adhere to the desired specification. In this section, I investigate how vertical assumptions can be transformed into component-level constraints, and how system guarantees are generated upon enforcing the vertical assumptions onto the underlying composition.

In APBD, the final design is obtained via mapping of the desired specification onto an implementation space made up of the pre-characterized AP components [17]. Mapping is cast as an optimization problem, where a set of performance metrics and quality factors are optimized over a space constrained by both system requirements and component feasibility constraints. Therefore, to ensure that correct systems are constructed, A_S, shown in Figure 4.2, the optimization formulation should include the effect of vertical contracts by vertically propagating A_S onto the components as constraints and intersected with the compatible composition space, as dictated by the pre-exisiting "horizontal" component contracts.

Let A_C be the union of the assumption spaces for all components in composition, and, similarly, G_C be the union of all guarantee sets. In composition, let A'_C and G'_C be the *compatible* assume/guarantee tuples based on Definition 3. G'_C now represent the set of all feasible performance guarantees of the composition under the corresponding assumptions in A'_C. However, the expected set of behavior, under the assumption set A_S, at the system-level may be independently defined by the system architects. A_S should be projected onto the component-level, where it generates an additional assumption set A'_S, in which the vertical contract assumptions are represented using component-level parameters. Since simply satisfying the compatibility conditions of the component-level contracts A'_C is not, in general, sufficent to satisfy A'_S. A'_C needs to be intersected with A'_S and only configurations in $A''_C = A'_C \cap A'_S$, will guarantee both a valid composition and the desired system behavior. $G''_C \subseteq G'_C$ is the set of guaranteed behavior of the composed system under the assumptions A''_C. By projecting back A''_C and G''_C up to the system-level, I generate the new *system-level contract* as the tuple (A''_S,G_S) where A''_S and G_S are obtained from A''_C and G''_C, respectively, after projection through the system-level performance map ϕ_{sys}. The set of systems represented by system contracts necessarily obeys vertical contracts made by the system architect, as well as ensure the component-level horizontal contracts defined by the circuit designers are compatible, giving a correct system agreed by all parties. The newly generated system-level contract can then be used for compositions at higher abstraction levels thus enabling hierarchical

system construction.

As an example, in Section 4.2.1, we derive vertical contracts on a simple analog linear system in feedback and show how they are propagated to constrain system design exploration within the desired design space. In Section 4.1.4, A projection heuristic is proposed to efficiently sample from the spaces A''_C and G''_C to optimize the design and minimize the cost function defined for the set G_S.

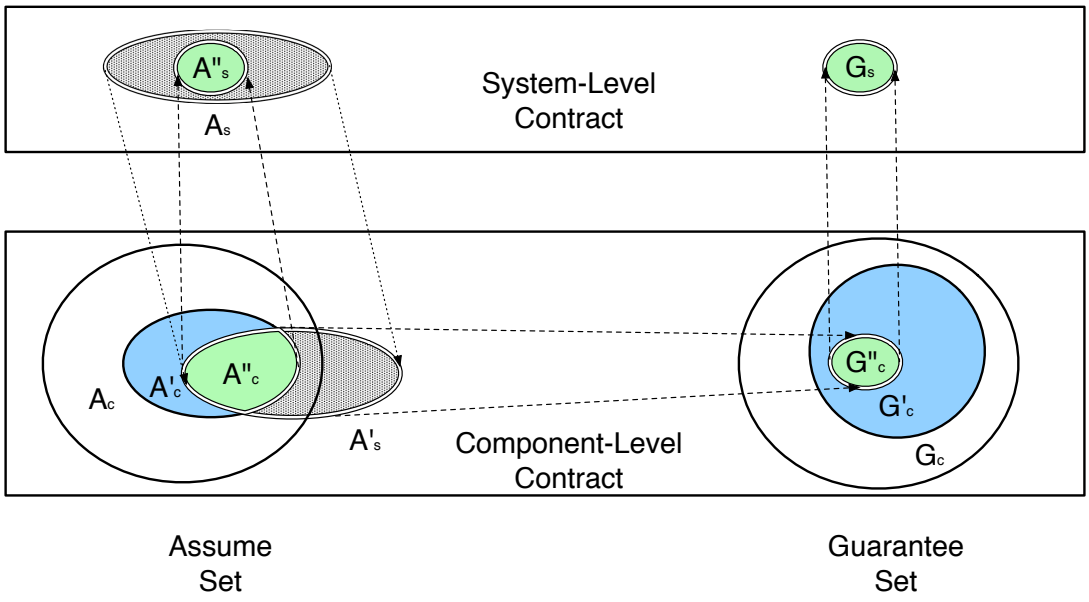


Figure 4.2: Vertical Propagation of System-level Contracts

4.1.4 System Optimization

Algorithm 1 Optimization of contract-composed systems.

1: **Given** A connected to f on shared variables λ
2: **Input** AP_A, AP_f, ϕ_{Sys}, $Spec$, $\mathcal{A}_\mathcal{C}$;
3: **Output** $u_C, y_C, x_C, \kappa_C, cost_{min}$;
4: Initialize variables;
5: **while** step $<$ MAX AND cost $>$ THRESHOLD **do**
6: **while** $\mathcal{A}_A(\lambda 2, \lambda 1) > 0$ AND $\mathcal{A}_f(\lambda 1, \lambda 2) > 0$ AND $\mathcal{A}_C|\lambda 1, \lambda 2 > 0$ **do**
7: $\lambda_1 \leftarrow$ pick_assume($\mathcal{Y}_A|\lambda$, cost, step)
8: $\lambda_2 \leftarrow$ pick_assume($\mathcal{Y}_f|\lambda$, cost, step)
9: **end while**
10: $u_f|\lambda, y_A|\lambda \leftarrow \lambda_1$
11: $u_A|\lambda, y_f|\lambda \leftarrow \lambda_2$
12: $\mathcal{P}_{A_{proj}} \leftarrow$ project ($\mathcal{P}_A$) given $u_A|\lambda$, $y_A|\lambda$
13: $\mathcal{P}_{f_{proj}} \leftarrow$ project ($\mathcal{P}_f$) given $u_f|\lambda$, $y_f|\lambda$
14: $\mathcal{K}_C \leftarrow \{\mathcal{P}_{Aproj}, \mathcal{P}_{Aproj}\}$
15: **minimize** $cost_{y_C}$ given
$y_C \leftarrow \phi_{Sys}(u_C, y_C, x_C, \kappa_C \in \mathcal{K}_C)$ such that
$Spec(y_C) \leq 0$ satisfied
$\mathcal{A}_\mathcal{C} \leq 0$ satisfied
16: **end while**

The system design space is now a function of both compatibility conditions of component-level *horizontal contracts* and *vertical contracts* of the system model. These conditions ensure the validity of both component and system models; however, they make design optimization very challenging. As discussed Chapter 3, assume-guarantee reasoning is inherently circular, so the compatible region can only be represented through an implicit relationship and derived recursively until the set of all fixed-points that satisfy all assumptions are found, which, in general, can be computationally intractable. To overcome this problem, the optimization algorithm features a projection-based heuristic, as seen in Algorithm 1, which explores the valid design regions through stochastic sampling. Effectively, this is a three-step procedure:

- **Assume** - locate a compatible set of values satisfying all assumption in the outer loop (line 6-11)
- **Project** - for a given set of assumed values, project the design space into the guarantee set (line 12-14)
- **Optimize** - minimize the given cost function in the inner-loop within the projected guarantee set(line 15)

In Algorithm 1, the input APs are A and f at level l, and the output AP C is at level $l+1$. In addition, the system specification is also given, and ϕ_{Sys} is the behavioral model of C.

Subroutine $pick\_assume$ randomly samples values on the shared variables λ between A and f, within the range bounded by the outputs of the APs. To ensure a fair sampling of the *compatible region*, there must be multiple iterations of the outer-loop, where the compatible region is sampled using a stochastic schedule similar to the annealing schedule in the optimization loop. Notice that in this step, I also check if any vertical contract assumptions $\mathcal{A}_C$ is violated to avoid expensive optimization runs in the inner loop.

The subroutine $project$ projects the performance feasibility models of the APs onto the guarantee sets under the selected values on λ by setting equality relations in the classifier functions $\mathcal{P}_A$ and $\mathcal{P}_f$. The $project$ operation enforces the *component-level contracts*. This step also enforces component feasibility, since if the selected values from $pick\_assume$ can not be feasibly realized by the guarantee sets of those values, the projected space is empty. Within the projected guarantee space, all component models are compatible with respect to the given assumptions, so conventional optimization methods can be applied. Vertical assumptions on variables that have not been explicitly addressed in the (*pick_assume*) step are treated as constraints in the optimization problem. Effectively, this assume-project process partitions up the design space into horizontally compatible regions among the components, and optimization is performed on the project subspace under constraints from system specifications and vertical contracts from the system-level.

Specifically, for this implementation, I use adaptive simulated annealing [52] as the core optimization engine. For analog systems, the design space is, in general, a non-linear non-convex high-dimensional space, making optimization non-trivial and usually requires a general-form optimization solver. Other optimization techniques such as genetic optimization[54]) or mathematical programming[26] can also be used, with special consideration for either the data structure or mathematical form of the optimization problem.

4.2 Case Study

In this section, I apply both both horizontal and vertical contracts to an interesting case study: the composition of an analog feedback network, first in the general form, then applied to a specific design case, the Sallen-Key bi-quadratic cell.

4.2.1 Analog Feedback Systems

Analog feedback systems are extremely common for many applications that require control or synthesis of complex functions. (e.g. phase-lock-loops (PLL), sigma-delta modulator, voltage regulators, or filters.) An ideal feedback network, as shown in Figure 4.3, is composed of a feed-forward path A and a feedback path f, where A and f are linear and unidirectional. The transfer function of the ideal feedback system is:

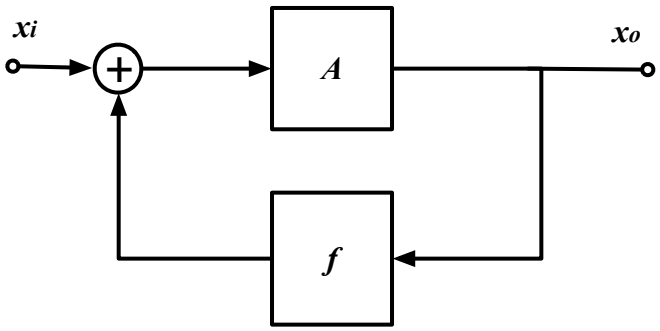


Figure 4.3: Ideal Feedback System

$$G_{ideal} = \frac{x_o}{x_i} = \frac{A}{1 - Af}. \tag{4.1}$$

Equation 4.1 represents the reference equations for any designer of a linear feedaback system.

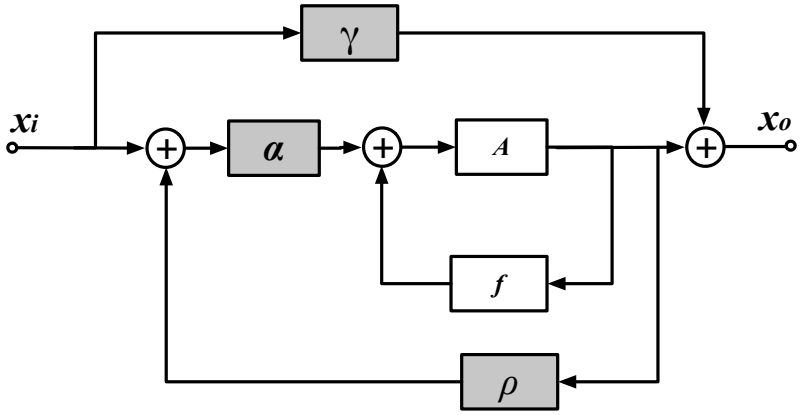


Figure 4.4: Real Analog Feedback System

However, real analog feedback systems are made of active and passive components that are neither linear nor unidirectional. Figure 4.4 shows a more realistic representation of the system behavior, where α is unintended signal attenuation, and γ is the unwanted feed-forward path between input and output while ρ represents the unwanted signal path from output to input.

From Figure 4.4, the system transfer function becomes

$$G_{real} = \frac{\alpha A}{1 - A(f + \alpha\rho)} + \gamma \tag{4.2}$$

.

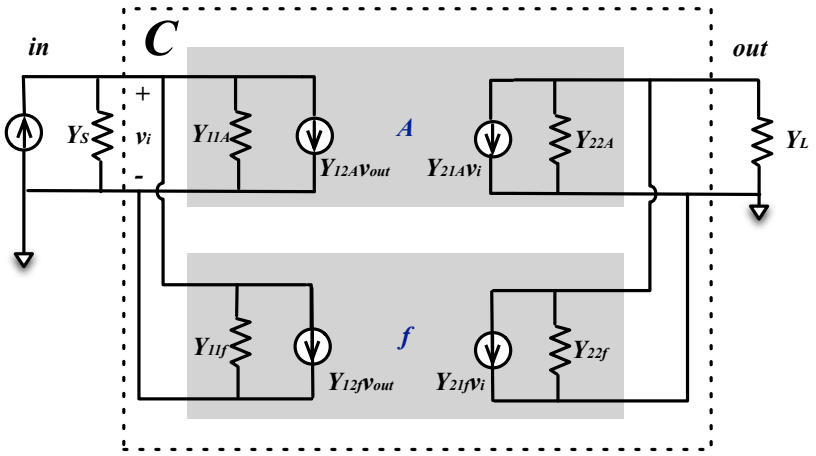


Figure 4.5: Shunt-shunt two-port feedback composition

When designing analog feedback systems, designers generally assume γ and ρ to be small with respect to the desired paths A and f to minimize the effects of the unwanted paths and obtain the desired system behavior (Equation (4.1)). Here, I represent the feedback system using the two-port network representation. In this representation, components are abstracted into four-terminal "black-boxes" represented by characteristic parameters between port 1 and port 2 of the components, where each port is represented by two terminals as shown in Figure 4.5. For example, $Y_{12} = \frac{I_1}{V_2}|_{V_1=0}$ denotes the current flow of port 1 as a function of port 2 voltage. A two-port components are assumed to be linear and capture all possible feedback configurations as shown in Table 4.2. In addition, the two-port parameters capture both feed-forward and feedback signal characteristics for a component, there by accounting for unwanted paths in a feedback system.

In the example in Figure 4.5, which is a feedback network in shunt-shunt configuration, the unwanted paths of Figure 4.4 can be accounted for by the Y-parameters of the components A and f. Specifically, γ, the unwanted feed-forward path, is actually the feed-forward path through component f, which is captured by Y_{21_f}. ρ, the unwanted feedback path is the feedback path through A, which is represented by Y_{12_A}. Now, it becomes obvious that in order to minimize the effects γ and ρ on the system, Y_{21_f} and Y_{12_A} must be minimized, so I add the assumption:

$$|Y_{12_a}| \ll| Y_{12_f}|, \quad |Y_{21_a}| \gg| Y_{21_f}| \tag{4.3}$$

Table 4.2 summarizes corresponding assumptions for all other feedback configurations, using the two-port representation. In fact, as also mentioned in [55], circuit designers already use these assumptions to simplify analysis and derive design parameters, but a design methodology must rigorously account for and enforce these assumptions during composition to ensure correct results. The two-port representation also account for signal attenuation at the input and output ports (Y_i and Y_o for shunt-shunt feedback). Once assumptions in Equation 4.3 are made, the system behavioral model reduces back to Equation 4.1, using the Model equations in Table 4.2.

Configuration	Model	Assumptions
Series-Shunt	$A = \frac{-H1_{21_a}}{Z_i Y_o}$ $f = -H1_{12_f}$	$\lvert H1_{12_a}\rvert \ll \lvert H1_{12_f}\rvert$ $\lvert H1_{21_a}\rvert \gg \lvert H1_{21_f}\rvert$
Shunt-Shunt	$A = \frac{-Y_{21_a}}{Y_i Y_o}$ $f = -Y_{12_f}$	$\lvert Y_{12_a}\rvert \ll \lvert Y_{12_f}\rvert$ $\lvert Y_{21_a}\rvert \gg \lvert Y_{21_f}\rvert$
Series-Series	$A = \frac{-Z_{21_a}}{Z_i Z_o}$ $f = -Z_{12_f}$	$\lvert Z_{12_a}\rvert \ll \lvert Z_{12_f}\rvert$ $\lvert Z_{21_a}\rvert \gg \lvert Z_{21_f}\rvert$
Shunt-Series	$A = \frac{-H2_{21_a}}{Y_i Z_o}$ $f = -H2_{12_f}$	$\lvert H2_{12_a}\rvert \ll \lvert H2_{12_f}\rvert$ $\lvert H2_{21_a}\rvert \gg \lvert H2_{21_f}\rvert$

Table 4.2: Models and assumptions for two-port feedback configurations.

Now, the desired *system behavioral model*,

$$\frac{V_{out}}{I_{in}} - \frac{A}{1 - Af} = 0$$

using the shunt-shunt model in Table 4.2, is valid if the *vertical contract assumptions*

$$|Y_{12_a}| - |Y_{12_f}| \ll 0 \tag{4.4}$$

$$|Y_{21_f}| - |Y_{21_a}| \ll 0 \tag{4.5}$$

are satisfied in composition. However, notice that the model is now in terms of two-port parameters of the components, which themselves are non-ideal and may be complicated. Thus, further assumptions may be needed to reduce the system model, as will be seen in Sections 4.2.2-4.2.4. Furthermore, *component-level contracts* ($\mathbf{C}_A$ and $\mathbf{C}_f$) must also be enforced to maintain compatibility of component contracts in composition.

4.2.2 Sallen-Key Bi-quadratic Cell Composition

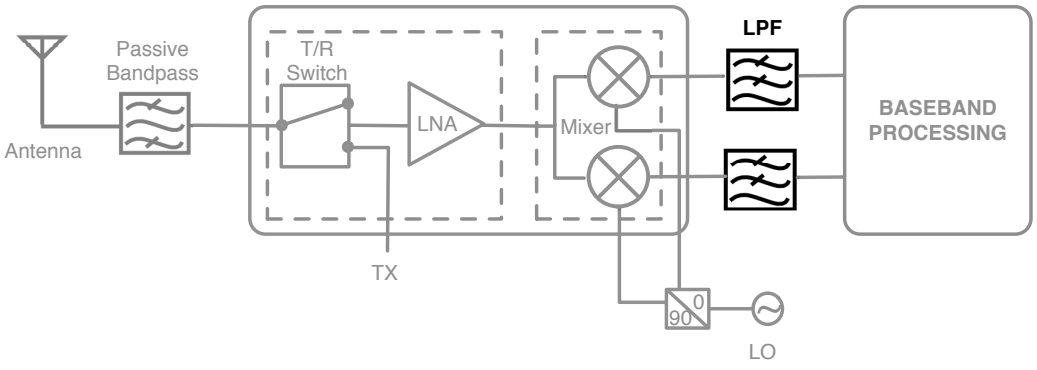


Figure 4.6: UWB Direct-conversion receiver system

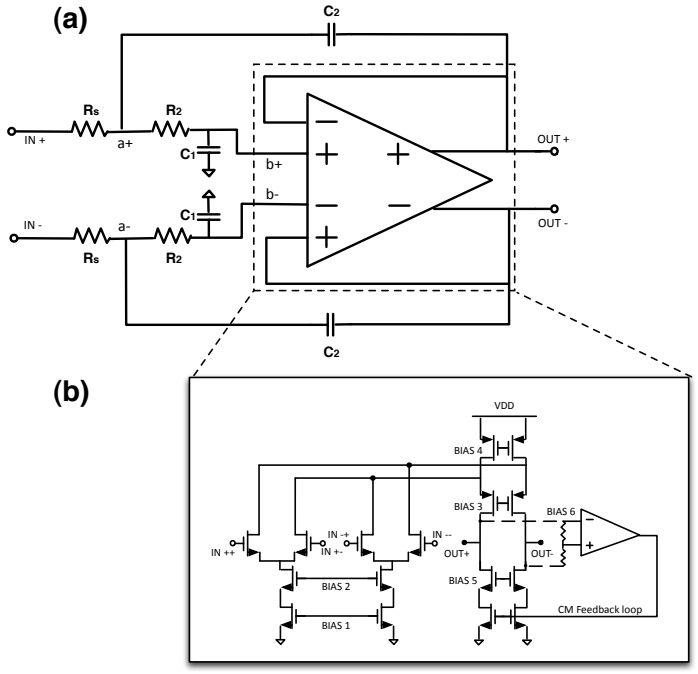


Figure 4.7: (a) Differential Ultra-wideband Sallen-Key Low-pass Filter System (b) Differential difference amplifier (DDA) transistor-level schematic

In this section, I go over a concrete example using a simple, yet practical case study: a Sallen-Key (SK) bi-quadratic cell. This methodology, however, targets bigger and less well-studied systems than the Sallen-Key cell. This example is meant as a good demonstration for the reader: it has an intuitive circuital functionality, yet it is capable of fulfilling complex system requirements, as witnessed by the wide industrial adoption of the cell. In this study, the SK cell is used for an UWB direct-conversion receiver, as shown in Figure 4.6, where the base-band filter is needed to remove unwanted frequency components from the down-converted signal. I specifically focus on the design of a Sallen-Key cell [56], which is a widely adopted topology for its low power consumption and high linearity, and it has recently been used also for UWB applications [57]. The design of the cell is shown in Figure 4.7a. In the following, I will study the composition of the forward path amplifier in closed-loop unity-gain configuration, together with the RC-network in feedback configuration. I focus specifically on the outer feedback loop, which directly determines the filter transfer function, and, as such, its design is constrained by system-level requirements.

4.2.3 Component Characterization

The main component of the Sallen-Key cell is a Differential Difference Amplifier (DDA) [58] (see figure 4.7b, which has been previously designed and characterized using 90nm, 1.2V technology from United Microelectronics Corporation (UMC). Similar to component characterization in Chapter 3, the performance space of the amplifier in closed-loop unity gain configuration was

characterized by running 2500 batch simulations, while strategically varying circuit-level configuration variables such as the transistor length, width, biasing, etc. Moreover, for each configuration, a set of interface assumptions on the operating environment were modeled using RC networks at the input (source) and the output (load) ports. The range of values of the loading assumptions were:

$$R_{source} \in [100, 1000]\,\Omega \quad C_{source} \in [0.01, 1]\,pF$$
$$R_{load} \in [1, 1000]\,k\Omega \qquad C_{load} \in [0.1, 10]\,pF$$

Before extracting the performance parameter, a circuit-level stability assumption, $(\phi_m > 45^\circ)$, was enforced to ensure only stable amplifiers are provided to the system designer. Each set of stable performance outputs and interface assumptions are transcribed into AP_{DDA}, as summarized in Table 4.3.

Performances									
Power	BW	Noise	Gain	HD3	SR	R_{in}	C_{in}	R_{out}	C_{out}

Table 4.3: Characterized DDA Performances

4.2.4 Vertical Assumptions

At the system-level, the ideal frequency domain transfer function for a second-order low-pass filter is

$$T_{LPF}(s) = \frac{K}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1} \tag{4.6}$$

When applied to the Sallen-Key filter in 4.7a, the system behavioral model becomes:

$$\frac{V_{out}}{V_{in}}(s) = \frac{K}{s^2(R_sR_2C_1C_2) + s(R_sC_1 + R_2C_1 + R_1C_2(1-K)) + 1} \tag{4.7}$$

where K is the gain of the amplifier (ideally 1, in this configuration). The bandwidth and quality factor of the cell are:

$$BW_{SK} = \frac{1}{2\lambda\sqrt{R_sR_2C_1C_2}} \tag{4.8}$$

$$Q_{SK} = \frac{\sqrt{R_sR_2C_1C_2}}{C_1(R_s + R_2) + R_1C_2(1-K)} \tag{4.9}$$

Power, gain (K), and noise performances are derived from AP_{DDA}.

The above model would be valid if the amplifier was ideal and all paths were unidirectional. The real system is much more complicated, and the system model must account for the DDA's non-ideal transfer function, non-infinite input and non-zero output impedance of the DDA, and the mutual loading effects between the cell and the rest of the receiver chain.

To derive the necessary assumption conditions, I leverage the assumptions derived in Section 4.2.1 for two-port network in shunt-shunt feedback configuration, as shown in Figure 4.5, while accounting for non-ideal DDA behavior based on the characterized performance model from Section 4.2.3. The forward path (A) of the two-port network consists of R_2, C_1, and the DDA (in figure 4.7b, it is the path between node a and out); the feedback path (f) is across C2. From the impedance information of the DDA and the Sallen-Key configuration, I can derive the 2-port parameters, shown in Table 4.4, where $Z_{out} = \frac{R_{out}}{1+sR_{out}C_{out}}$, C_s and C_l are parasitic loading capacitances at the source and load of the Sallen-Key filter.

Y_{11A}:	$\frac{1+sR_{in}(C1+C_{in})}{R_{in}+R2+sR_{in}R2(C1+C_{in})}$	Y_{12A} :	$-\frac{1}{KR2}$
Y_{21A}:	$\frac{KR_{in}}{Z_{out}(R_{in}+R2+sR_{in}R2(C1+C_{in}))}$	Y_{22A}:	Z_{out}^{-1}
Y_{11f}:	$sC2$	Y_{12f}:	$-sC2$
Y_{21f}:	$-sC2$	Y_{22f}:	$sC2$
Y_S:	$\frac{1}{R_s+sC_s}$	Y_L:	$\frac{1}{R_l+sC_l}$
Y_i:	$Y_s + Y_{11A} + Y_{11f}$	Y_o:	$Y_l + Y_{22A} + Y_{22f}$

Table 4.4: Two-port Y-parameters of Sallen-Key filter.

The assumptions in Equation (4.4) allow undesired paths in the filter to be ignored, but they still do not take into account the loading of the DDA input and output impedances on the overall cell, which result in a complex higher-order system of equations that do not fit the desired behavior, Equation (4.7). Thus, additional assumptions must be made in order to constrain the system behavior to fit the desired system functionality. Table 4.5 and 4.5 shows the complete list of vertical assumptions derived for frequencies $\omega < \omega_{DDA}$, while Table 4.7 shows the DDA loading assumptions at the corner frequency of the filter. Note that $Zsource_{actual}$ ($Zsource_{load}$) include the output (input) impedances of the DDA loading onto itself, which shows why *compatible regions* are difficult to explicitly specify.

$\mathcal{A}_{SK1}$	$\lvert Y_{12_a}\rvert \ll \lvert Y_{12_f}\rvert \Rightarrow \lvert \frac{1}{sR2C2}\rvert \ll \lvert K\rvert$
$\mathcal{A}_{SK2}$	$\lvert Y_{21_a}\rvert \gg \lvert Y_{21_f}\rvert \Rightarrow \lvert s^2C1C2R2Z_{out} + sC2\rvert \ll \lvert K\rvert$

Table 4.5: Sallen-Key system-level non-ideal path assumptions.

$\mathcal{A}_{SK3}$	$R_{in} \gg R2$	$\mathcal{A}_{SK8}$	$Z_{out} \ll Z_l$
$\mathcal{A}_{SK4}$	$R_{in} \gg R_s$	$\mathcal{A}_{SK9}$	$Z_{out} \ll R2$
$\mathcal{A}_{SK5}$	$C_s \ll C2$	$\mathcal{A}_{SK10}$	$Z_{out} \ll Z_s$
$\mathcal{A}_{SK6}$	$C_{in} \ll C1$	$\mathcal{A}_{SK11}$	$\omega_{SK} < \omega_{DDA}$
$\mathcal{A}_{SK7}$	$C_{out} \ll C2$		

Table 4.6: Sallen-Key system-level non-ideal component assumptions.

$\mathcal{A}_{DDA1}$	$\lvert Zsource_{assume} - Zsource_{actual}\rvert < \delta_{source}$
$\mathcal{A}_{DDA2}$	$\lvert Zload_{assume} - Zload_{actual}\rvert < \delta_{load}$

Table 4.7: DDA loading assumptions.

Now that the component model, system-level behavioral model, and all assumptions have been defined, the performance of the Sallen-Key filter can be optimized using Algorithm 1. Since the system target a UWB signal with 500 MHz double-sided bandwidth, the main system specification constraint requires the filter bandwidth to be at least 250 MHz (single-sided, when mixed down to base-band) to retain the necessary frequency content of the base-band signal. However, depending on the specific application, other system objectives may differ. To show how the methodology allows design flexibility and ease of configuration, I optimize the system for several possible objectives commonly found in UWB applications: 1) minimum power, 2) maximum base-band gain, 3) maximum bandwidth, and 4) maximum stop-band attenuation.

4.3 Results

Table 4.8 shows the results for various optimization objectives, which demonstrates flexible system reconfiguration in the design flow. The system and its underlying IP component can be easily tuned to satisfy various objectives for different potential UWB applications. The fastest optimization run to converge to an optimal design is the minimum power objective, and the most time consuming

was the max stop-band attenuation objective. This is because I added extra constraints to ensure the lower band signals are not overly attenuated just to maximize stop-band attenuation. In addition, it can be observed that as the number of designs evaluations increased, the average time **per design evaluated** increased because the *compatible region* was being exhausted, so finding new compatible designs took longer, which reinforces the intuition that the preprocessing step in the algorithm helps speed up design space exploration.

The main focus here is to examine the accuracy of the constructed system, compared with the desired system model, by enforcing vertical assumptions. Figure 4.9 shows a sample comparison of the transfer function of the filter between the system model and circuit-level simulations. The system-model matched circuit simulations very well within the frequency of interest. To further examine the error performance, I ran circuit simulations for 8000 different design configurations. (4000 enforced with vertical assumptions and 4000 that were not) Figure 4.8 shows the histogram distributions of the errors for gain and bandwidth, comparing system model with circuit-level simulations. Note that although I am using the exact same system model, the ideal Equation (4.7), designs generated under contract constraints are much more accurate: average error reduction of 10% for gain and 60% for bandwidth. Improvements in bandwidth was more significant because bandwidth was mostly influenced by the system behavior, where as other performances were more related to component performances. In addition, there were much less variance in the distribution of the errors for the *Contract* designs, suggesting that *Contract* designs consistently tracked circuit-level simulations results, offset by some constant.

Several factors may have contributed to the remaining residual errors. First, the loading assumption of the components were modeled as a first-order RC pair, where as the actual loading of the DDA by the system is a higher-order RC path. Similarly, the input and output impedance of the DDA were lumped into equivalent RC pairs, which also discarded high-order effects on the system model. Lastly, as mentioned, the assumptions ensured that the system model was valid within the frequency of interest; however, the ignored higher-order terms may introduce poles or zeros close to the band of interest, distorting the transfer function of the filter. But overall, the results are very accurate, and the new vertical assumptions are critical in enforcing valid system compositions in APBD.

	Min Power	**Max Gain**	**Max Bandwidth**	**Max 500MHz Attenuation**
Power	**0.3 mW**	1.3 mW	1.2 mW	1.28 mW
BW	280 MHz	285 MHz	**380 MHz**	250 MHz
Baseband Gain	-4.58 dB	**-0.48 dB**	-3.9 dB	-2.94 dB
Attenuation @ 500MHz	-13 dB	-12.2 dB	-9.3 dB	**-16 dB**
Designs Evaluated:	6597	37031	28045	83689
Runtime	77 sec	32 min	19 min	152 min

Table 4.8: Summary of Optimization Results

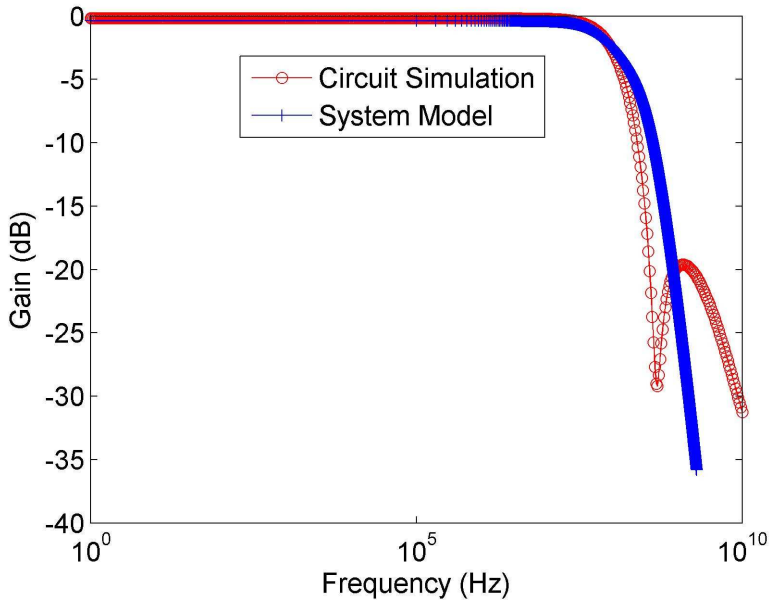


Figure 4.8: Comparison of System Model vs. Circuit Simulation for Sallen-Key Filter

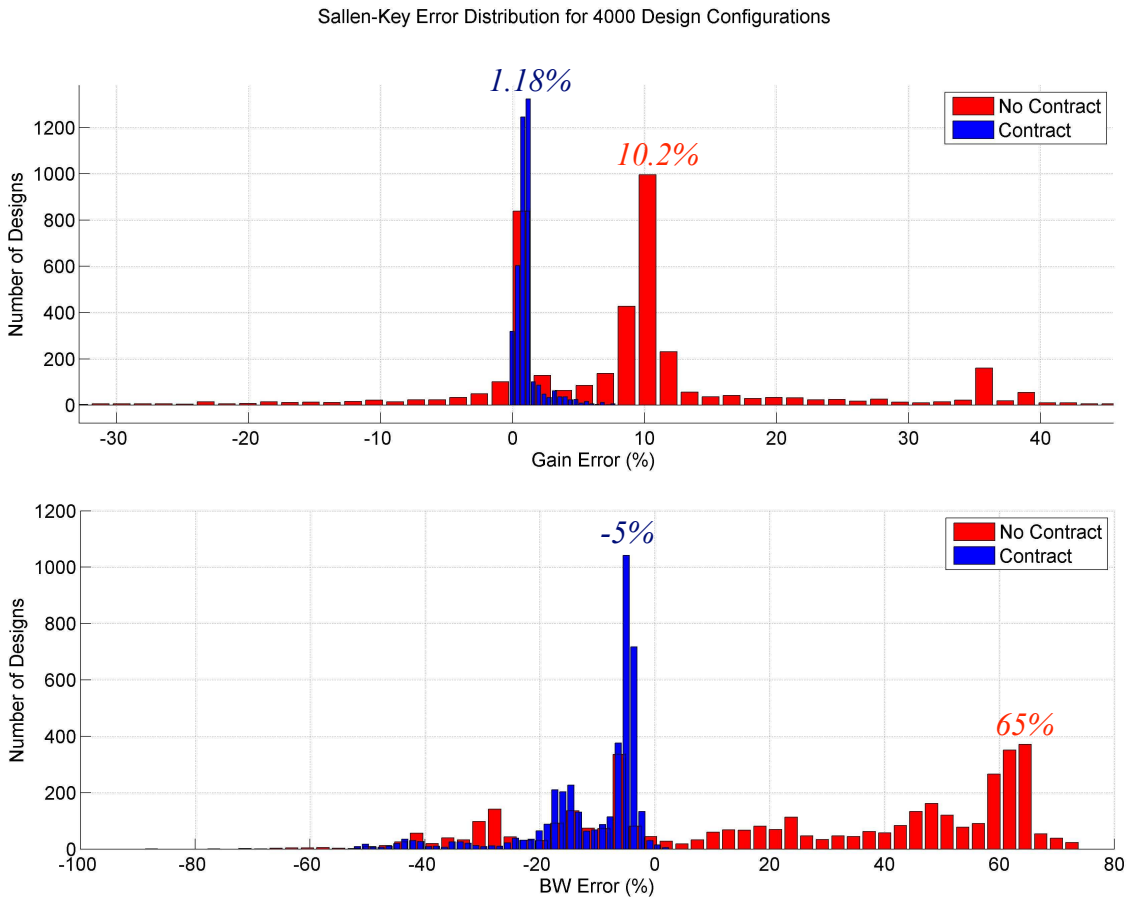


Figure 4.9: Error histogram distribution comparing system model to circuit simulation on 4000 contract-based configurations vs 4000 no-contract configurations.

Vertical contracts are essential to build correctly behaving systems, and need to be considered in any design flow where system architecture and component designs are orthogonalized. Thus, various assumptions for designing the system need to be mapped together. In this chapter, we've discussed to process "vertically" propagation of these assumptions as constraints down to the component-level. The set of valid compositions that satisfy both the vertical contracts and the compatibility conditions of component-level horizontal contracts provides system-level guarantees, which are used in the definition of system-level contracts. As an initial step towards correct-by-construction designs, enforcing vertical assumptions in contract-based analog composition ensure that mapping of the desired system specifications into the final implementation remains accurate and reliable, which minimizes the number of iterations needed for design validation, shrinking the

product design cycle and improving the efficiency of design teams. Furthermore, the constructed system-level contracts can be used to compose various subsystems together into the final system, allowing subsystems to be developed independently, further improving the productivity of design teams.

Chapter 5

Application: UWB Receiver for Intelligent-Tire-System

In this chapter, I apply the contract-based composition methodology for design and integration of a complete industrial design example: UWB receiver system for an Intelligent-Tire-System (ITS). ITS is an distributed on-vehicle wireless sensor network for data acquisition of real-time road-surface and vehicular information from complex intelligent sensors located *inside the tire*. Due to the harsh environment and application requirements, the design of ITS is extremely challenging and requires a multi-disciplinary team including control system design, signal processing, integrated circuit design, communications, real-time software design, antenna design, energy scavenging and system assembly. We consider specifically the design and composition of the UWB receiver system, a critical unit located on the vehicle responsible for wirelessly receiving sensor data from the tires and pre-processing for base-band data extraction algorithms. We demonstrate the complete design flow from system modeling to system construction and optimization. First, I give a brief introduction to ITS, before introducing a system-level model and requirements for the communication system. Based on the model, an architecture and design specification for the receiver system is derived. Then, using the contract-based composition methodology introduced in previous chapters, the complete receiver system is composed and optimized from a library of pre-characterized components, specifically the low-noise amplifier (LNA), mixer, and a low-pass filter system composed of second-order filter cells. The design process shown in this chapter is meant as a template to follow for future applications of the contract-based composition methodology form analog systems.

5.1 Intelligent Tires

5.1.1 Background: Automotive Safety Systems

Road traffic injuries still represent about 25% of worldwide injury-related deaths (the leading cause) with an estimated 1.2 million deaths(2004) each year [59]. Passive safety devices, such as crumple zones, seat-belts, and airbags, work passively to prevent injuries and are standards today. Obviously, these devices, albeit effective, are nowhere near to *preventing accidents*. Active safety is the frontier for OEMs and suppliers to eliminate deadly accidents, with the ultimate goal of avoiding a crash altogether. Active safety systems use information about the external environment of a vehicle to change its behavior in pre-crash time period or during the crash event. Eventually, the completely *autonomous zero-accident car* will be possible based on wireless and wired networks of powerful sensors (see Figure 5.1, courtesy of General Motors) and complex control algorithms implemented on a distributed computing platform.

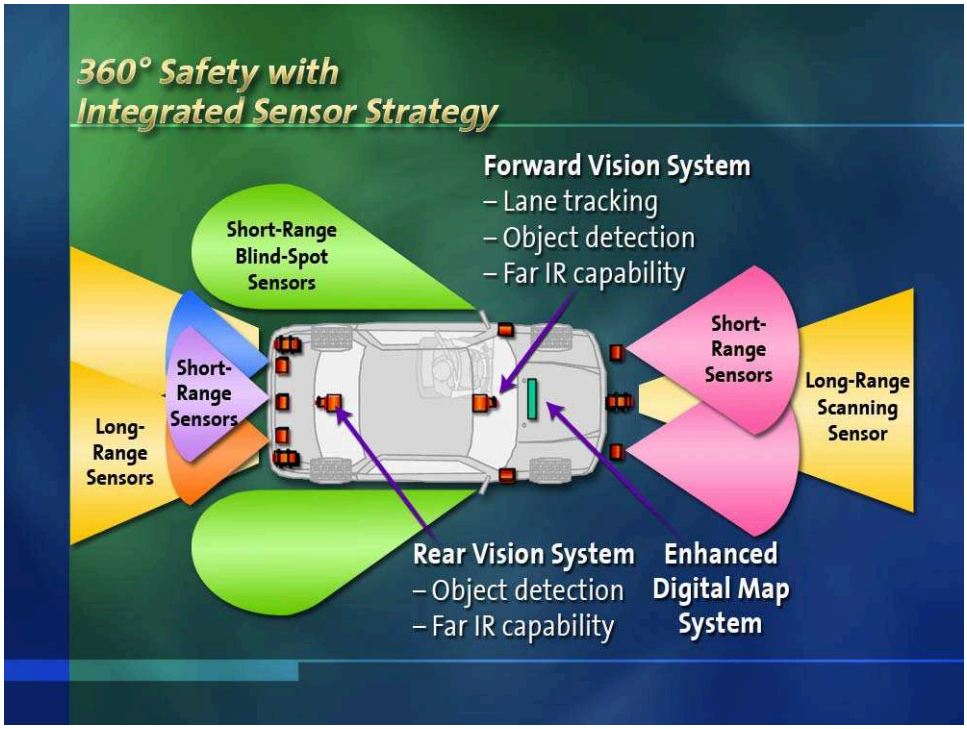


Figure 5.1: 360 degree Integrated Safety

The active safety control systems described above are based upon the estimation of vehicle dynamics variables such as forces, load transfer, actual tire-road friction (kinetic friction) μ_k, and maximum tire-road friction available (potential friction) μ_p, which is probably the most important parameter for the improvement of vehicle dynamic control systems [60]. The more accurate

and “real time” the parameter estimation is, the better the overall performance of the control system. Today, most of these variables are indirectly estimated using on-board sensors. With a more accurate estimation, even the road surface condition can be identified in real-time.

To address the real-time road surface data-acquistion problem, the Intelligent-Tire-System [ITS] was proposed. [61] Currently state-of-the-art tire monitoring systems [62, 63, 64, 65, 66] primarily acquire low-duty cycle data such as tire pressure, temperature, and/or material strain of the tire. However, they are not equipped to sense and transmit high-speed dynamic variables used for real-time active safety control systems. Until recent developments in low-power wireless communication and energy-scavenging, real-time data acquisition and analysis directly from tires have been resource-intensive and remained mostly in the research domain since it was not easily adoptable as a consumer product.

5.1.2 Intelligent-Tire-System

ITS is distributed architecture, shown in Figure 5.2, for a data acquisition system that is based on a number of complex intelligent sensors *inside the tire* that form a wireless sensor network with coordination nodes placed on the body of the car.

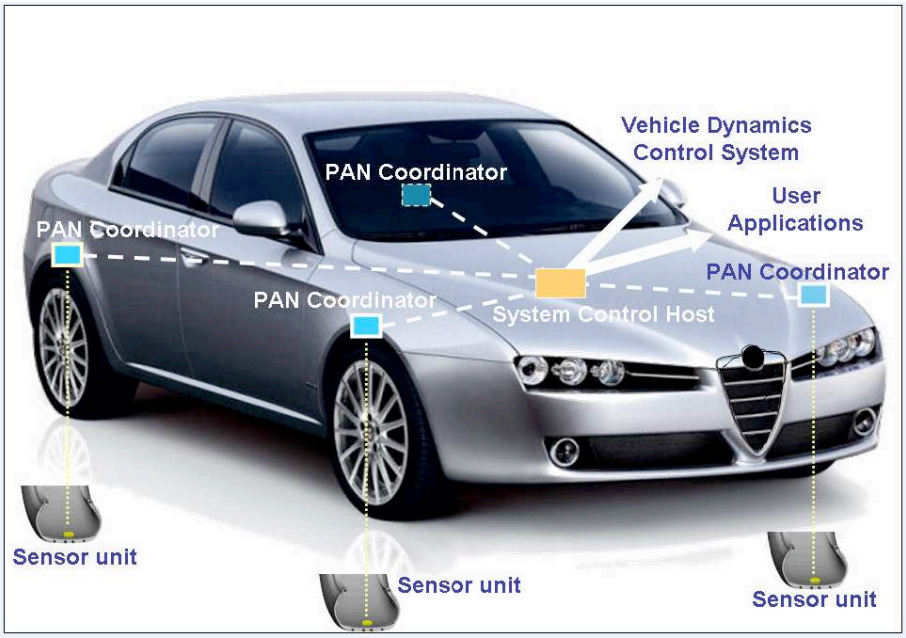


Figure 5.2: System architecture

The data collected offer real-time road surface and vehicular information, based upon complex accelerometers data processing and modeling, necessary to significantly improve active safety and active dynamics control systems including:

- *Tire Level:* Simple temperature and pressure information; lateral and longitudinal forces; potential friction estimation; tire load; tire wear; and aquaplaning.
- *Vehicle Level* vehicle load distribution; dynamic load transfer estimation; and road friction.

For example, Figure 5.3 shows the estimation of the vehicle load transfer in non-stationary dynamic maneuvers consisting in multiple acceleration and deceleration sequences.

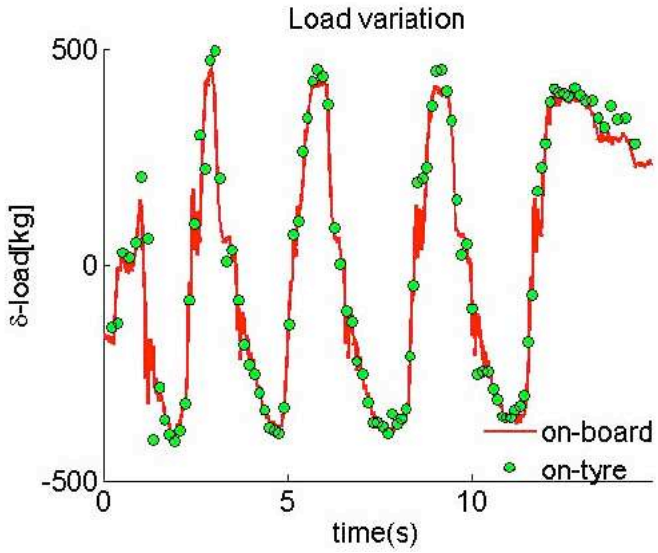


Figure 5.3: Load transfer during multiple acceleration-deceleration maneuvers. Circles represent the estimated load transfer with the intelligent tire system while the solid line is the traditional load estimation method based upon sensors on vehicle.

The main components of the system are organized in a hierarchical manner in a Personal Area Network (PAN) defined as a collection of cooperating devices which are associated and share the same address space. At the lowest level sensor nodes, located inside the tires, are responsible for data acquisition, processing and transmission to the in-vehicle equipment. At the upper level of the hierarchy, the *PAN coordinator* manages the communication with the sensor nodes on a single tire, receives data from them, and is the master of synchronization. PAN coordinators can be connected to the *System Control Host*, which interfaces the PAN coordinators with the vehicle main control, via a wired network or even a vehicle system bus such as CAN and FlexRay. The resulting network architecture has a cluster tree structure.

The design of ITS is extremely challenging due to the very limited available energy on the tires combined with strict application requirements for data-rate, delay, size, weight and reliability in a highly dynamical environment. Moreover, it required expertise in multiple engineering disciplines including control system design, signal processing, integrated circuit design, communications, real-time software design, antenna design, energy scavenging and system assembly. In

this chapter, I discuss specifically about the uplink communication from tire sensors to the PAN coordinator, which one of the most critical links in the system in order to deliver real-time information to the vehicle. Specifically, I look at the design and composition of the UWB wireless receiver system located on the PAN coordinators.

5.2 UWB Communication System Planning and Specification

The communication environment in ITS is very harsh. Since the sensors are located inside the tire body, wireless signals must traverse through the tire mesh to reach the on-vehicle receivers. The anatomy of modern tires, Figure 5.4, is very complex, consisting many layers of steel, nylon, polyester, and rubber materials.

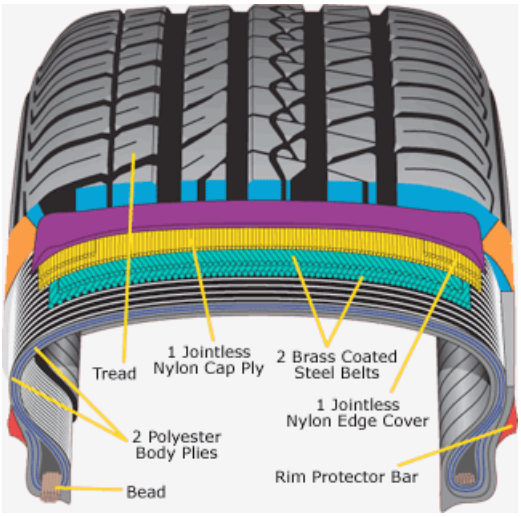


Figure 5.4: Anatomy of a tire

A true LOS channel is impossible, since the tire mesh attenuates the signal dramatically. In addition, there are two large reflectors in the immediate vicinity of the node: the wheel rim and the wheel arch of the cars body. Both of these are virtually always metal and are curved such that they tend to reflect incident waves back into the area, confining them. These environment characteristics creates a rich multi-path profile for the transmitted signal, and the received signal power is the combined energy of various reflected paths of the transmitted signal arriving with different time delays. Given such conditions, impulse-based UWB radio transmission is preferred.

5.2.1 UWB Communication

Ultra-Wide-Band (IR-UWB) transmission is preferred to narrow-band transmission and spread spectrum techniques due the presence of severe multi-path and lack of line-of-sight [67]. UWB

technology has emerged in recent years as an ideal candidate for low cost, low power, short-range wireless data transmission. In addition to being robust to inter-symbol interference due to multi-path fading, the UWB systems hide signals below the noise floor causing little or no interference *to* existing narrow-band systems. Furthermore, due to the low-duty cycle of the signal patterns, UWB signals have a high-instantaneous SNR by concentrating the transmitted energy within a short-time frame, which mitigates performance degradation of the system due to interference *from* narrow-band systems.

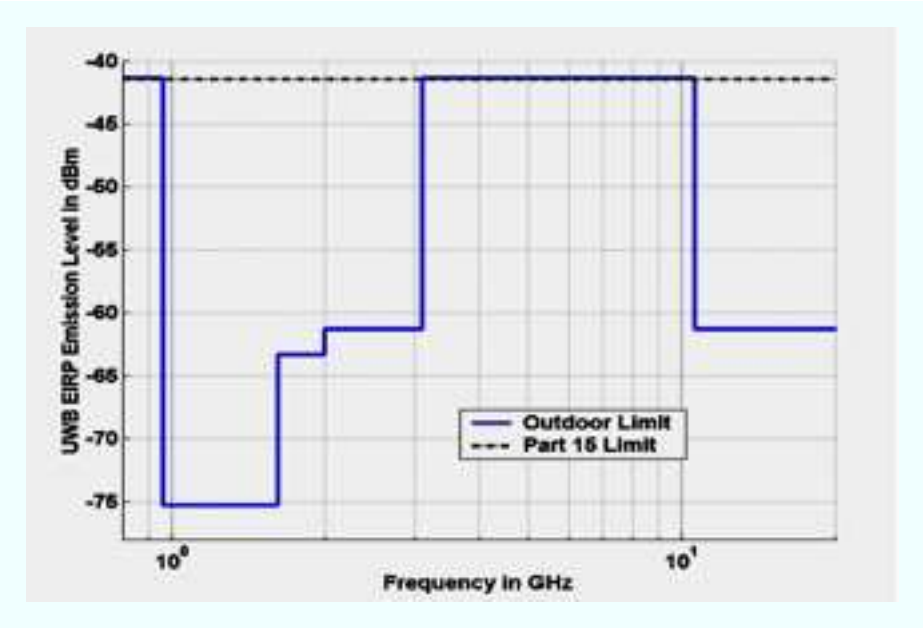


Figure 5.5: FCC spectrum mask for UWB signals

FCC defines UWB as any radio technology for which the emitted signal bandwidth, B_f, exceeds the lesser of 500MHz and 20% of the center frequency [68].

$$B_f = 2 * \frac{f_H - f_L}{f_H + f_L} \tag{5.1}$$

where f_H and f_L are the higher and lower -10dB point of the frequency spectrum of the signal, respectively. In 2002, FCC has allocated the 3.1-10.6 GHz band for the unlicensed use of UWB applications, subject to power spectral density emission limits illustrated in Figure 5.5 to avoid interference to existing radio technologies in the allocated frequency range. [69]

For the ITS application, impulse-based UWB technology was utilized due to the simple transmitter architecture on the tire sensors, which makes it ideal for the low power high data rate uplink transmission to the vehicle.

5.2.2 Tire UWB Channel

The first step to designing any communication system is to understand the transmission channel that carries the signal. From the channel characteristics, the system requirements for the receiver system can be derived. The UWB channel can be mainly modeled as the following components: *channel attenuation, noise, multi-path power-delay-profile (PDP), and interference*. First, channel attenuation of the transmitted signal is expected due to distance dependent pathloss, as well as attenuation through the tire rubber and metal mesh. The noise profile of the channel is very hard to characterize or predict. Here, I use thermal noise of the electronics as the main contribution of noise. In addition, UWB signals exhibit a rich multi-path profile, where the signal energy is scattered through the channel, and each path expected to arrive at the receiver at different times. Thus, the PDP of the signal through the channel must also be modeled. Lastly, interference from other nearby communication systems must be accounted for. In particular, strong narrowband signals near the frequency of interest may interfere with the transmitted signal and need to be accounted for. Wide-band interference (WBI) from nearby unwanted UWB applications are not expected because ITS employs a time-domain-multiple-access (TDMA) medium access protocol, thus multi-user interference is not expected to corrupt the channel. In addition, due to the isolated location of the sensors inside the tire, a natural barrier from unwanted signals is formed, improving attenuation to interfering signals.

Channel Measurement Setup

To accurately capture the channel characteristics of the system, a Hyundai Accent vehicle body was used for the ITS channel measurements. The wheel arch and all machinery inside including the suspension were preserved. The SkyCross UWB antennas are placed inside the tire under the tire tread and at the highest point inside the wheel arch. The transmit signal from inside the tire consisted of 100ps pulses, and the received signals on the vehicle were amplified and sent to a 20GS/s, 6GHz input bandwidth oscilloscope. The setup in BWRC (Berkeley Wireless Research Center) is shown in Figure 5.6.

Figure 5.6: Channel measurement setup

The measurements are performed for two tires, Hankook 175/70R13 and Pirelli Pzero Nero M+S 204/45R16, at 8 positions around the rotation of the tire, i.e. every 45 degrees.

Attenuation

The channel attenuation is designated α as plotted in Figure 5.7. The values for the Pirelli tire are generally larger than for the Hankook tire. This is easily attributed to the thicker and more robust construction of the Pirelli tire.

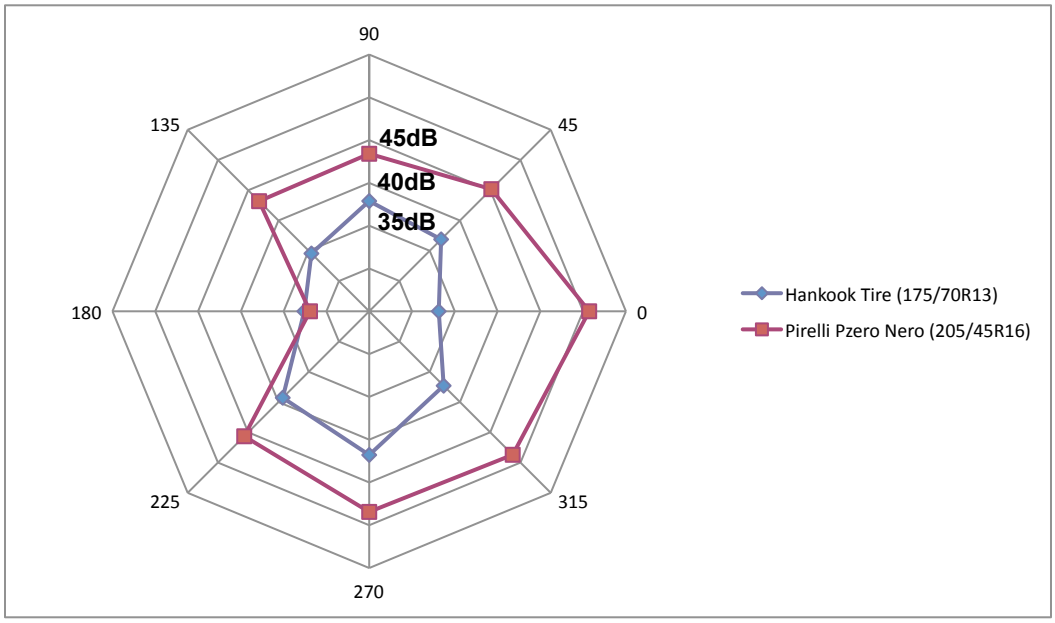


Figure 5.7: α for Hankook (blue) and Pirelli (red).

In the case of the tire channel, the LOS is probably through the tire thread and, therefore, is very weak. The strongest rays travel through the side-walls and experience at least one reflection before arriving at the receiver. Thus, the majority of the received signal power are due to the multi-path signals, which can be modeled as the Power Delay Profile (PDP).

Power Delay Profile

The power delay profile of UWB signals have been studied extensively for both indoor and outdoor communication systems. [70] However, these environments are much larger than the wavelengths present in the signal and they are mostly empty. In contrast the area around the tire is quite different. There are two large reflectors in the immediate vicinity of the node: the wheel rim and the wheel arch of the car's body. Both of these are virtually always metal and are curved such that they tend to reflect incident waves back into the area, confining them. Furthermore, the radius of curvature of these two bodies is on the order of the wavelength, making reflections much more complex. Curvature of the wheel-well surface further increase multipath reflections of the signal.

Since the multi-path profile of the UWB channel is random in nature, and depends heavily on the actual operating environment, it is very hard to characterize using direct channel measurements. Instead, measured channel impulse response is fitted onto a statistical model. In this application, the measured channel response is fitted onto a modified Saleh-Valenzuela (SV) model based on the UWB model developed for the IEEE802.15.4a standard. [70].

The SV channel model assumes that the total received signal is partitioned into different paths, or rays, which arrive in clusters. The clusters arrive according to a Poisson process, and the power

envelope for the clusters follows an exponential-decay random process. Each cluster is made up of rays, which also arrive according to a Poisson process and decay according to an exponential random process, as dictated in [70]. Mathematically, the channel impulse response is represented as

$$h(t) = \sum_{l=0}^{L} \sum_{k=0}^{K} \alpha_{k,l}^{i} \delta(t - T_l^i - \tau_{k,l}^i) \tag{5.2}$$

where

- $\{\alpha\}$ are the gain coefficients of each multipath element and attenuates with increasing delay from the first ray,
- $\{T\}$ are the delay of the clusters of ray arrivals, assumed to be a Poisson process
- $\{\tau\}$ are the delay of the different multipath components for each cluster, assumed to be a Poisson process.

Figure 5.8 shows an example of the PDP of the SV channel model to show the differentiation between clusters and rays. Here, the gain coefficients of each ray and cluster are assumed to be exponentially decaying.

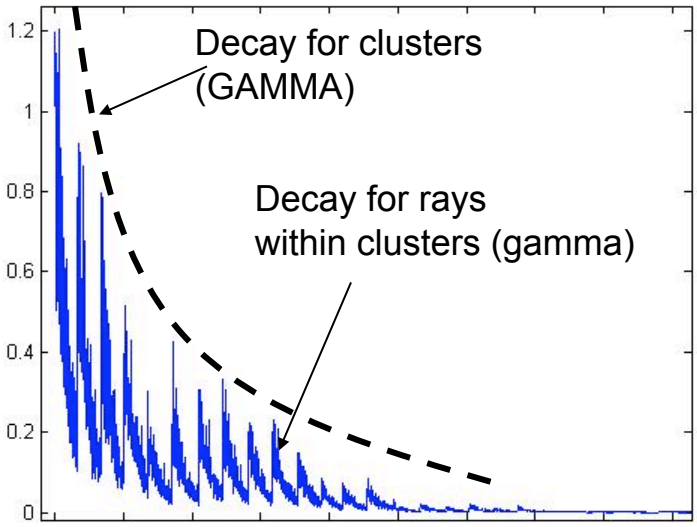


Figure 5.8: SV-Model cluster and ray decay

However, when comparing the model response with the measured channel impulse response of the tires, it was apparent that the standard UWB SV model generated too much incoming energy at

the early times due to the exponential envelope. Intuitively, this early-time energy is due to a strong line-of-sight (LOS), or at least significant energy traveling in a geometrically straight line from the transmitter to the receiver. In the case of the tire channel the LOS is probably through the tire tread, and therefore is very weak. The strongest rays travel through the sidewalls and experience at least one reflection before arriving at the receiver. Thus, the exponential random envelope for the cluster arrivals was deemed inappropriate. The exponential envelope for the cluster power was changed to a Rayleigh random envelope. (Figure 5.9) The Rayleigh distribution has maximum energy at some time greater than zero, but usually a small number. In this case, this is a few nanoseconds. All other aspects of the model were unchanged: Poisson process for cluster and ray arrival times and exponential decay of ray power within a cluster. This new model is referred to as the SV-R model. A comparison of the measured channel response and the SV-R model generated response is shown in Figure 5.10, showing a close match in behavior.

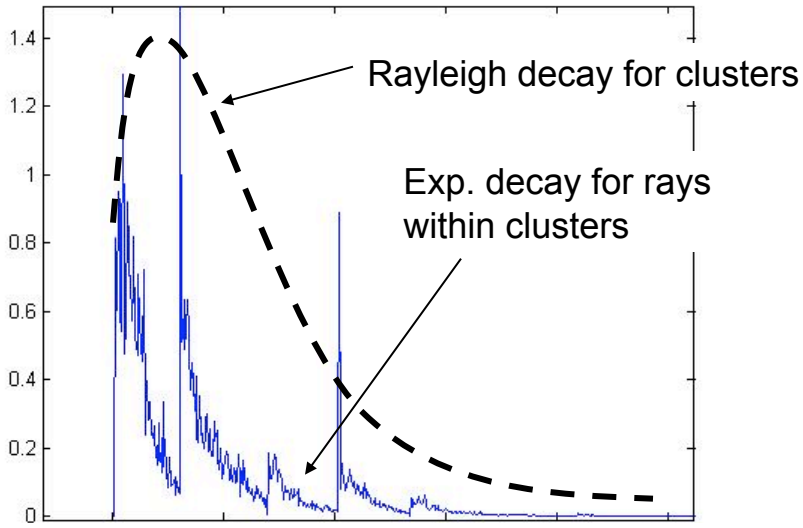


Figure 5.9: Rayleigh SV UWB channel model.

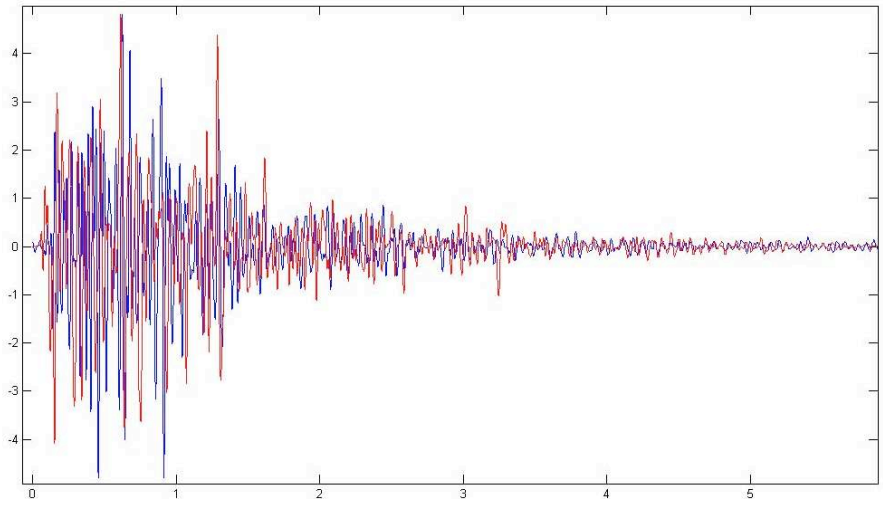


Figure 5.10: Impulse response of SV-R model (red) compared to the measured data (blue). The x-axis is in 10 ns.

The multipath delay spread, which is defined as the time at which the impulse response falls below the noise floor is between 30-40 ns.The arrival time process for the clusters is governed primarily by T whereas the ray arrival time process is governed by the parameter τ. Typical values for T are slightly less than 10ns, and τ is typically a few nanoseconds. These values are significantly lower than the scenarios found in the 802.15.4a standard. This is due to the much shorter flight distances involved in the tire area compared to the scenarios considered in the standard. T and τ were found not to vary much in different positions. Much greater variation was observed for cluster decaying factor and ray decaying factor, γ_C and γ_r, which are controlling parameters for the Rayleigh distribution functions, respectively. They are plotted in Figure 5.11.

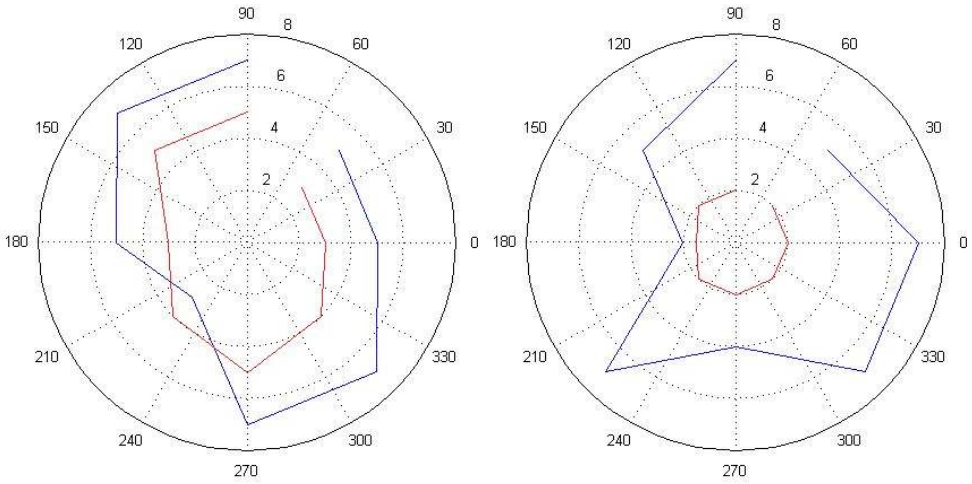


Figure 5.11: γ_c (outer, blue) and γ_r (inner, red) for Hankook (left) and Pirelli (right) in ns.

Narrowband Interference

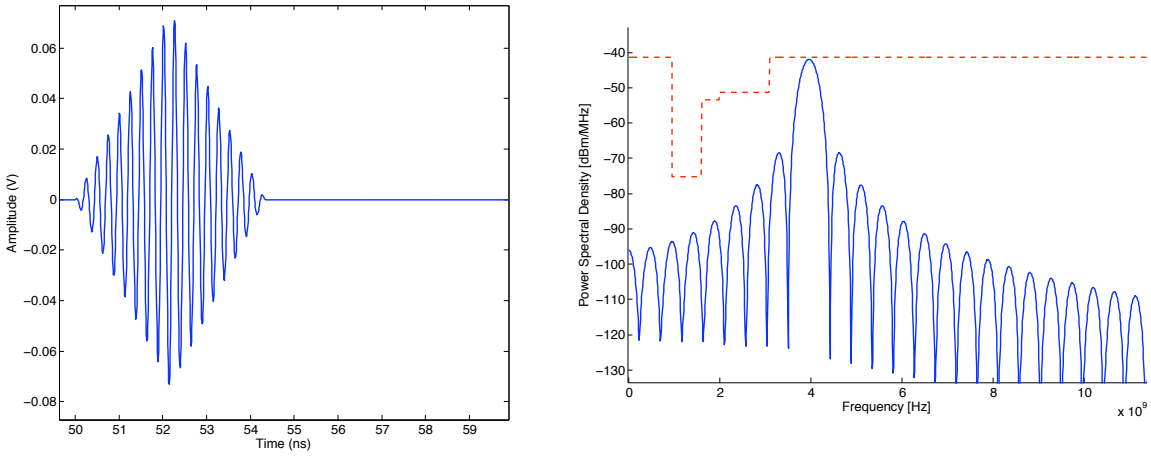
Due to the wide bandwidth of UWB signals, they are prone to interference from many sources with may degrade the receiver performance adding unwanted modulation to the desired signal and by saturating the system components. In addition to designing the system to provide enough headroom to withstand in-band interference, the non-linearity of the electronic system may create in-band harmonics for out-of-band interferers, which also must be accounted for in the channel model. In the ITS application, narrowband interference is of more concern because the MAC protocol and the system environment protects the sensor nodes from interference caused by other nearby wide-band systems

Interferer	Frequency	BW	Output Power	Attenuation	**Received Power**
WiFi	2.4 GHz	30 MHz	20 dBm	80 dB	**-60 dBm**
Bluetooth	2.4 GHz	1 MHz	5 dBm	58 dB	**-53 dBm**
WiMax	3.5 GHz	20 MHz	47 dBm	85 dB	**-38 dBm**
UNII (low)	5.2 GHz	30 MHz	16 dBm	60 dB	**-44 dBm**
UNII (high)	5.8 GHz	30 MHz	29 dBm	69 dB	**-40 dBm**

Table 5.1: Narrow-band interference signals for ITS.

Near the 3.1-10.6 GHz band, several narrowband standards may cause interference in the system, as shown in Table 5.1. For each interfering signal, attenuation is assumed based on transmit distance, filtering, and antenna band selection before the LNA of the receiver.

5.2.3 Signal Transmission

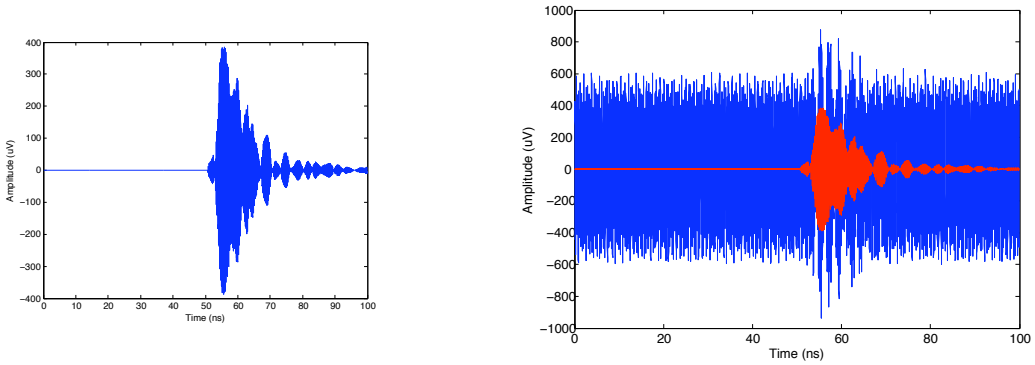


(a) Transmitted Pulse

(b) Power Spectral Density

Figure 5.12: (a) Triangular sinusoidal pulse with a pulse width of 4.35ns; (b) PSD of transmitted signal with 500MHz 10-dB bandwidth.

The transmitted pulse for ITS is a 4.35-ns triangular sinusoid pulse (Figure 5.12a) with carrier frequency centered at 3.96 GHz. Figure 5.12b shows the power-spectral-density of the pulse, which fits below the UWB mask dictated by FCC and has a 500MHz 10-dB bandwidth. Figure 5.13a shows the transmitted pulse after channel attenuation and multi-path effects, and Figure 5.13b shows the actual signal arriving at the receiver antenna, in which the actual desired signal is hidden below added narrowband interference signals.



(a) With channel attenuation & multi-path effect (b) With narrowband interference

Figure 5.13: Received Signal: (a) with attenuation and multipath only; (b) with added narrowband interference, with desired signal in red.

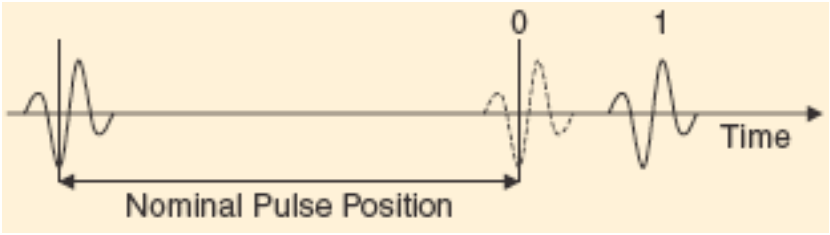


Figure 5.14: Binary pulse-position-modulation.

Only binary modulation schemes were explored for the Intelligent Tire system, since complex modulations would also increase power consumption due to more complex architectures. Specifically, pulse-position-modulation (PPM) was selected to carry the information at a data-rate of 10 Mbps. The data-rate is based on the sampling frequency of the tire sensors, the encoding scheme, as well as the packet structure, as described in [61]. For PPM, information is conveyed via the position of a pulse in the time domain with respect to a specific location, as illustrated on Figure

5.14. With respect to other binary modulation schemes, PPM is more robust to channel noise than most PAM systems. The bit detection process is simple; however, it requires careful synchronization between the transmitter and the receiver since the locations of the '0' bit and '1' bit are critical for this modulation scheme. Luckily, UWB signals in the ITS channel have a wide delay spread relative to its pulse width due to the abundance of multi-path components, which helps relax the synchronization requirements. However, synchronization must still be on the order of 10s of nanoseconds. Compared to BPSK, PPM allows the use of non-coherent receiver architectures such as energy detection receiver since the phase of the incoming signals does not need to be tracked, which simplifies the complexity of the receiver architecture.

5.3 System Construction

5.3.1 Receiver Specifications

The ITS application requires the bit-error-rate (BER) of transmission to be less than 10^{-3} so that the packet-error-rate (PER) is much less than 1%. With PER of less than 1%, the medium-access-control (MAC) protocol is designed to be robust against any transmission errors that may occur during a single wheel cycle. In [71], a detailed analysis of the BER for UWB PPM modulation was studied, showing that for BER of 10^{-3}, an EbN0 (energy-per-bit to noise ratio) of 11 dB is required. From the EbN0 ratio, the required SNR can be determined for the system output to achieved the required BER.[72]

$$SNR(dB) = \frac{E_b}{N_0}(dB) + 10 \cdot log_{10}\frac{DR}{BW} \tag{5.3}$$

where DR and BW is the data-rate and bandwidth of the system, respectively. Thus, this system need to achieve an SNR of -6 dB. From this SNR figure, the required sensitivity and noise figure of the system can be represented as:

$$\begin{aligned} Sensitivity(dBm) &\leq P_{RX} - Margin \\ &\geq SNR_{required}(dB) + [-174\,dBm + 10 \cdot log_{10}BW + NF + NF_{channel}] \\ &\leq -56dBm \\ &\geq -93\,dBm + NF(dB) + NF_{channel}(dB) \end{aligned} \tag{5.4}$$

where P_{RX} is the maximum expected signal power at the receiver antenna, -50 dBm for the ITS channel, with a $Margin$ of 6 dB. NF is the noise figure of the entire receiver chain, and $NF_{channel}$ is the equivalent channel noise figure taking into consideration all possible random in-band interferers. From the sensitivity of the receiver, the minimum gain for the receiver needs to bring

the received signal to the voltage level of the least-significant-bit (LSB) of the analog-to-digital converter (ADC).

$$Gain(dB) \geq LSB(dB) - Sensitivity(dB) \tag{5.5}$$
$$LSB(dB) = 10 \cdot log_{10}\frac{Vdd}{2^n}$$

where $Sensitivity$ is the RMS voltage level of the power sensitivity of the receiver, in dB, and n is the number of bits of the ADC. In addition to the out-of-band interferers in Table 5.1 and the in-band interferers accounted for in $NF_{channel}$ in Equation 5.5, the non-linearity of the system components, such as the receiver LNA or mixer, maybe also introduce in-band harmonics of out-of-band interferers, which corrupts the desired signal. Thus, the linearity of the receiver must be constrained, specifically, the strongest distortion are from third-order harmonics, as second-order harmonics are in general far away from the band of interest. The linearity requirement of the system is dictated by:

$$IIP3(dBm) = P_{in}(dBm) - \frac{IM3(dBc)}{2} \tag{5.6}$$
$$IM3(dBc) + P_{in}(dBm) < Sensitivity(dBm) \tag{5.7}$$

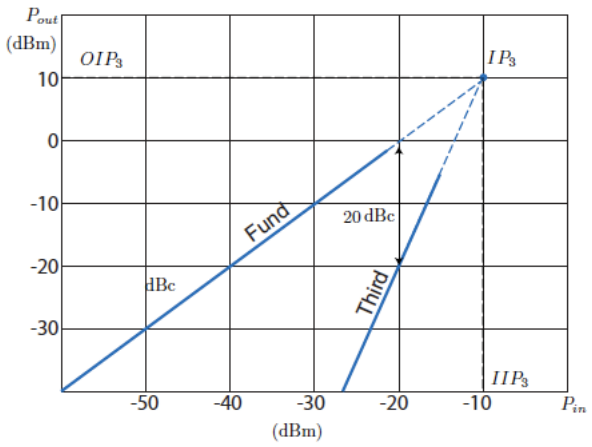


Figure 5.15: Third-order Intermodulation with IM3 of 20 dBc at P_{in} of -20 dBm.

where P_{in} is the input power of the signal, $IM3$ is the third-order intermodulation component, and $IIP3$ is the required input-referred third-order intercept point of the system. The relationship between $IM3$ and $IIP3$ is shown graphically in Figure 5.15. As shown in Equation 5.7, to avoid

receiver desensitization, I want the power contribution of the IM3 component to be lower than the sensitivity of the receiver at the input, for an assumed input power. And as mentioned, the system environment shields the receiver from other wide-band interference sources, as well as strong narrow-band interference. Again, for ITS, the maximum expected NBI P_{in} at the input of the receiver is -38 dBm, as shown in Table 5.1. The last specification for the receiver is the selectivity, which can be represented as base-band filter requirements. As seen in Table 5.1, the WiMax standard at 3.5 GHz is very near the desired signal band, 460MHz away from the center frequency of the transmitted signal. Thus, the system must provide 60 dB of attenuation in the stop-band of the down-converted base-band signal to prevent any nearby WiMax signals from corrupting the system. In addition, since the ITS signal has a 10-dB bandwidth of 500 MHz, it's 3-dB bandwidth is around 250 MHz, which require the base-band filter to have a bandwidth of 125 MHz to maximally capture the energy of the in-band signal. The overall specification for the uplink receiver system can be summarized in Table 5.2.

Specification	
Data Rate	10 Mbps
Fc	3.96 GHz
Signal Bandwidth (10dB)	500 MHz
BER	10^{-3}
Sensitivity	$\leq -56dBm; \quad \geq -93dBm + NF(dB) + NF_{channel}(dB)$
Gain	$\geq LSB(dB) - Sensitivity(dB)$
IIP3	$\geq -38dBm - \frac{Sensitivity(dBm)+38dBm}{2}$
Selectivity	60dB attenuation @ 460 MHz in Base-Band 125 MHz base-band filter 3dB-bandwidth

Table 5.2: Receiver Specifications

5.3.2 Receiver Architecture

Once the system environment and the received signal characteristics have been well-studied and modeled, a suitable architecture can be selected. The selected architecture for the ITS uplink receiver, shown in Figure 5.16, is a modification of the classical energy detection receiver that first down-converts the incoming signal band, and performs energy detection.

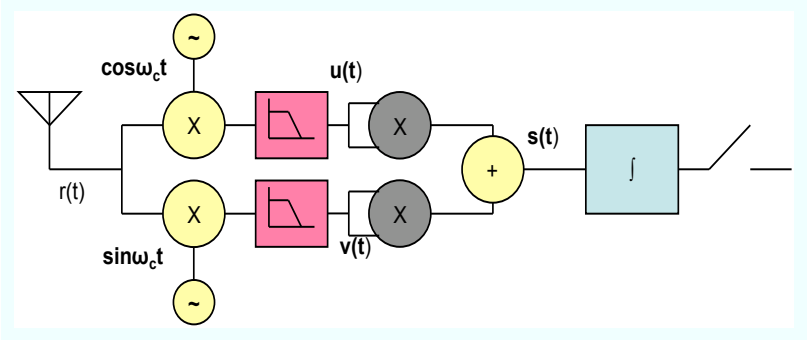


Figure 5.16: Direct-conversion energy-detection at base-band receiver for UWB detection.

Energy detection at base-band was selected because the ITS channel have a very rich and often unpredictable multi-path profile, which makes correlation-based receivers unreliable to use. Furthermore, because the system uses PPM modulation, a coherent receiver design is not necessary, since only the relative positions of each pulse need to be detected . Although energy detection receivers are prone to interferences from other signals, but the isolated location of the receivers and the rich PDP of UWB signals will help to mitigate this problem. In addition, by performing energy-detection in base-band, many higher-order interference and noise can be removed. Base-band energy detection also allow us to transfer the operation into the digital domain, without the need for an extremely fast and power-hungry ADC.

The incoming signal is first split into two paths and down-converted in I and Q channels. Thus the receiver is not sensitive to the phase of the incoming signal The two signals are then filtered to remove unwanted higher-order signals. The resulting signals are squared and added to produce the final signal. This signal is an estimate of the power of the modulating signal. The signal is finally integrated and the output is demodulated through base-band processing.

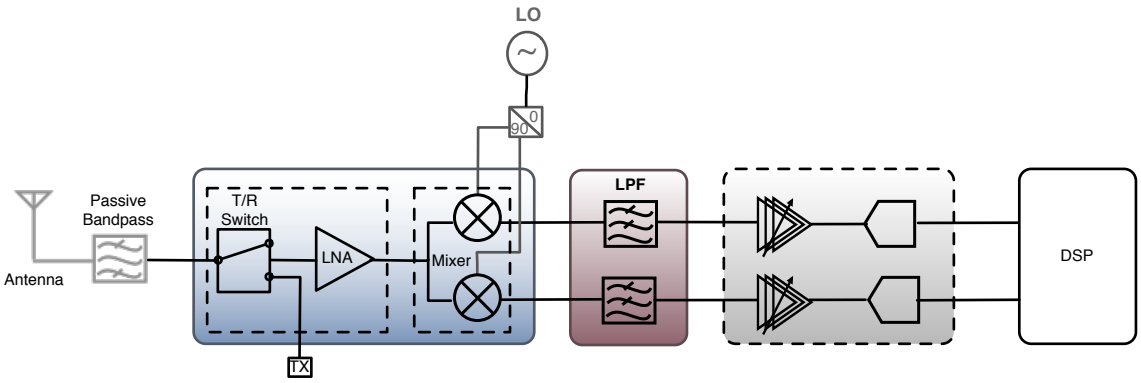


Figure 5.17: ITS Receiver Architecture.

Figure 5.17 shows the realization of the direct-conversion energy-detection receiver for the

ITS application. In this architecture instance, the system first processes the received signal using RF/analog components and performs energy detection using an on-chip digital processing core. The front-end processing system is composed of a transmit/receive switch, a low-noise-amplifier (LNA), and for each signal path, a down-converting mixers, low-pass filter (LPF), variable-gain-amplifier (VGA), and an analog-to-digital converter (ADC).

In this study, I explore the design of the receiver's analog system. Specifically, I use contract-based composition to explore the integration of LNA, Mixer, and LPF, using existing components, and use the result of this composition to incrementally drive the design constraints for the VGA and ADC. The constructed system is then validated in a virtual testbed constructed in Matlab, which allows us to incrementally verify the design using both real circuit designs and virtual components. Performances from circuit-level simulations can be annotated onto the testbed via the characterized AP components and co-simulated with parameterized virtual components. The parameters of the virtual components are then used to drive design specifications for unrealized components in the system, based on the provided guarantees of existing components, which are captured in the contracts.

5.3.3 Subsystem Construction

The basic circuit components of the receiver are reused from previous case studies discussed in Chapter 3 and 4. To quickly review, the first block, TRLNA consists of the T/R switch, the wide-band (3.1 - 4.8 GHz) input matching network, and the LNA, which features a stagger tuning technique to achieve gain flatness over the wide band. The second block, Mixer, includes a passive mixer and a low-noise buffer amplifier to boost mixer gain. Here, since I am also concerned about the interface of at the output of the Mixer block, output interface conditions and assumptions were included into the model: $Rout$, $Cout$,$Rload$, and $Cload$. The third circuit-level component, SK-Cell, consists of a differential-difference-amplifier, common-mode feedback network, and a RC feedback network to form a second-order Sallen-Key low-pass filter cell. The process technology used was 0.13μm 1.2V technology.

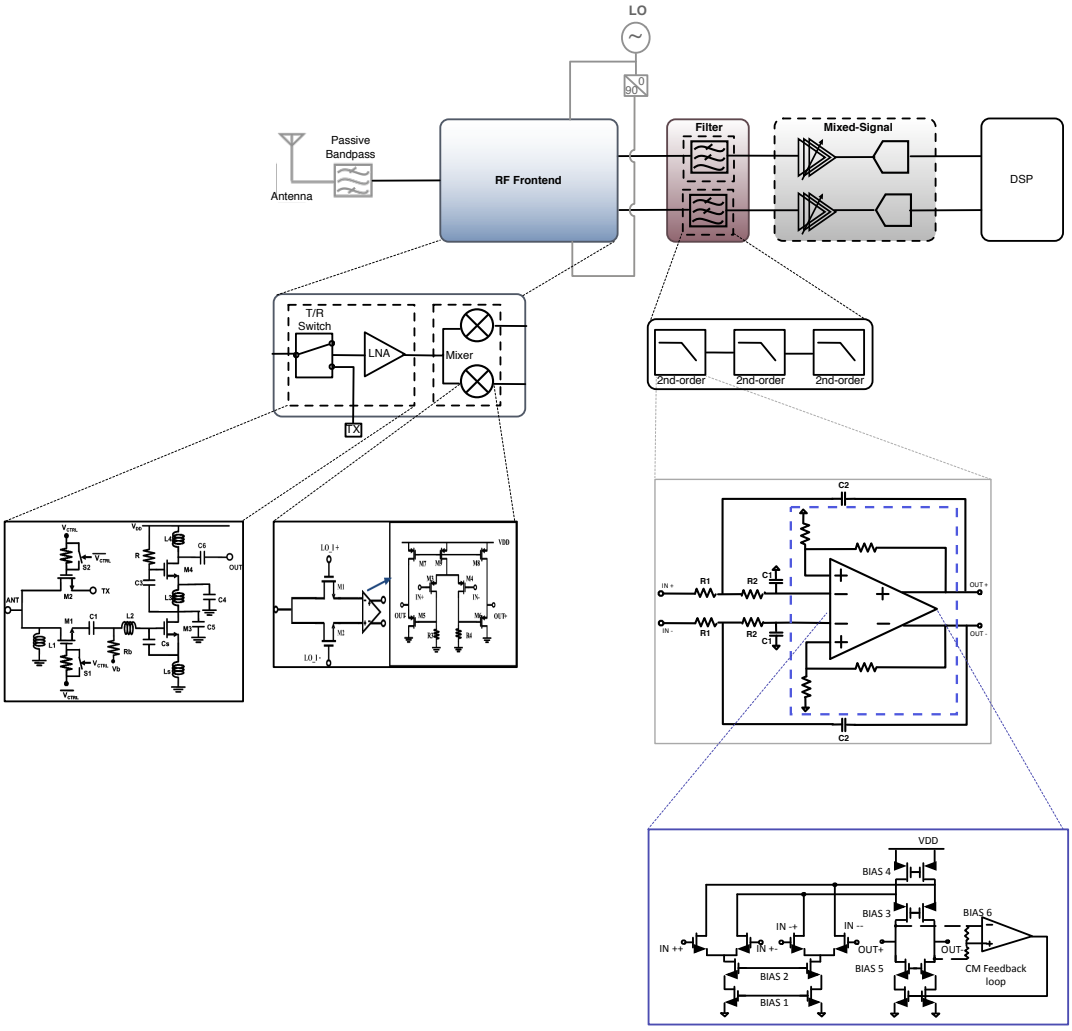


Figure 5.18: ITS Receiver Hierarchy.

The components may be composed together in a single flattened abstraction level; however, the exploration space for this approach would be unnecessarily large, and include many undesirable performance regions. Instead, I compose the circuit components into sub-systems and introduce new abstractions: the RF front-end and the Filter. Following the propagation flow illustrated in Figure 4.2, the appropriate APs of the sub-systems can be constructed. Figure 5.18 shows the complete design hierarchy of the ITS receiver.

	1	2	3	4	5	6	7	8	9	10	11	12
LNA	NF	Gain	Idc	IIP3	Rin	Cin	Rout	Cout	Rsource	Csource	Rload	Cload
Mixer	NF	CG	Idc	IIP3	Rin	Cin	Rout	Cout	Rsource	Csource	Rload	Cload

Table 5.3: Characterized performance of LNA and Mixer

Table 5.3 shows the characterized performances for the LNA and Mixer components. Note that the performance vectors slightly differ from the characterized performances in Chapter 3. This is because the dimensions of interest at the system-level is different for this study, so I abstract away the unnecessary details. As discussed in Chapter 3, before evaluating the system performance, component compatibility must be verified so that only appropriate designs are composed. Once $Rload_{LNA}$ and $Cload_{LNA}$ are checked against Rin_{Mixer} and Cin_{Mixer}, I locate the compatible component instances to compose. Again, the source loading of the Mixer did not significantly impact the Mixer performance and were enforced a-priori using a static contract check. Equations 5.8 $\sim$ 5.13 are evaluated upon finding compatible components to generate the performance of the RF subsystem component. Here, the cascade equations do not place strong assumptions on the component performances, and I do not want to over-constrain the design space, so the vertical assumptions of the RF subsystem is simply the feasibility of the component performances, which are evaluated based on the support-vector machine classifier of each component.

$$Gain_{RF}(dB) = Gain_{LNA}(dB) + CG_{Mixer}(dB) \tag{5.8}$$

$$NF_{RF}(dB) = 10 \cdot log_{10}(F_{LNA} + \frac{(F_{Mixer} - 1)}{Gain_{LNA}}) \tag{5.9}$$

$$Power_{RF} = Vdd * (Idc_{LNA} + Idc_{Mixer}) \tag{5.10}$$

$$IIP3_{RF}(dBm) = 10 \cdot log_{10}(\frac{1}{IIP3_{LNA}} + \frac{Gain_{LNA}^2}{IIP3_{LNA}}) \tag{5.11}$$

$$Rin_{RF} = Rin_{LNA}; \quad Cin_{RF} = Cin_{LNA} \tag{5.12}$$

$$Rout_{RF} = Rout_{Mixer}; \quad Cout_{RF} = Cout_{Mixer} \tag{5.13}$$

where F is the noise factor of each component, and $Gain$ and $IIP3$ are in linear domain unless specified as dB. The horizontal interface assumptions of the LNA and Mixer are propagated into interface assumptions of the subsystem, as seen in Equations 5.14 and 5.15.

$$Rs_{assume\_RF} \Leftarrow Rs_{assume\_LNA}; \quad Cs_{assume\_RF} \Leftarrow Cs_{assume\_LNA} \tag{5.14}$$

$$Rl_{assume\_RF} \Leftarrow Rl_{assume\_Mixer}; \quad Cl_{assume\_RF} \Leftarrow Cl_{assume\_Mixer} \tag{5.15}$$

where I require

$$(Rs_{Assume} - \delta_{RsourceRF}) < Rsource_{RF} < (Rs_{Assume} + \delta_{RsourceRF}) \tag{5.16}$$
$$(Cs_{Assume} - \delta_{CsourceRF}) < Csource_{RF} < (Cs_{Assume} + \delta_{CsourceRF}) \tag{5.17}$$
$$Rload_{RF} > Rl_{assume} \tag{5.18}$$
$$Rload_{RF} \gg Rout_{RF} \tag{5.19}$$
$$(Cl_{Assume} - \delta_{CloadRF}) < Cload_{RF} < (Cl_{Assume} + \delta_{CloadRF}) \tag{5.20}$$

where δs here are 5% of the assumed values.

	1	2	3	4	5	6	7	
SK	NF	Gain	Idc	BW(3dB)	Q	w0	Gain(460MHz)	
	8	9	10	11	12	13	14	15
	Rin	Cin	Rout	Cout	Rs_{assume}	Cs_{assume}	Rl_{assume}	Cl_{assume}

Table 5.4: Characterized performance of 2nd-order Sallen-Key Lowpass Filter Cell

Table 5.4 shows the set of performances characterized for the Sallen-Key cell. The design and composition of the Sallen-Key cell is the same as the one presented in Chapter 4, with two main modifications. First, the process technology used in this study is 130nm. In addition, the unity-gain DDA was modified to include resistive pairs in the inner feedback loop to provide additional gain to the receiver chain at each stage of the LPF.

Similar to the performance models of the LNA and Mixer, the SK performance model contains performance (1∼7) and interface contract variables (8∼15). NF and Idc are used to analytically derive the performance of the LPF in composition, similar to the RF front-end characterization. Performances $Gain, Q$, and ω_0 are used to annotate the simplified behavioral model (Equation 5.21) of the SK cell, where Q and ω_0 are the quality-factor and the resonant frequencies of the SK cell, respectively.

$$H_{SK} = \frac{Gain_{SK}}{(\frac{s^2}{w_{0SK1}^2} + \frac{s}{w_{0SK1} * Q_{SK1}} + 1)} \tag{5.21}$$

where $Gain_{SK}$ is the gain provided by the DDA, and the bandwidth of the DDA is assumed to be greater than the bandwidth of the Sallen-Key. The 3db-BW and $Gain(460MHz)$ can be used to validate the model. Figure 5.19 shows the comparison of the frequency response of the SK cell between the simplified behavioral model (Equation 5.21) in blue and detailed SPICE simulations in red, for 20 different randomized SK design instances. Figure 5.20 shows the details of the comparison for a single design. It can be observed that within the frequency regions of interest (between 1-1000 MHz) that was characterized, the model matches circuit simulations extremely well.

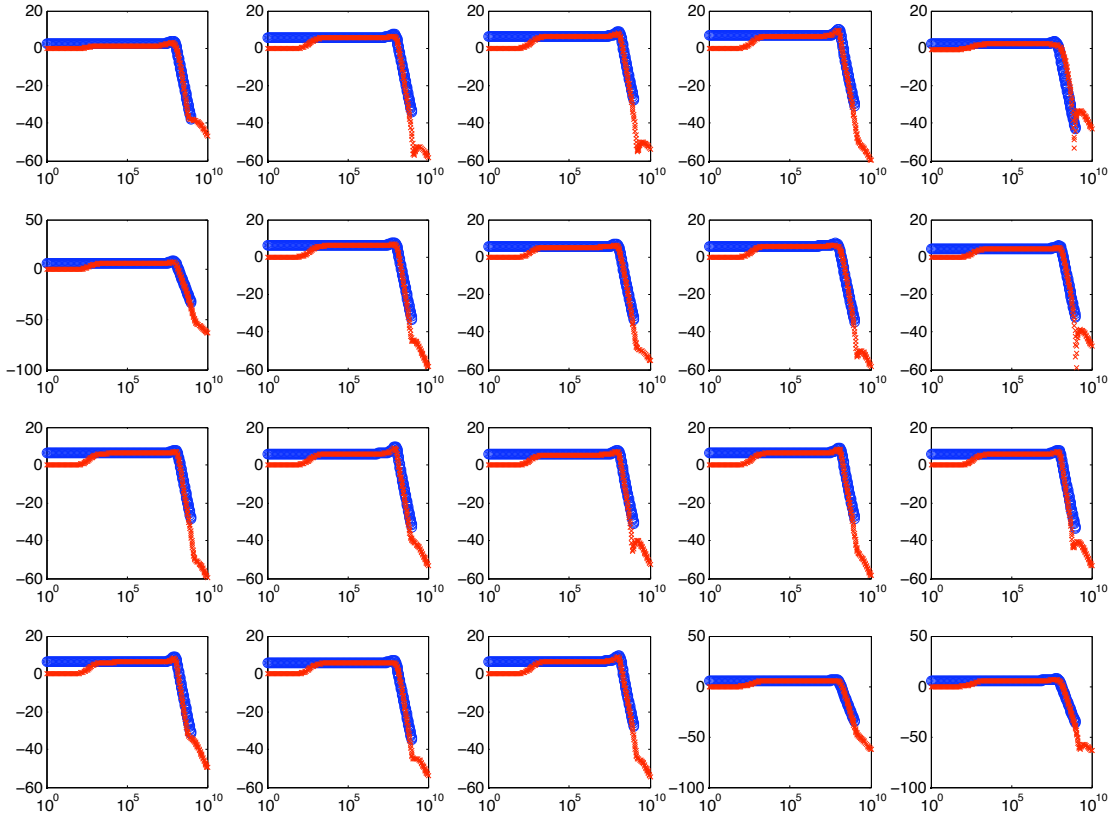


Figure 5.19: Comparison of Sallen-Key behavioral model (Blue) and SPICE simulation (Red) with different designs.

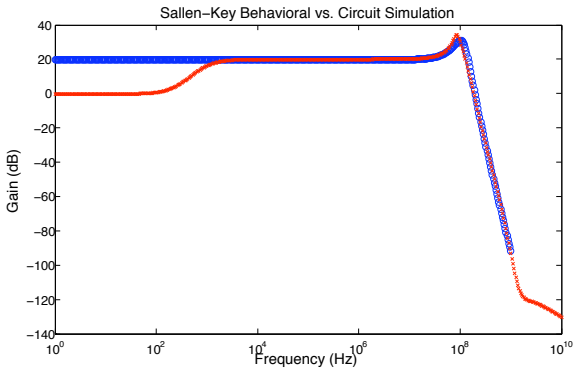


Figure 5.20: Comparison of Sallen-Key behavioral model (Blue) and SPICE simulation (Red) for single design instance.

The composition of the DDA and the RC feedback network into SK cells has already been discussed in Chapter 4, I focus the discussion here on the composition of SK cells into the base-band lowpass filter needed for the receiver. The horizontal interface assumptions of the Sallen-Key component are as follows:

$$Rsource_{SK} < Rs_{assume} \tag{5.22}$$
$$Csource_{SK} < Cs_{assume} \tag{5.23}$$
$$Rload_{SK} \gg Rout_{SK} \tag{5.24}$$
$$Rload_{SK} \geq Rl_{assume} \tag{5.25}$$
$$(Cl_{assume} - \delta_{Cload}) < Cload_{LPF} < (Cl_{assume} + \delta_{Cload}) \tag{5.26}$$

Here, the source loading of the SK cell does not significantly impact the performance of the component as long as they are less than the assumed interface values during characterization, where Rs_{assume} is set to be much lower than the $R1$ value of the SK cell during characterization. The loading of the SK cell is assumed to be high-impedance, much greater than the output impedance of the SK cell, and the loading capacitance of the component must be within a +/-δ_{Cload} margin of Cl_{assume}, where δ_{Cload} is 10% of the assumed value.

In addition to horizontal interface assumptions, there also exists vertical assumptions placed on the SK cells by the LPF subsystem. Unlike in Chapter 4, where vertical assumptions were placed to avoid non-ideal regions from being explored at the system-level, the vertical assumption here are used to find the desired regions for exploration.

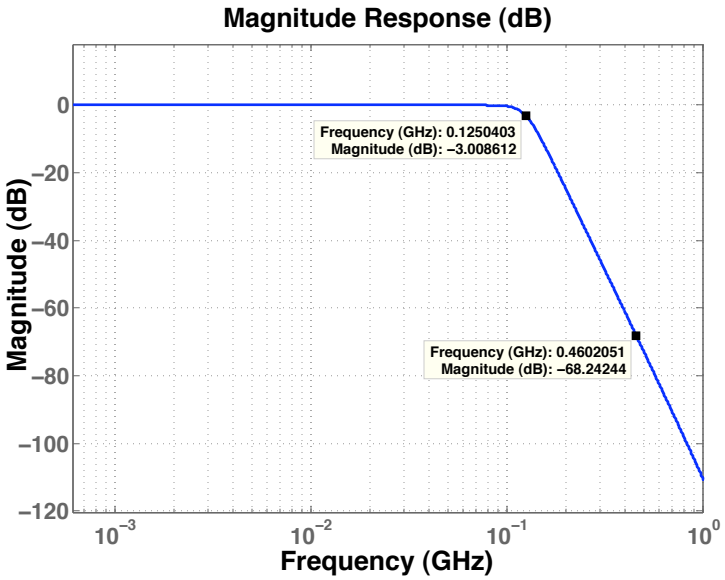


Figure 5.21: Base-band Filter Mask

As mentioned in Section 5.3.1, the selectivity of the receiver is determine by the pre-select filter before the LNA and the base-band filter. Specifically, the base-band filter must fit in a frequency mask (Figure 5.21) to provides a 3-dB bandwidth of 125MHz and a stop-band attenuation of 60 dB at 460MHz? with respect to base-band gain. Thus, we're not interested in composing all possible SK cell designs together, but rather, only consider the designs that will compose to form a lowpass filter that fits well within the mask. To determine the vertical assumptions on the SK cells, I use the following steps:

1. Determine minimum filter order and number of 2nd-order cell stages.
2. Find required poles and zeros of each ideal filter stage.
3. Obtain assumption constraints for performance of each component.

There are many filter design tools available for this. Here, I use Matlab's *fdatool*. In the ideal situation, a 3-stage 6^{th}-order Butterworth lowpass filter is needed to meet the mask of Figure 5.21. From the poles determined for each stage, I can find the necessary Q and the resonant frequency (ω_0) needed at each stage, where the Q is determined from Equation 5.27 and shown in Table 5.5 for each stage.

$$Q = \frac{|pole|}{2 \cdot Re(pole)} \tag{5.27}$$

	Q	ω_0
Stage 1	0.5176	$2\pi\cdot$ 125 MHz
Stage 2	0.707	$2\pi\cdot$ 125 MHz
Stage 3	1.932	$2\pi\cdot$ 125 MHz

Table 5.5: Required Q and Bandwidth for Low-pass Filter Subsystem.

Since the receiver architecture used is energy detection, ripples or peaks are allowed in the passband without dramatically degrading the performance of the receiver. The Q and ω_0 are not absolute requirements, but rather, can be used as inequality constraints to isolate designs of interest. Specifically, I want

$$Q_{SK} > Q_{assumed} \tag{5.28}$$

$$(\omega_{0assumed} - \delta_{\omega 0}) < \omega_{0SK} < (\omega_{0assumed} + \delta_{\omega 0}) \tag{5.29}$$

ω_{0SK} is constrained to be within δ margin of the assumed value, where δ here is 5% of the assumption, since a simple lower-bound constraint could cause the final constructed filter to have a stop-band attenuation of less than 60 dB. Once components satisfy both horizontal and vertical assumptions, the performance and behavior of the composed LPF can be estimated from:

$$Power_{LPF} = Vdd * (Idc_{SK1} + Idc_{SK2} + Idc_{SK3}) \tag{5.30}$$

$$NF_{LPF}(dB) = 10 \cdot log_{10}(F_{SK1} + \frac{(F_{SK2} - 1)}{Gain_{SK1}} + \frac{(F_{SK3} - 1)}{Gain_{SK2} * Gain_{SK1}}) \tag{5.31}$$

$$H_{LPF} = \frac{Gain_{SK1} * Gain_{SK2} * Gain_{SK3}}{(\frac{s^2}{w_{0SK1}^2} + \frac{s}{w_{0SK1} * Q_{SK1}} + 1) * (\frac{s^2}{w_{0SK2}^2} + \frac{s}{w_{0SK2} * Q_{SK2}} + 1) * (\frac{s^2}{w_{0SK3}^2} + \frac{s}{w_{0SK3} * Q_{SK3}} + 1)} \tag{5.32}$$

$$Rin_{LPF} = Rin_{SK1}; \quad Cin_{LPF} = Cin_{SK1} \tag{5.33}$$

$$Rout_{LPF} = Rout_{SK3}; \quad Cout_{LPF} = Cout_{SK3} \tag{5.34}$$

Figure 5.22 and 5.23 shows the comparison between the simplified behavioral model and circuit simulations, which again match quite well within the frequency region of interest.

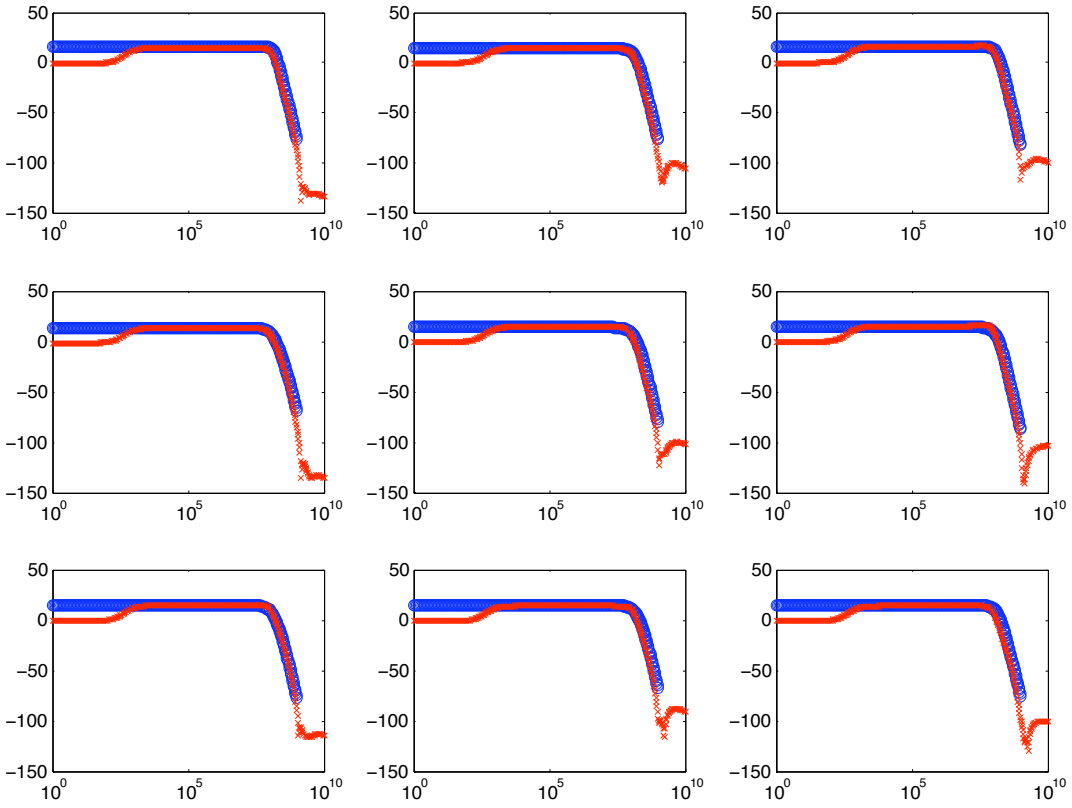


Figure 5.22: Comparison of LPF behavioral model (Blue) and SPICE simulation (Red) with different designs.

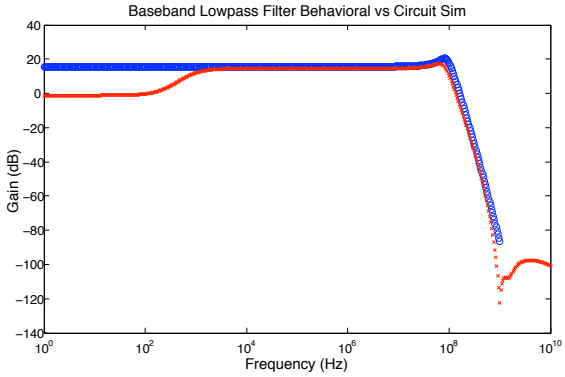


Figure 5.23: Comparison of LPF behavioral model (Blue) and SPICE simulation (Red) for single design instance.

The interface assumptions of the composed LPF is propagated from the SK AP components, under the same conditions as previously described:

$$Rs_{assume\_LPF} \Leftarrow Rs_{assume\_SK1}; \quad Cs_{assume\_LPF} \Leftarrow Cs_{assume\_SK1} \tag{5.35}$$

$$Rl_{assume\_LPF} \Leftarrow Rl_{assume\_SK3}; \quad Cl_{assume\_LPF} \Leftarrow Cl_{assume\_SK3} \tag{5.36}$$

Table 5.6 and 5.7 shows the extracted performances for the RF and LPF subsystems to be used in the composition of the UWB receiver. Figures 5.24 and5.25 illustrates the projected feasibility regions for the characterized performance spaces of the RF and LPF subsystems.

	1	2	3	4	5	6	7	8	9	10	11	12
RF	Gain	Power	NF	IIP3	Rin	Cin	Rout	Cout	Rs_{assume}	Cs_{assume}	Rl_{assume}	Cl_{assume}

Table 5.6: Characterized performance of RF Frontend Subsystem

	1	2	3	4	5	6	7	8	9	10	11	12	13
LPF	Gain	BW	Power	Noise	Attenuation	Rin	Cin	Rout	Cout	Rs_{assume}	Cs_{assume}	Rl_{assume}	Cl_{assume}

Table 5.7: Characterized performance of LPF Subsystem

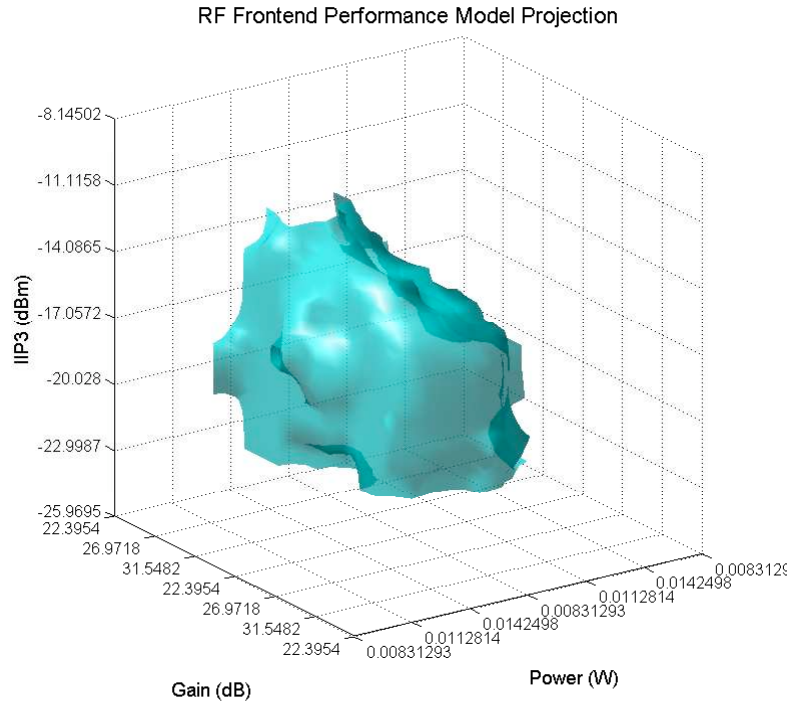


Figure 5.24: Projection of RF Front-end AP Component Model.

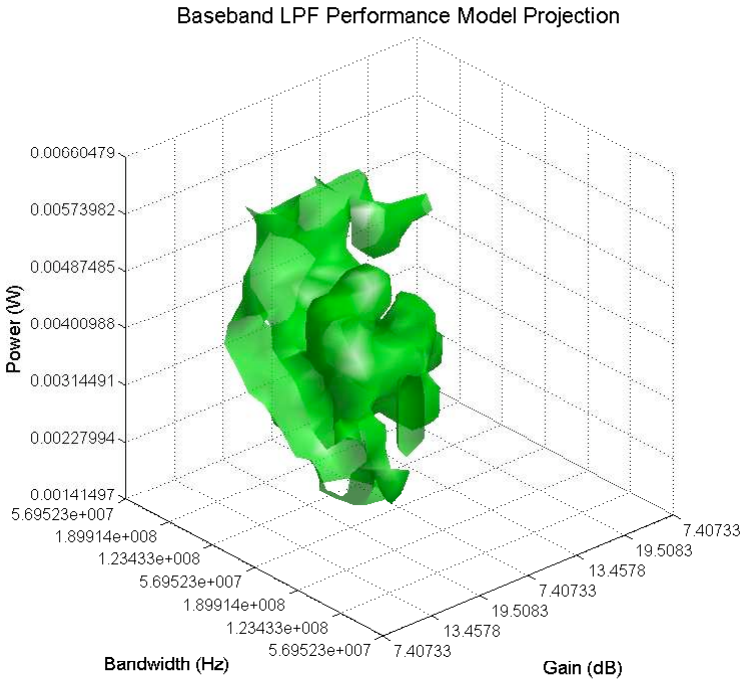


Figure 5.25: Projection of LPF AP Component Model.

5.3.4 System Exploration

With the subsystem APs constructed, system exploration of the UWB receiver system follows the same process as described in Chapters 3 and 4. First, I check contract assumptions to locate subsystem compatible designs. In this case, system-level composition is a cascade composition of components similar to the case study in Chapter 3.

Figure 5.26 illustrates the projection of the RF and LPF AP performance models into the corresponding performance dimensions at the interface of the system composition. The grid slices correspond to selected assumption conditions for the RF and LPF sub-systems, respectively. Here, I can clearly observe an example of how contracts partition the exploration space and focus the optimization engine only in the region of interest. Remember that for each AP, assumptions are characterized as a continuous space, with corresponding guarantee spaces. Thus, each selected point in the assumption space would generate a distinct partition in the guarantee space for the compatible region. It can also be observed that the quality and efficiency of the optimization algorithm heavily depends on how well the provided APs correspond to existing contract assumptions in the composition. If the compatible region is small, then it can be expected that locating compatible designs would be very time consuming.

Once a pair of compatible component design is located, the system-level behavioral models can be evaluated to provide performance estimations for the system constructed from the selected designs. Equations 5.37 $\sim$ 5.43 are the system-level performance behavioral equations, and Equations 5.44 and 5.45 show the propagation of sub-system interface assumptions into system-level.

$$Gain_{RX}(dB) = Gain_{RF}(dB) + Gain_{LPF}(dB) \tag{5.37}$$

$$NF_{RX}(dB) = 10 \cdot log_{10}(F_{RF} + \frac{(F_{LPF} - 1)}{Gain_{RF}}) \tag{5.38}$$

$$Power_{RX} = Power_{RF} + Power_{LPF} \tag{5.39}$$

$$IIP3_{RX}(dBm) \simeq IIP3_{RF} \tag{5.40}$$

$$BW_{RX-Baseband} = BW_{LPF} \tag{5.41}$$

$$Rin_{RX} = Rin_{RF}; \quad Cin_{RX} = Cin_{RF} \tag{5.42}$$

$$Rout_{RX} = Rout_{LPF}; \quad Cout_{RX} = Cout_{LPF} \tag{5.43}$$

$$Rs_{assume\_RX} \Leftarrow Rs_{assume\_RF}; \quad Cs_{assume\_RX} \Leftarrow Cs_{assume\_RF} \tag{5.44}$$

$$Rl_{assume\_RX} \Leftarrow Rl_{assume\_LPF}; \quad Cl_{assume\_RX} \Leftarrow Cl_{assume\_LPF} \tag{5.45}$$

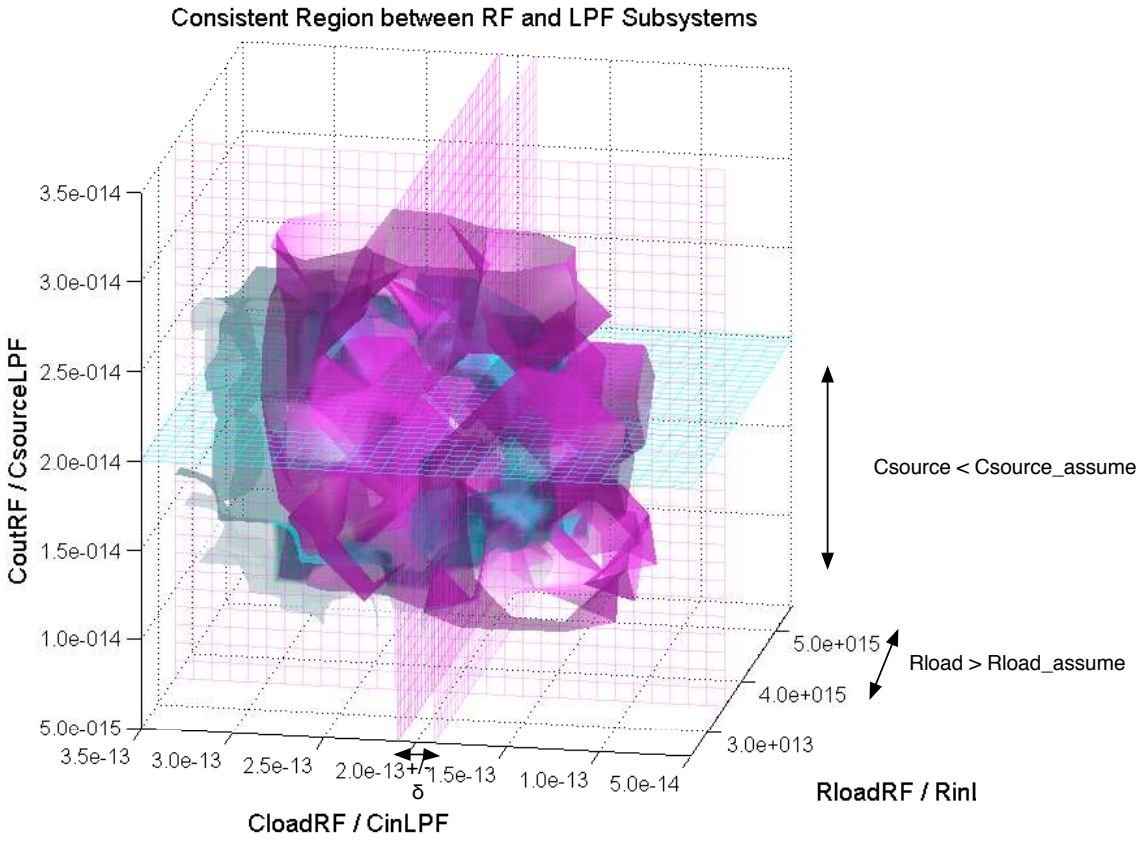


Figure 5.26: Combined Projections of RF (magenta) and LPF (cyan) AP models onto interface variables to show potential compatible regions.

Here, the base-band filter is assumed to operate in the linear region, thus non-linearity of the system is dominated by the non-linearity of the RF front-end subsystem. In addition, since I know that the LNA and mixer performance actually covers a wide bandwidth (designed for 3.1-4.8 GHz as discussed in [29]), the bandwidth of the receiver is dictated by the bandwidth of the base-band filter. In fact, these are static vertical assumptions that should be checked against the provided APs prior to composition considerations. Based on the evaluated values of the system performances, the system is optimized by evaluating a weighted-sum cost function of the general form:

$$Cost = \sum_{i} \alpha_i * Perf_i \tag{5.46}$$

where α_i are the corresponding weights for each performance. Depending on the values of the weights, I can optimize the system for optimal Noise, Power, Gain, IIP3, etc, or some combination

of performance criteria. Of course a more sophisticated cost function maybe chosen if a specific system characteristic is desired, for example, adjustable weighting functions (e.g.$tanh$) maybe used to adjust the impact of each performance to the overall system cost, depending on their value.

Once the optimal system configuration is selected, I can propagate this configuration to the circuit level by recursively performing a k-nearest-neighbor (KNN) search on the characterization space of each AP at each level. Again, this is not an exact mapping procedure, as one-to-one mapping from system performance space back to configuration space is still an open problem and is not addressed in the scope of this work. However, the set of NN configurations provide a good reference point for circuit designers to refine the circuit parameters to match system-level optimization results.

5.4 Results

Table 5.8 shows the optimization results for the various optimization objectives for the receiver system, and Table 5.9 shows their respective estimation errors, with respect the circuit-level simulations of the optimized configurations. The optimization runtime shown in Table 5.8 are the times for generation and optimizing over 1000 compatible design configurations for the receiver. Notice that the runtime for system optimization for this case were better than the runtime reported in previous chapters due the presence of more compatible designs in the APs at the subsystem level, which primarily resulted from careful pruning during characterization based on prior knowledge about the system. Also notice the additional hierarchy in the system did not impact the runtime performance of the optimization, since the APs already propagated the necessary physical information to the system level, and the KNN configuration mapping step was done only once on the optimized system configurations. Of course, initial overhead time is required to prepare the APs for various abstraction levels, as with any other design reuse methodology. But the benefit is that the APs can be used in the design and scaffolding of many other applications without the need to simulate or tune at the circuit-level.

	Gain	Power	BW	NF	IIP3	Attenuation @ 460 MHz	Optimization Runtime
Min Noise	42 dB	18.6 mW	125 MHz	**3.46 dB**	-19 dBm	-64 dB	2.16 min
Min Power	45.8 dB	**13.6 mW**	128 MHz	4.14 dB	-21 dBm	-59 dB	2.22 min
Max IIP3	40 dB	14.5 mW	126 MHz	4.58 dB	**-11.6 dBm**	-62 dB	1.87 min
Max Attenuation	43 dB	17.4 mW	129 MHz	4.76 dB	-15.2 dBm	**-77 dB**	2.28 min
Max Gain	**51 dB**	20.0 mW	127 MHz	3.88 dB	-19.2 dBm	-56.8 dB	2.31 min

Table 5.8: Optimization results for various objectives.

	Δ Gain	Δ Power	Δ BW	Δ NF	Δ IIP3	Δ Attenuation @ 460 MHz
Min Noise	0.40 dB	-0.57 mW	-22 MHz	-0.29 dB	2.18 dB	-2.69 dB
Min Power	0.49 dB	-0.29 mW	-10 MHz	-0.49 dB	1.52 dB	-6.57 dB
Max IIP3	0.71 dB	-0.21 mW	5 MHz	-0.05 dB	2.76 dB	-4.17 dB
Max Attenuation	0.39 dB	-0.06 mW	-6 MHz	-0.14 dB	5.61 dB	-8.06 dB
Max Gain	0.63 dB	-0.21 mW	-20 MHz	-0.13 dB	2.24 dB	1.71 dB

Table 5.9: System prediction error of optimization results compared with circuit simulation results using mapped circuit configurations.

	$Gain_{VGA}$	$NF_{Channel} + NF_{Mix}$
Min Noise	16 dB	29.5 dB
Min Power	12 dB	28.8 dB
Max IIP3	18 dB	28.4 dB
Max Attenuation	15 dB	28.2 dB
Max Gain	7 dB	29.1 dB

Table 5.10: Implication for VGA design and channel NF.

Assumptions	
Data Rate	10 Mbps
BER	10^{-3}
Sensitivity	-60 dBm
ADC Type	3-bit; V_{FS}: 200mV; Input impedance $\geq 1M\Omega$
Antenna Impedance	50 Ω

Table 5.11: Receiver environment assumptions during optimization

For all objectives, I assume the receiver drives a 3-bit ADC with 200mV full-scale input voltage (+/- 100mV) and high input-impedance. As mentioned on Section 5.3.1, I aim to achieve a BER of 10^{-3}, which requires EbNo of 11dB. For ADCs, the SQNR per bit is roughly:

$$SQNR = 6.02 \cdot N + 1.76dB \tag{5.47}$$

Thus, with 3-bits, the SQNR of the ADC is 19.82 dB, which achieves the requirements, while leaving enough margin for errors. In fact, a 2-bit ADC would also be viable,but the error margins would be lower. The LSB voltage of the assumed virtual ADC is 25 mV. The sensitivity of the

receiver was set to be -60 dBm, and the maximum NBI P_{in} was assumed to be -38 dBm. From the receiver requirements in Table 5.2, the system needs to meet:

$$Gain_{RX}(dB) \geq LSB(dBm) - Sensitivity(dBm) = 58dB \tag{5.48}$$
$$NF_{Channel}(dB) \leq 33dBm - NF_{RX}(dB) \tag{5.49}$$
$$IIP3(dBm) \geq -27dBm \tag{5.50}$$
$$\tag{5.51}$$

where $NF_{Channel}$ is the equivalent noise figure of the UWB channel, which includes contributions from random in-band interference and spurious noise, and can be measured by taking the difference between the SNR at the transmitter antenna and the SNR at the receiver antenna. Note that this can be used as part of a contract by application engineers. NF_{Mix} is the equivalent input-referred noise figure of the mixed-signal circuitry, including the VGA and ADC. Due to the high gain of the analog front-end system, the noise contribution from the mixed-signal circuits is relatively small, with exception of SQNR, as already mentioned. $Gain_{RX}$ can be used to determine the required gain between the output of the LPF and the ADC input. The IIP3 constraint is directly in the optimization problem formulation. Table 5.10 shows the implications of the optimization results to specify the design of currently unrealized virtual components (VGA), as well as the assumed channel environments.

	Gain	Power	BW	NF	IIP3	Attenuation @ 460 MHz
Mean	0.6 dB	0.2 mW	14 MHz	0.18 dB	2.06 dB	6 dB
Variance	1.24 dB	0.3 mW	18 MHz	0.15 dB	1.66 dB	8 dB

Table 5.12: Average and variance of accuracy for system performance estimation over 1000 different design configurations.

As seen in Table 5.9, Gain, Power, and NF have very low approximation error since they are primarily impacted by first-order terms. However, for bandwidth, IIP3, and stop-band attenuation, approximation errors were more significant due to greater dependence on higher-order terms that were not characterized by the contracts or the behavioral models in this case study. Even the presence of significant approximation error, circuit-level simulation of the final system still satisfied the constraints on IIP3 and stop-band attenuation, since additional margin were accounted for during specification. For bandwidth, the final system performance were greater than or close the 125 MHz requirement, thus, very little relevant energy content were lost. For the unsatisfied circuit designer, the circuit configuration from the optimization output is a very good starting point to tune the circuit topology to match the desired performance of the optimal configuration.

Figure 5.27 illustrates the optimization trace and configuration mapping for the Min Power objective. The optimized system configuration is mapped onto the NN configurations stored in the

AP of the RF and LPF subsystems. Then, for each NN mapping, there's a direct component-level configuration that can be mapped onto each of the components, which in turn is translated into circuit configurations.

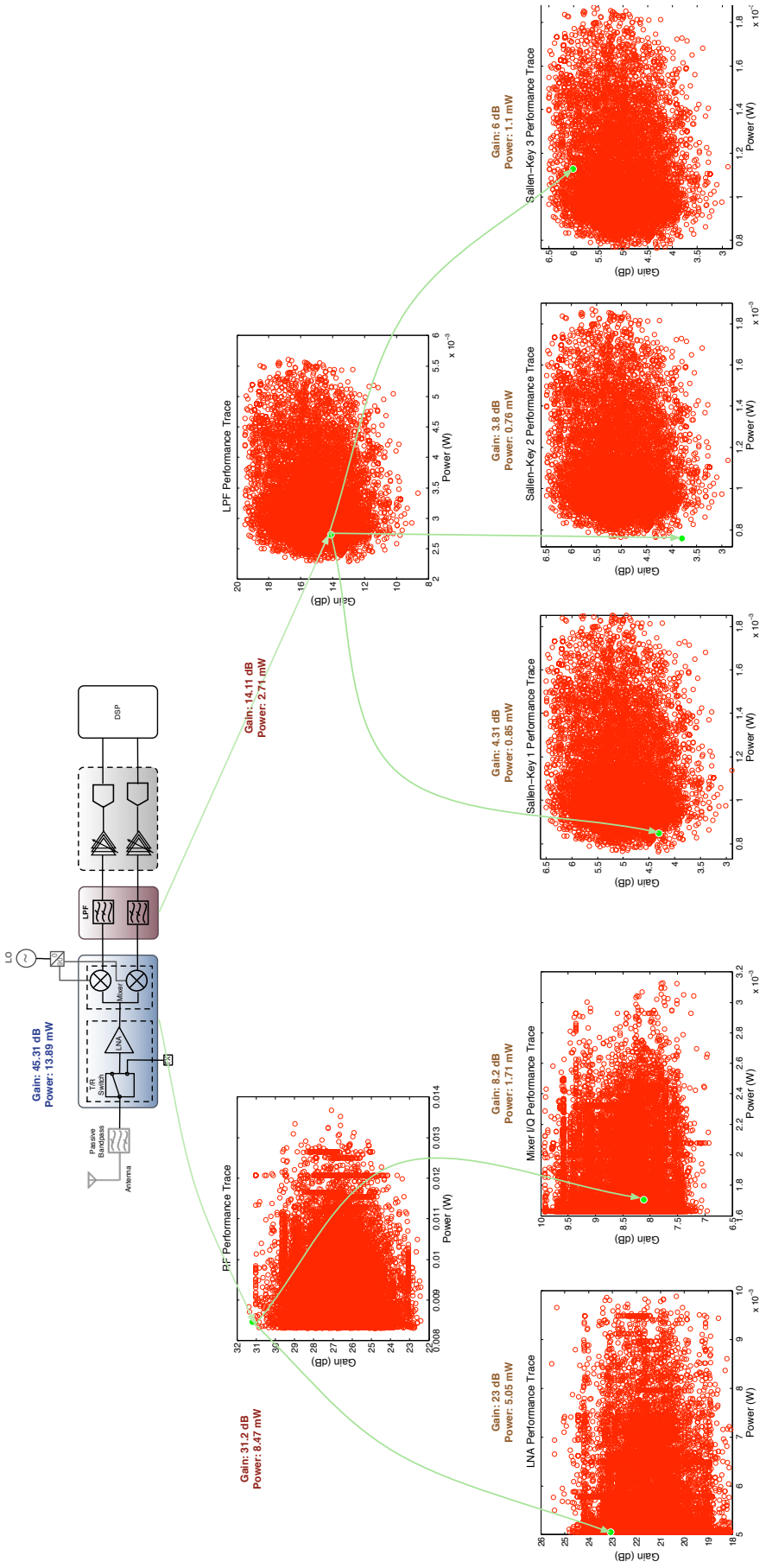


Figure 5.27: Optimization Trace for Min Power (projected onto Gain and Power dimensions).

Finally, I verify that the system is working properly in the transient domain by comparing circuit simulations with the system-level behavioral model built in Matlab. As shown in Figure 5.28, even in the presence of strong NBI, the filtered base-band signal closely matched the expected signal pattern at the system behavioral level, without any form or training or fitting of the behavioral model. Table 5.13 shows quantitative figures of the transient error, which are the RMS error of the comparison between the output signals (in time domain) of the behavioral model and the circuit transient simulation for 1000 UWB pulses. As shown, without NBI, the RMS error is 4 $mV_{\overline{RMS}}$, while with NBI, the RMS error nearly doubles to 7 $mV_{\overline{RMS}}$, given a peak signal voltage of about 40 mV. This was enough to preserve the BER behavior of the receiver at the system level, as both circuit simulation and Matlab showed BER of less that 10^{-3}. (0 demodulation error for 1000 randomly generated pulses.) Here, demodulation was performed in using virtual component models in the digital domain, based on the detection architecture illustrated in Figure 5.16.

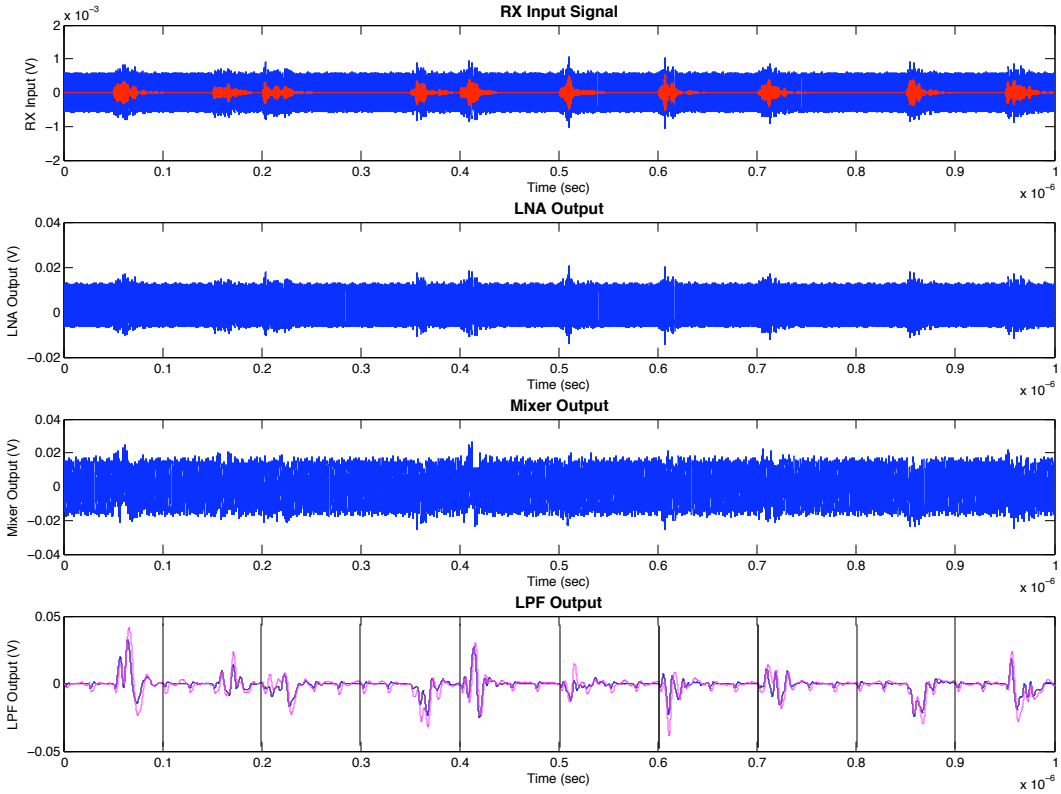


Figure 5.28: Time-domain plots of signal propagation (with NBI) in Receiver, compared against transient simulations in SPICE. (blue) Total Signal (red) Desired Signal (magenta) SPICE simulation output.

Input Signal Characteristic	RMS Error of Transient ($V_{\overline{RMS}}$)
Pathloss and multi-path interference only	0.004
Pathloss, multi-path interference, and NBI (Bluetooth, Wifi, WiMax, UNII Low, and UNII High)	0.007

Table 5.13: Optimization Results for Various Objectives

To compare the results of this work with other recently published receivers with similar design specifications, I list the energy per bit, data rate, and power of each system in Table 5.14, where the reported power consumption from this work is from circuit-level simulations. However, it should be noted that this is a very rough comparison and should be used merely as a frame of reference, as it is very difficult to compare systems built for different modulation, data-rate, and application requirements.

	Energy/Bit (nJ/bit)	Data Rate (Mbps)	Power(mW)
This work Min Noise	1.917	10	19.17
This work Min Power	1.389	10	13.89
This work Max IIP3	1.471	10	14.71
This work Max Attenuation	1.766	10	17.66
This work Max Gain	2.021	10	20.21
Ref. [73]	0.68	480	330
Ref. [74]	17	1	17
Ref. [75]	n/a	n/a	81
Ref. [76]	1.44	20	29
Ref. [77]	2.5	14.3	35.8

Table 5.14: Comparison of Receiver Performance with Literature.

This chapter demonstrated the application of contract-based system composition on the complete UWB receiver system for the ITS application, which includes:

- Application specification
- System modeling and architecture selection
- System specification
- Component characterization and contract specifications
- System optimization
- System validation

The optimized performances are comparable with literature and meet the application specifications. The resulting circuit configurations are ready to be transferred to the circuit designers for

either further fine-tuning and/or physical layout. Because the APs used in system exploration already contained lower level assumption and performance information, we've effectively minimized the risk of design iterations in the design flow. The resulting system performance can also be used to derive specification of unrealized virtual components in the system model, in this case, the VGA and the ADC. Since linear inequality relations and first-order models were used for contract assumptions, the estimation accuracy were good for linear and first-order terms, whereas nonlinear terms such as bandwidth or stop-band attenuation had higher errors. The higher error were offset by higher margins accounted for in the constraint formulation for the system optimization problem. This chapter is meant as an application reference for future adoptions of contract-based analog design.

Chapter 6

Conclusion

With the scaling of CMOS technology near its physical limits, additional advancements in electronics are increasingly dependent on design space exploration at the system-level. Although significant progress has been made in the digital domain to raise the level of abstraction, with the introduction of Transaction-Level Modeling, high-level synthesis techniques, and IP reuse, design in the analog domain have mostly remained in the circuit and layout level, heavily dependent on manual efforts from the designer. However, as electronics become more immersed in the physical world, an explosive growth in the number of new applications that require analog/RF/mixed-signal systems is expected with a wide variety in design specifications.

Analog systems are now the bottleneck in both design and verification phases of new electronic applications. New design methods must be introduced to deal with the greater demand for increased productivity of analog designers. This dissertation specifically targets the area of analog design reuse by proposing a method for analog system characterization and composition using contracts. Leveraging analog platform-based design (APBD), pre-characterized analog IP components, analog platforms (AP), are characterized under a set of assumptions to produce a set of performance guarantees, which form analog contracts for the AP. Using analog contracts, systems are composed together to satisfy design requirements, and the resulting system design is guaranteed to be correct-by-construction (within error margin δ) through validation of contracts for each AP component.

In this research, the use of contracts for analog composition is explored in a progressive case-study for the construction of an ultra-wideband receiver system. Applications of the methodology were demonstrated in both radio-frequency and low-frequency systems, including cascaded and feedback system configurations. From the integration of the UWB LNA and Mixer into the RF front-end subsystem, I study the role of horizontal interface assumptions in contract-based composition to preserve the validity of the component models. From the construction of analog feedback system in the base-band filter cells, I show that assumptions not only exist in the bottom-up phase of APBD. Vertical contracts of system-level APs on the underlying components are needed to ensure that design space exploration is in the region of interest for the system designer and that the system-level behavioral model accurately represent the actual circuit. Furthermore, the constructed

sub-systems were characterized as higher level AP components and composed together to construct the UWB receiver system. The necessary interface assumptions of the component-level contracts propagate into the system level through newly constructed sub-system APs, and I demonstrate a complete hierarchical approach to system construction using the proposed contract-based composition method. Results of the work show not only increased accuracy for system-level optimization and modeling, but also allowed removal of unnecessary interface circuitry, which further reduced system power consumptions.

The methodology presented in this work leverages domain knowledge from designers at various abstraction levels to provide a systematic approach to analog IP characterization, reuse, and system construction. Models are created by domain experts (e.g. RF circuit designer, system architect, etc.) at different levels using analog contracts to specify the assumed working environments and guaranteed outputs of the components. Models are then composed together to satisfy system specifications by first validating contract assumptions of various components, and then generating the estimated system outputs based on corresponding component guarantees. In addition, for partially constructed systems with unrealized components, the contracts of existing components in the system can help drive specifications for the design of the unrealized components, further reducing time-to-market of new products by minimizing specification engineering efforts. Although the case study used in this work is a receiver system, the application of the proposed composition methodology can be adopted to all RF, analog, and mixed-signal systems to leverage design reuse. Certainly, additional case studies for other applications can help provide more demonstration for the methodology and expose additional open questions to address.

6.1 Future Recommendations

The work featured in this dissertation is seminal for the use of contracts to enable analog system-level IP integration and reuse. With further advancements to bridge the gap between system-level and circuit design in the analog domain, innovative electronic applications can be realized with less risk, time, and financial commitment, while ensuring high quality design are generated through system-level optimization. Several open research topics can be explored to continue this work:

- Explore representation and modeling techniques for nonlinear assumptions in contracts. This work uses linear inequalities to represent contract assumptions, which may be an overly simplified model in some cases. Nonlinear macro-model representations for analog component assumptions should be explored to increase the accuracy of system-level design exploration, without incurring significant cost in terms of optimization and characterization runtime or computational complexity.

- Use analog contracts for analog equivalence checking. Since analog contracts are abstracted views of a component, they may also be used to compare equivalence of different components, where equivalence are with respect to the desired interface and performance parameters (e.g. gain or output impedance) of the components. This type of component-wise

equivalence checking allows tradeoff analysis to be performed locally for usage of different components in a system through a plug-n-play fashion, without running complete system simulations to verify equivalence.

- Extend analog contracts to capture assumptions on process variability. Variability has become a dominant issue in modern semiconductor systems as process technology head into 13-nm process and beyond. New systems must be designed with variability of components inherently assumed. Contracts can be used to capture the assumed statistical distributions for process variability at the system-level for each of the underlying components. This results in more robust and resilient system designs, which can be verified at the system level. However, how variability assumptions and guarantees can be captured is still very much an open question, and will most likely require nonlinear modeling techniques for contracts, as mentioned above.

- Use template-based test-benches to automatically characterize analog components. Although this work, as well as previous works in APBD, provides a systematic approach to component characterization, it's still very much manual and requires designer effort for each new topology. Complete automatic characterization is not possible, since designer knowledge and input is always needed. But a library of test-bench templates to automate common characterization procedures (e.g. interface conditions, linearity, gain, etc.) would significantly improve the usability of the methodology.

- Use preprocessing techniques on AP models to speed up system optimization. As was observed from the case-studies in this work, system optimization runtime is dependent on how *well-formed* the component models are. If the given component models are inherently compatible, optimization time is significantly reduced, conversely, if the compatible regions is extremely small with respect to the represented design space of each component model, even an initial design was difficult to locate. Thus, preprocessing the AP component models prior to optimization may help significantly improve the overall runtime. Specifically, two approaches maybe considered:

  - Leverage constraint satisfaction techniques such as SAT-modulo theorem (SMT) solvers to preprocess AP components to locate compatible regions prior to optimization. With recent improvements in SMT solvers, they can be used isolate only compatible component designs to send into the optimization engine, which help remove the number of constraints to satisfy during optimization, improving runtime.
  - Use convex optimization to isolate the regions of interest. Although analog performance regions are in general non-convex, the design space can be approximated as a convex region initially to isolate the most likely regions for each component that may be compatible and satisfy the system requirements. Once the approximate regions are located, the AP components can be parsed to only represent the given regions, and a

more detailed non-convex optimization engine can be used to locate the optimal design points.

With both techniques, a tradeoff with the pre-processing complexity and runtime versus the actual optimization runtime must be evaluated.

- Build robust support tools and integration with existing tools. Although this work demonstrates the application of the methodology on various case studies, robust and comprehensive tool support is still missing. A robust software infrastructure that integrates well into existing tool-flows in industry is needed to promote significant mass adoption of this methodology.

- Lastly, analog contracts can be leveraged for automatic architectural synthesis of heterogeneous system. Indeed, this has always been the goal for PBD, to leverage platform stacks and a library of components to map an application onto various architectures and make appropriate system-level tradeoffs. Contract-based composition is an enabler that allows system-level architectural construction to remain in realistic and valid regions despite raising the level of abstraction. In addition for evaluating tradeoffs between RF, analog, mixed-signal, digital, and software domains, packaging-level issues may also be evaluated using a similar approach. System-in-Package vs. System-on-a-Chip design decision is non-trivial. The decision for the right level of integration should depends on the performance of the available components, interconnect conditions, and system architectures and specificifications. Enabling the effective communication between chip designers and packaging specialists is extremely important, which can best be captured with the use of contracts.

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