Towards a Synthesizable Standard-Cell Radio

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Technical Report No. UCB/EECS-2012-219
http://www.eecs.berkeley.edu/Pubs/TechRpts/2012/EECS-2012-219.html

December 1, 2012

Towards a Synthesizable Standard-Cell Radio

By

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Kristofer Pister, Chair

Professor Jan Rabaey

Professor Paul Wright

Fall 2011

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Abstract

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Radios available today are designed to be high performance devices. These radios require careful design by experienced and skilled RF IC designers, more expensive RF processes, and large chip areas for RF passives. The resulting cost of these devices is at the dollar level without the off chip components, and the careful design required makes integration of these radios with other circuits (microprocessors, sensors, etc) an expensive proposition. We believe that radios that require limited design skills while still having good performance will enable widespread use of wireless technologies.

This motivation leads to the design of a fully integrated frequency shift keying (FSK) transceiver and phase-locked loops (PLLs) built with standard cells in a .18μm CMOS process without any off-chip components. Building a transceiver and PLLs with standard cells dictates that an inverter-based ring oscillator, rather than an LC oscillator, will be used for LO generation. Even though the frequency stability of a ring oscillator poses an obstacle in FSK modulation, this approach reduces the effort required when re-designing the receiver in a different process. Additionally, an inverter-based ring oscillator takes up much less area compared to an LC oscillator.

The receiver prototype built in a .18μm standard CMOS process occupies only 500μm x 350μm of area, has a sensitivity of -76dBm at 10kbps data rate,

and consumes 6mW from a single 1.8V supply while operating in 915MHz ISM band.

The transmitter prototype built in a .18μm standard CMOS process includes a power amplifier and a fractional-N all-digital PLL. This fractional-N PLL uses an embedded time-to-digital converter (TDC) with multi-path to increase TDC resolution, and includes digital correction circuitry to resolve issues from clock skew. This PLL prototype occupies 500μm x 500μm of area, generates a 915MHz LO signal from a 10MHz reference, has phase noise of -90dBc/Hz at 1MHz offset and 2.62ps-rms jitter while consuming 4.2mA from a 1.8V supply. Even though this fractional-N all-digital PLL is built almost entirely with standard cells, the performance of this PLL is comparable to other state-of-the-art all-digital PLLs recently published in ISSCC. To illustrate the idea of portability, this transmitter in a .18μm standard CMOS process is ported to a 65nm CMOS process for completeness and this transmitter takes up $0.04mm^2$. In a fine-line process, a complete transceiver can occupy only $0.1mm^2$ of area or smaller.

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Acknowledgment

First of all, I would like to thank my advisor, Professor Kristofer Pister, for his support and guidance throughout my Ph.D. career. His vision and broad knowledge on all aspects of the WSN have been inspiring and challenging. I would also like to thank my qual committee members, Professor Jan Rabaey, Professor Elad Alon, and Professor Paul Wright for valuable discussions concerning my work. My interaction with Jan's and Elad's students have helped to shape my research direction. Furthermore, this work would not be possible without the help from many graduate students in the EECS department. I particularly enjoy discussing my PLL and RF designs with Steven Lanzisera, John Crossley, and Jiashu Chen. I am also grateful for the foundry service donation from ST Microelectronics. Finally, I would like to thank my parents and my brother, Yu-Jih Su, for their support over the past several years. Thank you.

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Berkeley, California

Chapter 1

Introduction

Over the past ten years, we have seen a tremendous growth in wireless systems. In this *1000 radios per person* scenario [21], there would be a market for high performance radios that can communicate with high data rate and have long communication range. However, there will also be a market for radios that do not deliver high performance, but offer low cost instead. We believe that radios that require low manufacture and design cost while still having reasonable performance will enable widespread use of wireless technologies.

1.1 Implementation Requirements

To reduce the design and manufacture cost of a radio, here are a list of approaches.

- **Minimize RF IC engineering:** Experienced RF IC designers are hard to find. An RF design typically requires at least one test chip to verify its functionality and performance. As a result, RF designs tend to be costly and unpredictable, and the design time of a high performance radio could be up to a year or longer. On the other hand, digital designers, with the help of synthesis tools and standard cells, can design complicated systems with behavioral languages. By trading off some RF performance with ease of design, we believe that a radio built with standard cells and synthesis tools can help dramatically reduce the complexity and cost associated with designing a radio and make porting a radio to a different process/technology much easier. Additionally, the

design time of such a radio can be reduced by a factor of 10X. This approach has been demonstrated in building an UWB transmitter [36]. Some Researchers at University of Michigan are working on building a narrowband transceiver using similar approaches [37].

- **No on-chip inductors:** On-chip inductors are bulky passive components in RF designs. They do not scale with technologies. Additionally, they require careful simulations using special CAD tools, such as HFSS, to verify their characteristics, such as quality factors, inductance, and etc. The cost of using RF processes will be more expensive than using standard CMOS processes. All these add up the cost of a high performance radio.

In addition to low-cost, the radio we have in mind needs to operate in the presence of interference and have moderate communication range while consuming minimum power.

- **Wide-band linearity:** Wireless devices need to operate in the presence of interference. Without filtering, strong out-of-band jammers can easily compress the receiver front-end. Either passive front-end filters or other circuit techniques need to be used to suppress out-of-band interference.

- **Reasonable sensitivity:** Receiver sensitivity impacts link budget, which impacts the communication range. Typical commercial 802.15.4-compliant radios have receiver sensitivity of better than -90dBm, and link budget of better than 90dB when the transmitter output is at 0dBm. For indoor environment, communication range of 10 meters typically requires link budget of at least 70dB.

- **Low power:** Commercial 802.15.4-compliant radios have power consumption in the range of 10mW to 100mW. Power consumption of a radio dictates the life span of the battery used in a wireless sensor node. It is important to minimize the power consumption.

Figure 1.1 and figure 1.2 summarize the differences between the requirements of a high performance radio available today and the requirements of our radio.

High performance radios	Our radio requires
▪ Experienced RF / analog designers	▪ Digital designers
▪ RF processes / RF CAD tools	▪ Standard CMOS process
▪ Large chip areas for RF passives	▪ Small chip areas
➢ Expensive	➢ Cheap
▪ Design time of ~1 year	▪ 1 month design time
	Additional features • Low Power • Easily portable to any arbitrary process/technology • Reduced cost of re-design • Faster time to market

Figure 1.1: High Performance Radios versus Our Radios

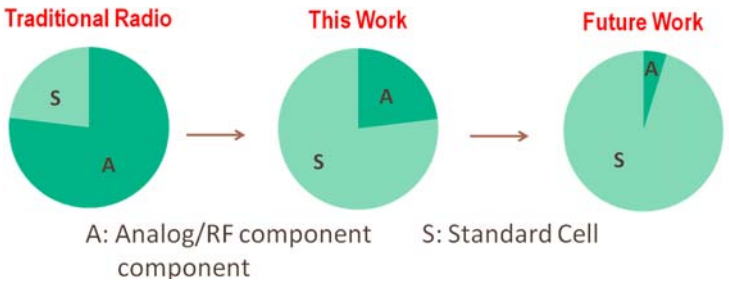

Figure 1.2: Approach

Figure 1.3: Smart Energy

1.2 Target Specifications

Looking across a broad range of applications, we decide to design a low-cost radio that can communicate over 10 meters indoor, has data rate of 10kbps, support FSK and OOK, and operate in ISM band. Indoor communication range of 10 meters requires link budget of at least 70dB. FSK and OOK are popular modulation schemes among low power applications due to their relaxed hardware requirements. The complete specifications are summarized in table 1.1. One application for such a radio is a smart home for energy conservation. The idea behind a smart home is to put a great number of different types of sensors and controllers throughout a house as seen in figure 1.3. There can be solar power monitoring devices, pool pump controller, AC controller, temperature sensors, light sensors, room occupancy sensors, current consumption sensors, and etc. Each sensor or controller, when attached to a radio, can then communicate with one another to achieve energy conservation. Connecting these sensors through wires would not be practical nor cost-effective. In a smart home application, radios with communication range of 10 meters and data rate of 10kbps is sufficient to form a connected network and deliver necessary information to one another.

Table 1.1: Target Specs

Parameter	Specification
Carrier Frequency	ISM (915MHz, 2.4GHz)
Modulation Scheme	FSK/OOK
Data Rate	10kbps
Sensitivity	Better than -70dBm
Active Power Consumption	As low as possible

1.3 Thesis Organization

This chapter has discussed implementation requirements, target specifications, as well as potential applications of a radio that requires minimum RF IC engineering, small foot print, and low power. The goal of this research is the design and implementation of such a radio. Additionally, we would like to design this radio in a process-portable way and to demonstrate the portability by implementing this radio in more than one standard CMOS process.

2 presents the transceiver front-end architecture as well as the frequency synthesizer design in the system. Comparisons between ring oscillators and LC oscillators are also presented. A survey of different types of frequency synthesizers and their noise contributions are also discussed. 3 describes the differences between mixed-signal PLLs and all-digital PLLs as well as the advantage of all-digital PLLs over mixed-signal PLLs. 4 provides a brief introduction on time-to-digital converters (TDCs) that are widely used in all-digital fractional-N PLLs. 5 details the design and implementation of our transceiver prototype in a .18μm standard CMOS process, including all the necessary blocks to perform the transmission and reception wirelessly. In order to demonstrate the portability, we port our first prototype to a 65nm standard CMOS process and the results are discussed in 6. Finally, 7 concludes with a brief summary of results and discussion of future research directions.

Chapter 2

Radio Architecture

In the last chapter, we covered implementation requirements, target applications, and target specifications. Given that one of our main objectives is to minimize RF IC engineering for portability enhancement and engineering cost reduction, it is important to choose a radio architecture that is digital-designer friendly. Additionally, this architecture needs to be able to provide wide-band linearity without using any on-chip inductors. Furthermore, it needs to have decent sensitivity while consuming low power.

2.1 Transceiver Front-End Architecture

Using direct modulation at the transmitter is a common technique among low power radios because it alleviates the need for an up-conversion mixer. This reduces the design effort, area, and power consumption at the transmitter. Figure 2.1 shows the transmitter architecture of our choice. FSK signals are sent out by changing the output frequency of the fractional-N all-digital phase-locked loop (PLL). Having PLL output jump between two tones sets some requirements on how fast the PLL needs to lock onto each tone. Since our design is an all-digital PLL, the coefficients associated with each tone can be stored in the memory and swapped in to reduce the lock time of the PLL. Section 2.2 will discuss more about the architecture of the fractional-N all-digital PLL.

Even though direct conversion receivers inherently provide image rejection, they are also known for their issues related to quadrature paths, DC offset, I/Q mismatch, and flicker noise [1]. To avoid these issues, a low-IF

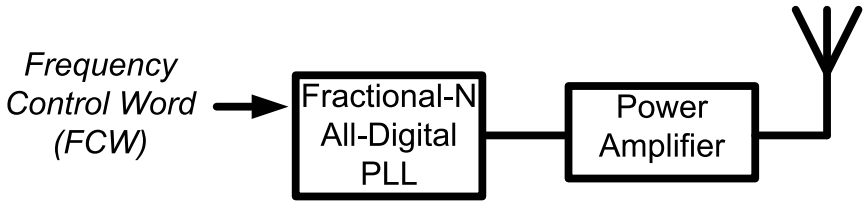

Figure 2.1: Transmitter Architecture

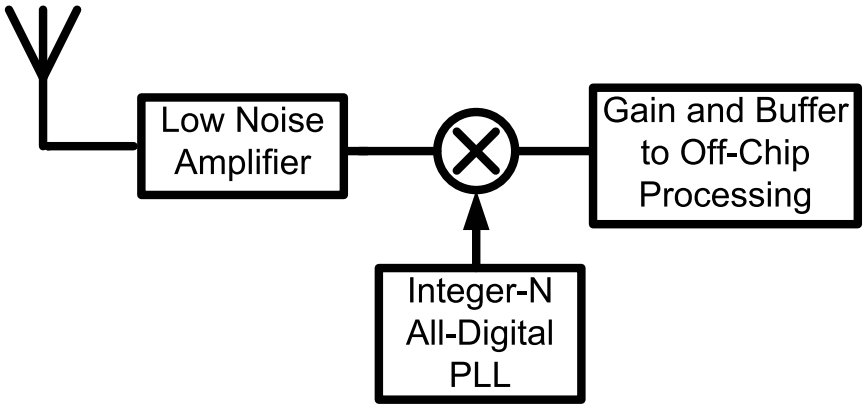

Figure 2.2: Receiver Architecture

receiver architecture is chosen. The RF signal coming in from the antenna is converted to a low intermediate frequency (IF) band, and directly digitized for demodulation, without the second step of down conversion. This low-IF receiver, shown in figure 2.2, is composed of a low-noise amplifier, a passive mixer and an integer-N all-digital PLL. The details of this integer-N all-digital PLL will also be discussed in section 2.2.

2.2 Local Oscillator and Frequency Synthesizer

Local oscillators (LO) and frequency synthesizers are critical blocks in both the transmitter and receiver architecture of our choice.

2.2.1 Local Oscillator

There are two types of local oscillators commonly used: ring oscillators and LC oscillators. A three-stage inverter-based ring oscillator is shown in figure

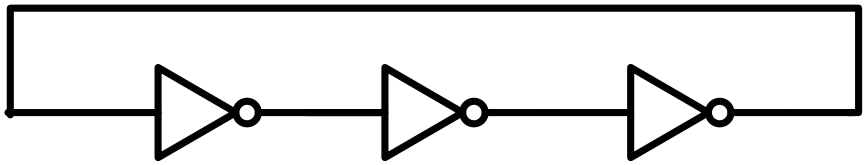

Figure 2.3: Ring Oscillator

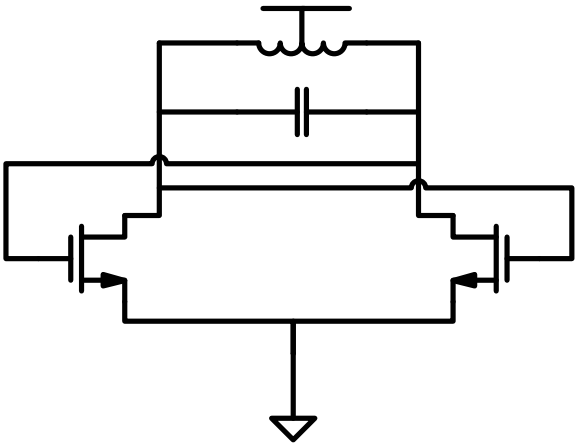

Figure 2.4: LC Oscillator

5.19. This type of ring oscillator is widely used in clock generation for digital systems. The oscillation frequency of such a ring oscillator depends on the delay of inverters.

A different type of oscillator, an LC oscillator shown in figure 2.4, uses a LC tank with a pair of cross-coupled devices. The purpose of the cross-coupled devices is to re-charge the energy lost from the LC tank. At steady state, the energy lost from the LC tank is equivalent to the energy added by the cross-coupled devices. The oscillation frequency of an LC oscillator is the resonant frequency of the LC tank. With a high-Q LC tank, an LC oscillator can have great phase noise performance. Because of band pass characteristics of the LC tanks, LC oscillators generally have better phase noise than ring oscillators [2]. As a result, in order to meet stringent spectrum mask at the transmitter side and to have great sensitivity at the receiver side, most radios available today use LC oscillators for LO generation.

Even though LC oscillators provide better phase noise, ring oscillators have advantages over LC oscillators as well.

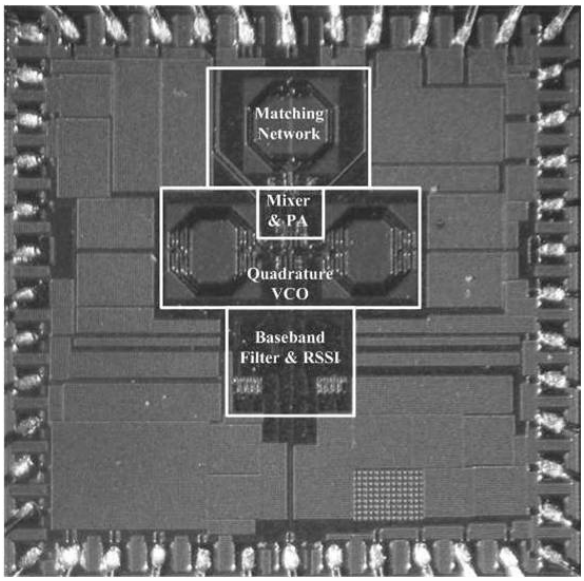

Figure 2.5: 2.4GHz Radio

- **Small Size:** On-chip inductors are bulky and do not scale with technologies. As an example, figure 2.5 is a 2.4GHz radio [3]. A great portion of the active area in this design is occupied by on-chip multi-turn spiral inductors. Inverter-based ring oscillators, on the other hand, are made of active devices and take up very small area.

- **Wide Tuning Range:** To change the oscillation frequency of an LC oscillator, the resonant frequency of the LC tank within it needs to be adjusted. Given that

$$\omega_{resonance} = \frac{1}{\sqrt{LC}}$$

  Keeping the inductor the same size, and sizing the capacitor to be four times bigger will only reduce the oscillation frequency by half. On the other hand, a moderate change on the supply voltage of a ring oscillator can easily alter its oscillation frequency by a factor of 10X. Ring oscillators have a much wider tuning range compared to LC oscillators and radios using ring oscillators have the potential to operate in multiple ISM bands using one single ring oscillator.

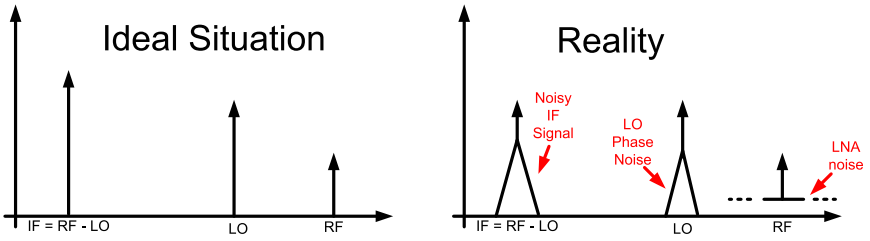

Figure 2.6: Receiver Noise Sources

2.2.2 Frequency Synthesizer

Due to process and temperature variations, the oscillation frequency of an oscillator can be different from die to die and change with temperature. It is therefore important to lock the oscillation frequency of an oscillator to a known stable reference, such as a crystal, through a frequency synthesizer. Additionally, a frequency synthesizer suppresses the phase noise of a ring oscillator within the closed-loop bandwidth of the system. It is worthwhile to see how phase noise of the LO signal adds noise into a receiver front-end. In an ideal situation, the RF signal mixes with the LO signal and gets down-converted to IF as shown in figure 2.6. In reality, the receiver front-end adds noise onto the RF signal. The phase noise adds skirts around the LO signal. This noisy RF signal convolves with the noisy LO signal to generate the noisy IF signal.

Two common form of frequency synthesizers are a multiplying delay-locked loop and a phase-locked loop. We will discuss the pro and con of a multiplying delay-locked loop and why we decide to use a phase-locked loop for our prototype at the end.

2.2.2.1 Multiplying Delay-Locked Loop

A delay-locked loop (DLL) is commonly used to generate multiple phases with the same frequency as the reference clock for a communication system. A variant of a DLL, called multiplying delay-locked loop (MDLL), can synthesize a clock signal with frequency that is a multiple of the input reference clock [27, 31, 30]. An example MDLL is shown in figure 2.7. Additional circuitry, not shown in the figure, is needed to control the Select bit. It operates as follows. Assuming this MDLL has multiplying factor of N, at every N-th VCO cycle, the Select bit will go high to allow the reference clock

signal to go through and block the returning signal from the delay line itself. In other words, after N cycles, this delay line takes in a clean signal from the reference clock, rather than the noisy signal fed back from itself. This complete replacement of VCO signal by the reference signal is as if this sampled system has infinite bandwidth. The phase detector compares the reference clock signal with the N-th VCO clock signal and the error signal is integrated through a loop filter to drive the phase error towards zero. This system is a first order loop because there is only a single integration from the loop filter. As a result, such a system is unlikely to become unstable and comparatively easy to design. In an ideal situation, the reference clock comes in to clean up the delay line periodically as shown in figure 2.8. Because the reference clock signal comes in every N VCO cycles to replace the noisy signal fed back from the delay line, the noise is completely removed from the system after every N VCO cycles assuming an ideal reference. An MDLL can potentially achieve great phase noise performance. However, in reality, a phenomenon depicted in figure 2.9 makes such a system unrealistic for a wireless system. Since the reference clock signal is used to replace every N-th rising edge of the VCO node, the system essentially cleans up all the VCO noise accumulated over N-1 VCO cycles in one single VCO cycle. The period of the last VCO cycle could be dramatically different from the previous N-1 cycles. This phenomenon takes place periodically. As a results, MDLLs are known to have large reference spurs and are seldom used for LO generation in a wireless system because reference spurs can influence the operation of adjacent channels or jam the frequency bands of others. A phase-locked loop, a second order system, is more suitable for LO generation used in a wireless system.

2.2.2.2 Phase-Locked Loop (PLL)

There are two types of PLLs: an integer-N PLL and a fractional-N PLL. Integer-N PLLs can only lock the LO frequency to an integer multiple of the stable reference. The output frequency step size of an integer-N PLL is equivalent to the reference frequency. PLL is actually not a continuous-time system, but a discrete-time system. For stability reason, the loop bandwidth of a PLL is limited by the reference frequency [4, 38]. The rule of thumb is to design the loop bandwidth to be at one tenth of the reference frequency. As a result, there exists a tradeoff in an integer-N PLL: loop bandwidth versus output frequency step size. For example, if one would like to design a PLL

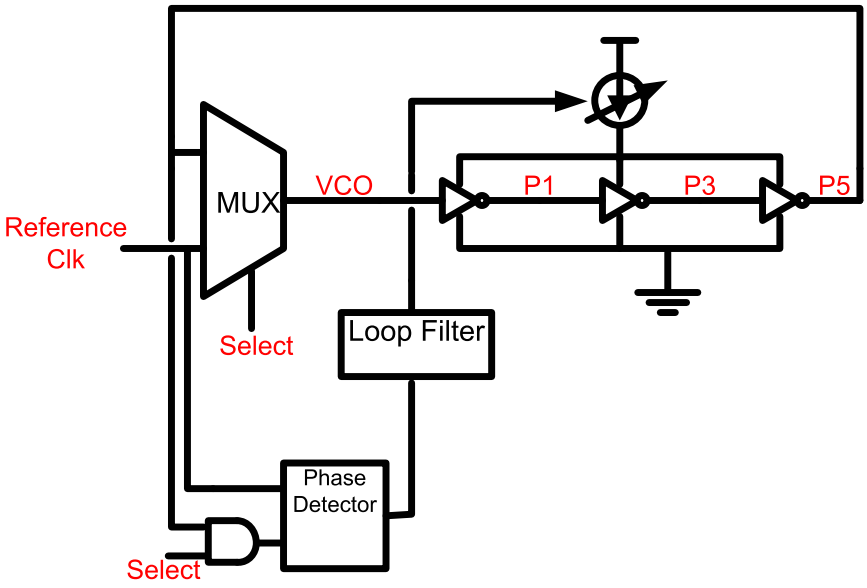

Figure 2.7: Multiplying Delay-Locked Loop

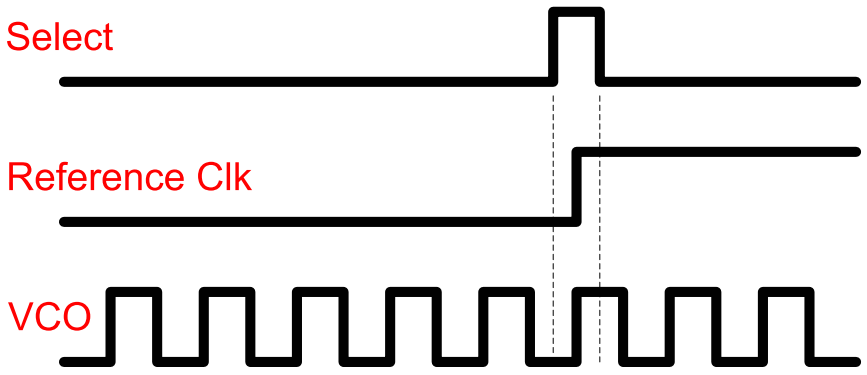

Figure 2.8: Ideal Waveform

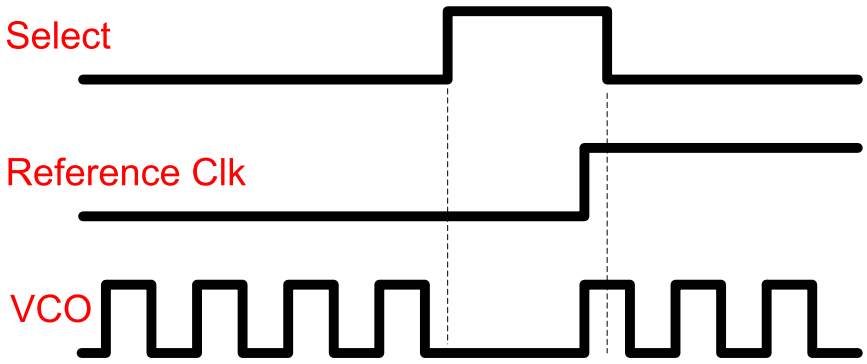

Figure 2.9: Real Waveform

with bandwidth of at least 1MHz, the reference would need to be at least 10MHz. If the reference is at least 10MHz, the smallest output frequency step size will be at least 10MHz. In many cases, an output frequency step size of less than 10MHz is needed. A fractional-N PLL decouples loop bandwidth from output frequency step size. It can synthesize output frequency with step sizes smaller than the reference frequency. Hence, to achieve a wide-band PLL with a fine output frequency step size, a fractional PLL can be used.

Figure 2.10is a behavioral model of a PLL. The Kvco/s represents the transfer function characteristics of the VCO, with Kvco being the VCO gain. VCO itself integrates frequency and outputs phase. Hence, it is an integrator and contributes a pole into the transfer function of the system. This VCO gain is typically determined by VCO implementation, such as the tuning range requirement. The Kp and Ki/s represent the digital loop filter in a digital PLL, and represent a combination of charge pump and analog RC filter in a conventional charge-pump mixed-signal PLL. Overall, this system has two poles and one stabilizing zero in the open loop transfer function. The loop filter contributes a pole and a stabilizing zero, whereas the VCO contributes the other pole to the loop transfer function. Given the desired bandwidth (BW) and phase margin (PM), the coefficient Kp and Ki can be calculated based on the following method.

The open loop transfer function from input reference to PLL output is

$$H(s) = \frac{\phi_{vco}(s)}{\phi_{ref}(s)} = (K_p + \frac{K_i}{s})\frac{K_{vco}}{s} = K_p(1 + \frac{\omega_z}{s})\frac{K_{vco}}{s},\ where\ \omega_z = \frac{K_i}{K_p}$$

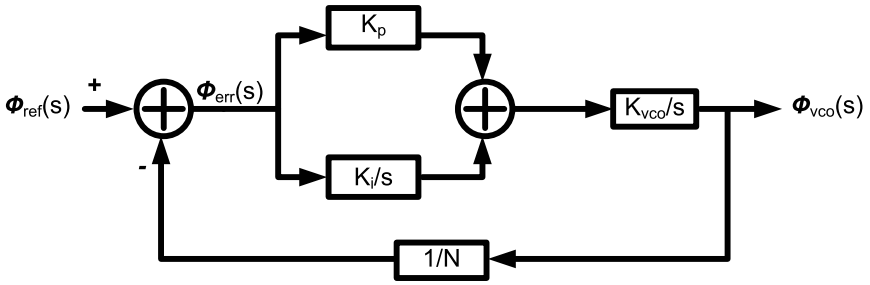

Figure 2.10: Behavioral Model of a PLL

With the phase margin being PM and desired closed loop bandwidth being BW, it can be shown that

$$PM = arctan(\frac{\omega_{BW}}{\omega_z})$$

$$\omega_z = \frac{\omega_{BW}}{tan(PM)}$$

Based on the fact that

$$|H(j\omega_{BW})| = N$$

$$K_p = N\frac{\omega_{BW}^2}{\sqrt{\omega_{BW}^2 + \omega_z^2}}\frac{1}{K_{vco}}$$

$$K_i = K_p\omega_z$$

The PLL open loop transfer function is plotted out in figure 2.11.
The closed loop frequency response of the PLL

$$Z(s) = \frac{(K_p + \frac{K_i}{s})\frac{K_{vco}}{s}\frac{1}{N}}{1 + (K_p + \frac{K_i}{s})\frac{K_{vco}}{s}\frac{1}{N}} = \frac{\frac{K_pK_{vco}}{N}s + \frac{K_iK_{vco}}{N}}{s^2 + \frac{K_pK_{vco}}{N}s + \frac{K_iK_{vco}}{N}} \tag{2.1}$$

Since this is a second-order system, Z(s) can be expressed as [32]

$$Z(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

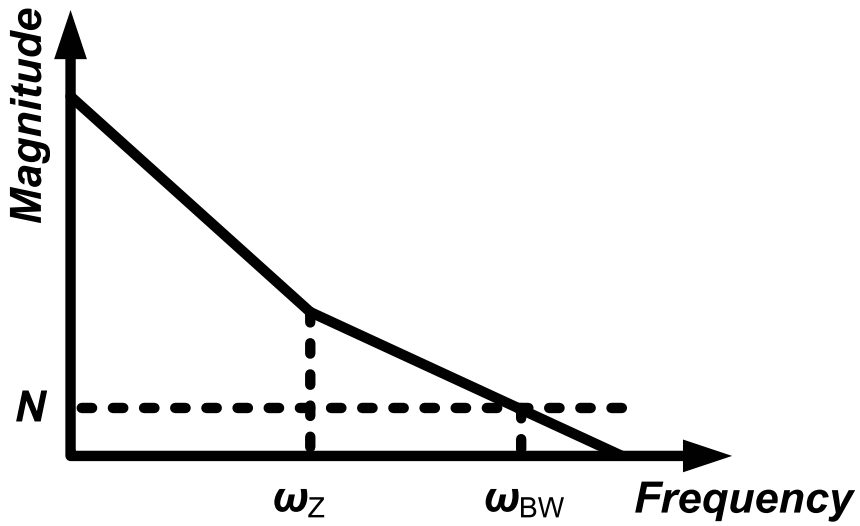

Figure 2.11: PLL Transfer Function

where $\zeta$is the damping factor and ω_n is the natural frequency of the system.

When $\zeta > 1$, the system is over-damped and the step response is a decaying exponential with no oscillation. However, as ζincreases, the dynamic response becomes sluggish. When $\zeta < 1$, the system is under-damped. At the extreme case when $\zeta = 0$, the system oscillates indefinitely and is unstable. In practical systems, no matter what value$\zeta$is, there exists a peaking at the closed loop frequency response Z(s) as shown in figure 2.12. This peaking amplifies the reference noise at that frequency band and is undesirable from a noise standpoint of view [33]. Typically, PLL designers choose $\zeta$to be around 0.6 to achieve a butterworth maximally flat closed loop magnitude response with reasonable step response.

2.2.2.3 Noise Analysis

One of the main purposes of using a PLL is to synthesize a clean LO signal. Each block in a PLL may contribute noise, but their transfer functions to the output differ. Generally speaking, the noise can be introduced into a PLL from point A, B, and C on figure 2.13. Their transfer functions to the output are as follows.

- Point A represents noise from the reference signal and point B represents noise from the divider. The transfer function from point A or

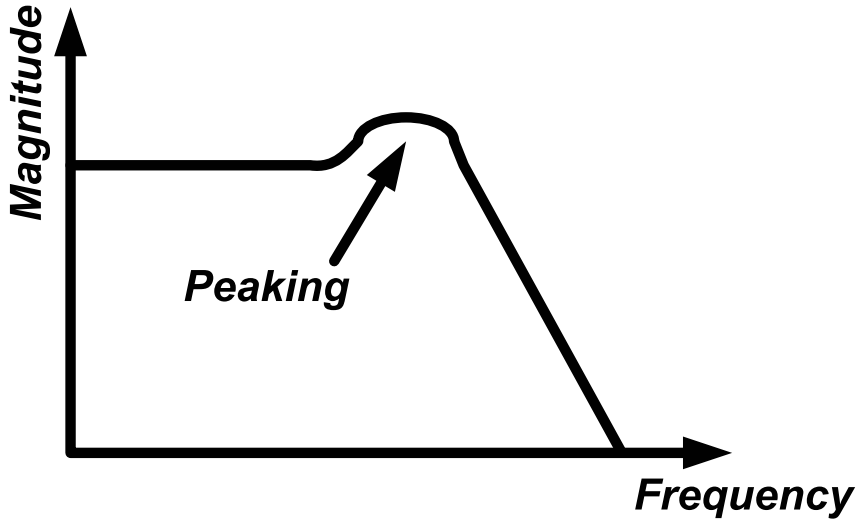

Figure 2.12: Closed Loop Magnitude Response

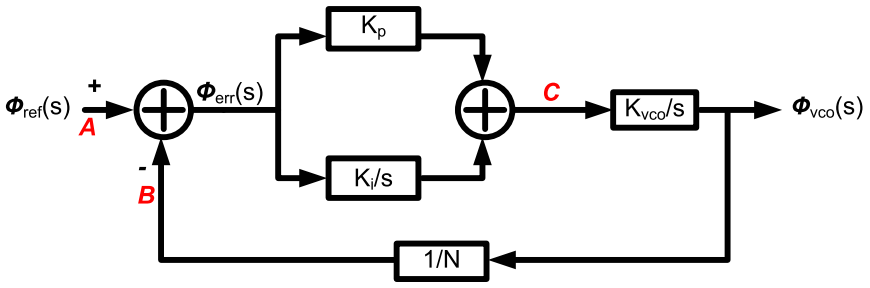

Figure 2.13: Behavior Model of a PLL

point B to the PLL output are the same and they are equivalent to 2.1. In other words, the noise from the reference or the divider will get to output within the closed loop bandwidth of the PLL.

- Point C represents noise from the loop filter and also supply noise of the VCO. The transfer function from point C to the PLL output is:

$$Noise(s) = \frac{\frac{K_p K_{vco}}{N} s + \frac{K_i K_{vco}}{N}}{s^2 + \frac{K_p K_{vco}}{N} s + \frac{K_i K_{vco}}{N}} \frac{K_p s + K_i}{s}$$

The first part of the Noise(s)

$$\frac{\frac{K_p K_{vco}}{N} s + \frac{K_i K_{vco}}{N}}{s^2 + \frac{K_p K_{vco}}{N} s + \frac{K_i K_{vco}}{N}}$$

is a low pass filter.
The second part of the Noise(s)

$$\frac{K_p s + K_i}{s}$$

is a high pass filter.

Together, they form a band pass filter. In other words, the supply noise of the VCO will go through a band-pass filter before reaching the PLL output. When the closed loop bandwidth increases, the impact of VCO supply noise on overall PLL noise will decrease and the impact of noise from the input reference clock will increase. On the other hand, when the closed loop bandwidth decreases, the impact of VCO supply noise on overall PLL noise will increase, and the impact of noise from the input reference clock will decrease.

Based on the analysis shown above, if the reference clock is very clean and the VCO is built of a ring oscillator, which has poor phase noise, a PLL should be designed to have a large bandwidth because the reference clock will help clean up the VCO phase noise within the bandwidth of the PLL. On the other hand, if the reference clock has poor phase noise and the VCO is an LC oscillator with a high-Q LC tank, it would be wise to design the PLL with low bandwidth instead. Otherwise, the reference clock will degrade the VCO signal within the bandwidth of the PLL.

Chapter 3

Mixed-Signal PLLs versus All-Digital PLLs

PLLs are widely used in a variety of communication and digital systems. In a radio front-end, PLLs are used to generate LO signals. In a digital system, PLLs are used to generate reliable clock signals. A majority of commercial products use mixed-signal charge-pump PLLs (CPPLLs) for either LO or clock generation. A simplified view of an integer-N CPPLL is shown in figure 3.1. In order to make a fractional-N CPPLL, a sigma delta modulator needs to be added and the divider needs to be a multi-modulus divider as shown in figure 3.2. As technology continues to advance, it becomes more and more challenging to design a high-performance mixed-signal PLL that runs off the same supply voltage and meets the strict DRC rules. Researchers hence start to look into the design of all-digital PLLs (ADPLLs) to help alleviate the issues associated with mixed-signal PLLs in a fine-line process. A simplified view of an integer-N ADPLL is shown in figure 3.3. To build a fractional-N ADPLL, one method is to convert the charge pump in figure 3.2 to a multi-bit time-to-digital converter. A more digital approach removes the divider and directly computes the ratio between the output and reference frequency using a counter and a TDC. In either case, a multi-bit time-to-digital converter will be required. A divider-less fractional-N ADPLL is shown in figure 3.4 [6]. The PI Controller in the figure is a proportional and integral controller with the integral path providing a pole and proportional path providing a stabilizing zero, and the TDC is a time-to-digital converter frequently needed in an ADPLL, especially if the ADPLL is a fractional one. The benefits of all-digital PLLs are listed below.

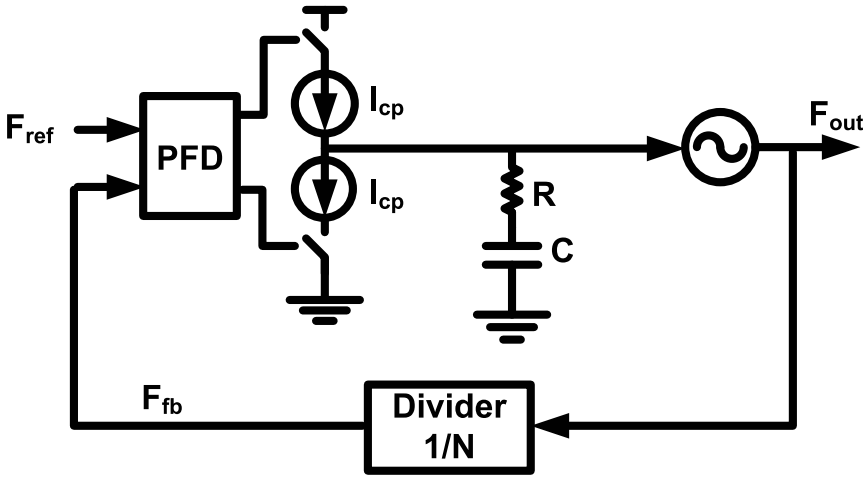

Figure 3.1: A Simplified View of an Integer-N CPPLL

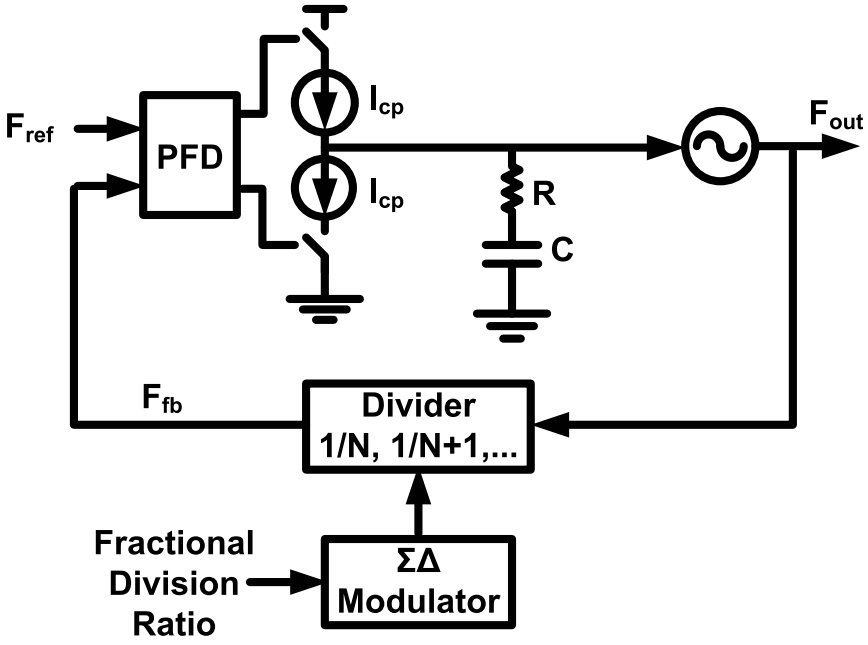

Figure 3.2: A Simplified View of a Fractional-N CPPLL

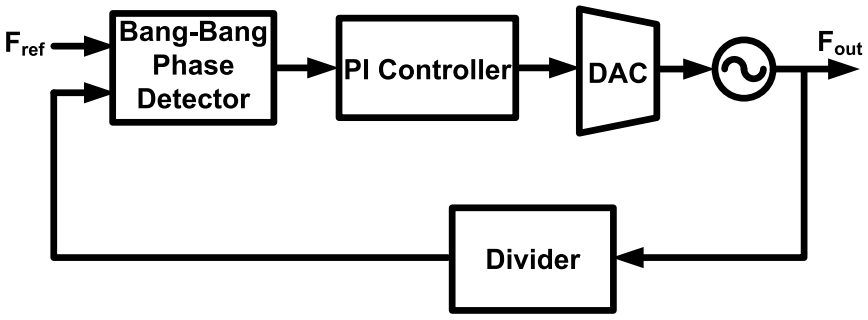

Figure 3.3: A Simplified View of a Integer-N ADPLL

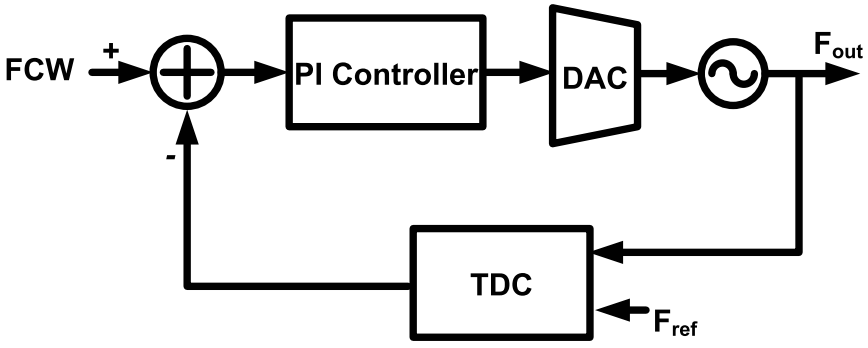

Figure 3.4: A Simplified View of a Divider-less ADPLL

- No capacitive leakage: The leakage current from an on-chip capacitor increases as technology continues to advance. Capacitive leakage from an analog loop filter will introduce spurs at the output of PLL because the loop will need to periodically add charges onto the capacitor to keep the PLL in the locking state. This periodical refill of charges takes place at every reference cycle and will result in reference spurs at the output. With a digital loop filter, since the information is converted and stored as bits, there will not be reference spur caused by capacitive leakage.

- No tradeoff between magnitude of charge pump current and loop filter capacitor value: In a CPPLL, the noise from the current source inside the charge pump contributes to the in-band noise at the PLL output, as described in 2.2.2.3. It can be shown that the influence from the charge pump current source to the PLL phase noise is inversely proportional to the magnitude of the current. Higher charge pump current contributes less noise to the overall system. However, given the same bandwidth and phase margin, an increase in the charge pump current will require a larger capacitor at the loop filter. This tradeoff does not exist for the ADPLL shown in figure 3.4 because the equivalence of the charge pump and the analog RC loop filter is a digital loop filter which does not introduce any noise at all.

- Large loop filter coefficient tuning range: A digital loop filter in an all-digital PLL is composed of mainly adders and accumulators. Changes on the digital loop filter coefficients can lead to changes on the loop bandwidth or phase margin of an all-digital PLL. Compared to analog loop filters, digital loop filters can allow wider tuning ranges given the same layout area, which means ADPLL allows wider tuning ranges on its loop bandwidth and phase margin as well.

- No noise introduction from PFD, charge pump, and loop filter: All the noise introduced from the PFD, charge pump, and loop filter will degrade the phase noise of the PLL, as described in 2.2.2.3. In the ADPLL shown in figure 3.4, the timing information is converted to digits through the TDC at a very early stage. No additional noise can be introduced from the digital equivalent of PFD, charge pump, and loop filter.

Even though an ADPLL has all these benefits over a mixed-signal CPPLL, the challenge of building a high-performance ADPLL lies on the design of

a high resolution and highly linear TDC. We will discuss some basic TDC architectures in the following chapter.

Chapter 4

Time-to-Digital Converter

All-digital integer-N PLLs using bang-bang phase detectors may achieve decent phase noise and jitter performance [5]. A bang-bang phase detector will output whether the reference signal is leading or lagging and it literally acts like a 1-bit TDC. A fractional-N PLLs, however, usually require multi-bit TDCs as the fractional error estimator. Two simplest forms of TDCs are an inverter delay line and a Vernier delay line [8, 28]. In the case of an inverter delay line (figure 4.1), the smallest resolution of the TDC is limited by the smallest unit delay of an inverter from that particular process. To achieve improved resolution, a Vernier delay line (figure 4.2) uses delay blocks with different unit delays, t1 and t2. The resolution of a Vernier delay line is the difference between t1 and t2. Even though a Vernier delay line can achieve better resolution, it has narrower range and takes up larger area. Other circuit techniques have been demonstrated in which the time residue can be amplified to achieve even greater time resolution [29], but the complexity of those circuits and the area taken up by those designs increase dramatically.

The purpose of a TDC in a fractional-N PLL is to estimate time or phase differences that are smaller than a VCO period. For example, assuming the VCO in the system is running at 1GHz, the smallest time step available in the system is therefore 1ns. In order to resolve any time or phase differences smaller than 1ns, a TDC is required. In a .18μm process, the unit delay of an inverter is close to 50ps. In other words, time resolution of 50ps can be achieved with a inverter delay line TDC. In modern radio design, this 50ps time resolution may not be sufficient to result in acceptable quantization noise. Additionally, the unit delay of an inverter changes due to process or temperature variations. At startup and periodically, this TDC will need to

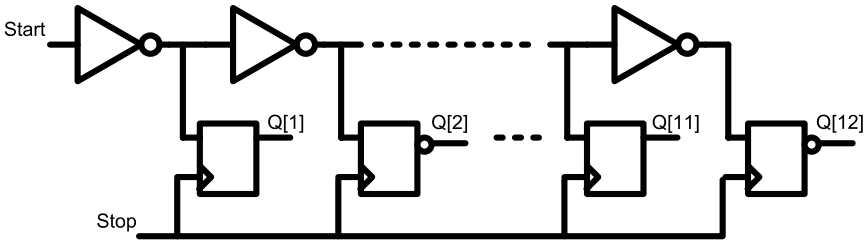

Figure 4.1: An Inverter Delay Chain TDC

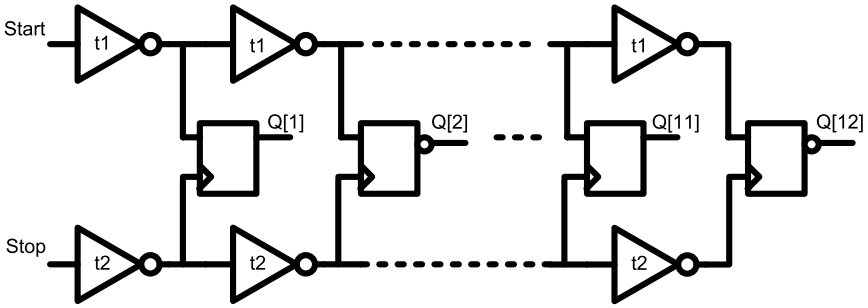

Figure 4.2: A Vernier Delay Line TDC

be calibrated against the main VCO in order to guarantee the accuracy of the unit delay of the inverters. As will be discussed in the next chapter, if the VCO is re-used as the TDC, not only area overhead can be avoided, but also calibration will not be required.

Chapter 5

Proof of Concept

As a proof of concept, we taped out two designs in a .18μm standard CMOS process without any RF options. The transceiver architecture of our choice is shown in figure 5.1.We will first discuss the design of a fractional-N PLL and a power amplifier in the transmitter, and then move on to talk about an integer-N PLL with a receiver front-end in the receiver. This radio is designed to work in the 915MHz ISM band. The entire transceiver is built with standard cells, with the only exceptions being the current sources and pass-transistor logic. Current sources are used for tuning DCO output frequency, controlling PA output power, and gain of the LNA. Pass-transistor logic is used in the passive mixer.

5.1 Transmitter

This direct modulation transmitter uses a fractional-N PLL to send out FSK signals, with tone spacing of around 400kHz, using a 10MHz reference.

5.1.1 All-Digital Fractional-N PLL

Mixed-signal fractional-N PLLs and several all-digital fractional PLLs recently published use a multi-modulus divider in the feedback path to synthesize an output frequency step size smaller than the reference frequency [6]. A more digital architecture removes the divider and directly computes the ratio between the output and reference frequency through a time-to-digital converter (TDC) [7]. This ratio is then compared with a Frequency Control

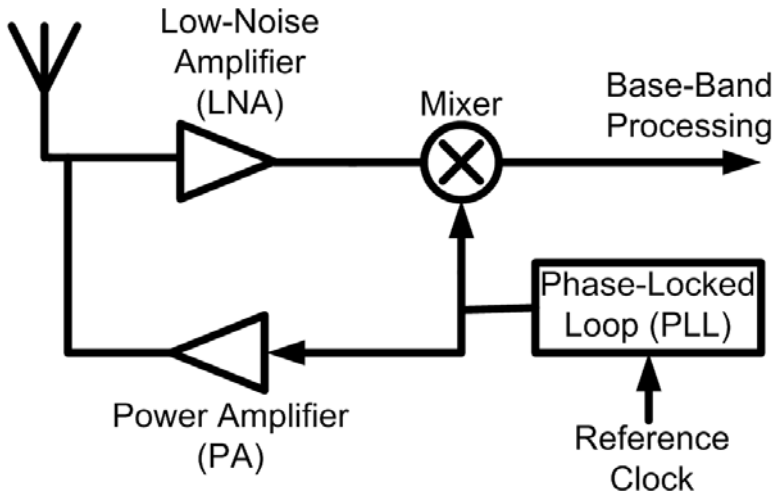

Figure 5.1: Transceiver Architecture

Word (FCW) to determine the phase difference. In this approach, phase information is kept in the digital domain and cannot be further degraded by noise. The digital processing capability is also enhanced.

A bang-bang phase detector, a 1-bit TDC, can be used in an integer-N PLL. However, fractional-N PLLs require multi-bit TDCs. TDCs are used in digital PLLs to convert time domain information to digits for further processing. As discussed in 4, a delay chain of inverters and a Vernier delay line are two simple forms of TDC. The former approach cannot resolve resolution better than an inverter delay, whereas the latter one can resolve finer resolution, but suffers from area increase and device mismatch. In addition, calibration between the TDC and DCO are necessary in both approaches. In this design, the TDC is embedded in the DCO [9, 10], and no area overhead or calibration is required. The relationship between output frequency step size and reference frequency is

$$Frequency\ Step\ Size = \frac{Reference\ Frequency}{Number\ of\ TDC\ Steps} \tag{5.1}$$

Figure 5.2 shows the fractional-N PLL architecture in this design. In this figure, the blocks in color green are designed with behavioral Verilog, compiled and auto placed and routed using Synopsys tools. The blocks in blue are designed using only standard cells that come with the design kits. The only block that is custom designed in transistor level is the all-digital current

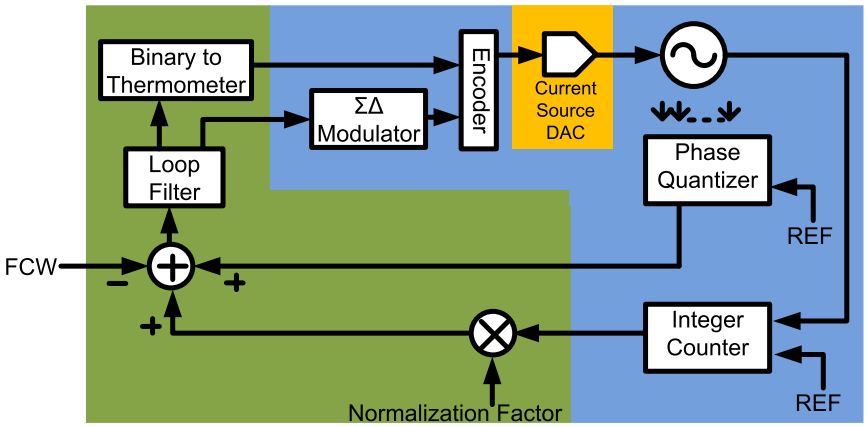

Figure 5.2: All-Digital Fractional-N PLL Architecture

source DAC described in 5.1.1.2. Overall, digital synthesis tools are used to design and layout a great portion of the PLL, including a binary to thermometer decoder, a loop filter, some arithmetic blocks, and digital correction circuitry.

This PLL operates as follows: the output of the integer counter is summed with the output from the phase quantizer to create a feedback digital word that is sampled by the input reference clock. This feedback digital word is then compared with the frequency control word (FCW). The resulting phase difference is filtered through a digital PI controller before updating the DCO frequency. We will go into details of each individual block.

5.1.1.1 Ring Oscillator

A differential ring oscillator, shown in figure 5.3 is used for this fractional-N PLL. This ring oscillator includes multi-paths to reduce the delay per stage [20]. Rather than having the cross coupled inverters between P0 and P13 as commonly seen in differential ring oscillators, the cross coupled inverters are between P13, P2 and P0, P15. The cross coupled inverters are sized to be half of the main inverters in the ring because the main inverters in the ring need to be strong enough to drive the cross coupled inverters out of latch-up.

Even though more degrees of multi-path can be added to further reduce the delay per stage [12], such as the configuration shown in figure 5.4 (cross coupled inverters are between P13, P2; P13, P4; P0, P15; and P0, P17), one level of multi-path has reduced the delay per stage to around 30ps. Since the

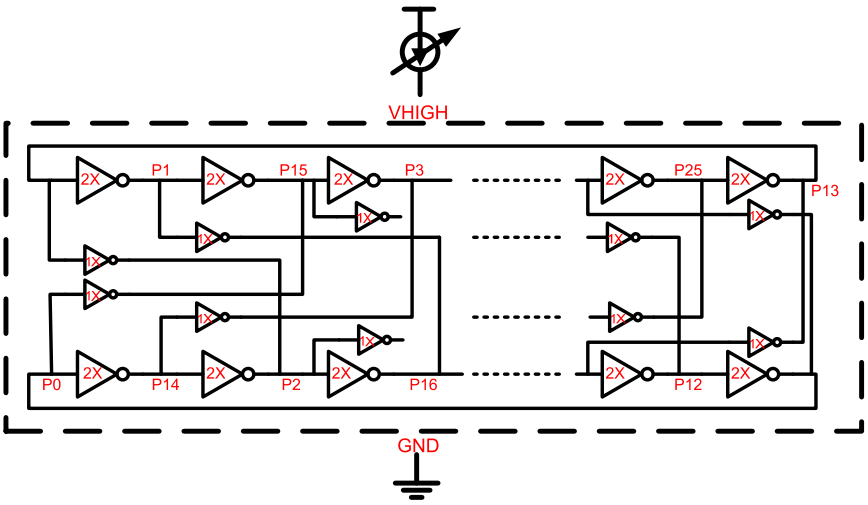

Figure 5.3: Differential Ring Oscillator with Multi-Path

TDC is essentially the DCO itself, this 30ps is the quantization error of the TDC. The quantization error of the TDC will directly impact the in-band phase noise at the PLL output since the transfer function from this point to the PLL output is low pass. The relationship between PLL output phase noise and TDC quantization noise

$$PN\ (Phase\ Noise) = 10log[\frac{(2\pi)^2}{12}\left(\frac{\Delta t_{inv}}{T_v}\right)^2\frac{1}{f_R}] \tag{5.2}$$

where Δt_{inv} is the delay per stage in the ring oscillator, T_v the oscillation period, and f_R the reference frequency [11]. Given delay per stage of 30ps, oscillation period of 1111ps, and reference frequency of 10MHz, the in-band phase noise contribution from the TDC quantization error is at -96dBc/Hz. Assuming the reference clock into this PLL has phase noise of -130dBc/Hz at close-in, because the division ratio between DCO frequency and reference frequency is 90, and the phase noise gets amplified by [25, 26]

$$20log(DivisionRatio)\ dB$$

the in-band noise floor at the PLL output from the reference clock will be slightly better than -90dBc/Hz. Therefore, in this design, the TDC quantization error will not be a dominant factor contributing to the phase noise.

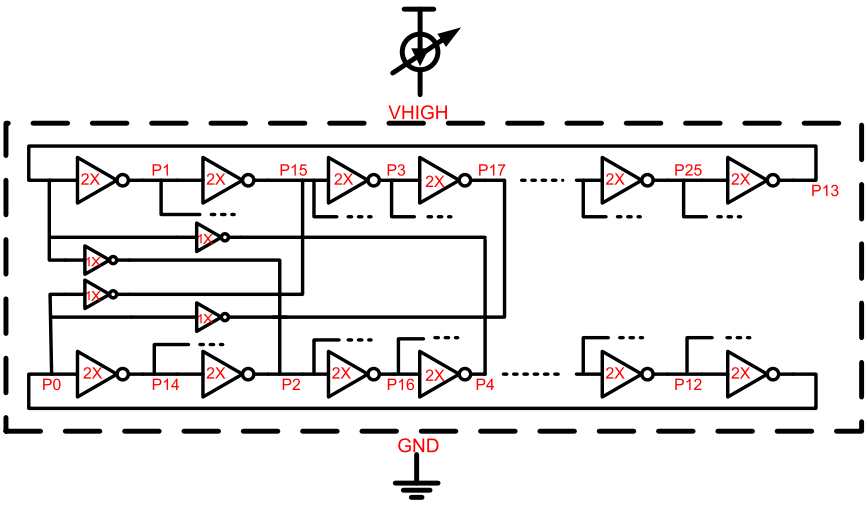

Figure 5.4: Differential Ring Oscillator with More Degrees of Multi-Path

5.1.1.2 Digital to Analog Converter

The digital to analog Converter (DAC) shown in 5.3 is a 16-bit current source DAC. This current source, shown in figure 5.6, has the higher 6 bits statically set through a serial interface, and the lower 10 bits controlled by the PLL. Among this lower 10 bits, the upper 5 bits are made of unitary arrays to insure monotonicity and linearity. A binary-to-thermometer decoder converts binary data to thermometer format in order to control the unitary arrays. The lower 5 bits is through a 1^{st} order sigma delta modulator operating at half of the DCO frequency. The sigma delta modulator, shown in figure 5.5, is simply a 5 bit accumulator and the output of the modulator is the top carryout (CO) bit.

Writing out the Z-domain transfer function

$$-E = (K - E \bullet z^{-1}) - CO$$

$$CO = K + (1 - z^{-1})E$$

The average of the modulator output (CO) is equivalent to the input of the modulator, and the quantization error (E) goes through a high pass filter. The size of the 1X current source in figure 5.6 is chosen to allow mismatch among them smaller than the finest bits out of the sigma delta modulator.

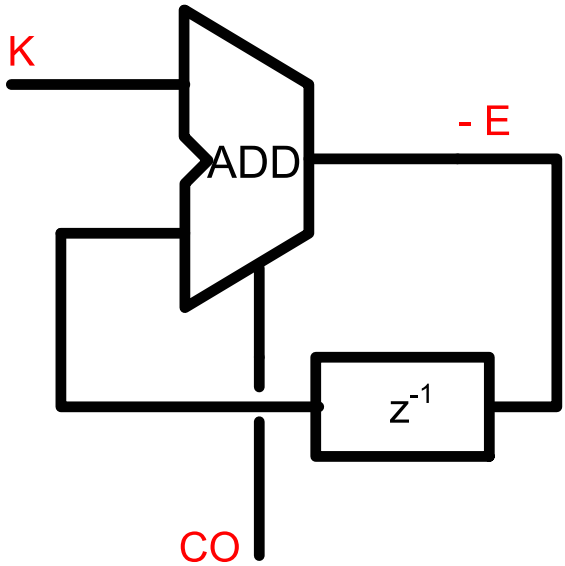

Figure 5.5: Sigma Delta Modulator

In simulation, the finest bit can alter the frequency by 30kHz at 915MHz oscillation frequency. Since the lower 10 bits are controlled by the PLL, the loop can tune the frequency of DCO by 30MHz. The higher 6 bits use binary arrays, which tend to result in large variations. To make sure the DCO can output any frequency within the desired range, the tuning range of the entire fine control is 32X, which is twice the magnitude of the least significant bit of the coarse control. This redundancy helps resolve potential issues related to binary array mismatches. The switches for the current sources are placed on top of the current sources to minimize capacitive coupling to the supply node (VHIGH node in figure 5.3) of the ring oscillator.

5.1.1.3 A DCO without a Current Source DAC

In this work, the current source DAC used to control the ring oscillator oscillation frequency is the only block in the PLL not designed with standard cells. There are ways to design a DCO using only tri-state buffers, which exists in standard cell libraries. By altering the number of buffers that is on at each stage, the oscillation frequency will change accordingly [37]. Figure 5.7 shows an example of using tri-state buffers to form a DCO. The layout of this DCO architecture can be tedious and the power consumption would

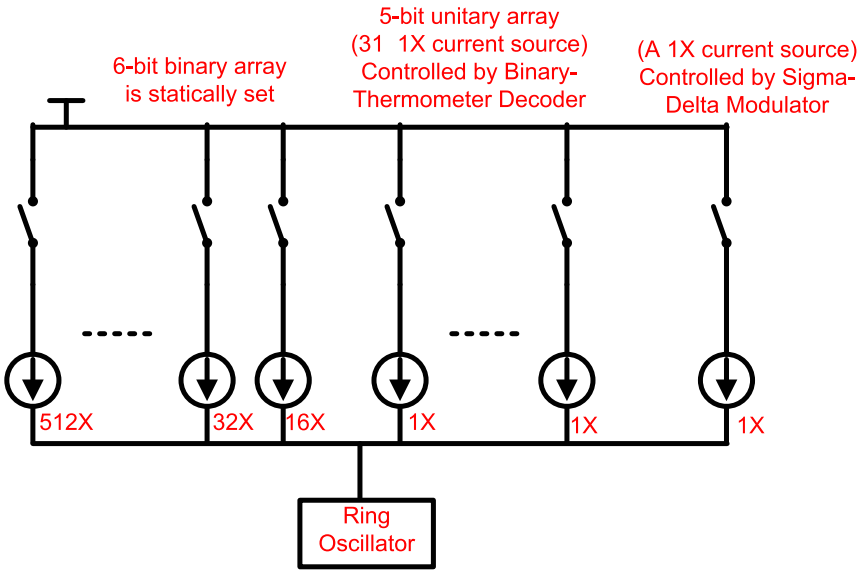

Figure 5.6: DAC

be higher because in order to achieve the frequency resolution needed, each stage of the ring needs to have a great number of parallel tri-state buffers. A similar DCO architecture that does not require current source DAC is shown in figure 5.8. The frequency resolution of this structure tends to be fairly limited and due to the additional load added at the output of each inverter, the power consumption will be higher compared to a current starved ring oscillator. However, either of these structures could be a great alternative for a standard-cell DCO.

5.1.1.4 Integer Counter and Phase Quantizer

The integer counters used in this design are asynchronous counters composed of a chain of DFFs with each DFF having its inverse of output connected back to the input, as shown in figure 5.9. This design uses two sets of counters. When the first counter is counting the number of VCO cycles that has taken place within the current reference cycle, the system is reading in the final count from the second counter, which represents the number of VCO cycles that had taken place within the previous reference cycle. Essentially, the two sets of counters are ping-ponged between two consecutive reference cycles.

The phase quantizer, shown in figure 5.10, is composed of 26 DFFs that

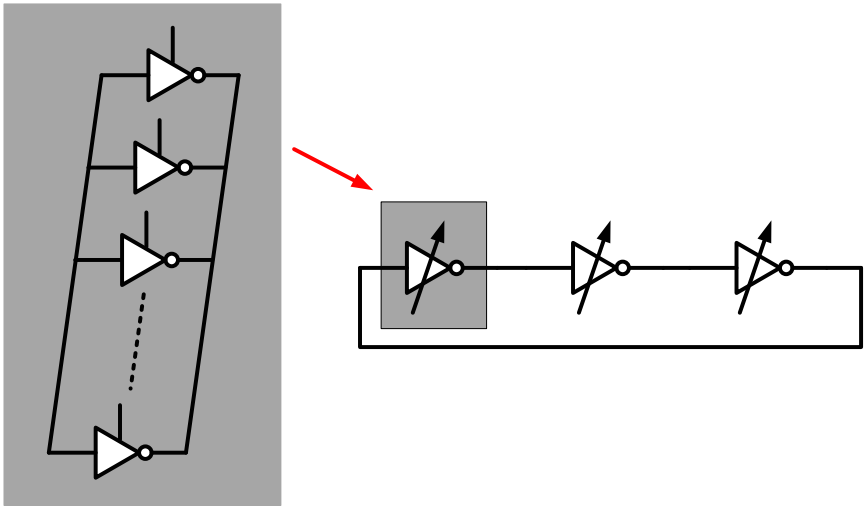

Figure 5.7: DCO with Tri-state Buffers

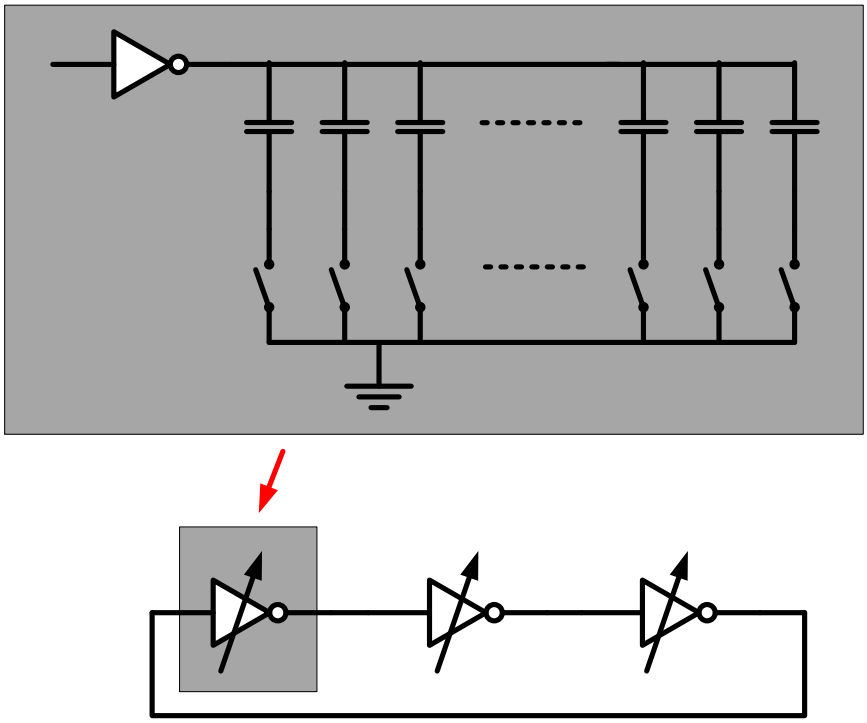

Figure 5.8: DCO with Capacitors and Switches

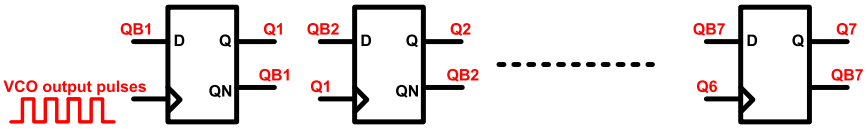

Figure 5.9: Integer Counter

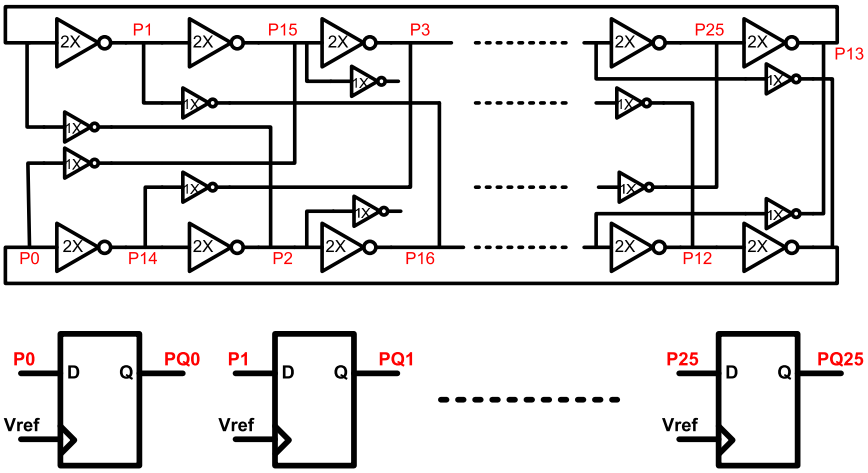

Figure 5.10: Phase Quantizer

sample intermediate nodes inside the DCO at the rising edge of the reference clock.

In this design, the integer counter increments at every rising edge of P0. If the rising edge of P0 has propagated to, for example, P2, the fractional count output from the phase quantizer will be 2. The output of the phase quantizer follows:

$$Fractional\ Count = 0\ if\ PQ < 25:0 >= 1xxx...xxx001$$

$$Fractional\ Count = 1\ if\ PQ < 25:0 >= xxx...xxx0011$$

$$\vdots$$

$$Fractional\ Count = 25\ if\ PQ < 25:0 >= 11xxx...xxx00$$

.

The linearity of the phase quantizer will impact the magnitude of the fractional spur at the PLL output [6]. The DFFs in the phase quantizer are placed within close proximity to have better matching among themselves. Monotonicity is also important. In the event that this phase quantizer is not monotonic, it may be hard to interpret the output from the phase quantizer. Monte-Carlo simulations are used to verify that this phase quantizer is monotonic with 3-sigma level of confidence. In our implementation, to ensure that there are no monotonicity issues due to mismatches between consecutive DFFs, a fractional count is picked when at least two adjacent DFFs outputs are high. In the event that only a single DFF outputs a high, an error flag is stored. During our testing, no error flag has been detected.

Because the pull-up and pull-down strength of DFFs may not be equal, the edge of a given stage in the DCO may be captured by the DFF before the corresponding edge of the prior stage on a given reference clock cycle. To avoid this problem, we use a differential DCO to ensure that we are always sampling the same type of edge transition. A differential DCO is chosen to achieve better TDC linearity and monotonicity. This helps reduce the magnitude of the fractional spurs in this fractional-N PLL.

5.1.1.5 Digital Loop Filter

The digital loop filter is a proportional and integral (PI) controller. The integral path ensures that the loop will not settle until the phase offset reaches zero, and the proportional path is added to help stabilize the system, as the DCO and the integral path each contribute a pole to the transfer function at DC [14]. This loop filter runs on the reference clock, and the proportional and integral coefficients, α and β, allows 5 bits of tuning range. Given the loop bandwidth and phase margin, the proportional and integral coefficients can be found [18]. The phase margin of this PLL is chosen to be 45 degree, and the loop bandwidth is chosen to be 1MHz. To figure out the digital loop filter coefficient, we first find Kp and Ki based on the derivation shown in 2.2.2.2. The Kp and Ki found are for a continuous-time analog filter (figure 5.11). Bilinear transformation is used to convert those coefficients to the ones of a digital loop filter (figure 5.12).

$$s = \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}}$$

where $T_s$is the reference clock period of the PLL.

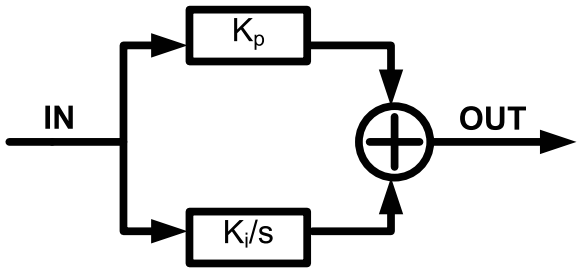

Figure 5.11: Continuous-Time Filter

The s-domain transfer function of the analog filter is

$$H_{analog}(s) = K_p + \frac{K_i}{s}$$

Through the bilinear transformation

$$H_{analog}(z) = \frac{\frac{K_i T_s}{2} + K_p + z^{-1}(\frac{K_i T_s}{2} - K_p)}{1 - z^{-1}}$$

$$H_{digital}(z) = \alpha + \beta \frac{1}{1 - z^{-1}} = \frac{(\alpha + \beta) - \alpha z^{-1}}{1 - z^{-1}} = H_{analog}(z)$$

$$\alpha = K_p - \frac{K_i T_s}{2}$$

$$\beta = K_i T_s$$

5.1.1.6 Digital Correction Circuitry

This fractional PLL also includes a digital correction circuitry. Without such correction, this PLL would not have worked. Figure 5.13 helps illustrate why there is a need for such a correction. Both the reference clock and DCO signals go into the integer counter and phase quantizer. In an ideal situation when there is no signal path mismatch between reference clock path and DCO signal path, the correct answer will be 89.7 as seen in figure 5.13. However, due to path mismatch, the reference clock may arrive at

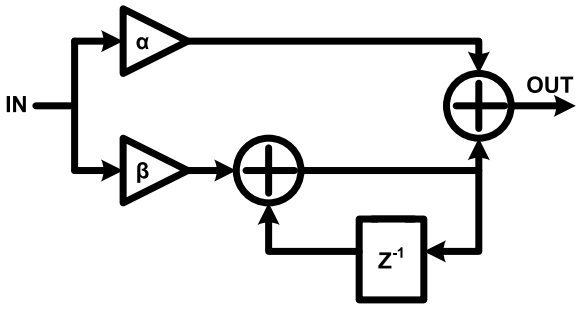

Figure 5.12: Digital Loop Filter

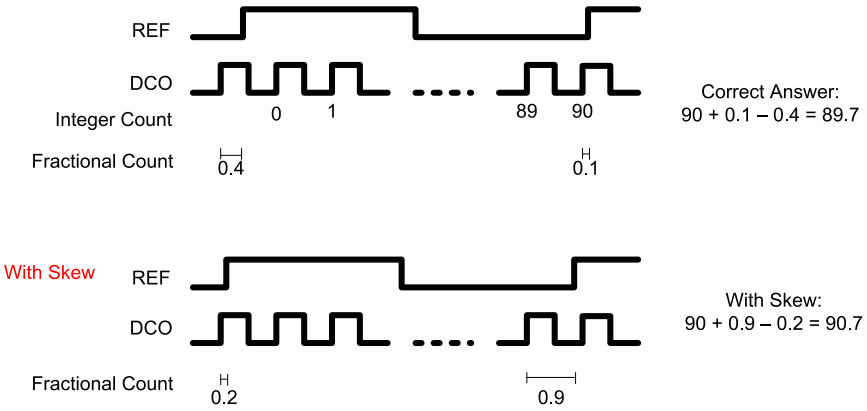

Figure 5.13: Integer Mis-count

phase quantizer earlier or later with reference to the DCO signal [13]. In this particular example, the reference clock arrives at the phase quantizer earlier with reference to the DCO signal, and results in an incorrect answer of 90.7.

The digital correction works in the following way to detect and correct this mis-count due to signal path mismatch. At the start-up of the PLL operation, a state machine will locate a correct count by looking through the history of previous summations from integer counter output and phase quantizer output. This correct count is continuously updated over the course of the PLL operation. By comparing the current count with this correct count, the state machine can detect and correct a mis-count whenever it happens.

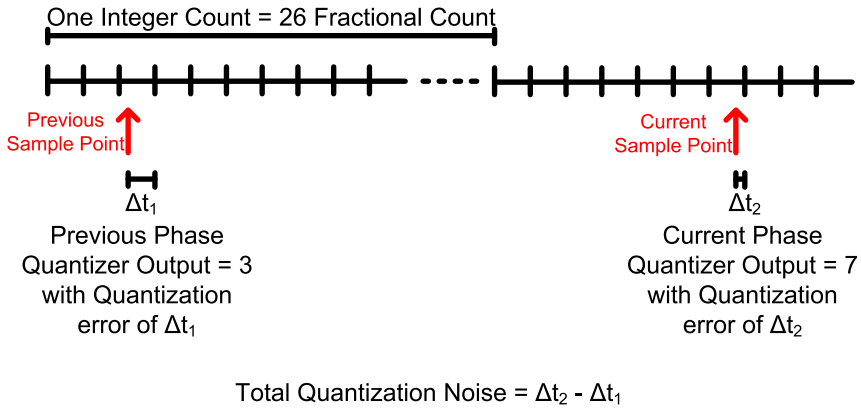

Figure 5.14: First Order Noise Shaping

5.1.1.7 First Order Noise Shaping

Having the TDC embedded into the DCO results in one additional benefit. Because the quantization noise from the previous reference cycle is accumulated to the current reference cycle, there is a first order noise shaping on its quantization noise. First order noise shaping is essentially a high pass filter that attenuates the low frequency components and amplifies the high frequency components. In other words, the impact of the quantization noise to the PLL output at close to DCO center frequency is attenuated. This idea can be better illustrated with the help of figure 5.14. The total quantization noise at each reference cycle is the difference between the quantization noise from the current reference cycle and the previous reference cycle. A first order noise shaping results.

5.1.2 Power Amplifier

The power amplifier in the transmitter is shown in figure 5.15. A final stacked driver follows a chain of inverter drivers. The purpose of this final stacked driver is to provide better impedance matching to the 50Ω antenna [17]. With a target output power of 0dBm, and voltage headroom of $1.4V_{p-p}$, the estimated current consumption from supply will be around 1.75mA. However, with a single inverter pushing/pulling 3.5mA, and V_{p-p} of 1.4V, the natural impedance will be $0.7\text{V}/3.5\text{mA} = 200\Omega$. A stacked structure can help provide better impedance matching to the 50Ω antenna. With the stacked

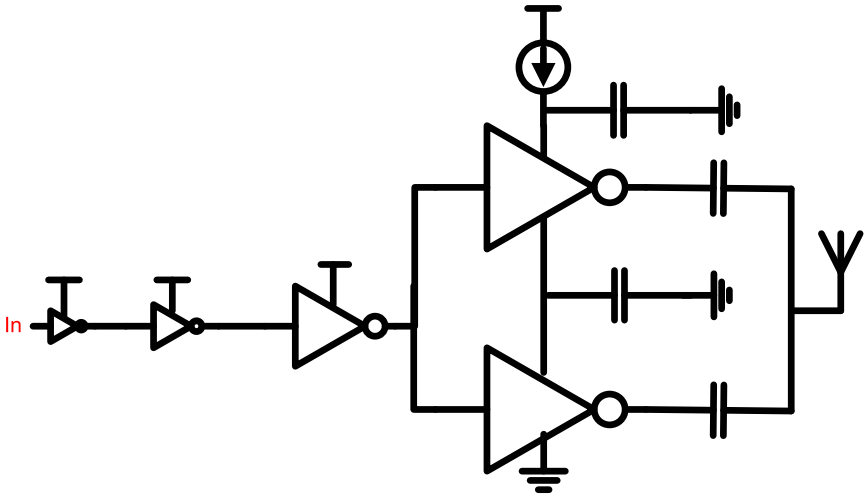

Figure 5.15: Power Amplifier

structure, assuming PMOS and NMOS as ideal switches, the V_{p-p} will be 0.7V. With two drivers, each pushing/pulling 3.5mA, the natural impedance will be 0.35/7mA = 50Ω.

5.2 Receiver

The reference frequency for the PLL is chosen to be at 10MHz. This results in channel spacing of 10MHz, which allows two channels to exist at 915MHz ISM band.

5.2.1 All-Digital Integer-N PLL

The all-digital integer-N PLL architecture is shown in figure 5.16. The bang-bang phase detector, a 1-bit TDC, compares the output from the programmable divider with the stable reference. The resulting phase difference goes through a loop filter before controlling the oscillator frequency. In order to demonstrate a radio with multiple channels, a programmable divider, rather than a fixed divider, is included in this PLL to allow a programmable output frequency f_{osc}. The digital loop filter block is a PI controller identical to the one discussed in 5.1.1.5 and will not be covered in this section.

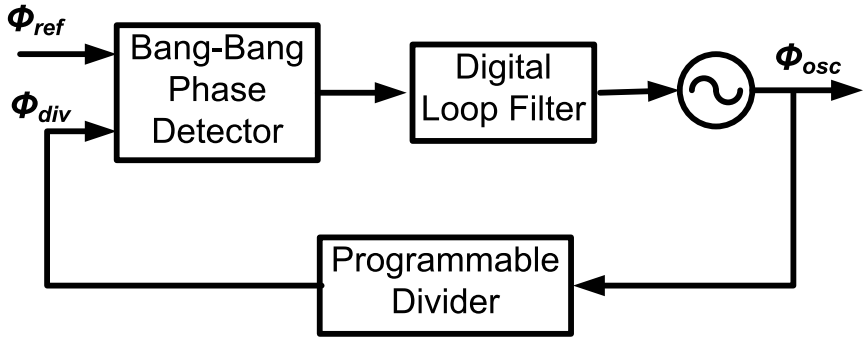

Figure 5.16: All-Digital Integer-N PLL Architecture

5.2.1.1 Bang-Bang Phase Detector

Bang-bang phase detectors have been used in integer-N PLL to achieve great jitter and phase noise performance. Rather than using a multi-bit TDC and a phase quantizer, this integer-N PLL uses a bang-bang phase detector (BBPD), shown in figure 5.18, to compare the reference phase with the divider output phase. A BBPD, when used in a PLL, makes the loop a non-linear system, as the overall loop gain changes depending on how big the phase error is at the input of the BBPD. When the phase error is large, the gain of the BBPD is reduced, which decreases the loop gain and vice versa. In order words, a PLL using BBPD (BBPLL) will never achieve oscillation. However, a BBPLL sometimes gets a bad reputation because it exhibits output noise even when there is no noise input to the system, a phenomenon called a limit cycle. Nevertheless, BBPLLs are the simplest and lowest power TDC possible, and it has been shown that a PLL with BBPD can be designed to match the performance of a linear PLL if the phase and frequency steps are chosen correctly [19]. This BBPD used in our design is similar to the popular phase frequency detector (PFD) commonly used in mixed-signal CPPLLs. In a PFD, the two outputs from the two DFFs, shown in figure 5.17, are used to turn on switches for two current sources in a CPPLL. In this BBPD, the two outputs are sent into a latch followed by a metastability filter made of two inverters cross-coupled through their supplies [15]. The final output of this BBPD then decides whether the DCO should speed up or slow down. The outputs of these two DFFs are normally low, forcing the outputs of the NAND-gates to be high and outputs of the metastability filter to be low. If the rising edge of the Vref arrives before Vdiv, V_q and V_qb_final will be

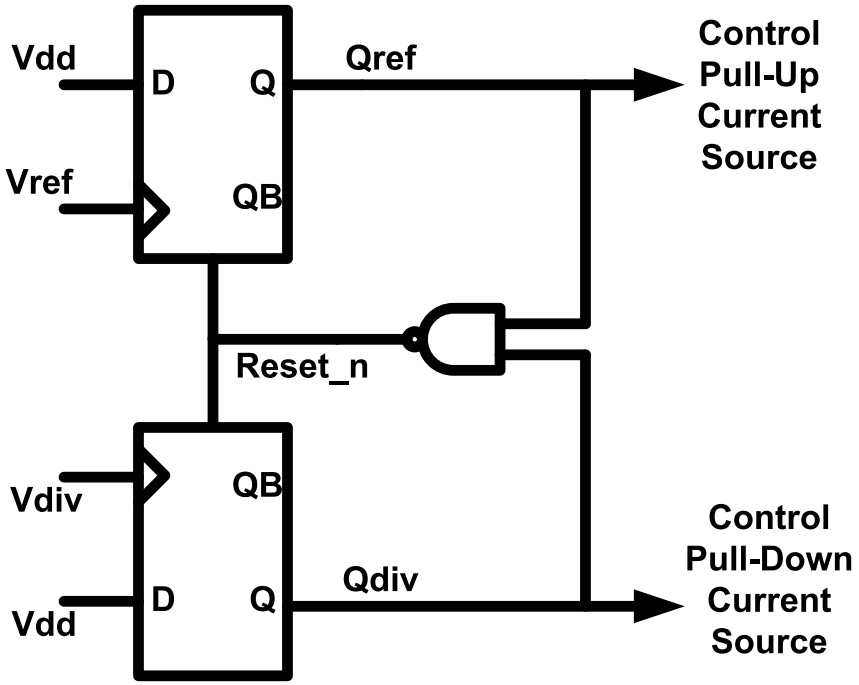

Figure 5.17: Phase Frequency Detector in Mixed-Signal CPPLLs

driven low, whereas V_qb and V_q_final stay high. The reset signal will be raised through additional circuitry not shown here after Vref and Vdiv both rise high and output of the metastability filter has settled.

5.2.1.2 Ring Oscillator

The ring oscillator for this integer-N PLL is composed of two inverter chains with cross-coupled latches, as shown in figure 5.19. This ring oscillator does not have any multi-paths like those in figure 5.3 because there is no TDC in this integer-N PLL and there is no quantization noise associated with this PLL. The DAC in the figure is identical to the one described in 5.1.1.2 and will not be covered in this section. The differential output of this ring oscillator go through a pair of cross-couple NOR gates to form non-overlapping clock signals to drive the passive mixer [34].

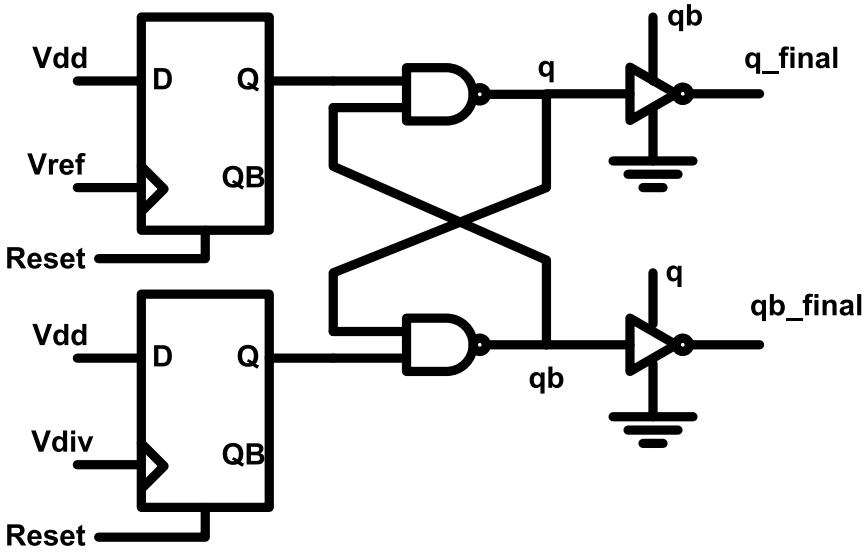

Figure 5.18: Bang-Bang Phase Detector

5.2.1.3 Programmable Divider

To have the receiver operate in multiple channels, a programmable divider, rather than a fixed divider, is implemented. This programmable divider consists of a prescaler, which divides the 910MHz clock signal down by a factor of 10 or 11, and a programmable counter and a swallower counter that each may be reset [16]. A circuit diagram of this programmable counter is shown in figure 5.20. The prescaler is a chain structure, and it divides the oscillator output by 10 or 11 depending on whether the ctrl signal from the swallow counter is high or low. The sole purpose of the swallow counter is to swallow up one additional count from the oscillator cycle to achieve a total division factor other than a multiple of 10.

As an example to illustrate the operation of this programmable counter, when dividing a 910MHz clock signal down to 10MHz, the programmable counter is preset to 9 whereas the swallow counter is preset to 1. Since the swallow counter is preset to 1, the ctrl signal into the prescaler will initially force the prescaler to swallow up one additional oscillator cycle. After that, the prescaler will go back to divide oscillator frequency by 10. The final division will therefore be 91.

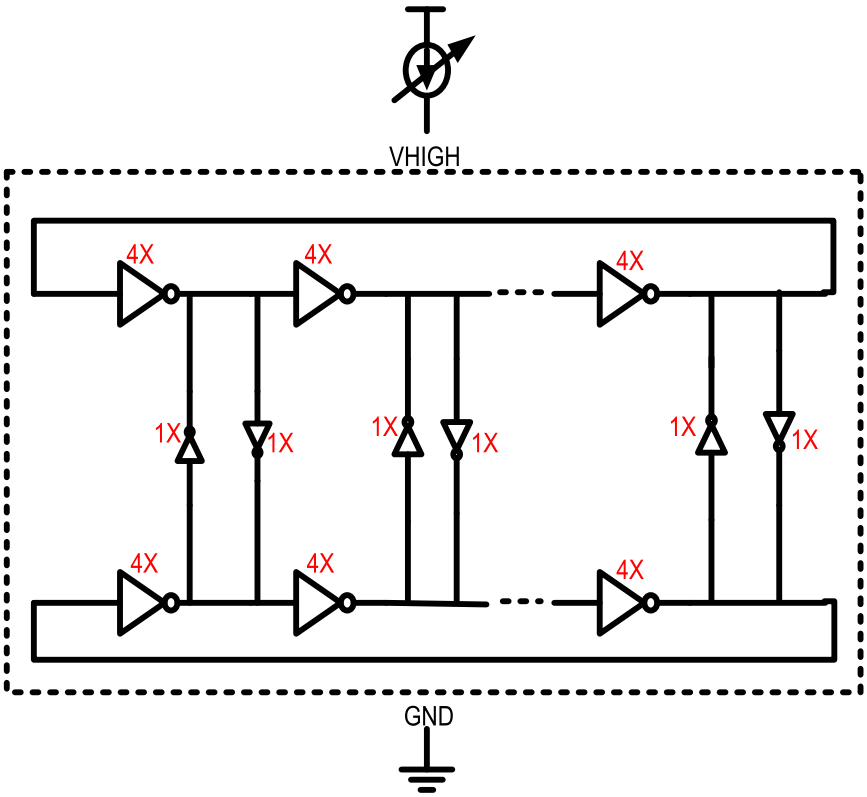

Figure 5.19: Ring-Oscillator

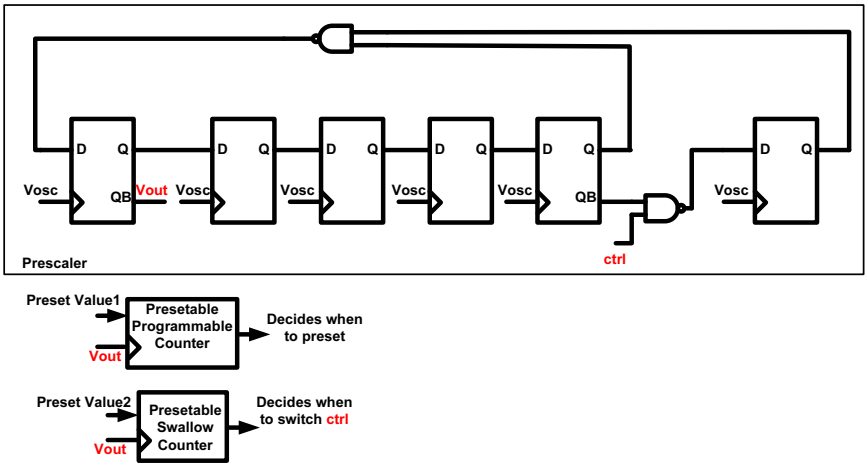

Figure 5.20: Programmable Divider

5.2.2 Receiver Front-End

Figure 5.21 illustrates the receiver circuits. The low-noise amplifier (LNA) is a self-biased inverter [17]. LNA is biased with pass-transistor logic. M3 functions as a resistor. A passive mixer follows the LNA. The mixer is driven by a frequency synthesizer. In this prototype, the frequency synthesizer generates a 910MHz clock from a 10MHz reference. The LNA converts the input voltage to current, which is alternately driven to one of two output capacitors by a pair of passive switches. In other words, the switches in the mixer sample the RF input voltage at the LO frequency. This LNA provides maximum gain, 20dB, at low power consumption, and its NF can be estimated as:

$$NF = \frac{1}{(g_{m1} + g_{m2}) \times 50} + 1 \ \ (Assuming\ \gamma = 1) \tag{5.3}$$

Simulation shows that the NF of this LNA is 5.5dB at 915MHz band, which matches well with the estimate from equation 5.3. The mixer contributes noise by converting noise from the image band as well as all odd harmonics down to baseband, and the NF of the mixer is 4.1dB from simulation. The total NF from simulation is 9.6dB which matches well with the 10dB measured from the test chip.

This receiver architecture provides great wide-band linearity by suppressing wide-band interferers at the intermediate RF node between the LNA and the mixer [3]. The amount of interference suppression is no comparison to SAW filters, but since the intention is to demonstrate a fully integrated receiver without any off-chip components (inductors or filters), this wide-band linearity is critical in desensitizing the LNA to wide-band interferers that would otherwise drive the LNA transistors into triode. Additionally, a resonant antenna can be used to provide additional filtering at the front-end.

5.3 Measurement Results

The measurement is done through a chip-on-board. Successful wireless communication is achieved with TX and RX at least 1 meter apart at data rate of 10kbps as shown in figure 5.22.

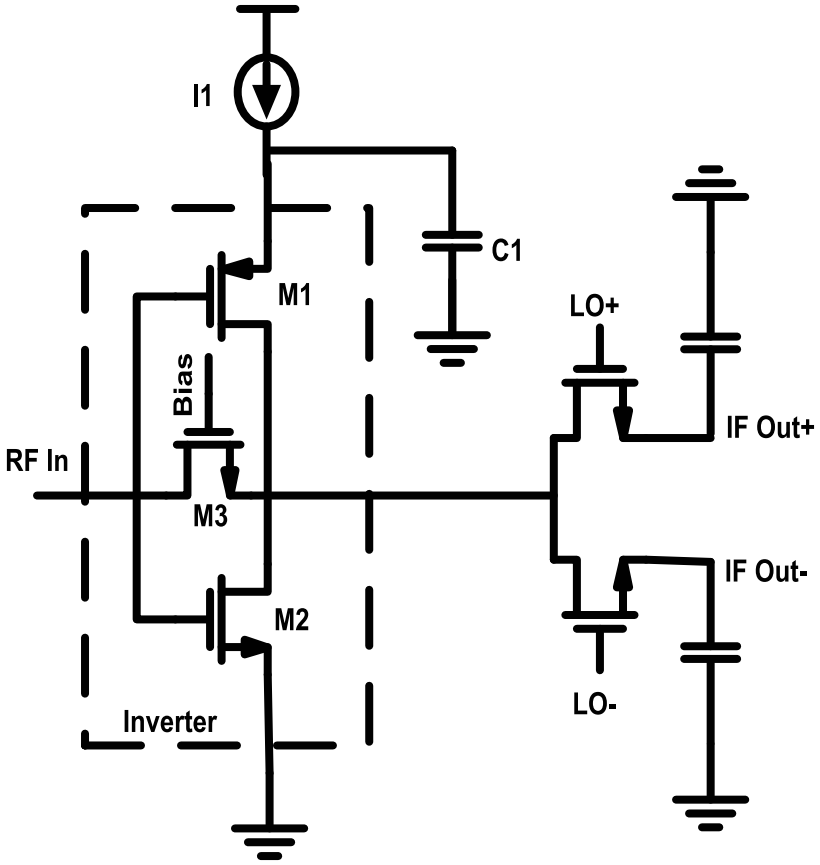

Figure 5.21: Receiver Front-End

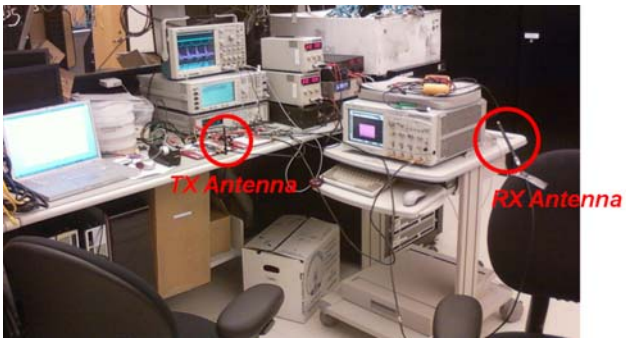

Figure 5.22: Wireless Communication

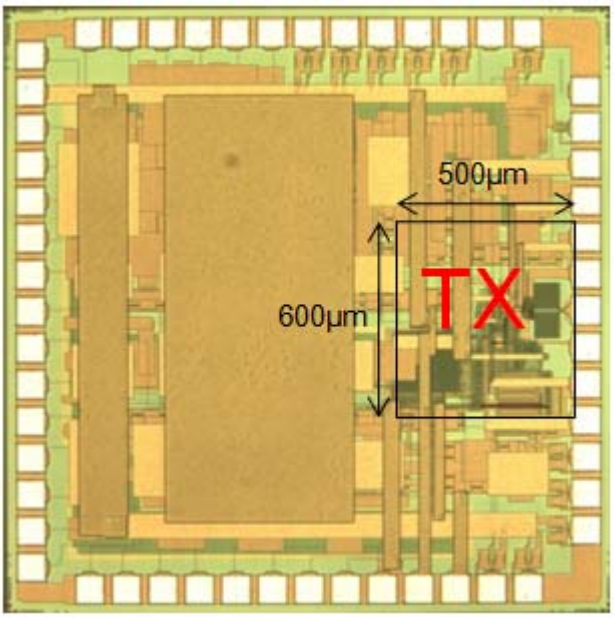

Figure 5.23: Transmitter Die Photo

5.3.1 Transmitter Measurement

The entire transmitter occupies 600μm x 500μm of area, in which all-digital fractional PLL takes up 500μm x 500μm, whereas the rest of area is taken up by the PA. The PA efficiency, including power drawn from the chain of inverter drivers, is 8% at -3dBm. A die photo of the transmitter chip is shown in figure 5.23. This design is pad-limited because additional signals are routed to the pads for testing purpose.

For the phase noise and jitter measurement, an Agilent signal source outputting clean 10MHz square wave is used as the reference. The phase noise measurement, figure 5.26, shows PLL bandwidth of 1MHz, -90dBc/Hz at 1MHz offset. The largest fractional spur of -35dBc at 400kHz offset and the largest reference spur is -50dBc at 10MHz offset. The jitter measurement, figure 5.25, shows rms period jitter of 2.6ps after looking at more than 10^6 cycles. The peak-to-peak period jitter of 26ps matches well with our expectation because the DCO frequency is close to 10^2 times the reference frequency. The entire PLL consumes 8.6mW, while the DCO consumes 2mW by itself. Table 5.1 compares this fractional PLL with two other recently published work.

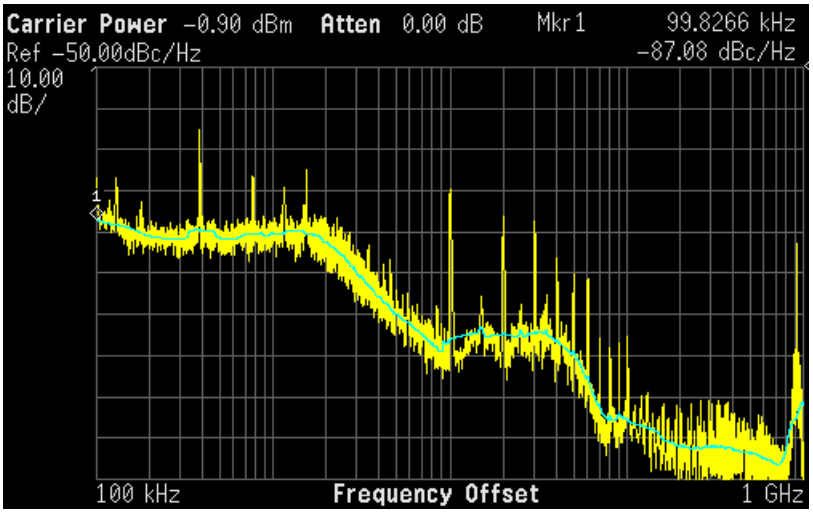

Figure 5.24: Phase Noise Measurement

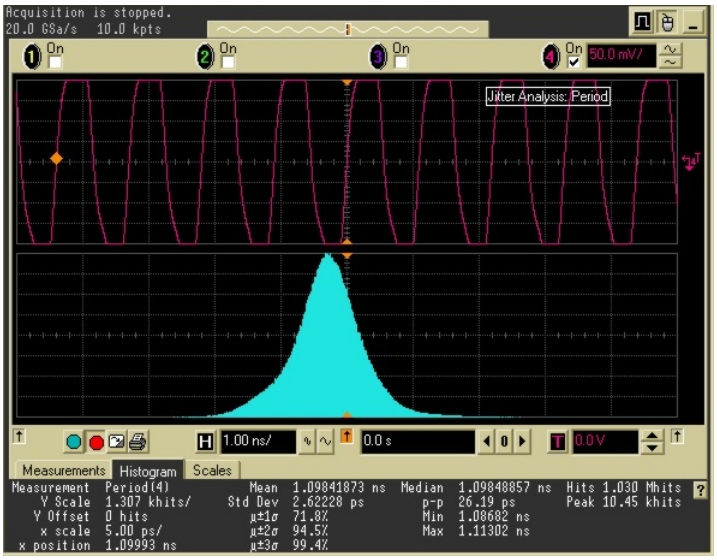

Figure 5.25: Jitter Measurement

Table 5.1: Performance Summary and Comparison

	[9]	[10]	This Work
Technology	65nm	65nm	.18μm
DCO Frequency	800MHz	750MHz	900MHz
Reference	2MHz - 40MHz	25MHz	10MHz
Period Jitter (rms)	N/A	4ps	2.6ps
TIE Jitter (rms)	21.5ps	N/A	13.9ps
Power Consumption	2.6mA	3.4mA	4.8mA
Area	$.027mm^2$	$.046mm^2$	$.25mm^2$

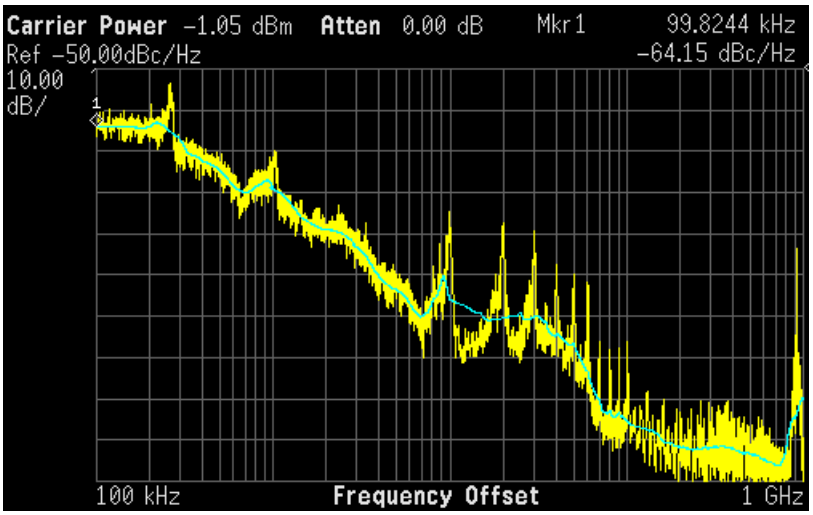

Figure 5.26: Phase Noise Measurement with Digital Correction Circuitry Off

As a demonstration, phase noise measurement results without digital correction circuitry on, discussed in 5.1.1.6, is shown in figure 5.26. Compared to figure 5.28, figure 5.26 has much higher phase noise within the bandwidth of the loop. This fractional PLL would not have worked without this digital correction circuitry.

To transmit FSK signals from this transmitter, a stream of 1's and 0's is sent into the PLL to change the division ratio of the PLL. The DCO output frequency is changed correspondingly. This results in direct modulation with the output being binary FSK signals.

5.3.2 Receiver Measurement

The test setup for the receiver is as follows. A signal source generates a FM signal with square wave modulation, which is essentially a FSK signal. This signal is then sent into the receiver. It goes through the LNA, gets mixed down to the baseband, and receives further amplification from a baseband amplifier. It then goes through a source follower before reaching the pad. This signal is then directly captured using an oscilloscope at a speed of 50M sample/s. With the baseband bandwidth of 2MHz, the analog waveform is oversampled by at least a factor of 10. All the digitized data is sent into a matlab script for demodulation.

The PLL in the receiver can operate in three different modes.

1. When this PLL is enabled, a 10MHz clean clock signal from an Agilent source is sent into the PLL as the reference clock. In this mode, the phase noise of the integer PLL is measured to be -80dBc/Hz at 1MHz offset with the largest reference spur at -55dBc, as shown in figure 5.28. The bandwidth of this PLL is designed to be 1MHz, but only has bandwidth of 300KHz from the measurement. The cause of this discrepancy is lack of PI controller coefficient tuning range.

2. When the PLL is disabled, the power spectrum of the free-running DCO spreads over a 2MHz band. When the DCO is free-running, its operating frequency jumps quickly from one to another. A comparison of the power spectrum of the free-running DCO and that of the DCO locked to a 10MHz reference through a PLL is shown in figure 5.29.

3. When this PLL is injection locked, a very clean signal generated from an Agilent signal source at the frequency of the DCO oscillation frequency is injected into the ring oscillator as shown in figure 5.27. When the frequency of the signal injected is close to the oscillation frequency of the free-running DCO, the DCO will be injection locked by this clean signal. The phase noise performance of the DCO will be dramatically improved and can come close to the clean signal injected. This feature of injection locking is added into the system to help realize how DCO phase noise can deteriorate the receiver sensitivity, and this will become clear in the next paragraph. The measured DCO phase noise with injection locking mechanism on is shown in figure 5.30. The phase noise at 100Hz away from carrier is already better than -90dBc/Hz in this case.

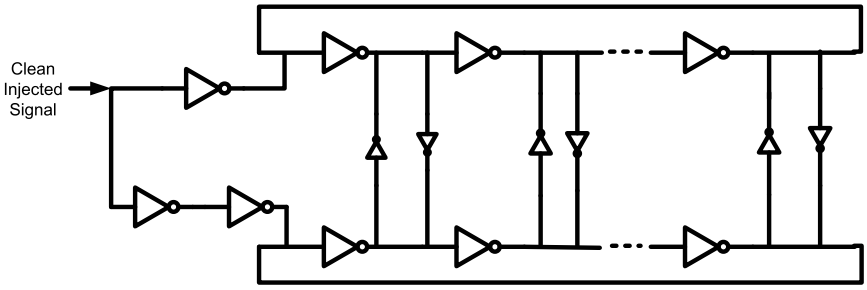

Figure 5.27: Injection Locking Mechanism

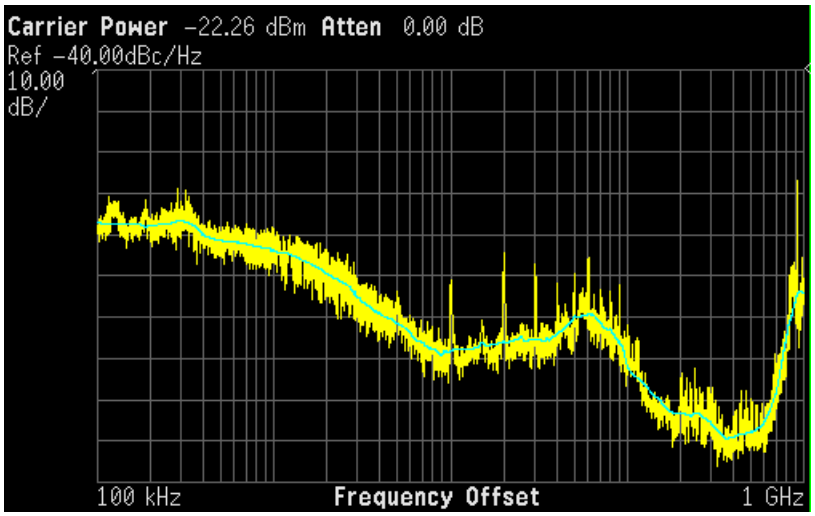

Figure 5.28: Phase Noise Measurement

The entire receiver occupies 600μm x 500μm of area, and has sensitivity of -76dBm at 10kbps. The power consumption of the receiver is 6mW. The receiver can successfully demodulate an alternating data stream 101010... with a bit error rate (BER) better than 10^{-3} when the signal strength is larger than -76dBm. A die photo of the receiver is shown in figure 5.31.

Given the receiver front-end NF of 10dB, required demodulation SNR of 10dB, baseband bandwidth of 2MHz, the sensitivity is estimated to be

$$Sensitivity = -174dBm + NF + SNR + 10log(Bandwidth)$$

$$Sensitivity = -174dBm + 10dB + 10dB + 63dB = -91dBm$$

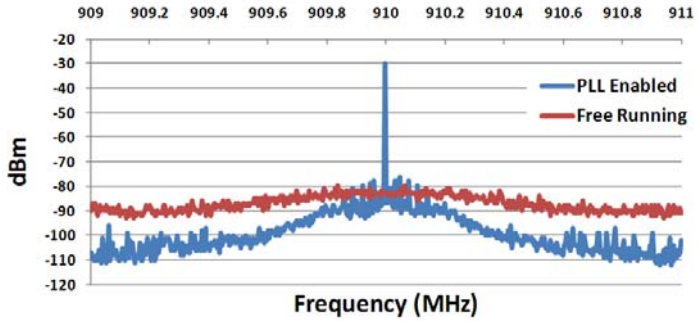

Figure 5.29: Free-Running versus PLL Enabled

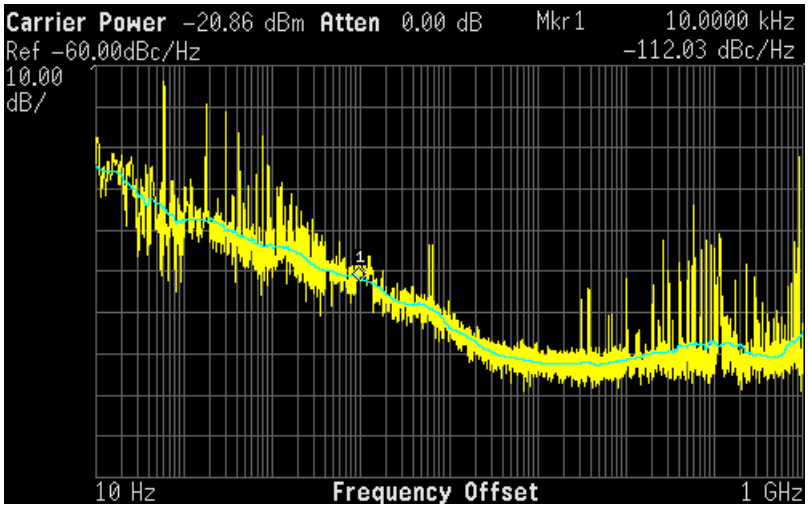

Figure 5.30: Injection-Locked DCO Phase Noise

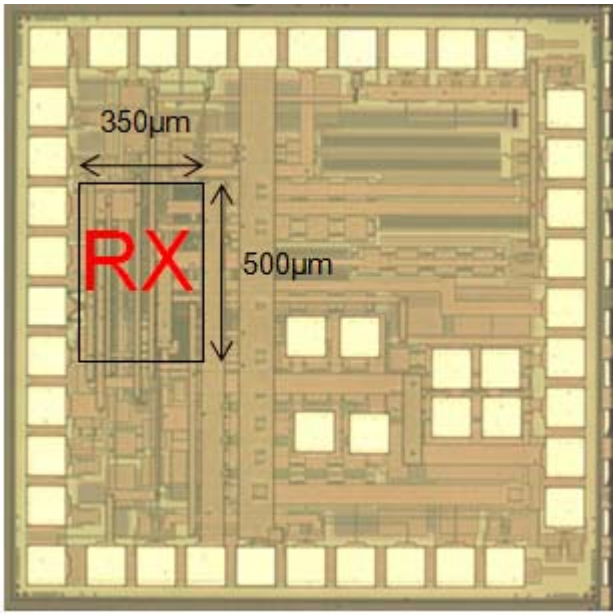

Figure 5.31: Receiver Die Photo

However, the measured sensitivity is -76dBm, which is 15dB higher than the estimated sensitivity. This is actually expected because a ring oscillator is used for LO generation. All the far-out noise from the receiver front-end outside the band of PLL is down-converted to baseband due to the inferior phase noise performance of a ring oscillator. Most wireless communication systems use LC oscillators for LO generation because LC oscillators provide much cleaner reference. To verify this degradation on the sensitivity is purely due to the inferior LO phase noise, sensitivity is measured with a very clean LO signal generated by the injection locked DCO. The measurement results show that the sensitivity can be as good as -93dBm when the LO signal is very clean.

Chapter 6

Transmitter Design in a 65nm Process

The proof of concept presented in chapter 5 is a radio built almost entirely with standard cells. In order to illustrate the idea of portability, the transmitter design is ported to a 65nm STMicroelectronics Standard CMOS process. Just as the transmitter discussed in 5, this direct modulation transmitter is composed of a fractional-N PLL and a power amplifier. This chapter will present our implementation of the transmitter in a 65nm process.

This 65nm transmitter is similar to the one discussed in 5. One minor design change is incorporated. A single synchronous integer counter, shown in figure 6.1, is used in the 65nm design. Previous design in .18μm CMOS uses two asynchronous integer counters to find out the number of integer DCO cycles in each reference cycle. Porting the existing transmitter, including design and layout, from a .18μm process to a 65nm one took a single engineer one month. With additional CAD support, the time it takes to port from process to process or from technology to technology can be reduced.

Other than paying attention to the precautions mentioned in 5.1.1, here are the steps taken to port the .18μm design to a 65nm process and complete this transmitter design.

1. The DCO is simulated using the 65nm model to ensure that it can oscillate at frequencies up to 2.4GHz in all process corners. Parasitic extraction needs to be performed after layout to make sure that the DCO can still oscillate at frequencies up to 2.4GHz. This requires transient simulations.

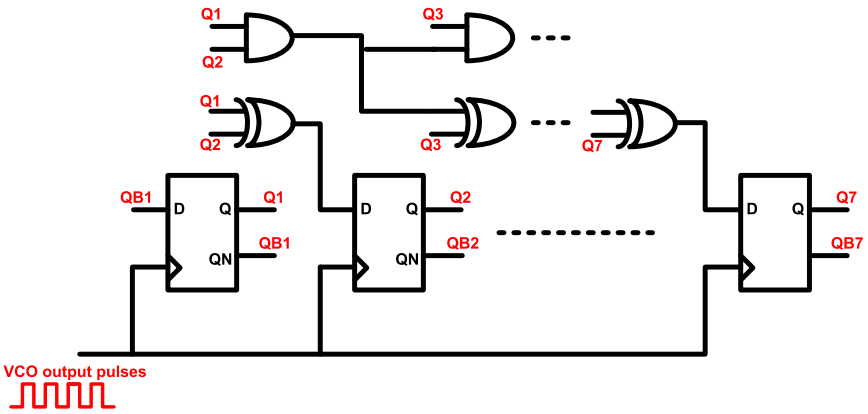

Figure 6.1: Synchronous Counter

2. Different sizes of DFFs are included in standard cell libraries, 1X, 2X, and etc. The larger the DFFs, the less the mismatch between them. Monte Carlo simulations are run to ensure the monotonicity and estimate the mismatch between the DFFs in the phase quantizer and to decide the size of these DFFs. In this particular process, DFFs with size 1X are sufficient to achieve monotonicity. When laying out the phase quantizer, one needs to be careful in placing the DFFs and connecting them with the DCO outputs to make sure the final phase quantizer outputs stay monotonic.

3. The integer counter and the sigma delta modulator are simulated to ensure that it can operate when DCO oscillates at frequencies up to 2.4GHz in all process corners and with parasitic capacitors and resistors added. This requires transient simulations.

4. The current source DAC needs to be sized to have smallest DCO frequency step of 60kHz, and mismatch smaller than the lowest bit to ensure monotonicity. As a result, these current sources are not minimum length devices.

5. The remaining digital block is synthesized through Verilog. The behavioral Verilog code is taken directly from the .18μm design. Assuming the digital synthesis tool flow is set up correctly, this part of the design can be completed within a day. This part of the design runs off the

20MHz reference clock. However, it is still important to make sure that there are no setup and hold time violations.

6. A complete design is then put together for a full-chip simulation. Given the number of gates in this design, it is difficult to use Spectre to run a long transient simulation to see the PLL achieves locking. BDASim, a much faster simulator compared to Spectre, is used to run a long transient simulation that is long enough to verify if the PLL achieves locking. This final full-chip simulation is important and should be performed to catch potential mistakes.

The complete layout of the PLL from the Cadence environment is shown in figure 6.2. Most of the layout area is taken up by the synthesized block, with the DCO, phase quantizer, integer counter and current source DAC placed and routed manually. Theoretically, the integer counter can also be synthesized, but due to lack of familiarity with the STMicroelectronics synthesis tool flow, I did not synthesize the integer counter because this integer counter needs to operate at up to 2.4GHz at all process corner. The DCO and phase quantizer are manually placed and routed to achieve better linearity, and lower parasitic, and to ensure monotonicity at the phase quantizer output.

6.1 Measurement

The transmitter is designed to operate at 2.4GHz. Figure 6.4 is a screen capture of the DCO output spectrum when it is free running. The oscillation frequency of the DCO over a single sweep spreads over 2MHz band. On the other hand, figure 6.4 is a screen capture of the DCO output spectrum when it is locked through the PLL to a 20MHz reference. A clear and stable carrier tone exists and phase noise around the carrier is suppressed. When the PLL is enabled, the phase noise is measured to be -80dBc/Hz at 1MHz offset, as shown in figure 6.5. By setting the proportional and integral controller coefficients in the PLL, the PLL is operating with bandwidth of 2MHz, which is one tenth of the reference frequency.

When operating at 2.4GHz ISM band, the fractional-N PLL consumes 3.9mA from a 1.3V supply and the power amplifier consumes 5.6mA from a 1.3V supply at 0dBm output power. The die photo is shown in figure 6.6. This is also a pad-limited design and the total active area is $0.04mm^2$.

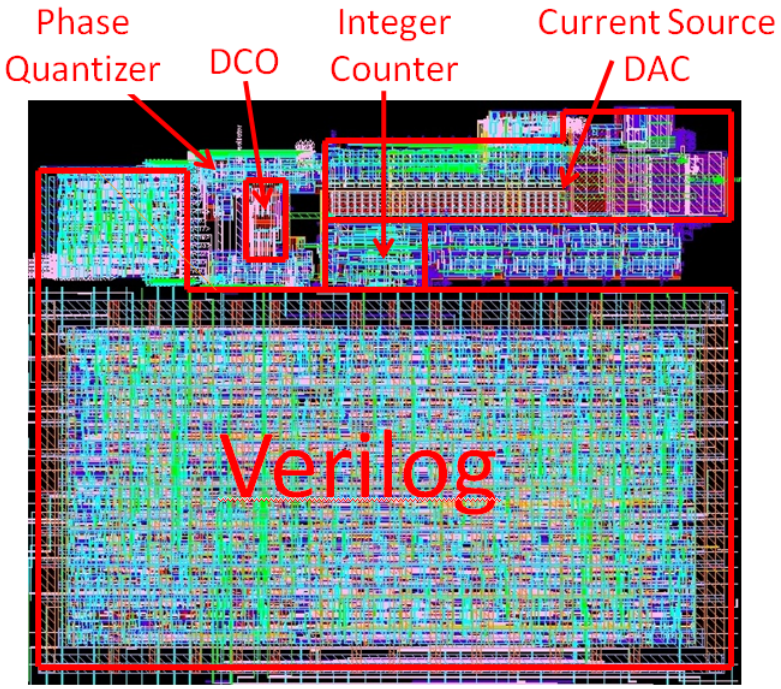

Figure 6.2: Cadence Layout

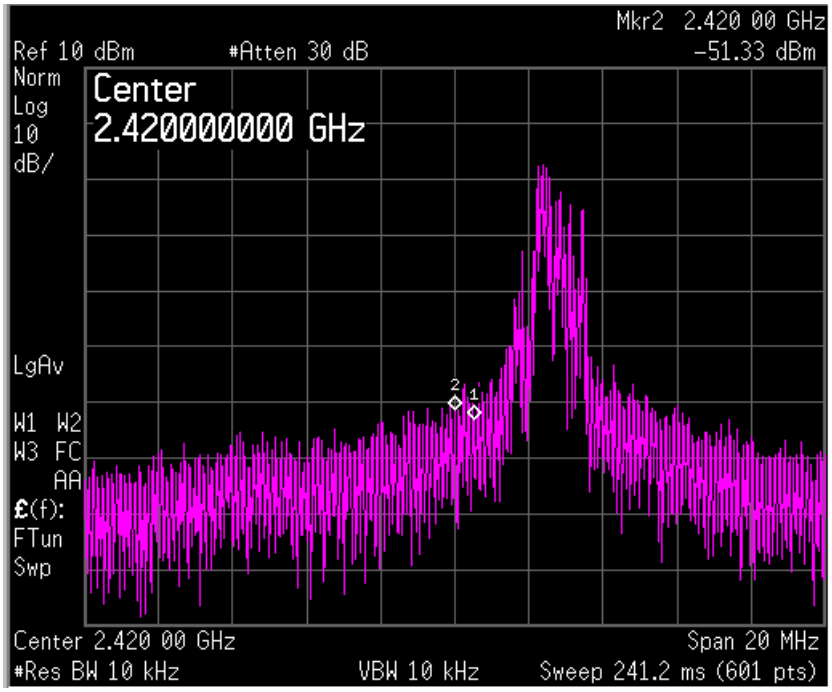

Figure 6.3: Spectrum of the 2.4GHz DCO Free Running

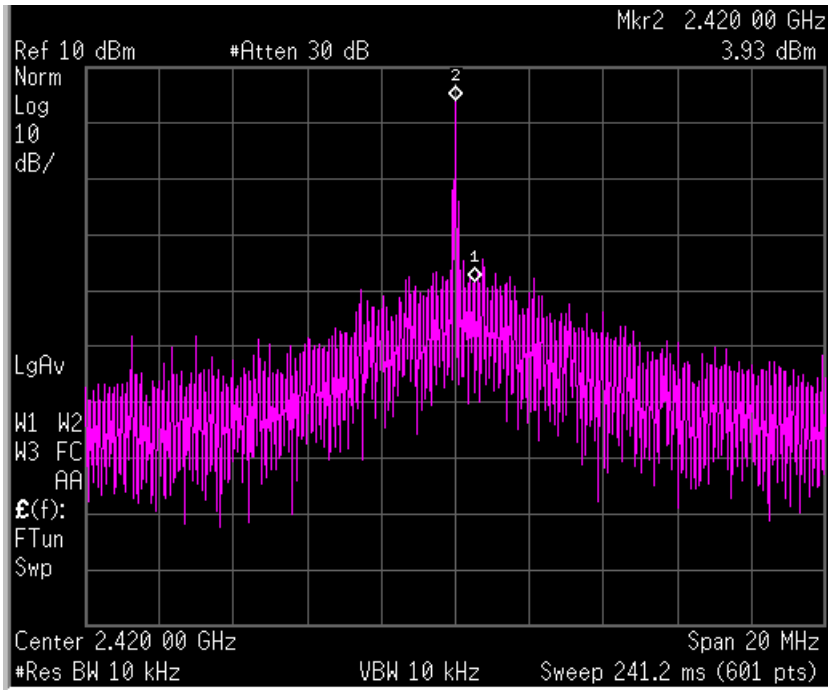

Figure 6.4: Spectrum of the 2.4GHz DCO Locked to a 20MHz Reference

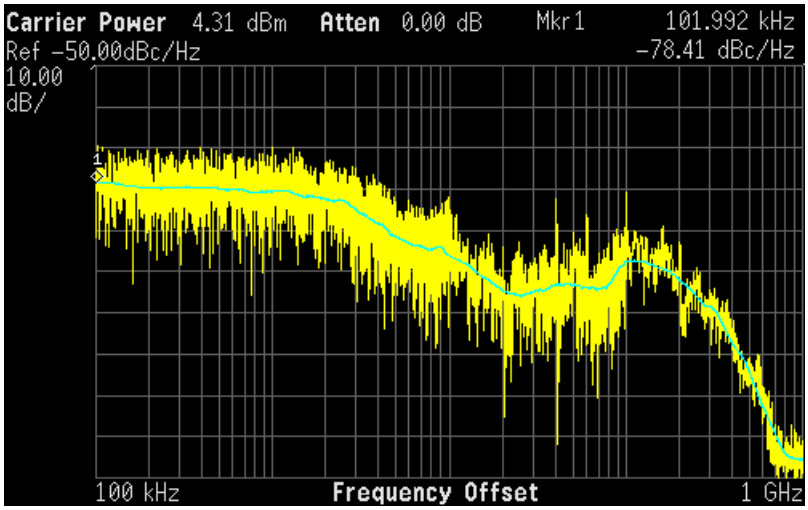

Figure 6.5: Phase Noise Measurement

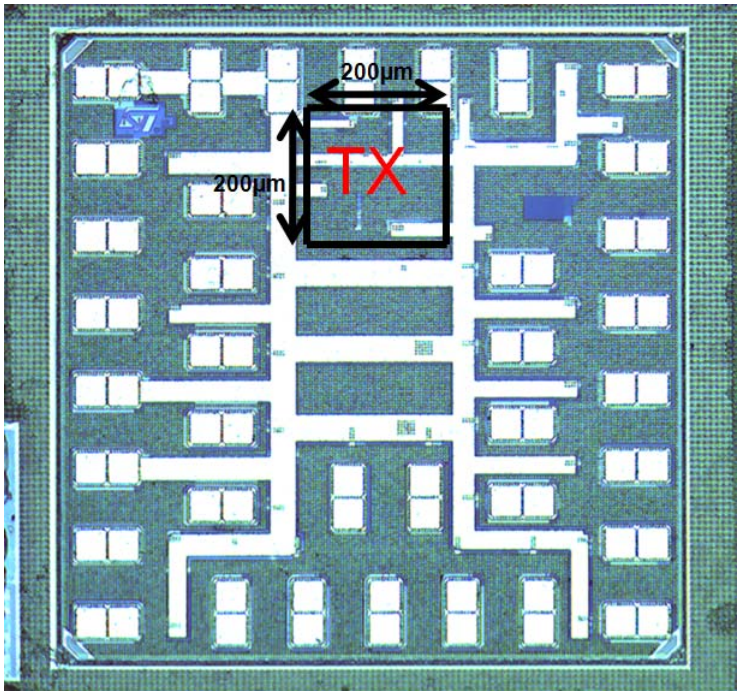

Figure 6.6: Die Photo

Chapter 7

Conclusion

7.1 Research Summary

This thesis describes the design and implementation of a radio built with standard cells and digital synthesis tools. This radio takes up $.5mm^2$ in a .18μm CMOS process, which is equivalent to roughly 5 cents per radio. Since this radio is built with standard cells and digital synthesis tools, the portability of such a radio to a different process or technology is greatly enhanced. The transmitter portion of the design is ported to a 65nm CMOS process for completeness and this transmitter takes up $0.04mm^2$. In a fine-line process, a complete transceiver can occupy only $0.1mm^2$ of area or less.

The receiver prototype built in a .18μm standard CMOS process occupies only 500μm x 350μm of area, has a sensitivity of -76dBm at 10kbps data rate, and consumes 6mW from a single 1.8V supply while operating in 915MHz ISM band.

The transmitter prototype built in a .18μm standard CMOS process includes a power amplifier and a fractional-N all-digital PLL. This fractional-N PLL uses an embedded time-to-digital converter with multi-path to increase TDC resolution, and includes digital correction circuitry to resolve issues from clock skew. This PLL prototype occupies 500μm x 500μm of area, generates a 915MHz LO signal from a 10MHz reference, has phase noise of -90dBc/Hz at 1MHz offset and 2.62ps-rms jitter while consuming 4.2mA from a 1.8V supply. Even though this fractional-N all-digital PLL is built almost entirely with standard cells, the performance of this PLL is comparable to other state-of-the-art all-digital PLLs recently published in ISSCC.

7.2 Future Research Directions

7.2.1 Receiver Sensitivity

The receiver sensitivity in our prototype is -76dBm. This sensitivity is sufficient to provide 10 meter indoor communication at transmitter output power of 0dBm. The primary objective of this work is to build a radio prototype that can be easily integrated with other circuits (microprocessors, sensors, etc) and takes up small area. However, to receive wider acceptance, it is important to improve the receive sensitivity to within 10dB from commercially available low power radios, which have sensitivities better than -90dBm. Priliminary simulations indicate that a slightly modified all-digital fractional-N PLL can improve the receiver sensitivity of this radio to be -80dBm or better. In this prototype, the LO signal is generated from a ring oscillator, rather than a LC oscillator. The quality of the LO signal degrades the sensitivity dramatically as discussed in 5.3.2. One area for future improvement is in the PLL design. The reference clock for the PLL in this work is 10MHz and 20MHz. This is chosen as it allows reasonable DCO to reference division ratio and small enough frequency resolution. A higher reference clock frequency could be used to achieve wider PLL bandwidth and to further suppress the intrinsic phase noise from the DCO. Additional, as research for high-performance PLL continues, other all-digital PLL architectures can be used to help alleviate the issues related to ring oscillator phase noise.

7.2.2 A Synthesizable Radio

This radio prototype uses digital synthesis tools to help reduce the design and layout effort. In particular, a great portion of the PLL is designed with digital synthesis tools. Even though part of the PLL, transmitter and receiver front-end are placed and routed manually, one could design and layout those remaining blocks and add those Megacells into existing standard cell libraries for auto place and route. Taking a step further, since those non-synthesized blocks are designed using standard cells, structural Verilog can be used to describe the remaining blocks to form a completely synthesizable radio.

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