Fundamental Conductance ÷ Voltage Limit in Low Voltage Tunnel Switches

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Fundamental Conductance ÷ Voltage Limit in Low Voltage Tunnel Switches

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***Abstract*—There is a fundamental conductance ÷ voltage limit in low voltage (<4kT/q) tunnel switching devices that obtain a sharp turn off by relying upon the band edges to abruptly cut off the available density of states. The Fermi occupation probabilities are thermally broadened by $4k_bT$. However, current is only allowed to flow in a narrow energy range limited by the applied voltage, V. This means that if we apply a voltage less than $4k_bT/q$, the conductance will be reduced by at least $qV/4k_bT$. Even with a perfect tunneling probability of 1 in a perfect quantum channel, the conductance quantum would be diminished by qV/4kT. Attempts at lowering the operating voltage below <4kT/q must come at the expense of smaller conductance.**

***Index Terms*—Tunneling Field Effect Transistor (TFET), Density of States, Tunneling, Energy Filtering**

I. Introduction

TUNNEL switches (such as Tunnel Field Effect Transistors) promise to dramatically reduce the power consumption of modern electronics significantly by reducing the operating voltage and overcoming the thermally limited subthreshold swing voltage of 60mV/decade[1-3]. When trying to achieve a very sharp turn-on there are two mechanisms that can be exploited. The applied voltage can be used to modulate the tunneling barrier thickness and thus the tunneling probability. It is also possible use the band-edge energy filtering or density of states overlap mechanism. The energy filtering turn-on is illustrated in Fig. 1. If the conduction and valence band do not overlap, no current can flow. Once they do overlap, there is a path for current to flow. This band overlap turn-on has the potential for a very sharp On/Off transition that is much sharper than that which can be achieved by modulating the tunneling barrier thickness[4]. However, as we will show in the next section, when the available system supply voltage, V_{dd}, is less than 100 mV at room temperature ($4k_bT/q$), there is a fundamental tradeoff between voltage and conductance.

II. Fundamental Tradeoff Between Voltage and Conductance

To understand what happens in a tunneling junction at low voltage, let's consider the simplest possible tunneling junction, a 1d nanowire a shown in Fig 2. Tunneling is occurring from the partially filled valence band on the p-side to the partially empty conduction band on the n-side. The band diagram across this junction is given by Fig. 1(b). The overlap between the conduction and valence bands is defined as $V_{OL}=qE_{OL}$ as shown in Fig 1(b). In addition there will be an applied voltage, V_{SD}, between the contacts. The overlap voltage, V_{OL} will be influenced by V_{SD} or by the gate voltage in a transistor.

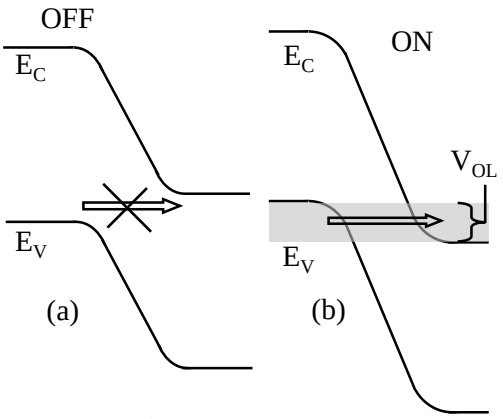

Fig. 1. (a) No current can flow when the bands do not overlap. (b) Once the bands overlap, current can flow.

Fig. 2. A simple 1d nanowire tunneling junction is shown.

The current is given by[5-7]:

$$I = \frac{2q}{h}\int_0^{qV_{OL}} (f_C - f_V) \times T \times \partial E \qquad (1)$$

The tunneling probability is given by T and often given by a simple WKB approximation: $T = \exp\left(\int k dx\right)$. The difference in the Fermi occupation probabilities is (f_c–f_v), where:

$$f_{c,v} = \frac{1}{e^{(E-E_{Fc,v})/k_bT}+1} \qquad (2)$$

The difference between electron and hole quasi Fermi levels is $(E_{FC}\text{-}E_{FV}) \equiv qV_{SD}$.

Now, let's consider the small bias regime where both the overlap voltage, V_{OL}, and the applied voltage, V_{SD}, are less than $4k_bT$. This is illustrated in Fig 3. Electrons can only tunnel in a narrow energy range given by V_{OL}. However, the thermal occupation difference is spread out over a $4k_bT$ energy

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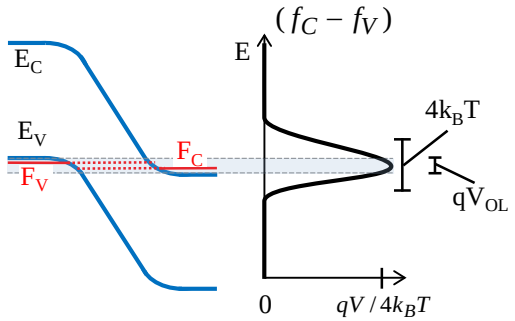

Fig 3: Electrons can only tunnel in a narrow energy range given by V_{OL}. However, the thermal occupation difference is spread out over a $4k_bT$ energy range. This means that the conductance will be reduced by a factor of $qV_{OL}/4k_bT$.

range. This means that the conductance will be reduced by a factor of $qV_{OL}/4k_bT$. Algebraically, we can see this by Taylor expanding f_c - f_v in the small bias regime:

$$f_c - f_v \approx \frac{(E_{Fc} - E_{Fv})}{4k_bT} \approx \frac{qV_{SD}}{4k_bT} \tag{3}$$

V_{SD} is the bias across the source and drain. Plugging this back into (1) gives:

$$\begin{aligned} I &\approx \frac{2q}{h} \times \frac{qV_{SD}}{4k_bT} \times \int_0^{qV_{OL}} \top \times \partial E \\ &= \frac{2q^2}{h} \times \langle \top \rangle \times V_{SD} \times \frac{qV_{OL}}{4k_bT} \end{aligned} \tag{4}$$

Here $\langle \top \rangle$ is the energy averaged tunneling probability. The conductance is given by:

$$G = I / V_{SD} = \frac{2q^2}{h} \times \langle \top \rangle \times \frac{qV_{OL}}{4k_bT} \tag{5}$$

On the right hand side, the quantum of conductance is multiplied by the factor $qV_{OL}/4k_bT$. In general, the overlap voltage, V_{OL}, must be less than the overall supply voltage, $V_{OL}<V_{dd}$, in order to make it possible to turn off the switch by preventing band overlap. Consequently, we arrive at the following inequality for the conductance/voltage ratio:

$$\frac{G}{V_{dd}} < \langle \top \rangle \times \frac{q^3}{2hk_bT} < \frac{q^3}{2hk_bT} \tag{6}$$

The first inequality stems from $V_{OL}<V_{dd}$, and the second inequality stems from the transmission probability $\langle \top \rangle<1$. The conductance/voltage ratio inequality, Eq. (6), says that low voltage switches inherently have poor conductance in the on-state, while high-conductance switches require $V_{dd}>4k_bT$. This should be regarded as a limit that applies to a single quantum channel.

In larger devices with a substantial transverse density of states, with many channels in parallel, the conductance/voltage ratio will scale according to the parallel channel count. We simply need to multiply the current, Eq. (1), by the transverse density of states. Thus the derivation shown above for 1d-1d wires contacting at facing wire ends also applies to other dimensionality cases [7, 8].

The possibility arises that a Tunnel Diode that employs barrier thickness modulation, rather than bandedge energy filtering might somehow not be subject to the inequality in Eq. (6). Achieving an interesting On/Off ratio ~10^6 for barrier thickness modulation typically requires a V_{dd}>100meV. For a single quantum conductance channel such a device automatically satisfies inequality (6).

III. Conclusion

There is a fundamental (conductance÷voltage) limit $<q^3/2hk_bT$ in energy filtering TFETs due to thermal broadening. As we try to reduce the operating voltages below 100 mV ($4k_bT$ at room temperature), the transistor conductance will be reduced by $qV_{OL}/4k_bT$. Consequently, if we want to operate at 10 mV, the conductance and thus transistor speed will be reduced by a factor 10. Even if we could achieve a perfect tunneling probability of 1, we cannot achieve a perfect quantum of conductance at voltages less than $4k_bT$!

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