# Multi-Mode Sub-Nyquist Rate D/A Converter for TV Band Cognitive Radio

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**Multi-Mode Sub-Nyquist Rate D/A Converter for TV Band Cognitive Radio**

By

Yuan-Shih Chen

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Professor Paul K. Wright

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## Abstract

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Advances in high-speed DAC implemented in deeply scaled-CMOS processes open up the possibility of direct IF and RF waveform synthesis in a next-generation digitized transmitter architecture. A state of the art CMOS current-steering DAC is capable of providing wide bandwidth and high dynamic range for direct RF waveform generation. This enables the mostly-digital implementation of a direct waveform synthesis transmitter for TV band cognitive radio. RF waveforms with various modulation schemes can be synthesized in the digital domain and directly converted by a high-speed DAC. The transmission characteristics can be dynamically adapted to time-varying spectral environment. This transmitter architecture brings the benefits of reconfigurability and frequency agility. However, conventional waveform synthesis requires a >2GS/s DAC to fulfill the Nyquist requirement for covering the whole TV band (54 $\sim$ 862MHz). Nevertheless, an alternative method is to convert the signals at a sampling rate below the Nyquist requirement and extract the image spectrum in higher Nyquist zones by bandpass filters.

This work demonstrates a proof-of-concept design of sub-Nyquist rate conversion and wideband direct synthesis using image spectrum. By utilizing the proposed multi-mode reconstruction, the DAC can shape the spectral envelope for enhancing the image spectrum located in the target channels. The desired transmission waveforms can be extracted from the second or third Nyquist zone by a bandpass filter. A circuit prototype demonstrating the proposed concept has been designed, fabricated, and measured in a general-purpose 65nm CMOS process.

This work presents the implementation of a 600MS/s 10-bit multi-mode sub-Nyquist rate DAC that enables wideband direct waveform synthesis for TV band cognitive radio transmitters. Measurement results show SFDR >55dB across the first three Nyquist zones

and a low power consumption of 30mW. The IM3 is < -60dBc in the first and second Nyquist zones and < -55dBc in the third Nyquist zone.

To my parents,my wife, and my son

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# Chapter 1

# Introduction

As the demand for high data-rate wireless and wide-range coverage of communications services increases rapidly, technologies to improve the flexibility and efficiency of spectrum utilization are becoming more significant. According to the spectrum measurement study conducted by Shared Spectrum Inc., the measurement results in Figure 1.1 show the spectrum utilization from 30MHz to 3GHz in 24 hours. The spectrum usage experiences vast temporal and geographic variations ranging from 15% to 85%. It shows the evidences of low utilization in most of the spectrum and overcrowded situations in certain frequency bands.

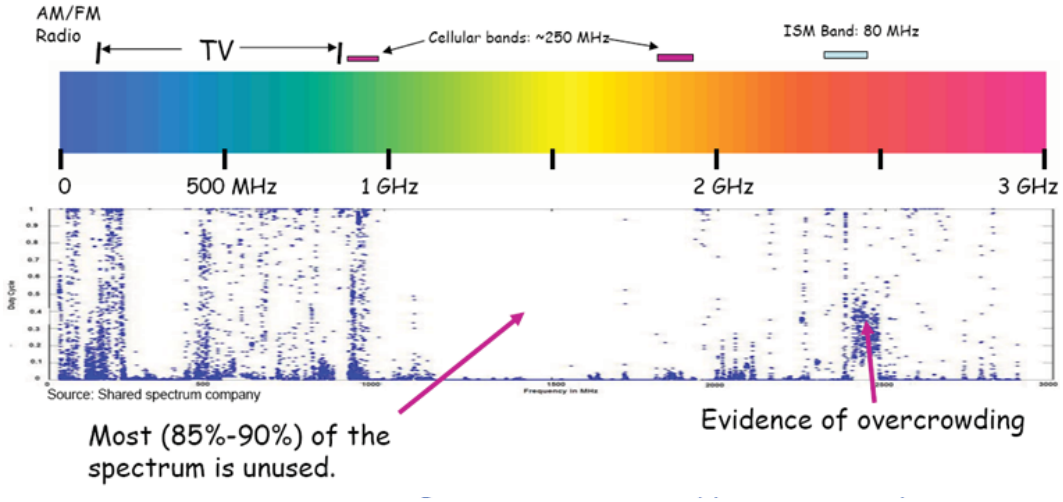


Figure 1.1: Spectrum utilization of 30MHz $\sim$ 3GHz in a 24-hour period

Cognitive Radio (CR) technology has been proposed as a way of improving spectrum utilization efficiency. A cognitive radio system senses the spectral environment over a wide frequency range and exploits the spectrum occupancy information to provide wireless links. It opportunistically uses the unoccupied spectrum segments while preserving the rights of privileged primary licensed users [1].

To communicate efficiently without interfering with licensed or unlicensed users, the cognitive radio network adapts its transmission and reception parameters dynamically. The seamless connectivity in a time-varying spectral environment is ensured by the reconfigurability and frequency agility of the cognitive radio terminals. Low power consumption is also required to save battery life on the mobile devices.

The current cognitive radio research directions are steered toward consumer-oriented scenarios so as to enable seamless adaptation of dynamic spectrum access to multiple networks in TV band white spaces. The future directions may include opportunity-discovery mechanisms minimizing network overhead (e.g., coordination between spectrum sensors) to promote flexible network topologies with less control, spectrum-aware network architectures and frequency-agile transceivers designed to accommodate popular customer applications such as video streaming, and spectrum-trading mechanisms to enable elastic spectrum reuse for various cognitive radio applications.

## 1.1 TV Band Cognitive Radio - "WiFi on Steroids"

Regulatory efforts are currently ongoing in many countries to open up secondary access to TV band white spaces, under the prerequisite of no harmful interference produced to primary users. The regulatory agencies include Federal Communications Commission (FCC) regulations in the USA, Office of Communications (OFCOM) in the UK, and the Electronic Communications Committee (ECC) in Europe. According to the FCC's National Broadband Plan in 2010 [2], the FCC should make 500 megahertz newly available for broadband use within the next 10 years, of which 300 megahertz between 225 MHz and 3.7 GHz should be made newly available for mobile use within five years. The FCC initiates a rule making proceeding to reallocate 120 MHz from the broadcast television bands and expand opportunities for innovative spectrum access models. The license-exempt use of TV band white spaces is very promising as a key component in the National Broadband Plan. It becomes a big driving force of the research on cognitive radio technologies.

As shown in Figure 1.2, white space is the name given to the vacant unused spectrum

between television channels. In the TV band, the airwaves have the potential to carry wireless data at speeds and distances that overtake the existing WiFi systems. This "Super WiFi" in those TV white spaces has a range of several miles, rather than the length of a football field, and it is capable of traveling through obstructions like trees or walls. Therefore, the TV white space has earned the nickname "WiFi 2.0" or "WiFi on Steroids". With a range of several miles as well as speeds close to cable modem broadband, we can easily see how the TV white spaces could open up a whole new realm of wireless technologies and fundamentally change how and where wireless communications are used.

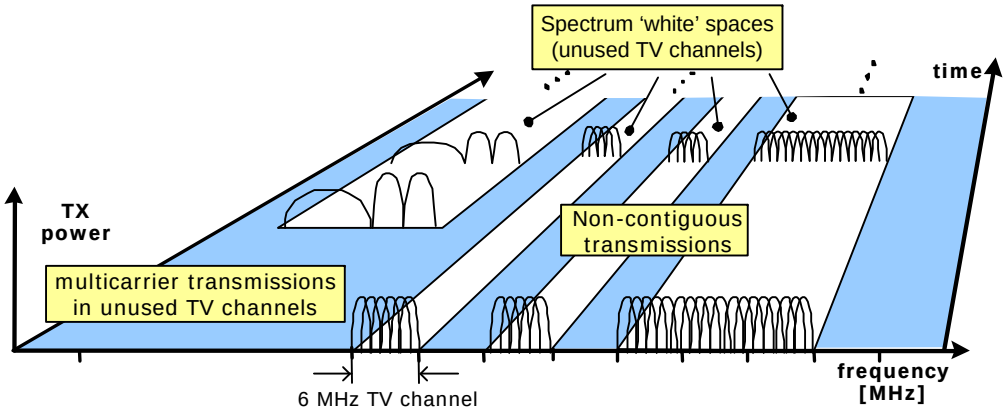


Figure 1.2: TV band white spaces

Regarding the current progress on TV white spaces, the FCC has worked with the concerned parties and come up with a plan that ensures that devices using the TV band white spaces will not interfere with adjacent broadcasts. The FCC has mapped TV channels and major wireless microphone usage (such as the Broadway theater district in New York City, or major sports arenas), and will require that wireless devices using the white spaces be configured to avoid the frequencies in use in a given area. Devices could be built to be location-aware, and automatically configure themselves based on information in the database.

A number of transitional steps will be necessary to allow for the gradual introduction of unlicensed devices on unused broadcast frequencies. The first step would allow unlicensed devices to operate on the guard bands and unassigned channels in the bands associated with TV channels 52-69. Since these channels have been designated for relocation early in the DTV transition, and since there are very few allocated stations, a significant amount of spectrum would be available for immediate sharing. As the band is vacated by current

licensed users, unlicensed devices would then be granted the full frequency range for dedicated unlicensed use while remaining cognizant of and avoiding interference to the public safety operations in the Upper 700 MHz band. Finally, as the DTV transition enters its final stages, former analog guard bands in the range of channels 2-51 (excluding Channel 37, reserved for radio astronomy), could be made available for unlicensed use.

As cognitive radios and TV band white spaces continue to draw more and more attention, they become an essential part of the emerging wireless communications standards and systems recently. The prospects of TV white space regulations have triggered development of new wireless standards, including IEEE 802.22, ECMA-392, and IEEE 802.11af. These various schemes proposed thus far have been reviewed and compared to identify which of them to use for real-life cognitive radio applications.

For wide-area broadband applications, IEEE 802.22 is a standard for Wireless Regional Area Network (WRAN) using white spaces in the TV broadcasting band (54MHz $\sim$ 862MHz) [3] [4]. This standard aims at using cognitive radio technologies to allow sharing of geographically unused TV broadcast spectrum, on a non-interfering basis, to bring broadband access to hard-to-reach, low population density rural areas. On the other hand, the FCC's allowance of personal/portable devices in TV white spaces also introduces other two standards: IEEE 802.11af [5] and ECMA-392 [6]. Those two standard are for portable or personal devices with low transmit power of 40mW or 100mW, operating within a smaller coverage.

As new standards and compatible products are developed, we can envision scenarios where multiple cognitive radio networks in TV band white spaces will likely overlap with each other creating the needs for coexistence mechanisms. A generic heterogeneous scenario is illustrated in Figure 1.3, where multi-radio devices take advantage of the TV band white spaces to achieve higher capacity and/or wide transmission ranges. In one typical case, a fixed wide area broadband network (e.g. IEEE 802.22) could provide wireless backhaul to homes, which use Wi-Fi (e.g. IEEE 802.11af) or ECMA-392 for in-home coverage. Alternately, IEEE 802.11af or ECMA-392 devices could form a neighborhood mesh network.

This is a new paradigm for wireless communications based on harnessing unused spectrum. Those spectrum agile radios enable new applications, such as wireless internet, remote patient monitoring, and public safety.

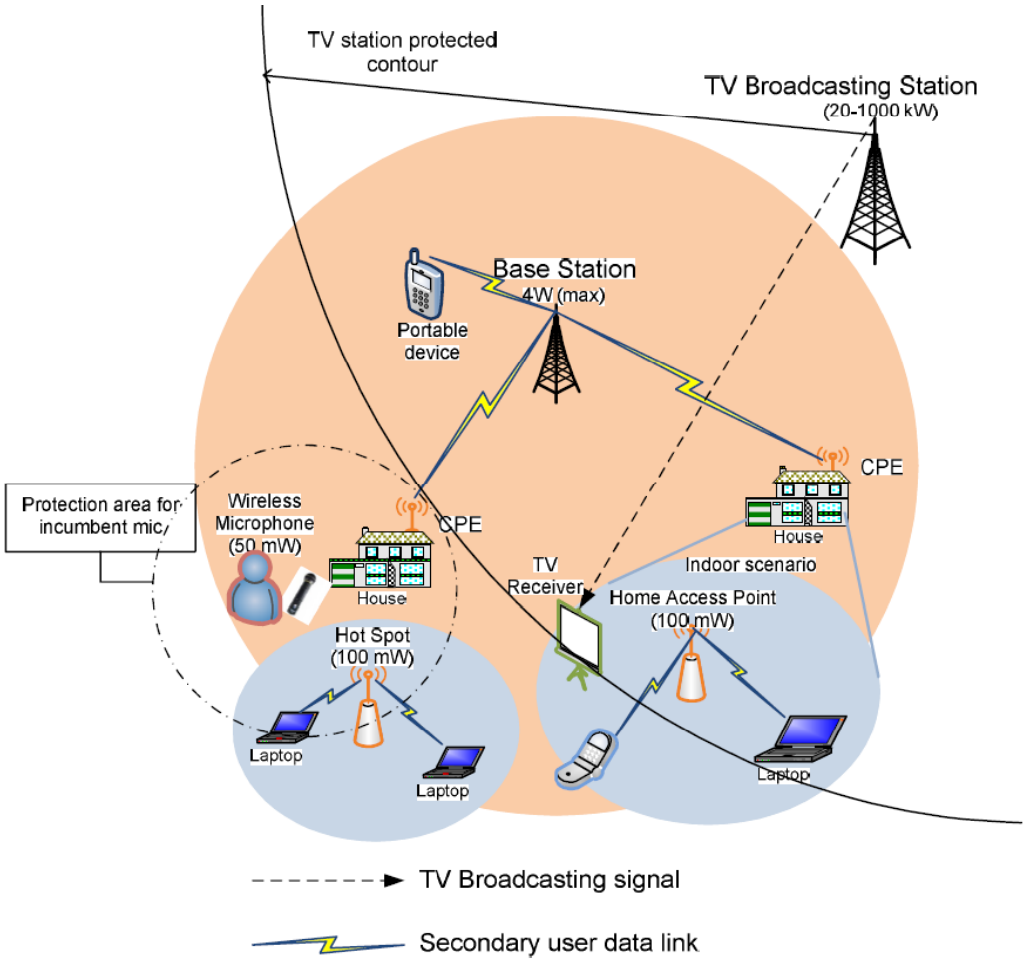


Figure 1.3: Heterogeneous coexistence of TV band radios

## 1.2 Related Work

The idea of cognitive radio was first presented officially in 1999 by Joseph Mitola III in his pioneering work [7]. The research of cognitive radios has been rapidly developed in the past decade [8]. Cognitive radio was initially thought of as a software-defined radio extension. Cognitive radio has the potential of reshaping the way of utilizing spectrum resources. This led to the FCC's initiation of a new spectrum policy in 2000 [9]. Many research efforts span from radio and reconfigurable hardware to communications theory as well as the networking layer. Through the continuing efforts of spectrum regulators and the research community, the TV white spaces are going to be opened for license-exempt uses

of cognitive radio applications. The TV band white spaces are expected to mitigate the anticipated spectrum shortage problem. The regulatory policies, industrial activities, and standardization will soon be developed.

The history of TV band radios can be traced back to the late 1920's. Since the TV broadcast services had been widespread in the past decades, various analog/digital TV broadcast standards and systems exist throughout the world today. The conventional TV broadcasts is a one-way transmission from the high power TV transmission towers to TV tuner. The design of high-power TV transmitters and high sensitivity tuners has been well exploited and engineered [10] [11] [12].

With the advances of circuits and technologies, classical analog TV "can tuners" have been replaced by much more integrated IC solutions. The low power and low cost CMOS tuners can be directly integrated onto the main board with reduced numbers of discrete components. To support the terrestrial broadcast TV in UHF/VHF band, tuners need to address issues, such as the interference rejection at integer multiples of the wanted signal as well as the in-band image rejection. Typical techniques include using external RF tracking filters with limited bandwidth that track the signal carrier, or the conventional up-down conversion super-heterodyne architecture. To achieve the wide tuning range and wide bandwidth, tunable analog/RF blocks are intensively used in the front-end of the conventional architecture.

There are many published examples of integrated TV band receivers. In [13], the competitive, low-cost solutions in CMOS technology presents the implementation of a tuner in 65nm CMOS process, supporting all most popular mobile TV standards, such as DVB-T/H, DAB based T-DMB, and ISDB-T. The extensive use of digital calibration hardware to improve the tuner performance and achieve a high degree of programmability required in multi-standard operation. In [14], a silicon tuner has been designed for the reception of analog or digital TV signals from a cable or a terrestrial network. It exhibits 5 dB NF over the 42-870 MHz frequency range and integrates a self-calibrated LC tracking filter. This allows 55 dB video SNR under fully loaded spectrum conditions. However, those examples are mainly focusing on the design of the TV band receiver. The transmitter designs in TV band radios have not been shifted from high-power TV tower to an integrated low-power and small form factor design.

This work explores practical TV band cognitive radio transmitter from system-level design to circuit implementation of critical blocks. The proposed direct waveform synthesis architecture is mostly-digital and frequency-agile. There are notable examples of reconfigurable, or software-defined transmitters [15]. Broadband, reprogrammable, and highly-

integrated implementation as well as novel techniques can be found in the literature [16–18]. The focus here is on the TV band frequency range where the spectrum white spaces are permitted for unlicensed use. Digital signal processing offers a degree of flexibility that is perhaps unmatched by analog circuits. This drives us to push the Digital/Analog boundary toward the front-end. Nevertheless, this trend implies that demand of high-speed wide bandwidth D/A converter to fulfil the system requirements.

To overcome the bottleneck of D/A conversion and the challenges of Nyquist rate synthesis, many signal reconstruction techniques have been proposed for enabling wideband signal synthesis. Past work presented Return-to-Zero (RZ) to flatten the SINC envelope and extend the possible operation region to higher Nyquist zones [19–21]. By using RZ reconstruction, the SINC roll-off in the DAC output is flattened while null frequencies are pushed to higher. This extends the usable region of signal synthesis from the first Nyquist zone to the second or the third Nyquist zone. Also, partial-order-hold (POA) technique for wide bandwidth operation had been proposed in [22]. The POH-DAC architecture is archived by a zero-order-hold DAC followed by a windowed-integration-based filter. It has the ability of broadband image reduction between 1.5 and two times the sampling frequency while also providing a flat-group delay. Interleaving two such POH-DACs results in a DAC with an excellent output signal reconstruction whereby the broadband sampling images below two times the sampling frequency in the output signal spectrum are strongly reduced.

In the research community of RF circuits, people tried to push the D/A interface closer to the RF front-end, which contributes the idea of RF-DAC. In [23] an IQ-modulator constructed using direct digital-to-RF converters for wide-band multi-radio applications achieves better than -43dBc of LO-leakage and -47dBc of image rejection. This idea has been demonstrated in 0.13um standard CMOS process. Another similar idea can be found in [24]. A low-distortion wide-band CMOS direct digital RF amplitude modulator uses a 10-bit linear interpolation current-steering DAC and a Gilbert-cell-based mixer to generate an amplitude modulated RF signal directly. In [25], a RF-DAC in 65nm CMOS is presented. The RF-DAC combines DAC and mixer functionality in a single building block. It is the basis for a direct-digital vector modulator used in reconfigurable broadband multi-standard transmitters for mobile communications. In [26], a 17b RF DAC is applied a fully digital multi-mode polar transmitter in 3G Mode.

In this work, a multi-mode sub-Nyquist rate conversion technique is proposed to achieve the goal of wide bandwidth waveform generation. The reconstruction mode can be dynamically reconfigured to achieve the best spectrum envelope for utilizing the image spectrum. A circuit prototype demonstrating the proposed concepts has been designed, fabricated and

measured. The prototype chip is able to maintain good SFDR across multiple Nyquist zones. This enables the direct waveform synthesis for the cognitive radio transmitters.

## 1.3 Thesis Organization

Chapter 2 begins by presenting an in-depth overview of cognitive radios for TV band white spaces, and reviewing the standards for TV band cognitive radios. After that, the system-level work is the main focus, which includes the transmitter architectures and direct waveform synthesis using sub-Nyquist rate conversion.

In Chapter 3, the concept and analysis of sub-Nyquist rate conversion are discussed. The multi-mode reconstruction technique has been proposed to overcome the wide bandwidth and high dynamic range requirements for direct waveform synthesis. The multi-mode sub-Nyquist rate DAC operation has been proposed to be a versatile solution for spectrum agile radio applications.

In Chapter 4, the circuit implementation and measurement results are presented. The sub-Nyquist rate DAC chip was fabricated in 65nm CMOS technology by ST Microelectronics. The chip is measured to be fully functional and characterized in static and dynamic performances. The performance and power measurements are presented in the end.

Finally, the conclusions and future work are summarized in Chapter 5.

# Chapter 2

# Mostly Digital Transmitter for TV Band Cognitive Radio

The growth in demand for wireless voice and data communications has driven recent research to develop highly-integrated next-generation radio transceivers. To reduce costs and power consumption, much effort has gone into implementing these transceivers in standard CMOS technology. Advances in high-speed DACs, implemented in deeply-scaled CMOS processes, open up the possibility of direct IF and RF waveform synthesis in a digitized transmitter architecture. The state of the art CMOS current-steering DAC is capable of providing wide bandwidth and high dynamic range for direct RF waveform generation [27]. The conventional waveform synthesis requires a DAC running at $>$ 2GS/s to fulfill the Nyquist requirement for covering the TV band (54 $\sim$ 862MHz). Nevertheless, an alternative method is to convert the signals at a sampling rate below the Nyquist requirement and extract the image spectrum in higher Nyquist zones by bandpass filters [19, 20].

In this chapter, the direct waveform synthesis transmitter is proposed for TV band cognitive radio applications. The reconfigurable digital waveform synthesizer and multi-mode sub-Nyquist rate D/A conversion are the two key components in this mostly-digital transmitter.

## 2.1 White Spaces in TV Bands

TV band white spaces refer to the vacant channels allocated to a broadcasting service but not used locally. On Feb. 13, 2009, Congress initiated the American Recovery and Reinvestment Act of 2009. As part of this initiative, the Federal Communications Commission (FCC) developed a National Broadband Plan. This plan sets its primary goal to ensure every American has access to broadband capability. It also promotes other objectives, including a detailed strategy to maximize broadband usage and affordability. The FCC has several tools available to help reach these goals: regulatory authority in spectrum policy and spectrum allocation ( both licensed and unlicensed). The importance of spectrum is further underscored by the fact that an entire chapter of the Commission's National Broadband Plan is devoted to spectrum usage and policy. The FCC has also highlighted the availability and use of TV White Spaces as a key component of the National Broadband Plan. As mentioned in section 5.12 in the plan, the FCC should move expeditiously to conclude the TV white spaces proceeding.

The TV broadcast band in the United States has evolved through a number of changes over time, primarily due to the FCC's desire to make more VHF and UHF bandwidth available for wireless two-way communications. To achieve this, the FCC adopted rules to allow unlicensed radio transmitters to operate in the broadcast TV spectrum at locations where that spectrum is not being used by licensed services - this unused TV spectrum is often termed "TV White Space". TV White Spaces are unused TV broadcast channels, made more available through the transition from analog to digital TV. The current TV channels and frequency allocation in the US is shown in Figure 2.1. The FCC has not dictated specific modulation or protocol requirements for TV Band Devices (TVBDs), allowing TV White Space to employ a wide range of devices and applications on an unlicensed basis, similar to Wi-Fi. The FCC has also ensured incumbent TV band users (TV broadcasters, public safety, registered microphone users, etc) have priority over TV White Space Device operation. To make certain incumbent users are protected, TV White Space devices must communicate with an Internet geographic database to obtain a current list of available White Space channels. Available channels may vary, depending on TVBD device type and location.

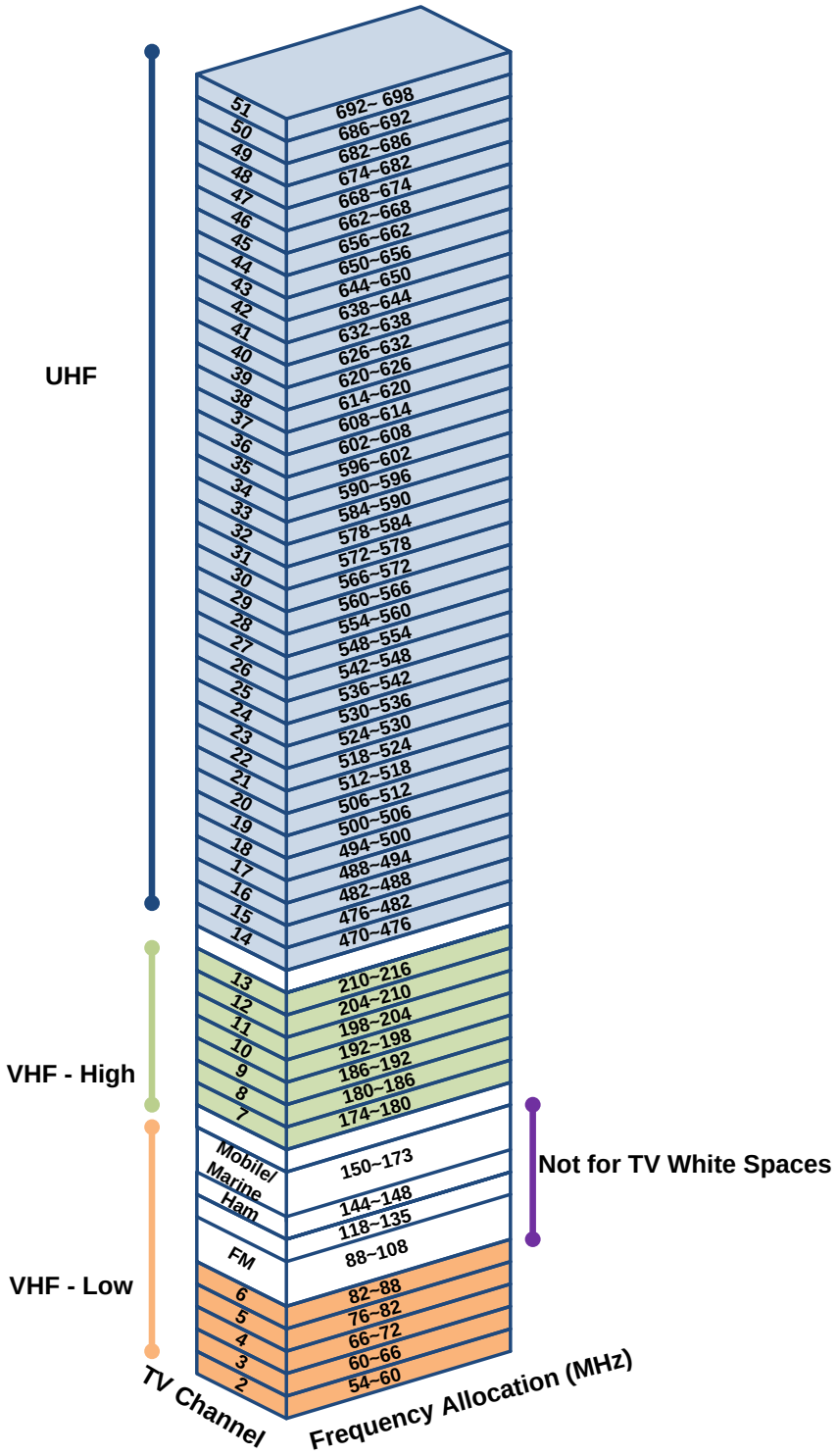


Figure 2.1: Overview of TV Channels in US

Table 2.1: Overview of the FCC rules for TV white spaces

| Device types/ Capability | | Allowed TV Channels | Max EIRP | Incumbent protection requirements | Allowed on Adjacent Channels |
|---|---|---|---|---|---|
| Fixed | | Ch 2 – 51 (except Ch 3, 4 and 37) | 4 W | Geolocation / Database | No |
| Personal/ Portable | Mode I | Ch 21 – 51 (except Ch 37) | 100 mW | Enabling signal from Mode II or Fixed Device | Yes (< 40mW EIRP) |
| | Mode II | | 100 mW | Geolocation / Database | Yes (<40 mW EIRP) |

The current FCC rules for TV band channels are listed in Table 2.1. the devices are divided into two categories: fixed and personal/portable. Fixed devices can transmit up to 4 W EIRP (equivalent isotropically radiated power) with a power spectral density (PSD) of 16.7 mW/100 kHz, and they must have geolocation capability and a means to retrieve a list of available channels from an authorized database. The fixed devices are restricted of operating in adjacent channels of active TV broadcasting channels. Fixed devices may operate in channels 2 to 51, excluding channels 3, 4, and 37.

Personal/portable devices are allowed a maximum EIRP of 100 mW (with PSD of 1.67 mW/100 kHz) on channels non-adjacent to TV broadcast services and 40 mW (with PSD of 0.7 mW/100 kHz) on channels adjacent to an active TV broadcasting channel. Personal/portable devices are classified into two modes: Mode I and Mode II. Similar to fixed devices, Mode II devices must possess geolocation and database access in order to obtain a list of available channels. On the contrary, Mode I devices are not required to have geolocation and database access, but they must obtain a list of available channels from a fixed or Mode II device. Personal/portable devices are only allowed in channels 21 to 51 (excluding channel 37). The main expectation is that fixed devices will most likely be used in rural areas, whereas portable devices may be highly used in metropolitan areas. The idea behind this channel allocation is to avoid the risk of interference with primary services, especially in high density population areas.

The available white spaces varies according to where you locate and what type of devices that you want to operate. The company, Sprectrum Bridge Inc, provides a centrailized

location-based database for visuallize the available white spaces. For non-highly populated areas, like Lake Tahoe, we can see the available white spaces for operating portable TV band devices from Figure 2.2. If we want to operate higher power, fixed TV band device, the number of available white space decreases as shown in from Figure 2.3. If we move our target location to the city area, like Berkeley, we can see the available white spaces from Figure 2.4.

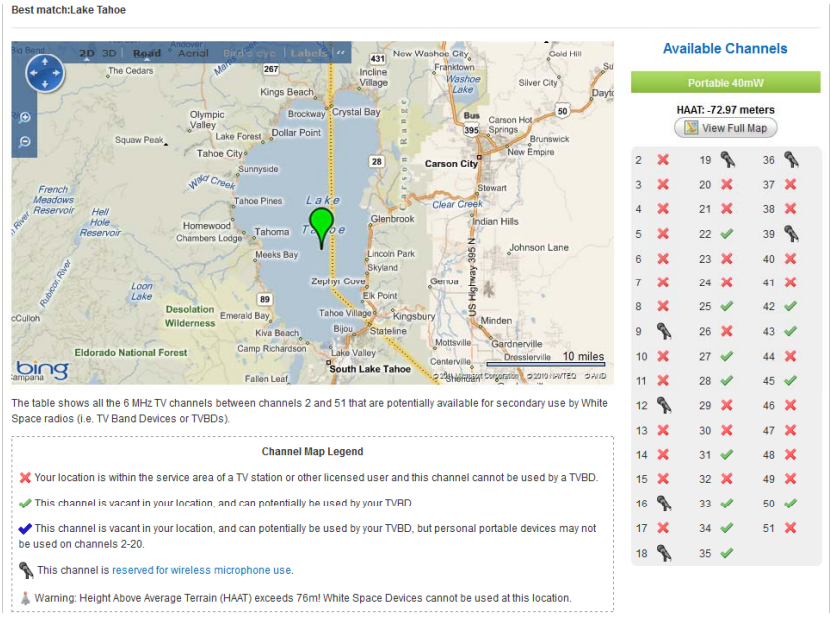


Figure 2.2: Available TV White Spaces for Portable Devices in Lake Tahoe

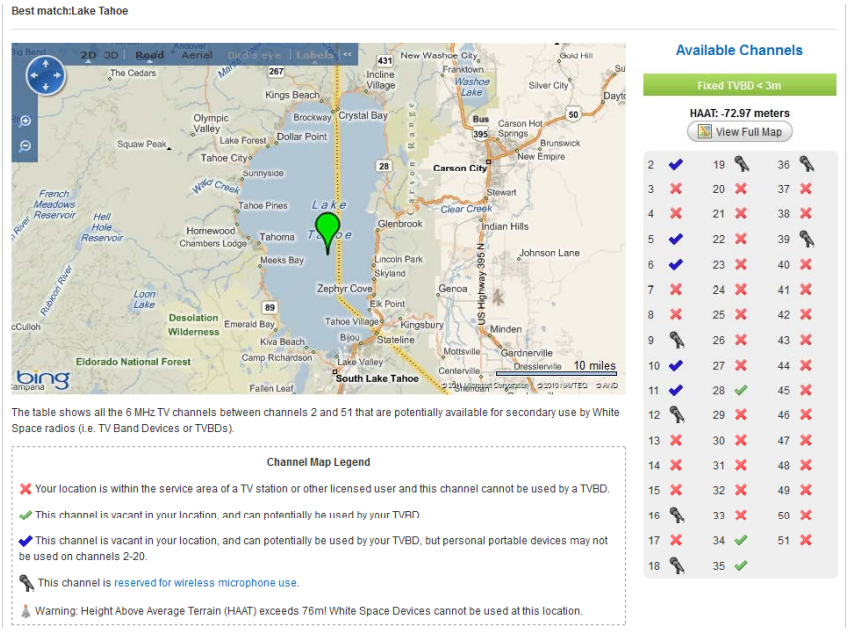


Figure 2.3: Available TV White Spaces for Fixed Devices in Lake Tahoe

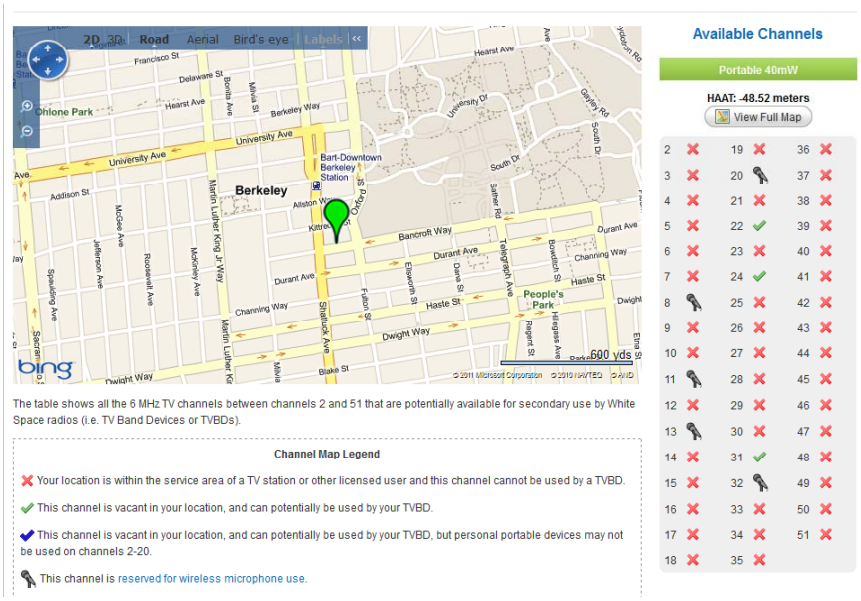


Figure 2.4: Available TV White Spaces for Portable Devices in Berkeley

For most of the U.S. land mass and population, there are significant amounts of TV White Space bandwidth available that can be used for a wide variety of applications. There is sufficient bandwidth available for Fixed Device (4W devices) use, which is needed to deliver wireless broadband to many communities in the country. In the majority of the country, there also appears to be sufficient white spaces available for portable/mobile applications, such as Wireless LAN - useful for augmenting 3G/4G services. A generous amount of bandwidth has been reserved for wireless microphone use. TV White Space is clearly an essential and significant element in the National Broadband Plan. Both the spectrum itself, as well as the database-driven spectrum allocation, make it a model for more efficiently deploying spectrum resources for a wide range of innovative applications.

- Whole home application: Television white spaces will enable wireless distribution of high-quality and high definition television for whole home, vastly improving the DTV experiences. The new standard will provide reliable and robust coverage anywhere in a home, while consuming much lower power. Robust delivery of high definition video inside home and across multiple walls.

- Community internet access application: Television white spaces will provide more widely available and cost effective access to the internet in underserved markets. The superior propagation characteristics provide much greater coverage range than existing unlicensed technologies. Robust coverage inside buildings and across campuses for wireless data applications such as wireless VoIP and mobile unified communications. Enhanced range for municipality, community and rural internet access without sufficient line of coverage.

- Smart services and other applications: Enhanced coverage for smart service and remote machine-to-machine and RFID deployments such as smart grid, smart metering, transportation, industrial automation, supply chain automation, asset tracking and environmental monitoring. New interactive applications for TV broadcasters, such as weather and news updates, upcoming program previews, interactive advertisements and games and web access. Most importantly, TVWS can provide enhanced range, robustness and quality for emergency-response and public service communication networks.

The TV White Spaces bring a new paradigm to wireless networking. By using a centralized database architecture for allocating spectrum, the FCC has taken the first step towards

policies and technologies that embrace a dynamic and highly efficient approach to increase spectrum availability and utilization for other licensed and unlicensed spectrum bands.

## 2.2 TV Band Cognitive Radio Standards

TV band cognitive radio is fundamentally different from the conventional TV broadcasts. TV broadcasts are one-way radio transmission, where the signals are transmitted from the high power TV towers to the tuners inside the televisions. For decades of technology development, the high-power TV broadcast towers and high sensitivity TV tuners have been explored and designed to reach the best performance.

The TV band cognitive radio aims at two-way communications. The transmitter design used in the high power TV towers is inadequate and obsolete to be the target solution for cognitive radio transmitters, because of the limited power budget for cognitive radio applications. Compared to conventional TV broadcast services, the low-power and small form factor TV band transceivers are the main area for further exploration and research. The TV band white spaces have motivated several standardization efforts, such as IEEE 802.22, IEEE 802.11af, and ECMA 392 for furthering cognitive networking. The introduction and highlights of the selected standards are presented in the following sections.

### 2.2.1 IEEE 802.22

On 27 July 2011, IEEE published the IEEE 802.22 standard for opportunistic use of the available TV white spaces [4]. IEEE 802.22 systems provide broadband access to wide regional areas around the world and bring reliable and secure high-speed communications to under-served and un-served communities. This new standard for Wireless Regional Area Networks (WRANs) takes advantage of the favorable transmission characteristics of the VHF and UHF TV bands to provide broadband wireless access over a large area up to 100 km from the transmitter. Each WRAN will deliver up to 22 Mbps per channel without interfering with reception of existing TV broadcast stations, using the white spaces between the occupied TV channels. This technology is especially useful for serving less densely populated areas, such as rural areas, and developing countries where most vacant TV channels can be found. IEEE 802.22 incorporates advanced cognitive radio capabilities including dynamic spectrum access, incumbent database access, accurate geolocation techniques, spectrum sensing, regulatory domain dependent policies, spectrum etiquette, and coexistence for optimal use of

the available spectrum. It also defines the air interface of WRAN . The airwaves in TV bands have superior propagation characteristics that can increase coverage and the ability to penetrate buildings at low power levels. This is the leading factor that helps IEEE 802.22 to provide better broadband service for far-out users. IEEE 802.22 focuses on wireless broadband access in rural and remote areas as its coverage area is much greater than other wireless broadband technologies, such as WiMAX and Wi-Fi.

IEEE 802.22 WRAN system consists of Base Stations (BS), fixed Consumer Premise Equipments (CPEs) ,and also personal/portable devices which can operate in the TV band white spaces. The fixed devices would have geographical location capability with embedded GPS device so that they can communicate with a centralized database to identify other transmitters in the area operating in the same TV band. In addition, there are other measures suggested by the FCC and IEEE to avoid interference, such as: dynamic spectrum sensing and dynamic power control. The personal/portable devices transmit lower power and shorter coverage for mobile applications.

The PHY layer needs to provide excellent in performance as well as simple in implementation. To avoid interferences, the PHY layer must be able to adapt to different conditions and also needs to be flexible to jump from channel to channel without errors in transmission or losing CPEs. This flexibility is also required to enable dynamical adjustment of the bandwidth, modulation and coding schemes. OFDMA is the modulation scheme for transmission in both up and down links. With OFDMA, it will be possible to achieve this fast adaptation needed for the BS's and CPEs. By using just one TV channel (6 MHz/channel in US; in some other countries 7 or 8 MHz/channel), the approximate maximum bit rate is 19 Mbit/s with the coverage of a 30 km distance. To allow the system to have higher performance, Channel bonding is one of the suggested features for dealing with the insufficient bandwidth which can combine up to 3 TV channels for the transceivers. Also, IEEE 802.22 defines 12 combinations of three modulations (QPSK, 16-QAM, 64-QAM) and four coding rates (1/2, 2/3, 3/4, 5/6) for data communications that can be flexibly chosen among to achieve various trade-offs of data rate and robustness, depending on channel and interference conditions.

### 2.2.2 ECMA-392

ECMA International started developing a high-speed wireless networking standard for utilizing the TV band white spaces, based on the contribution from Cognitive Networking Alliance (CogNeA). The ECMA-392 standard employs cognitive radio technology to avoid interference with licensed services and other incumbent users in compliance with the FCC

regulatory rules. It aims at multimedia distribution and internet access for low-power personal/portable cognitive devices in TV white spaces [6]. It specifies medium access control (MAC) sub-layer and physical (PHY) layer for operation in TV White Spaces. It also specifies a number of incumbent protection mechanisms which may be used to meet regulatory requirements.

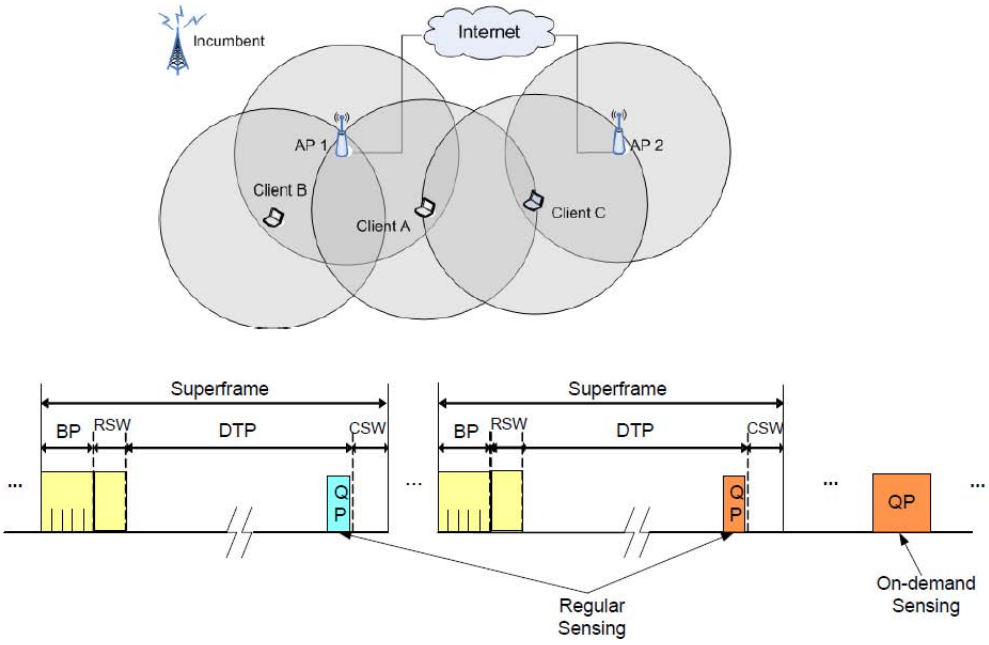


Figure 2.5: Overview of EMCA 392

The specification targets a flexible system that uses one or multiple vacant TV channels to provide the wireless communications, for example, in home distribution of audio and video, wireless internet access, etc. The various aspects of the PHY specifications are highlighted below. This PHY operates in the VHF/UHF TV broadcasting frequencies, subject to regulation. The extremes of the international regulations range of TV broadcast band is from 47 MHz to 910 MHz. Similar to IEEE 802.22, the channel bandwidth is equivalent to that of one TV broadcast channel, i.e., 6 MHz in US and 7 MHz, or 8 MHz in other countries. The channel bandwidth and channel numbering is dependent on the geographic location where the device is intended for operation. This PHY aims for personal/portable devices operating in TV white spaces with 100mW of transmit power. A high efficient MAC layer is also defined in this standard. To support world-wide spectrum regulation, a toolbox approach is adopted, while the FFT-based pilot sensing algorithms is mainly used as the


Figure 2.6: Example Applications of EMCA 392

spectrum sensing and estimation technique.

### 2.2.3 IEEE 802.11af - "White-Fi"

The IEEE 802.11af Task Group aims to make a transition from the existing Wi-Fi to a Wi-Fi-like protocol operating over the TV white spaces. The white spaces are made up of unused TV channels, which vary from location to location and from time to time. It has been set up to work on the 802.11 MAC and PHY layers to meet the legal requirements for channel access and coexistence in the TV white spaces [28]. The nickname, "White-Fi", is a term being used to describe the use of a Wi-Fi technology within the unused TV white spaces. It is believed that the White-Fi system offers sufficient advantages to invest the efforts on research and kick-start the development. The IEEE 802.11af standardization effort expects to fully standardized TV white spaces on the timeline of 2013.

The spectrum opportunity of TV white spaces consists of fragments of different numbers of available TV channels. This implies variable channel bandwidth can be utilized for wireless communications. The 802.11af plans to support the usage of multiple available channels in TV white spaces. The first type is to use multiple contiguous channels: 1, 2, 3, 4, (optional 8, 16) channels. The second type is to use multiple non-contiguous available channels: within 4 consecutive channels.

Many benefits can be gained from using TV white spaces in IEEE 802.11af system. First, since the TV white spaces locate at frequencies below 1 GHz, the 802.11af system is capable

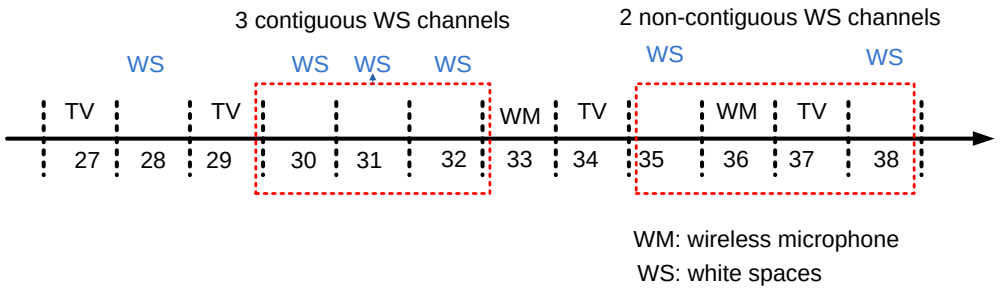


Figure 2.7: TV white Spaces Usage in 802.11af

of propagating for greater distances than current Wi-Fi systems. In contrast, the Wi-Fi signals operating in the ISM bands are easily absorbed, even in the lowest band of 2.4 GHz. Second, TV white spaces are that additional unused frequencies which can be accessed. However, to achieve the data throughput rates similar to that Wi-Fi uses on 2.4 and 5 GHz, the IEEE 802.11af system will be necessary to aggregate several TV channels to provide the high bandwidth. The synergy of propagation characteristics and additional bandwidth makes IEEE 802.11af an extension of Wi-Fi services in TV white spaces.

When using the IEEE 802.11af in TV white spaces, the overall system must not cause any undesired interference to the primary users such as existing television transmissions and wireless microphones. Using cognitive radio technology, the IEEE 802.11af system detects transmissions and moves to alternative channels. Also, similar to IEEE802.22, geographic sensing is another method proposed to minimize the harmful interference. To have a geographic database with the knowledge of available channels is another way of allowing the system to avoid interferences with used channels.

IEEE 802.11af devices, known as TV Band Devices(TVBDs), will come in two flavors: Fixed TVBDs and Personal/Portable TVBDs. Fixed TVBDs must operate from a known, fixed location, have a maximum 4 W EIRP, maximum 30m antenna height and must be able to determine and report their actual location (within 50m) to an authorized database to retrieve a list of available channels. Fixed TVBDs will be used for establishing long-range links and getting broadband out to unserved and underserved rural locations. They also can operate in any available channels, except reserved channels. Portable/Personal TVBDs are further divided into two categories, Mode I and Mode II. Mode II devices are like Fixed TVBDs in that they have internal geo-location capability and access to a TV

channel database. Mode I devices can not determine their location or check in with a TV channel database, but instead must get their channel list from a Fixed or Mode II TVBD. Portable/Personal TVBDs can use only channels 21 - 51, again, with the exception of reserved channels. For a single channel, a maximum link rate of 23.74 Mbps, or about half the maximum 54 Mbps link rate of 802.11g. Based on the past experience with the difference between PHY link rate and actual throughput, we can reasonably to assume a maximum throughput of a single White-Fi channel at around 10 - 12 Mbps.

Work has being started on the IEEE 802.11af standard for "White-Fi" applications in TV white spaces. In January 2012, "Super Wi-Fi" launched in New Hanover County, North Carolina. It is essentially Wi-Fi re-using the in-between spaces of TV channels below 700MHz and above 50MHz. Spectrum Bridge, a venture funded start-up (2007), and the county of New Hanover County in North Carolina and deploying on white space capable radio channels using 802.11 Wi-Fi as the Physical Layer protocol. Spectrum Bridge provides the channel list and other services while the radios are from Google, Microsoft, Cisco and KTS Wireless. New Hanover County is using their Wi-Fi network to surveil on a subdivision and collect telemetry from their water infrastructure although it appears they will provide citizen Wi-Fi at outdoor locations such as Hugh MacRae Park. In testing white spaces, the ranges can cover up to 1.5 miles on a point-to-point application of the spectrum including signal propagation through vegetation and buildings. With these newly approved radios and appropriate antennas, wireless service can reach far beyond traditional boundaries. By utilizing more favorable unutilized TV spectrum bands than the ISM, the "White-Fi" would be able to support resource-intensive multimedia services more easily than the current Wi-Fi.

## 2.3 Direct Waveform Synthesis Transmitter for TV band Cognitive Radio

Many transceiver architectures are feasible for TV band applications, such as conventional superheterodyne transceivers, direct conversion transceivers, and software-defined radio transceivers. A conventional RF transmitter performs modulation, up-conversion, and power amplification. To accommodate various standards and requirements of TV band cognitive radios, frequency-agility and reconfigurability are two essential requirements in selecting transceiver architecture, since the multiple TV band cognitive radio standards and devices are going to operate on the vacant TV band white spaces with stringent requirements on

spurious emission. A highly-reconfigurable radio is needed as a versatile and low-cost solution.

### 2.3.1 Transmitter Architecture

A conventional direct conversion transmitter block diagram is shown in Figure 2.8. The digital baseband circuitry generates two digital signals (I/Q), the in-phase and the quadrature phase bitstreams. These digital bitstreams are first digitally up-converted and interpolated to match the rate of DAC, and then converted to an analog signal by the following DAC. Next, these two analog signals are then filtered to remove spikes and other spurious non-idealities, mixed up to the RF frequency, and sent off to the front-end power amplifier for transmission. The disadvantage of this transmitter architecture is that the up-conversion mixer and the frequency synthesizer in the analog/RF front-end have to achieve a wide tuning range and fast adaptation, if we need to cover a wide frequency range and hop around agilely. The analog/RF front-end will face stringent design challenges and consume a lot of power to meet the requirements.

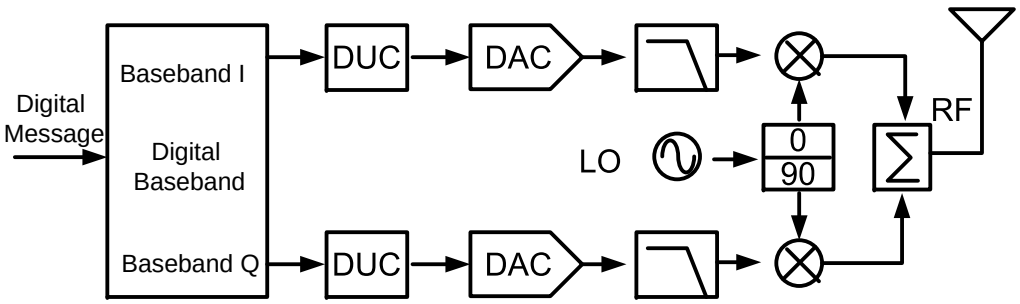


Figure 2.8: Conventional transmitter architecture

As we mentioned before, CR is a dynamically reconfigurable radio that adapts its operating parameters to the surrounding environment. By looking at this architecture closely, if the speed of the DAC can be increased substantially, the specifications for the filter stage and analog front-end would be relaxed. Therefore, the DAC can be moved toward the antenna, since part of the functions of the analog/RF front-end can be moved to the digital domain with DSP enhancements and compensation for analog impairments. As the advances of CMOS technology scaling, digital processing may be used to assist in removing or relaxing

the constraints on analog blocks, thus allowing a reduction of power consumption in the radio system. This leads to an transmitter architecture with flexibility and reconfigurability of digital processing, which is introduced in the next section.

In contrast to the traditional radio architecture, an alternative approach is to adopt mostly-digital implementation by moving the digital logics as close to the antenna as possible. Therefore, direct synthesis of digital waveforms and high-speed RF waveform conversion has drawn a lot of interests among researchers and engineers. This leads to the software-defined radio transmitter architecture for cognitive radio applications. As illustrated in Figure 2.9, the synergy of SDR and cognitive radio brings lots of benefits, including on-the-fly switching to multiple networks, reusability of components, and reconfigurability after manufacture.

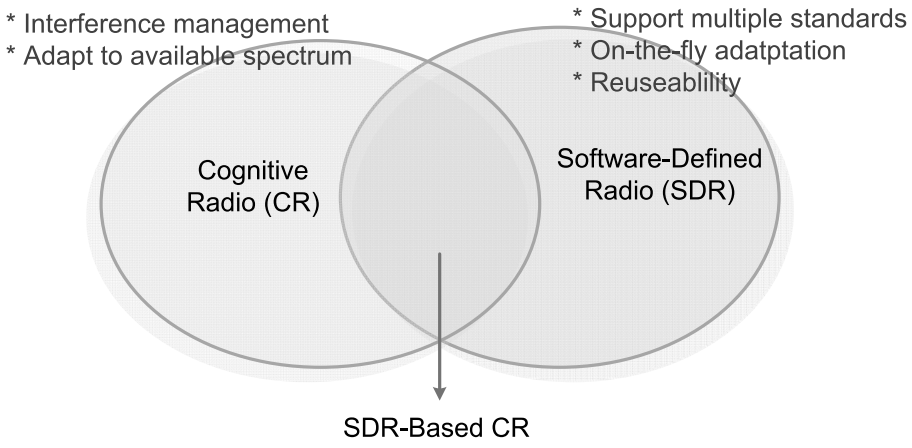


Figure 2.9: Synergy of software-defined radio and cognitive radio

In this work, the proposed architecture is based on the concepts of a direct conversion SDR style transmitter rather than a conventional superheterodyne architecture. The proposed transmitter is a direct waveform synthesis (DWS) transmitter, as illustrated in Figure 2.10. Under this mostly-digital transmitter architecture, the wideband IF/RF waveform is directly synthesized without the analog up-conversion stage (e.g. the mixer and the frequency synthesizer).

Waveform synthesis has been studied extensively in signal processing and communication communities [29–31]. A well-synthesized waveform, meaning one with good auto- and cross-correlation properties, can reduce computational burden at the receiver and in the meantime improve performance. This DWS transmitter architecture is mostly-digital, which can take

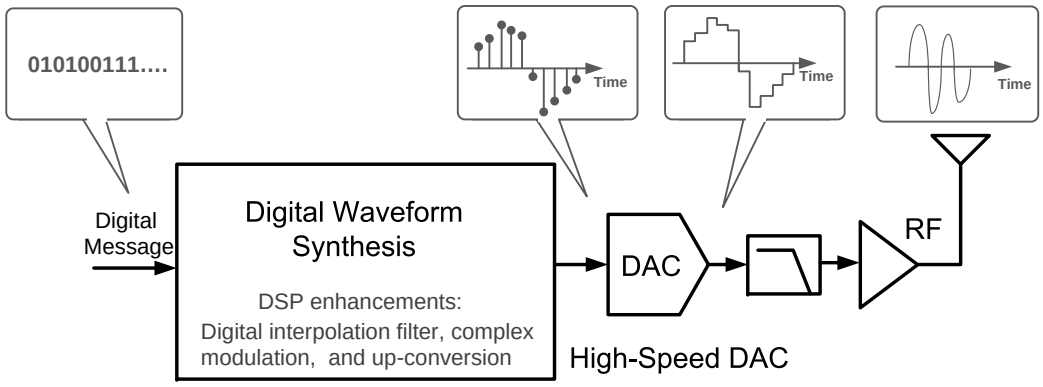


Figure 2.10: SDR-type transmitter architecture

advantage of the rapid performance increase due to the scaling of CMOS technology. All the complex modulation schemes and waveform generation are fully implemented in a generic digital processing unit or reconfigurable fabric (e.g. FPGA).

To hop around any available TV white spaces, the DWS transmitter achieves the best dynamic adaptation by directly synthesizing the waveform for transmission. With a full control of the waveform in the digital domain, the transmitter can quickly switch to various modulation schemes and transmitter parameters. The waveform is synthesized in the digital domain without using conventional heterodyne type or direct-conversion transmitter architectures.

The baseband waveform synthesizer produces the discrete sampled waveform in the digital domain. It supports complex I/Q modulation schemes and digital up-conversion. The digital interpolation filter adjusts the sample rate to match the sample rate between the baseband waveform generator and the DAC. The pulse-shaping filter, which is often the last baseband operation in the transmitter chain, is required to meet the specification of spectral mask and adjacent channel leakage power ratio(ACLR). It can also be integrated into the interpolating filter. It increases the sampling rate at the output of the filter and shapes the digital samples. This increase in sample rate is desirable as it allows a wider filter transition band, reducing the required number of coefficients in the digital filter. Then the synthesized discrete waveform samples are directly converted into a continuous-time analog waveform by a high-speed DAC with the sampling rate $f_{DAC}$. Also the higher sample rate also relaxes the requirements of the post-DAC reconstruction filter. Then the analog waveform is fed into the analog front-end module.

In TV band cognitive radio, one or more types of digital modulation schemes may be used depending on the requirements of the target data rate, channel conditions, spectral usage around the neighborhood. Digital modulation schemes differ greatly in performance and complexity. While simple linear PSK modulation schemes such as QPSK and $\pi/4$ QPSK offer the best trade-off between power and bandwidth requirements. Other more complex nonlinear modulations, such as GMSK provide high spectral efficiency with the desirable constant envelope behavior for low data rate wireless systems. The high-data rate transmission leads to the inclusion of schemes such as 8-PSK, M-ary QAM, and OFDM. Given the reconfigurability, the baseband can adapt from one standard to another. Also, the dynamic reconfiguration technology in FPGA permits the run-time adaptation of baseband hardware without interrupt he connectivity. This capability enables the run-time reconfiguration of transceiver baseband, modulation schemes, and waveform synthesis engine, etc.

The interpolation filters and complex numerically controlled oscillator (NCO) functions for digital mixer can be easily and efficiently implemented in the digital platforms, such as reconfigurable fabric or digital signal processors. Efficient implementation of OFDM modulation and demodulation is also possible on the reconfigurable fabric, since the inverse fast Fourier transform (IFFT) and fast Fourier transform (FFT) algorithms exhibit a high degree of parallelism. Also the digital up and down conversion chains, pulse shape filtering, CDMA bit level processing, Transmit Crest Factor Reduction, Turbo, Viterbi, and Reed Solomon decoding are all good condidates to benifit from the processing power and programmability in the digital domain.

By moving more functional blocks into the digital domain, we can benefit from CMOS scaling. However, for wideband applications, the primary challenge with this architecture is a drastic increase in the difficulty of digital-to-analog conversion. The transmit D/A converter operating nearly at the RF frequency must have high dynamic range and high precision to keep the output signals within the transmit spectral mask. This mostly-digital architecture without an up-conversion stage is essentially carrier-less, communicating at the baseband by sending out the digital synthesized waveforms. It takes the full advantage of the digital approach in waveform conditioning and adapts in a very short time. The nature of this radio lends itself to a digital implementation and promises power reduction through lower supply voltages and scaled geometries, as well as a more efficient and straight-forward transmitter design.

The advantages of the DWS transmitter are highlighted as follows:

- Digital combination of signals from multiple channels

- Software programmable or reconfigurable
- Full control of modulation schemes

## 2.4 Design Challenges on Digital/Analog Boundary

The bottleneck of this SDR-type transmitter is the digital-to-analog conversion stage. The wide bandwidth and high dynamic range requirements result in extreme stringent design specifications. In particular, the DAC speed and resolution become of utmost importance. To fulfill the Nyquist rate requirement, the sampling rate at DAC should be at least two times of the highest frequency component in the target synthesized signal frequency(Figure 2.11). Nyquist synthesis of the wider bandwidth requires the DAC clocking above GHz which may consume enormous amounts of power relative to our low power target. Additionally, the high-speed DAC may place severe limitations on jitter requirements. The power consumed in the wideband front-end stage as well as the necessary sensitivity and gain requirements for those blocks are also important. Finally, the area and power burden coming from digital signal processing and demodulation blocks must be considered.

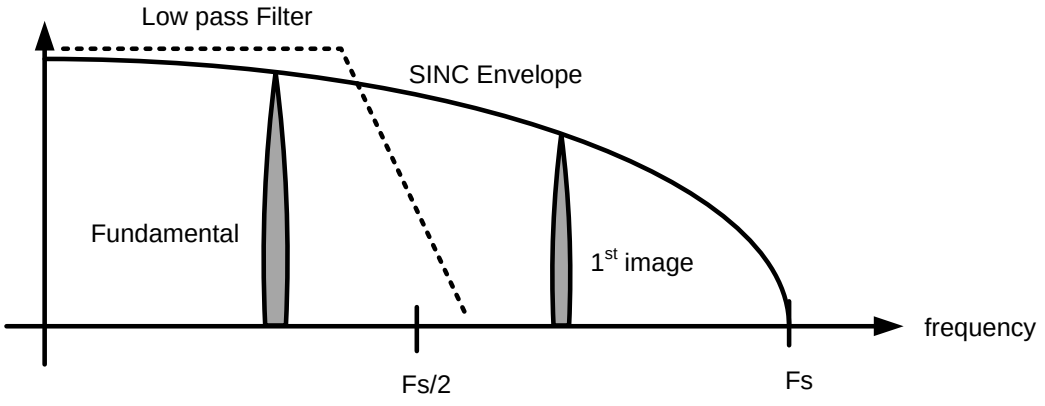


Figure 2.11: Nyquist rate synthesis using the fundamental spectrum

High sampling rate and high linearity are the two critical requirements in D/A conversion for thsi architecture. For example, in TV band CR applications, the DAC sampling rate must be above 1.6GS/s for synthesizing a 800MHz signal. If the filter stage is considered, the DAC sampling rate will need to be increased even higher to relax the specifications for realistic

filter design. Nyquist rate synthesis imposes strict design requirements in DAC sampling rate and system complexity. Also, the DAC needs to have $10 \sim 12$ bit resolution in order to support the modulation schemes in IEEE 802.22 or other standards.

To fulfill the Nyquist rate requirement, the sampling rate at DAC should be at least two times of the highest frequency component of the target synthesized signal frequency. A 10-bit DAC with 1.6GS/s with high SFDR (e.g. >60dB) is very challenging, even with state-of-the-art CMOS technology especially in low power applications. High-speed and high-linearity requirements result in high power consumption, high implementation cost and system complexity. This implies that the critical challenge is on the boundary of digital and analog. Our main objective is to investigate the technique of the digital-to-analog conversion for reducing the complexity of the signal processing blocks in the digital front-end.

In order to overcome the design specifications of Nyquist rate synthesis, a sub-Nyquist rate DWS transmitter is proposed as shown in Figure 2.12. It is similar to the conventional SDR-type transmitter but the synthesized digital waveform is directly converted by a high speed multi-mode sub-Nyquist rate DAC followed by a tunable band-pass filter.

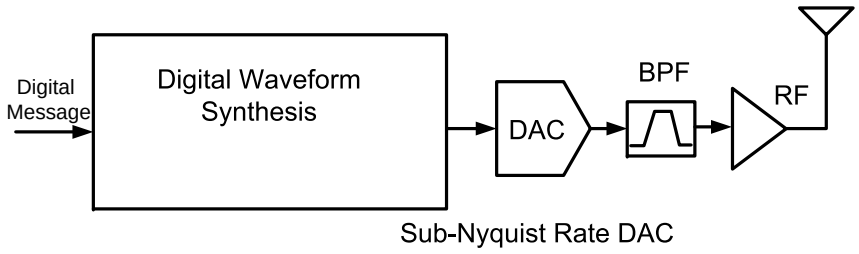


Figure 2.12: Sub-Nyquist rate DWS transmitter architecture

The conceptual frequency domain response is shown in Figure 2.13. Instead of using the fundamental spectrum, the first image can be extracted by a bandpass filter for transmission, therefore, eliminating an up-conversion stage.

In this mostly digital transmitter, we propose to clock the DAC below the Nyquist rate and utilize the image spectrum. With the reduced sampling rate, it helps the transmitter avoid the complex high-speed DAC design and high power consumption. Figure 2.14 shows the concept of sub-Nyquist rate conversion and the utilization of image spectrum. Intuitively, this is the reciprocal of the sub-sampling receiver. The technique of sub-sampling is now moved to the digital-to-analog conversion stage at the transmitter side. In order to synthesize

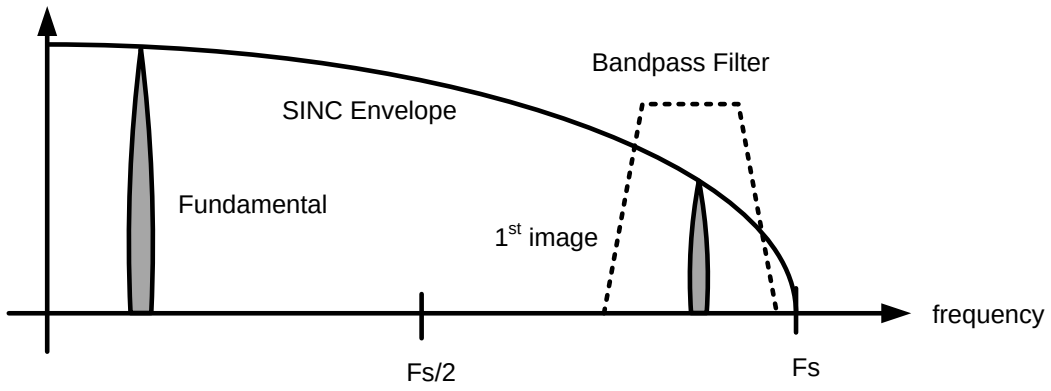


Figure 2.13: Utilize the image spectrum

the signal for transmission in higher Nyquist zones, the sampling rate of the DAC and the fundamental spectrum need to be configured carefully based on the frequency plan.

Due to the nature of non-return-to-zero (NRZ) reconstruction in the DAC output, the SINC roll-off attenuate the image spectrum located in higher Nyquist zones. Also, the null frequencies at the multiples of the sample frequency create the dead zones which prohibit direct wideband synthesis across Nyquist zones. To overcome the attenuation and null frequencies of the SINC envelope, special techniques have to be used in the reconstruction stage.

The prior art of direct waveform generation using the harmonics/image spectrum can be found in [19, 20]. Both of these two examples use the same technique, return-to-zero, which effectively flattens the SINC envelope and moves null frequencies to the higher regions.

In the next chapter, we will review and analyze the NRZ and RZ techniques in the prior art as well as the proposed two-phase holding (TPH) reconstruction, which enables the multi-mode sub-Nyquist rate front end.

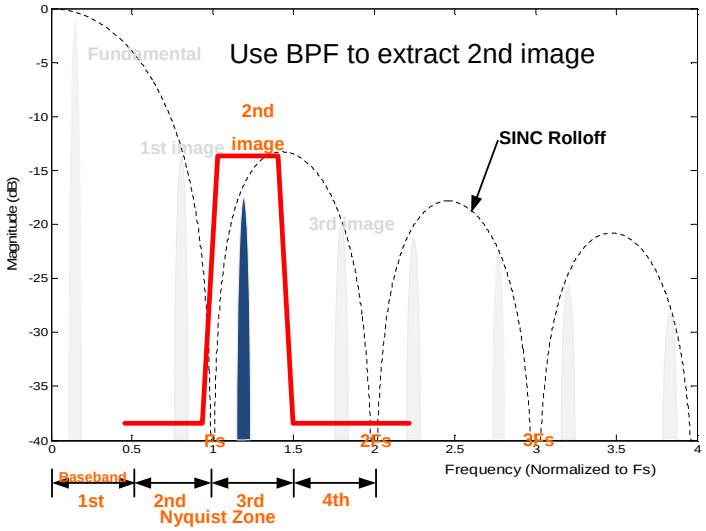


Figure 2.14: Sub-Nyquist rate digital-to-analog conversion

# Chapter 3

# Multi-Mode Sub-Nyquist Rate Digital-to-Analog Conversion

The previous chapter introduces the concept of direct waveform synthesis transmitter for TV band cognitive radio applications. Regarding the critical D/A conversion stage, the evolution of high-speed DACs in RF communication systems is driven by cost, power and performance. The state of the art DAC from Broadcom [27] demonstrates the possibility of implementing high-speed DACs above 2GS/s with high resolutions and high dynamic ranges. Other DACs [32–36] also show the good dynamic linearity performance over a wide output frequency range. Those advances and development, open the door to the direct generation of high bandwidth multi-carrier signals in communication systems. In this chapter, the signal reconstruction methods will first be reviewed. Then the proposed multi-mode sub-Nyquist rate conversion is introduced and discussed.

## 3.1 Analog Signal Reconstruction

### 3.1.1 Non-Return-to-Zero

In the time domain, the DAC takes the discrete samples and converts them into electrical signals, either current or voltage. Then the DAC reconstructs the continuous-time signal by holding the electrical value until the end of this sample period. The operation can be written

as the discrete samples, x[n], convolving with the DAC output holding reconstruction pulse, $h_0(t)$:

$$I_{DAC}(t) = \sum_{n=-\infty}^{\infty} X[n]h_0(t - nT_S) \tag{3.1}$$

where Ts is the DAC sample period. Figure 3.1 illustrates the operation of D/A conversion.

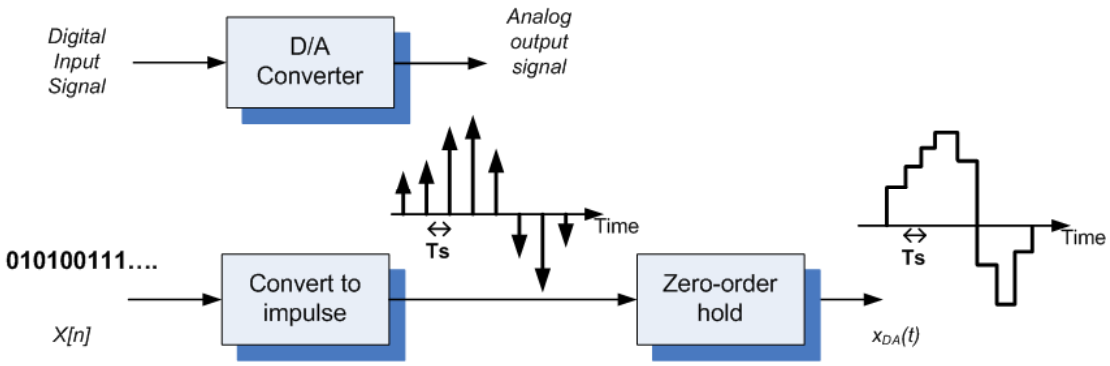


Figure 3.1: The time domain operation on the boundary of digital and analog

The Fourier transform of the reconstructed output $I_{DAC}(t)$ is

$$I_{DAC}(j2\pi f) = X(e^{j2\pi f T_s}) \cdot H_0(j2\pi f) \tag{3.2}$$

and

$$X(e^{j2\pi f T_s}) = \frac{1}{T_s}\left(\sum_{n=-\infty}^{\infty} X_a(j(2\pi f - \frac{2\pi n}{T_s}))\right) \tag{3.3}$$

$H_0(j2\pi f)$ is the frequency response of the reconstruction pulse. If Zero-Order-Hold (ZOH), also known as Non-Return-To-Zero (NRZ), is chosen, the response of $H_0(j2\pi f)$ is easily shown to be $H_{NRZ}(j2\pi f)$.

$$H_{NRZ}(j2\pi f) = \frac{2sin(\pi f T_s)}{2\pi f} e^{-j2\pi f T_s/2} = SINC(f \times T_s) e^{-j2\pi f T_s/2} \tag{3.4}$$

The spectral characteristic is shown in Figure 3.2 where the terms annotated here are defined in [37]. The DAC output reconstructed by NRZ has the SINC envelope in the frequency domain. Mathematically, the spectral characteristic of DAC outputs without

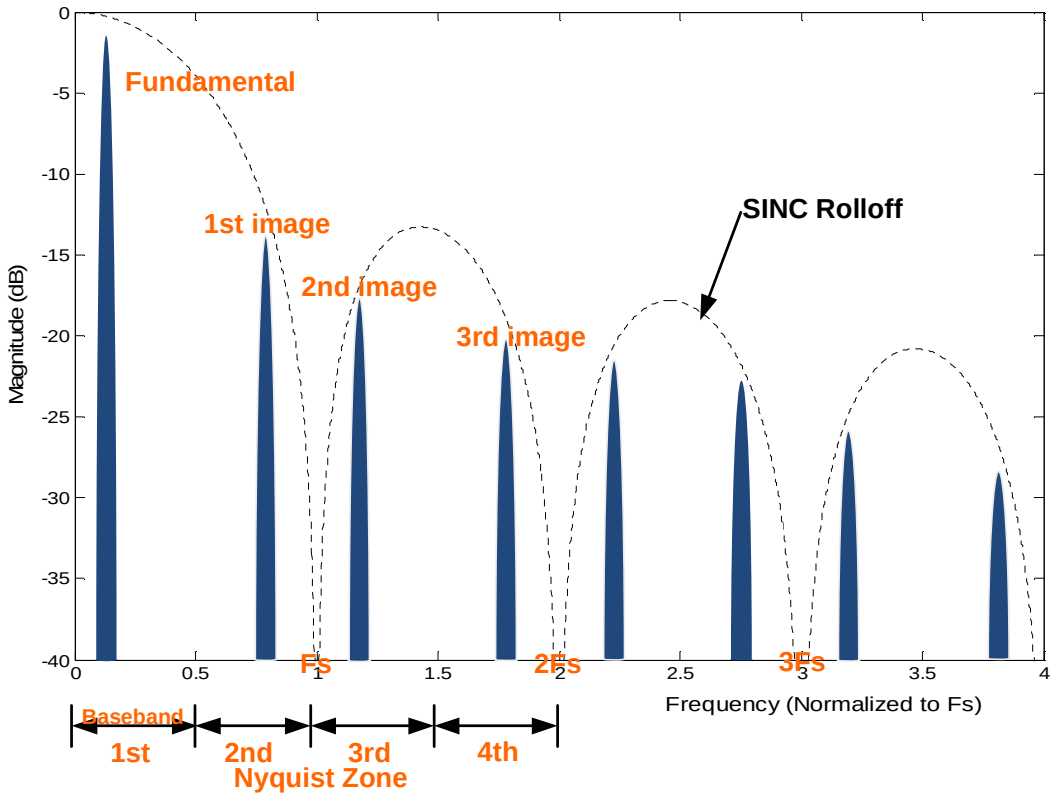


Figure 3.2: The frequency domain response of NRZ reconstruction

quantization noise is the SINC function multiplying the continuous-time baseband spectrum located around the multiples of Fs.

$$I_{DAC}(j2\pi f) = \frac{1}{T_s}\left(\sum_{n=-\infty}^{\infty} X_a(j(2\pi f - \frac{2\pi n}{T_s}))\right)H_{NRZ}(j2\pi f) \tag{3.5}$$

As mentioned in the previous chapter, the SINC roll-off should be taken into account if sub-Nyquist rate conversion and the image spectrum are used for direct waveform generation. In the following section, we will review the return-to-zero technique for its applications in wideband synthesis.

### 3.1.2 Return-to-Zero

To flatten the SINC roll-off, one of the possible solutions is to reduce the holding period of the DAC output. This leads to the well-known Return-to-Zero (RZ) techniques in signal reconstruction at the DAC's outputs [19,20]. Figure 3.3 shows the time domain operation of RZ. The output is reset every other half clock cycle. The output is similar to the conventional NRZ DAC, except that the output pulses only have half the width and the first null frequency is pushed at 2 Fs.

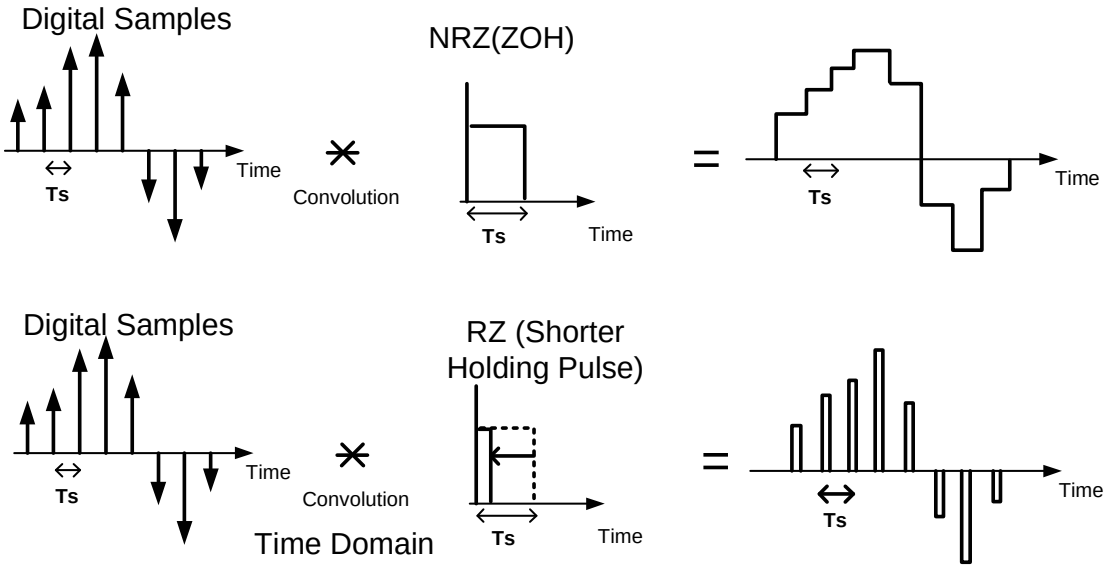


Figure 3.3: The time domain operation of NRZ and RZ

For a shorter holding pulse, the frequency response of the holding pulse $H_{RZ}(j2\pi f)$ is easily shown to be:

$$H_{RZ}(j2\pi f) = \frac{T_p}{T_s} SINC(f \times T_s) e^{-j2\pi f T_p/2} \tag{3.6}$$

where $T_p$ is the holding pulse width and $T_p/T_s$ is the magnitude scaling factor.

By reducing the width of the holding pulse, $T_p$, the null frequencies are moved to higher frequencies. For example, if the holding pulse is reduced to 1/4 of the original period, the null frequencies are pushed to the frequency four times higher. Figure 3.4 shows the effect of holding pulses with different duty cycles. The SINC roll-off is flattened due to the null frequency being pushed to higher frequencies. However, the magnitude of the fundamental

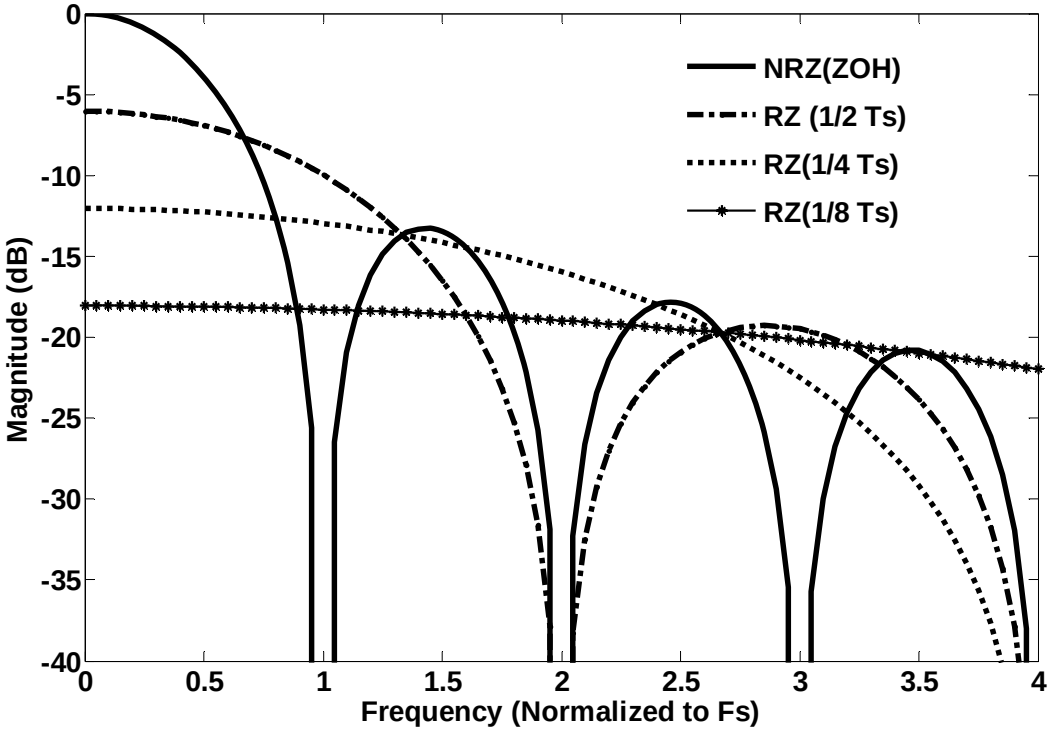


Figure 3.4: NRZ and RZ with various duty cycles

spectrum and its images is attenuated because the shorter holding pulse contributes less signal energy. RZ flattens the response and delivers more power around the second and third Nyquist zones. But the attenuated signal strength significantly impacts the performance of the transmitter. The reconstruction process of NRZ or RZ can be viewed as a filter function for shaping the spectrum envelope. NRZ and RZ are two common types of reconstruction processes due to the simplicity of hardware implementation.

RZ technique is used for direct wideband signal generation. In [19], a 1.2 GS/s DAC demonstrated direct waveform generation for four 5MHz WCDMA signal in 900MHz by using the first image spectrum. In [20], the same technique is applied to demonstrate the RZ technique for multiple Nyquist zone operation.

## 3.2 Proposed Two-Phase Holding

After discussing the NRZ and RZ techniques in the previous section, the two-phase holding (TPH) reconstruction is proposed to shape the spectrum envelope more aggressively in this work. As illustrated in Figure 3.5, the sample period is divided into two phases. In the first phase, the DAC takes the digital sample and holds for $T_p$. In the second phase, the DAC produces the inverted version of the digital sample in the output for $T_s - T_p$.

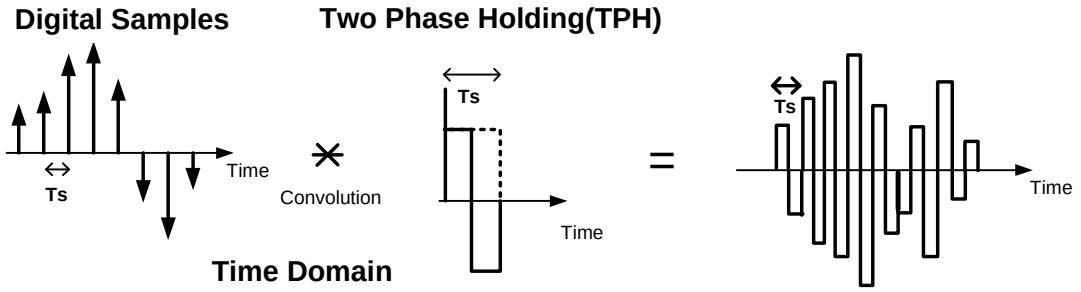


Figure 3.5: The time domain operation of TPH

The frequency response of two-phase holding (TPH) can be expressed as the following equation:

$$H_{TPH}(j2\pi f) = \frac{T_p}{T_s} sinc(f \times T_s) e^{-j2\pi f T_p/2} + \frac{T_s - T_p}{T_s} sinc(f \times (T_s - T_p)) e^{-j2\pi f (T_s+T_p)/2} \quad (3.7)$$

As shown in this example, the output holding pulse has two phases and each phase is half of the clock period. The output alternates between the original and inverted samples. Because the inverted phase provides signal energy into the analog output waveform instead of resetting in the second phase, the magnitude of the output image spectrum is enhanced. The TPH operation can be viewed as the superposition of one RZ operation and the other time-shifted and inverted RZ operation.

Intuitively, the frequency response of this two-phase operation is a high-pass response by nature since the DC is zero. The spectrum envelope is shifted to higher frequencies. Especially, the signal is enhanced significantly around the sampling frequency Fs. More signal energy is directed to have higher signal gain around the second and third Nyquist zones in comparison with NRZ or RZ operation. By manipulating the sampling rate and the holding pulse period, the spectrum envelope can be configured to achieve a better flat

response with minimum attenuation over the target bands. Figure 3.6 shows the envelopes of TPH reconstruction. As we can see that TPH mode creates a better response covering 400MHz $\sim$ 800MHz than that of NRZ or RZ mode. This frequency range is where the major TV white spaces locate.

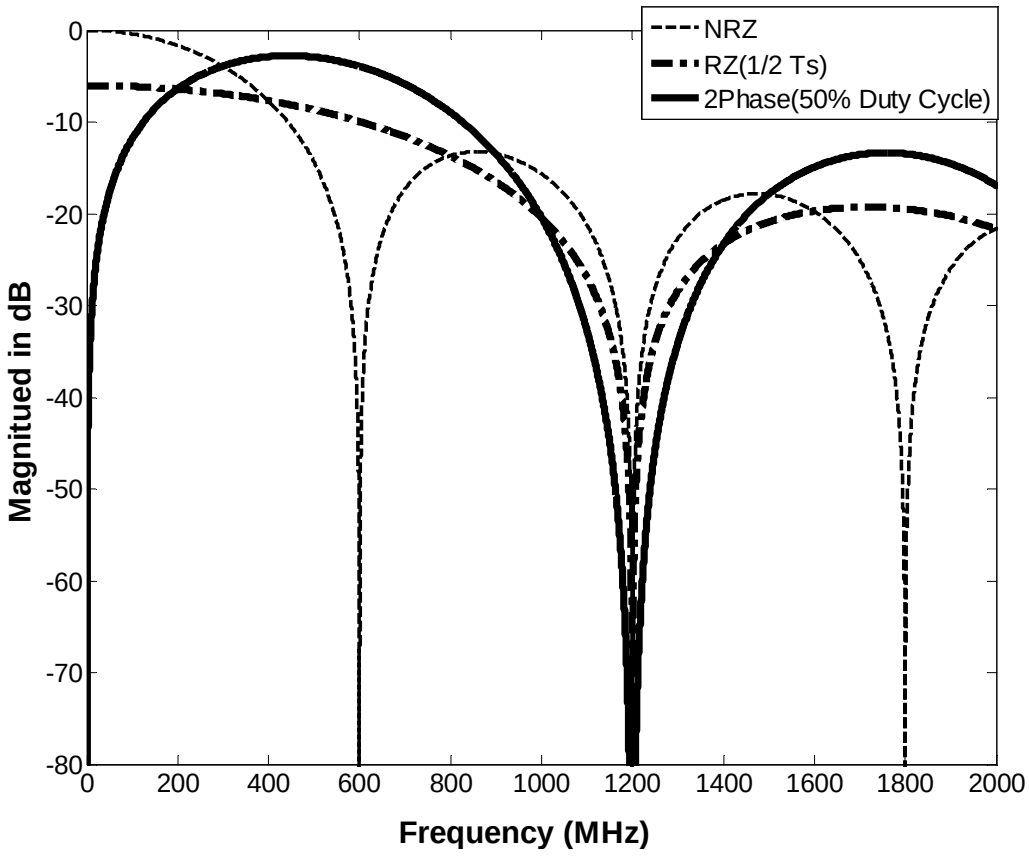


Figure 3.6: Two phase holding with 50% duty cycle

## 3.3 Variable Duty-Cycled Two-Phase Holding

We can further control the duty cycle of two phases so that the spectrum envelope is shaped to enhance different Nyquist zones. Figure 3.7 shows an example of the 25% duty cycle with two-phase operation. This operation provides more energy in high-frequency band in the fourth and the fifth Nyquist zones, around 1000 to 1400 MHz. Without 25% TPH,

this region is highly attenuated in NRZ and RZ and 50% TPH modes due to the location of null frequencies.

It is possible to utilize higher order image spectrum for direct waveform synthesis since the spectrum envelope is shaped into a wider range in the 25% duty cycle TPH mode. This operation provides an opportunity in using even high order harmonics/image spectrum like the fourth or the fifth Nyquist zone.

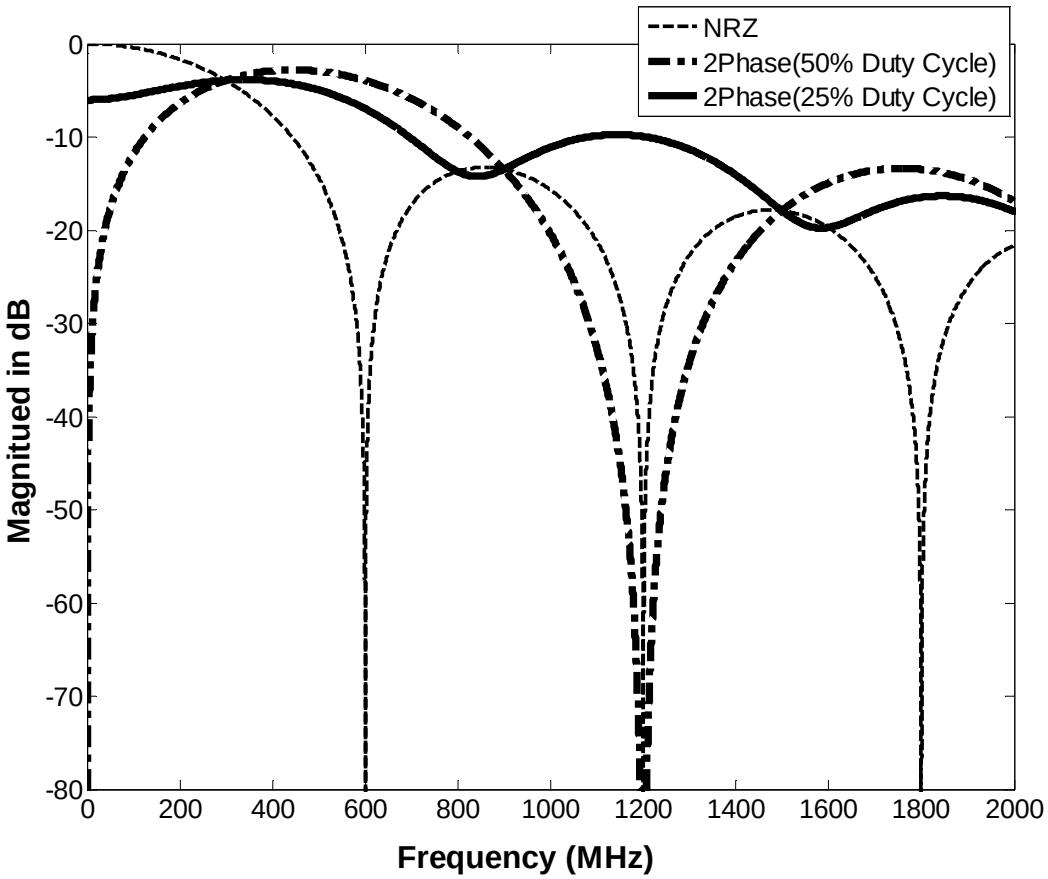


Figure 3.7: Two phase holding with 25% duty cycle

The sensitivity of the duty cycle variation and sampling period variation is analyzed by the system-level simulation in Matlab. The effect of the sampling period variation, ±5%, is shown in Figure 3.8. Clearly, the variation of the sampling period effectively moves the location of the nulls around the multiple of the sampling frequency. Also the magnitude response has less than 0.3 dB deviation from the nominal response from 200MHz to 900MHz.

The effect of the duty cycle variation, ±5%, is shown in Figure 3.9. If the duty cycle of the

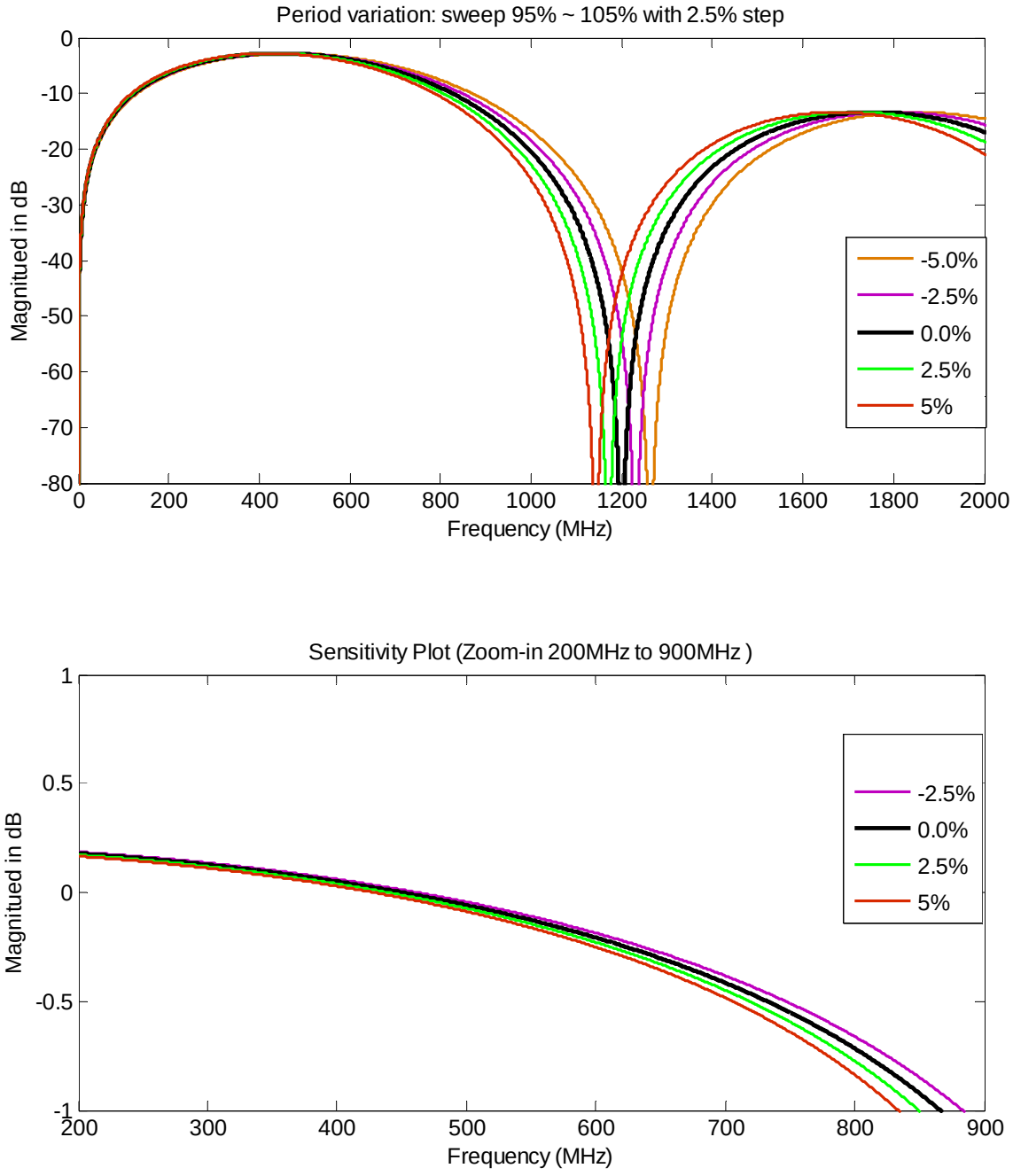


Figure 3.8: Two phase holding with period variation

two phase is not ideal 50%, the original and inverted samples won't be able to canceled out perfectly. So the envelope does not have the deep notches around the multiple of the sampling

frequency. Also the magnitude response deviates less than 0.15 dB from the nominal response from 200MHz to 900MHz.

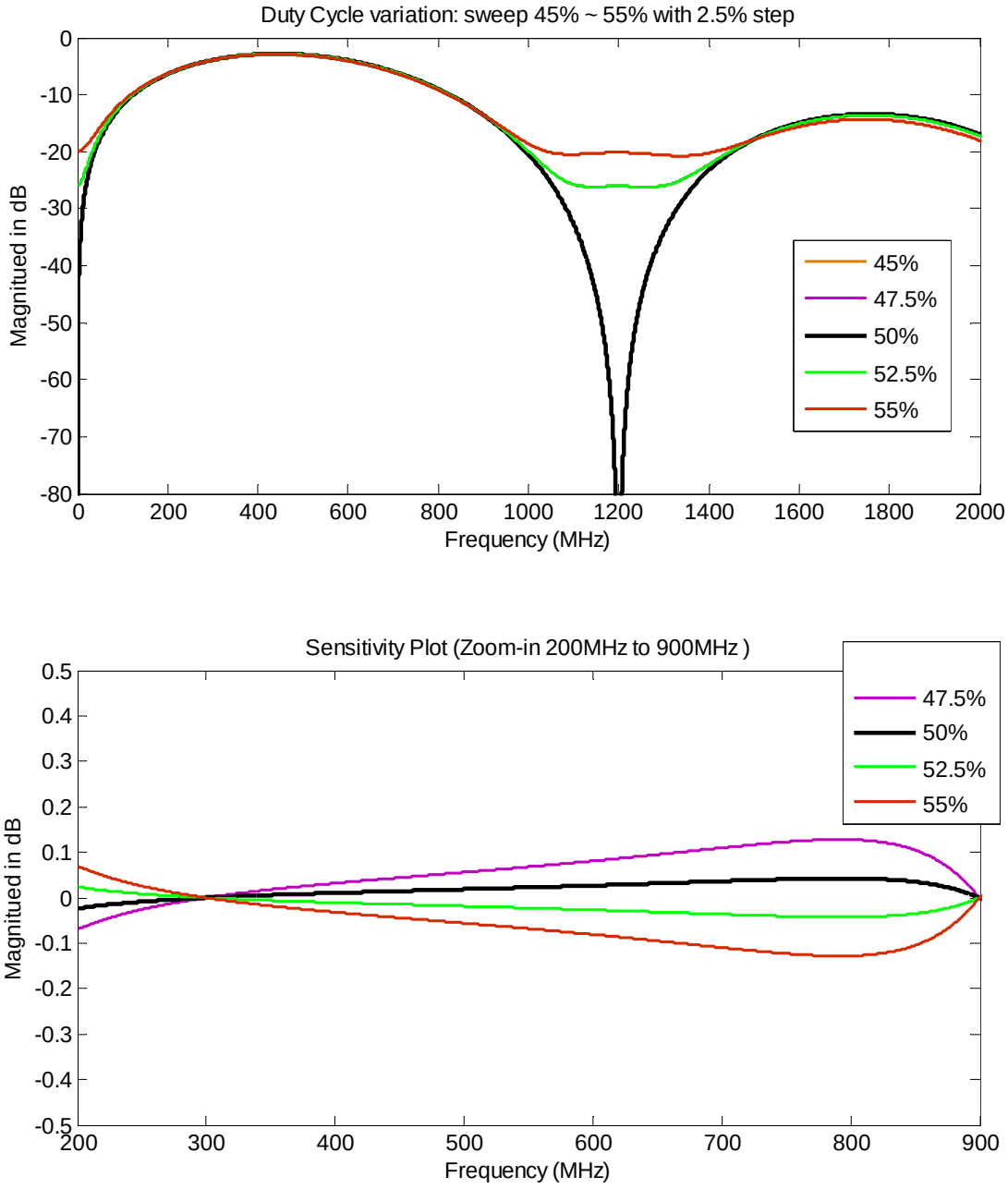


Figure 3.9: Two phase holding with duty cycle variation

## 3.4 Multi-mode Sub-Nyquist Rate Conversion

Combining the advantages of NRZ, RZ, and TPH mode, the multi-mode sub-Nyquist rate DAC is proposed for direct waveform synthesis in TV band cognitive radio applications. There are three major reconstruction modes: NRZ, RZ and TPH mode. The proposed multi-mode DAC uses a specially designed output switching stage for generating two-phase inverted output samples in each sampling period. In TPH mode, the DAC output switch is configured into two phases $T_p$ and ($T_s$ - $T_p$). The duty cycle of two-phase holding can be configured as 25% and 50%. The proper operation mode is selected based on the target channel of synthesized RF waveform. Figure 3.10 summarizes the proposed multi-mode operation and their corresponding spectral characteristics.

The target TV band is 54MHz $\sim$ 862MHz. To achieve the best response in the frequency domain, the DAC output switching stage is dynamically reconfigured into NRZ, RZ or TPH mode, depending on the transmission TV channels. To optimize the full TV band, the best sampling rate is 600MS/s, which provides the best spectrum envelopes. For synthesizing RF waveforms in the lower TV channels, the multi-mode DAC configures the output switches to perform conventional NRZ operation. To utilize higher channels around the second and third Nyquist zone, the DAC reconfigures the output switches to TPH mode. This proposed sub-Nyquist rate DAC operates over a wideband range because of the flexibility to adapt the DAC into different reconstruction modes.

Depending on the synthesis requirements, NRZ, RZ, or TPH mode can be applied for reconstruction. The target signal for transmission is synthesized in either the fundamental from the first Nyquist zone or image spectrum over higher Nyquist zones.

## 3.5 Implementation Considerations and Issues

The implementation of sub-Nyquist rate DAC reflects the issues and design considerations in terms of static and dynamic specifications. The important design trade-offs have been discussed and investigated in more depth in the literature [37]. The design choices that optimize these tradeoffs are adopted in the final DAC design.

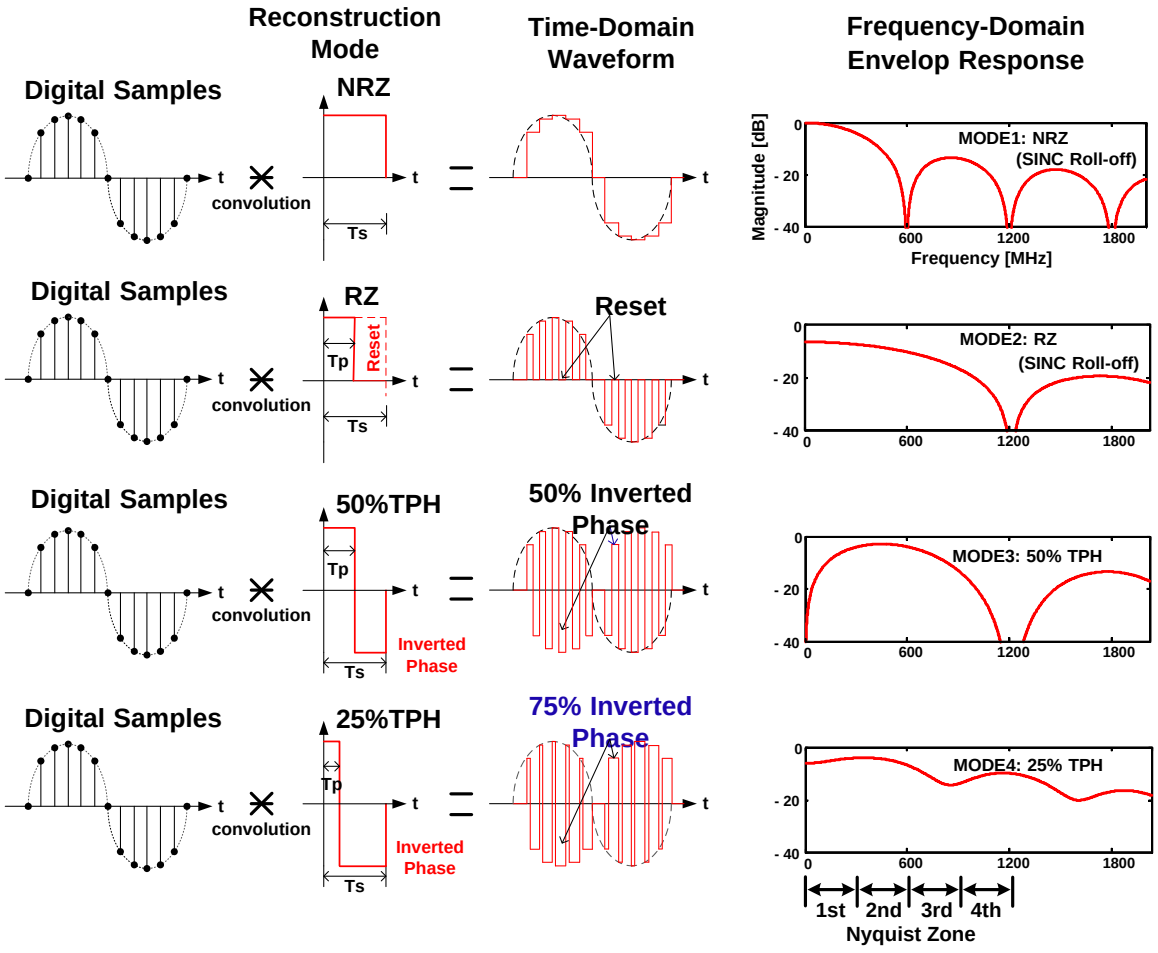


Figure 3.10: Summary of multi-mode reconstruction

### 3.5.1 DAC Architecture

The semiconductor process technology significantly affects the choice of DAC's architecture. Bipolar and BiCMOS provides higher speed while dissipating more power. In CMOS technology, DACs typically operate with a single supply with separate analog and digital power and ground pins. More advanced CMOS DACs overcome the performance limitation and offer low cost and low power consumption. These high-speed DACs used in the transmit signal path construct the complex modulated analog waveforms with wide bandwidth, high dynamic range and high sampling rate. For high-speed applications the current-steering architecture is widely used as the architecture of choice [27, 32, 33, 38, 39].

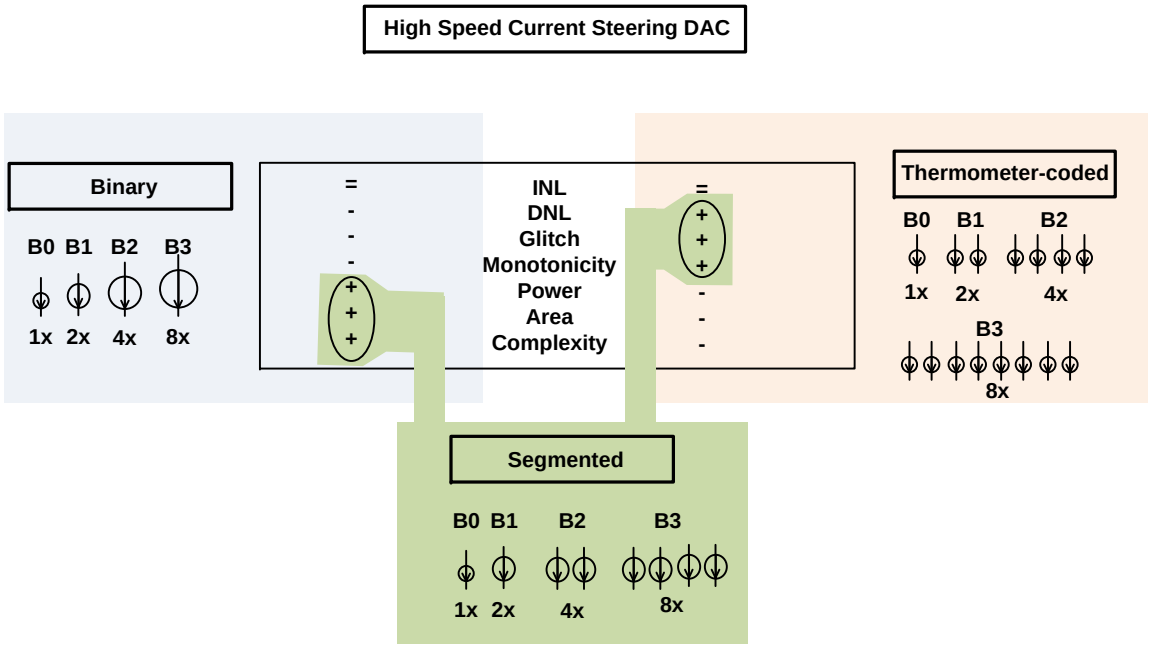


Figure 3.11: Binary, Thermometer-coded, and Segmented DAC

Thermometer-coded converters have significantly better DNL, less glitch energy, and monotonicity, while binary-weighted converters use less area with no need of the decoder for input codes [36]. A segmented design was chosen to combine the advantages of thermometer-coding and binary-weighted coding in a single DAC. Thermometer coding is used for the MSBs of the converter, while binary weighting is used for LSBs. The obvious question here is how to segment the converter (i.e. how many bits should be represented by unit-element array and how many by binary-weighted elements). This issue has been analyzed in [40]. Based on Matlab simulation, the optimal segmentation for this design is 6-bit thermometer-coded and 4-bit binary-weighted.

### 3.5.2 Static Linearity

The specification of communication systems and radios are usually characterized in the frequency domain. Linearity is one of the most important factors for evaluating high-speed DACs. For cognitive radio application, multiple carriers or multi-channels have to be syn-

thesized and transmitted simultaneously by transmitter DACs. The peak power remains the same but the average power decreases. This requires DACs to have high dynamic range and high linearity in order to meet the specifications of the output spurious emission. Therefore, frequency domain (AC linearity) performance is considered with static (DC linearity) and time domain specifications. Both AC and DC nonlinearities will manifest themselves and cause distortion, noise, and spurs.

The DC linearity is specified by differential nonlinearity (DNL) and integral nonlinearity (INL). DNL is defined as the worst-case deviation from an ideal one-LSB step, $\Delta$, between two subsequent output codes. INL is defined as the maximum deviation from a linear approximation to the DAC's real transfer function as shown in Figure 3.12. Assuming that the DAC output values ($Y_k$) are corrected for gain and offset error, the DNL and INL at an input code, $X_k$, can be expressed as

$$DNL_k = \frac{Y_k - Y_{k-1}}{\Delta} - 1, \quad INL_k = \frac{Y_k - X_k\Delta}{\Delta} \tag{3.8}$$

The worst-case DNL and INL are

$$DNL = \max_{k \in 1 \ldots 2^N} \{|DNL_k|\}, \quad INL = \max_{k \in 1 \ldots 2^N} \{|INL_k|\} \tag{3.9}$$

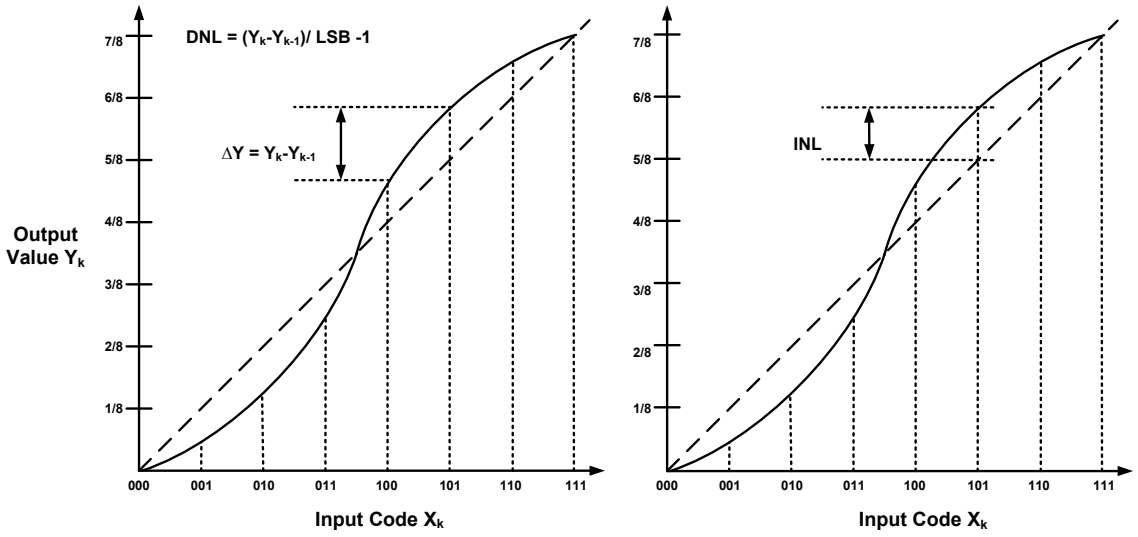


Figure 3.12: DNL and INL

For a current-steering D/A converter, the INL is mainly determined by the matching behavior of the current sources. A parameter that is well suited for expressing this technology versus DAC-specification relation is the INL yield. This INL yield is defined as the ratio of the number of DACs with an INL smaller than LSB to the total number of tested DACs.

### 3.5.3 Distortion

All DACs exhibit certain degree of harmonic distortion. The harmonic distortion is a measure of how well the DAC reproduces a perfect sinusoid at its output when its input is driven with a numeric sequence representing an ideal uniformly sampled sinusoid. The distortion can results from non-ideal static behavior and non-ideal dynamic behavior.

We can use the information from the DAC transfer curve to evaluate the frequency domain behavior to the first order. Frequency domain characterization of high-speed DACs is based on single tone or multi-tone sine waves response seen in the DAC's analog output. By driving the DAC with digitally synthesized sine waves, the output spectrum can be simply analyzed or measured by a spectrum analyzer.

The dynamic linearity of conventional DACs is generally specified in terms of Spurious Free Dynamic Range (SFDR) and Intermodulation Distortion(IMD) in units of dBc. SFDR is the most often quoted AC specification, which defines the RMS power of the fundamental and the largest unwanted spurious tone within the band of interest (usually from DC to Nyquist frequency), as shown in Figure 3.13 . SFDR is usually expressed in dB as:

$$SFDR = 10 \cdot log_{10} \frac{P_s}{P_{Spur(max)}} \tag{3.10}$$

The ideal sinusoidal input is distorted by the non-ideal static of the DAC. The static characteristics relate to how the transfer function deviates from a straight line. The output spectrum will contain harmonic content due to the non-ideal transient and static behavior. The transfer function shown in Figure 3.14 is intentionally exaggerated for the purpose of illustrating how static linearity error could cause the distortion at the DAC's output. The transfer function of modern high-speed DACs barely deviates from the ideal straight line, but even the slight deviation might cause harmonic spurs to appear in the output spectrum.

In conventional current-steering DACs, the SFDR degrades rapidly with the increasing input frequencies due to the distortion and the non-ideal transient response. In the literature, the sources of dynamic distortion have been extensively discussed. The possible sources which degrade the SFDR performance are summarized below.

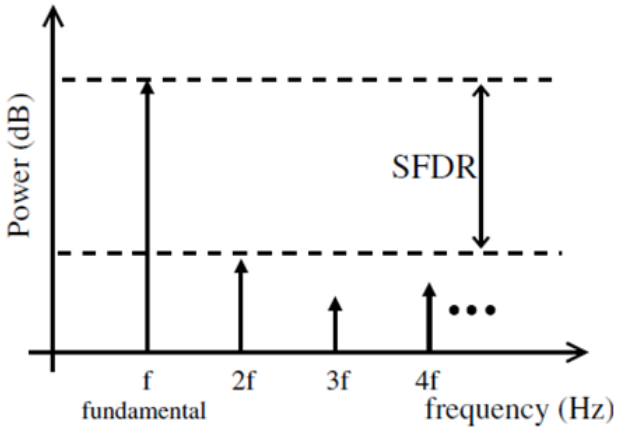


Figure 3.13: Spurious free dynamic range

- Amplitude mismatch: Process mismatch in the current sources results in non-ideal VTC and the static errors after the DAC settles to its steady-state. Amplitude error due to current mismatch can be divided into deterministic and random; process gradients cause spatial deterministic errors, and short distance mismatch causes spatial random errors. These subclasses distinguish the signal errors (INL) on the way they scale when a specific physical parameter (dimension of transistors) changes. If the current source transistor size is increased, the random components of mismatch drop and the systematic increase. For every extra bit of accuracy required, the area increases by a factor of four to reduce the random errors, but the deterministic errors scale up similarly.

- Code-dependent glitch: Code-dependent glitches will produce both out-of-band and in-band harmonics when the DAC is reconstructing a digitally generated sine wave as in a direct digital synthesis (DDS) system. The midscale glitch occurs twice during a single cycle of a reconstructed sine wave (at each mid-scale crossing), and will therefore produce a second harmonic of the sine wave, as shown in Figure 3.15. Note that the higher order harmonics of the sine wave, which alias back into the first Nyquist zone (DC to fs/2), cannot be filtered.

- Code-dependent and frequency-dependent output impedance: The tail current sources are not ideal. The output impedance of the current cells are modulated by the input signal and output swing. This will introduce the nonlinear distortion across frequency.

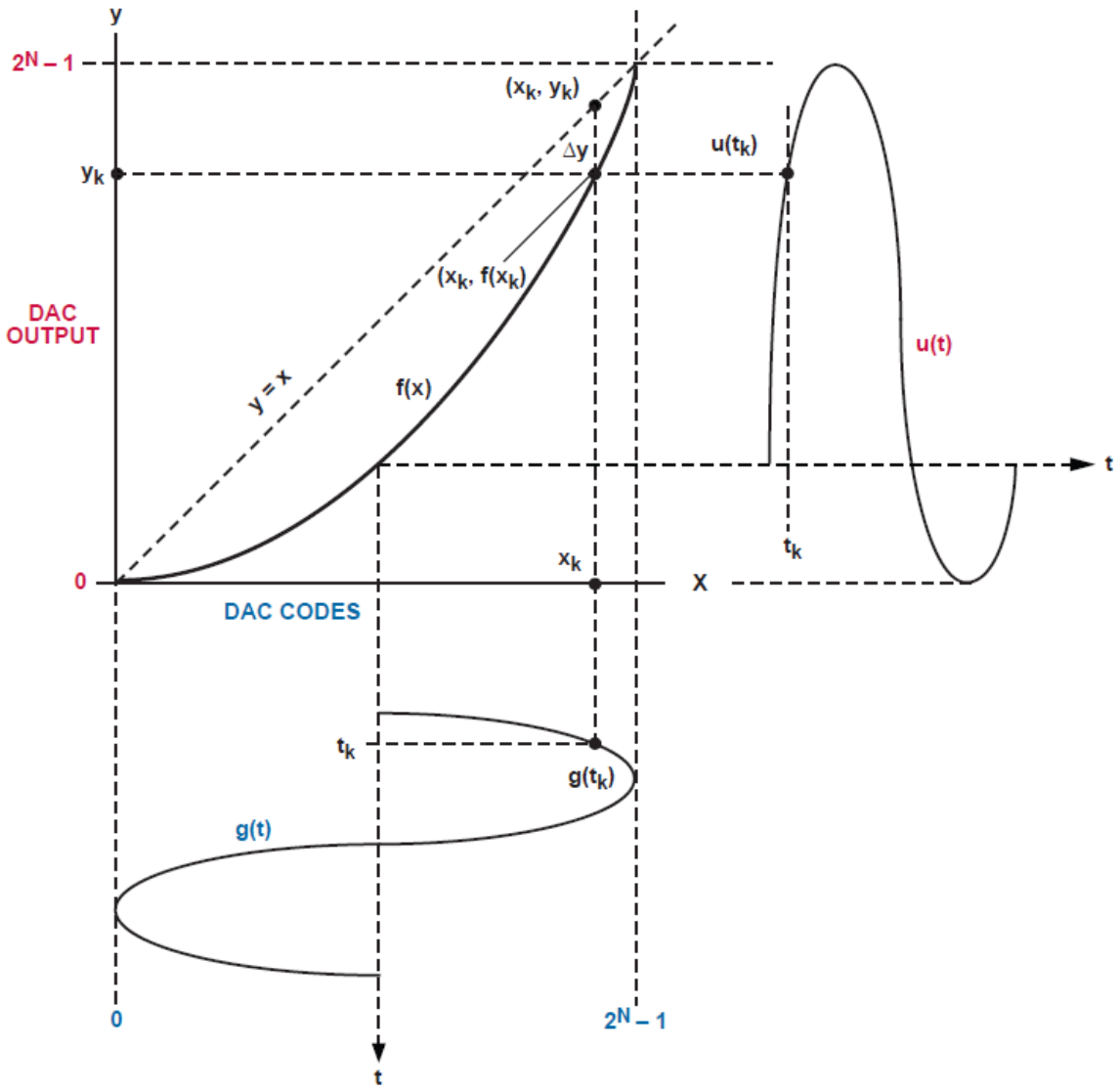


Figure 3.14: Distortion caused by the non-ideal transfer function curve

- Charge Feedthrough: This phenomena can arise from the switch control signals to the output node, and from the common source node to the biasing nodes. Also, the nonlinear V/I transfer function of the switch transistors which creates spikes in the switch common source node. The feedthrough/coupling of data-dependent switching signals causes interferences on the biasing nodes.

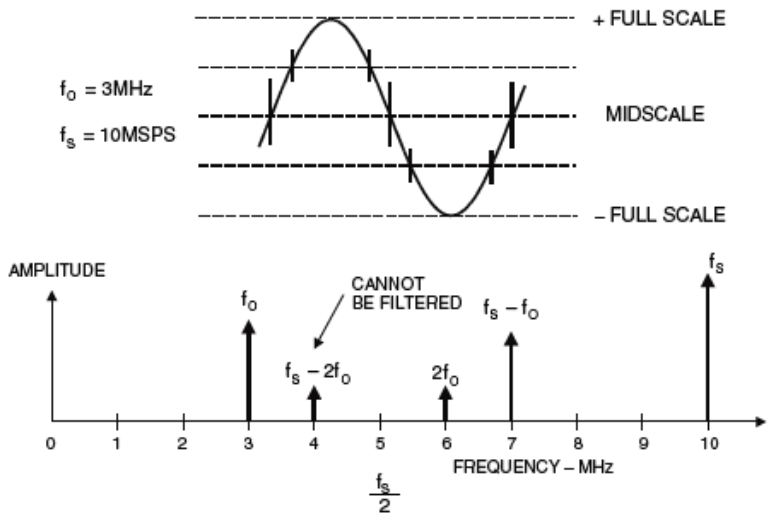


Figure 3.15: code dependent glitches and harmonic spurs

- Timing Mismatch: Relative timing imprecision (skew) and spread of the waveform characteristics of the individual current pulses caused by clock skew, process mismatch in latches, drivers and switches, unequal loading or interconnect lengths, the timing jitter in the clock network.

- Noises: The possible noises sources are cross-talk, substrate noise, ground bounce, power supply noise, and device noise.

Note that what has been discussed here is sinusoidal linearity. The ongoing trend of wide-band high-speed DAC design is to employ DACs in the radio systems to process broadband signals and modulation schemes(e.g. for QAM or similar modulation schemes). The signal handled by DACs are more complicated than just a single sinusoidal tone. This implies that the knowledge developed to design DACs with better sinusoidal linearity may be less relevant to design DACs for these wideband or complicated modulated signals. Therefore the knowledge of the dynamic behavior of this circuit has to be related to more generic or more complicated signal properties such as correlation, power, probability distributions, etc. from the beginning of any analysis based on certain system-level, or application-specific assumptions. It needs new innovations and circuit techniques to maintain a wide range of high SFDR at the DAC output up to the Nyquist frequency or even higher Nyquist zones.

### 3.5.4 Timing Accuracy

Timing accuracy is one of the dominant factors that affects the DAC performances. The undesired variations of the clock signal period over time is usually referred as clock jitter or timing jitter. The sources of timing variations are from the circuits that generate and process time-reference signals, such as oscillators, PLLs, or clock buffers, etc. In a DAC, timing jitter can originate either from an off-chip clock reference or due to the noise generated by the noise in the clock buffers and the interference coupled from biasing, substrate or power supply nodes. These signals influence the performance of data converters significantly.

Signal-to-Distortion ratio (SDR) is a commonly-used measure for the effect of timing jitter on DAC. The impact of timing jitter on SDR can be expressed by the equation below:

$$SDR(dB) = 3.01(N-1) - 10\log_{10}(\sigma^2 f_{in} f_s) - 9.03 \tag{3.11}$$

where N is the number of bits and $\sigma$ is the RMS jitter. As shown in Figure 3.16, we have to manage the jitter down to around 4ps level to achieve 60 dB SDR performance. The SDR curve is -20dB/dec with the RMS jitter.

As suggested in [41], the timing error can be translated into a Pulse Width Modulation process, which links with the branch of sampling and interpolation theory in non-uniform timing effects.

The effect of non-ideal clock on system performance can be analyzed or measured. In the frequency domain analysis, phase noise in oscillators and clocks becomes one of the limiting degradations in modern radio systems.

The effects of phase noise on sampled data systems, wideband systems, or digital radios are well addressed and discussed with issues related to phase noise in [42].

$$SNR_{sig} = SNR_{clk}(\frac{f_{clk}}{f_{sig}})^2 \tag{3.12}$$

As the signal frequency gets higher, the SNR degrades in a 20 log fashion. This illustrates the reason why sub-sampling systems require clocks with much better phase jitter than baseband systems. In those systems, the signal frequency occupies one of the higher Nyquist zones. However, DACs exhibit different characteristics due to the inherent SINC function. These are clearly seen at each of the output images. Relative to full scale, the spur amplitudes remain constant. When viewed in dBc, as the signal frequency goes up, the modulation spurs get worse in the same manner as described in the following equations. The SINC function applies to both the signal amplitude and the induced clock phase noise.

The SINC function is defined as

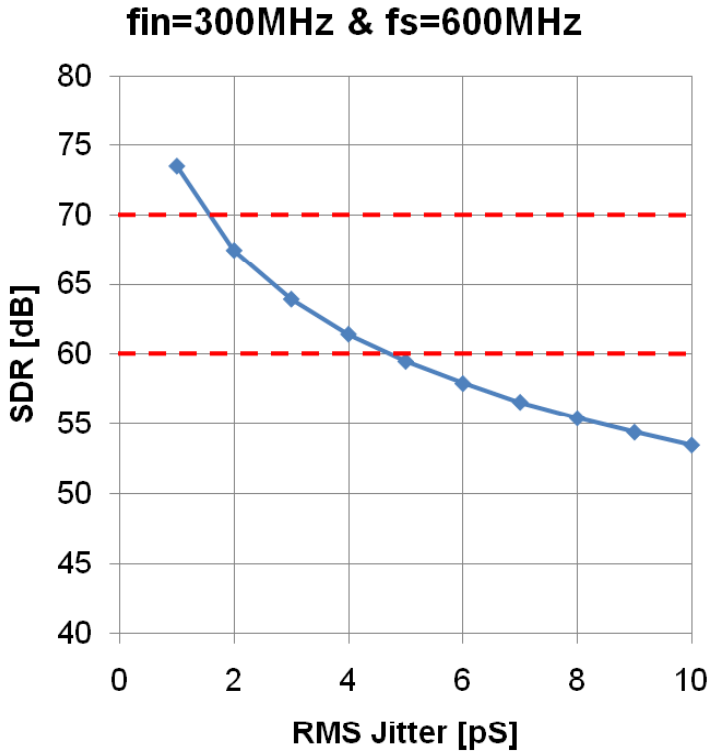


Figure 3.16: SDR versus RMS jitter

$$SINC = \frac{sin(\frac{\pi f_{sig}}{f_{clk}})}{\frac{\pi f_{sig}}{f_{clk}}} \tag{3.13}$$

The noise and signal can be expressed as

$$\frac{N}{S} = {\sigma_\theta}^2(\frac{f_{sig}}{f_{clk}})^2 \tag{3.14}$$

The noise is directly proportional to the clock phase noise and signal frequency. Then, squaring the SINC function (because power spectral densities are being examined) and multiplying these two to get a composite noise transfer function out of the DAC yields

$$\frac{N}{S} = {\sigma_\theta}^2\frac{sin(\frac{\pi f_{sig}}{f_{clk}})^2}{\pi^2} \tag{3.15}$$

The periodic nulls caused by the sinusoid still exist. However, the denominator of the SINC function is what causes the roll-off at higher frequencies. This attenuation has been

exactly canceled by the increasing phase noise at higher frequencies described the above equation. This leads to an important conclusion: the phase noise out of a DAC will not grow at higher frequencies. In our sub-Nyquist rate conversion, this helps us understand the impact of phase jitter when utilizing the image spectrum in higher Nyquist zones.

### 3.5.5 Speed and Settling Time

DAC settling time is important in applications such as RGB raster scan video display drivers, but frequency-domain specifications such as SFDR are generally more important in communications. This is a relatively high-speed digital-to-analog converter and the driving capability of output currents is needed. The estimated loading includes the parasitic loading from pads and off-chip PCB components. As a first-order estimation, the amount of current necessary to charge this capacitor fast enough, the standard formula for charging a capacitor is used for calculating the required currents. Assuming the worst-case single-end swing is $\Delta V_{swing}$ and the sampling period is $\Delta T_s$ , an rough calculation of the required current is:

$$\begin{aligned} I &= C_{load} * \frac{\Delta V_{swing}}{\Delta T_s} \\ &= C_{load} * \frac{\Delta V_{swing}}{\frac{1}{F_s}} \\ &= C_{load} * \Delta V_{swing} * F_s \end{aligned} \tag{3.16}$$

### 3.5.6 Power

It is crucial for any transceiver ICs designed for cognitive radio applications to be extremely low power. The power consumption in a CMOS current-steering DAC can be divided into three categories. The first part is analog in nature and independent of the sampling frequency. The full-scale output current is the major portion of the current in the analog supply. The dominant source of power consumption in high-speed current steering DAC is the array of current sources. Since the design is differential, each element consumes a constant amount of currents. The power consumption is simply the product of the total current by the supply voltage.

$$P_{CS} = (2^N - 1) * I_{uint} * V_{DDa} \tag{3.17}$$

where N is the number of bits of the DAC. A popular output current for previous designs

was 20 mA because it provided 1-V signal swings in 50ohm systems. An obvious place to reduce power is to lower the full-scale current. The nominal output current is lowered to 10 mA in this test case and can range from 8 mA to 12 mA. Note that there is overhead power consumption coming from the bandgap reference and various bias circuits. Inclusion of these bias circuits can have a significant effect on the spurious performance of the DAC.

The second part comes from the digital logics and the clock section and directly scales with the sample frequency and the data activity. CMOS has the advantage that the power consumed will benefit from advances in process and supply voltage scaling. The power consumption of the digital portion includes the thermometer-code decoder, latches and the local decoding logics embedded in the current switch array. It can be estimated by the following equations:

$$P_{digital} = C_{digital} V_{DDd}^2 f_s \tag{3.18}$$

The third part comes from the clock generation and clock distribution network.

$$P_{clock} = C_{clk} V_{DDd}^2 f_s \tag{3.19}$$

The total power

$$\begin{aligned} P_{total} &= P_{CS} + P_{digital} + P_{clock} \\ &= (2^N - 1) * I_{uint} * V_{DDa} + (C_{digital} + C_{clk}) V_{DDd}^2 f_s \end{aligned} \tag{3.20}$$

### 3.5.7 Summary of Specifications

The specifications of this DAC is summarized in Table 3.1.

Table 3.1: Summary of design specifications

| | |
|---|---|
| **Resolution** | 10bits |
| **Sampling Rate** | 600MSps |
| **Full-Scale Current** | 10mA |
| **Technology** | LP/GP 65nm CMOS process |
| **Output Swing** | 0.5V (single-ended) / 1V (differential) |
| **Supply Voltage** | 1.0V (PLL/Digital part)<br>1.2V (Current Switch) |
| **DNL** | < 0.5 LSB |
| **INL** | < 0.5 LSB |
| **SFDR** | > 60 dB across multiple Nyquist zones |
| **IM3** | > 60 dB |

# Chapter 4

# Experimental Prototype

In this chapter, a prototype circuit of the sub-Nyquist rate DAC is presented. Design parameters and the effect of circuit non-idealities derived from chapter 3 are used as a starting point for the circuit design. There are many challenges throughout the design process, including the matching requirements, investigating the floorplan and the SNR versus power tradeoff [41] [43]. Digital-to-analog converters can be built using different topologies with various strengths and weakness in terms of integral non-linearity, differential non-linearity, chip area, settling time, and matching. A 65nm CMOS test chip has been designed and manufactured for demonstrating the important concepts for the multi-mode sub-Nyquist rate conversion. The measurement results are presented towards the end of this chapter.

## 4.1 Circuit Design

### 4.1.1 DAC Architecture and Segmentation

The test-chip prototype consists of a low power 10bit, 600MS/s multi-mode DAC and clock generation circuits for TV band cognitive radio transmitters. The top-level block diagram is shown in Figure 4.1. All functional blocks, except the output transformer, are integrated on the same chip.

As mentioned in the previous chapter, the current-steering architecture is the most common used for high-speed DAC design. The thermometer/binary partitioning is one of the most important architectural issues in the design phase. The segmentation choice of segmen-

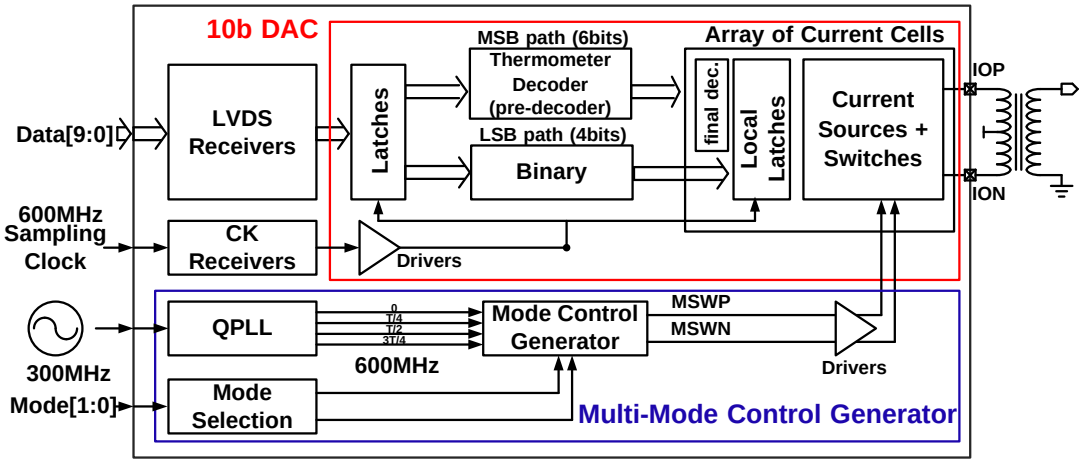


Figure 4.1: The block diagram

tation is based on MSB/LSB glitches, timing precision requirements, switching noise from digital logic, as well as speed-area-power tradeoffs. The DAC is implemented as a 10-bit segmented current-steering DAC. The main DAC is segmented into a 6-bit thermometer-coded MSB array and a 4-bit binary-weighted LSB array.

The output currents from the MSB array and LSB array are tied together to generate differential output currents, $I_{OP}$ and $I_{ON}$. The MSB array comprises 63 identical current cells. Each current cell is designed to output a nominal current of 16x $I_{unit}$, where $I_{unit}$ is the DAC unit current. The LSB array comprises 4 current cells which output a current of 1x $I_{unit}$, 2x $I_{unit}$, 4x $I_{unit}$, and 8x $I_{unit}$, respectively. In this design, the nominal $I_{unit}$ is 10uA and the output currents $I_{OP}$ and $I_{ON}$ drive 50 ohm impedance from the transformer and yield 1 V differential signal swing at $V_{op,on}$.

### 4.1.2 Sizing and Matching of Current Source Array

There are several constraints that affect the minimum value of the reference current, including matching requirements, signal-to-noise ratio, and speed considerations. Transistor mismatch in the current source array of the DAC is the dominant source of nonlinearity and low frequency performance.

As mentioned in the previous section, this 10-bit DAC is segmented as 4-bit LSB in

binary and 6-bit MSB in thermometer-coded. The variation of unit current can be expressed as

$$\sigma_\varepsilon = \sigma(\frac{\Delta I_d}{I_d}) \tag{4.1}$$

The worst-case INL can be formulated as

$$INL = 2^{\frac{B}{2}-1}\sigma_\varepsilon = 16\sigma_\varepsilon \tag{4.2}$$

Where B is the number of total bits. Since the INL spec is $INL \leq 0.5LSB$, we can find $\sigma_\varepsilon \leq \frac{0.5}{16} = 3.125\%$

Similarly, the worst-case DNL can be expressed as

$$DNL = 2^{\frac{B_{LSB}}{2}-1}\sigma_\varepsilon = 5.6\sigma_\varepsilon \tag{4.3}$$

Where $B_{LSB}$ is the number of LSB bits. Since the DNL spec is $DNL \leq 0.5LSB$, we can find $\sigma_\varepsilon \leq \frac{0.5}{16} = 8.93\%$

Clearly, the INL spec is the dominant factor of the matching requirement. To meet the INL yield requirement of 99.7%, this translates that the target $\sigma_\varepsilon$ should be one third of the $\sigma_\varepsilon$ derived from the INL requirement. That means

$$\sigma_\varepsilon = \frac{3.125\%}{3} = 1.042\% \tag{4.4}$$

Based on the above $\sigma_\varepsilon$ and the variation parameters from 65nm CMOS process, the required minimum area of the unit current source can be determined to meet the 1% static matching requirement. As defined in Pelgrom's paper [44], mismatch is the process that causes time-independent random variation in physical quantities of identically designed devices. Essentially, this means that each unit current source in the array generates a current that varies slightly from the desired unit current, $I_{unit}$. Therefore, the current sources have to be designed in such a way that random variations do not degraded the static linearity of the DAC below its specifications. The mismatch of two identical MOS current sources can be modeled by the differences of their threshold voltages $V_{T0}$ and the current factors $\beta$.

The standard deviation of the saturation current of two identically-sized transistors is described by the following formula:

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{T0})}{(V_{GS}-V_{T0})^2} + \frac{\sigma^2(\beta)}{\beta^2} \tag{4.5}$$

where

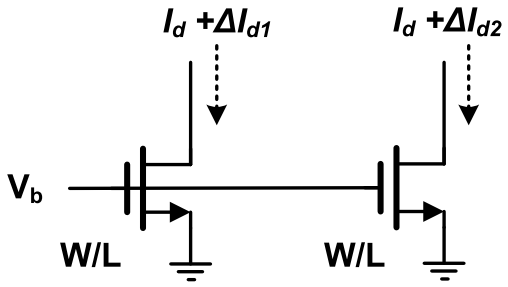


Figure 4.2: Mismatch between two MOS current sources

$$\sigma^2(V_{T0}) = \frac{A^2_{V_{T0}}}{WL} + S^2_{V_{T0}} D^2 \tag{4.6}$$

and

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{{A_\beta}^2}{WL} + S^2_\beta D^2 \tag{4.7}$$

Note that $A_\beta$, $S_\beta$, $A_{V_{T0}}$, and $S_{V_{T0}}$ are process parameters. $D$ is the distance between the two transistors. $W$ and $L$ are their geometrical dimensions. Using these equations, an equation for the minimum size device that provides a reasonable current standard deviation can be determined.

$$WL_{min} = \frac{1}{2}[A^2_\beta + \frac{4\sigma^2(V_{T0})}{(V_{GS} - V_{T0})^2}]\frac{\sigma^2(I_d)}{I^2_d} \tag{4.8}$$

In Pelgrom's equation for $W \times L$ area constraint, most of those parameters in the above equations are process-dependent. The single cascode configuration was selected at this design as shown in Figure 4.3. For this design, high performance analog(HPA) device is used for MS1 to have better matching and higher $R_{out}$. The dimensions of unit current source are given as 8um in gate-length and 3um in gate-width.

In the literature, various techniques have been proposed to improve matching between current sources, such as Dynamic Element Matching (DEM) [45], or calibration techniques [46]. Many papers show that those techniques indeed improve the linearity of the DAC at low frequencies. However, at high frequencies those techniques usually do not help very much and could possibly even degrade the performance, because both techniques can cause extra tones in the output spectrum and complicate the layout design significantly. To design for high frequency performance, simplicity in design/layout and low parasitic capacitances

will bring the most benefits. So in this work we adopted this strategy in the design without introducing any complicated matching techniques in this work other than proper transistor sizing.

Since the DC current of MS1 is fixed and the width/length of MS1 is fixed by the matching considerations, the remaining design freedom left for MS1 is its drain voltage. $VD_1$ is pushed down to 0.2V to free the voltage headroom for the cascode and the switching transistors. This value takes into account for remaining glitches as well. The capacitances were minimized by the iteration of circuit and layout design.

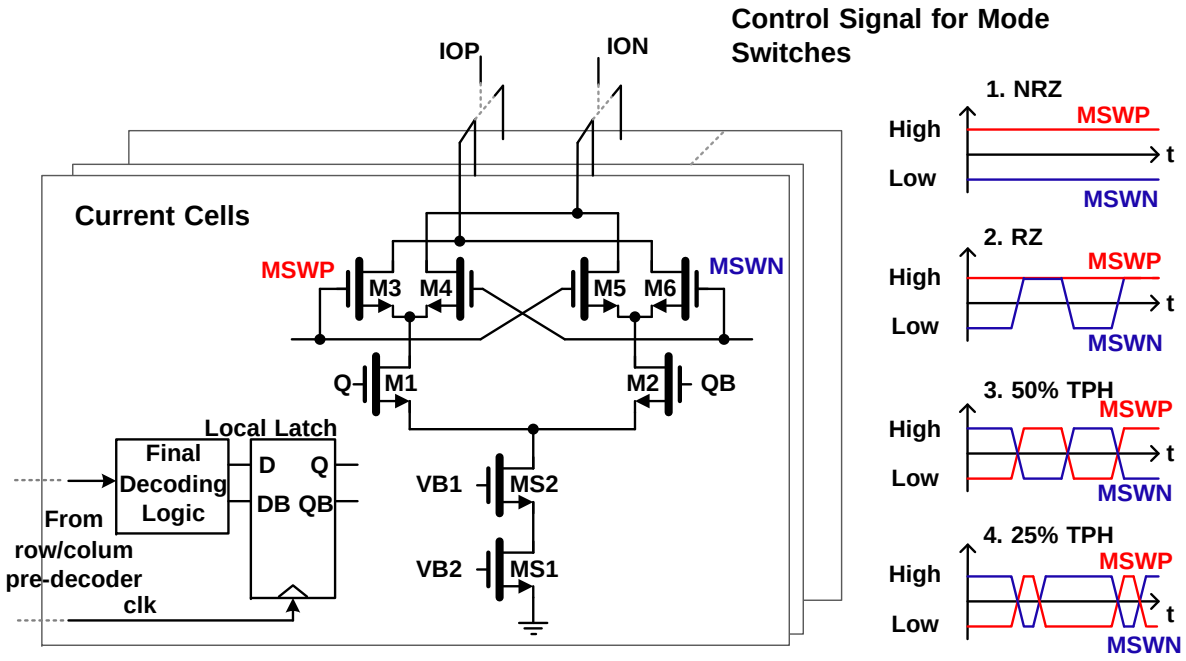


Figure 4.3: Schematics of current cells with mode control signals

A small MS2 size was used to reduce capacitances. The voltage $VD_2$ was set to $VD_2 =$ 0.35V and the dimensions to L = 0.28um, and W = 0.42um for the length and width of the LSB, respectively.

### 4.1.3 Switch Cells

The design of the switch cells addresses charge feedthrough phenomena, spikes and signal dependent modulation of the switch common source node, and local timing errors. The critical design parameters for the switch are its width and length dimensions, as well as its control signals including slope, swing and the actual transient shape.

A large size of the switches has a detrimental impact on the local timing errors caused by the switches, assuming all circuits preceding them have a fixed power budget. The switch size is the central point of the design-for-timing strategy for random timing errors. Since the capacitive loading of the switch gate has a stronger contribution to timing errors than switch mismatch, the smaller the switch transistors are (smaller area, thus gate capacitance), the smaller the timing errors will be for all circuits preceding the switches (chain effect) given a fixed power budget.

The multi-mode operation is realized by the cascaded output butterfly switches and the control signals, MSWP and MSWN, from multi-mode control generator. The schematics of current cells with mode control signals are shown in Figure 4.3.

In NRZ mode, where MSWP is high and MSWN is low, the DAC output currents ($I_{OP}$ and $I_{ON}$) are switched by the input data (Q and QB) as a conventional DAC. In RZ mode, the DAC output is reset by turning MSWP and MSWN high simultaneously in the reset phase. In TPH mode, the DAC output alternates between positive and negative values with the fully differential MSWP and MSWN applied on the butterfly switches. The period of the inverted phase is controlled by the duty cycle of MSWP and MSWN. The operation mode can be reconfigured in real-time by changing the selection signals, Mode[1:0]. Depending on the synthesis requirements, NRZ, RZ, or TPH mode can be applied for reconstruction. The target signal for transmission is synthesized in either the fundamental from the first Nyquist zone or image spectrum over higher Nyquist zones.

### 4.1.4 High-Speed Thermometer Decoder and Latches

In DAC design and floorplan, the rule of thumb is to keep the structure regular. For 6-bit binary-to-thermometer decoder, there are 63 outputs wires to be routed to current switch array. The routing of those digital wires will be a big burden in the layout and floorplan. In this work, a two-step decoding strategy is adopted to keep regular routing structure while achieving low wiring complexity and good timing error management.

As shown in Figure 4.4, the two step decoding consists of 3-to-7 row/column pre-decoder

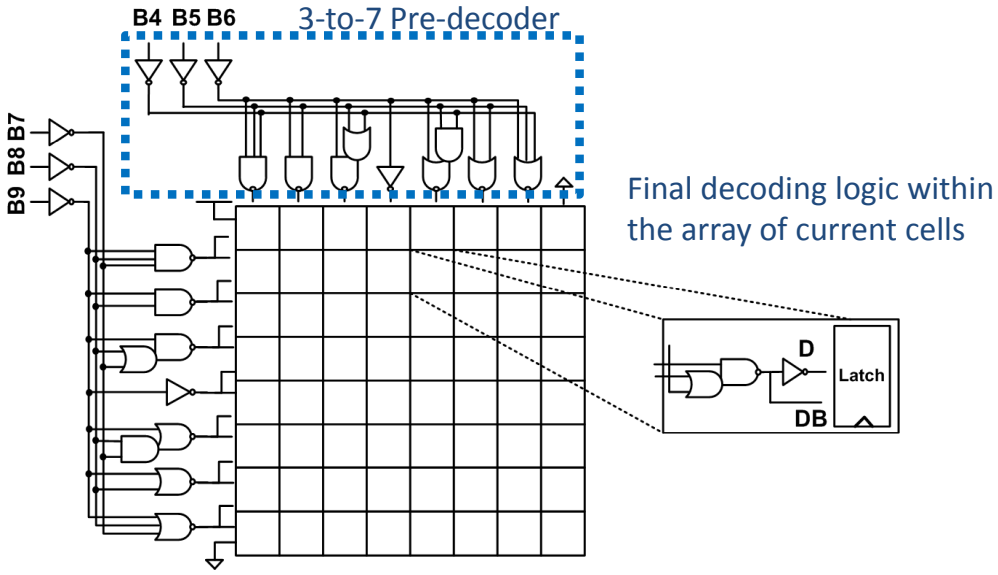


Figure 4.4: Binary-to-thermometer code decoder

and simple final decoding logic inside the switch cell array. The regular routing structure was kept whereas only 7 lines routed vertically and 14 lines horizontally. Inside each switch cell, we have the same final decoding logic, which takes one signal from column decoder outputs and two signals from row decoder outputs. The regular structure is good for managing the timing/skew issues on those routing and logic structure. This helps to make our life easier and have less coupling from those digital lines.

CML drivers are often used to obtain maximum possible clock speed because of the reduced swing. However, the steepest transitions are obtained using regular CMOS logic. In this design, the latch of Figure 4.5 is used. The differential output signals for driving the switch cells are optimized to have a high-crossing point. This design reduces the glitches in the common source node of the switch cells during the switching transients. Since any spread in switching moment is proportional to the switching time, the absolute transition of the driving signal for the switch cells should be as fast as possible. Both good matching and a fast transition result in a fairly large size of the driver transistors. The sizing of the decoding logic, the latch and the driver is optimized as a tapered chain. The thermometer decoder and digital blocks are manually designed in standard 1V CMOS logic.

The static performance of a current steering DAC is limited by random and systematic errors. The former are caused by device mismatches and can only be palliated by increas-

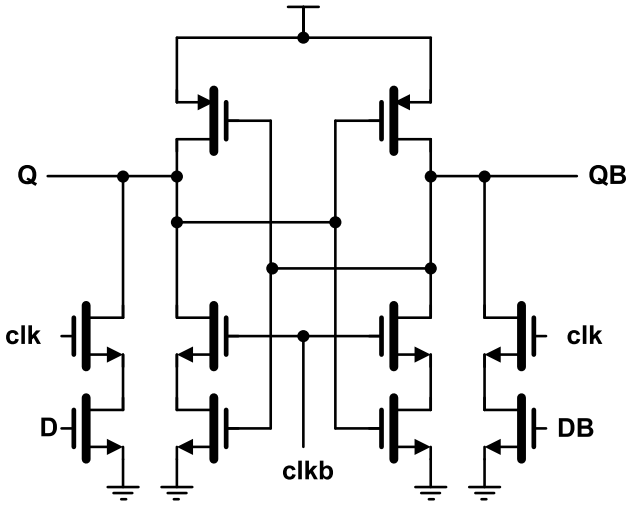


Figure 4.5: The schematic of the latch inside switch cells

ing the active area of each current cell. The latter came from thermal gradients, CMOS technology-related error components (doping gradients, oxide thickness gradients, etc...), edge effects, etc. Dynamic Element Matching (DEM) is commonly used to mitigate random and systematic variations [19]. Conventional DEM implementation is very complicated due to massive digital signal routing for distributing the randomized results [45]. For example, a 6-bit binary-to-thermometer decoder has to generate 63 scrambled decoder outputs every cycle for driving the switch cells. Those routing wires have to go into the switch cell array and result in extra area overhead and the penalty of additional parasitics.

In order to reduce the complexity, a simplified method is used in this two-step decoding design to scramble the mapping of thermometer-coded units. The outputs of row and column 3-to-7 pre-decoders are scrambled, so that the mapping of thermometer cells are randomized as shown in Figure 4.6.

This can be further extended to be a low complexity "psuedo-DEM" by only dynamically re-arranging the 3-to-7 pre-decoder. This method can greatly save the effort of handling the signal routing of DEM because the dynamic randomization process only need to be implemented in the row/column decoder, which scrambles only 7 outputs of each decoder on the fly. The signal routing for the decoder output are still regular inside the switch cell array.

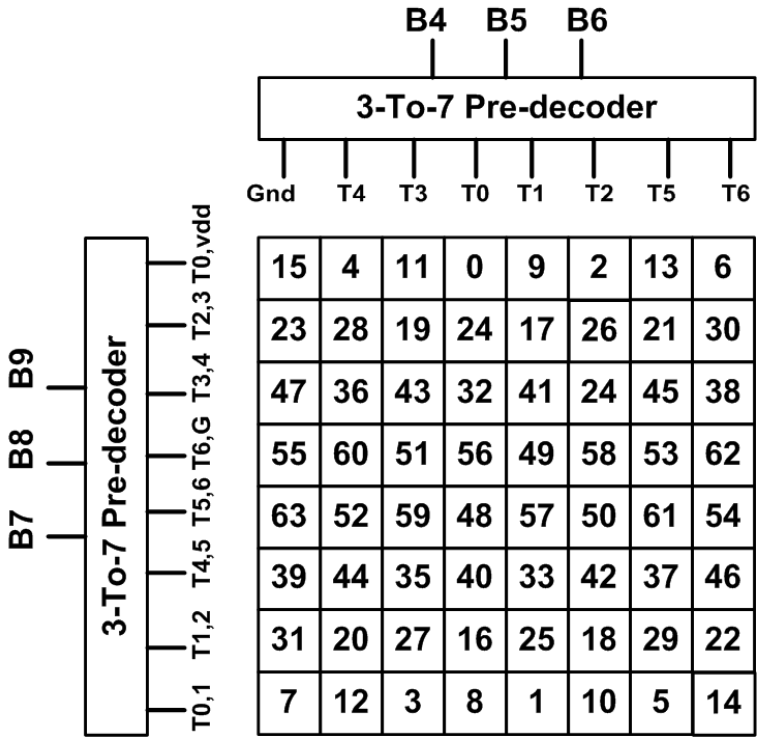


Figure 4.6: Scrambled mapping of the unary array

### 4.1.5 Multi-Mode Control and Variable Duty-Cycled Clock

The multi-mode control generator provides the control signal, MSWP and MSWN. This block can produce seamless transition between different modes. There are no glitches between mode transitions. The clock source can be chosen either from an on-chip QPLL or directly from external clock sources or signal generator as a backup solution. For the purpose of debugging, we can bypass the QPLL and use the external clock for generating multi-duty cycle clock. The low-jitter low-power QPLL is designed by my colleague, Nam-Seog Kim. The details of this QPLL are skipped here.

### 4.1.6 Floorplan and Layout

The DAC floorplan is very crucial for the implementation of high-speed DACs. The floorplan is shown in Figure 4.9. In this design, the four binary cells (1x, 2x, 4x, and 8x) are placed in the center of the array. The thermometer-coded cells (16x) surround the center

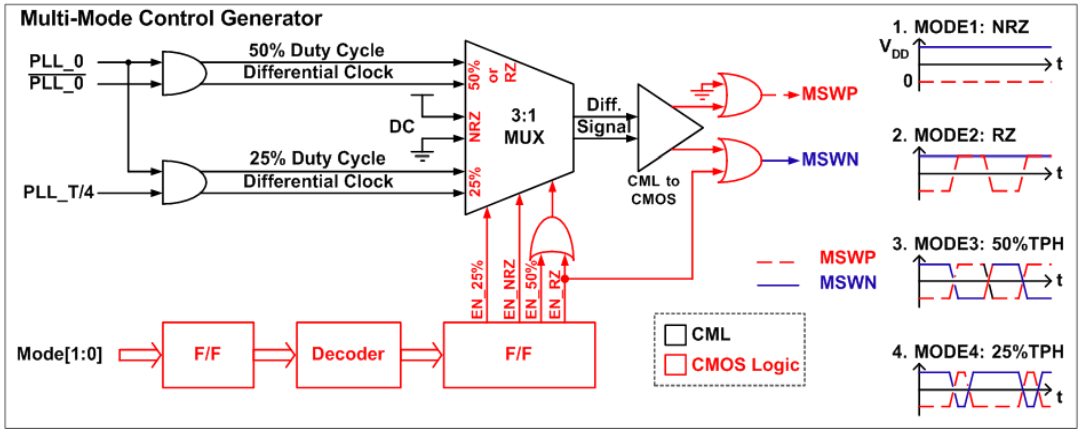


Figure 4.7: The circuitry of clock and multi-mode control signal generation

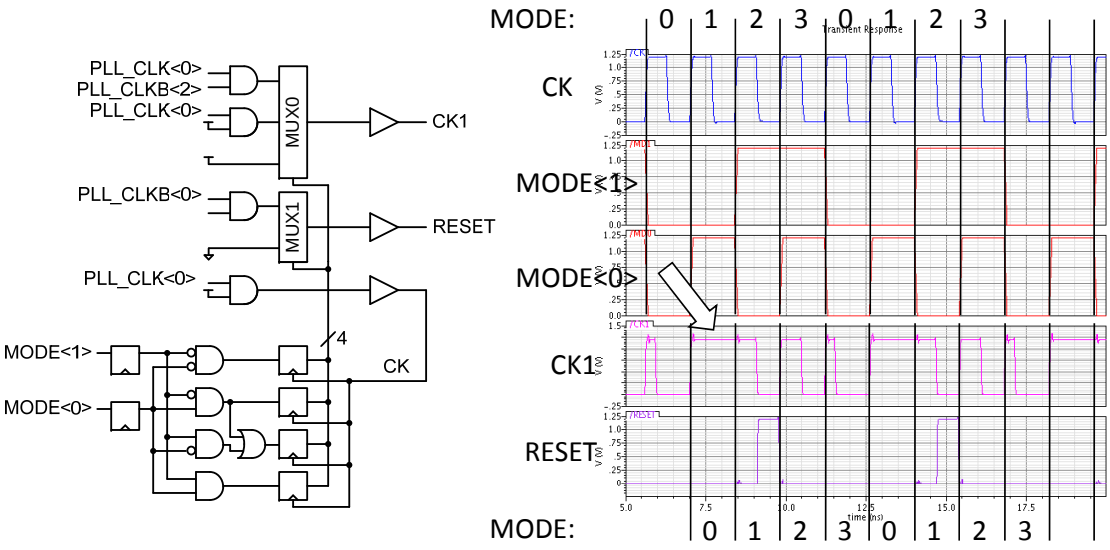


Figure 4.8: Transition of modes

of binary cells. The layout strategy is to design the template of 16x SW and CS cell first. And binary cells (1x, 2x, 4x, and 8x) are modified based on the 16x cell template. To have a better matching between biasing cells and SW/CS cells, the biasing cells here are also designed by reusing the same 16x cell template. The biasing cells are placed on both the left and right side of the array. The outer part is surrounded by the dummy cells. The use

of dummy cells create an equal environment for the cells inside the switch array and current source array.

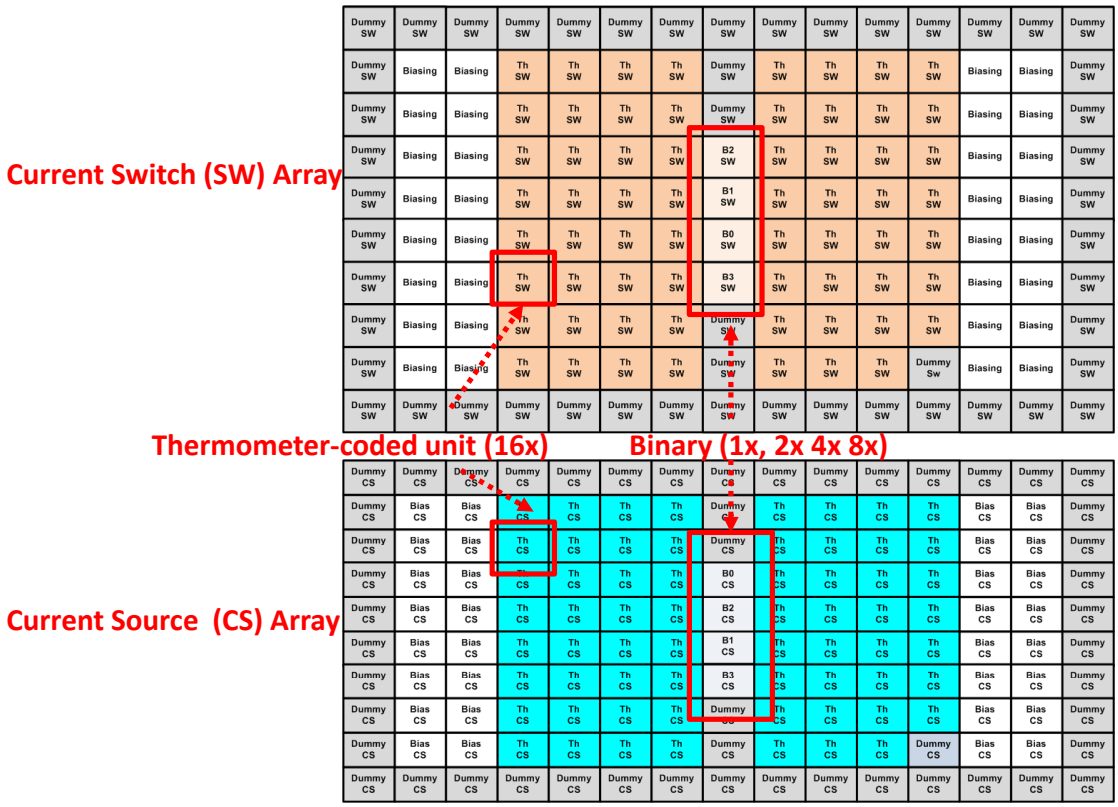


Figure 4.9: DAC floorplan

The CS and SW units are further divided into subunits for common-centroid layout. This helps to have better matching while reducing deterministic error. A 16x CS unit is divided into four 4x sub-units. A 16x SW unit is divided into two 8x sub-units. Partitioning of each current source transistor in four subunits connected in parallel, placed in four separate arrays, and biased locally to reduce deterministic errors. The SW unit was not further divided into 4x SW for 2D common centroid because this will introduce more overhead in pre-decode routing.

The most critical issue under this design is the timing error of the clock that drives the final latches. The clock skews under the worst-case scenario are mitigated by the technique of averaging as shown in the Figure 4.10. Also, it is crucial to design the whole signal paths from the digital code driving the switching cells to the output current summing nodes as well matched as possible. A symmetrical tree structure for output current routing is used in

an effort to keep all possible delays in the signal path the same. This part has been carefully investigated by post-layout RC extraction and simulation. Also the same technique is applied to mitigate the skew from the summing network of the output currents.

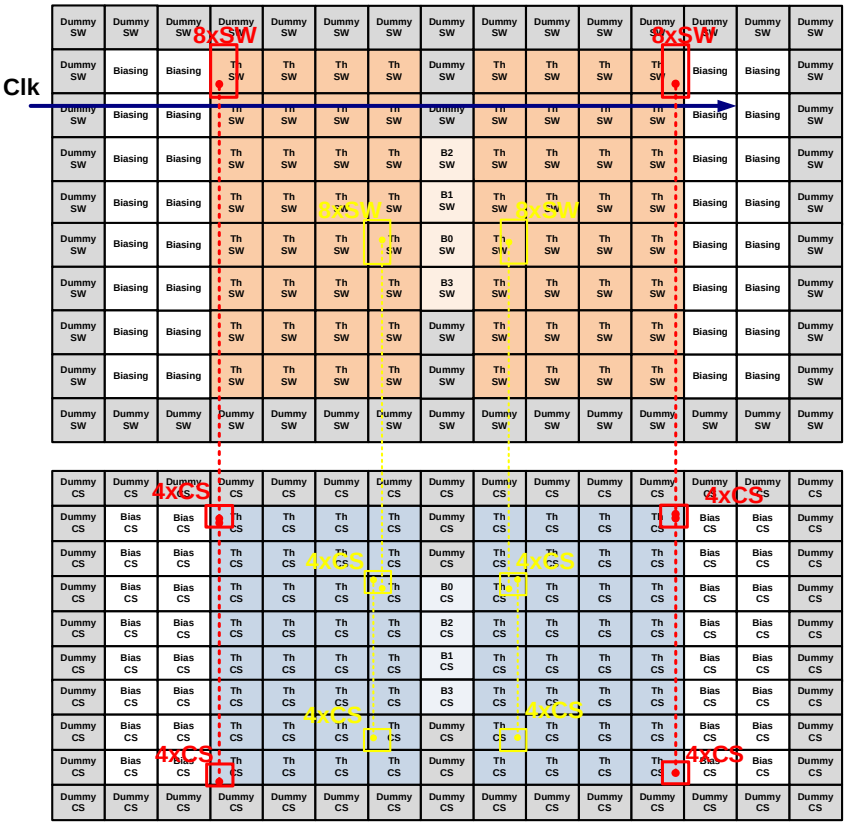


Figure 4.10: 2D common centroid floorplan

Layout design plays a crucial role in the performance of the converter. A lot of attention has been paid in realizing a well-structured layout of cells. There are two main goals for the layout: a square form factor, so the array can be tiled easily; and a smaller area, so the parasitics from layout will be minimized and won't degrade the dynamic performance. The layout of the current sources array and switch array was done carefully. To optimize the layout, we also iterate the design based on post-layout simulation results.

The final DAC core Layout is shown in Figure 4.11. The core area is about 300um by 350um. The main blocks are the SW array, the CS array and the row/column decoder. The differential output currents are summed up in the top. After putting together all the blocks,

it is not feasible to simulate a full DAC with post-layout extraction due to the complexity of the netlist with extracted RC parasitics. Instead, PL extraction and simulation are carefully done for critical signal paths and sensitive parts of the design, such as the decoder path and output current summing skew.

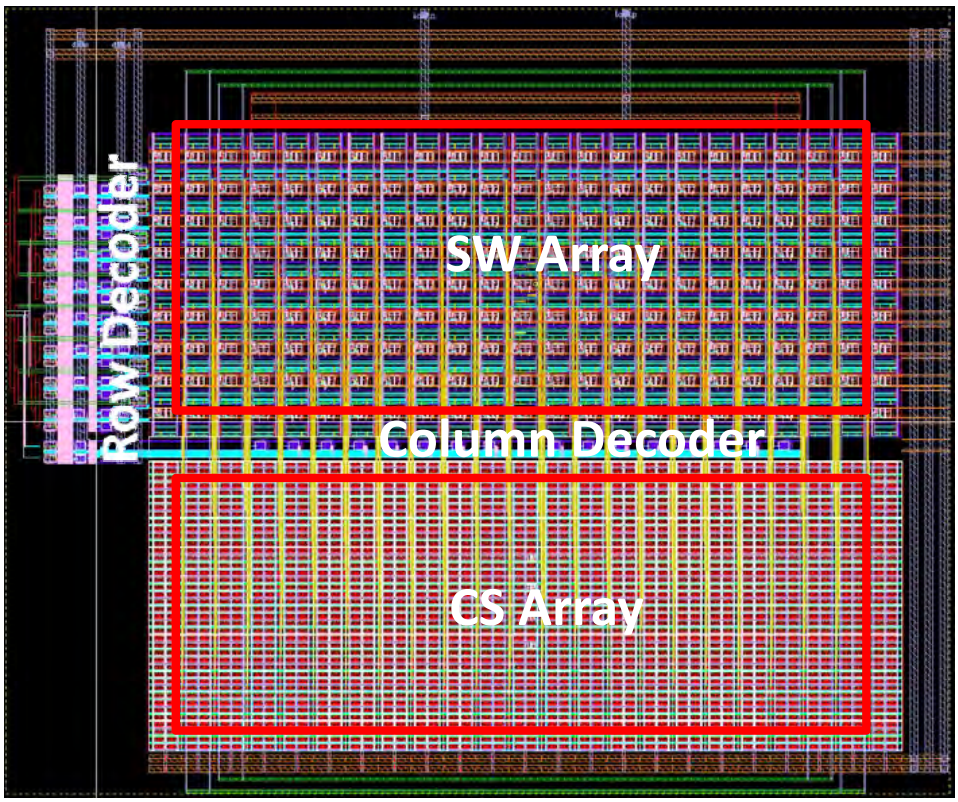


Figure 4.11: DAC core layout

### 4.1.7 Peripheral and Bias Circuitry

The current source transistor and its cascoded transistor are biased to be produced the desired output current. For this purpose, a high-swing bias circuit was used. The circuit used a precise tunable reference current from an off-chip current source IC. As shown in Figure 4.9, the biasing cell is designed by reusing the same switch cells and current sources. With the slight modification of switch cells and current sources, the biasing cells look similar to the original 16x tile of switch cells and current sources. Those biasing cells are placed on

the left and right side of the SW array and CS array.

Separate supplies and biasing for the clock buffers, the decoder and local synchronization latches, drivers, and current source array are used to prevent the circuit blocks from the coupling of switching noise and interferences via the biasing/supply lines. Local decoupling capacitances were distributed inside the switch array, current sources array and other vacant areas near the core circuit blocks. Those distributed decoupling capacitances serve as the local pools of charges to allow a portion of the switching charges required by switching circuits to be drawn by them instead of the external power supply via inductive leads.

As the supply lines carry current, any resistance will cause voltage drop on the supply line, which in turn can cause the mismatch between the individual gate-source voltages of the current source transistors. As a result, the value of the currents will be affected by the IR drop along the supply line, causing not only DNL problems, but also INL problems when no randomization technique was applied in the array. In this work, the routing of the supply lines for the DAC current sources is carefully designed by using wide power supply lines and binary trees for the supply grid. Multiple of DC pads per supplies were used to reduce the bonding wire inductance interfacing the on-chip to the off-chip supplies.

## 4.2 Test-Chip Prototype

The prototype DAC was fabricated in a 1.2V general-purpose 65nm seven-metal one poly digital CMOS process. The chip microphotograph is shown in Figure 4.12. The total chip size measures 2.2mm by 1.4mm, while each DAC occupies only 300um by 350um. There are two DACs on the top left and middle, which is connected to clock generation circuitry located in the bottom left. Ten pairs of LVDS receiver pads are in the bottom of the pad ring. One standalone DAC and clock generation circuitry are located on the left side.

A standard 6-layer FR4 Printed Circuit Board (PCB) was designed for chip testing and the prototype demonstration. Instead of using a conventional package for the chip, the chip-on-board technology is used here in order to reduce parasitics and facilitate testing. The prototype PCB was designed to guarantee the delivery of 10 bit parallel high speed data and the signal integrity of the critical analog outputs and clock signals (Figure 4.13). RF components and analog traces are very sensitive to noise from power supplies and digital blocks. The power supplies are carefully divided into different domains: digital power, analog power, LVDS power and DAC analog power. Each power domain has its own power plane on PCB and on-board regulator modules. The 6-layer PCB provides enough freedom in the

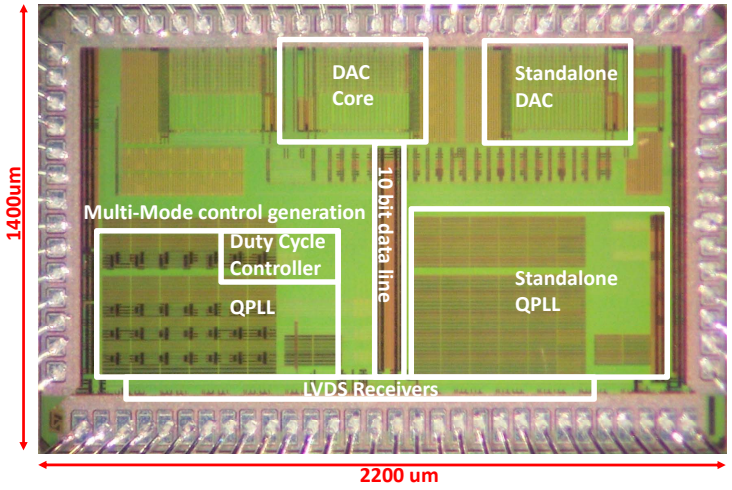


Figure 4.12: Chip microphotograph

power plane and traces allocation. The critical clock and analog traces are routed with 50 ohm impedance control, which provides precise transmission line characteristics. The supply voltages for clock receivers and PLL and DAC are generated on the test board; each with a dedicated voltage regulator. Although, the PCB played an important role on the quality of the measurements of high-speed converters, most details of this PCB design are omitted here.

## 4.3 Measurement Results

### 4.3.1 Measurement Setup

Figure 4.14 shows the measurement setup. An Agilent 81134A pulse generator is used to provide two pairs of differential clock signals for the test chip. A custom design data generation system on the FPGA board provides 10-bit high speed test patterns to the DAC. The internally-developed FPGA boards, IBOB (Interconnect Breakout Board) and ROACH (Reconfigurable Open Architecture Computing Hardware), and design flows at BWRC are used to quickly make the prototype digital blocks down to the reconfigurable fabric or even synthesized the layout going to the silicon implementation. These FPGA boards here are programmed to equivalently serve as an logic analyzer that can be attached to the chip test

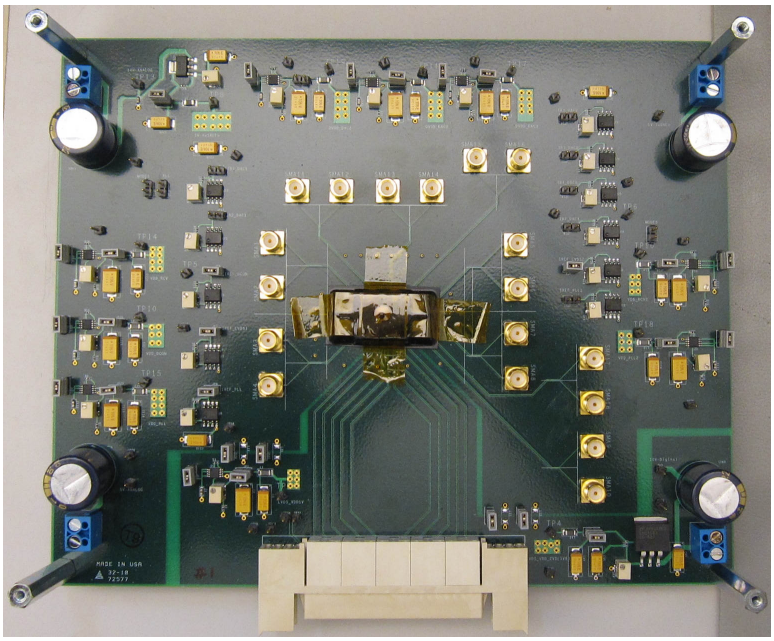

Figure 4.13: Prototype printed circuit board

board through the Z-Dok connector.

The IBOB and ROACH can be programmed in the same way as the BEE2 system with the Simulink-based design entry. The IBOB hosts a Xilinx Virtex II Pro XC2VP50 FPGA [47], which contains two PowerPC microprocessors on-chip. Registers and block RAMs in the FPGA can be address-mapped and accessed through the PowerPC microprocessor. In the simplest setup, the registers can be programmed on the FPGA to connect to the corresponding Z-Dok pins. A subsequent write operation (to the register) functions as an input to the chip under test and a read operation (from the register) functions as an output from the chip under test. This simplest form is used in automated testing, where the control signals and waveform configurations (frequency control word, mode selection, start, stop, and reset) are set via the PowerPC microprocessor. So the waveform generation can be controlled dynamically by setting the corresponding registers.

The input clock signals are generated from Agilent 81134A pulse generator, where two pairs of clock signals directly drive the test chip, and another single-end one is routed from the trigger-out port to drive the IBOB. So the on-chip clock and the IBOB clock are provided by the same external clock source. In addition, the phase of the IBOB clock can be tuned in 90 degree increments for phase alignment. From IBOB or ROACH, the synthesized sinusoidal waveforms are generated by DDFS-based logics and can be controlled by the respective

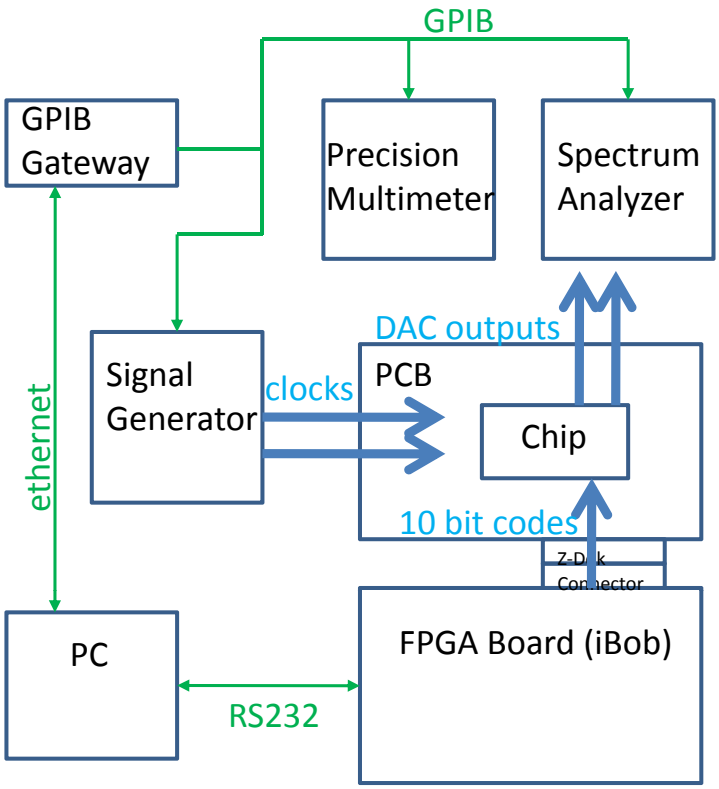


Figure 4.14: Measurement setup

registers on the FPGA. In a more elaborate testing scheme, the FPGA is programmed to generate various modulated waveforms. Therefore, a flexible waveform generator can be implemented on the FPGA, which runs concurrently with the sub-Nyquist rate DAC chip.

All the test setups are controlled by the Matlab scripts from the laptop. The automated process speeds up the measurement controlled by GPIB bus over the instruments.

### 4.3.2 DC Linearity Measurements

The static performance is characterized through DNL and INL measurement. A daughter board with precisely matched resistors is used for DC linearity measurement (Figure 4.15). The FPGA board, IBOB, generates the 10 bit digital codes sweeping from "0000000000" to "1111111111", and the precision multi-meter measures the DC currents and voltages at the output nodes. The measured currents are then used to evaluate the INL and the DNL of

the converter. To reduce the impact of noise from the measurement, each output current that corresponds to an input code was measured 10 times, and then the averaged results was used in the INL and DNL evaluation.

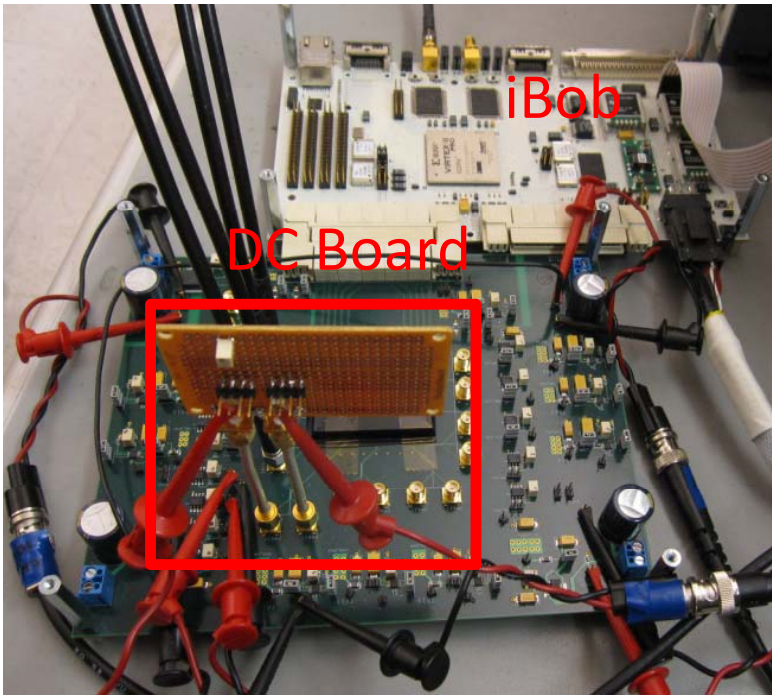


Figure 4.15: DC linearity measurement setup

DNL and INL plots are shown in Figure 4.16. The worst-case DNL and INL are +0.11/0.13LSB and +0.27/-0.22LSB, respectively.

### 4.3.3 AC Linearity Measurements

To analyze the dynamic performance of the DAC, an Agilent E4440 PSA spectrum analyzer was employed. The Agilent PSA has many features that make it ideal for DAC dynamic testing, including adjacent channel power ratio, noise spectral density, and phase noise measurement. Since the spectrum analyzer can only take single ended input, all AC measurements have been performed by connecting the output of the DAC to an off-chip transformer on the AC daughter board that translates the differential output signals to a single ended one.

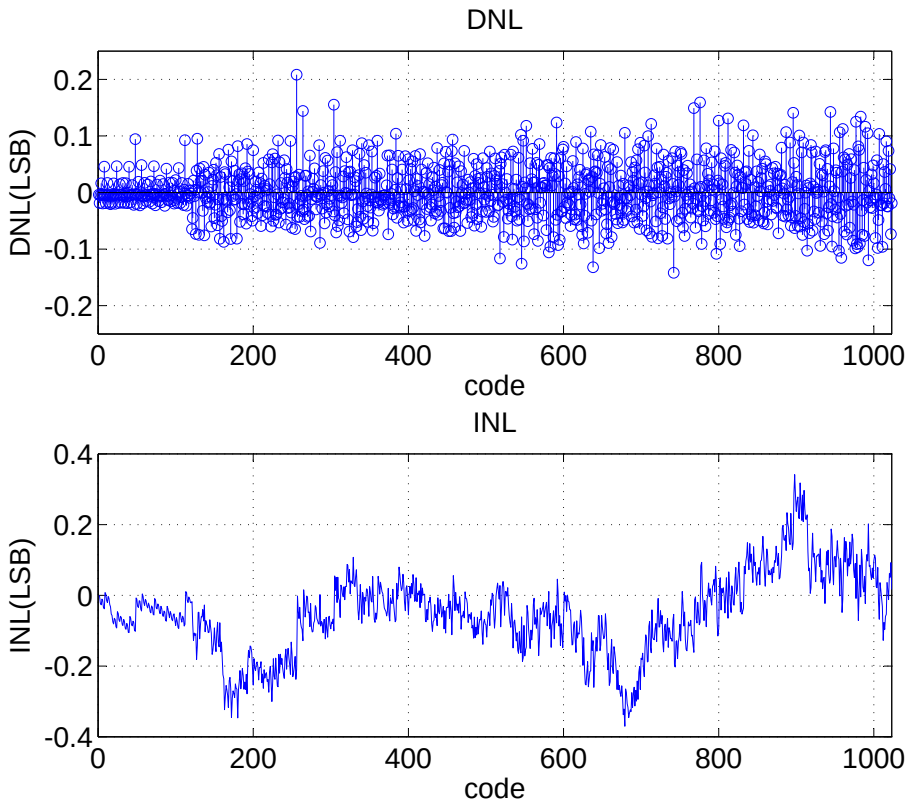


Figure 4.16: Measured DNL and INL plots

As shown in Figure 4.17, the AC linearity measurements are performed through a transformer which has a limited bandwidth. This means that the transformer may cause the artifacts that degrade SFDR measurement. For example, if the signal frequency is higher, the amplitude gets attenuated. However the spurious tone and harmonics folded back to the lower frequency zone within the transformer bandwidth don't get attenuated. Those artifacts from the transformer can be calibrated out by characterizing the frequency response of the transformer and adding back the loss due to the transformer.

### SFDR Measurement

Spurious-Free Dynamic Range (SFDR) measurements look at all the spurious tones within the Nyquist band. The SFDR is the difference, in dBc, between the peak amplitude of the output signal and the peak spurious tone over the specified Nyquist bandwidth.

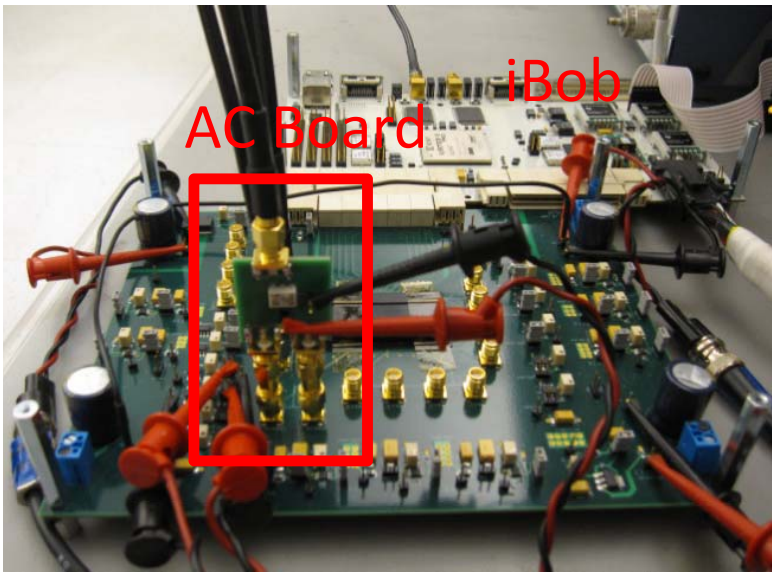


Figure 4.17: AC linearity measurement setup

Typically, the dominating spur is the harmonics, usually the second or third harmonic of the input signal.

To demonstrate the idea of SFDR measurement and waveform generation, the in-house FPGA board, ROACH (Reconfigurable Open Architecture Computing Hardware), is used as our programmable waveform generation. An DDFS block implemented on ROACH is used to generate a single tone for SFDR measurements. The depth and width of the lookup on DDFS affect the phase angle resolution and the amplitude resolution of the signal respectively. The following formula produces a perfect sinusoidal sequence of $2^K$ DAC codes, with $K \geq N+3$. It generates once cycle of a perfect sinusoid sampled at uniformly spaced time intervals.

$$g_n = round(\frac{2^N - 1}{2}(1 + \sin(\frac{2\pi n}{2^k})) \tag{4.9}$$

The function, round($x$), rounds x to the nearest integer.

This equation assumes that the DAC decodes digital input words as unsigned integers from 0 to $2^N - 1$. Due to the speed limit of ROACH, we time-interleaved two DDFS blocks and use double-data rate sampling in the FPGA output registerer. This helps us achieve our target data rate of 10-bit digital codes feeding to the DAC.

For NRZ mode, the SFDR is measured within the first Nyquist zone (from DC to Nyquist frequency).For RZ and TPH mode, the SFDR of the first image and second image are measured within the second and third Nyquist zones, respectively. The SFDR at lower

frequencies is most likely dominated by the combined effects of matching errors, IR drops and transformer effects. Figure 4.18 shows the result of SFDR measurements of three modes. The SFDR curves of the fundamental tone and its image spectrum are measured within their corresponding Nyquist zones.

The spectrum of the output signal of the first image at 590MHz in 50%TPH mode, measured at 600MS/s are shown in Figure 4.19.

Figure 4.20 shows the composite SFDR plot and the comparison with state-of-the-art CMOS DAC [27]. The composite SFDR plot of NRZ mode in the first Nyquist zone and 50% TPH mode in the second and third Nyquist zones demonstrates a wide range of SFDR >55dB up to 1GHz. By utilizing 50% TPH mode, the SFDR of image spectrum at the second and third Nyquist zones is better than that of conventional Nyquist rate synthesis, which uses the fundamental tone from a DAC with much higher sampling rates.

### IM3 Measurement

IM3 measurements look at close-in third-order intermodulation components. To measure the two-tone test, simply two DDFS modules with half-scale amplitude are implemented on ROACH. The frequency and the spacing of the two tones can be independently tuned by digital codes on the fly. This increases the flexibility of our two-tone test procedure.

The terms $2F_1 \pm F_2$ and $2F_2 \pm F_1$ represent the third-order intermodulation distortion (IMD) products of the DAC. The third-order IMD performance is the worst-case ratio of the peak value of each term to the peak value of the two input tones. The typical spacing for the two tones for IMD testing is 1 MHz. The terms $3F_1 \pm 2F_2$ and $3F_2 \pm 2F_1$ represent the fifth-order intermodulation distortion (IMD) products of the DAC. These terms are usually smaller in amplitude than the third-order IMD products, and are further away from the desired signals.

A plot of the IM3 measured at 600MS/s in NRZ and 50% TPH mode is shown in Figure 4.21. It demonstrates IM3 less than -60dBc in the first and second Nyquist zones and less than -55dBc in the third Nyquist zone, sampling at 600MS/s.

Figure 4.22 shows a spectrum of the output signal of a two-tone test centered at 570 MHz and 620 MHz at sampling rate at 600MS/s.

Non-ideal switching properties associated with the DAC can result in increasing power levels for the lower order harmonics. Compared to IM3 measurements, the SFDR results clearly show a lower bandwidth than the IM3 results. Note here that IM3 has smaller span while SFDR measurement are across the whole Nyquist band. The spurious tones are folded

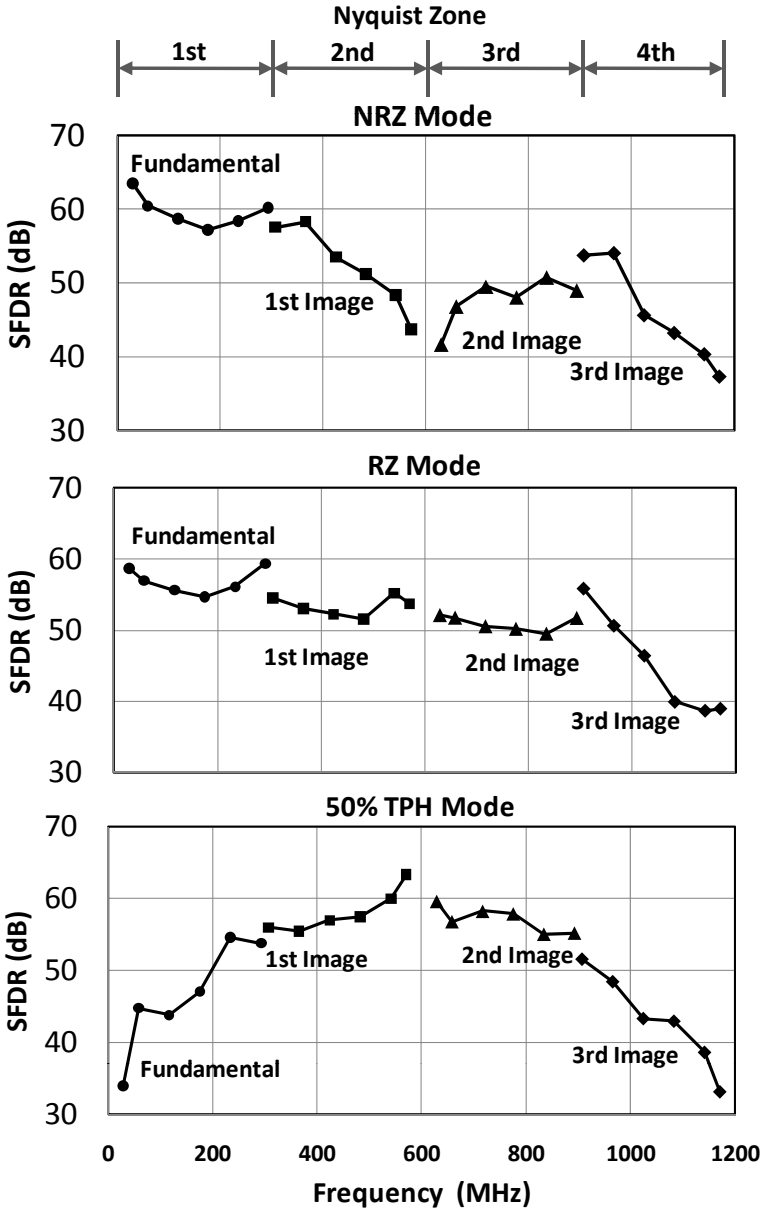


Figure 4.18: Measured SFDR curves: NRZ, RZ, and 50%TPH mode

back to its Nyquist zone which degrades the SFDR. This explains why the IM3 has better reported numbers than SFDR.

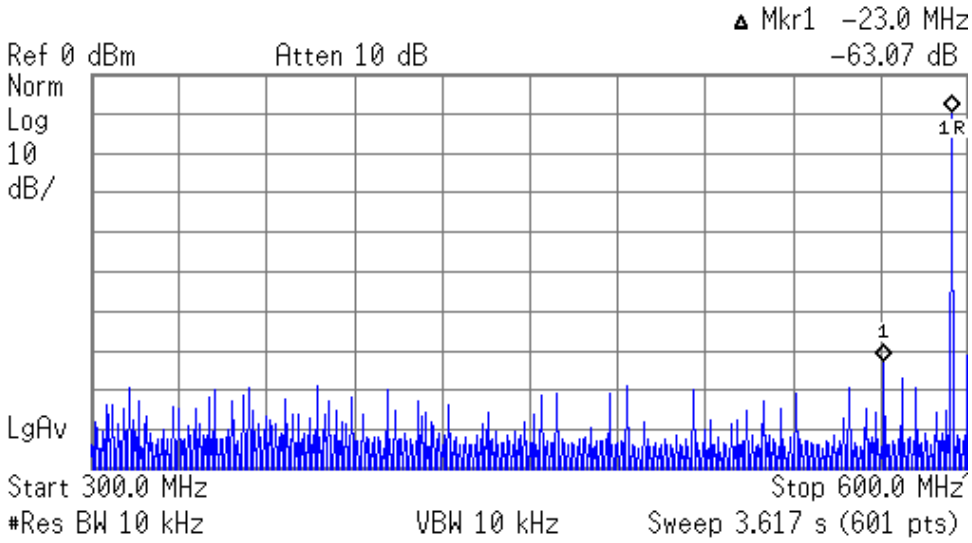


Figure 4.19: Output spectrum of the 1st image at 590MHz in 50%TPH mode, sampling at 600MS/s

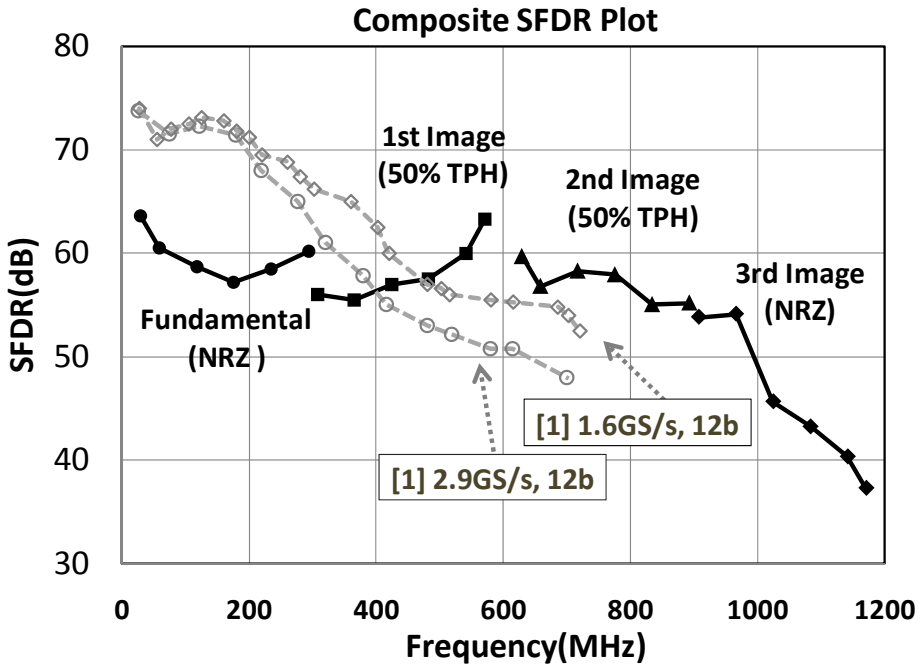


Figure 4.20: Composite SFDR plot (NRZ + 50% TPH)

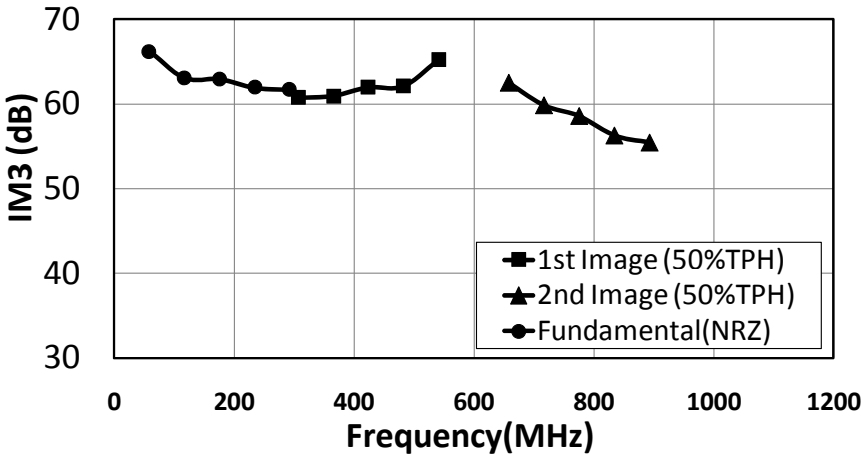


Figure 4.21: Measured IM3 versus signal frequency: NRZ + TPH mode

**Amplitude Response**

By sweeping the test tone in the single tone test, the normalized output magnitude response is measured to show the spectrum envelopes of NRZ, RZ and 50% TPH mode. The loss through the output transformer is factored out of the measured amplitude response. Figure 4.23 shows the measured amplitude response versus signal frequency, sampling at 600MS/s. The multi-mode operation shapes the spectrum envelope and shifts the energy from fundamental in 1st Nyquist zone to the image frequency at higher Nyquist zones.

### 4.3.4 Power Consumption

A breakdown of the chip's power consumption is illustrated in Figure 4.24. A constant amount of the power, 12mW, is consumed by the current cells. The digital decoding logics, data buffers and latches consume 7.5mW of power. A large portion of the power, 10.5mW, is consumed in the clock buffers, needed to distribute a high-speed clock and mode control signals across the chip.

In this testing setup, two parts of the power consumption are not counted in the breakdown analysis. First, the biasing and the reference circuit consume 1.28mW of power. Second, the I/O peripheral and high-speed LVDS receivers consume 40mW power in total for receiving the high-speed 10 bit data from the off-chip FPGA. This part can be eliminated if

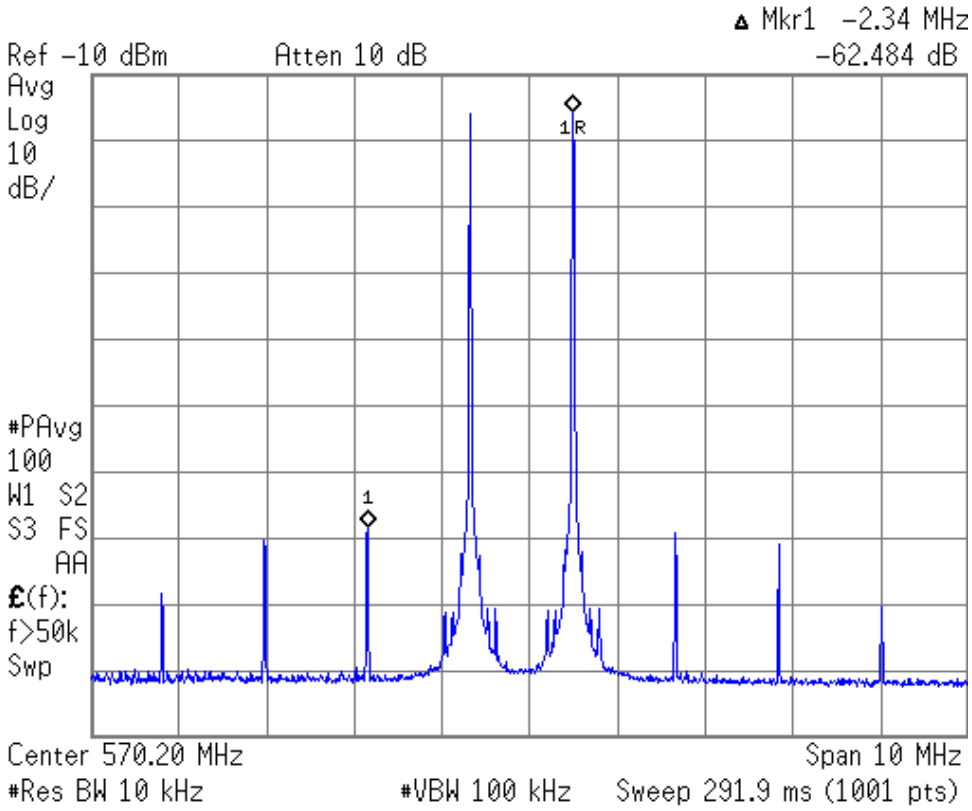


Figure 4.22: Output spectrum of two-tone IMD centered at 570MHz in 50%TPH mode, 600MS/s

the DAC is used for embedded applications and integrated as part of the transmitter chain. Therefore, there will be no need of delivering these high-speed digital signal from off-chip sources.

The performance of this DAC is summarized in Table 4.1.

### 4.3.5 Comparative Analysis

Table 4.2 shows a comparison with the published state-of-the-art CMOS DACs [27, 32, 33, 38, 39]. These CMOS DACs are driving 50 ohm load with various output currents ranging from 10mA to 50mA. Also, the resolution (number of bits), sampling rate, output swing, SFDR and IM3 performance of these DACs are different from each other duo to the specific target applications.

A direct comparison of the absolute power dissipation will make no sense, since each

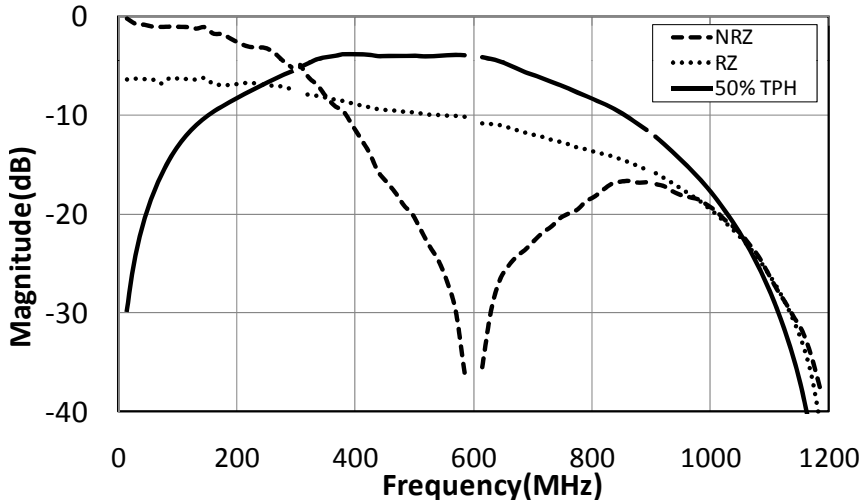


Figure 4.23: Measured amplitude response

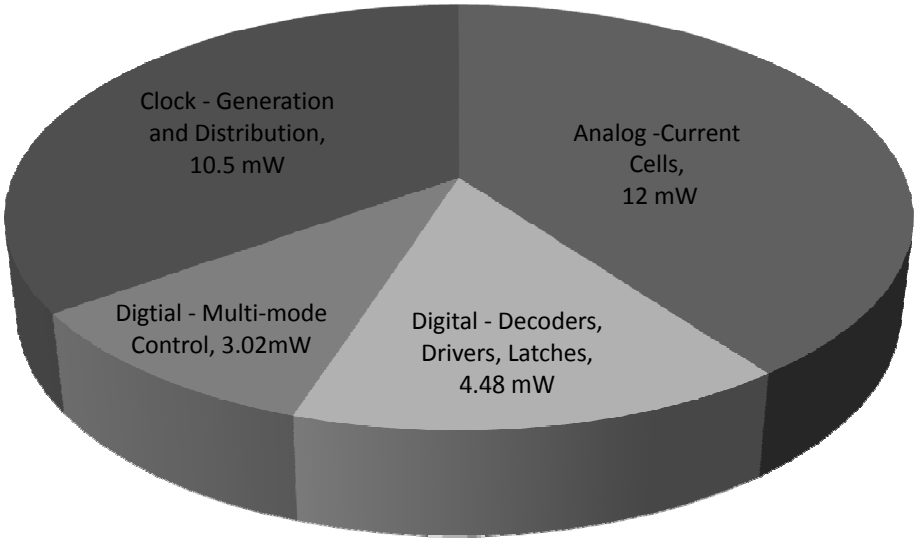


Figure 4.24: Power consumption breakdown

DAC was optimized and designed for different targets. Unlike ADCs, there is no general or commonly-used figure of merit (FOM) for evaluating the power efficiency of DACs. A simple

Table 4.1: Performance summary of the multi-mode sub-Nyquist rate DAC

| | | | |
|---|---|---|---|
| **Resolution** | 10bits | | |
| **Sampling Rate** | 600MS/s | | |
| **Full-Scale Current** | 10mA | | |
| **Output Swing** | 0.5V (single-ended) / 1V (differential) | | |
| **Supply Voltage** | 1.0V (Clock/Digital part) / 1.2V (Current Cell) | | |
| **$DNL_{PEAK}$** | 0.11/-0.13 LSB | | |
| **$INL_{PEAK}$** | 0.27/-0.22LSB | | |
| **Single-tone SFDR** | NRZ | >55dB (Fundamental, in 1st Nyquist zone) | |
| | 50%TPH | >55dB (First Image, in 2nd Nyquist zone) | |
| | 50%TPH | >55dB (Second Image, in 3rd Nyquist zone) | |
| **Power Dissipation** | DAC | 19.5mW | |
| | Clock Generator | 10.4mW | |
| **Area** | DAC Core only: 350um x 300 um | | |
| **Technology** | 65nm CMOS process | | |

Table 4.2: Comparison of published CMOS current-steering DACs

| | This Work | [26] | [35] | [36] | [38] | [39] |
|---|---|---|---|---|---|---|
| **Tech (nm)** | 65 | 65 | 180 | 180 | 250 | 350 |
| **Resolution (bit)** | 10 | 12 | 14 | 12 | 16 | 10 |
| **$F_{clk}$ (GHz)** | 0.6 | 2.9 | 1.4 | 0.5 | 0.4 | 1 |
| **$I_{load}$ (mA)** | 10 | 50 | 30 | 15 | 20 | 16 |
| **Swing (Vppd)** | 1 | 2.5 | 1.5 | 0.75 | 1 | 0.8 |
| **Power (mW)** | 30 | 188 | 200 | 216 | 400 | 110 |
| **FOM (mW/MSps)** | 0.05 | 0.06 | 0.14 | 0.43 | 1.00 | 0.11 |

FOM is used here for comparing the designs along by two dimensions of power and sample rate. This is just the first-order comparison to see how much power consumed for every mega-samples per second. According to the comparison table, this work achieves a better FOM (0.05 mW/MSps) and less total power consumption, while delivering the comparable

SFDR performance as the state-of the-art DAC in [27].

$$FOM = \frac{Power(mW)}{SamplingRate(MSps)} \tag{4.10}$$

The advantage of a sub-Nyquist rate DAC in power savings can be analyzed by breaking down the sources of power consumption. The total power consumption in a high-speed DAC can be decomposed into three parts: the analog power, the digital power and the clock power. The analog power is relatively independent of the clock frequency. The digital power and clock power scale linearly with the clock frequency. For a given output swing and a fixed analog/digital supply voltage, we can expect that the total power consumption goes up linearly as the clock frequency increases as shown in Figure 4.25. By applying sub-Nyquist rate conversion, we can run the DAC at 600MS/s to cover the target TV band, while consuming 30mW of power. If we use a conventional Nyquist rate DAC (1.6GSps or higher) instead, the power consumption will go above 60mW by our first-order estimation. Obviously, this is due to the big power overhead from the clock distribution network and the digital circuit operating at a much higher clock frequency.

The estimation here is based on a simplified model of power consumption. We can further derive a more precise model for the power consumption and a more complicated FOM by taking the more factors into account, such as resolutions, output swing and dynamic performances.

Compared to Nyquist rate synthesis, the sub-Nyquist rate conversion can help reduce the amount of power consumed in the digital and clock portion because the reduced sampling rate needed in the digital and clock portion.

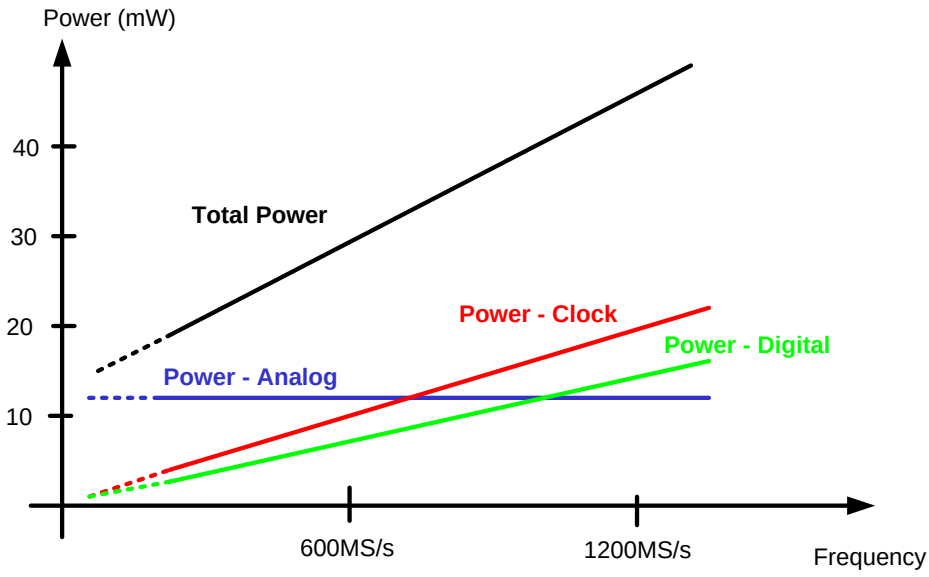


Figure 4.25: Power consumption versus frequency

# Chapter 5

# Conclusion

## 5.1 Summary

In this work, we present a direct waveform synthesis transmitter that provides as a frequency-agile solution for TV band cognitive radio applications. It enables full digital control and wideband synthesis waveform. The proposed multi-mode sub-Nyquist rate conversion technique shapes the spectrum envelope for generating wideband flat response over the target TV band (54 $\sim$ 862MHz). The transmitter architecture features mostly-digital implementation. Compared to Nyquist rate direct synthesis, this DWS transmitter reduces both system complexity and power consumption by half.

The contribution of this work is two-fold: theoretical and practical. The scope of this work has covered from the radio system architecture to the circuit implementation. On the theory side, this dissertation explores both the optimal system and circuit solution for TV band cognitive radio applications. In the existing literature, the bottleneck of D/A conversion stage in SDR-based transmitter has been somewhat lack of new techniques for breakthrough. Signal processing techniques was applied to exploit across digital and analog boundary. The proposed multi-mode sub-Nyquist rate D/A conversion enables the direct waveform synthesis.

On the practical side, a prototype integrated sub-Nyquist rate DAC was designed and fabricated in a general-purpose 65nm CMOS process. While this DAC did not advance the state of the art for the conversion speed and SFDR, the sub-Nyquist rate conversion technique was shown to be an alternate for delivering comparable SFDR performance using

higher Nyquist zones. This technique opens up the possibility of combining the functionality of digital-to-analog conversion and up-conversion in a single block.

In summary, the research contributions include:

- A direct waveform synthesis transmitter using Sub-Nyquist rate conversion technique to reduce overall complexity and cost.
- Circuit implementation in general-purpose 65nm CMOS process and system prototype for demonstrating the proof-of-concept design.
- Distributed output re-sampling switches and multi-phase control for multi-mode reconstruction.
- Design of a high-speed Sub-Nyquist rate DAC for wideband waveform synthesis

## 5.2 Suggestions for Future Work

In the evolution of cognitive radio development, bandwidth and reconfigurability are still two main challenges. SDR-based CR devices are the ultimate target on the road map of the future radio technology development, as shown in Figure 5.1. We are expecting that the advanced CMOS technology accelerates the development of mostly-digital transmitters and fulfills the bandwidth and reconfigurability requirements of cognitive radio applications. Intuitions gained from this work enlighten the future advances of sub-Nyquist rate conversion and next-generation digitized transmitter architectures. There are several directions that can further improve the performance of sub-Nyquist rate DACs.

- Both I and Q channels can be implemented on chip so that the SSB signal can be directly generated on chip to demonstrated wider range of waveform synthesis across multiple Nyquist zones.
- To make the SFDR and IMD test easier, an on-chip board Direct Digital Frequency Synthesis (DDFS) can be implemented with DAC cores. The on-chip DDFS can avoid the use of the 10 bits high-speed parallel data transmitted through off-chip and PCB traces. This was the limiting factor of AC linearity test in this implementation. The highest conversion rate was constrained by the speed of 10 bit digital codes from off-chip FPGA board.

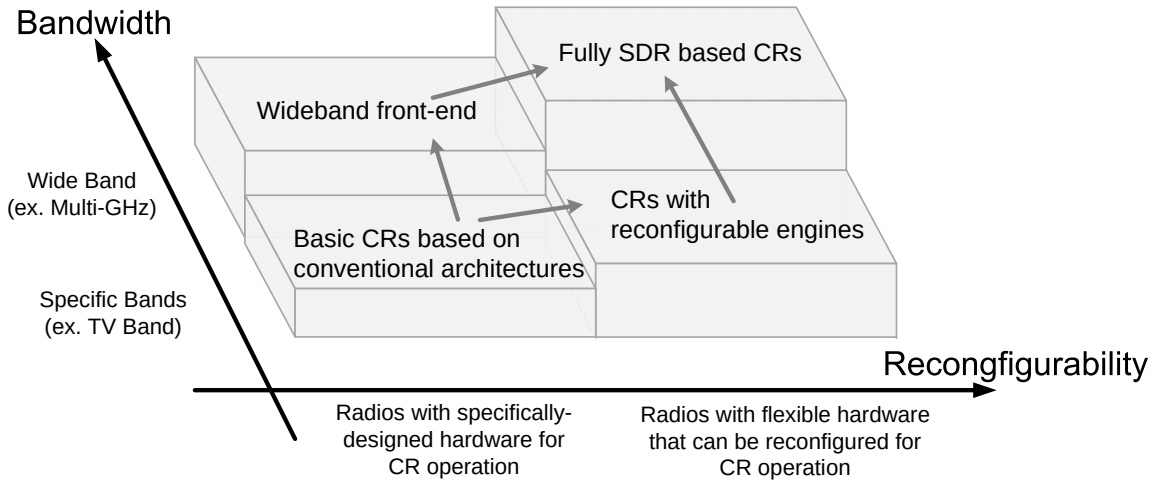


Figure 5.1: The evolution of cognitive radios

- The multi-mode output switch can be replaced by thick-oxide device to enhance the reliability and sustain higher output swing.
- The conversion rate of the DAC can be further increased in deeply scaled CMOS. This will provide wider bandwidth for cognitive radio applications.
- There are several minor changes which can be applied on the DAC core design: revising local re-synchronization latch design, using binary tree for supplies and output current, applying DEM or Digital Random Return to Zero (DRRZ) to remove the code-dependent switching transients [48].

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# Appendix A

# Appendix A: TV Band White Spaces

| Bands | Channel | Frequency | Notes |
|---|---|---|---|
| VHF | 2 – 6 | 54 ~ 88 MHz | |
| | 7 - 13 | 174 ~216 MHz | |
| UHF | 14 - 36 | 470 ~ 608 MHz | |
| | 37 | 608 ~ 614 MHz | reserved for radio astronomy |
| | 38-51 | 614 ~ 698 MHz | |
| | 52- 69 | 698 ~ 806 MHz | |
| | 70 - 83 | 806 ~ 890 MHz | |

Figure A.1: US TV channels