Interference Management Techniques for Multi-Standard Wireless Receivers

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Interference Management Techniques for Multi-Standard Wireless Receivers

by

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Professor Paul K. Wright

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Abstract

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The performance of wireless standards is improving steadily for a foreseeable future. Wireless communications are used for a variety of applications from data steaming to Internet access. There is an increasing need for wireless connectivity with emerging applications. More frequency spectrum is going to be opened-up and the number of standards seems to increase even further to cover this gap and the question arises of how to design the next generation of wireless receivers.

From a general perspective it is very appealing to have a single handheld device that can support a large number of wireless standards. Consequently, mobile handsets have started supporting multiple modes over the past few years. Since there are too many standards, integrating multiple dedicated radios on one platform is leading to bulky, complex designs and hence hardware sharing is becoming the only solution. One of the last hurdles in the realization of a multi-standard receiver is the elimination of off-chip SAW filters. Direct conversion receivers are widely implemented due to low cost and high-levels of integration at the cost of sensitivity to interferes and second order distortion, which are key contributors to degrading system sensitivity. This thesis describes two linearity enhancement techniques for an RF receiver.

A self-calibrating even-order distortions technique is presented whereby different mechanisms responsible for even-order distortions, characterized by IIP2 metric (Second Harmonic Input referred Intercept Point), were independently calibrated, resulting in robust performance independent of the amplitude and frequency of the blocker. Second, an active dynamic blocker-notching scheme is proposed and tested. The filter uses the blocker frequency to up-convert a DC null to the pass-band, attenuating the blocker before entering the receiver. The prototype circuits are fabricated in a 90nm CMOS technology. Measurements were performed on a PCB with a packaged chip.

IIP2 measurements were performed with the blocker frequency and power swept. The IIP2 of more than 60dBm for wide range of blockers as high as -10dBm has been achieved which satisfy the most stringent IIP2 requirements. To test the functionality of the dynamic notch, a blocker signal and a desired signal are summed and injected into the front-end

receiver. The amount of desired blocker attenuation and the amount of undesired in-band signal attenuation are both measured versus the offset frequency of the blocker. Blocker attenuation as large as 20dB is observed at only 40 MHz offset while the in-band attenuation increases by only 2dB. The resulting increase in noise figure due to the blocker is 4dB. When all of this data is taken into account, the overall SNR improvement due to the notch filter is as high as 14dB. This proves that the technique may be effective for attenuating blockers.

To My Mother, Professor Shahnaz Atabak

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Chapter 1

Introduction

In 1864 James Clerk Maxwell derived the fundamental equations for electromagnetic fields. Shortly afterward, Heinrich Hertz validated the equations based on a experiment which propagated the electromagnetic waves into the free space. The radio was invented later on with the patent of Guglielmo Marconi, the first patent in wireless communications. The idea was to put information on these free-space propagating EM waves to get rid of the wires.

Since then, quite a large number of brilliant minds (and also billions of dollars!) from different fields contributed to evolving the wireless communication. Looking at the pace of progress, one would observe the kink, [58], at the mid-twentieth century where two groundbreaking scientific discoveries happened. Invention of the transistor by William Shockley at Bell laboratories and on the information theory side, the definition of the channel capacity by Claude Shannon. Microelectronics and information theory ever since have progressed quite dramatically that connectivity and mobility is a commodity. Variety of wireless standards are providing different services, e.g. voice and data transfer, Internet access, etc. among different geographical regions. The ever-increasing need for bandwidth has been fulfilled with developing semiconductor technology, and as a result, the wireless services have kept improving steadily.

Wireless communication is routinely used in everyday life and it is more like a commodity these days than a fancy technology. It's used for all kind of information transferring without a need for troublesome, expensive infrastructure to connect the devices. Consequently more and more platforms are being built upon it and hence the quest for bandwidth has been steadily intensified.

The wireless service industries need to keep pace with markets needs. Therefore, they have started to include more and more radios on one platform that would result in bulky complex designs which not only takes massive amount of resources to design but also this approach can't be sustained with the continually increasing number of standards and fast-changing technology which requires porting designs frequently.

Hence hardware sharing or multi-standard modules have become a must to meet the ever-increasing market's need. One of the most important issues in the realization of multi-standard receivers is the elimination of off-chip SAW filters so that signals from different

Figure 1.1: Marconi's station

bands can enter the shared hardware.

One can imagine this wide-band system would process a number of non-desired, interferers, along with the desired signals. Now the blocks that were designed to only deal with desired signals should be able to withstand blockers, sometimes many orders of magnitudes higher than desired signals. This issue would be exacerbated by the fact that in more advanced nodes, transistors have poor linearity performance and supply voltage reduction deprives designer from a pool of circuit tricks that would allow them to tackle this issue.

Hence, during past few years a number of promising solutions have been offered from different themes in the wireless systems to enable multi-mode multi-standard operation so that society would witness faster and smarter device which are enabler to communicate with almost everything in the environment, from satellite GPS all the way down to inside our bodies.

This thesis will first present the fundamentals of wireless receivers and what are the important parameters one should be looking at optimizing. Then it will discuss the trends in the wireless industry and will present the state-of-the-art systems with their pros and

cons.

Overall there are two schools of thought for attacking the blocker problem. One is to optimize each block to linearity so it could process the blockers without loosing their sensitivity. The other approach is to get rid of the jammers as soon as possible.

Both approaches have been pursued in this work and the pros and will be presented in chapters 5 and 6.

Chapter 2

Fundamentals of Wireless Receivers

In this chapter, fundamentals of wireless receivers will be reviewed. It begins with the introduction of direct conversion receiver and its inherent trade-offs. Furthermore, performance metrics characterizing receivers will be covered.

2.1 Receiver Architecture

The application of wireless receiver is to identify the desired signal, transform it from the electromagnetic domain to electric signals, and process them (frequency shift and amplification) such that the analog to digital converters can be able to convert them to the digital domain. Where to put the border for this transition depends on the accuracy and speed of these converters and hence the definition of wireless receiver and its architectures should be revisited every once in while due to rapid change in the technology. The so call holy grail is to put an ADC right after the antenna [53]. Looking at today's ADC performances, it reveals the speed of operation and the dynamic range required haven't been met concurrently. As a result, traditional architectures still play a vital role.

Among different receiver architectures that have been invented, heterodyne and direct conversion receiver are the most used ones. However, due to extremely simple architecture, the direct conversion receiver [2] and [60] has become the receiver topology of choice for monolithically integrated receivers. In the cellular market, direct conversion architectures have superseded the well established heterodyne architecture.

In heterodyne receivers, the RF signal is first down-converted to an intermediate frequency (IF). Then, the signal would be filtered with high Q IF filter which could not be implemented in the RF domain. Afterward the final down-conversion would occur. This approach requires a few number of off-chip filters for band-selection and image rejection, two reference clocks and is quite power hungry and overall, not friendly to integration.

On the other hand, the direct conversion architecture requires minimum number of filters since it doesn't need image rejection as the frequency shifting is happening once. However, this approach suffers from a number of disadvantages. Most important ones arise from the

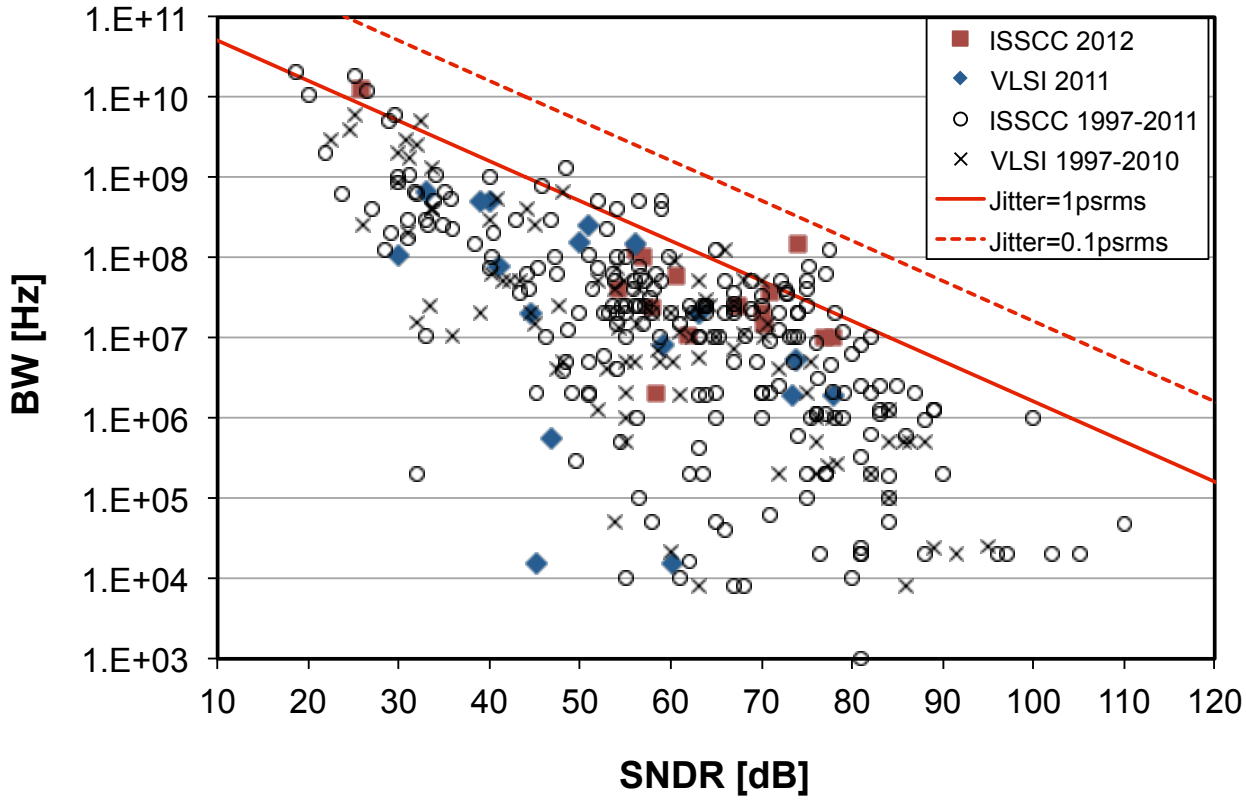

Figure 2.1: ADC performance [55]

fact that signal is directly retrieved from a low-frequency regime. That makes the system very sensitive to any phenomena leading to generation noise/non-desirable content at low-frequency.

In terms of noise, when it comes to low-frequency regime, the flicker noise will be dominant mechanism. Unfortunately it exacerbates as transistors scale down. From non-desirable content generation, the main mechanisms responsible for them are even order distortions as they have an inherent down-conversion mechanism mathematically. These two effects, specially the second one, will make the design of DCR challenging. One chapter of this thesis is dedicated to the issue of the even-order distortions and will be covered in details.

2.2 Wireless Receiver Performance Metrics

In order to characterize wireless receivers, performance metrics have to be defined. In this section, fundamental parameters which characterize a wireless receiver are discussed. The quality of wireless signal is deteriorated by receiving undesired signals through-out the chan-

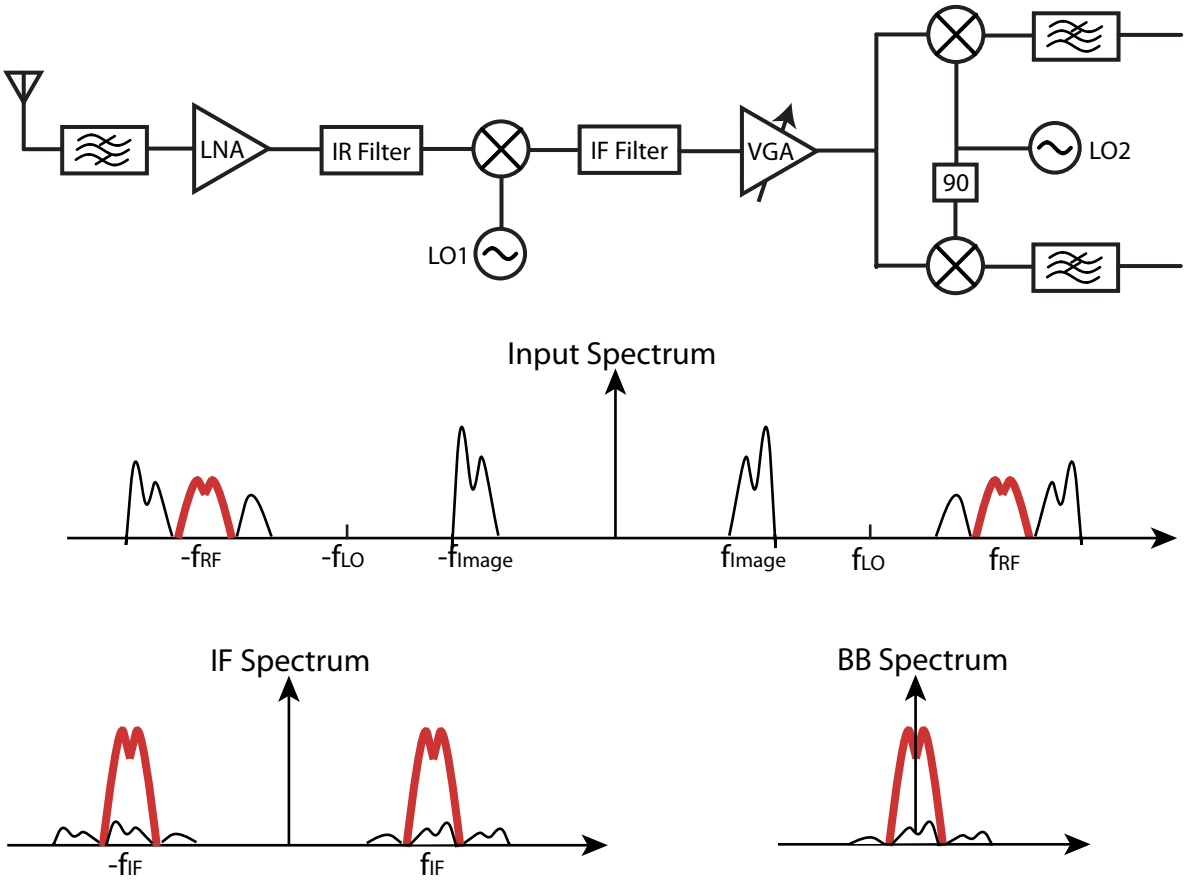

Figure 2.2: Superheterodyne receiver

nel. Also other than the noise added by the channel, the wireless transceivers add their own noise and unwanted signal degrading the quality even further.

Above shows a typical challenging scenario of a receiver receiving a weak desired signal from a far away transmitter and at the same time, a close-by transmitter is jamming the receive with a strong unwanted signal.

Since jammers in channels can be several orders of magnitude greater than the desired signal, implementing a system that is able to detect the weak wanted signal while receiving a strong interferer presents the major RF design challenge of incorporating a low noise system with good linearity.

To characterize an extent to which wireless receivers deteriorate signal quality, various parameters are used.

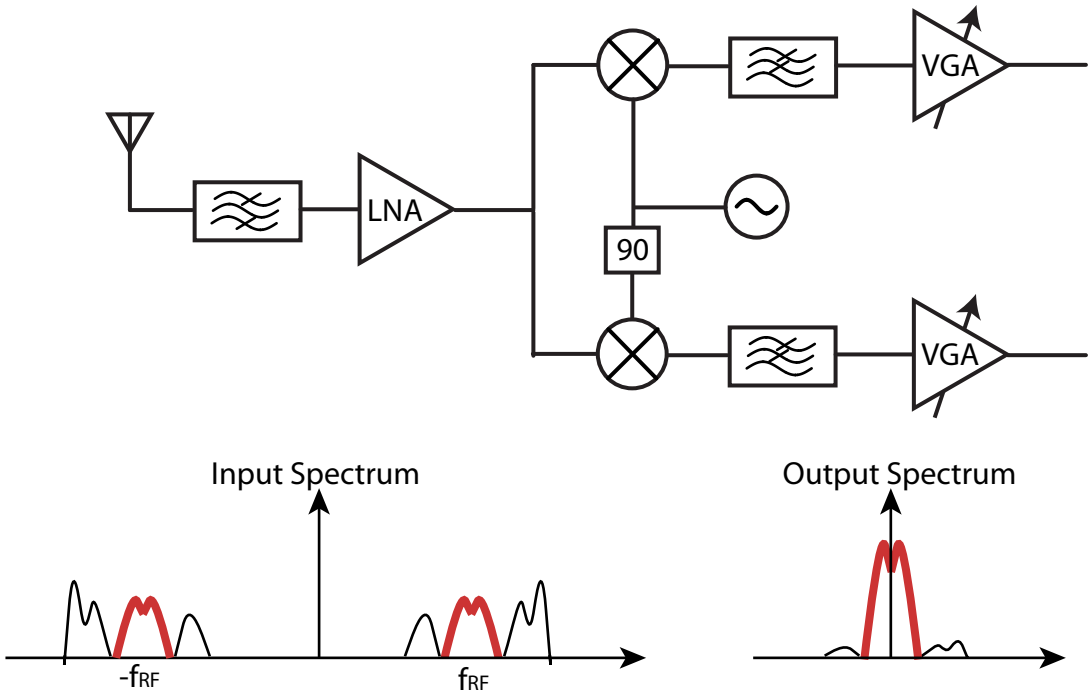

Figure 2.3: Homodyne receiver

Noise

Random fluctuations of physical quantities would cause picking up signals at the frequencies of interest that are not related to our desired signal and would place a threshold on the minimum signal one can detect. This is a serious problem in wireless receiver as the signals they are trying to pick-up sometimes are extremely small (on the order of microvolt). The metric for that in wireless receivers is noise figure. Generally noise in CMOS receiver is coming from three sources [31]:

Thermal noise is due to thermal movement of charge carriers. Any circuit elements that include resistor in its modeling, has thermal noise. The spectral density of thermal noise is constant and can be modeled as white noise.

Shot noise exists in structures that charge carriers are passing a potential barrier such as P-N junctions or the gate barriers. The power spectral density of this type is constant as well and can be modeled as a white noise.

Flicker noise is due to trap and release of the carriers at the silicon channel and the oxide. The time constant of this phenomenon causes the power spectral density to have $1/f$ characteristics.

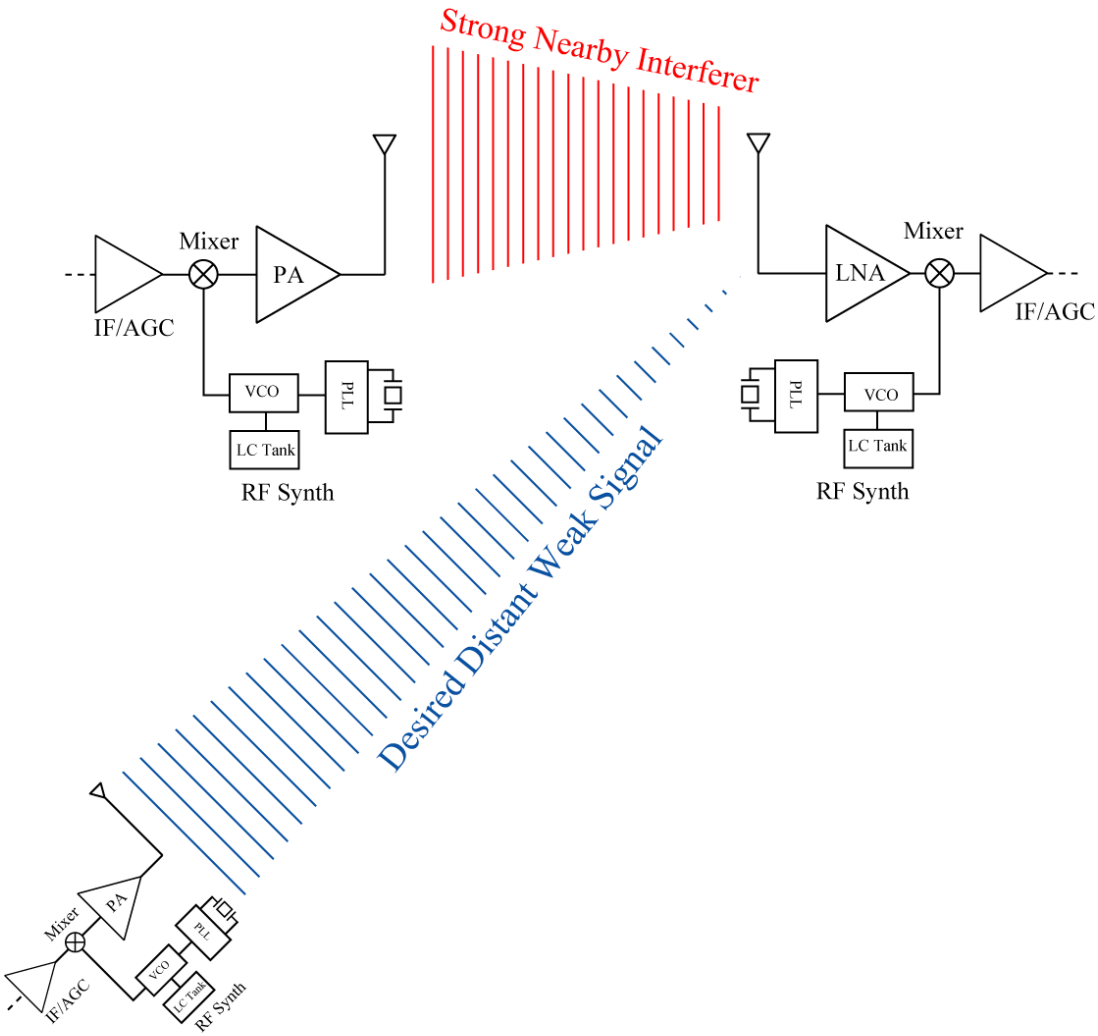

Figure 2.4: Near far issue in wireless receivers [56]

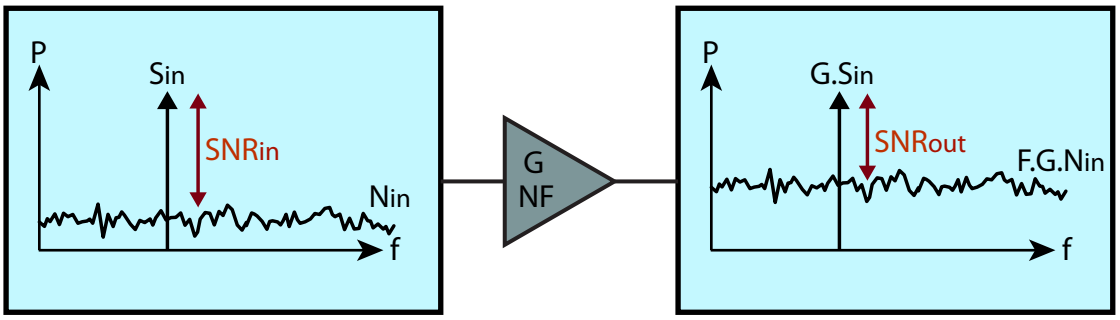

Figure 2.5: Signal to noise ratio at input and output [26]

No matter what the source of the noise, one needs to characterize the overall noise performance of the receiver. This can be done with the following equation. Since the input noise which is coming from black body radiation to the system and the desired signal will see the same gain down the chain, the signal to noise ratio would get exacerbated due to the noise added by the system. This ratio is called noise factor and the logarithm of F is defined as the noise figure:

$$\text{NoiseFactor} = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \tag{2.1}$$

$$\text{NF} = 10\log(\text{NoiseFactor})[\text{dB}] \tag{2.2}$$

The receiver noise factor is an important parameter in determining the weakest signal that the system can process. This translates directly into a maximum distance from the transmitter where communication is possible. The output noise power of a receiver, being a function of the noise factor, bandwidth and receiver gain, can be calculated as follow:

$$\text{N}_{\text{OUT}}[\text{dBm}] = -174\text{dBm} + 10\log\text{BW} + \text{NF}[\text{dB}] + \text{G}[\text{dB}] \tag{2.3}$$

Now if one divides the output noise by the receiver gain to get the equivalent input referred noise, that would set the minimum signal that the system is able to detect.

$$\text{MDS}[\text{dBm}] = -174\text{dBm} + 10\log\text{BW} + \text{NF}[\text{dB}] \tag{2.4}$$

The noise floor is directly proportional to bandwidth. Consequently, higher data rate systems which require more bandwidth for a specific modulation scheme, the minimum detectable signal rises.

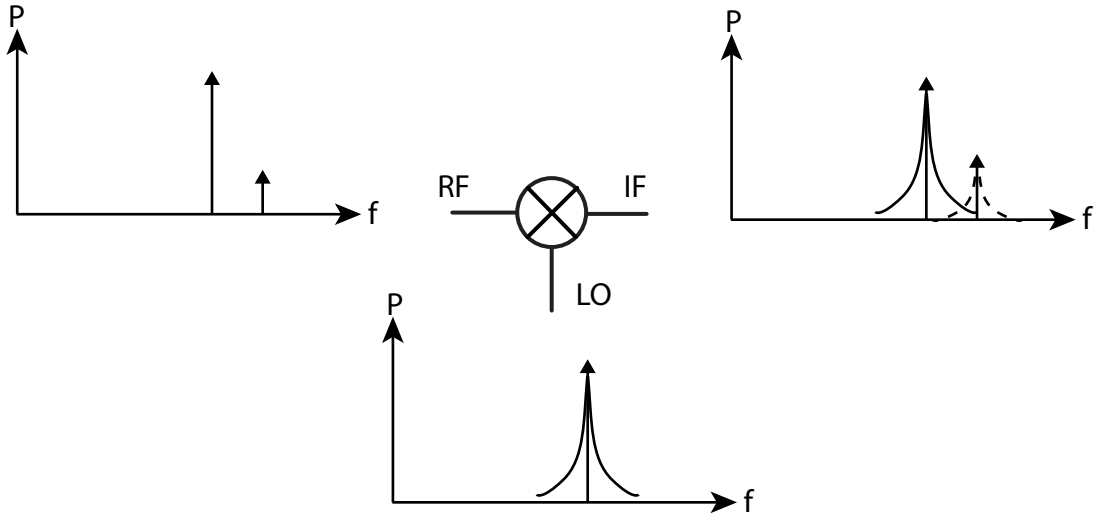

Figure 2.6: Reciprocal mixing

Sensitivity

Sensitivity is defined as the minimum signal power required for a specific quality of received information. In digital information, this would be measured by the bit error rate. Basically, sensitivity is the required power level to achieve a specific signal to noise ratio:

$$\text{Sens[dBm]} = \text{MDS[dBm]} + \text{SNR[dB]} \tag{2.5}$$

Phase Noise

The local oscillator of the system is the unit in charge of frequency shifting of the received RF signal. The ideal condition from a mathematical point of view is to have a tone in the frequency spectrum to shift the frequency content. However, due to non-idealities and the existence of noise, the phase of the waveform has a jitter component which would spread the energy of the tone in the spectrum.

$$LO(t) = A\cos(\omega_{LO}t + \phi_{n(t)}) \tag{2.6}$$

$\phi_{n(t)}$ represents phase noise. Basically it would modulate the signal that results in sidebands forming around the carrier. Phase noise is characterized in the frequency domain in terms of dBc/Hz at a given offset frequency from the carrier frequency.

Phase noise in wireless receiver is responsible for a phenomenon called reciprocal mixing. Since the function of mixer is multiplying the RF signal with the LO signal in the time domain, that would translate to convolution in the frequency domain. Now if there are blockers near the RF signal, lets say X Hz away, coming through the RF port, they would

be down-converted and fall ON top of the desired signal with the noise energy X Hz away from the carrier.

The noise level in the wanted signal band caused by reciprocal mixing can be expressed as follow:

$$\mathrm{P_{n,recmix}[dBm]} = \mathrm{P_{blocker}[dBm]} + \mathrm{L(\Delta f)} + \mathrm{10logBW} \tag{2.7}$$

where $\mathrm{P_{blocker}}$ is the blocker level, Δf is the offset between the blocker and the wanted signal frequencies while BW denotes the wanted signal bandwidth. The assumption is that the phase noise is constant across the BW of the desired signal. If the bandwidth of the signal is large and it changes across it, that should be taken under consideration.

Nonlinearity

Nonlinear systems can be categorized as systems which are capable of generating new frequencies. In other words, their output frequency spectrum is not necessarily the same as the input.

To begin the study the effects of nonlinearities, one should start with the time-invariant, memoryless nonlinear systems. For such systems, the output signal can be expressed using a Taylor series expansion as:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + ... \tag{2.8}$$

Harmonics

If a sinusoid is applied to a nonlinear system, the output contains frequency components that are integer multiplies of the input frequency. Putting $A\cos(\omega t)$ in the above equation one obtains:

$$\begin{aligned} y(t) &= a_0 + a_1 A\cos(\omega t) + a2A^2\cos^2(\omega t) + a_3 A^3\cos^3(\omega t) \\ &= a_0 + a_1 A\cos(\omega t) + \frac{a_2 A^2}{2}(1+\cos(2\omega t)) + \frac{a_3 A^3}{4}(3\cos(\omega t) + \cos(3\omega t)) \\ &= a_0 + \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{2.9}$$

From the above equation, one can calculate the expected harmonics power in the output spectrum. There are a few important metrics obtained from the above equation:

Gain Compression

All designed systems have specific dynamic range. The minimum signal that the system can be detected which is set by the the gain and noise budget. The maximum signal which is

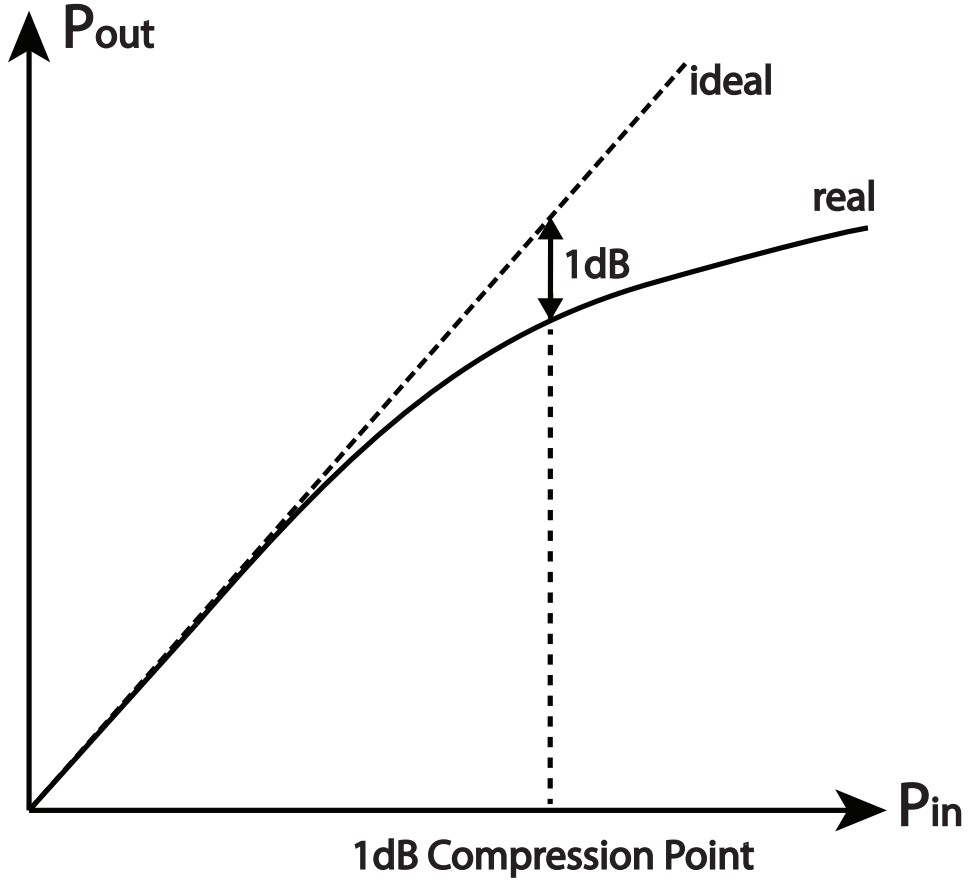

Figure 2.7: Gain compression

function of the gain and available headroom and the linearity characteristics of the building blocks.

The small-signal gain a_1 parameter valid only for sufficiently low-power regimes. As the amplitude of the power of the input signal increases, the power of output signal increases linearly until certain amount. Then, the gain of the system at that particular frequency starts changing. This phenomenon is natural as there is always limitations to the amount of signal power a system can generate.

To quantify the effect, a parameter called 1dB compression point (1dB CP) is defined. It is defined as the input signal level at which the output signal level drops by 1dB compared to a perfectly linear device. Consider a system in which it can be defined by nonlinearities up to third order. As expanded above, the gain which the fundamental tone would see is:

$$G = a_1 + \frac{3}{4}a_3A^2 \tag{2.10}$$

where A is the amplitude of the input signal. Evidently, the second term is responsible

for the gain compression. First, one might notice about the importance of the sign of a_3. Considering the conservation of energy in the electronic system, a_3 should be negative for a signal large enough. Then the 1dB compression point would be:

$$\sqrt{0.11\frac{4|a_1|}{3|a_3|}} \tag{2.11}$$

Generally, the 1dB CP gives system designer a sense of how linear the system is and when it will enter the nonlinear regime so one should start to worry about other mechanisms.

Desensitization

This phenomenon is much more troublesome for RF designer than the compression. Since in this one, the desired signal remains weak and the interference is the one jamming the radio.

So why desensitization is harming the system? Imagine a scenario in which a high power undesired signal is accompanying a desired low power signal. The gain of the system is compressed due to processing of this large undesired signal. Hence, the noise figure would rise according to the:

$$\mathrm{F_{Total}} = \mathrm{F_1} + \frac{\mathrm{F_2}-1}{\mathrm{G_1}} + \frac{\mathrm{F_3}-1}{\mathrm{G_1G_2}} + ... + \frac{\mathrm{F_k}-1}{\mathrm{G_1G_2...G_{k-1}}} \tag{2.12}$$

If the gain drops, G_1, the noise contribution from the following stages becomes important. Now the minimum detectable signal should have a higher power to be seen through the noise.

To quantify the effect, the equations is the same as the compression scenario with the difference in the input signal. This time there are two signals, desired and the jammer, $x(t) = (A_S\cos(\omega_S t) + A_L\cos(\omega_L t))$, then the output is:

$$y(t) = (a_1A_S + \frac{3a_3A_S^3}{4} + \frac{3a_3A_SA_L^2}{2})\cos(\omega_S t) \tag{2.13}$$

Having in mind $A_S << A_L$, one can obtain the gain which the desired signal sees:

$$y(t) = (a_1 + \frac{3a_3A_L^2}{2})A_S\cos(\omega_S t) \tag{2.14}$$

As discussed before, the a_3 term is negative and as a result, the gain would be decreased with increasing the blocker power. Based on the above equation, one can calculate the amount of gain drop as the blocker power increases.

Intermodulation Distortion

Intermodulation distortion (IMD) happens when the input signals are not pure tones anymore. In such scenarios, the components in the output spectrum are not necessarily harmonics of one another. These distortion products originate from the difference and sum of input tones and their harmonics. To quantify these effects, one can consider the following

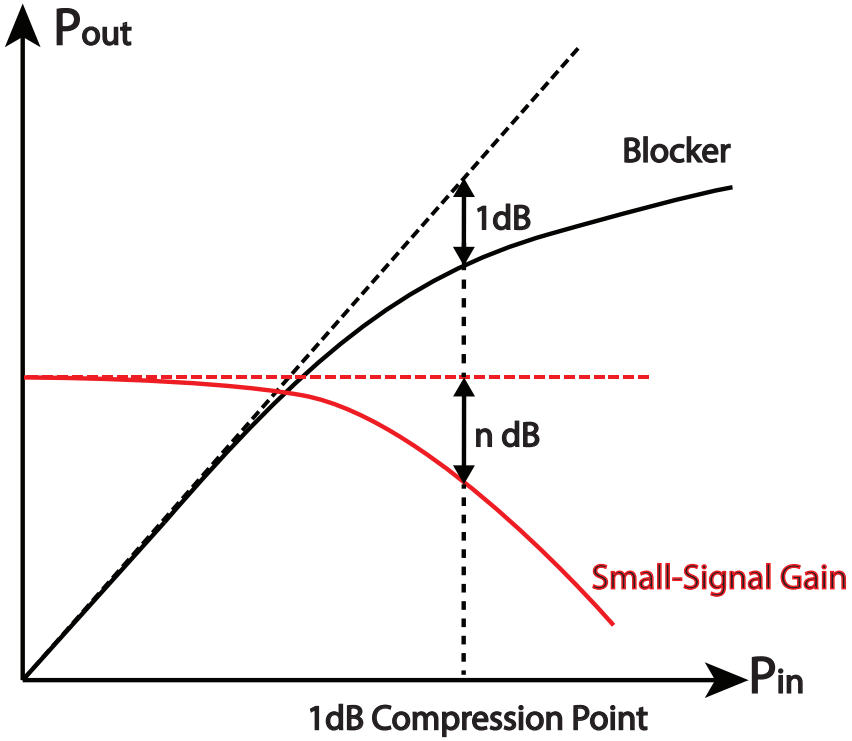

Figure 2.8: Desensitization

input signal in which the $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$. Calculating up to third order one would get:

$$y(t) = a_0 + a_1(x(t)) + a_2(x(t))^2 + a_3(x(t))^3 \tag{2.15}$$

Expanding this equation would result in component at fundamentals and also at $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. Products at $\omega_1 \pm \omega_2$ result from second-order nonlinearity (described by the coefficient a2) and are referred to as second-order intermodulation distortion (IMD2). Products at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ result from third-order nonlinearity (described by the coefficient a_3) and are called third-order intermodulation distortion (IMD3). Second-order distortion products at $\omega_1 \pm \omega_2$ are problematic mainly in Homodyne receivers. On the other hand, third-order intermodulation products are problematic in all the receivers regardless of their architecture since they can be quite close to the incoming desired RF signal in the frequency spectrum.

For fundamentals:

$$(a_1 A_1 + \frac{3a_3 A_1^3}{4} + \frac{3a_3 A_1 A_2^2}{2}) \cos(\omega_1 t) \tag{2.16}$$

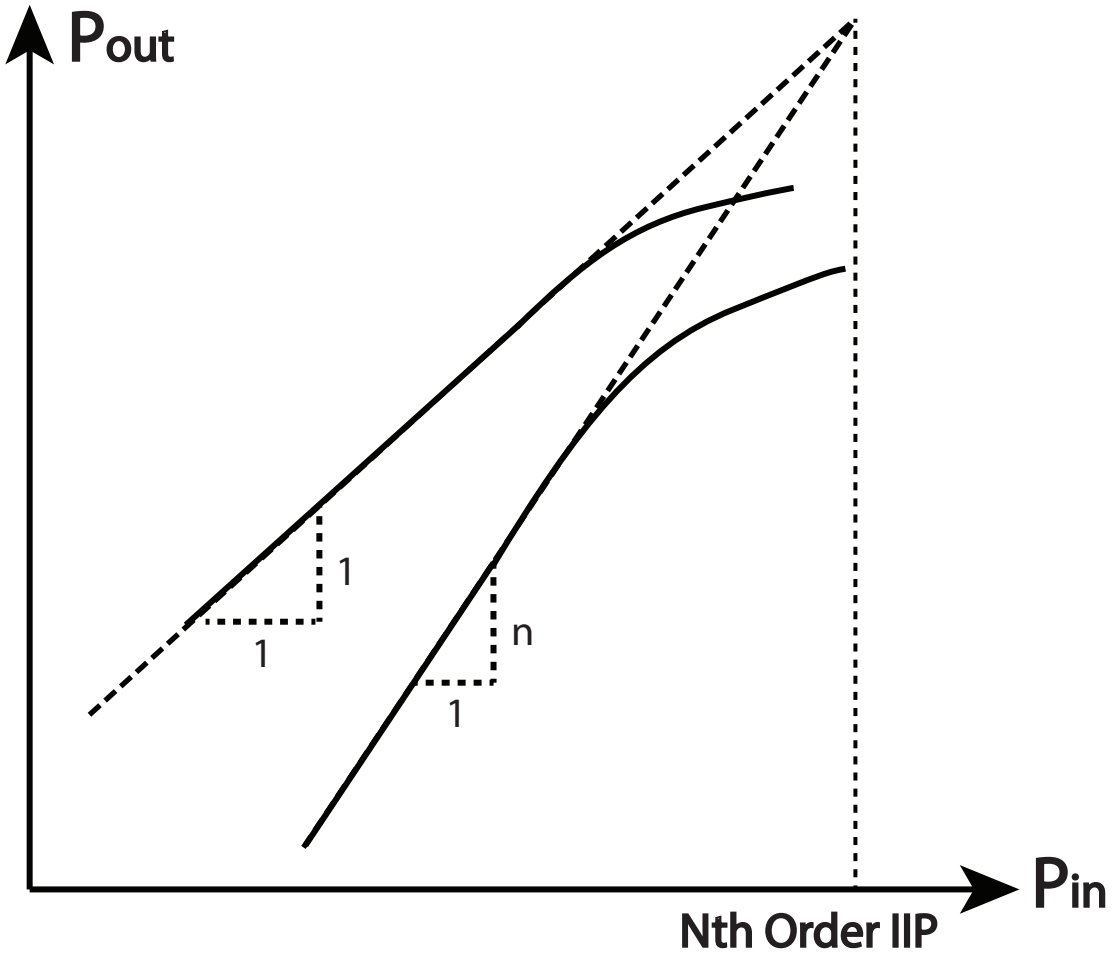

Figure 2.9: Intercept point

$$(a_1 A_2 + \frac{3a_3 A_2^3}{4} + \frac{3a_3 A_2 A_1^2}{2}) \cos(\omega_2 t) \tag{2.17}$$

$$a_2 A_1 A_2 \cos[(\omega_1 + \omega_2)t] + a_2 A_1 A_2 \cos[(\omega_1 - \omega_2)t] \tag{2.18}$$

$$\frac{3a_3 A_1^2 A_2}{4} \cos[(2\omega_1 + \omega_2)t] + \frac{3a_3 A_1^2 A_2}{4} \cos[(2\omega_1 - \omega_2)t] \tag{2.19}$$

$$\frac{3a_3 A_2^2 A_1}{4} \cos[(2\omega_2 + \omega_1)t] + \frac{3a_3 A_2^2 A_1}{4} \cos[(2\omega_2 - \omega_2)t] \tag{2.20}$$

N-th order intermodulation distortion is a useful metric in evaluating a system for its nonlinear behavior. The way to measure it is to inject a two equal tones close to each other

and set the amplitude such that the N-th order terms become visible in the spectrum. Then one can calculate the input referred intercept point at that given input signal with:

$$\mathrm{IIP_n[dBm]} = \mathrm{P_{IN}[dBm]} + \frac{\mathrm{P_{IN}[dBm]} - \mathrm{P_{IMD_n}[dBm]}}{\mathrm{n}-1} \tag{2.21}$$

Second and third order intercept point are the most importanct for wireless receivers.

Cross Modulation Distortion

Cross modulation is a nonlinear phenomenon in which amplitude modulation of one signal would transfer onto another signal due to odd-order nonlinearities.

$$x(t) = A_S \cos(\omega_S t) + A_B[1 + m(t)] \cos(\omega_B t) \tag{2.22}$$

$$y(t) = (a_1 + \frac{3}{4} a_3 A_L^2 [1 + 2m(t) + m^2(t)]) A_S \cos(\omega_S t) \tag{2.23}$$

The above equation shows that a distorted version of the AM modulation of the blocker signal has been transferred to the desired signal. Cross modulation is a very important metric in transceivers where both the transmitter and the receiver operate concurrently (full duplex system).

Dynamic Range

Dynamic range is the input signal level range the receiver can process with a specific quality. It's defined as the difference in power level between the 1dB compression point and the system noise floor.

$$\begin{aligned} \mathrm{DR[dB]} &= \mathrm{CP_{1dB,IN}[dBm]} - \mathrm{MDS[dBm]} \\ &= \mathrm{CP_{1dB,IN}[dBm]} + 174\mathrm{dBm} - 10\log(\mathrm{BW}) - \mathrm{NF[dB]} \end{aligned} \tag{2.24}$$

Chapter 3

Trends and Challenges in Wireless Receivers

3.1 Multi-Mode Operation: An inevitable Trend

System Point of View

In order to keep up with the market's need, the wireless service industries have started integrating more and more radios on one platform [58]. A state-of-the-art is shown in Figure 3.1. Evidently with increasing the number of standards and consequently front-end modules, this approach becomes bulky, costly and gradually impossible. [41, 34, 84] are a few examples of current designs in multi-standard radios. Figure 3.3 clearly shows the current trend which can be called evolutionary progress of wireless front-end design. It needs to be revisited and a so-called quantum leap is needed to realize a radio that can work from couple of hundred megahertz to a few gigahertz. For example, consider a radio that is supposed to work with the standards in Figure 3.2. Thus from system point of view, having a front-end which can support multiple modes of operation is in tremendous demand, a system which can be reconfigured to transmit and receive different waveform at different frequencies.

CMOS Point of View

In parallel, progress in the CMOS technology has gone a far way in the last decades. Transistors are getting smaller and faster and hence the computation power and the frequency of operation have gone-up considerably, allowing engineers to communicate and process data at an astonishing pace. However, how does that benefit (if at all) radio designers? One thing which should be considered is the drastic increase in the mask cost, Figure 3.4.

Figure 3.4 shows having low-power, small-footprint computing modules comes at the enormous increase in the cost of mask and fabrication facilities which can be considered non-recurring engineering (NRE) cost, [58]. At the same time, the issues which were not

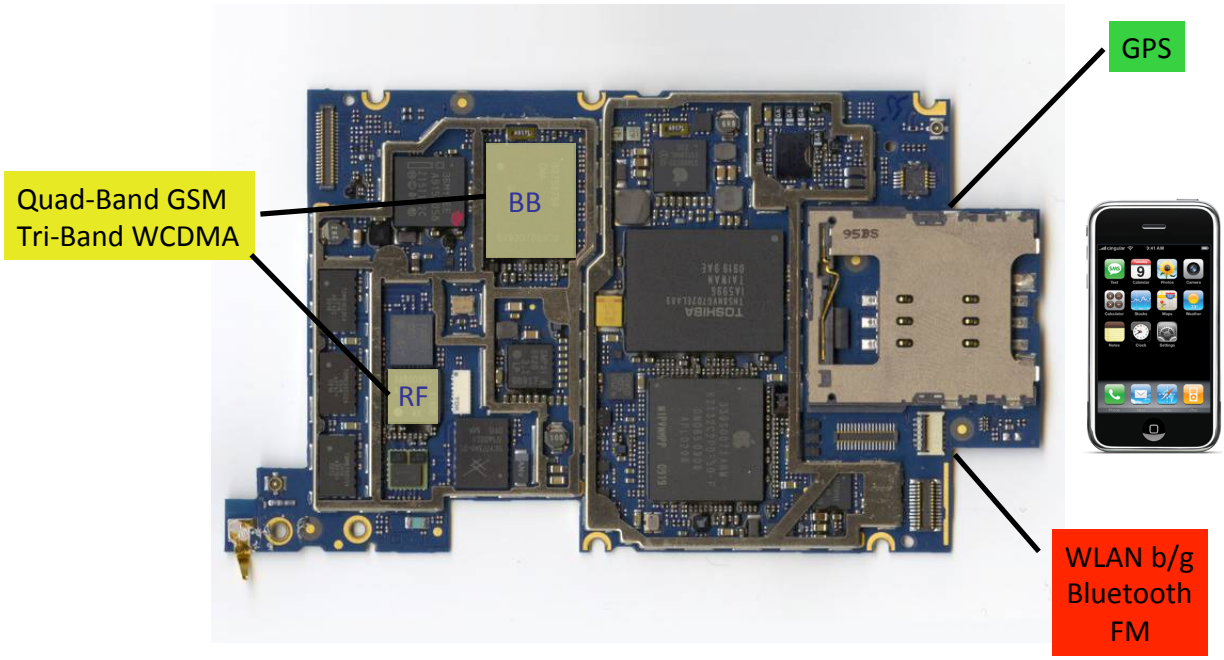

Figure 3.1: State of the art mobile handset. Source: isuppli

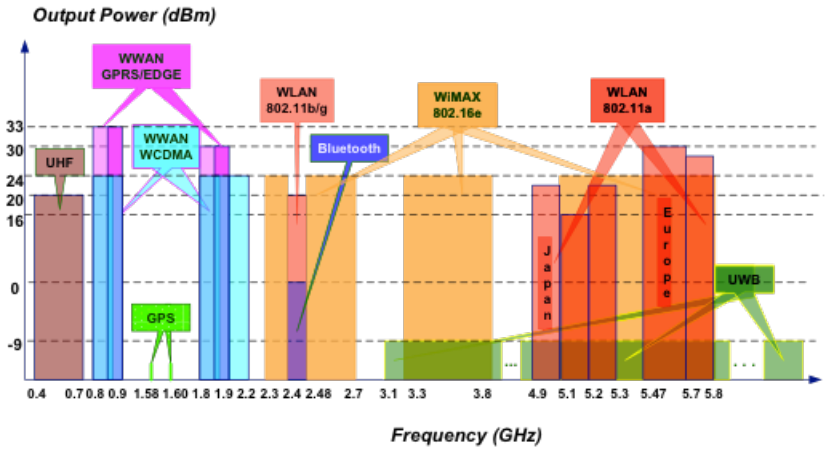

Figure 3.2: Frequency and power allocation for different standards

critical in the previous nodes get exacerbated with scaling, e.g. reliability and variability. This consumes more time of designers to get a robust design.

At the same time, cost per transistor is going down for logic, but for analog and RF cost per area is going up since passives don't scale with technology. Having in mind the cost of chip area and designer's time, the inevitable direction is to take advantage of the computation power available on the silicon. This concept has been around for a while under

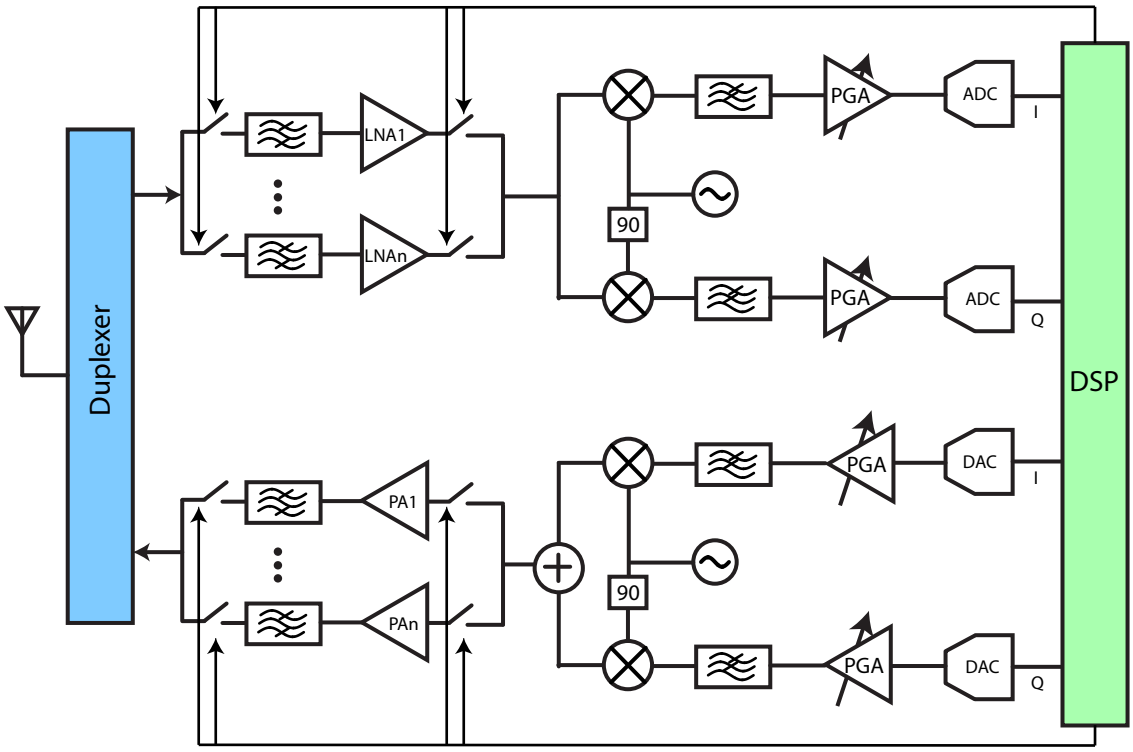

Figure 3.3: Typical multi-Standard transceiver architecture

the general category of software defined radios (SDRs) [53, 63, 12]. The general idea is to have an ADC in front of the antenna to convert the data into digital format and perform all the filtering and processing in the digital domain, or in the other way, change the mode of the module with software. Yet, there are extremely challenging issues to solve in the RF circuits before getting there [67, 58, 64, 66, 65].

Software Defined Radios

As it was discussed in the previous section, the natural way of thinking about the future of the wireless architectures is to have a flexible hardware with the capability of being reconfigured based on the required scenario. How does reconfigurability benefit the wireless industry?

Other than the form factor discussed above, cumbersome design iterations for achieving required performance would be diminished. To emphasize the importance of this phase, one should consider the vast amount of time designers should spend to tweak their modules to meet the required performance over the process corners. This task keeps getting harder and harder as the technology shrinks due to more complicated devices and more variabilities.

Hence the motivation for having the same infrastructure which can be re-tuned is rather

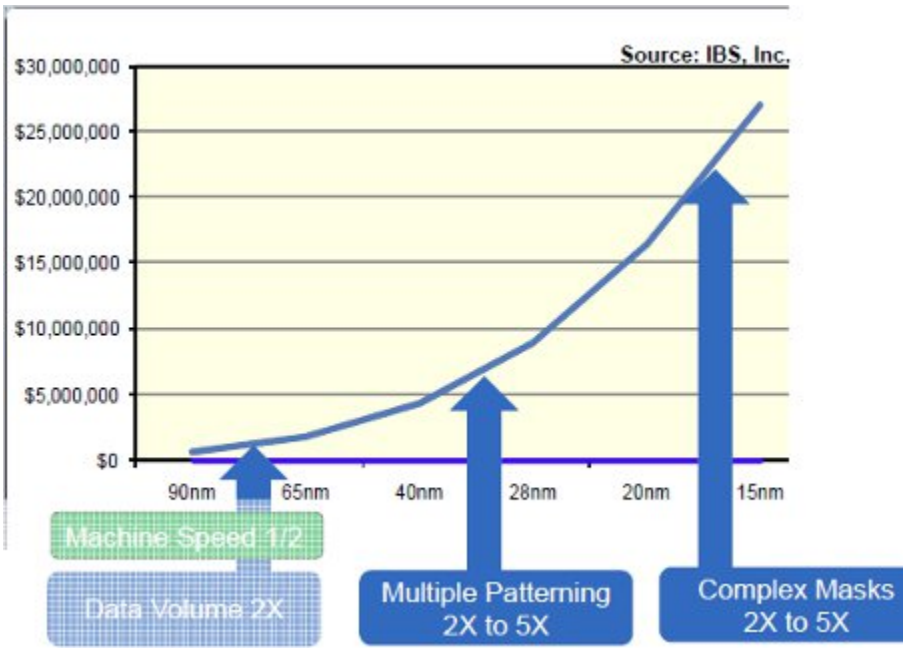

Figure 3.4: Mask cost versus process

high for service providers that are facing monthly updates on the standards. This is not the first time the electronics industry is going through this phase. As the quest for computation was rising, dedicated logic gates seemed an implausible approach and the trend tilted toward arrays of programmable gates (FPGA) so each customer can program the logics for the specific applications. Of course the performance would be lower than the dedicated designed logic, but after a certain threshold, expandability is by far the mot important issue to be addressed.

The benefits of incorporating such front-ends does not stop there. The other crisis the limitation of spectrum. The figure below shows the current allocation of the spectrum, showing that there is barely any room for new bands. There are two solutions for opening the new bands. One is to release spectrum, e.g. President Obama signed an order in 2010 to release 500MHz more spectrum. However, the allocated spectrum is not under constant use. Figure 3.5 shows the spectrum usage as a function of time.

Clearly if one could have the option of detecting the unused portion of the frequency spectrum and hopping to that slot, that would free a vast domain of spectrum for the users. The very idea of SDR can embed this functionality.

The question to be answered is considering all the benefits, why SDRs have not paved their way to the market yet [21]?

There are a few reasons ranging from management to technical levels. Among the technical levels, perhaps the most challenging part is the filtering requirements. This issue is even worse for modules implemented in the newer technologies.

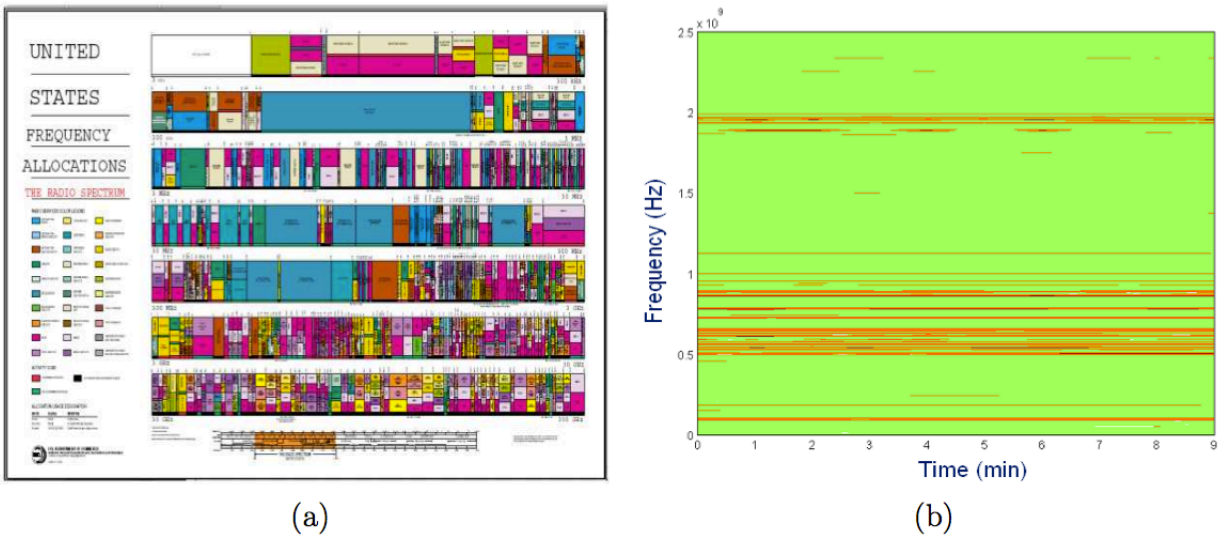

Figure 3.5: CC spectrum allocation and the measured usage at the Berkeley Wireless Research Center. The measurements were performed in the 0-2.5GHz frequencies over a period of 10 minutes, [52]

Removing the filter will let the signals from the entire spectrum enter the system. Having in mind these systems are designed for typically retrieving the very weak desired signal, there are a few fundamental issues that potentially can hinder the above-mentioned functionality.

Looking at Figure 3.6, one can summarize the issues due to receiving strong jammers at the input of this time-varying system:

- A very strong jammer can saturate the receiver and prevent it from processing further signal in the spectrum. In the extreme case one can imagine a jammer that rails-out the receiver blocks. Also this issue exacerbates as the interferer signal gets closer to the channel since the gain of the chain is maximized for that particular band. The more typical scenario is the increase in the minimum detectable signal due to lower gain if the system.

- Reciprocal mixing is the other problem which is quite fundamental. When a jammer enters the receiver, even if the modules are designed to tolerate that power level, the frequency shifting action can still impose serious limitations on the blocker handling. Since with today's technology still the received signal should be down-converted to be be digitized with reasonable power consumption, there should be a oscillator to perform the task. The desired characteristics of that module is to generate a single tone in the frequency spectrum. However, the non-ideality of the block which is characterized by phase noise will cause other parts of the spectrum to be down-converted on top of the

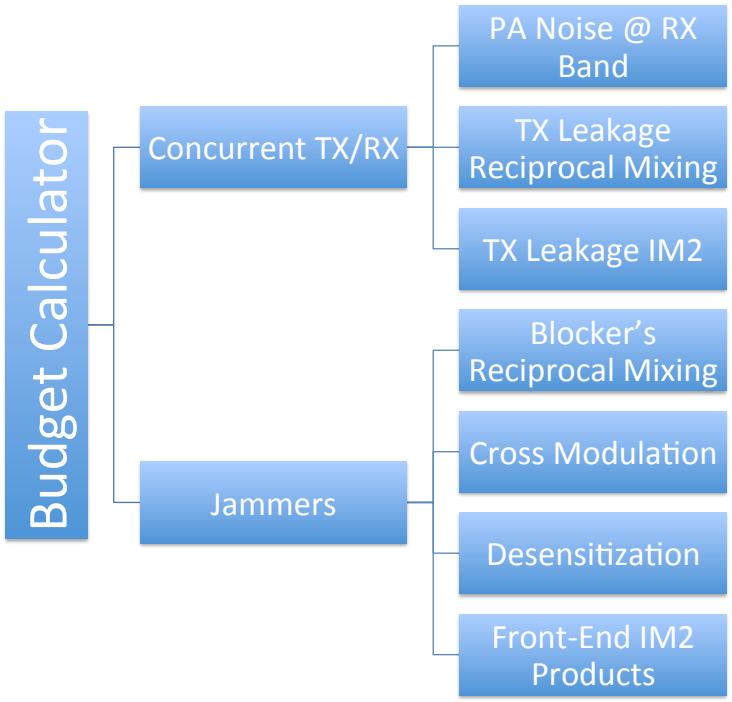

Figure 3.6: Budget calculator for wireless receivers

desired signal. There are two regions which is quite sensitive. close to the desired signal and the regions around harmonics of the oscillation frequency. The latter is not a big concern once the carrier frequency is in the GHz range. Since the third harmonics falls couple of GHz away from the desired band and it will get attenuated by the passive filtering.

- Other than the saturation that can happen for any system, the receiver is a time-variant system which means the output signal frequency can be a linear function of the input frequencies. Now if the arrangement of blockers are such that the linear function of the jammer frequencies fall on top of the desired signal, the signal to noise ratio (SNR) would be degraded. The difference between these scenarios and the above mentioned one is that for the latter to be effective, the power level of the blockers should not necessarily be high to impact the performance whereas for the former, since there is no information at that specific frequency, the power level becomes important in the picture.

3.2 Tackling the Problem; ON Chip or OFF Chip?

As mentioned in the previous section, for realizing software-defined-radio, perhaps the most cumbersome barrier is the existence of blockers. For example, covering the frequency band

Figure 3.7: SAW Filters

of operation up to 6GHz is not a challenging task with today's technology. The fundamental question to be answered is what are the options for dealing with this challenge?

The answer varies based on the required form factor, cost, etc. Generally the solutions can be categorized into the on-chip vs off-chip components. One school of thought, which is quite dominant over the past decade, is that everything should eventually be on CMOS.

On the parallel path, there has been a huge progress in the field of integration of heterogeneous systems. The advantage of using such devices is the unprecedented quality factor which can never be achieved in the pure CMOS technology.

OFF CHIP SOLUTION

- Surface Acoustic Wave (SAW): SAW devices are used as filters, resonators and oscillators and appear both in the RF and IF (intermediate frequency) stages of present cellular handset designs. Their size is about few mm^2 though which is a fundamental bottleneck for having too many of them on one platform for having multiple band of operation.

- Bulk Acoustic Wave (BAW): BAW filters are electromechanical devices which operate at frequencies from around 1 to around 15 GHz. BAW filters are smaller than microwave ceramic filters and have a lower height profile. They have better power handling capability than SAW filters and achieve steeper roll off characteristics. A typical BAW duplexer takes up a footprint of about $5mm$ by $5mm$ which again poses the same issue as SAW counterparts introduce.

- MEMS (capacitive transducer) are also being suggested as potential replacements for off-chip filters. The idea of using micro electro-mechanical resonators has been the sub-

ject of academic discussion and academic/industrial research for almost 40 years. The problem with realizing a practical resonator in a MEMS device is the large frequency coefficient of silicon, aging, material fatigue and contamination. A single atomic layer of contaminant will shift the resonant frequency of the device. Also the other main issue with these resonators which seem to be fundamental, is the power handle-ability of these resonators. If one wants to increase the frequency of operation, the geometry of these devices should be scaled down. That would reduce the power handling as it will be explained below. The fundamental mechanism of operation of these devices is having a time-varying capacitor and extracting the current out of that.

$$i_{out} = \frac{d}{dt}(CV) = C\frac{dV}{dt} + V_{DC}\frac{dC}{dt} \tag{3.1}$$

Where the second term in Eq. 3.1 is the current picked-up by electrodes. The capacitor in the MEMS structures is time-varying based on the input voltage. $C \propto \epsilon\frac{A}{d}$. If the dimensions of these devices scale down, the gap between the electrodes would get smaller (d) and as a result, the high power signals can cause the mechanical system to enter the non-linear regime and in the extreme case, the resonator plates can collide. This issue is quite serious since one is using these filters to knock-out the high power jammers that the electronic systems can not tolerate. But at the same time these devices seem to work great for low-power interferences which are not a bottleneck and yet they are having a hard-time processing the strong jammers.

ON CHIP SOLUTION

The fundamental question to be addressed is if the holy grail of the wireless systems is being flexible multi-standard, what is the extent that one can benefit from scaled CMOS? How does that change with scaling?

What mechanical filters do is remove the blockers right after the antennas. Then the remaining blocks are responsible for processing the desired signals and in-band blockers which have profiles carefully engineered according to the standards. Consequently from the system point of view, it's manageable to allocate the design metrics for different building blocks for meeting the required dynamic range. That is the minimum detectable signal which sets the gain and noise figure, and also being able to tolerate the maximum power level entering the system, which is one of the dominant factors in the power consumption.

The most desired solution is to put the electronic block designed to perform the filtering function in front of the antenna. Depending on the type of the filter, in series or shunt with the front-end. The approach has been pursued [47], however, there are two critical issues which should be taken under careful considerations:

- Noise: As explained by the cascaded noise figure equation, the reason designers traditionally put the low-noise-amplifier (LNA) blocks in the beginning is to suppress the

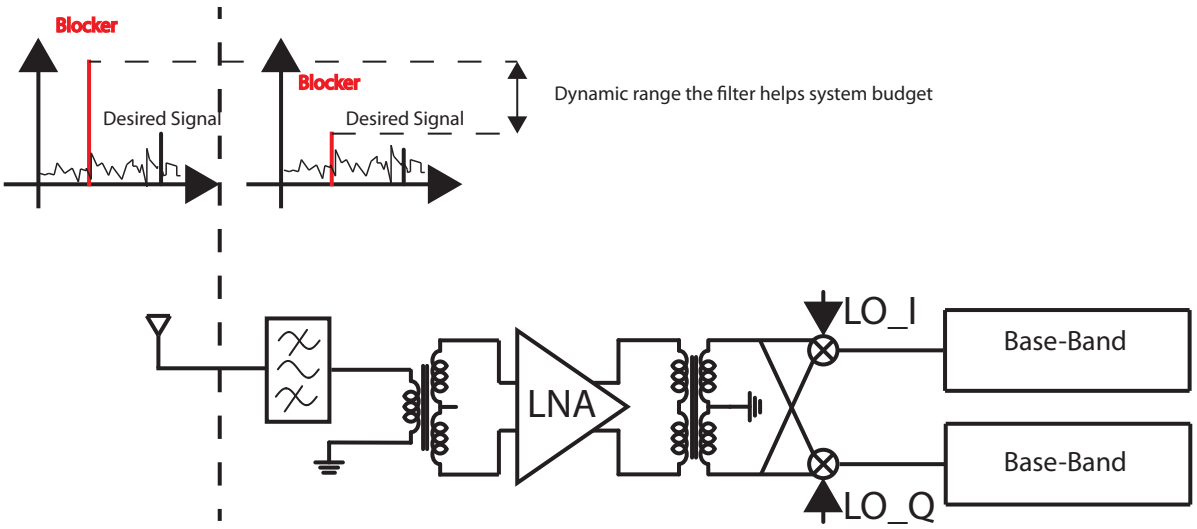

Figure 3.8: Filter function for blocker removal

noises added by the consequent blocks which are in charge of frequency translation, further filtering and amplification and finally digitizing. The LNA plays a vital role in retrieving the minimum detectable signals. Now by adding an electronic block BEFORE the LNA, one might get the desired filtering characteristics, but the amount of noise that would be pumped into the receiver is usually unacceptable. Why this is not an issue for mechanical filters? Well, to some extent it is. One can model these filters with equivalent electrical model of resistor, capacitive and inductor. The important point is they can demonstrate high quality factors not achievable with electronic components. However, since L and C do not have noise, the only noise source is the resistive part and actually they do hit the performance by a few dB. However, one needs not worry about a lot of different noise mechanism in CMOS like channel noise, reciprocal mixing due to phase noise and the harmonics of the oscillators etc.

- Linearity: Probably the harder problem to tackle, is designing electronic blocks that are functional for high power signals. In the designing phase, one would carefully bias the transistors in the right regime and carefully connect devices together to get the required performance. If the block is supposed to process a high power blocker, the different nodes in the block start to fluctuate and consequently transistors would come out of their desired operating points and as a result, the performance would deviate from the designed phase. On the other hand, scaling the CMOS technology is reducing the dynamic range available to designers as the power supply is shrinking at the same time. This makes designing such blocks much harder in the advanced nodes.

Maybe the other way to look at this issue is to ask when can we deal with blockers? Or

the other way to put it, when it's not too late?

Filtering before the LNA

The two problems to tackle is how to design a block which can do the filtering without increasing the noise-floor significantly. At the same time the block should be able to manage to keep the performance while processing large signals.

Filtering after the LNA

As explained above, the fundamental issue is when the blockers are entering the carefully designed LNA, the noise floor and the gain would drop and rise respectively and hence the noise floor of the system would increase significantly causing the loss of dynamic range. There are extensive techniques [86, 8, 15, 6, 17, 14, 85, 69, 44, 29, 25, 39, 42, 7, 45, 18] which can be utilized to squeeze as much of linearity as possible from the LNAs, however, the techniques are process-temperature sensitive and at the same time they are not suitable for high power blockers.

Filtering after the mixer and before digitization

At this stage, other than the issues mentioned above, another fundamentally limiting mechanism would happen. Suppose the mixer which is the block in charge of the frequency translation is linear enough so it would not introduce additional non-idealities when the input signal is high power. It's a reasonable assumption if one adopts a passive configuration. However, there are three terminals for the mixer and the bottleneck is the third port which is fed by the oscillator. The two dominant issues regarding this port while the block is processing jammers:

1. The blockers that fall on top of the odd harmonics of the reference clock. Since the mixing action basically is forcing the signal to toggle between path A and B, mathematically it's a pulse train. Hence by looking at the Fourier transform of the pulse train, one can see that there would be components at the odd harmonics of the reference clock and if there are jammers at those frequencies, they would be down-converted and fall on top of the desired signal. There are different techniques, [70, 13, 79, 16, 61], to reject the harmonic down-conversion and they're quite effective. Also this is less of an issue if the operation is at GHz regime since the harmonics are couple of GHz away and passive attenuations alleviate the issue.
2. The close-in blockers prove to be much more difficult to handle when it comes to the non-ideality of the local oscillator. Phase noise would cause the spreading of the tone of the reference clock and hence the energy in the near frequencies is considerable. If there is a signal in the near-by frequencies, they can be down-converted on top of the desired signal. This phenomenon is called reciprocal mixing [67] and it's a critical factor in system level planing for handling the blockers.

Since even if one designs a perfect LNA that can handle ANY signal level, this phenomenon would bury the desired signal under the high power jammers. The issue gets exacerbated by acknowledging the fact that based on Leeson's equation [43], the phase noise is fundamentally limited to the quality of passives. That means if one wants to avoid using heterogeneous integration, the reciprocal mixing is a fundamental limitations on the maximum power in close-in signals that wireless receivers can handle.

Chapter 4

Review of State-of-the-Art Wireless Receivers

For the reasons mentioned in the previous chapter, current state-of-the-art solutions incorporate several external filters and duplexers to alleviate the noise and linearity issues imposed by signals and noise outside the band of interest. Figure 4.1 shows an example of quad-band GSM/EDGE and tri-band WCDMA which is using 10 SAW filters, 3 duplexers and several matching network components [23]. Other than the obvious cost and size implications, the front-end partitioning by these components opposes the idea of flexibility which is the ultimate goal. Hence in this chapter we will review and analyze the current proposed solutions for removing the filters and dealing with blockers with on-chip approaches. It's worth mentioning the emphasis is on the techniques that achieve filtering in the RF domain since doing so in base-band means RF blocks should still tolerate the jammers and doesn't pave the way for SDR realm. Another thing to note is that these approaches should all have the assumption of not having the copy of the jammers. For example in case of concurrent operation of TX/RX, [9, 38], the copy of the blocker is available and can be deployed in the cancellation schemes.

4.1 Spatial Filtering

The original use of multiple antenna in wireless systems was to enable sending independent data on each channel and increasing the throughput of the physical media. In receivers multiple antennas are also being used to counteract the multi-path issues. However, the same architectures can be used to do the spatial filtering, exploiting the fact that the desired signal and the interfering signal come from different angles. Then from the Figure 4.2 one can derive the phase difference between antennas 1 and 2 as:

$$2\pi\frac{d}{\lambda}\sin(\theta) \tag{4.1}$$

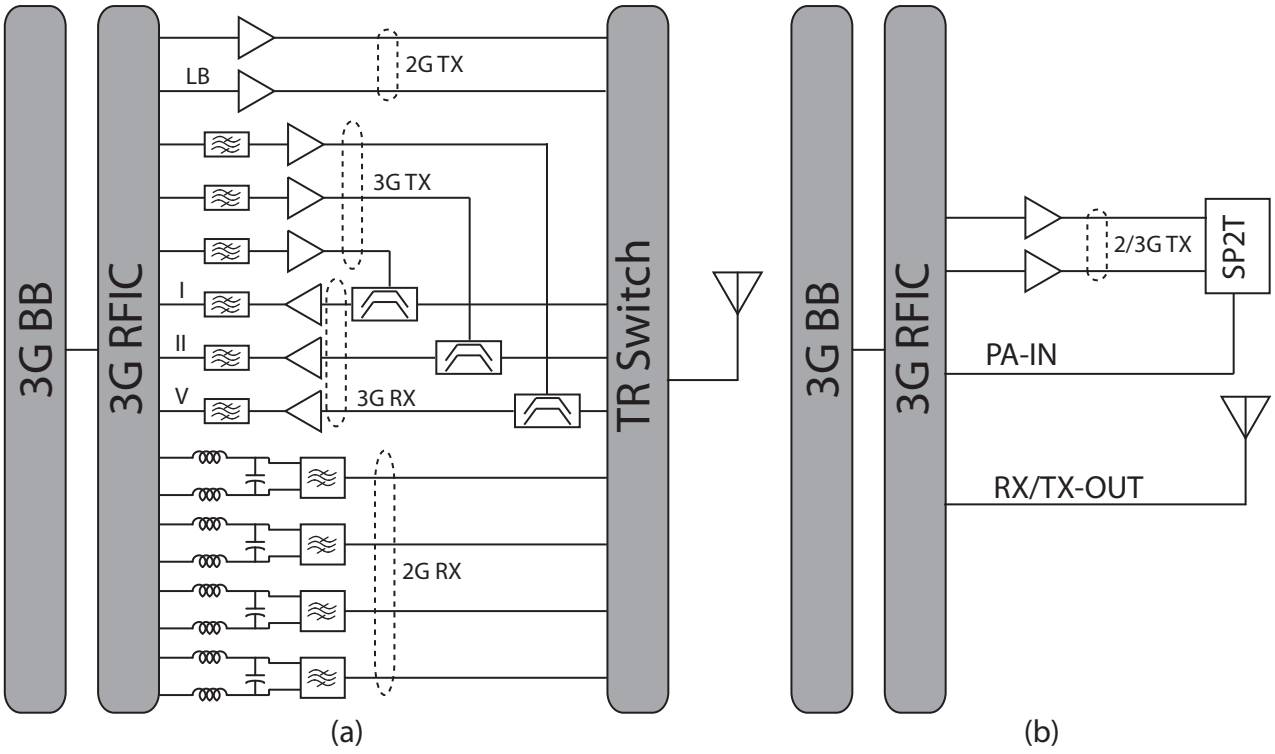

Figure 4.1: Current (a) and future (b) architectures of 3G receivers [23]

Since the desired signal comes with the angle of θ_1 and the interference comes with the angle of θ_2, [57] shows that by using channel estimation techniques one can get the direction of the desired signal and cancel N-1 jammers with N antenna elements.

There are two issues that make this approach quite unattractive for cellular domain. First and by far the more important one is the use of multiple antenna is prohibited for SDRs since the increase in form factor contradicts the purpose of removing the SAW filters. Secondly, it is not a wide-band solution since the cancellation is a function of $\frac{d}{\lambda}$ and λ is quite large in low-frequency regimes. The other subtle problem arises from the phase-shifting requirements in the system which can be done either in the RF or base-band. If it's done in the baseband, that would mean the RF blocks should process the jammers and there is no blocker power alleviation for them, and wide-band phase shifting in RF is not an easy solution [75].

4.2 Translational Loop Filters

The idea of translational loop filters is to replicate the blocker at one path and then subtract it from the main branch so from then on; the system front-end and dependencies on the cancellation mechanism can be categorized in two subcategories.

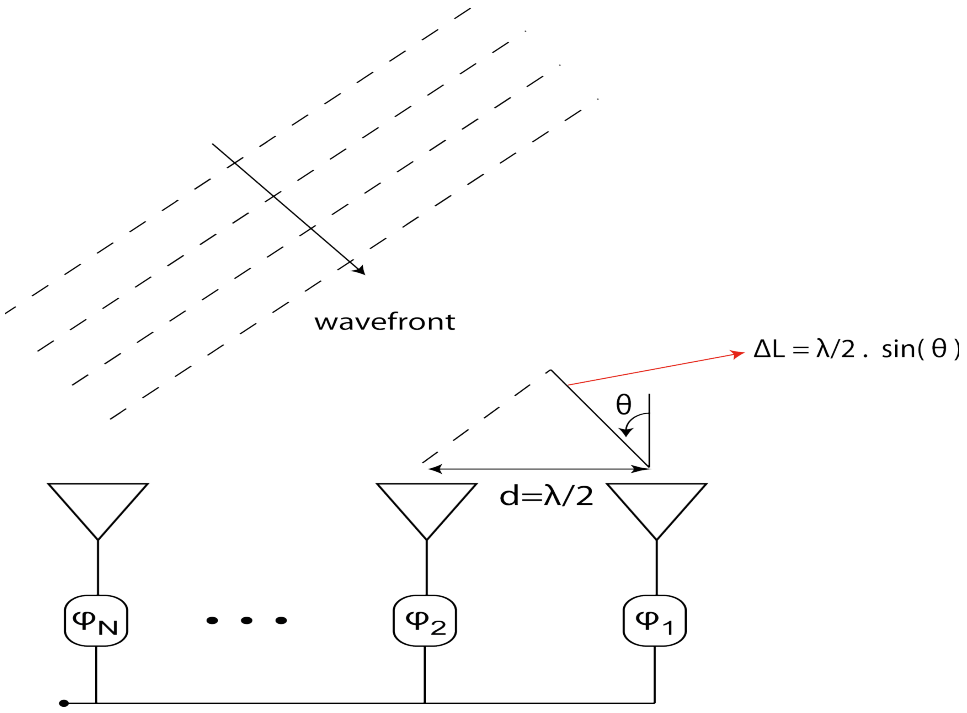

Figure 4.2: System diagram of incorporating multiple antennas

Feedforward Cancellation

One solution is to divide the incoming signal from the antenna into two branches and subtract the blocker at the output of the LNA. This approach has been pursued in [30, 10, 22, 72]. Basic idea is to copy the incoming signals, remove the desired signal and subtract the remaining at the LNA output. The first question one should ask is why go through all the trouble? The answer comes back to the limitation of passive quality factors. The Q is not good enough to be able to remove the blockers at front-end. So how does this technique bypass this limitations? First the incoming signals will be down-converted, pass through a high Q base-band filter to remove the desired signal and then it will be subtracted at the LNA output. Since the filtering is done at the base-band, the effective quality factor is much better. But that doesn't come for free.

The availability of quadrature LO signal in the receiver makes it easy to implement a notch in the single side manner.

However, this approach suffers from number of issues:

Matching Requirement There are two paths, the main and the auxiliary, and since the cancellation mechanism is feedforward, there is no procedure for fixing the residual errors and hence the cancellation is a huge function of matching between the path. Both a) gain and b) phase prove to be very important factor in the amount of attenuation

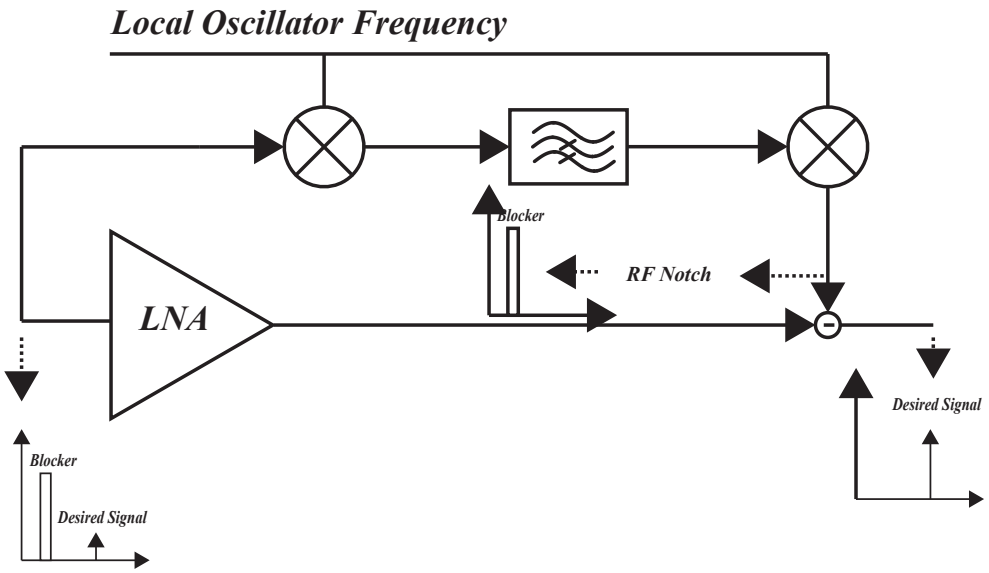

Figure 4.3: Feedforward scheme for blocker removal in receivers

one would get.

Noise Performance The other fundamental issue that is always of concern is the noise added to the system. Every new function added to the system degrades the noise performance, specially if the block is placed in the first stage. However, two factors helps designer for such blocks. First is the fact that these blocks can be turned-off if there is no blocker which can be monitored, and the second is the higher NF constraint once there is a blocker entering the system. For example in 3GPP, the noise figure limit when there is blocker is 15 dB [49].

Feedback Notch Filtering

This approach has been pursued in [72, 80, 81] and the very feature that makes it very interesting is that there is no need to control the gain and phase of the loop as long as the feedback is stable. However, this approach shares the other issues the feedforward solution has and on top of those, it suffers from stability, a problem that all the feedback systems have, but one which is harder to solve in the RF regime.

Positive Feedback Translational Loop

This solution has been pursued in [37, 36] and has some interesting characteristics. The idea is to down-convert the blocker and the desired signal, filter out the desired signal and subtract the blocker at the input of the LNA. The loop is positive feedback to enhance the

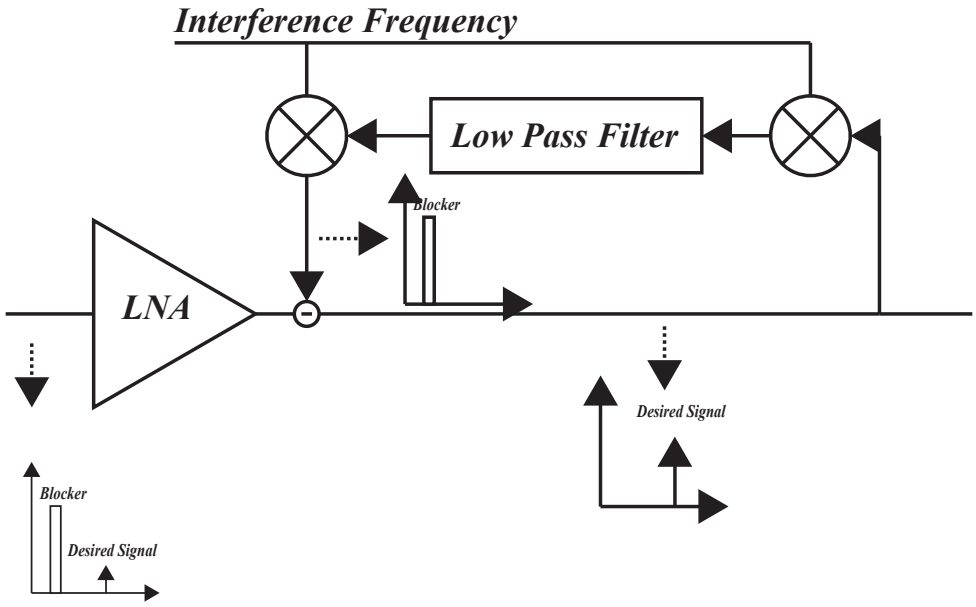

Figure 4.4: Feedback scheme for blocker removal in receivers

sharpness of the filter. Cancellations at the input of the LNA which saves the LNA from high dynamic.

However, there is a time-delay in which the LNA should process the signal in order to get the loop up and running. Doing so the impedance seen from the antenna would be:

$$Z_{IN} = \frac{Z_{LNA}}{1 - \frac{Z_{LNA} * G_{BPfilter}}{K}} \tag{4.2}$$

in which the K is set such that $\frac{Z_{LNA}}{1-\frac{Z_{LNA}}{K}} = Z_{Antenna}$ so the in-band signal is matched and the out-of-band is going to be attenuated by:

$$AT(dB) = -20log\left(\frac{Z_{IN}}{Z_{ANT} + Z_{IN}} * \frac{Z_{LNA} + Z_{ANT}}{Z_{LNA}}\right) \tag{4.3}$$

However, the stability of the system is based upon the value of K and there should be a good control over the value of the K. Other factor one should consider is that the amount of attenuation is proportional to the input impedance of the LNA and the lower it gets, the more attenuation is achieved. However, extremely low input impedance would translate to noisy power-hungry block which is not a good candidate for cellular applications.

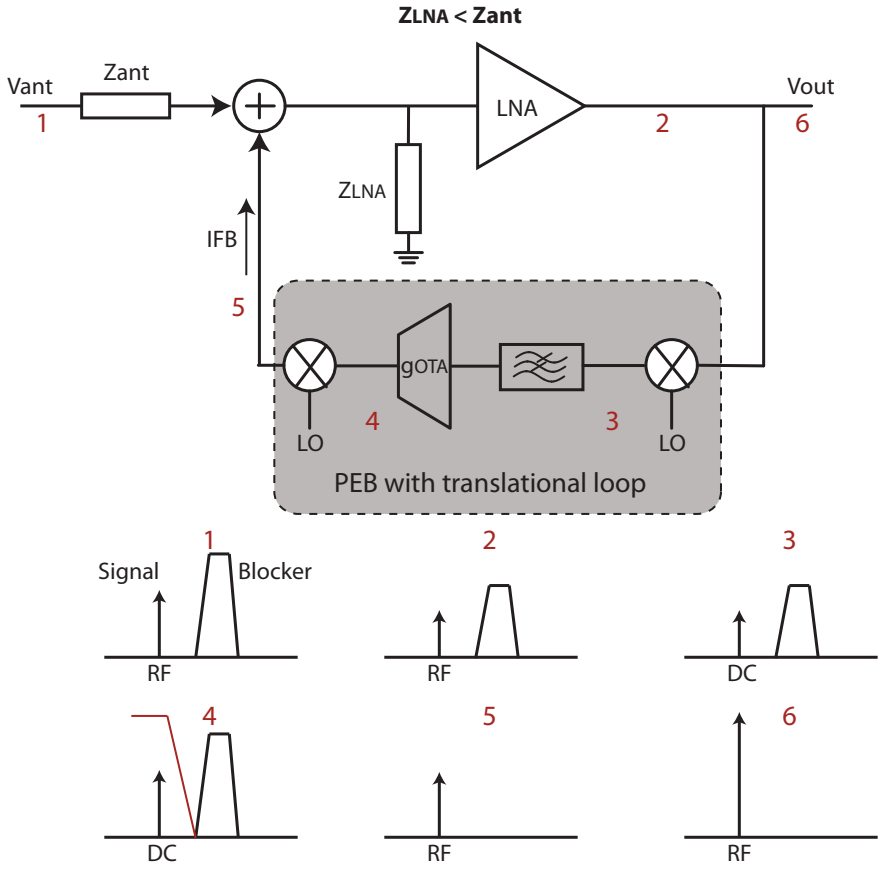

Figure 4.5: Positive feedback translational loop [36]

4.3 Q-Enhancement Techniques

Q-enhancement filters are basically using the fact that one can see negative resistance looking at the cross-coupled pair with positive feedback loop. Since Q is inversely proportional to the resistive losses, the negative impedance increases the Q and hence the selectivity [73].

Looking at Figure 4.6, there are a few factors that should be pointed out. First is the fact that the positive feedback scenario makes it sensitive to oscillation and there should be a calibration circuitry to monitor that section. Perhaps the more important fact is the nonlinear behavior of this approach. The performance is a function of exact magnitude of the impedance of the cross-coupled pair and due to large-signal behavior of the transistor, that's a function of the input power. On top of this, one should consider the noisy behavior of this approach which made the designers put the block after the first stage of the LNA. Overall, this might be a good architecture when dealing with low power signals in the GPS and assuming there is a SAW filter in the front-end, but doesn't prove to be attractive for

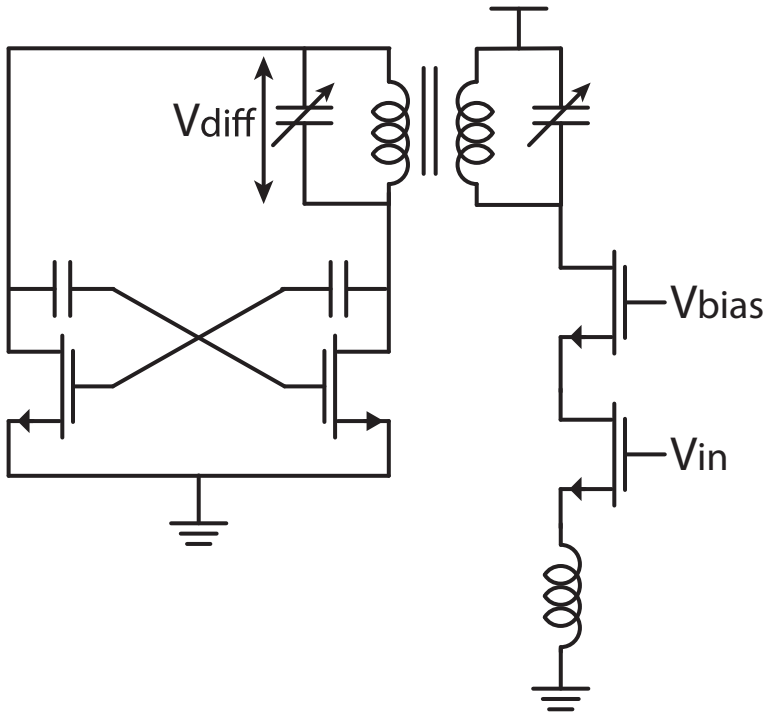

Figure 4.6: Q-Enhancement architecture

cellular domain.

4.4 Mixer-First Approach

This solution uses an intuitive and contradictory approach. If the LNA starts entering nonlinear regime with strong jammers, and amplification of the jammers would cause the following blocks to saturate as well, then why not get rid of the LNA and start with the mixer?

To remind ourselves, the very first reason designers had to use LNA was to bring-down the minimum detectable signal power, as can seen from cascaded noise figure equation. It wasn't intended for boosting up the signal for ADC since that could be done just before the ADC in the IF domain. Now what would happen if one removes the LNA? With older technologies that would have created excessive noise figure for the system as the frequency convertors were extremely noisy. With the advances in technology, CMOS switch performance gets better and better. They become faster and for the same overdrive voltage, their resistance gets smaller. From the circuit aspect, there have been many works [50, 51, 40] supporting the fact that exploiting passive mixers leads to superior noise and linearity performance. Having all this, recent demonstration of LNA-less or Mixer first architectures [20, 4, 5] have

shown superior performances.

Even with state-of-the art technology, for the mixer switches to become low-noise, they ought to be sized large enough for reasonable noise performance since they are the first block in the system. So now the issue is two fold:

- The power consumption of the LO buffers becomes the dominant energy sink in the system. The issue would be exacerbated in the multi-phase systems for harmonic rejection. One can argue eliminating the LNA has opened more budget to burn in the buffers which is true to some extent.

- One subtle point which is the case in all the systems incorporating passive mixers but is of much more concern in the mixer-first architectures is the amplification of the base-band noise due to time-variant nature of the system.

  Looking at the Figure 4.7 one would see the amount of the noise contribution due to the base-band will be:

$$V_{n,out} = V_{n,amp}\left(1 + \frac{R_{FB}}{R_{IF-RF}}\right) \tag{4.4}$$

  Figure 4.7 shows the contribution from base-band noise is dependent on the impedance one would see looking at the mixer from base-band, which can be obtained as:

$$Z_{in} = \frac{1}{4\pi F_{LO} C_{par}} \tag{4.5}$$

  Eq. 4.5 is based on the assumption that the resistive impedance at the RF side is large enough not to discharge the capacitor in one clock cycle considerably. So what will happen is that as the parasitic capacitance increases due to sizing-up the mixer, this resistor gets smaller and hence the noise contribution from base-band will increase.

  However, what makes this base-band noise contribution very important is the LO waveforms. If there is an overlap between the consecutive LO cycles, then the impedance seen from base-band to RF will be dropped significantly and hence the noise contribution from the base-band will start to dominate. On the other side, there is a trade-off between the linearity and noise performance. The reason is simple. If there is no overlap, there would be times when the input RF signal would see no path to the base-band and hence a high impedance path. So if there is an LNA, it would see a high impedance load which degrades its linearity performance.

  For the case of mixer first, this issue is less of a concern since there is no LNA and one would rather not to have any overlap. However, due to relatively large size of the switches, it's not easy to control the overlap regions of the clocks.

  Also, the other issue in the mixer first, is low-impedance at the RF side seen from base-band. In traditional designs, on the RF side of the mixer is an LNA with relatively

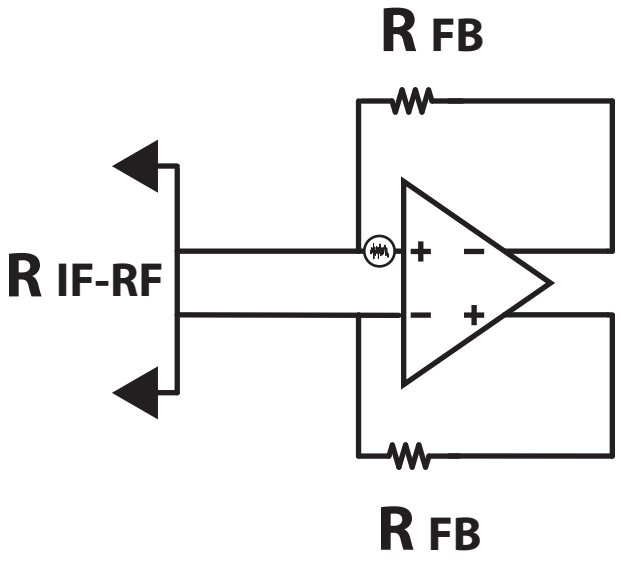

Figure 4.7: Baseband noise amplification

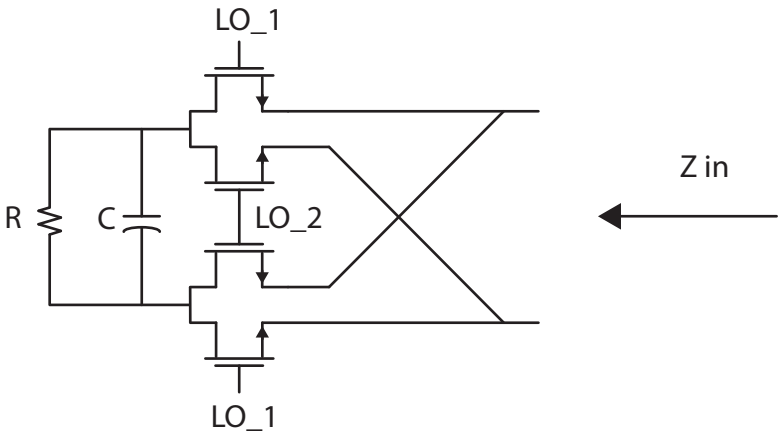

Figure 4.8: Impedance seen by the base-band looking at the RF side

large input impedance. In mixer-first architecture however, the impedance at the RF side of the mixer is antenna's impedance which is 50Ω. And hence according to Eq. 4.7, the base-band noise will be of higher concern.

Overall, the mixer-first approach seems very promising and scaling-friendly since the quality of switches gets better and better. As far as the antenna impedance is of concern, there are discussions [1] to increase the impedance to few hundred ohms which

is going to help the mixer-first. The fundamental issue with increasing the antenna impedance will be higher Q of the antenna and being more sensitive to routing which can be a killer in cellular phones as the routings change from one version to another.

4.5 Injection Locked Interference Copying and Cancellation

This approach which has been pursued by [78] the idea is to have a copy of the antenna input in which the desired signal is removed from the copy and then to subtract the result at some node in the receiver. So the basic idea is familiar and it's the one translational loop filters are meant to do. The way those filters achieved the high enough quality factors to remove a relatively close signal at that frequency range was through down-conversion and exploiting the base-band filter characteristics. In this approach the high-Q filter is achieved through a positive feedback system, i.e. injection locked oscillator, Figure 4.9.

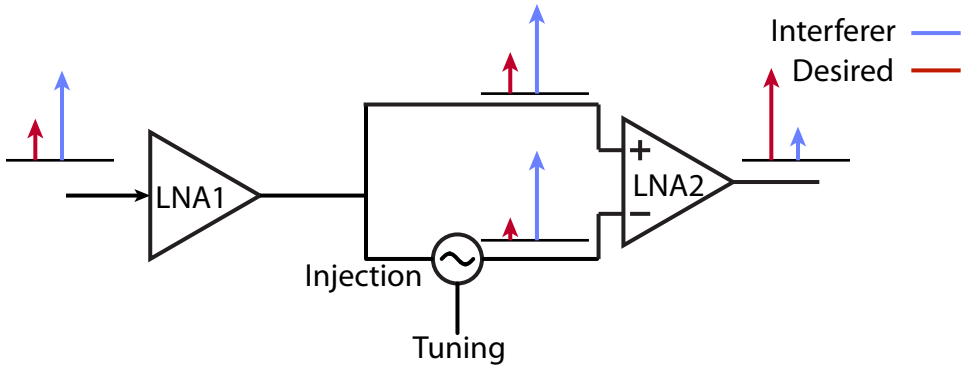

Figure 4.9: Exploiting injection locked oscillator in interference cancellation [78]

The notch filter is implemented through using a PLL in the injection locked oscillator (Figure 4.10). Using a PLL would allow tracking the phase of the blocker signal which proves to be very important once the signal is changed from CW tone to modulated one. Then using the PLL would allow the notch to be broadened so as to remove the whole blocker. First the LNA amplifies both desired signal and the blocker, the output of the first one branches out to the second LNA and injection locked oscillator and then to second LNA. Hence, with proper gain and phase alignment, the second LNA only sees and amplifies the desired signal.

As far as the for the core of the injection locked oscillator, a cross-coupled pair with the injection port is designed, Figure 4.11, incorporating a bank of capacitors and varactors for coarse and fine tuning. The locking range of the injection locked systems is [62]:

$$\omega_{LR} = \omega_0 \frac{I_{inj}}{2QI_{osc}} \tag{4.6}$$

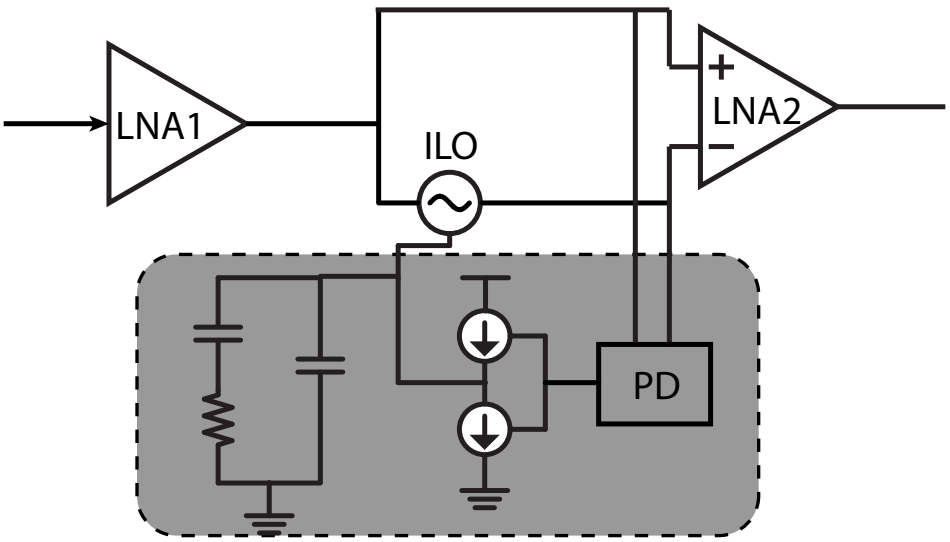

Figure 4.10: Circuit diagram of the injection locked oscillator

In which I_{ing} and I_{osc} and Q are injection port, core oscillator and the quality factor of the tank respectively. In order not to lock to the desired signal, the locking range is set to rather a low range and hence if this block is supposed to work on broad range of frequencies, the ω_0 should be able to get calibrated to cover the required spectrum.

Also as it was mentioned before, the required gain alignment between the two paths would force the designers to have a programmable bias to control the gain of the block.

This technique shares the same problems as the feedforward translational loops. That is the first LNA has to process the blocker which makes the design susceptible to high power blockers. Other issues include the gain and phase alignment of the two paths. However, it might be even harder with this approach as the gain of the injection locked oscillator is not as easily determined as the time-invariant amplifier blocks.

4.6 Passive-Mixer-Based High-Q Bandpass Filters

There is a very fundamental factor behind these type of filters' school of thought. As the technology scales, the quality of capacitors and switches gets better and better and yet the quality of inductors remains more or less the same. Worse than that, the area of the inductors won't change and now in the cellular regime, they are now the most area-hungry components on the integrated circuit platform. Producing bandpass filers with inductors and capacitors not only is area-hungry, but also it suffers from inherent low quality factors which can't pave the way for SAW-Less receivers. The idea is to replace these inductors with capacitors and resistors. There has been a thorough analysis done on this case and the effects of non-idealities on this technique [48], the idea is to have a compact low-pass filter with

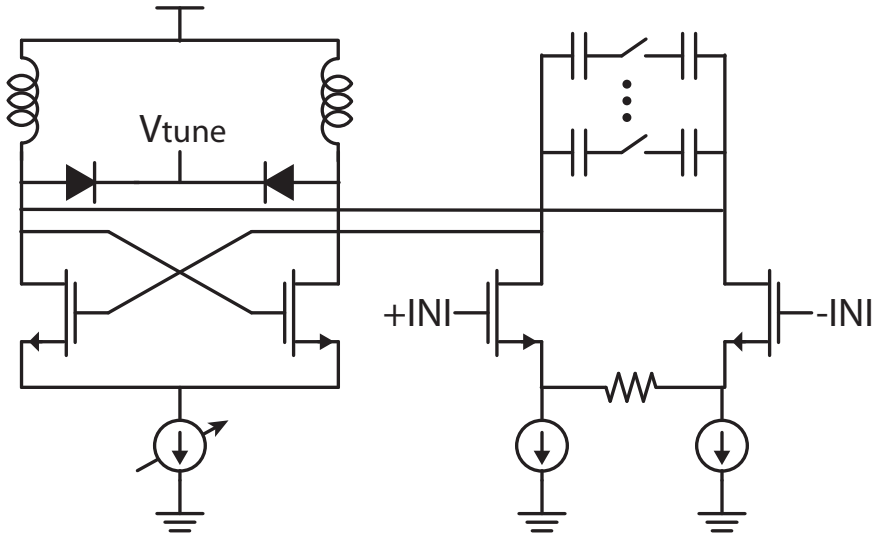

Figure 4.11: Circuit schematic of the core of the injection locked oscillator

capacitors and then up-convert that characteristic to the desired signal frequency through the high performance switches available in scaled CMOS technology. Basically, assuming the ideal frequency shifter, transferring the same slope in low-frequency to the GHz regime, tremendously increase the quality factor of the structure. For example, say the 10dB change which occurred from DC to 1MHz, now is happening from 2.4GHz to 2.401GHz. It can be shown [48] that the input impedance of such filters is:

$$Z_{in} = R_{SW} + \frac{2}{\pi^2}\left(Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO})\right) \tag{4.7}$$

As can be seen in Eq. 4.7, the performance of this filter is sensitive to the switch resistance (for the stop-band characteristics) and to the ratio of switch resistance to the parasitic capacitances (for the pass-band characteristics). In other words, the performance is function of the ratio between conductance and capacitance, $\frac{g_m}{C_{par}}$, on the other hand we know the f_T of transistors is defined as [31]:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs} + C_{gd}} \tag{4.8}$$

As the channel length scales, f_T of devices increases and hence the switch performance of the aforementioned block improves. Also there is the phase noise problem which causes reciprocal mixing. The way this filter works is that it down-convert the blockers and attenuates them. Looking from RF-side, one would see the up converted signals from base-band. Now if there is reciprocal mixing, then the blocker would fall on top of DC and looking from RF side, it would fall on top of the desired signal, degrading the noise figure of the system.

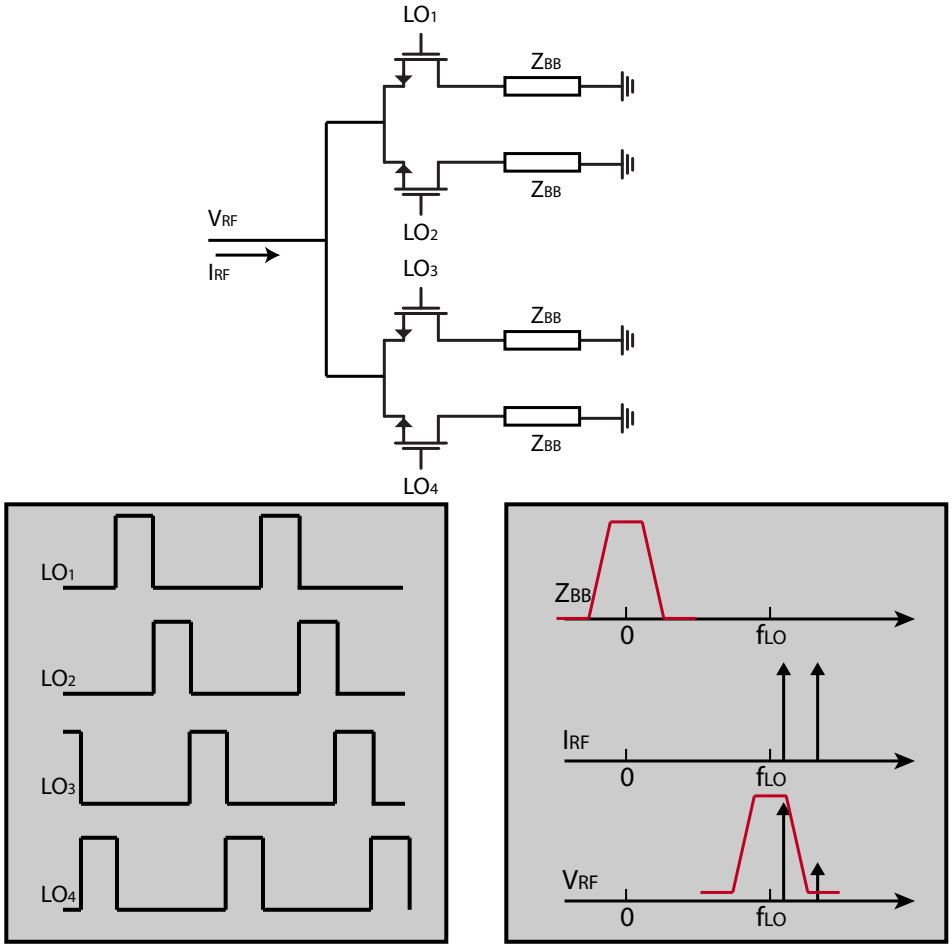

Figure 4.12: Switched capacitor bandpass filter concept [49]

The other issues which are not of major concern is the presence of second order distortion in switches and IQ mismatch in the LO which both degrade the noise figure by generating content on top of the desired signal. Proper layout techniques can dramatically improve these effects though.

There is one very important factor regarding the characteristics of this filter. As can be seen in the analysis [48], the assumption is that the input signal is in current domain and consequently the voltage generated at the RF node is set by the I-V conversion of the base-band and up converting that to the RF side. Now if one drives this module with a voltage source, then the performance is different and the quality factor would drop drastically. Looking at the designer's circuit [49], one would notice incorporating three of these filters, two of those placed after the signal has been converted to the current domain by the input transistors of the LNA.

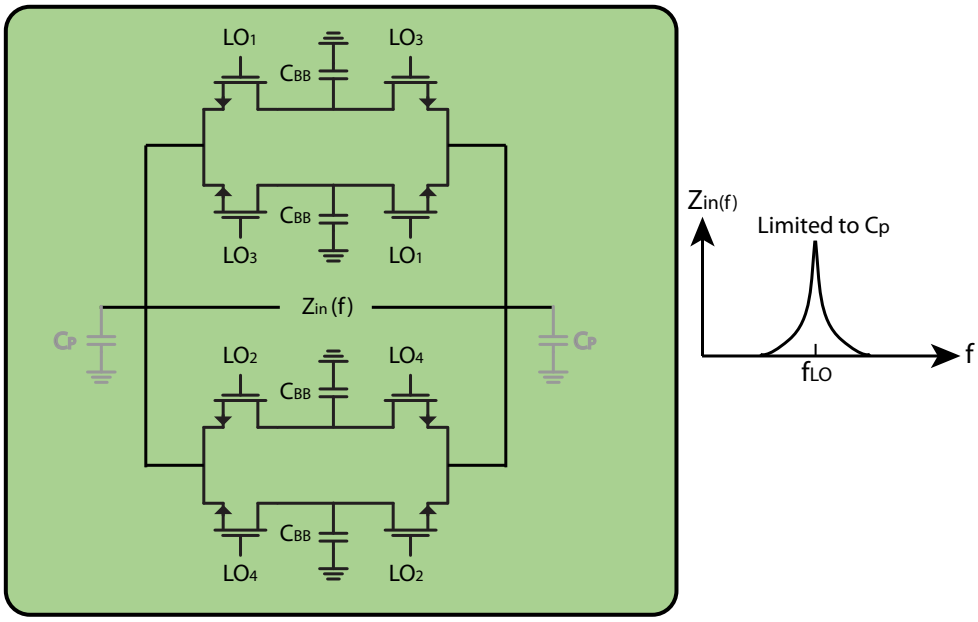

Figure 4.13: Switched capacitor bandpass filter circuit schematics

4.7 Historical Approach

Now that the state-of-the-art for coping with closely located interference signals has been reviewed, it might worth asking this question of whether or not these issues existed earlier in the history of radio and what was the common solution for that?

Again their approach could be divided between RF domain or IF domain. For the latter case, there were dynamic notch designs [11], as can be seen in figures 4.14 and 4.15 which show incorporating variable and fixed notch approach respectively. In the former the strong blocker would be demodulated by the additional FM demodulator and that would help the variable taps in the second amplifier to be tuned and cancel the large blockers. In the latter the frequency of the blocker should be detected first and then that would be translated to the fixed notch to be removed.

In [74] the authors proposed a cross-coupled interference canceler scheme in which by assumption of interference signal is much stronger than the desired one, which is the case that's challenging to deal with, the system would separate the two signals and would give the jammers at the upper branch, Figure 4.16, and the desired signal at the lower branch.

Briefly the way it works is that the top PLL first locks to the strong interference and the output of VCO lags 90 degree due to quadrature structure. Then another 90 degree angle assures the cancellation of the jammer for the lower path, and the same way the upper path would give the desired signal. Looking at this approach, one would see a lot of similarities between this approach and the translational loop ones.

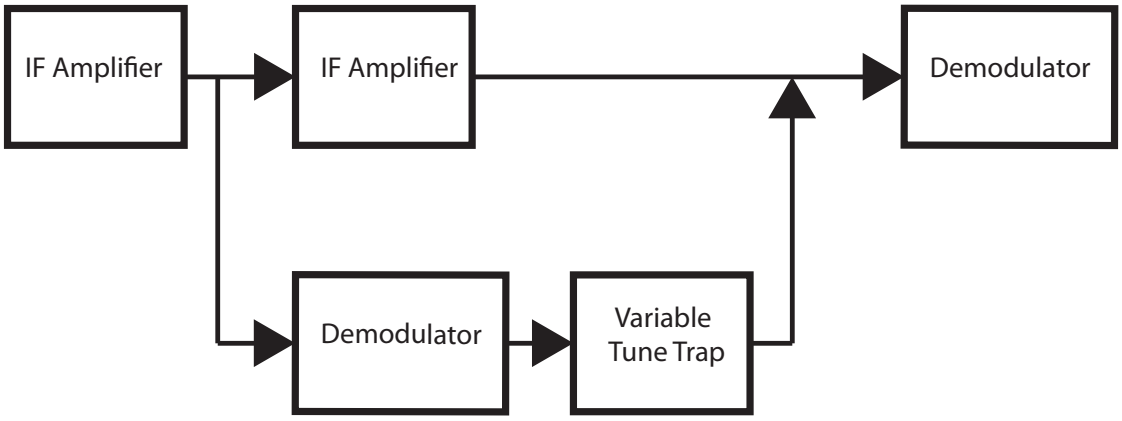

Figure 4.14: System diagram of variable notch filter for FM radios

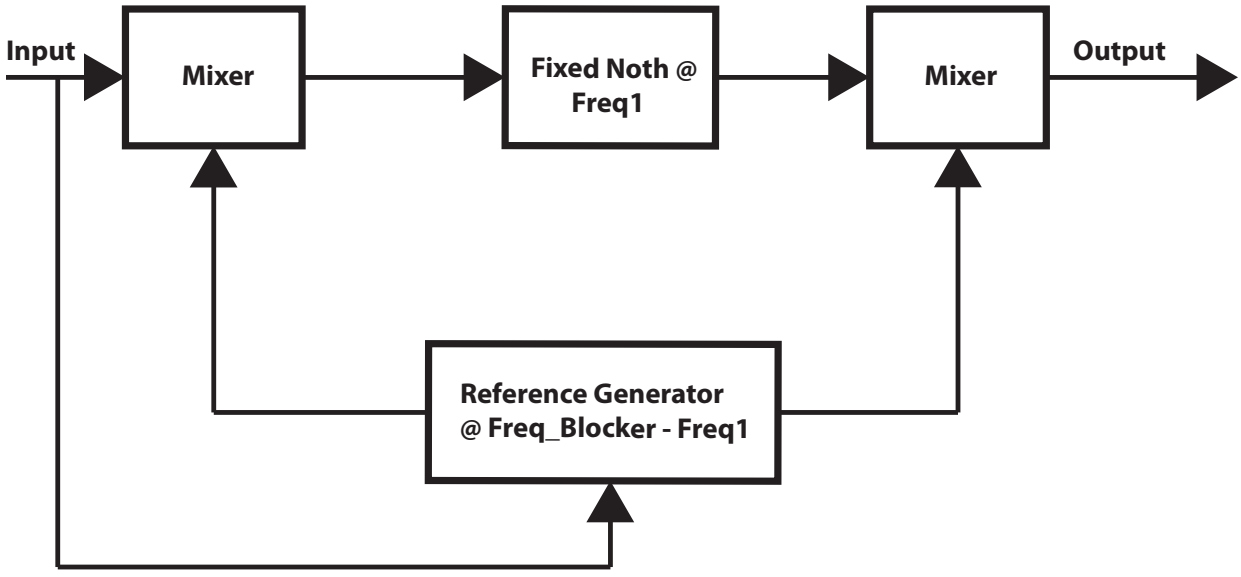

Figure 4.15: System diagram of a fixed notch filter for FM radios

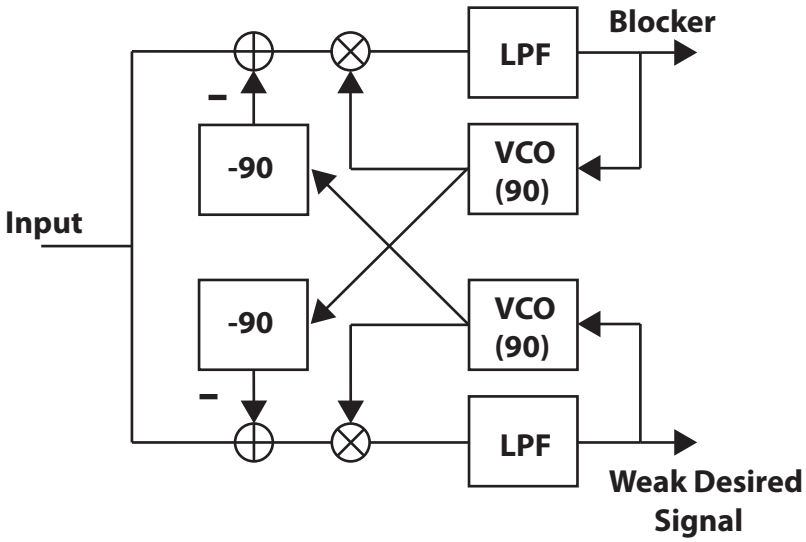

Figure 4.16: Cross-coupled FM system with the interference canceler

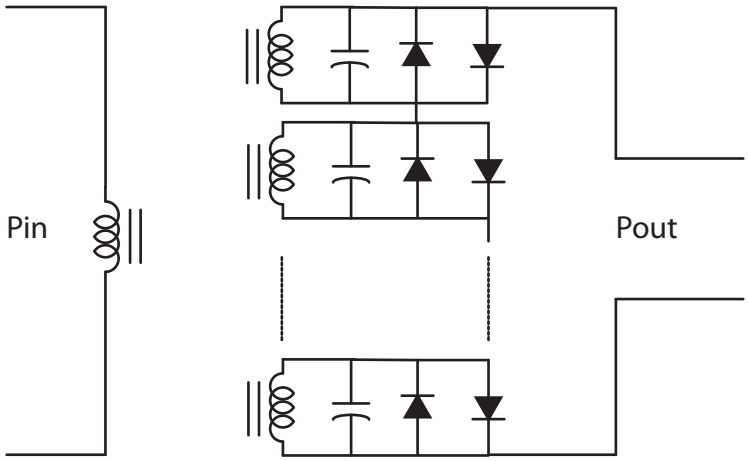

Figure 4.17: Conceptual representation of frequency selective limiters (FS)

If one asks wireless receiver designers what is the most desirable block to have is, perhaps many would agree to have a frequency selective limiter (FSL) which is passive and broadband and will just cut the signals that are higher than certain power and will keep the rest unchanged. Well, actually there exists such a block.

Exploiting the nonlinear excitation of magnetic spin waves in an magnetized ferrite such as yttrium-iron-garnet (YIG) can give such functionality. Microwave energy enters the YIG

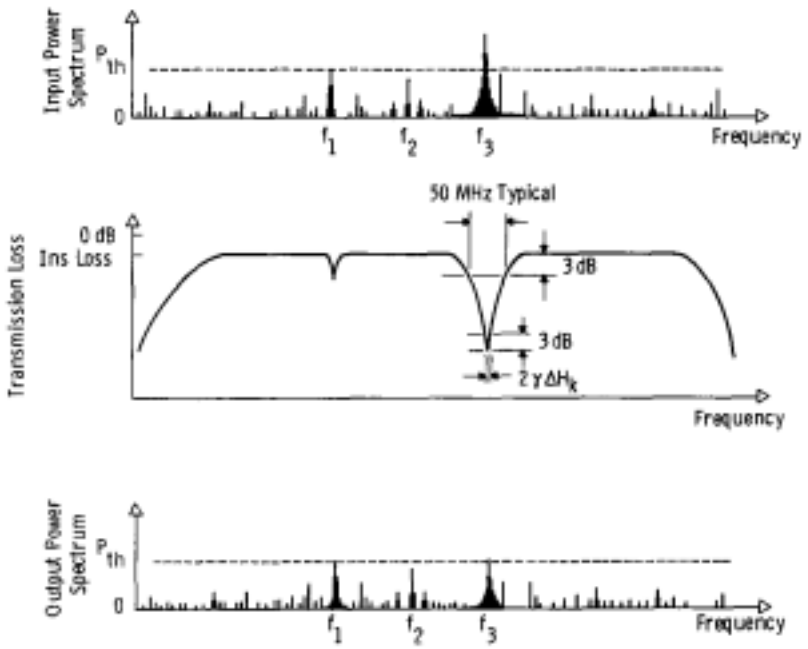

Figure 4.18: Typical frequency response of an FSL for different power input levels and the resulting output power [3]

material and produces linear, low-loss response in the ferrite when the signal power is low. Above a certain RF magnetic field strength, the nonlinearity in the precession of the magnetic dipoles in the ferrite starts dominating the natural losses and energy would transfer exponentially to short wavelength subharmonic spin waves. This nonlinear coupling takes place in a bandwidth on the order of the spin-wave line-width ΔH_k. The conceptual representation of how this filter behaves is shown in Figure 4.17.

The threshold magnetic field for which the attenuation starts can be calculated as [3]:

$$H_{Threshold} = \frac{\omega}{\gamma 4\pi M} \frac{\Delta H_k}{\sin^2(\theta_k)} \tag{4.9}$$

Eq. 4.9 shows the threshold magnetic fields for the spin wave number k and the propagation angle θ_k. The γ is the gyromagnetic ratio, the ω_R is the precession resonance. As can be seen in Eq. 4.9, the threshold is a function of physical entities that are not easy to control for broadband operation. The other issue is that the magnetic bias field which controls the frequency of operation and the threshold power is not friendly to integration.

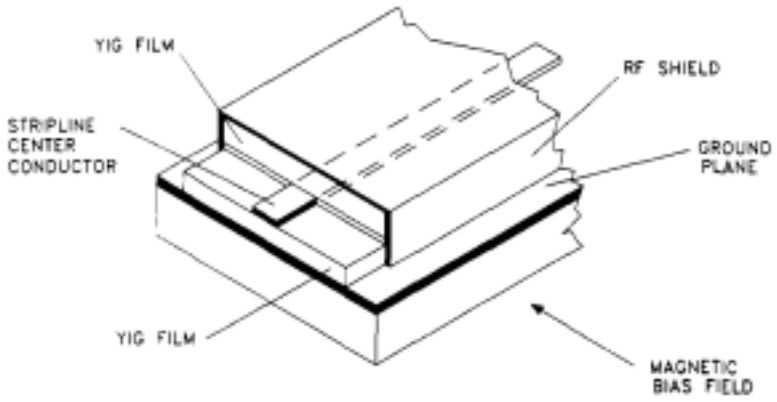

Figure 4.19: Stripline FSL using YIG [3]

Chapter 5

Self Calibrating Direct Conversion Receiver for Stable IM2 Metrics

Even order distortion is a well known concern in RF wireless receivers. In homodyne receivers, even-order nonlinearities produce low-frequency intermodulation distortion products which would fall on top of the desired signal which is also at the same frequency regimes and hence increase the noise floor. Previously this issue was greatly alleviated due to usage of high quality factor filters available. These filters would greatly alleviate the distortions since the blockers are not in their passband and would be attenuated considerably before entering the receiver. As a result, their intermodulation products would be much less of a concern. However, as mentioned in the previous chapters, the wireless trend is toward removing filters in attempt to realize hardware sharing between different standards and hence high power jammers could enter the system and be processed by building blocks which accentuates the effect of even-order nonlinearities.

5.1 Coping with Jammers: Two schools of thought

The fundamental question if we want to have a broadband wireless receiver is where we should cancel the blockers. In other words, when is it not too late? There are two schools of thought as shown in Figure 5.1.

One is to optimize and calibrate each building block in the receiver so we can squeeze as much of linearity out of them as possible. The other one is to limit the magnitude of the blockers entering the receiver. Filters can be categorized in the latter, however, that's not the only option. As discussed in the previous chapter, frequency selective limiters are the other categories which would limit the signal power at all frequencies where the power passes a certain threshold. For handling the blocker in the most efficient way, incorporating both approaches might be the best candidate. However, one should not underestimate the designers' time needed in order optimize each building block to meet the requirements over process and temperature, especially in modern scaled technologies.

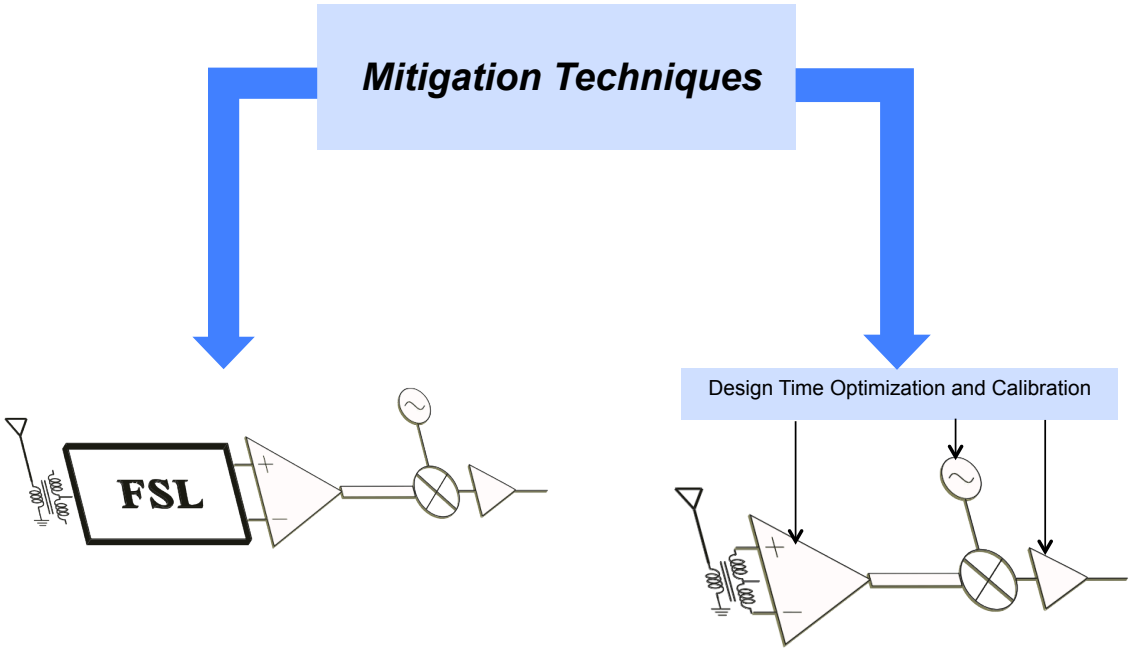

Figure 5.1: Where to deal with blockers

5.2 IP2 Metrics Characterization

The conventional approach of characterization of IP2 metric of a receiver is by applying a two tone, $A\left(\cos(\omega_1 t) + \cos(\omega_2 t)\right)$ and observing the spectrum content at $\Delta\omega = \omega_1 - \omega_2$ and $\Delta\omega$ should be chosen such that it falls in the desired band. This method is convenient for direct conversion receiver designs since the IM2 content is observable without further need of processing (e.g. frequency shift, etc.). There is one subtle point which typically is overlooked for the case of multi-standard receivers or SAW-Less receivers. As it will be discussed in the later sections, there are a few mechanisms responsible, Figure 5.3, for the generation of IM2 components and hence as expected, the metrics is sensitive to not only the difference in the blocker frequencies, but also to the actual frequency of the blockers. That means the IP2 vs. $\Delta\omega$ is not enough information and the actual place of blockers is important since, ideally, in SAW-Less receivers they can be everywhere in the spectrum and as long as their frequency separation is within the channel bandwidth, the IM2 content would appear at the SNR calculations. This is the motivation for understanding the mechanisms responsible of generation of IM2 and their trade-offs and coming up with a simple solutions, in design time or in the calibration phase. The required IP2 is based on the allowed SNR degradation to specific blockers. For example IM2 content 20dB below the noise floor of the system would degrade the noise figure by 0.04dB and 10 dB below that would cause 0.4dB.

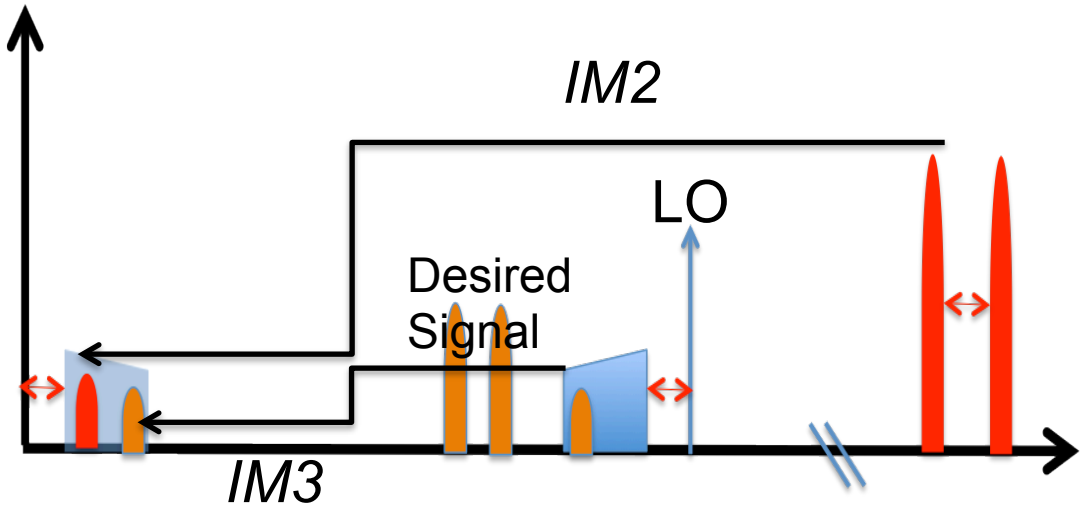

Figure 5.2: Wideband susceptibility of systems to IM2 contents

$$IIP2_{Spec}[dBm] = 2\,(P_{In,Max}[dBm] - 3) - IM2_{In,Max}[dBm] \tag{5.1}$$

Where the first term on the right refers to the total power of the interferers at the antenna and the latter refers to the maximum allowable input referred IM2 contents. The next question is what are the mechanisms responsible for the generation of the IM2 content?

5.3 IM2 Generation Mechanisms

The different mechanisms responsible for IM2 generation have been well studied analytically and also verified on silicon [26, 46, 40, 24, 28, 27, 83, 76, 33, 19, 35]. However, dominant mechanisms might change due to chosen architectures and the adopted technology. This section will review these mechanisms and discuss their importance in direct conversion receiver architecture implemented with sub-micron channel length CMOS technology. The design strategy for achieving stable IM2 metrics will be discussed afterward.

Self Mixing

This effect is due to the parasitic coupling between the RF and LO ports. That is RF and LO signal would be multiplied with themselves and hence a squared version of the input would appear at the output and fall on top of the desired signal. To quantify the effect, looking at the I-V characteristics of the mixer, Figure 5.4, one can calculate the effect of this leakage phenomenon through the following equation ([46]):

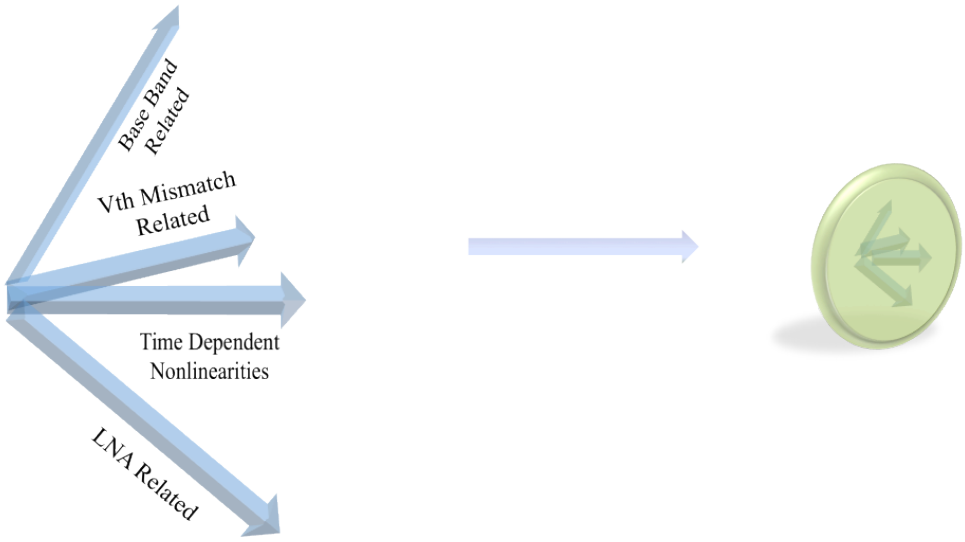

Figure 5.3: Vectors responsible for IM2 generation

$$I_{out} = \begin{cases} (g_{m,RF}V_{in})(V_{LO} + Av_{RF-LO}V_{in})/V_L & V_{LO} + Av_{RF-LO}V_{in} < |V_L| \\ g_{m,RF}V_{in}sign(V_{LO} + Av_{RF-LO}V_{in}) & V_{LO} + Av_{RF-LO}V_{in} > |V_L| \end{cases} \tag{5.2}$$

Where A_{RF-LO} is the leakage gain from the RF to the LO port and V_L represents the required voltage for complete switching.

After passing the threshold, V_L, the mixer is no more sensitive to this phenomenon but before that, i.e. in the transition phase, there would be IM2 content at the mixer output given by:

$$\frac{g_{m,RF}V_{in}^2 Av_{RF-LO}}{V_L} \tag{5.3}$$

If the LO waveform is $V_{LO} = V_M \sin(2 * \pi * t/T_{LO})$ and the V_M is much larger than V_L, then the switching time T_{Sw} is $T_{LO}\frac{V_L}{\pi V_M}$. The IM2 content is obtained as the product of T_{Sw} waveforms times Eq. 5.3, $(2g_{m,RF}A_{RF-LO}/\pi * V_M)\, V_{in}^2$. The transition time is determined with LO buffers and one can minimize it by sizing the buffer accordingly, i.e. trading the power consumption for IP2. Also deploying layout techniques like orthogonal signaling between RF and LO path can suppress the IM2 component even further and make the self-mixing negligible effect.

Also there is LO to RF coupling which of course would be improved with layout techniques. Also the effect is slightly less important since the LO is fixed and doesn't change dynamically.

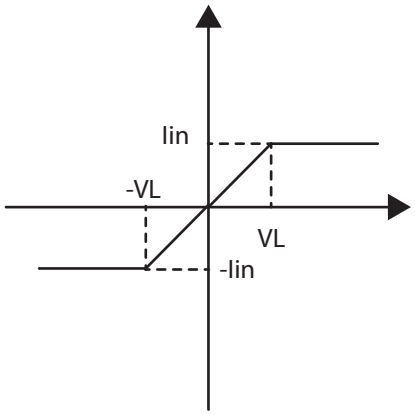

Figure 5.4: I-V characteristics of mixers

LNA Nonlinearity

The magnitude of the second-order intermodulation due to the LNA can be relatively high. However, because of the ac-coupling capacitor after the LNA, this effect can be made quite negligible. There is a trade-off in selecting the magnitude of this ac-coupling capacitor in current mode receivers. It can easily increase the load to the LNA by as much as 50% if one deploys a small capacitor and it could introduce a large parasitic capacitance to the ground.

The RF impedance at the output node of the LNA plays an important role in the IP2 metrics of the receiver. It has been analyzed quite extensively in [46] and the conclusion is the lower the parasitic capacitance at that node, the better the IP2 metrics. One option is to tune out the capacitance at that node via an inductor. Another option is to deploy a transformer at that node which has other important benefits. The ac-coupling capacitor can block the IM2 content of the LNA. However, if the output current of the LNA becomes unbalanced, that could cause generation of IM2 content. One way to think about it is that unbalanced signals can be modeled as balanced signals plus a common mode signal and the common mode to differential mechanisms can generate the IM2 at the output [46]. Placing the transformer would balance the output of the LNA by suppressing the common mode content at the primary side.

Switching Pair Nonlinearity

The switching pair mismatch in the direct conversion receiver is the dominant contributor to the even order intermodulation distortions. If the mixer switches are perfectly matched, the generated even-order distortion would not leak to the output. The differential distortions won't leak and the common mode distortions cause no harm as long as they don't saturate the following stages, which is never the case for even order distortions.

Passive mixer architecture has been proven to be superior to its counterparts in noise, linearity, power and simplicity and it's by far the most adopted topology for mixers in state-of-the-art receivers. For this reason, this architecture has been studied for even-order distortion in this thesis. Extensive analysis has been done on both active and passive configurations in literature [26, 46] and the focus of this work is to find the main distortion generation mechanisms once the whole wireless system is being designed and the interactions between mixer and other blocks become of concern. The goal is to tackle those issues in the design time or by the automated calibration circuitries if the scenario is sensitive (change with time or process corner).

A passive mixer's even-order intermodulation distortion generation mechanisms can be summarized in three categories:

I Switching pair mismatch

(a) Threshold Voltage Mismatch

(b) Sizing Mismatch

II LO Waveform Dependency

III Interaction with Base-Band Mismatch

- **Switching Pair Mismatch**

One way to think about this problem is to decompose the IM2 generation phenomenon in two separate mechanisms. First RF signals (two tone or modulated blocker) pass the LNA and see the mixer as a load. The mixer is a time varying load, Figure 5.5. That will generate IM2 components at the RF side which can leak to the output due to mismatches.

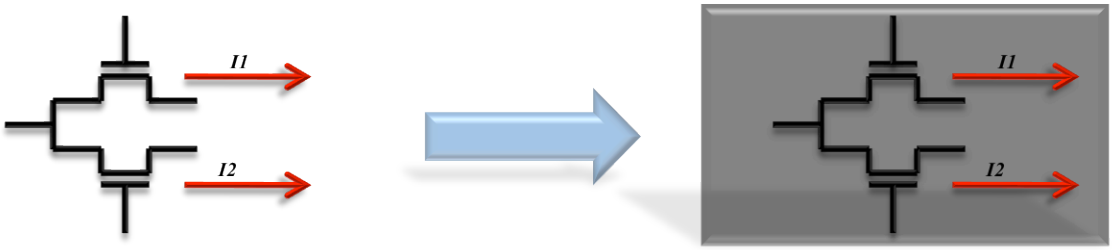

Figure 5.5: Mixer as a black box with time-varying impedance characteristics

The approach taken here is first the IM2 voltage at the RF node is found and then the output IM2 current resulting from that voltage would be calculated.

In this section, the architecture is a single ended to differential mixer with NMOS-only switches. It is a simple architecture yet provides a good intuition of the fundamental mechanisms in the IM2 generation. For the double balanced IQ mixer, simulations have been performed to finalize the design. In the following derivations, K stands for $\mu_n c_{ox} \frac{W}{L}$. ΔT refers to the overlap time of the LO waveforms, V_G is the bias voltage of the gates and V_{GT} is $V_G - V_{Th}$.

The IM2 voltage generated on the RF side due to the LNA output current can be written as:

$$I = K \underbrace{[V_G - V_{Th}]}_{a}[V_D] - \underbrace{\frac{K}{2}}_{b} V_D^2 \tag{5.4}$$

$$b(V_D)^2 - aV_D + I = 0 \tag{5.5}$$

$$V_D = \frac{I}{KV_{GT}} + \frac{I^2}{2K^2V_{GT}^3} \tag{5.6}$$

In which the second term would give the IM2 voltage at the output.

One can write down the equation of the output even-order distortion current of the mixer based on the matching criteria between the mixer's transistors. Here it has been divided into four categories based on locations of the source and drain (on the RF or IF

side), and what is the source of mismatch, sizing $K = \mu C_{ox}\frac{W}{L}$ and threshold voltage, V_{Th} mismatch. V_{RF} in these equations refer to the IM2 voltage on the RF side.

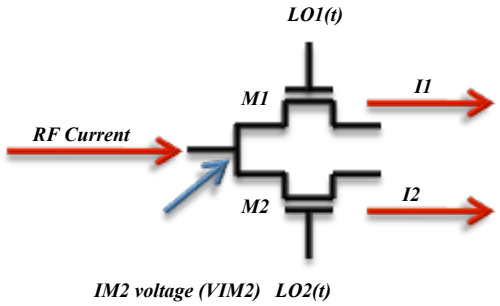

Figure 5.6: Differential mixer input and output currents

I The sources of the switching transistors are at the RF side, Ks are equal and there is a mismatch in the threshold voltages. Writing down the equations one obtains:

$$I_1(t) - I_2(t) = K[V_{LO1} - V_{RF} - V_{Th1}][-V_{RF}] - K[V_{LO2} - V_{Th2}][-V_{RF}] \\ -\frac{K}{2}[V_{RF}]^2 + \frac{K}{2}[V_{RF}]^2 \tag{5.7}$$

$$I_1(t) - I_2(t) = -K[V_{RF}][(V_{LO1} - V_{LO2}) + (V_{Th1} - V_{Th2})] \tag{5.8}$$

$$I_1(t) - I_2(t) = -K[V_{RF}][V_{LO} + V_{mm,Th}] \tag{5.9}$$

II The drains of the switching transistors are at the RF side, Ks are equal and there is a mismatch in the threshold voltages.

$$I_1(t) - I_2(t) = K[V_{LO1} - V_{mm} - V_{Th1}][V_{RF}] - K[V_{LO2} - V_{Th2}][V_{RF}] \\ -\frac{K}{2}[V_{RF}]^2 + \frac{K}{2}[V_{RF}]^2 \tag{5.10}$$

$$I_1(t) - I_2(t) = -K[(V_{LO1} - V_{LO2}) + (V_{Th1} - V_{Th2})][V_{RF}] \tag{5.11}$$

$$I_1(t) - I_2(t) = -K[V_{RF}][V_{LO} + V_{mm,Th}] \tag{5.12}$$

The above mentioned cases result into the following equation:

$$\Rightarrow I_{Out,mm} = KV_{mm,Th}V_{RF} \tag{5.13}$$

The same procedure can be performed for the mismatch between Ks:

III There is a mismatch between Ks and the source of the transistors are on the RF side: (in the overlap period)

$$\begin{aligned} & K_1[V_{LO1} - V_{RF} - V_{Th}][-V_{RF}] - K_2[V_{LO2} - V_{RF} - V_{Th}][-V_{RF}] \\ & = [-V_{RF}][K_1V_{LO1} - K_2V_{LO2} - (V_{RF} + V_{Th})[K_1 - K_2]] - \left(V_{RF}^2(\frac{1}{2})(K_1 - K_2)\right) \end{aligned} \tag{5.14}$$

$$I_1(t) - I_2(t) = [V_{RF}][KV_{LO1} + -\frac{\triangle K}{2}V_{LO1} - \frac{\triangle K}{2}V_{LO2} + (V_{RF} + V_{Th})[\triangle K]] + [V_{RF}]^2\frac{\triangle K}{2} \tag{5.15}$$

Noting the ratio between the overlap time and the period is $\frac{\Delta T}{T}$, one obtains:

$$\begin{aligned} I_1(t) - I_2(t)|_{@IF} &= V_{Th}V_{RF}\triangle K - V_{RF}\triangle K[DCofLO] \\ &= - \triangle K\left([DC\ of\ LO] - V_{Th}\right)V_{RF}\frac{2 \triangle t}{T_{LO}} \end{aligned} \tag{5.16}$$

IV There is a mismatch between Ks and the drain of the transistors on the RF side: (in the overlap period)

$$K_1[V_{LO1} - V_{Th}][V_{RF}] - K_2[V_{LO2} - V_{Th}][V_{RF}] - [V_{RF}]^2[\frac{1}{2}][K_1 - K_2] \tag{5.17}$$

$$I_1(t) - I_2(t)|_{@}IF = [V_{RF}][KV_{LO1} - \frac{\triangle K}{2}V_{LO1} - KV_{LO2} - \frac{\triangle K}{2}V_{LO2} + V_{Th} \triangle K] \tag{5.18}$$

$$I_1(t) - I_2(t)|_{mm} = V_{RF} \triangle K[V_{Th} - DC\ of\ LO] \tag{5.19}$$

The ratio between the overlap time and the period is $\frac{\Delta T}{T}$. Hence the resulting IM2 components is:

$$I_1(t) - I_2(t)|_{mm} = V_{RF} \triangle K[V_{Th} - DC\ of\ LO]\frac{2 \triangle t}{T_{LO}} \tag{5.20}$$

K value mismatch outside the clock overlap area can produce IM2 components.

Assume transistor number one is on and the other one is in the off state. The output current in that phase would be:

$$I_1(t) = V_{RF}[K - \frac{\triangle K}{2}][V_{LO-} - V_{Th}] = \underbrace{V_{RF}K[V_{LO-} - V_{Th}]}_{a} - \underbrace{V_{RF}\frac{\triangle K}{2}[V_{LO-} - V_{Th}]}_{b} \tag{5.21}$$

Term b has opposite sign for positive and negative cycles and they would add-up and create IM2 components given by:

$$\triangle K[V_{LO,amp} - V_{Th}]V_{RF}\frac{[1 - 2\frac{\triangle t}{T_{LO}}]}{2} \tag{5.22}$$

Now putting together the results from Eq. 5.6 and the above mentioned equations one obtains the output IM2 current due to threshold mismatch:

$$V_{mm}V_{RF}K\left(\frac{2\triangle t}{T_{LO}}\right) \tag{5.23}$$

The output IM2 current due to K mismatches:

For the overlap period:

$$\Delta K(V_{GT} - V_{DC} - V_{RF})\frac{2\Delta T}{T_{LO}} \tag{5.24}$$

and the outside the overlap period:

$$\triangle K \underbrace{V_{GT}}_{rms,\ recified} V_{RF}\left(\frac{1 - \frac{2\triangle t}{T_{LO}}}{2}\right) \tag{5.25}$$

Noting the voltage on the RF side:

$$V_{RF} = \frac{I^2}{2K^2(\underbrace{V_{GT}}_{rms})^3} \tag{5.26}$$

One obtains the following results:

The IM2 current due to threshold voltage mismatch:

$$(V_{mm})\left(\frac{\triangle t}{T_{LO}}\right)\left(\frac{1}{K}\right)\left(\frac{1}{VGT_{rms}^3}\right)(I^2) \tag{5.27}$$

IM2 current due to K mismatch in the overlap time:

$$-\left(\frac{\triangle K}{K^2}\right)\left(\frac{\triangle t}{T_{LO}}\right)\left(\frac{VGT_{DC}}{VGT_{rms}^3}\right)(I^2) \tag{5.28}$$

IM2 current due to K mismatch in the overlap time outside the overlap time:

$$-\left(\frac{\triangle K}{K^2}\right)\left(\frac{1}{4}\frac{T-2\triangle t}{T_{LO}}\right)\left(\frac{1}{VGT_{rms}^2}\right)(I^2) \tag{5.29}$$

- **LO Waveform**

Each mixer switch is being fed by a branch of the quadrature VCO. The duty cycle is 25%. If there are mismatches in the pulse-width applied to the individual switches, that would effectively generate the leakage gain for the even-order distortions. There are two ways to tackle this issue. One option is by careful optimization of the inverters driving the gate of the mixers' switches to make sure the duty cycle of the applied waveform are the same. This of course would not be a good candidate for multi-standards designs since changing the frequency would require new designs. Thus the better option is to have the capability to delay the clock, to engineer the crossing point, and also change the slope by adjusting the fingers of the PMOS and NMOS of the inverters, as shown in Figure 5.7.

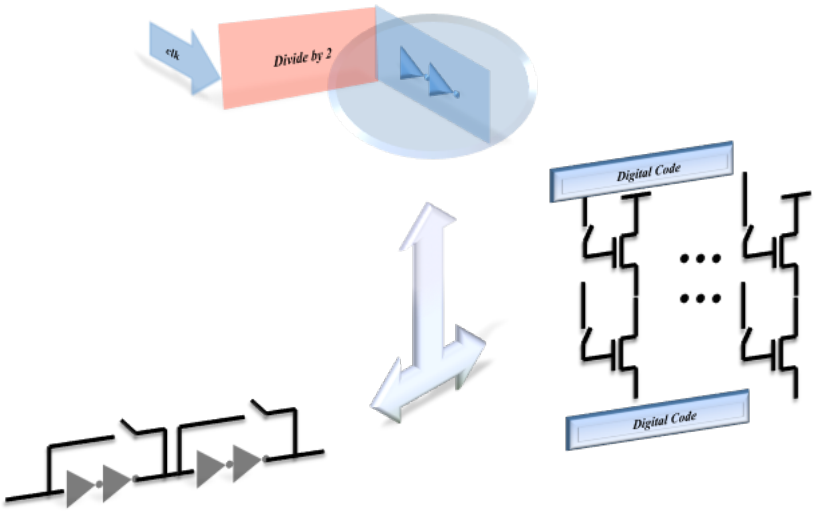

Figure 5.7: Course and fine tuning of the applied clock

Other than tuning the clock duty cycle there remains one more factor one should consider while designing these clock buffers and that's the crossing point of the consecutive waveforms, $LO_1(t)$ and $LO_2(t)$ in the Figure 5.8.
Assuming the duty cycle are fixed and they're equal for different switches, there would be three options to engineer the crossing points of the LO waveforms:

1. Crossing occurs at the middle point of the waveforms *Figure*5.8
2. Non-overlapping waveforms *Figure*5.9
3. Overlapping waveforms *Figure*5.10

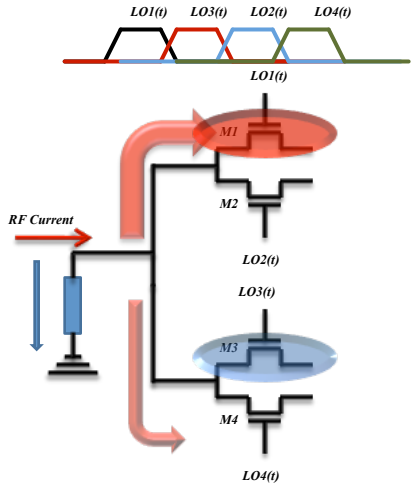

Figure 5.8: Waveforms crossing at 50%

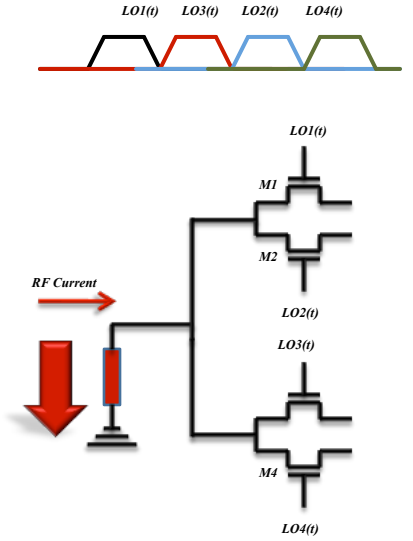

Figure 5.9: Non-overlapping waveforms

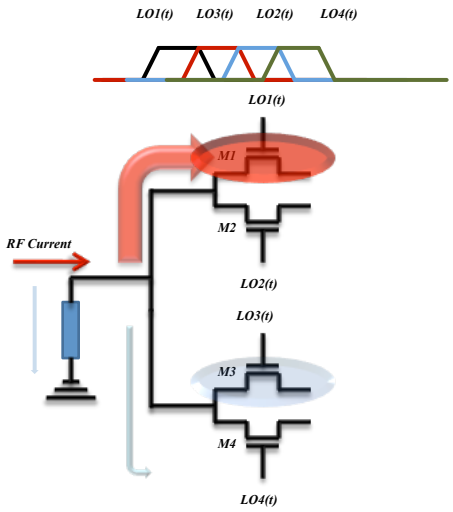

Figure 5.10: Overlapping waveforms

There are a few parameters that would determine which option one should pick. Linearity of the system i.e. P_{1dB}, IP_3, noise figure (NF) and of course even-order distortions (IP_2).

From linearity's perspective, overlapping scenario is desirable since that would assure always having a low-impedance load for the LNA which would result into high linearity. From the noise figure point of view, it's desirable to have no overlapping. The reason lies in the fact that overlapping causes the impedance seen from the baseband side to the RF side to decrease. Looking at Figure 5.11 one can see the path seen by upper channel's TIA. Instead of having the output impedance of the LNA as the load, which can be large, the other channels' TIA plus the impedance of the switches as the load is quite low. Considering the TIA equivalent noise source at the input of the amplifier, Figure 5.12, one can write the output noise due to the base-band as:

$$V_{n,Out} = V_{n,In} * \left(1 + \frac{R_{FB}}{R_{IF-RF}}\right) \tag{5.30}$$

Thus to minimize the output noise one wants to maximize the R_{IF-RF} according to Eq. 5.30.

Based on above mentioned arguments, linearity and noise figure favor opposite scenarios. What about even order distortions? It's not as obvious as the previous cases. It's a function of the impedance at the RF side of the mixer. As it has been analyzed in [46], this impedance plays an important role in the IP2 metrics of the receiver. Its role becomes more important once the design deploys the non-overlapping waveforms since now the LNA sees a higher impedance path and could go to the unbalanced regime. As discussed before, placing the transformer alleviates this phenomenon.

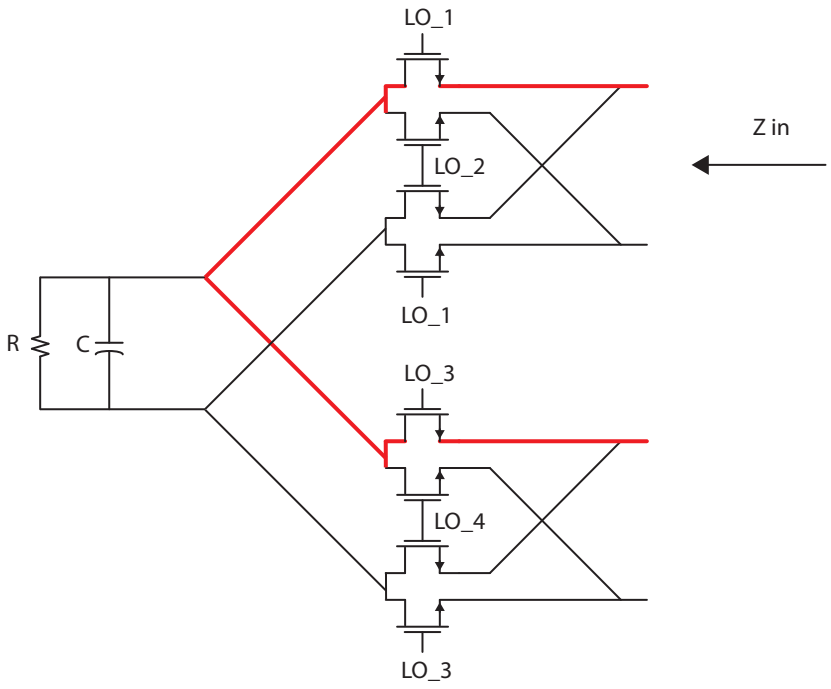

Figure 5.11: Impedance path during the overlap time

- **Interaction with Base-Band Mismatch**

  As mentioned before, the main disadvantage of using passive configuration is the bilateral property of the switches. Other than degrading the noise performance of the system, it would deteriorate the IP2 as well through two mechanisms:

  1. The bias voltage mismatch at the base-band side of the mixer could affect the IP2 metrics. The phenomenon is the same as the threshold mismatch since both of them affect the zero-crossing time instant of $V_{gs} - V_{Th}$ waveform. This is not the case in active mixer since the switches are either in the off or saturation mode and hence they don't have the interchanging source-drain scenario in the passive configuration.
  2. Cross-talk is the other issue for passive mixers due to their bilateral property. If there is IM2 content at one channel, it gets up-converted to the RF section and subsequently it will be down-converted to the other channel. This phenomenon is known as I-Q cross talk and has been extensively analyzed in [50, 51]. Intuitively, there are two mechanisms responsible for this effect. One is the LO-waveform overlapping. Looking at Figure 5.10 one can see in the overlap time, I and Q channels see each other and hence the IM2 of one channel can leak to the other. Clearly if the overlap section is removed, Figure 5.9, this is no more the case.

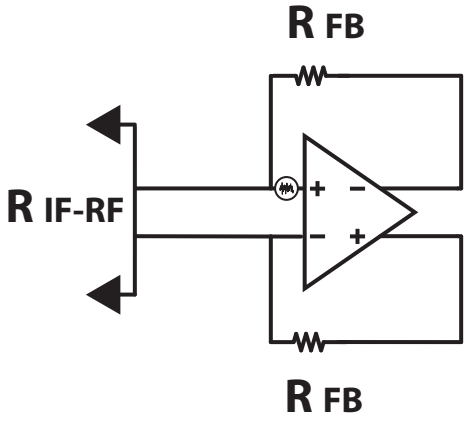

Figure 5.12: TIA noise source

However, now the RF impedance would be of importance and here is why. The IM2 would be up-converted to the RF node due to the bilateral property of the passive mixer. Now, if there is memory in that node, the content can stay at the node until the other channel's switches turn on and it would be down-converted on the other channel. Hence even the non-overlapping scenario is not going to help here and one should minimize the history elements at the RF node. That could be done either by using inductive tuning or by using more advanced technology nodes since the ratio of the parasitic capacitors to the required resistance would decrease.

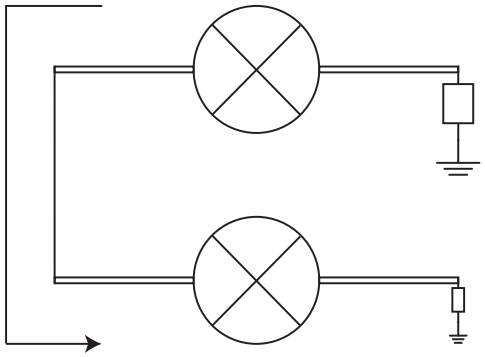

Figure 5.13: Mixer with baseband load's mismatch

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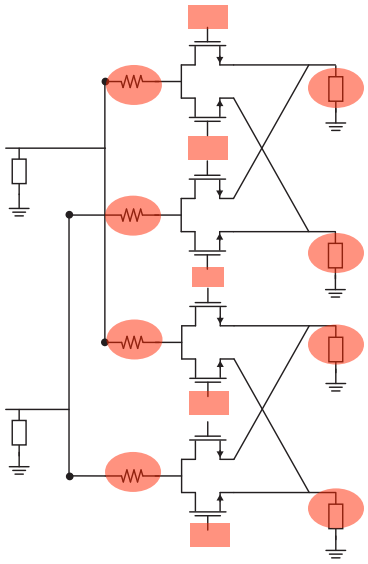

Figure 5.14: Passive mixer with baseband load

To investigate the I-Q cross-talk, a simulation was run in which mixers were perfectly matched. The base-band amplifier in one channel is calibrated and in the other one is not. Now one channel supposedly has a high IP2 metrics but the other one suffers from mismatch. What simulations showed was that both channel suffered from high IM2-contents.
Now if instead of tuning the uncalibrated amplifier, one tries to increase the IP2 of both channels by blindly changing the DAC voltage of the calibrated amplifier, the peak of the IP2 won't fall on top of each other. Whereas by tuning the uncalibrated version, both peaks happen simultaneously as shown in Figure 5.15

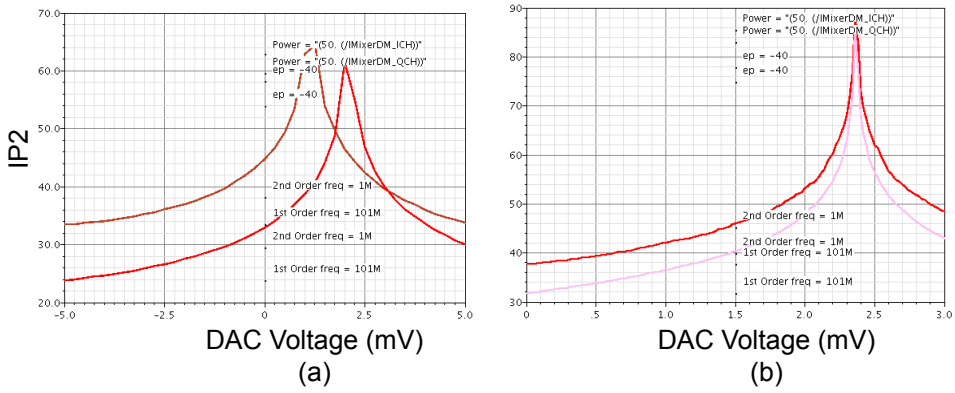

Figure 5.15: Crosstalk between I and Q channels

5.4 Automatic IP2 Calibration Chip

To validate the above mentioned theories on silicon, two prototype designs have been designed and fabricated in 90nm CMOS technology. In the first version some of the adjustments were allowed to be manual but in the second one, everything is automatic. Figure 5.16 shows the system level diagram of the designed chip.

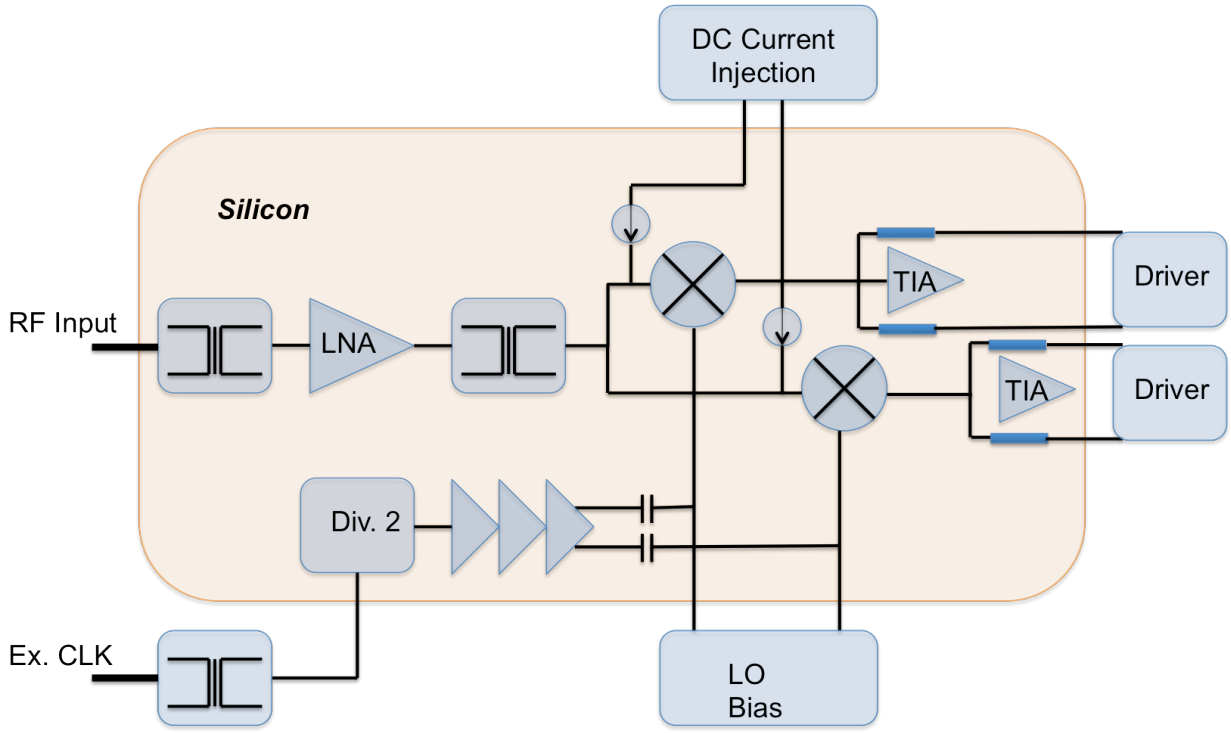

Figure 5.16: System level diagram of the chip

Simulation Procedure

BSIM4 has been used for the simulations. Two simulation setups have been used. In the more accurate version, RF tones and the LO waveforms have been treated as large signals in the Periodic Steady State (PSS) analysis. Then, the harmonics and the intermodulation distortions are monitored. To get the performance vs. frequency, one needs to perform the simulations repeatedly with blockers' frequency swept. This setup is advantageous when the power of the blocker is high since the PSS solves the circuit while treating the blocker as a large signal, hence capturing the nonlinearities due to the high power blocker. The other simulation setup is to find the circuit response by the PSS with only the LO waveforms applied. Then inject the RF tones by the Periodic AC Analysis (PAC). This analysis gives the frequency response of the time-varying blocks, i.e. the performance vs. frequency.

Table 5.1: LNA Specifications

Frequency Band	2.3-2.7GHz
Linearity	P_1dB = 0dBm
Noise Figure	$< 4dB$
Power Supply	1.2
DC Current	10mA

Here the blocker is treated as a small signal, hence the nonlinearities arising from high-power blockers are neglected. Commonly, the combination of both analyses is required to characterize the system.

There are two important factors to consider while dealing with IM2 simulations. One is that the charge-based MOSFET models are better candidates for simulating hard-switching blocks like mixers. Hence BSIM6 can give more accurate results.
In IP2 simulations, mixing actions will set the limit of the minimum IM2 contents that could be monitored before getting buried in the numerical noise. There can be 100dB difference between the power of the output of the inverters driving the mixer and the IM2 tone!

Receiver Chain Blocks

As it was discussed in the previous section, the LNA itself doesn't contribute to the IP2 but if the block get compressed, it's un-even outputs can create IM2 content at the base-band. Hence the main factor for designing the LNA is to have high compression point and also design the output network to help even further to balance the output signals of the LNA.

Capacitor cross-coupled common-gate architecture has been chosen due its simplicity and high P_1dB, Figure 5.17. Cross-coupling breaks the noise and input matching tie. An input balun has been used to do the single ended to differential conversion, Figure 5.18. The LNA is designed to work from 2.3-2.7GHz with P_1dB around 0dBm and noise figure of less than 4dB, Table, 5.1.

The output network has been designed targeting to suppress two mechanisms responsible for the generation of the IM2 content, Figure 5.19. First is due to the output impedance of the LNA. If R_{IF-RF} is low, it could boost the contribution of the base-band noise and also degrade the IP2 performance [50, 51]. Hence incorporating cascode configuration helps to alleviate this issue, Figure 5.22. Second one is the memory element at the RF node, Figure 5.21, which would cause generation of IM2 and I-Q cross-talk. As discussed previously, using a transformer has a two-fold advantage. One is tuning-out the parasitic capacitors at the RF side of the mixer and the other one is balancing-out the differential output current of the LNA. The balun has been designed, Figure 5.20, to tackle these issues.
The loading on the LNA is minimized by using TIA as low-input impedance base-band, large switches and a nearly 1-1 transformer ratio not to alter the impedance. One could use 1:N transformer with $N > 1$, but it turns out 5-4 ratio (which this design adopted) was optimum

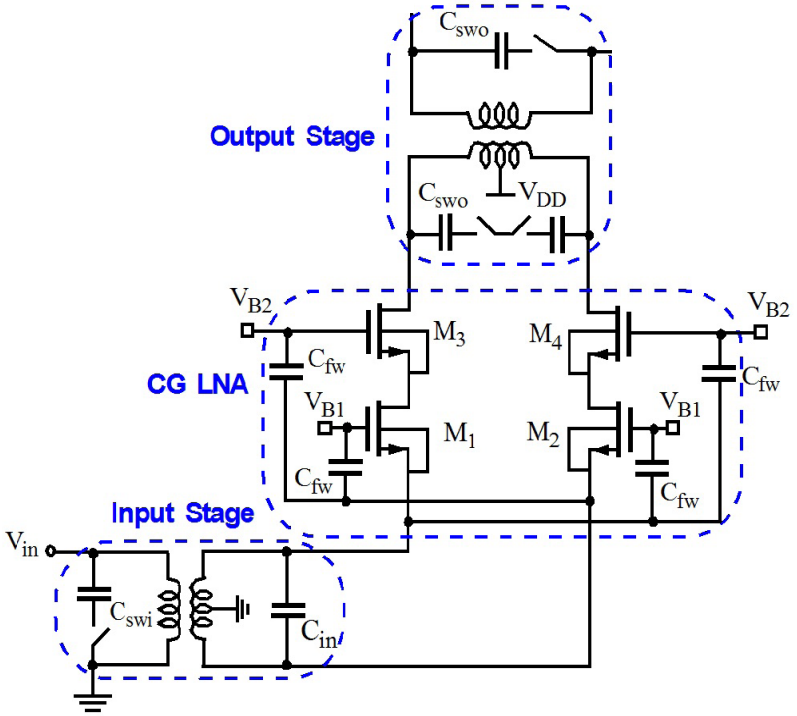

Figure 5.17: Common gate LNA

considering both loading on LNA and tuning out the capacitors on primary and secondary sides due to the LNA and mixer switches respectively.

After designing the LNA and the output network, the next thing to consider in the system is the passive mixer issues. As it was discussed extensively above, there are couple of factors regarding the passive mixer:

1. Switching pair mismatches: (a) Threshold Voltage Mismatch (b) Sizing Mismatch
2. LO Waveform
3. Interaction with Base-Band Mismatch

The sizing of the switches is set by the LNA loading criteria to meet the linearity requirement. For 90nm technology, the switch size became large enough so the sizing mismatch was not of concern. In Figure 5.23 (a) the comparison of the two mismatch mechanisms has been done. The threshold mismatch goes from -5mV to +5mV and the sizing mismatch form -3 to +3%, both ranging on the pessimistic side. The z-axis is the IM2 content of the output current of the mixer. The simulation confirms the output is much more a function of threshold voltage mismatch than the sizing mismatch. On the right part (II) of Figure

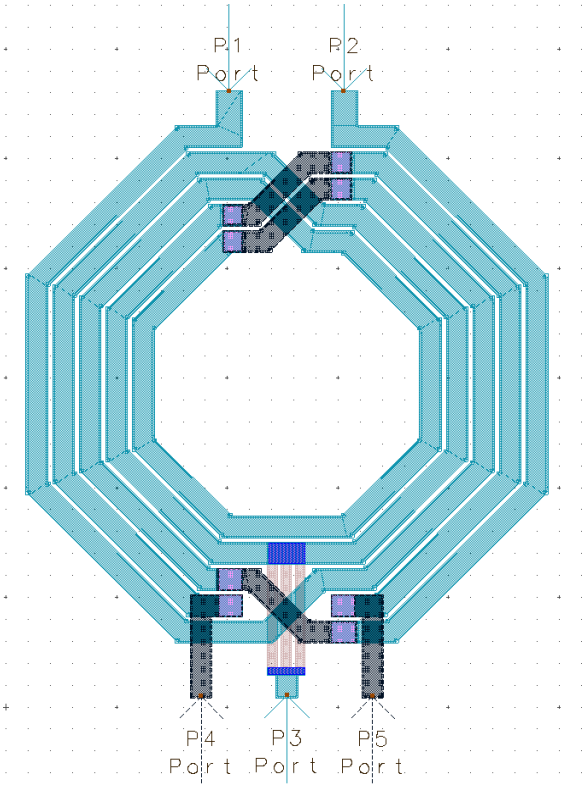

Figure 5.18: Input balun

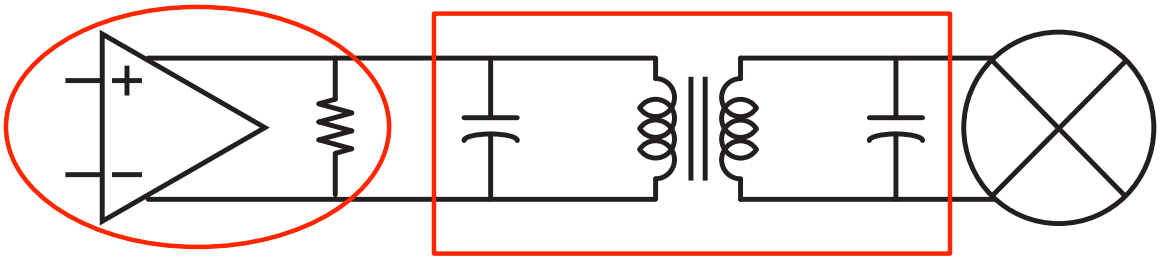

Figure 5.19: LNA output network design consideration

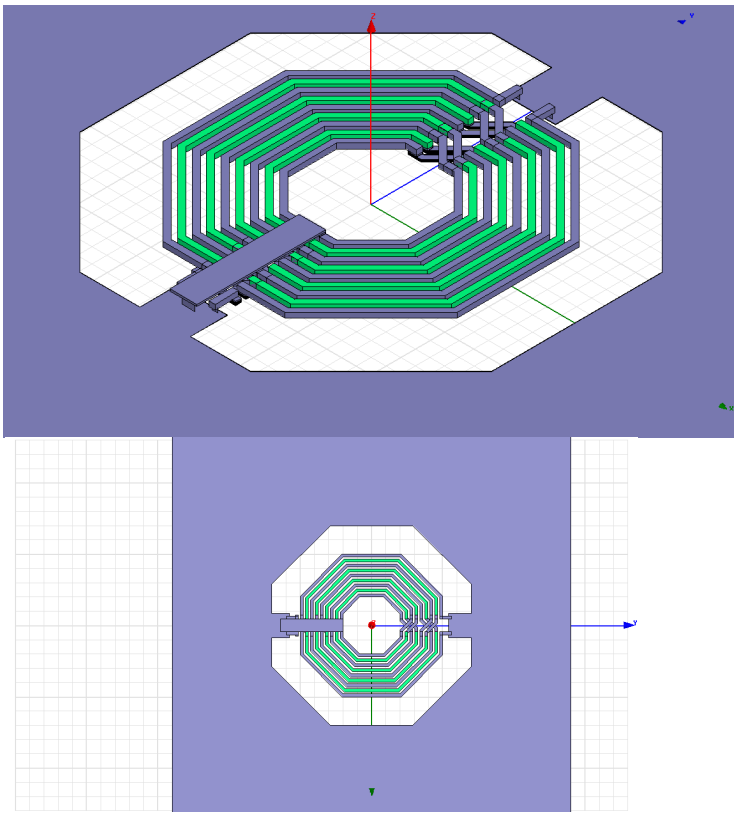

Figure 5.20: Output balun

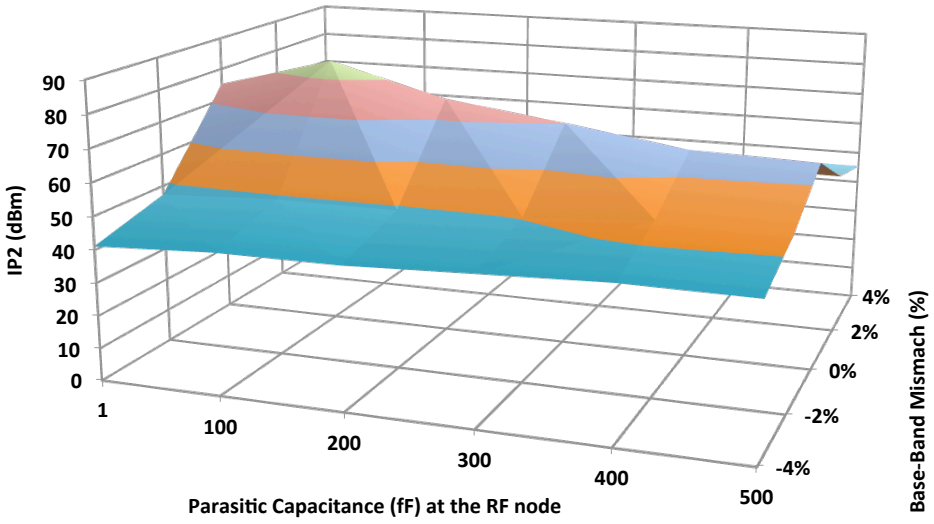

Figure 5.21: Parasitic capacitance effect on the IP2 performance

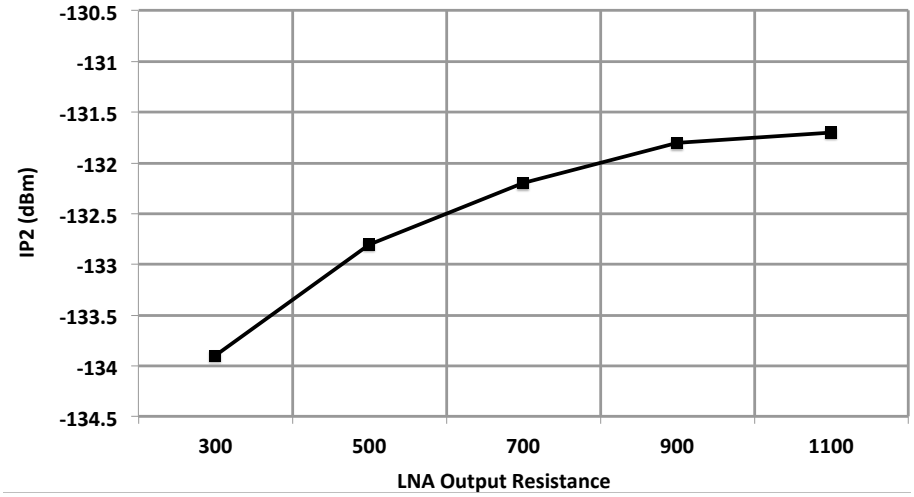

Figure 5.22: LNA output impedance effect on the IP2 performance

5.23, the simulation of threshold mismatch on one side and base-band mismatches which goes from -1 to +1%. The transistor of the base-band circuitries are larger due to $\frac{1}{f}$ noise requirements and hence the range of the mismatch is smaller. Simulation results show a) the baseband mismatch does have an effect on the IM2 content of the output of the mixer and b) the sensitivity to the base-band mismatch is comparable to the threshold mismatch.

Hence, threshold and baseband mismatches should be calibrated. The calibration starts with the baseband amplifier. In order to cancel the input voltage offset, the inputs of the op-amp would be shorted together, Figure 5.24, so the offset would be amplified by the open-loop gain of the amplifier and will be sensed at the output. What the calibration engine does is that it starts with current sources on two sides of the small resistor (top part of Figure 5.24) configured unbalanced. Then, at each step, it switches on one current source from the side with the lowest magnitude of current and switches off the other side until the comparator which is connected to the output of the TIA senses the zero crossing. That means at that instant the state-machine has created the effective offset voltage across the resistor. Since the resistor is small (20Ω), it doesn't affect the amplifier's performance. Now the switch which has shorted the inputs of the TIA would be open and it is the mixer's turn to get its threshold offset calibrated.

DC current I_D is being passed through a mixer, Figure 5.25. If the switches are exactly the same, the (calibrated) TIA output should give zero differentially. However, if there are mismatches due to sizing or threshold voltage, then the current won't be divided equally and TIA's output is nonzero. As it was mentioned in the previous section, the sizing mismatch is not of concern. To just correct for threshold mismatch, one can use the following equation for the effective offset between the gate of two CMOS switch:

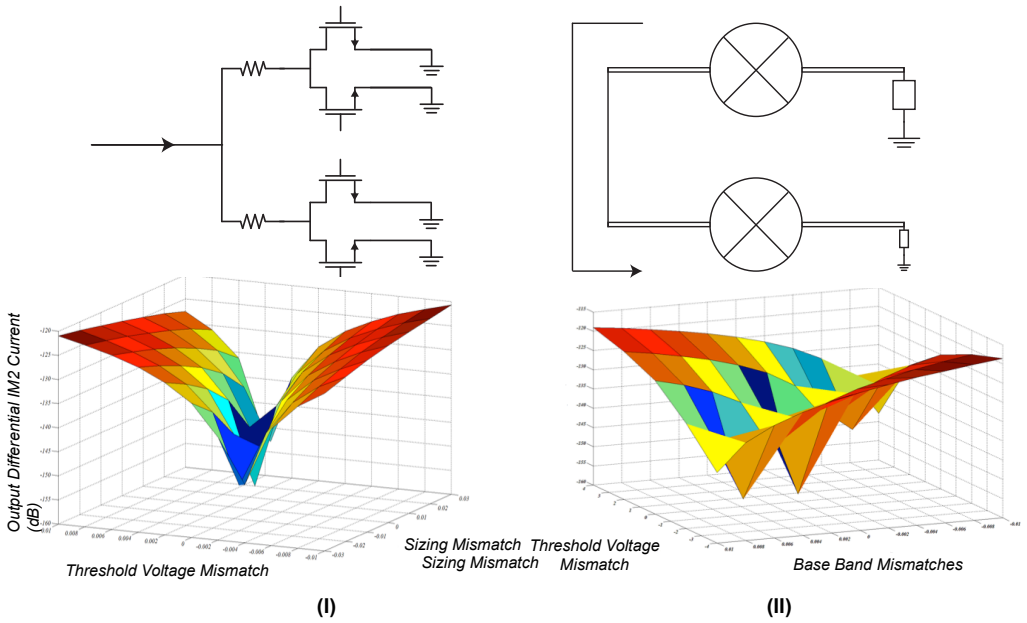

Figure 5.23: Threshold vs. sizing (I) and threshold vs. baseband (II) comparison for IM2 generation

$$V_{OS} = V_{TH1} - V_{TH2} + \sqrt{\frac{2I_{D,1}}{\mu_n C_{ox}\frac{W_1}{L_1}}} - \sqrt{\frac{2I_{D,2}}{\mu_n C_{ox}\frac{W_2}{L_2}}} \tag{5.31}$$

From the above equation, one can see by lowering I_D, one can minimize the sizing mismatch effect on the offset voltage. Thus the offset voltage being read at the output is mostly function of V_{Th} mismatches. Hence in Figure 5.25, the injected DC current is on the order of hundreds of nano amps. The threshold mismatch compensation is performed digitally after the base-band offset compensation. The simplified digital calibration logic flow for each procedure is shown in Figure 5.26. When Phase I calibration is finished, the enable signal is sent out to both sections (Q1-Q2 and Q3-Q4 branch) by a D-flip flop (DFF). A comparator will check if the mismatch is compensated at the output of the TIA. A gated clock (Clk_GP) is generated and sent to a 66-bit shift register to generate the threshold-sweeping signal. Once the mismatch is compensated, the complete signal (VTH_Calib_Done_P) for the first section will be generated and enables the calibration procedure for the next section.

5.5 Measurement Results

The prototype circuit is fabricated in a 90nm CMOS technology and measures $1.9x1.95mm^2$, Figure 5.30. Measurements were performed on a PCB with a packaged chip Figure 5.31.

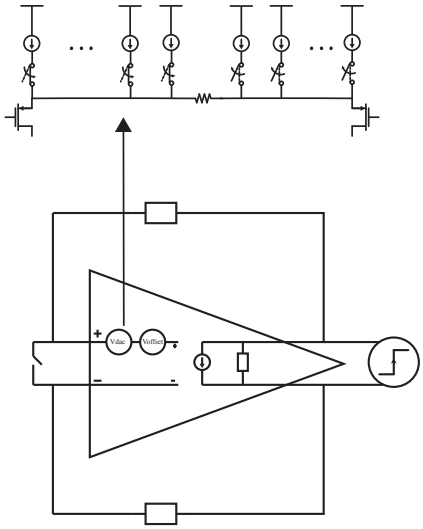

Figure 5.24: Baseband calibration scheme

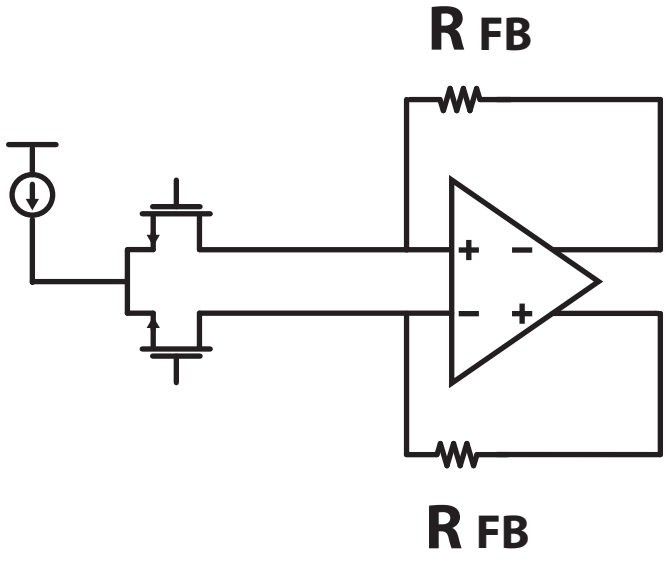

Figure 5.25: Injecting a DC current to the mixer

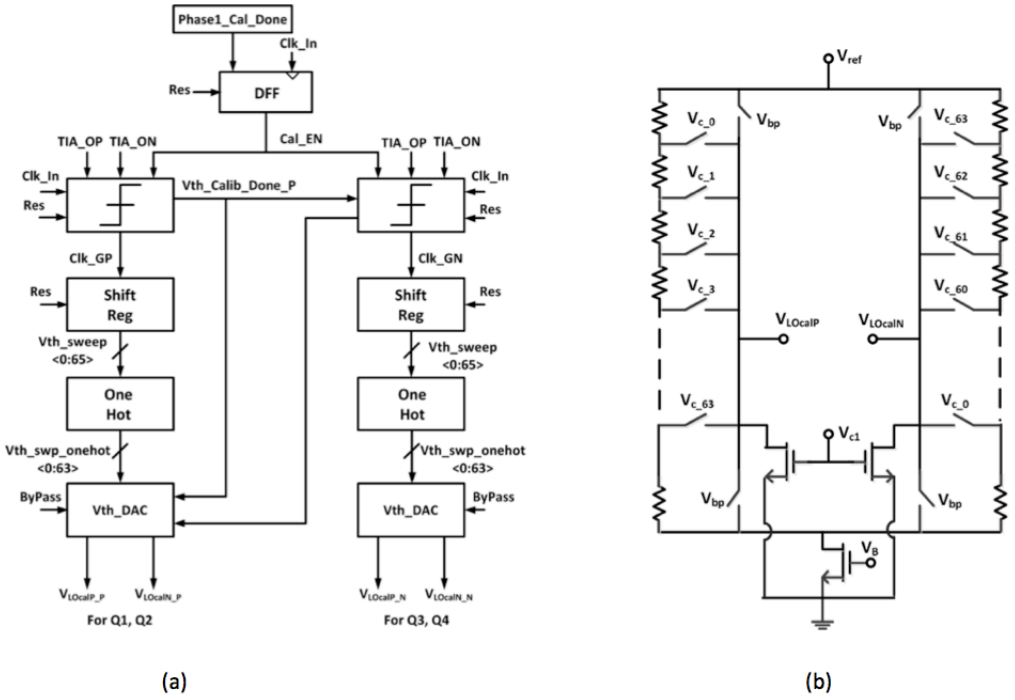

Figure 5.26: (a) Architecture of the baseband calibration circuitry incorporated within the TIA section and (b) schematic of the mixer fed with digitally controlled gate bias voltages.

The 4.8GHz clock signal feeding the divide-by-two circuitry and the low frequency clock for calibration engine is brought from off-chip.

The IP2 measurement, Figure 5.27 have been performed by sweeping the blockers' frequency and power. First, a low-frequency pulse train (10MHz) is applied to the chip to perform the calibrations. Then, a two-tone signal has been applied with frequency separation of 1MHz to make sure the IM2 content resides in the channel bandwidth of the receiver which is 10MHz. Due to the requirement of removing the front-end filters for multi-standard applications, the sensitivity of the system to the blockers' profile would become an issue as it has been discussed before. Hence the testing has been done while sweeping the blockers' frequency and power characteristics.

The frequency of the blocker has been changed from -150MHz to +150MHz with respect to the local oscillator. The calibration has been done ONLY in the start-up time of the circuitries. Figure 5.28 shows the measured results of the IP2 metrics vs. different frequencies. The IP2 of more than 60dBm for blockers at different frequencies has been achieved which satisfy the most stringent IP2 requirements. IP2 measurement has been performed for the blocker as high as -10dBm in 100MHz away offset. Again, the IP2 of more than 60dBm has been achieved, Figure 5.29.

Figure 5.32 shows the semi-automatic version in which the mixer's calibration, gate-

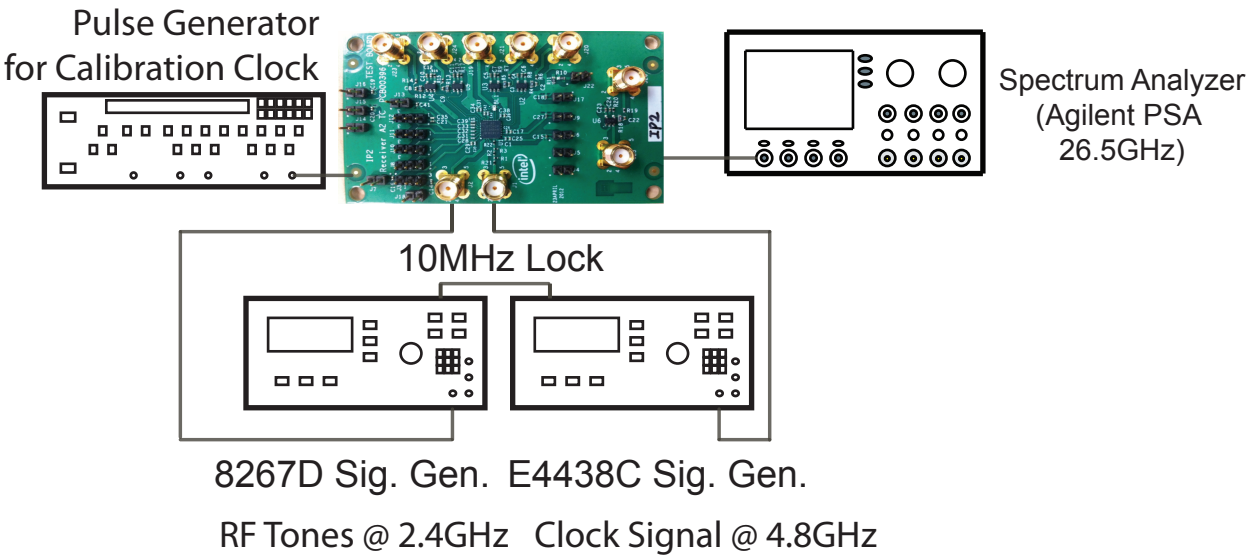

Figure 5.27: Measurement setup

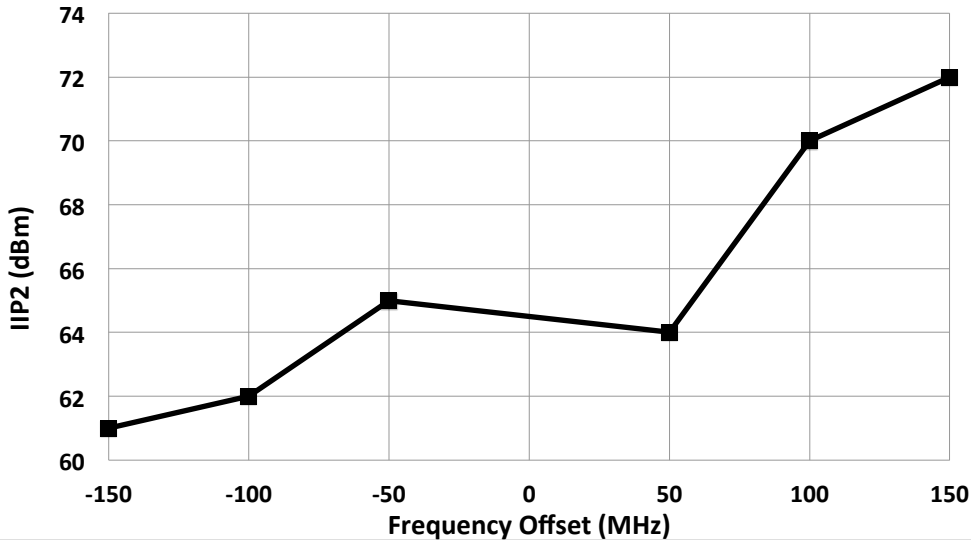

Figure 5.28: IIP2 vs. blocker frequency (LO=2.4GHz and tone separation=1MHz)

voltage adjustment and DC current injection, could be done on the board level with trimpots, Figure 5.32. Both versions gave the same results.

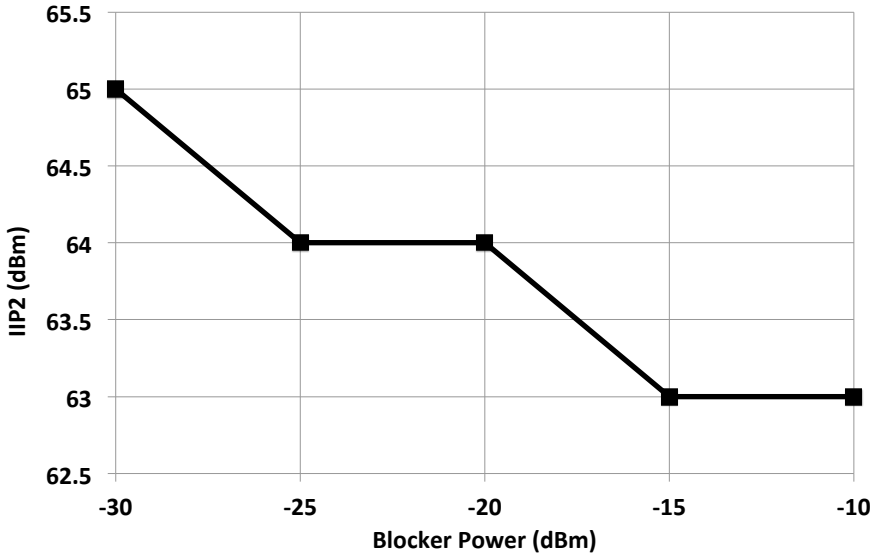

Figure 5.29: IIP2 vs. blocker input power (dBm) (LO=2.4GHz and blockers @ 2.3GHz)

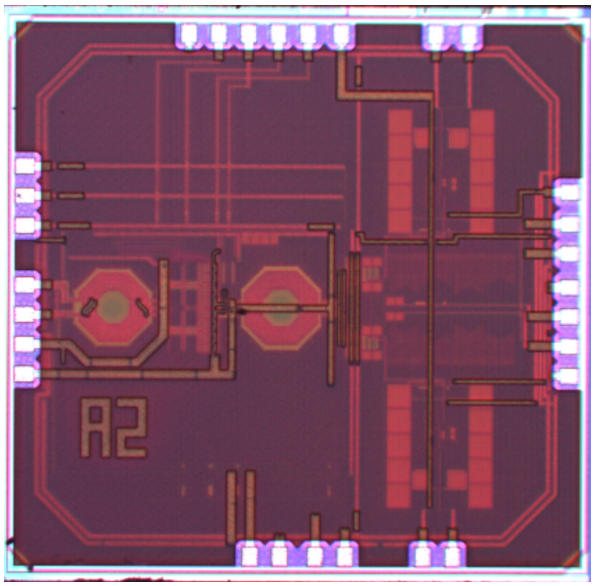

Figure 5.30: Die photo of the self-calibrating IP2 chip

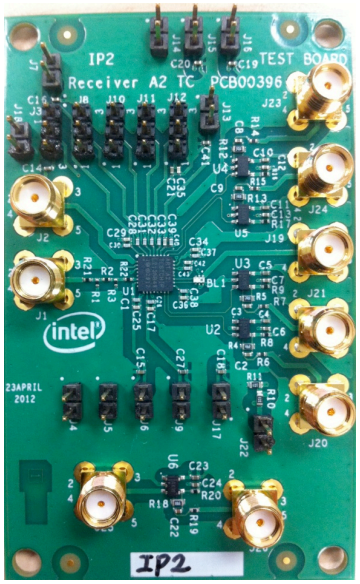

Figure 5.31: PCB of the self-calibrating IP2 chip

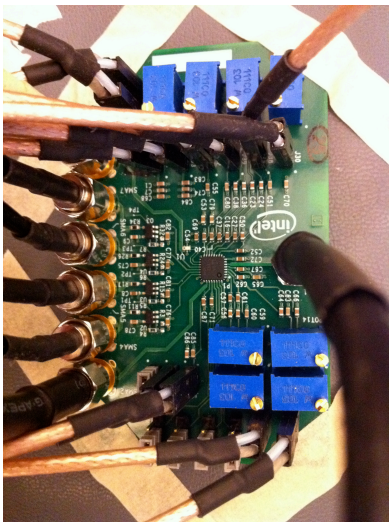

Figure 5.32: PCB of the manual-calibrating IP2 chip

Table 5.2: IP2 Chip Performance Summary

Gain	32dB
Noise Figure	5dB
P_1dB	-22dBm
$IP3$	-8dBm
Power	50mW
IP2	$>$ 60dBm Stable
Power Supply	1.2

Chapter 6

A Current Mode Receiver with an Integrated Adaptive Notch Filter

The quest for smaller and faster transistor has been a constant driver behind the Moore's law. Both Analog/RF and digital communities are benefiting from newer generations of transistors with increased speed/computation per unit time/area respectively. Pushing the limits of the technology also opens-up new application platforms which enable the designers to implement the functionalities not possible before (e.g. terahertz imaging system, etc.). However, one should be very careful in making general statements, e.g "the performance will be better with more advanced nodes". Building blocks designed with scaled transistors do NOT outperform in all the metrics. Among them $g_m r_o$, c_μ and voltage headroom are the most fundamental properties which degrade with scaling. The former plays a critical role for gain and isolation characteristics while the latter severely limit the designers' architectural choice and reduces the linearity of the blocks.

There are two main architectural decisions to be made in designing an RF receiver. The first is the frequency planning, that is what type of processing should be done at which frequency slot. Over the past few years the direct conversion outperformed low-IF receivers due to its simplicity and by using calibration and layout techniques designers have been able to tackle the issues of leakage between the ports, drift in DCs etc. However, this doesn't necessarily mean this approach will STAY optimal as the device library of the designers are due to change constantly. Recent designs [54, 32, 82, 70, 71] have been able to do more processing in the RF section and basically combine the RF-Analog-ADC in an attempt to implement Mitola's [53] software defined radio. Although the performance needs to be improved for competing with traditional approaches, this fact proves that designers should constantly revisit their arguments for picking up specific architecture.

The other system level decision is about the signaling type, i.e. voltage or current based design. The trade-offs in the system level optimization are quite different whether the blocks are designed to process the current or voltage. Perhaps the most attractive aspect of current domain mode is the low-swing nodes in the receiver chain. This behavior becomes more attractive in the newer technology nodes since the supply voltage reduces and fluctuating

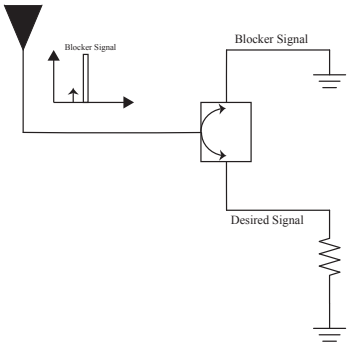

Figure 6.1: Conceptual schematic of the notch filter

the internal nodes of the system can saturate the transistors, moving them away from the optimal bias points.

Considering the direction of the technology toward faster transistors with reduced voltage handling ability on one side and the trend in the wireless receivers toward multi-standard on the other side, the idea of exploring the design trade-offs in the current mode domain becomes more attractive.

The first question is what is the format of the received signal at the antenna? The answer is "it depends". Assume there is a transmission line between the antenna and the LNA input port. If the received RF signal has the power of P_{in} and the antenna in matched to the transmission line, the current and voltage wave in the transmission line have the amplitudes of $\sqrt{\frac{2P_{in}}{Z_o}}$ and $\sqrt{2Z_oP_{in}}$ respectively. If the received signal has the power of -10dBm that would translate to 10mV and 2mA of voltage and current respectively in a 50Ω system. This level of voltage swing is substantial portion of the supply headroom. The trend for future generations of wireless receiver is toward antennas with even higher impedance.

Consequently, for the current mode system, the signal up to the LNA's input is voltage and then it would be converted to the current domain.

In this chapter a deign of a current mode receiver has been discussed. The RF signal would be converted to current at the LNA and it will stay in the current mode prior to digitization. Nevertheless, the signal at the input of the LNA is a voltage mode signal, and if the blocker is high power, the voltage fluctuation can degrade the LNA's linearity.

This chapter describes a linearity enhancement technique for RF receivers. An active dynamic blocker-notching scheme is proposed. The filter uses the blocker frequency to up-convert a DC null to the passband, attenuating the blocker before entering the receiver and hence reduces the voltage swing at the input of the LNA due to blockers. The short circuit at the blocker frequency is created by up-converting the DC response of an inductor to the pass-band of the notch using the blocker signal as the LO. When the blocker passes a certain threshold, it can be used to injection lock an oscillator driving the notch filter mixer to the blocker frequency. In this way the notch will automatically track the largest blocker.

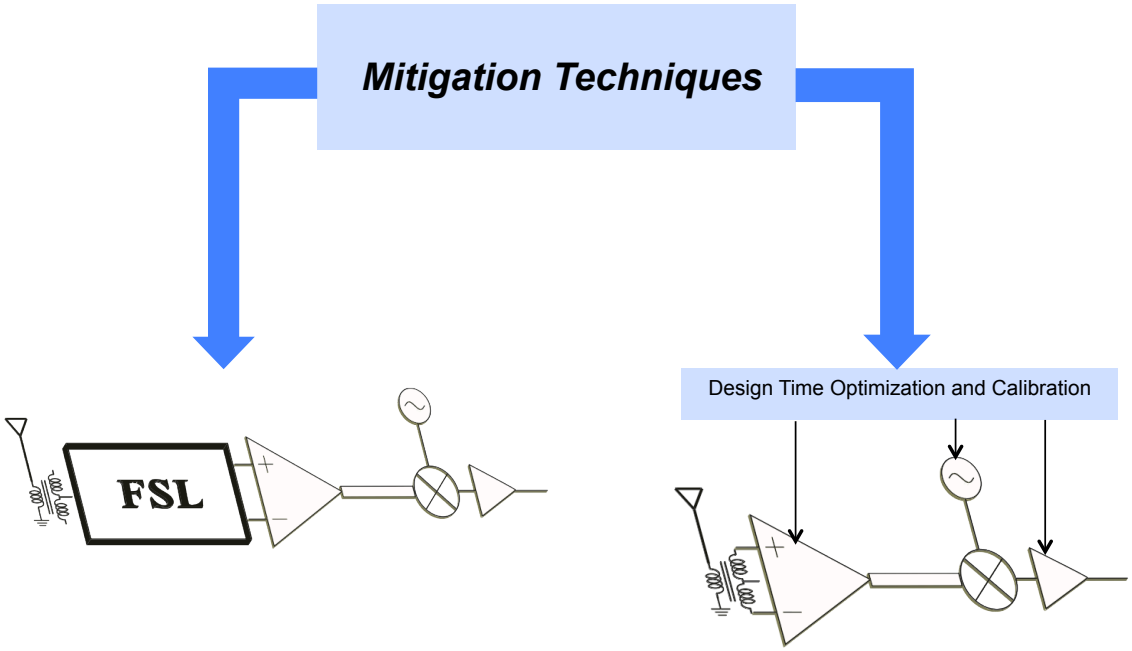

Figure 6.2: Schools of thought for dealing with blockers

6.1 System Overview

As it was mentioned in the previous chapters, there are two schools of though for dealing with blockers. One is to optimize building blocks for linearity with circuit techniques and careful design tricks. However, there is only so much one can do in that dimension. The other approach is to get rid of blockers before they enter the receiver. One of the famous solutions is incorporating mechanical filters to benefit from their unprecedented narrow passband characteristics. However, as it has been discussed before, the trend toward multi-standard makes it inevitable to get rid of all the off-chip components including filters.
Figure 6.3 depicts the system level diagram of the designed receiver system. The notch blocks are placed right after the antenna. The need for a balun will be explained.

6.2 High-Q Structures on CMOS Platform

The high quality factor structures on CMOS are very desirable since the subsequent blocks in the chain can be designed without having to worry about the out-of-band blockers. Hence, with a specific power budget, designers can squeeze more sensitivity and/or accuracy out of their blocks.
Despite the need for high quality factor components, scaling hasn't been able to help on this matter since the passives' quality, specifically inductors, don't follow the same trend. In

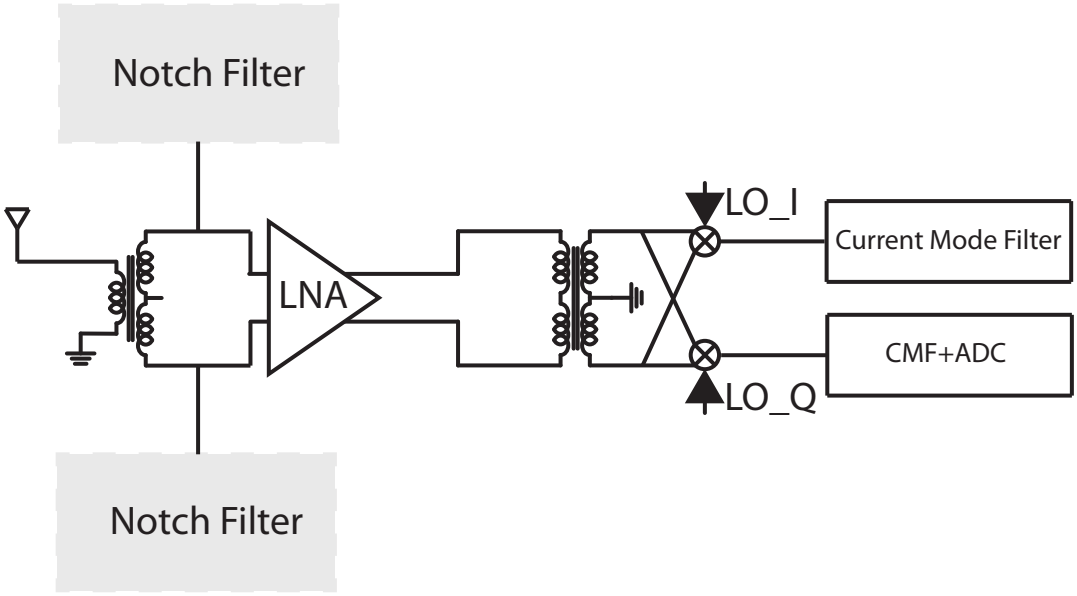

Figure 6.3: System level diagram of the receiver with adaptive notch

fact at some point it would get worse due to constraints on metal thickness and vicinity to substrate. However scaling does improve the quality of CMOS switches and capacitors. This enables designers to synthesize pass-band and notch-filter characteristics through frequency shifting of base-band filters. [48] has demonstrated a high-Q band-pass filter through up-conversion of capacitor low-pass behavior. Band-pass filter in theory have several advantages over notch filters. First is the reuse of the clock of the system to synthesize the band-pass structure since the filter's center frequency aligns with the receivers desired band. Also incorporating the band-pass in theory suffices for rejecting all of the blockers if the quality factor of the structure is high enough. Despite all the advantages of synthesized band-pass filters, the main drawback of those structures comes from the required input signal format. Their driving source should have a high impedance source, or the other way to put it, the input signal should be in current domain. This puts a huge hurdle to have them right after the antenna. Antenna radiation resistance is 50Ω and hence the antenna is considered a voltage drive source. Also high power blockers can cause fluctuations at the RF side of the filter and degrade their performance. On the other side, incorporating a notch filter would partially alleviate this issue since now blockers should ideally see a short circuit at the input of the filter structures, Figure 6.1, and hence there shouldn't be a huge fluctuation on the filter nodes and so close-by high power blockers can be handled more easily. The main drawback for the notch is the need to have separate frequencies for each blocker. However, at any given time, the number of high power blockers at close-by frequencies shouldn't be too many and hence a combination of notch and bandpass filters might be a good solution.

6.3 High-Q Notch Filter Design

Essentially a notch filter is a short circuit at the desired (blocker) frequency. Synthesizing a notch at RF frequencies without an inductor requires incorporating switches and a high-pass filer in base-band. The simplest high-pass filter is again an inductor. At DC it's short and at frequencies high enough it is basically an open-circuit. However, channel bandwidths are between a few hundred KHz to tens of MHz. Inductors which provide high impedance at a few MHz should have value on the order of μH. This means huge area which is not affordable on today's extremely expensive silicon area.
Up to now it seems this idea pushed the issue of inductor design from RF domain to DC. However, there is one difference. One can synthesize the inductor in low-frequency domain with extremely high quality-factor and low form-factor.

The architecture in Figure 6.4 can emulate the inductor if the unity-gain frequency of the amplifier is low-enough. The impedance looking into this structure is:

$$Z_{in} = \frac{R_F}{1 + A(s)} \tag{6.1}$$

Expanding $A(s)$ in terms of its DC gain and pole frequency (assuming a dominant pole) would result in:

$$A(s) = \frac{A_{dc}}{1 + \frac{s}{\omega_{3\text{dB}}}} \tag{6.2}$$

Now for $f \ll (1 + A_{dc})\omega_{3\text{dB}}$ one can rewrite the input impedance as:

$$Z_{in} \approx \frac{R_F}{A_{dc}} + \frac{R_F}{A_{dc} * \omega_{3\text{dB}}} * s \tag{6.3}$$

Where the unity gain frequency $\omega_u = (1 + A_{dc})\omega_{3\text{dB}}$
Thus one model the input impedance with resistor and inductor of values:

$$L \approx \frac{R_F}{\omega_u} \tag{6.4}$$

$$R \approx \frac{R_F}{A_{dc}} \tag{6.5}$$

As can be seen in equations 6.4 and 6.5, there is a trade-off between the magnitude of the inductor and the resistive loss. To have short impedance for high power signals one needs to minimize the resistive loss. For having $\frac{R_F}{A_{dc}}$ about 1Ω and the inductor value on the order of μH, one should use extremely low values for feedback resistor which requires an amplifier with very low unity-gain frequency, Eq. 6.4. Increasing the resistor value can help this issue but at the same time requires more gain to keep the loss below the certain value. This design ended-up with $A_{dc} = 70dB$, Figure 6.5, $R_F = 10K\Omega$ & $L = 10\mu H$, Figure 6.6.

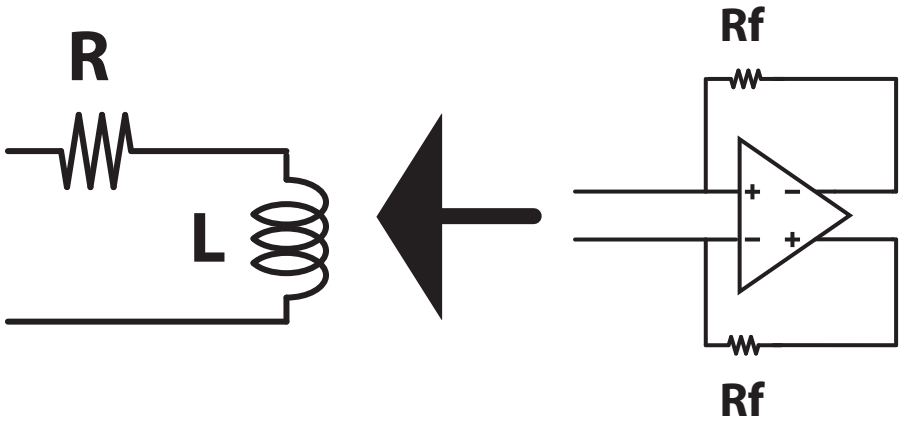

Figure 6.4: Feedback amplifier for synthesizing an inductor

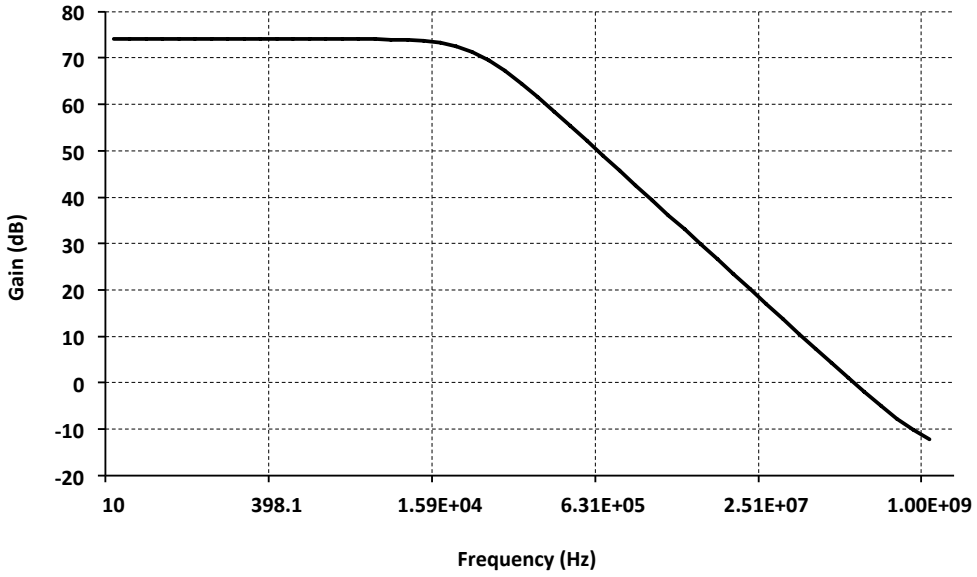

Figure 6.5: Gain of the operational amplifier for the synthesized inductor

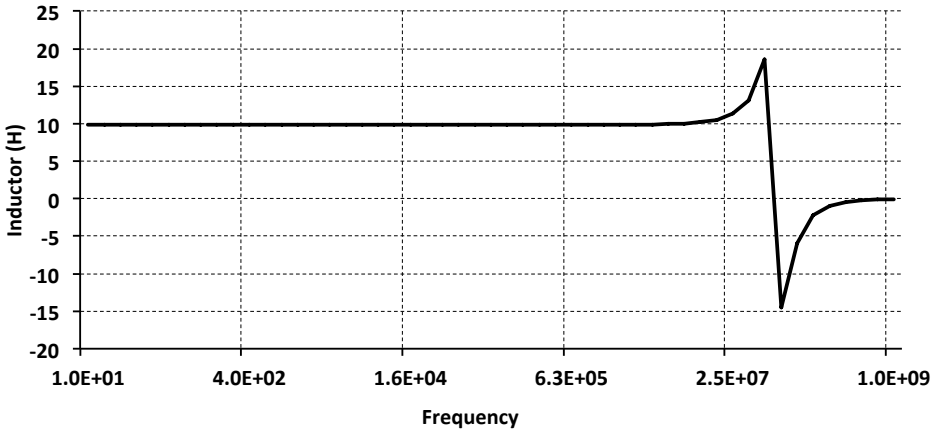

Figure 6.6: Synthesized inductor's magnitude vs. Frequency

After designing the inductor, one needs to shift the transfer function to the desired RF frequency. This can be done with a help of a passive mixer, Figure 6.7. Figure 6.8 shows more detailed representation of the schematics.
As can be seen from the figure, there are two switches from the input of the amplifier which go to AC ground. The reason for placing them is the requirement of constant flow of current for inductors, otherwise the voltage across the inductor would spike. The overlapping time between the switches should be carefully designed to avoid the spike and at the same time not to degrade the quality factor of the notch filter.

As it was discussed before, the input impedance of the synthesized inductor has been minimized to improve the depth of the notch. Figure 6.8 shows that the switches are in series with the synthesized inductor and hence the depth of the notch filter is determined by the sum of their impedances and both are equally important. On the other hand, the transfer function of the notch filter in its pass-band is critical since that would determine the loss of the desired signal.

Since the blocker current flows through the switch, the finite on-resistance of the switch ($\approx 10\Omega$) generates a voltage across the switch and goes highly non-linear with input power $>$ 10dBm(20-40mA will flow to the switch and generate $>$ 200mVacross it, which is enough to start making the NMOS-only switch off). Using a CMOS switch can allow for higher power handling capability.

There is an optimum size and that depends on technology and to be more specific, depends on f_T, Eq. 6.6, as that's the measure of ratio of device resistance to its parasitic capacitance. Hence the more scaled technology would drastically improve the performance of this technique.

$$R_{ON} * (C_{gs} + C_{gd}) = \frac{1}{\omega_T} \tag{6.6}$$

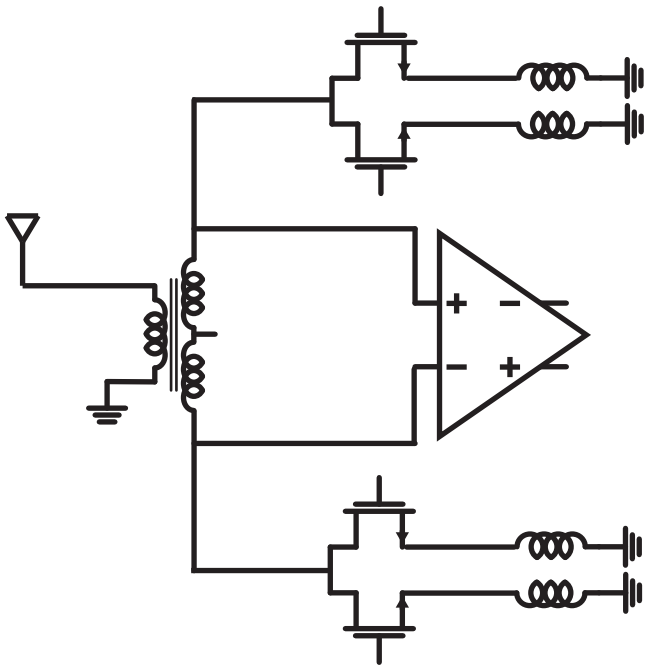

Figure 6.7: Conceptual Schematics of the notch

(need to mention the transformer here)

Figure 6.9 shows the simulation of the notch filter with the balun but the receiver is replaced with its equivalent load. As can be seen in the figure, near 20dB rejection can be achieved with the notch bandwidth of 10MHz.

One of the major concerns for having a block right after the antenna is degrading the sensitivity due to the noise pumped from that block where the received signal is extremely weak. As can be seen in Figure 6.10, the increase in NF is less than 1 dB.

Figure 6.12 shows the block diagram of the receiver with adaptive notch filter. In the next section design of each block would be discussed.

6.4 FRONT END ARCHITECTURE

LNA The g_m stage includes a common source cascode configuration with the balun at the input and a transformer at the output, Figure 6.13. The matching has been achieved by the use of a low-K balun, Figure 6.14. The transformer at the output renders better IP2 performance (Chapter 5). The cascode is a must for the current mode designs since the output impedance of the LNA has a drastic effect on the noise performance other than the traditional benefit of reverse isolation. It's desirable to have as high output impedance as possible. This greatly relaxes the sensitivity of the system to the

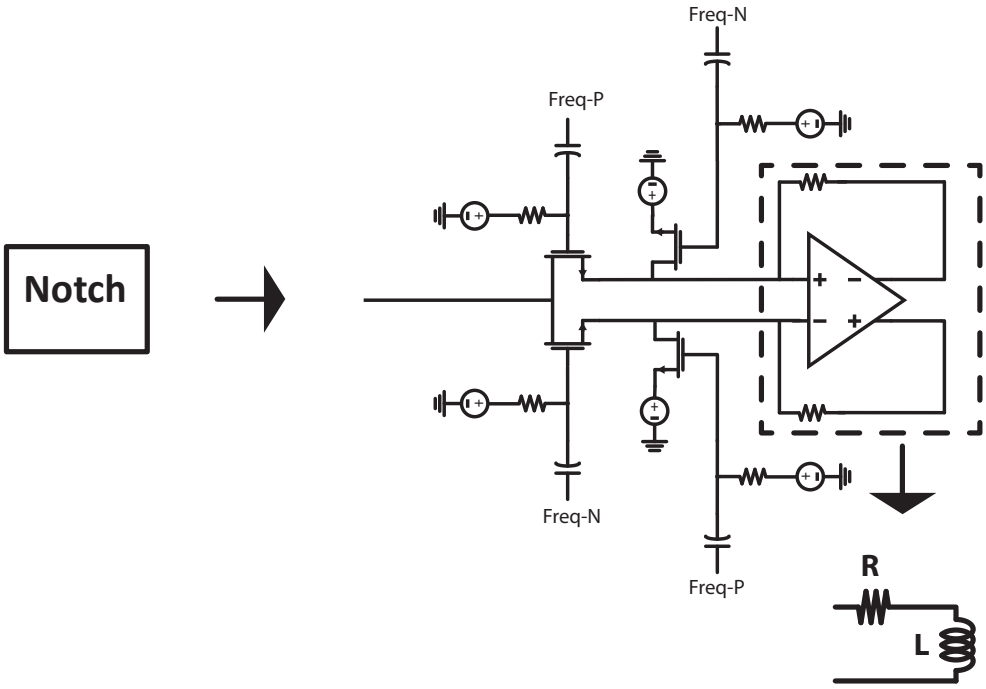

Figure 6.8: Active inductor with switches

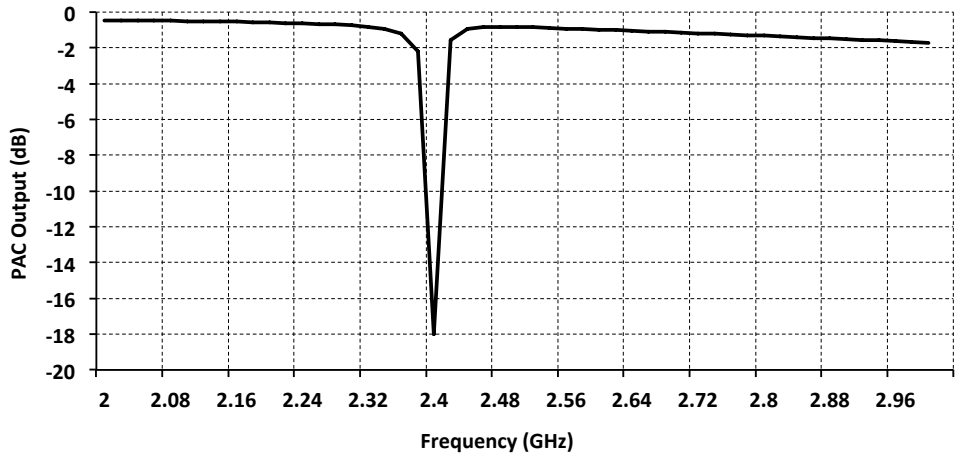

Figure 6.9: Frequency response of the notch filter

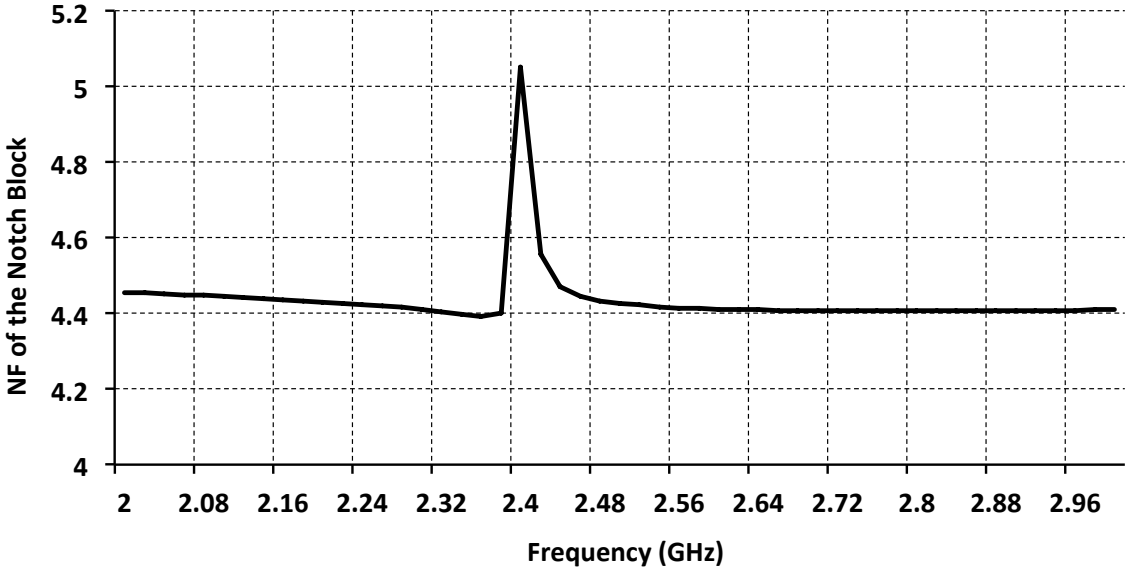

Figure 6.10: NF vs. frequency of the notch

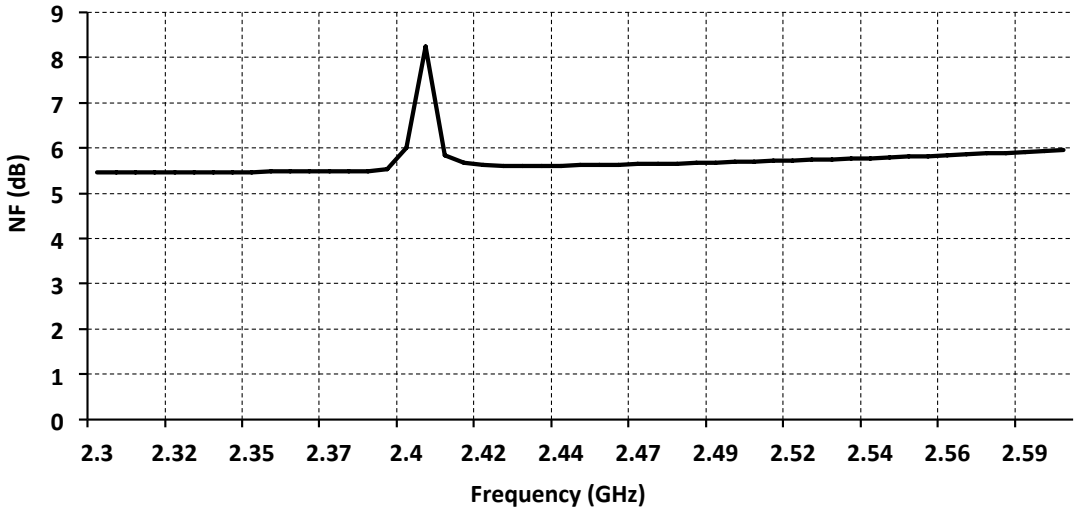

Figure 6.11: NF vs. frequency of the whole system when the notch filter is ON

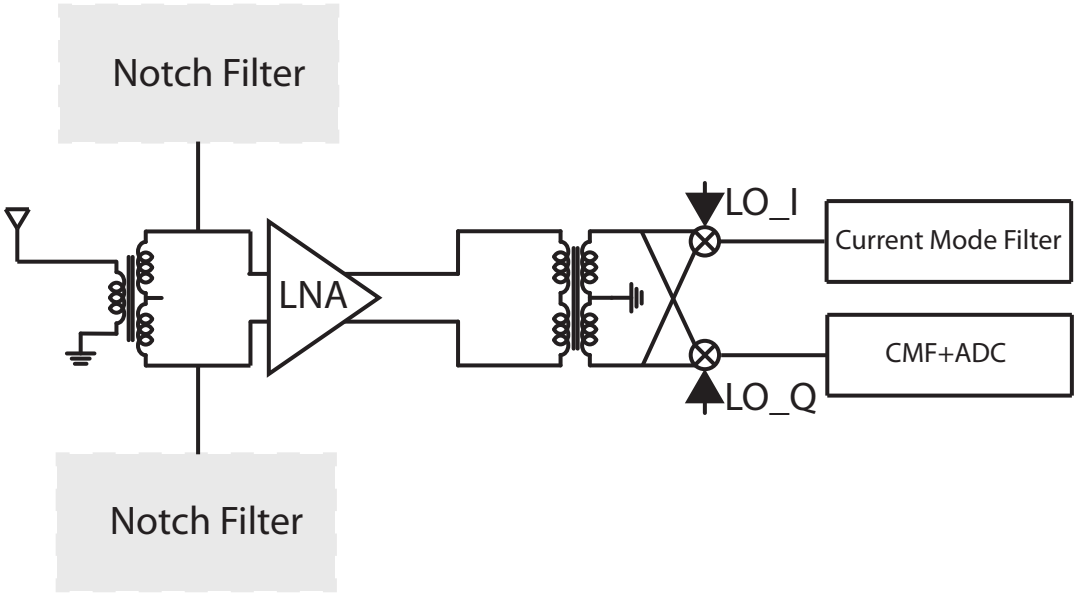

Figure 6.12: Block diagram of the receiver with an adaptive notch filter

base-band design.

For the current mode receivers, there is a specific g_m for attaining the required sensitivity. The advantage of a common source stage is the flexibility to choose the conductance without worrying about the matching as is the case for common gate architectures. It's worth mentioning this choice doesn't sacrifice the **dynamic range**. The reason lies in the fact that lowering g_m to attain a higher saturation point would reduce the sensitivity thus the dynamic range will not increase. Eq. 6.7 shows the equivalent input voltage noise at the antenna considering RF and base-band noise sources. Clearly high g_m is desirable for detecting weak RF signals. In this system, common source architecture has been chosen hence the g_m was not sacrificed and another mechanism is responsible for dealing with large blockers. The LNA burns 10mA from a 1.2V supply.

$$Vnoise_{@input} = \sqrt{\frac{4KT2\gamma}{g_m} + \frac{In_{BB}}{(\frac{\sqrt{2}gm}{\pi})^2}} \tag{6.7}$$

Input Balun A low-k balun has been used which has a two-fold advantage. It increases the impedance of the antenna seen from the LNA side, therefore improves the performance of the notch filter, and matches the antenna to the common source LNA without degrading the noise figure (Figure 6.15). The impedance of the antenna seen from the LNA side increases since the low-k balun has a higher transformation ratio and also the series inductor, L_1k^2, boosts the impedance in the series to parallel conversion.

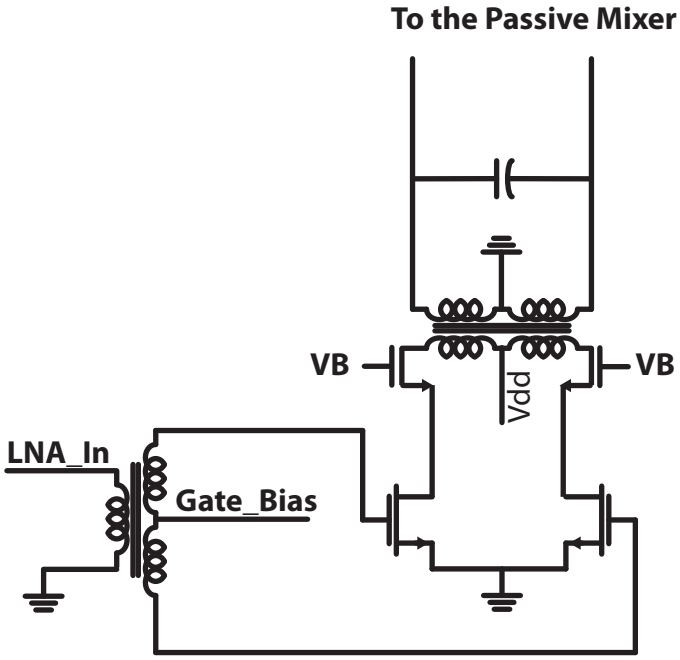

Figure 6.13: Schematic of the LNA with input balun

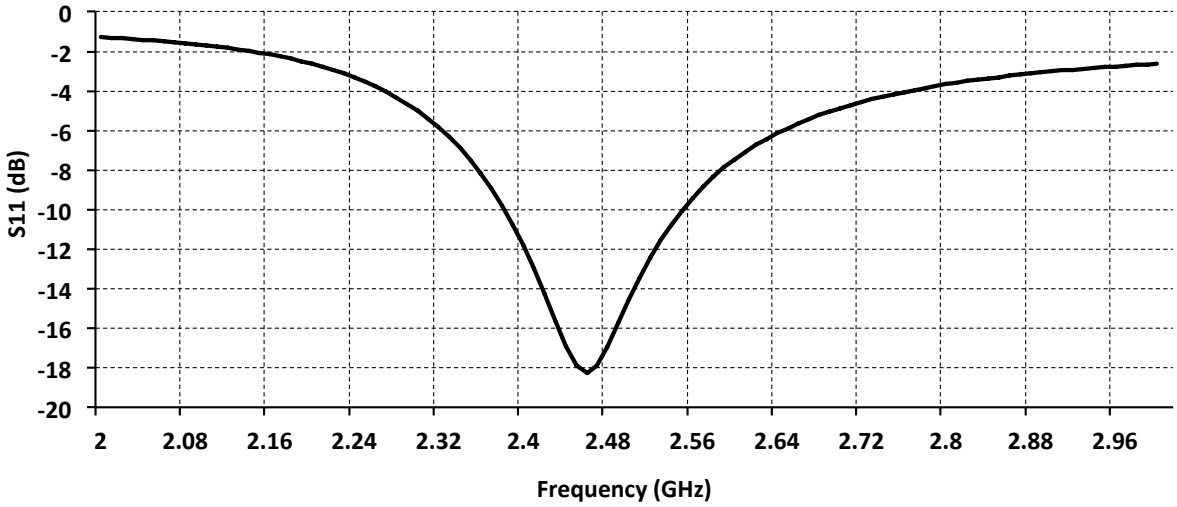

Figure 6.14: Matching of the common source architecture by a low-K balun

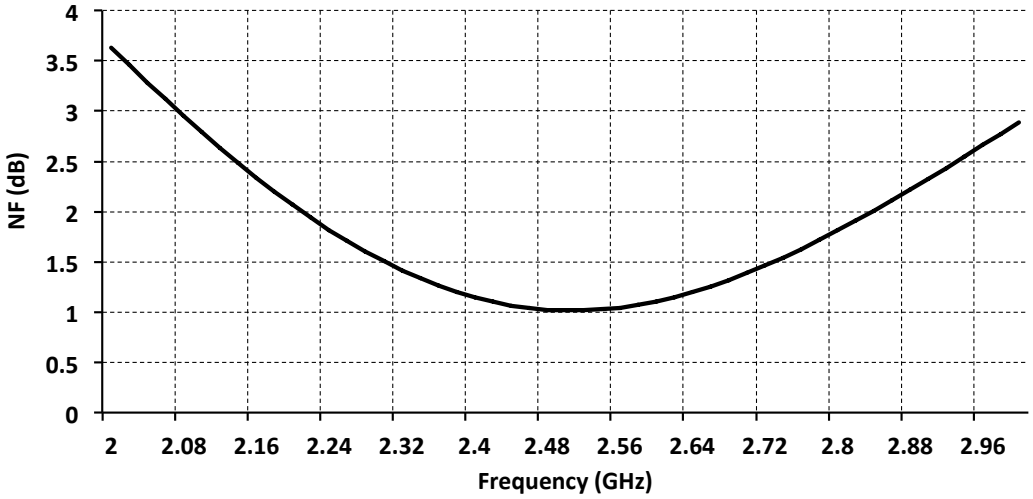

Figure 6.15: Noise figure of the LNA

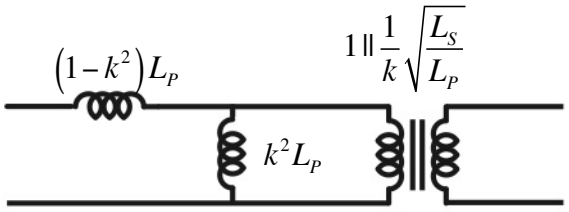

Figure 6.16: Balun equivalent circuit

The notch filter's performance improves since the low impedance of the filter seen by the blocker is now being compared to a higher impedance instead of 50Ω, results in higher attenuation.

Mixer As discussed before, with today's technology, it's not a must to do the frequency translation right after the front-end low-noise module. Nonetheless, the important feature one expects from this module is to translate the signal frequency without folding signals and noise from other parts of the spectrum, or adding their own in-band noise. On top of those, one expects them to have as high linearity as possible. Passive mixers seem to satisfy all the above-mentioned requirements. However, by nature, they are a bi-directional modules in which both sides of the block can interact with one another. This property introduces number of issues which break the traditional way of thinking of two frequency domains as independent domains. Among the different metrics, receiver noise and even-order intermodulation-distortion performance are more susceptible to the bi-directional properties of the mixer. The latter has been extensively

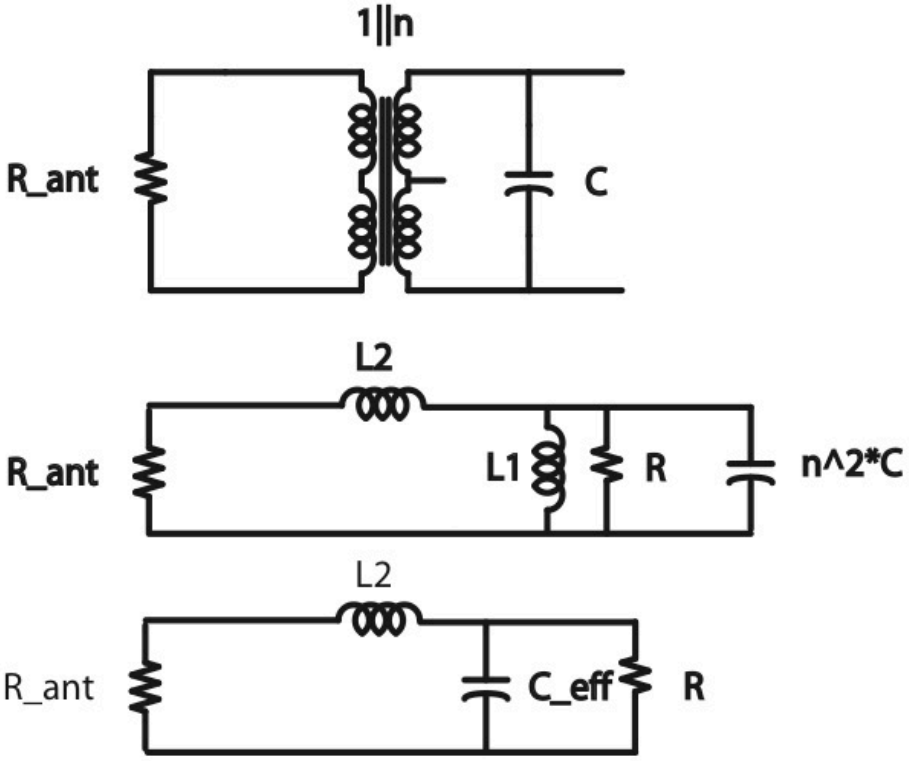

Figure 6.17: Impedance step-up matching

discussed in the previous chapter and the former is the issue of low-impedance looking to the RF side of the mixer. Figure 5.11 and Eq. 5.30 shows the importance of having 25% clock with carefully engineered overlap time and how to set the output impedance of the LNA block. This further proves the importance of moving to higher impedance antennas before adopting mixer-first solution.

Baseband Filter Baseband design criteria in the receiver may seem decoupled from the RF part. Nevertheless, baseband specifications are set dominantly by the RF side in the current mode receivers which use bilateral passive mixers. Baseband specifications can be categorized into two domains, linearity and noise performance.

As discussed, the LNA load impedance can't exceed certain amount in the current mode design to attain the required linearity. LNA load impedance can be distributed between the AC-coupling capacitor after the LNA, the mixer's switches and the baseband input impedance. Managing to keep low impedance gets challenging in SAW-Less receivers since the interferer will pass through the blocks without the mechanical filters could provide. Hence the baseband should provide a low-impedance path across a wide

bandwidth so that the output of LNA would not fluctuate while a far-away blocker is passing through the system.

Noise figure is the other challenging requirement in current mode design, since the baseband noise contribution is a function of R_{IF-RF}. Having 25% duty cycle for clock and high impedance network at the output of the LNA greatly help, nonetheless the baseband block should be low noise.

Figure 6.18 shows the adopted architecture which is based on [59]. The filter is a 4th order biquad which helps to suppress the jammers before digitization. Also it resembles the delta-sigma ADC in a sense that it pushes the noise of input and cascode devices to the out-of-band regime. Equations 6.8 and 6.9 show the output noise due to input and cascode transistors assuming the capacitors C_1 and C_2 are equal and only the 2nd order biquad is considered (up to the C_2). The overall equation is just a cascade of the two 2nd order filters.

Figure 6.19 shows the frequency response of the structure. The bandwidth has been set to 10MHz. Figure 6.20 shows the compression point vs. the blocker's power coming from the mixer (A) at two different off-set frequency. The baseband filter consumes 3.3mA from a 1.2V power supply and its in-band noise is 8pA per $\sqrt{Hz}$.

$$i_{n,input} = \frac{SC(SC + g_m)}{S^2C^2 + SCg_m + g_m^2} \tag{6.8}$$

$$i_{n,cascode} = \frac{g_m SC}{S^2C^2 + SCg_m + g_m^2} \tag{6.9}$$

Current Mode Sigma-Delta ADC The end-goal of all wireless receivers is to convert the data on the carrier into digital format. Where to perform the digitization is a function of architecture and more importantly technology. For 90nm technology, sigma-delta offers great performance in terms of both power consumption and reconfigurability. One can easily trade resolution for bandwidth with a certain power budget. Over-sampled data converter using noise-shaping have easier anti aliasing requirements and higher resolution.

Integrators used for sigma-delta are in discrete-time which employ switch-capacitor technique. The trend in the ADCs for higher conversion rates, lower power consumptions, lower area and lower supply voltages makes deploying discrete time sigma-delta challenging.

High sampling frequency requires high GBW for amplifiers in Discrete-Time (DT) Sigma Delta with high slew rate. Also low-voltage makes switches in SC-circuits non-linear with high resistivity. Deployment of continuous-time Sigma-Delta modulators would require lower amplifier gain-bandwidth and slew rate. This leads to lower power consumption or higher sampling frequency. Anti-aliasing is inherent. High coefficient

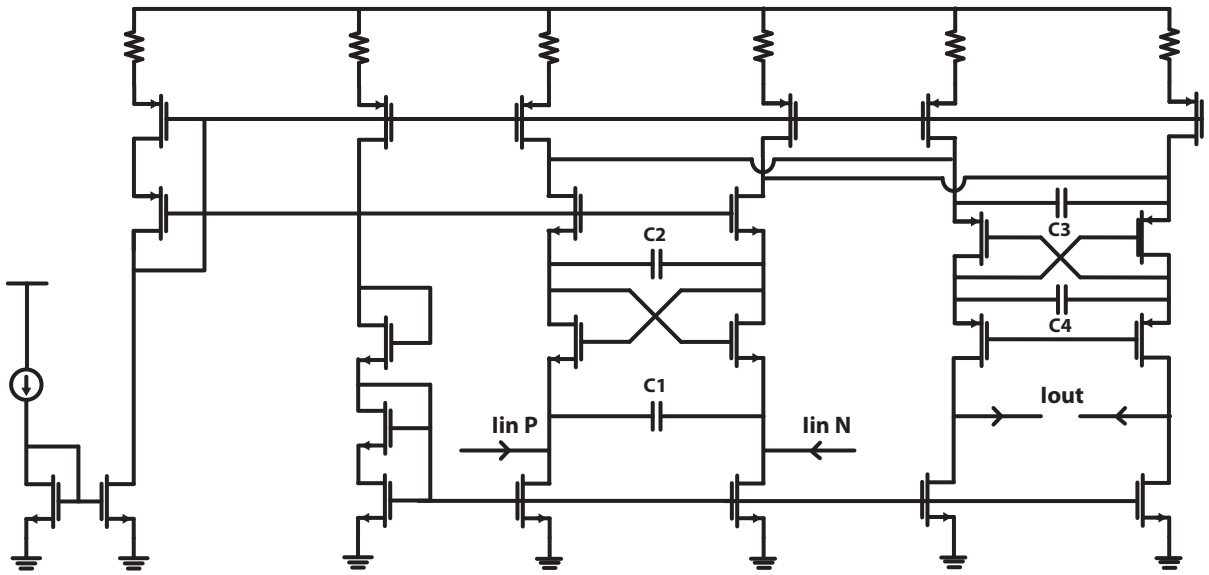

Figure 6.18: Schematic of the current-in current-out baseband filer

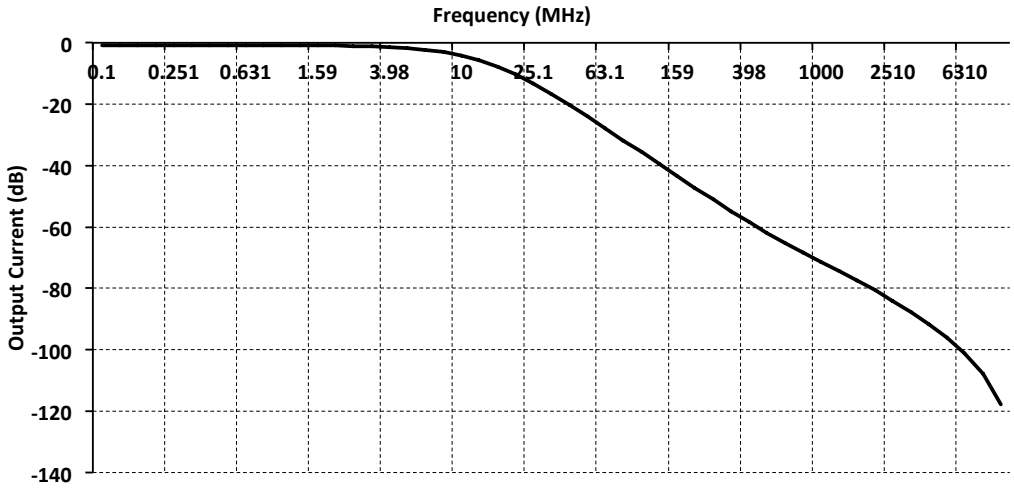

Figure 6.19: Frequency response of the baseband current mode filter

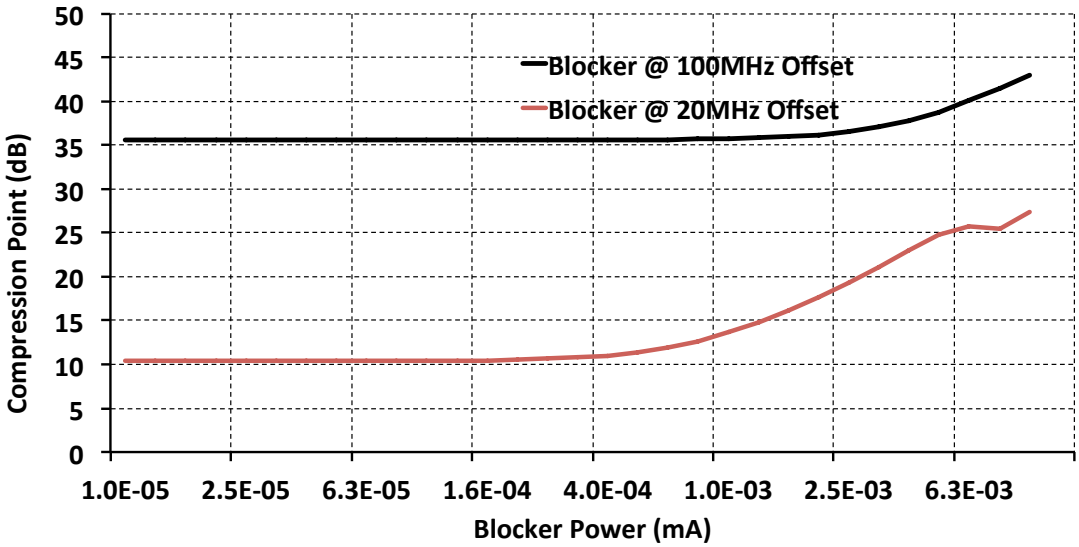

Figure 6.20: Baseband filter compression point vs. blocker power

Table 6.1: ADC Targeted Specification

Baseband Bandwidth (MHz)	**Targeted SNR (dB)**
40 (802.11ac)	> 60
20 (802.11n)	> 66
10 (802.11b/g)	> 72

mismatch and clock jitter sensitivity are the bottleneck of the CT Delta-Sigma converters.

Sampling rate of 1.28GHz has been chosen which gives the OSR of 16, 32 and 64 for 80, 40 and 20 MHz channel bandwidth. The order of CT Modulator is 2 mainly for stability. To meet desired SNR target, Table 6.2, a 4-bit quantizer has been chosen which relaxes jitter, slew rate and dynamic requirements.

The input of the ADC is in current mode and the first integrator converts the signal to the voltage for digitization. The current mode input has a two-fold advantage; better linearity and also the baseband current mode filter placed after the mixer can be connected directly to the ADC.

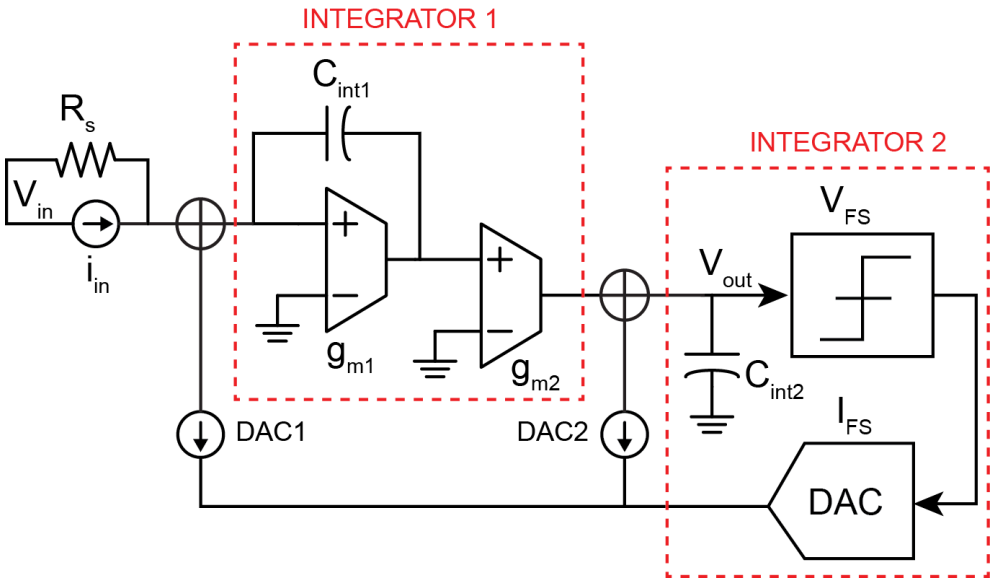

Figure 6.21: Schematic of the sigma-delta ADC with current domain input

6.5 Measurement Results

To test the functionality of the dynamic notch, the receiver has been fabricated, Figure 6.22, packaged and a four layer printed circuit board has been designed for testing, Figure 6.23. The measurement setup is shown in Figure 6.24. A blocker signal and the desired signal are summed and injected into the front-end receiver. In the present prototype, the blocker signal is used directly to drive the notch filter, while in an actual system an injection locked oscillator can be used to automatically track and lock to the blocker. The amount of desired blocker attenuation and the amount of undesired in-band signal attenuation are both measured versus the offset frequency of the blocker (Figure 6.25). As evident, blocker attenuation as large as 20-dB is observed at 40 MHz offset while the in-band attenuation increases by only 2-dB. The resulting increase in noise figure due to the blocker is 4-dB and has been plotted versus frequency along with the effective added dynamic range, Figure 6.26. When all of this data is taken into account, the overall SNR improvement due to the notch filter is as high as 13-dB. This proves that the technique may be effective in attenuating blockers.

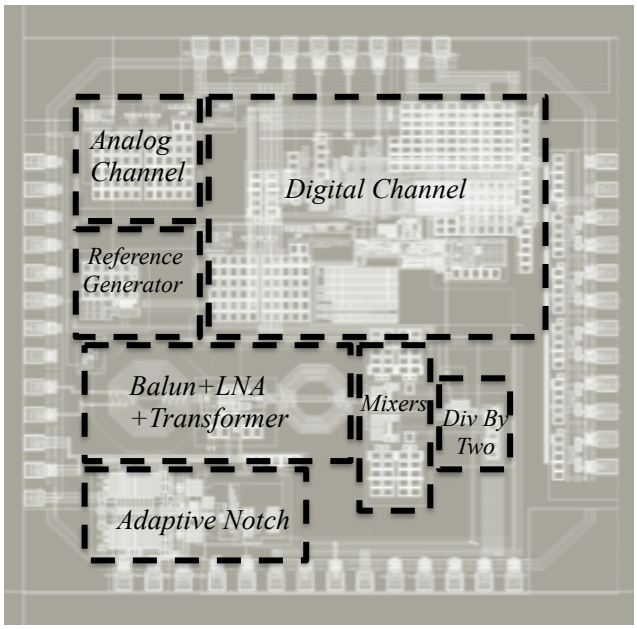

Figure 6.22: Die photo of the current mode receiver with an integrated adaptive notch filter

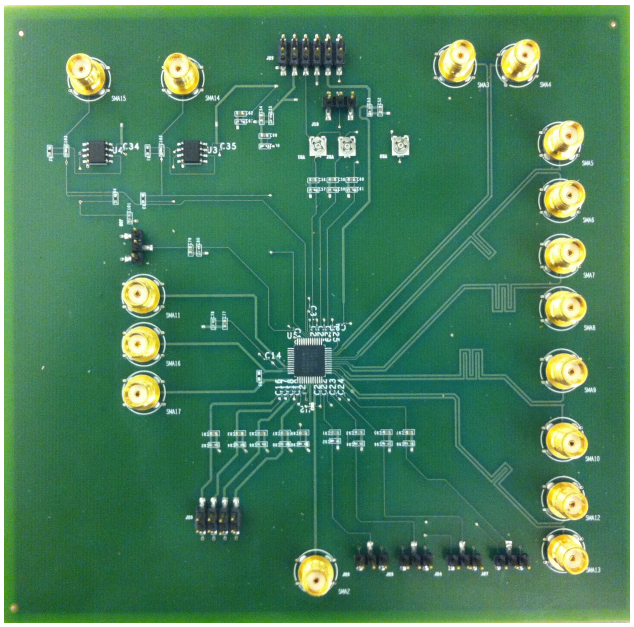

Figure 6.23: PCB of the current mode receiver with an integrated adaptive notch filter

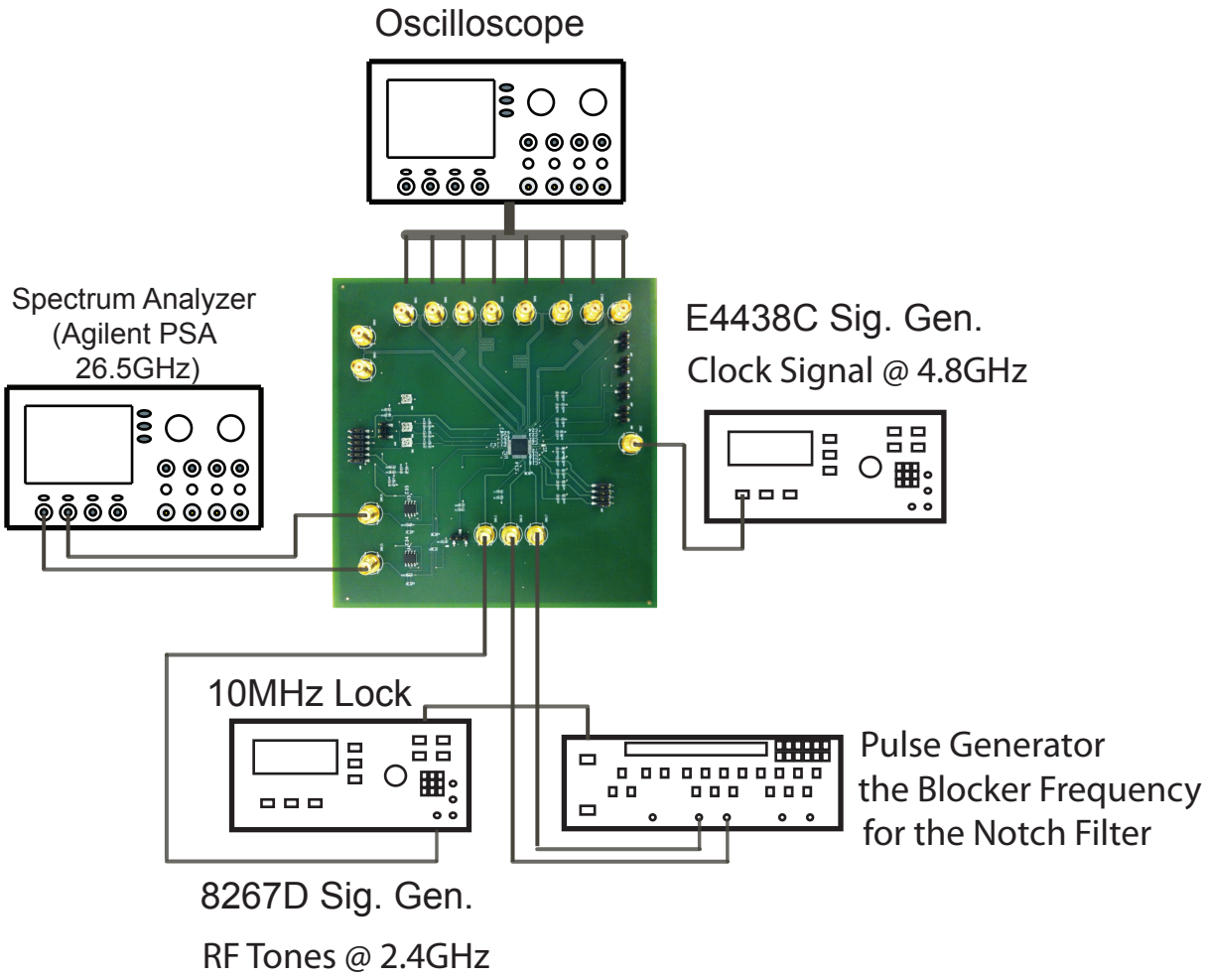

Figure 6.24: Measurement setup

Table 6.2: Adaptive Notch Filter Chip Performance Summary

Frequency	2.5GHz
Gain	110mS
NF	5.5dB
Channel Bandwidth	10MHz
Out-of-Band IIP3	-6 dBm
Out-of-Band IIP2	55 dBm
SNR Improvement	$>$ 10 dBm
Power	52mA (Analog) + 18mA (Digital)
Supply Voltage	1.2V
Technology	90nm

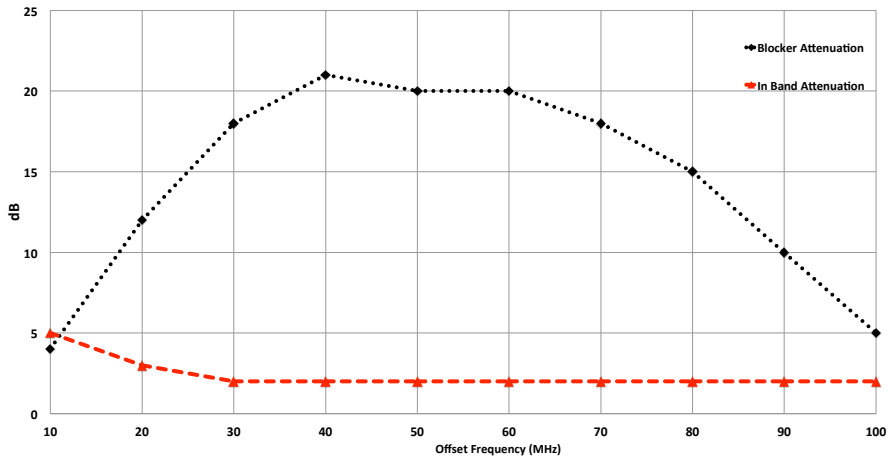

Figure 6.25: Notch performance vs. frequency offset of blocker: Blocker attenuation and undesired signal attenuation

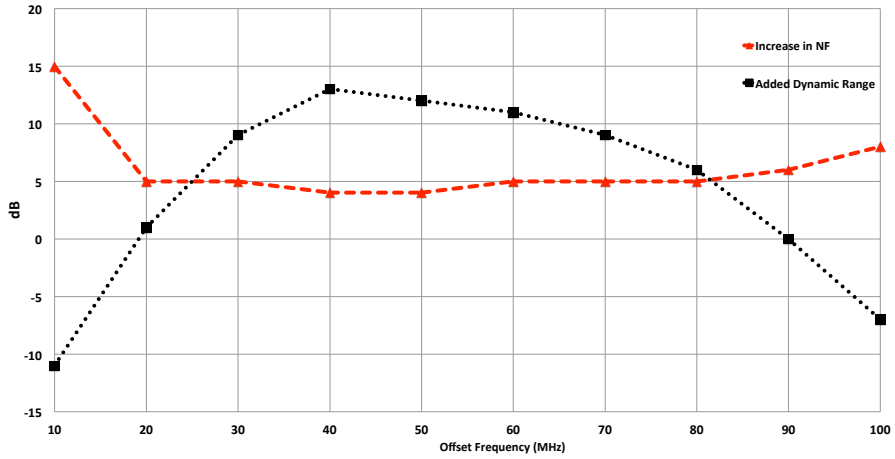

Figure 6.26: Notch performance v. frequency offset of blocker: Increase in NF and the overall increase in receiver dynamic range

Chapter 7

Conclusion

Receiver architecture has been an intense area of research in the past decade. Numerous architectures deviating from classic superheterodyne receiver such as direct-conversion receivers, low-IF receivers and wideband IF have been proposed to overcome external SAW filters resulting in smaller integrated radios. Today there is a growing need to realize a multi-standard radio capable of operation in a wideband of signals. The brute force approach of running multiple separate radios in parallel is impractical due to ever-increasing number of standards. Dedicating separate front-end modules along with SAW filters for each standard would result in extremely large chip area and highly complex designs which requires tremendous design effort. Moreover, transferring the design from one technology node to more advanced nodes would take exponentially more time for designers with these complex systems. These have been extensively discussed in chapter 3 of this thesis.

On the other side, scaling CMOS technology has exacerbated some of the key transistor parameters required for RF/Analog designs. Moreover, reduction in the supply voltage has drained designers' architectural choices which further complicates the evolutionary path toward multi-standard designs. Additionally, supply reduction deteriorates linearity of building blocks which is a big concern when dealing with interferers. Hence traditional architectures don't satisfy the upcoming challenges and new solutions should emerge. Chapter 4 reviewed state-of-the-art solutions proposed for overcoming these challenges and discussed their bottlenecks.

Overall, there are two schools of thought. One is to optimize each building block in the receiver for the maximum linearity possible to tolerate blockers entering the system. The other one is to get rid of blockers as soon as possible so the subsequent blocks can be designed with maximum energy-efficiency.

Chapter 5 discuss the former with the emphasis on one of the toughest criterion to meet for multi-standard applications, IP2. It began with analyzing different mechanisms responsible for generating second-order distortion and identifying the dominant ones. Then it offered an automatic calibration for each individual effect separately, therefor the performance is stable over wide-range of frequencies and power levels.

The latter approach has been discussed in chapter 6 which proposes a novel approach for

removing the blocker right after the antenna by creating a notch at that specific frequency, and the frequency can be adaptive.

The ultimate solution is to filter-out any signal that is high power before hitting the receiver since even our desired signals don't have to be at that power-level range to meet the required SNR.

The progress toward so called software-defined radio has taken major steps. The bottlenecks for removing the SAW filters and widening the bandwidth have been identified and some of their solutions have been proposed. To complete the path, one should not only adopt the new architectures and techniques on the silicon, but also there is a need to do more of a system-level planning from silicon to the package, PCB and the antenna. At the time of writing this dissertation, there is a project in Berkeley Wireless Research Center (BWRC) embarking on this path and as the name of it shows, the goal is to have RF modules programmed like FPGAs, or RF-FPGA.

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