Low Dimensional Materials for Next Generation Electronics

Steven Chuang

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2014-65
http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-65.html

May 13, 2014

Low Dimensional Materials for Next Generation Electronics

By

Steven Chuang

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Ali Javey, Chair
Professor Tsu-Jae King Liu
Professor Peidong Yang

Spring 2014

Abstract
Low Dimensional Materials for Next Generation Electronics
by
Steven Chuang
Doctor of Philosophy in Engineering
University of California, Berkeley
Professor Ali Javey, Chair

Ever since the invention of the transistor, aggressive channel length scaling has been pursued to achieve higher performance and greater packing density. In order to preserve gate control at short channel lengths, the transistor channel has evolved from bulk to low dimensional substrates, such as 2D thin films and 1D nanowires. For scaling to continue, it is vital that we understand the processing and physics of low dimensional materials.

Chapter 2 focuses on quasi-2D ultrathin body InAsSb-on-insulator n-FETs. III-V materials offer high mobilities for excellent on-state currents, and by using a thin film platform we could potentially obtain good off-state characteristics. Previously we have demonstrated high performance InAs-on-insulator n-FETs. In this study we implement InAsSb transistors on SiO_2 and achieve a ~2x enhancement in effective mobility over analogous InAs devices. Top-gated devices are demonstrated with an I_{ON}/I_{OFF} of 10^2-10^3 and an intrinsic conductance of ~0.56 mS/μm.

1D InAs nanowire (NW) n-FETs are explored in chapter 3. In particular, the nanowire transistors are used to study ballistic transport, the theoretical current density upper limit. We experimentally observe ~ 60nm channel length devices reaching ~80% of the ballistic limit. Length dependent studies on the same nanowire are used to extract a mean free path of ~150nm for the 1st and 2nd electron subbands. We find the mean free path to be independent of temperature, suggesting that surface roughness scattering is the dominant scattering mechanism.

Chapter 4 explores 2D transition metal dichalcogenide (TMDC) thin films. TMDC thin films offer the physical limit of scaling, and ohmic contacts to its conduction and valence bands are required for it to realize low power complementary logic. Previous studies show that elemental metal energy levels are pinned near the conduction band of TMDCs and do not offer effective hole injection. To address this we explore a high work function transition metal oxide, substoichiometric molybdenum trioxide (MoO_x, $x<3$), as a hole injection layer to MoS_2 and WSe_2.

MoS_2 diodes and p-FETs are demonstrated with MoO_x contacts. WSe_2 p-FETs with MoO_x contacts show a ~10x on-current improvement over devices with Pd contacts.

In chapter 5 we present heterojunction diodes formed by thin films of InAs and WSe_2. In traditional epitaxial heterojunctions, the number of possible material combinations are limited by lattice constraints. In this study we overcome this restraint by transferring one layer upon another to form a heterojunction. Specifically, InAs/WSe_2 heterojunction diodes are fabricated and measured. A forward/reverse current ratio $>10^6$, reverse bias current $<10^{-12}$A/μm^2, and ideality factor of 1.1 are observed.

To
my family and friends,
colleagues and mentors,
and Elsie

Table of Contents

List of Figures

Acknowledgements

Firstly, I would like to thank Prof. Ali Javey for offering me this truly unique opportunity to work in his lab. Over the past 5 years, I was able to push my limits and develop as a professional under his guidance. He gave insightful suggestions and kind guidance over many occasions. For that I will always be in his debt. He is an extremely hard worker, with painstaking care to detail and endless drive to push the boundaries of science. Not only so, he is also patient and inspirational to everyone he advises. I will look up to him as an example for many years to come.

Secondly, I would like to thank all the professors who helped me during my time at Berkeley. My qualification exam was made possible by chair Prof. Tsu-Jae King Liu and committee members Prof. Peidong Yang and Prof. Daryl Chrzan. It was exhilarating to be able to discuss my research closely with leaders of their respective fields. All of the work presented here could not have been done without close collaborations with various esteemed members of academia. Prof. Jing Guo from University of Florida was instrumental in many key simulation results. Prof. Yu-Lun Chueh from National Tsing Hua University and Prof. Bob Wallace from the University of Texas at Dallas provided us with invaluable material characterizations. Prof. Sanjay Krishna provided us with custom MBE wafers that were essential for many of our III-V studies.

I would also like to take this chance to thank the members of Prof Javey's lab that I was able to work with over the past few years. You all contributed to a dynamic and productive environment that I doubt I would ever find anywhere else. In no particular order…

Dr. Alexandra Ford was the first mentor I met here, and she taught me most of the ropes I use to this very day. Prof. Johnny Ho, Prof. Joseph Fan, Prof. Yu-Lun Chueh and Prof. Hyunhyub Ko also welcomed me warmly early on in my career

and taught me many things. Many of my device fabrication skills were inherited from Prof. Kuniharu Takei, a true processing genius and wizard. Prof. Rehan Kapadia, Prof. Junghyo Nah and Dr. Angada Schid taught me many useful insights in device physics and simulations. Not only is Dr. Corsin Battaglia a solar cell expert, he also is a superb musician and great company at Yoshi's jazz concerts. Dr. Daisuke Kiriya and Dr. Hiroki Ota are astoundingly wise chemists who advised me on experiments, safety and the Japanese culture countless times. Dr. Zhibin Yu, Prof. Chuan Wang and Dr. Yongjing Lin are exceptionally efficient and friendly experimentalists who advised me in many matters. Dr. Tania Roy, you are like a mother to us all, thank you for your care and company.

Many of my studies could not have been done without Hui Fang, and it was great working with him for all these years. Mahmut Tosun, you were a fine companion in many of my adventures in academia. Kevin Chen and Peter Zhao, you two are great company and hard workers, keep it up. Thomas Rembert, I will always remember your moments of brevity and jokes. Sujay Desai, it was always nice talking with you, and thanks for the help with all of those experiments. Mark Hettick, thanks for taking on the various responsibilities of the lab safety officer, I know you'll do great. Maxwell Zheng, it was great discussing physics with you, thanks for all the help. Xingtian Yi, thank you for your assistance with the MoO_x work. Louis Kang, Arunima Balan, and Jerry Chang, it is amazing that you were able to contribute to my work so early in your careers, I have high hopes for you.

I wish all of you the best of luck in the future. Keep in touch.

Finally, a very warm and special thanks to all my family and friends who supported me thus far. You have all helped me achieve my childhood dream of becoming an inventor and a scientist.

Chapter 1

Introduction

1.1 Transistor Scaling and Challenges

Ever since the invention of the transistor, its channel length has been scaled to improve performance and packing density. However it is hard to stop the current flow in a highly miniaturized transistor, which leads to unacceptable increases in off-current and leakage power. Simulations of bulk Si MOSFETs show the off-current increasing by 8 orders of magnitude as the channel length is reduced from 1.5µm to 0.8µm [1]. The origin of this leakage is depicted in figure 1a, where the drain electrode leaks current in regions far from the influence of the gate.

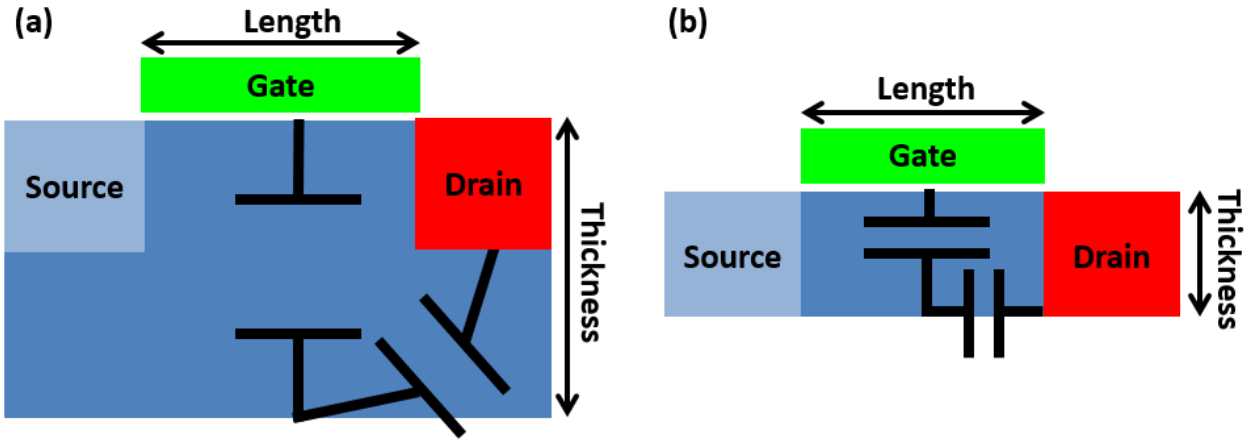

Figure 1.1.: Cross-section schematic of a (a) bulk and (b) thin film MOSFET, depicting competition between the gate and drain.

Shortening the channel length brings the drain electrode influence closer to these regions, further exacerbating the situation. To summarize, it is highly desirable to continue reaping the benefits from device scaling, however doing so requires the suppression of off-state currents.

1.2 Low Dimensional Semiconductors

One route to suppress off-currents while continuing device scaling would be to use low dimensional channels. The idea is to reduce regions far away from the gate where leakage may occur. For example, by moving to thin film substrates, we can reduce the leakage paths at the bottom of the channel (Figure 1.1b). To this end, many different device structures have been proposed as shown in figure 1.2.

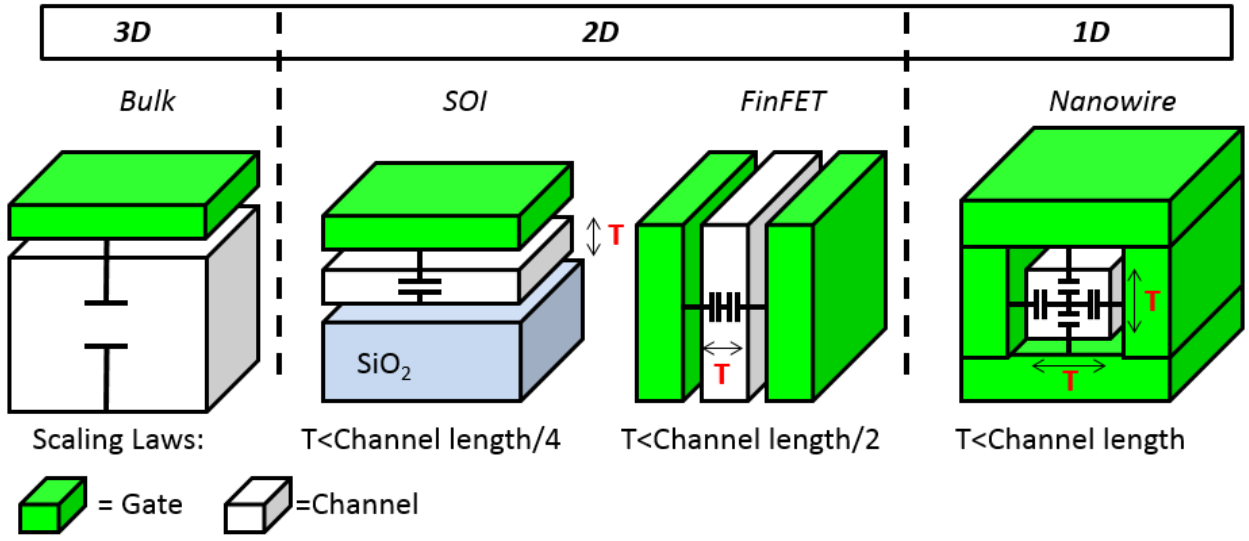

Figure 1.2.: Low dimensional semiconductor transistor structures and their respective scaling laws [2].

The question then becomes how much we need to reduce these dimensions, as highly scaled features are difficult to fabricate and process. The maximum thickness and/or width that a transistor can tolerate with acceptable short channel effects can be approximated with scaling laws, listed at the bottom of figure 1.2 [2]. The implications are daunting: ITRS predicts that in 7 years we will reach 10 nm physical gate lengths for high-performance logic [3], and channel widths/thicknesses must be a fraction of that. It is crucial that we understand the device physics and processing of low-dimensional semiconductors in order to prepare for highly scaled devices of the future.

In this dissertation, the use of novel materials to explore the physics of low dimensional devices will be discussed.

1.3 III-V Semiconductor Thin-films and Nanowires

Low dimension III-V semiconductors are attractive candidates for future electronics. Traditionally, III-V semiconductors have been known for their excellent transport properties. InAs, in particular, offers electron mobilities 10x greater than conventional silicon [4]. By moving to low dimension channels, we can potentially achieve exceptional on-state performance with suppressed off-state leakage. In addition InAs has a relatively large Bohr radius [5], therefore we expect to observe quantization effects in low dimensional InAs devices.

One route towards low dimensional InAs involves transferring thin films onto SiO_2/Si substrates, as depicted in figure 1.3 below.

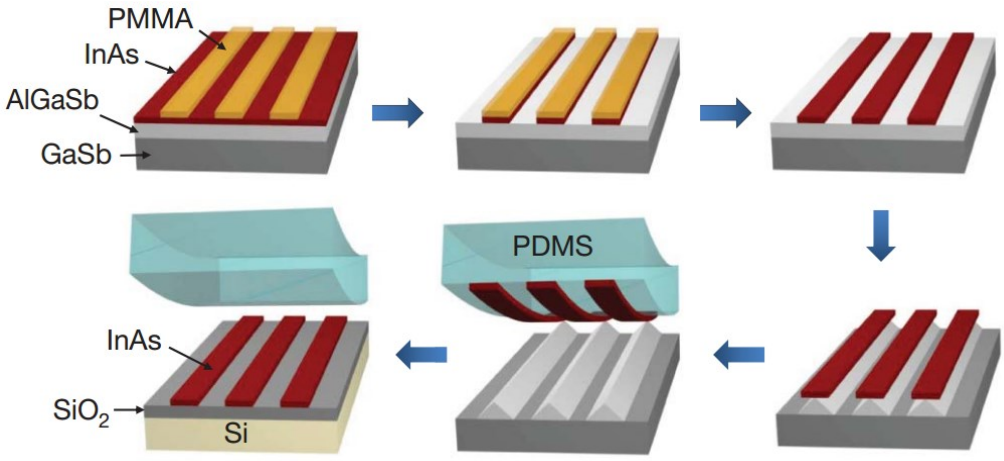

Figure 1.3.[1] [6]: Processing schematic for transferring ultra-thin InAs membranes onto a SiO_2/Si substrate. A PMMA mask is used as a mask to etch selected regions of InAs epitaxially grown on a GaSb substrate. Afterwards the PMMA is removed and the AlGaSb sacrificial layer is partially etched to allow the InAs membrane to be transferred onto PDMS. The InAs thin film is then transferred from the PDMS onto a SiO_2/Si wafer.

[1] Figure reproduced with permission of authors and publisher from H. Ko, K. Takei, R. Kapadia, S. Chuang et al., "Ultrathin compound semiconductor on insulator layers for high performance nanoscale transistors", Nature, 468, 286–289, 2010.

This platform holds significant advantages over previous InAs thin film studies. InAs thin films were traditionally grown on III-V substrates, however it was highly desired to incorporate them onto robust, industry-friendly Si substrates. Previous incorporations of InAs onto Si involved the complex growth of numerous buffer layers in order to account for lattice differences [7]. In our method, we use a much simpler 3 layer III-V stack and, through a series of selective wet etches, transfer the InAs layer onto SiO_2 (Figure 1.3). High performance transistors were demonstrated, indicating high material quality and potential for logic applications [6].

After having demonstrated the viability of InAs-on-insulator transistors, we were spurred to fabricate higher performance devices by incorporating other materials on SiO_2/Si. Notably, InSb is one of the few materials with a higher mobility than InAs. With this in mind, chapter 2 reports the incorporation of Sb into the InAs thin film in order to improve the mobility of the resulting transistors.

In another method to obtain low dimension III-V substrates, single crystalline InAs nanowires are grown via a vapor-liquid-solid (VLS) technique and drop-casted onto SiO_2. This platform offers a rare opportunity to study the limit of transistor on-state performance. The highest on-state current regime is characterized by ballistic transport, where carriers reach extremely high velocities due to the lack of scattering events. InAs offers low carrier effective masses and high carrier mean free paths, making them prime candidates to observe ballistic transport. In addition, by using quantized nanowires, we can limit conduction to single subbands and extract their carrier velocities from I-V characteristics. This study is presented in chapter 3.

1.4 Transition Metal Dichalcogenide Thin Films

Transition metal dichalcogenide (TMDC) transistors are motivated by the excruciating difficulty of fabricating ultra-thin devices out of 3D crystal structures (Si, III-V, Ge etc.). A 3D crystal is defined by symmetry operations that extend infinitely in all 3 dimensions, and only by breaking these definitions can a surface be formed. Thus even ideal surfaces of 3D crystals are, at an atomic scale, rough and uneven. As we approach atomic level thicknesses, this roughness will cause unacceptable thickness variations across the film. The physical limit of scaling, i.e. a single atomic layer substrate, cannot be formed from 3D crystals as the surface roughness will inevitably lead to holes in the film. In addition, 3D crystal surfaces

are known to form dangling bonds and native oxides, which interfere with gate control in transistor applications.

In contrast, TMDCs are one of the few materials known to exhibit 2D crystal structures. By definition these structures terminate in perfectly flat surfaces. Ideally, they offer atomically uniform thicknesses and surfaces that do not form dangling bonds or native oxides. In addition, the thickness uniformity makes it possible to fabricate atomically thin films. The transistors fabricated with these films exhibit exceptional gate control, with down to 60mV/dec subthreshold swings demonstrated at room temperature [8].

One of the toughest challenges facing TMDC transistors are ohmic contacts to electrons and holes. Large contact resistances to TMDCs hinder intrinsic carrier transport studies and mask the benefits from channel length scaling. Efficient hole injection into TMDCs, in particular, has not been well studied and is needed to realize low power TMDC complementary logic. Chapter 4.3 describes a method to obtain low resistance hole contacts to TMDCs. Specifically, sub-stoichiometric MoO_x is used as a high work function contact to MoS_2 and WSe_2 to reduce their respective hole Schottky barrier heights.

1.5 InAs/WSe_2 Thin Film Heterojunctions

Junctions play a major role in a transistor's characteristics. Transistors are named after their defining junctions, be it the metal-oxide-semiconductor field-effect transistors (MOSFETs), Schottky junction transistors, or bipolar-junction transistors (BJTs). Understanding and developing new junctions is critical for enabling not only high performance transistors, but also novel devices and applications.

Currently, single crystalline semiconductor heterojunctions are grown by epitaxial techniques, and they require the lattice constants of participating materials to be similar. This severely limits the variety of heterojunctions that could be fabricated. In chapter 5, we combine the thin film transfer techniques previously described to explore novel InAs/WSe_2 heterojunctions. Notably this heterojunction consists of 2 different crystal structures, and is impossible to fabricate with traditional epitaxial methods.

References

[1] N. Arora, *MOSFET Modeling For VLSI Simulation: Theory And Practice*; World Scientific: Singapore, 2007.

[2] M.-D. Ko, C.-W. Sohn, C.-K. Baek, and Y.-H. Jeong, IEEE Transactions on Electron Devices, 60, 2721 (2013).

[3] International Technology Roadmap for Semiconductors (http://public.itrs.net/).

[4] J. A. del Alamo, Nature, 479, 317, (2011).

[5] H. T. Grahn, *Introduction to Semiconductor Physics*; World Scientific: Singapore, 1999.

[6] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, A. Javey, Nature, 468, 286–289, 2010.

[7] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, R. Chau, IEEE IEDM Tech. Digest 2009, 319–322 (2009).

[8] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, A. Javey, Nano Letters, 12 (7), 3788–3792, 2012.

Chapter 2

[2]Quasi-2D InAsSb Transistors

2.1 Introduction

High mobility semiconductors show great promise as the channel material of ultra-fast, low-power field-effect transistors (FETs) and have been actively explored in the past few decades [1-4]. The demonstration of high performance InAs XOI n-FETs motivates the search for III-V candidates with even higher mobilities. Among them, mixed anion $InAs_xSb_{1-x}$ has one of the highest electron mobilities and saturation velocities of all known semiconductors [5]. However, it also has one of the smallest bandgaps [5, 6]. For such devices, ultrathin body (UTB) architectures are essential to enable acceptable leakage currents. Conventionally, $InAs_xSb_{1-x}$ devices have been fabricated as complex quantum well structures on III-V or Si substrates. While the devices exhibited promising initial results, due to leakage from gate and/or not fully depleted body, they suffered from high I_{OFF} [7-10]. In consideration of supporting substrates, Si is a well-established material and is highly preferred over III-V semiconductors. However, using direct MBE growth to integrate both n and p channel materials onto Si for CMOS will be very challenging due to the large lattice mismatch between different desired materials and Si/SiO_2. Previously, we demonstrated the transfer of InAs ultra-thin membranes onto Si/SiO_2 substrates to form high performance n-FETs, termed

[2] © 2012 IEEE. Reprinted, with permission, from Steven Chuang et al., Ultrathin-Body High-Mobility InAsSb-on-Insulator Field-Effect Transistors, IEEE Electron Device Letters, April 2012.

"XOI" in analogy to the well-established Silicon-on-Insulator (SOI) field. The mobility of InAs XOI devices was found to be as high as ~5000 cm^2/Vs for body thicknesses of ~>20 nm and decreases to ~1600 cm^2/V-s when scaled down to 8 nm in thickness [11]. Here, we extend the XOI concept to $InAs_xSb_{1-x}$ as a demonstration of even higher mobility III-V FETs, especially for ultrathin body thicknesses of <10 nm which are required for scaled transistors based on small bandgap semiconductors.

2.2 Thin Film Transfer and Device Fabrication

Firstly, ultrathin $InAs_{0.7}Sb_{0.3}$ layers of different thicknesses (T_{InAsSb}=7 and 17 nm) were transferred onto Si/SiO_2 substrates following the epitaxial layer transfer (ELT) technique described previously [11]. $InAs_{0.7}Sb_{0.3}$ was grown on a 60 nm $Al_{0.4}Ga_{0.6}Sb$ sacrificial layer on GaSb substrate by molecular beam epitaxy. The InAsSb layer was then pattern etched by using a mixture of citric acid (1 g/ml of water) and hydrogen peroxide (30%) at 1:20 volume ratio (etch rate, ~0.7 nm/sec), and the AlGaSb layer was selectively etched by ammonium hydroxide (1.5%, in water). Ni (T_{Ni} = 40 nm) source (S) and drain (D) electrodes were fabricated using lithography and metallization. For top gated FETs, a 10 nm-thick ZrO_2 gate dielectric was deposited by atomic layer deposition (ALD) at 115 ^oC, followed by a forming gas anneal at 150 ^oC for 10 min. Subsequently, Ni top-gate (G) electrodes, overlapping the S/D, were fabricated. Fig. 2.1(a) shows a TEM image of the 7 nm InAsSb layer on Si/SiO_2 with a Ni/ZrO_2 high-κ stack, while the HRTEM image in Fig. 2.1(b) illustrates the single-crystallinity of the InAsSb channel, exhibiting highly abrupt interfaces between InAsSb and Si/SiO_2 without any visible voids.

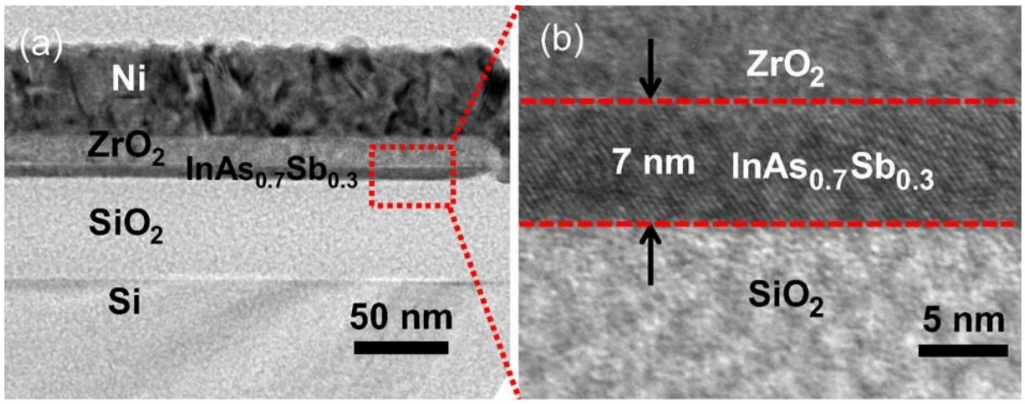

Figure 2.1. (a) TEM image of a ~7-nm-thick $InAs_{0.7}Sb_{0.3}$ XOI (body oxide thickness of 50 nm) substrate. The nanoribbon is coated with a ZrO_2/Ni bilayer (~25 and ~50 nm, respectively). (b) HRTEM image showing the single-crystal structure of an $InAs_{0.7}Sb_{0.3}$ nanoribbon with atomically abrupt interfaces with ZrO_2 and SiO_2 layers on the top and bottom surfaces, respectively.

2.3 Back-gate Devices and Mobility Extraction

In order to probe the electrical properties of InAsSb XOI FETs, back-gated devices were fabricated and characterized. A 50 nm thick thermally grown SiO_2 was used as the gate dielectric. Fig. 2.2(a) shows the transfer characteristics of 7 nm and 17 nm thick InAsSb XOI FETs at V_{DS}=0.5 V, for source-drain separation lengths L=2.7 μm and 3.4 μm, respectively.

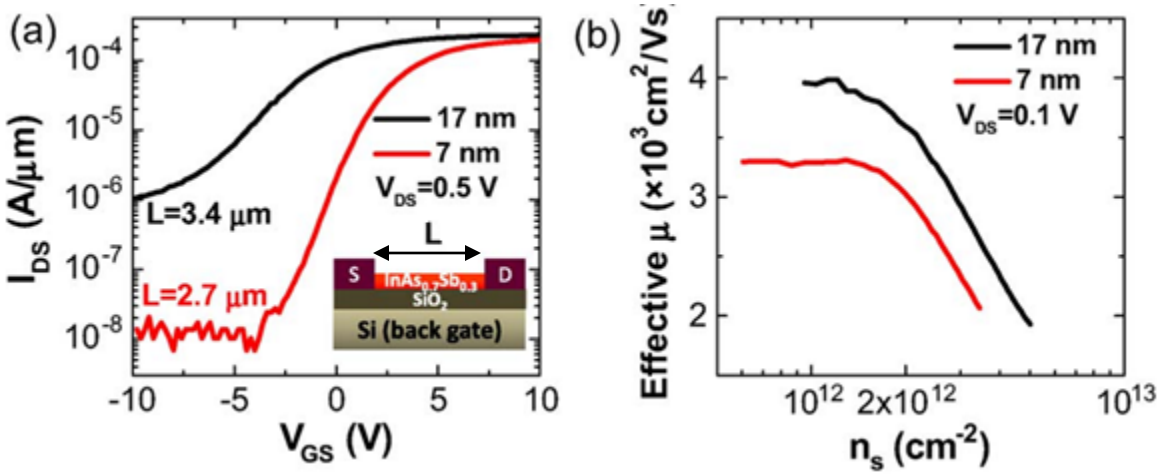

Figure 2.2. (a) Typical back gate I_{DS}-V_{GS} for 7 nm and 17 nm thick $InAs_{0.7}Sb_{0.3}$ XOI n-FET on 50 nm SiO_2 at V_{DS}= 0.5 V. The inset shows the schematic of the back gated devices. (b) Effective mobility extracted from I_{DS}-V_{GS} characteristics at V_{DS}= 0.1 V.

The back-gated 7 nm thick device exhibits an I_{ON}/I_{OFF} ratio of ~10^4, more than 2 orders of magnitude greater than the 17 nm device. This significant improvement in OFF current can be attributed to better electrostatic control from gating a thinner body [12]. The raising of bandgap by confinement will also contribute to a lower OFF current, since the barrier for thermionic emission of carriers would be higher. Specifically, since InAsSb has a large Bohr radius (between 34 nm and 65 nm, which are for bulk InAs and InSb, respectively [13]), heavy quantum confinement is expected in ultra-thin body membranes. An approximate expression for the ground state energy of electrons and holes can be derived by solving the 1-D Schrodinger Equation for a finite potential well. The effective bandgap would be 0.6 eV and 0.32 eV for 7 nm and 17 nm $InAs_{0.7}Sb_{0.3}$, respectively. Fig. 2.2(b) shows the extracted effective mobilities (μ_{eff}) as a function of the 2D carrier density at V_{DS}= 0.1 V for the long-channel, back-gated FETs (with T_{ox}=50 nm) shown in Fig. 2.2(a). The mobility was obtained from the expression,

$$\mu_{eff} = \frac{\partial I_{DS}}{\partial V_{DS}} \frac{L_G}{C_{ox}(V_G - V_T - 0.5V_{DS})}$$

where V_T is the threshold voltage extracted from the linear I_{DS}-V_{GS} curve, $C_{ox} = \varepsilon_{ox}\varepsilon_0 / T_{ox}$ is the gate oxide capacitance per unit area (ε_{ox} ~3.9 is the dielectric

constant of SiO_2, ε_0 is the vacuum permittivity, and T_{ox}=50 nm is the SiO_2 thickness). Here, we utilized the simple parallel plate model and the effects of quantum capacitance and fringe field are ignored, which is a valid assumption given the thick gate oxide (i.e., small oxide capacitance) of the back-gated devices and the channel width>>thickness.

The effective mobility histograms extracted for long-channel $InAs_{0.7}Sb_{0.3}$ (thickness, 7 nm and 17 nm) and InAs (thickness, 8 nm, and 18 nm) XOI FETs are shown in Fig. 2.3.

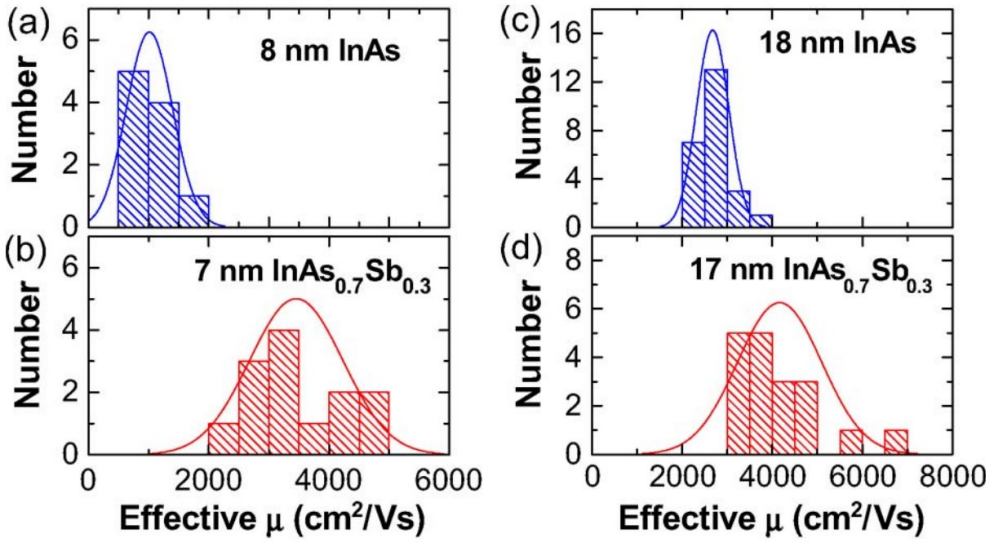

Figure 2.3. Histogram plots of effective mobility (at n_s= 2×10^{12} cm^{-2}) in InAs and InAsSb XOI n-FETs of (a) T_{InAs}=8 nm, (b) $T_{InAs0.7Sb0.3}$=7 nm (c) T_{InAs}=18 nm, and (d) $T_{InAs0.7Sb0.3}$=17 nm.

Note that the dimensions (including channel width, *W,* typically ~320-380 nm) of each device was directly measured by SEM and used to normalize the current and extract mobilities. InAsSb devices exhibit average effective mobilities of ~3400 cm^2/V-s and ~4100 cm^2/V-s at n_s= 2×10^{12} cm^{-2} for 7 nm and 17 nm thicknesses, respectively. Note that the mobility degradation with thickness is mainly due to enhancement of surface roughness and surface polar phonon scattering [14]. These mobility values present ~2× enhancement over InAs XOI FETs with similar thicknesses (Fig. 2.3). The variation of the mobility may be caused by the different amount of interface trap states (D_{it}) introduced during processing. This mobility improvement coincides with the previously reported Hall mobility difference

between $InAs_{0.7}Sb_{0.3}$ (μ_{Hall}~42,000 cm^2/V-s) and InAs (μ_{Hall}~22,000 cm^2/V-s) [15] at a doping concentration of 5×10^{16}-3×10^{17} cm^{-3}, which is around the electron density in our unintentionally doped samples. Hence it is promising to further enhance the mobility by increasing the Sb content of the channel, although this comes at the cost of a lower band-gap.

2.4 Top-gate Devices

Next, the electrical properties of top-gated InAsSb XOI FETs are explored. As shown in Fig. 2.4(a) and (b), a 7 nm thick InAsSb FET (L=500 nm) exhibits I_{ON}/I_{OFF} ~2×10^2 when defining I_{OFF} at V_T-1/3V_{DD} and I_{ON} at V_T+2/3V_{DD} at room temperature (V_T is taken at I =10^{-6} A/μm), and exhibits an I_{ON} of ~0.38 mA/μm at V_{DS}=V_{GS}=0.6 V. A subthreshold swing of SS ~178 mV/dec is obtained, which is larger than that of InAs FETs (SS ~125 mV/dec) [16]. This suggests that the InAsSb interfaces exhibit a higher density of trap states than InAs. The source contact resistance, R_S, of the 7 nm thick InAsSb was extracted using the Transmission Line Method. The extracted R_S is ~200 Ω•μm, which is close to that of 8 nm InAs FETs' (~230 Ω•μm) [16].

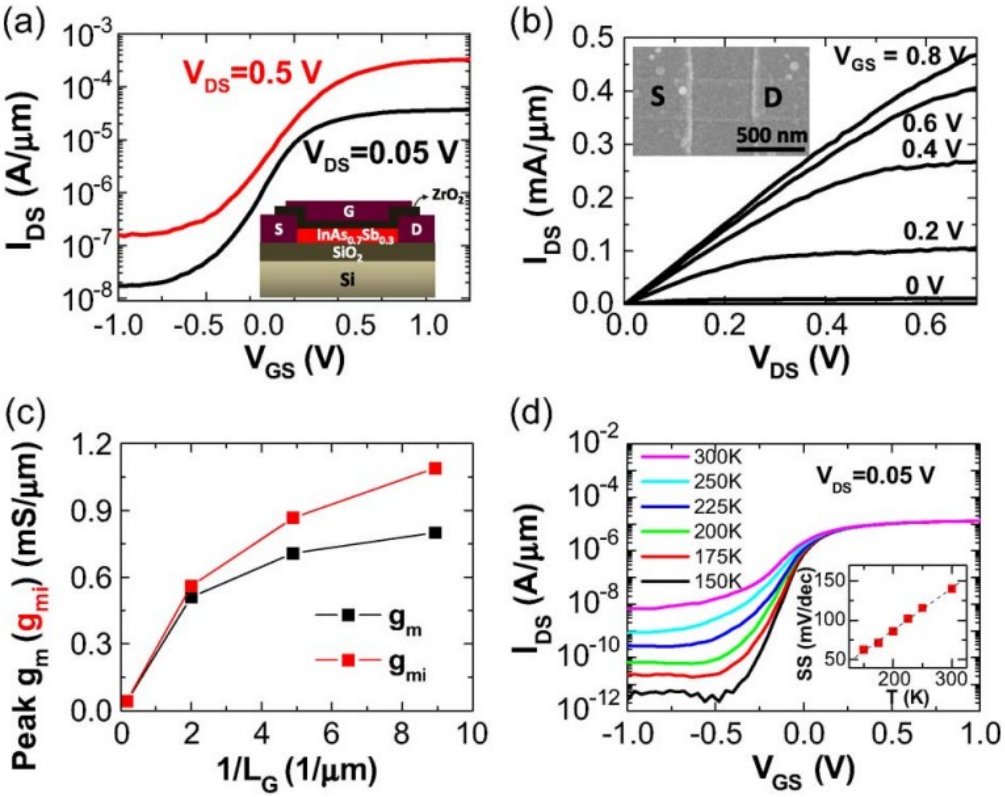

Figure 2.4. (a) Top gate I_{DS}-V_{GS} for a 7 nm thick $InAs_{0.7}Sb_{0.3}$ XOI n-FET at V_{DS}= 0.05 and 0.5 V. The gate length is ~500 nm. Inset is schematic of top gated InAsSb XOI FETs. (b) I_{DS}-V_{DS} curve of the same device in (a). Inset shows the top view SEM image (false-color) of a representative device. (c) g_m and g_{mi} as a function of the gate length. (d) Top gate I_{DS}-V_{GS} as a function of temperature at V_{DS}=0.05 V. Inset shows SS as a function of T, with linear fitting.

2.5 Extrinsic and Intrinsic Transconductance

The extrinsic transconductance g_m of the top-gated FET (L~500 nm) at V_{DS}=0.5 V, peaked at ~0.51 mS/μm. The intrinsic transconductance,

$$g_{mi} = g_m / (1 - g_m R_S - g_d R_{SD})$$

was extracted to exclude the contact resistance effects (R_{SD}=R_S+R_D=2R_S). The peak intrinsic transconductance of the device is ~0.56 mS/μm. Fig. 2.4(c) shows g_m and g_{mi} as a function of inverse gate length, which exhibits non-linearity for shorter

channel lengths, possibly arising from quasi-ballistic transport. Further study need to be done to improve the I_{OFF} and *SS* of sub-500nm channel length devices. Compared to previously reported $InAs_{0.8}Sb_{0.2}$ QWFETs (L=1 μm, g_{mi}=0.50 mS/μm) on GaAs substrates and InSb QWFETs (L=85 nm, g_{mi}=0.71 mS/ μm) on Si, our InAsSb XOI FETs show a peak g_{mi} of ~0.56 mS/μm for L~500 nm (Fig. 2.4(c)) while eliminating the complexity from growing thick buffer and δ doping layers [9, 10]. Moreover, it has higher I_{ON}/I_{OFF} at room temperature.

2.6 Interface Trap Density Extraction

Fig. 2.4(d) shows the temperature dependent transfer characteristics. The interface trap density (D_{it}) was extracted from $D_{it} = C_{it}/q^2$, with C_{it} from,

$$\frac{dSS}{dT} = \frac{2.3k}{q}\left(1+\frac{C_{it}}{C_{ox1}}+\frac{C_{InAsSb}}{C_{ox1}}-\frac{\frac{C_{InAsSb}^2}{C_{ox1}C_{ox2}}}{1+\frac{C_{it}}{C_{ox2}}+\frac{C_{InAsSb}}{C_{ox2}}}\right)$$

With ε_{ox1}= 16, t_{ox1}= 10 nm, ε_{ox2}= 3.9, t_{ox2}= 1200 nm, ε_{InAsSb}= 15.7, and t_{InAsSb}= 7 nm, D_{it} is determined to be ~1×10^{13} $cm^{-2}\,eV^{-1}$, which is slightly higher than that of InAs XOI FETs' (~3×10^{12} $cm^{-2}\,eV^{-1}$) [16]. Note that this D_{it} value presents only a rough estimate of the order of magnitude for the average trap density within the bandgap. The traps close or beyond the conduction band edge are not extracted using this analysis technique, but they can also alter the charge carrier density and transport properties. Detailed capacitance-voltage characterization in the future is needed to better understand and optimize the surface/interface properties.

2.7 Conclusions

In conclusion, high electron mobility $InAs_{0.7}Sb_{0.3}$ transistors have been fabricated on Si substrates using the XOI configuration. The devices exhibit excellent electrical properties, while future work on improving the InAsSb/high-K dielectric interface needs to be done. In the future, even higher Sb content and thinner body InAsSb XOI n-FETs, together with InGaSb XOI p-FETs, are promising to be integrated for high speed and low power complementary MOSFET circuits.

References

1. R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications," *IEEE Trans. Nanotech.* Vol. 4, 2005, pp. 153-158.

2. D. A. Antoniadis, and A. Khakifirooz, "MOSFET Performance Scaling: Limitations and Future Options," *IEEE IEDM Tech. Dig.*, 2008, pp. 1-4.

3. D.-H. Kim, and J. A. del Alamo, "Scalability of Sub-100 nm InAs HEMTs on InP Substrate for Future Logic Applications," *IEEE Trans. Electron Devices* Vol. 57, 2010, pp. 1504-1511.

4. Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," *IEEE IEDM Tech. Dig.*, 2007, pp. 637-640.

5. B. R. Bennett, R. Magno, J. B. Boos, W. Kruppa, and M. G. Ancona, "Antimonide-based compound semiconductors for electronic devices: A review," *Solid State Electron.* Vol. 49, 2005, pp. 1875-1884.

6. A. Ali, H. Madan, R. Misra, A. Agrawal, P. Schiffer, J. B. Boos, B. R. Bennett, and S. Datta, "Experimental Determination of Quantum and Centroid Capacitance in Arsenide–Antimonide Quantum-Well MOSFETs Incorporating Nonparabolicity Effect," *IEEE Trans. Electron Devices* Vol. 58, 2011, pp. 1397-1403.

7. B.-R. Wu, C. Liao, and K. Y. Cheng, "High quality InAsSb grown on InP substrates using AlSb/AlAsSb buffer layers," *Appl. Phys. Lett.* Vol. 92, 2008, pp. 062111-1–062111-3.

8. S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding and R. Chau, "85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications," *IEEE IEDM Tech. Dig.*, 2005, Vol. 763.

9. A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ramirez, P. Schiffer, T. N. Jackson, S. E. Mohney, J. B. Boos, B. R. Bennett, I. Geppert, M. Eizenberg and S. Datta, "Advanced Composite High-κ Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors," *IEEE IEDM Tech. Dig.*, 2010, pp.134-137.

10. T. Ashley, L. Buckle, S. Datta, M.T. Emeny, D.G. Hayes, K.P. Hilton, R. Jefferies, T. Martin, T.J. Phillips, D.J. Wallis, P.J. Wilding and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," *Elec. Lett.* Vol. 43, 2007.

11. H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature* Vol. 468, 2010, pp. 286-289.

12. Y.-k. Choi, K. Asano, N. Lindert, V. Subramanian, T.-j. King, J. Bokor and C. Hu, "Ultra-thin Body SO1 MOSFET for Deep-sub-tenth Micron Era," *IEEE IEDM Tech. Dig.*, 1999, pp. 919-921.

13. H. T. Grahn, *Introduction to Semiconductor Physics*, Singapore: World Scientific, 1999, p. 121.

14. K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C.-H. Liu, Y.-L. Chueh, E. Plis, S. Krishna, H. A. Bechtel, J. Guo, A. Javey. "Quantum Confinement Effects in Nanoscale-Thickness InAs Membranes", Nano Letters, 2011, ASAP, doi: 10.1021/nl2030322.

15. D. Chattopadhyay, S. K. Sutradhar and B. R. Nag, "Electron transport in direct-gap III-V ternary alloys," *J. Phys. C: Solid State Phys*., Vol. 14, 1981, pp. 891-908.

16. K. Takei, S. Chuang, H. Fang, R. Kapadia, C.-H. Liu, J. Nah, H. S. Kim, E. Plis, S Krishna, Y.-L. Chueh, and A. Javey, "Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Appl. Phys. Lett.* Vol. 99, 2011, pp. 103507-1–1035073.

Chapter 3

[3]InAs Nanowire Ballistic Study

3.1 Introduction

The scaling of electronic transistors for performance and density enhancement has been a major driving force behind the advancement of modern integrated circuit technology. As scaling becomes increasingly difficult, the electronics industry is moving towards unconventional materials and non-planar structures. Both of these aspects are inherent in InAs nanowire (NW) transistors, making them a promising platform for future high performance transistors [1-5]. One critical goal in scaling is to obtain ballistic devices [6-9], where carriers are transported through the channel without undergoing scattering events. Ballistic devices are highly desirable as they offer minimal resistive voltage drop in the channel. Hence, ballistic operation presents the upper limit for the ON-state conductance of a transistor. InAs can potentially be used to fabricate ballistic transistors given its relatively long bulk electron mean free path (λ) [10]. In this regard, detailed characterization of λ of InAs NWs is required [11, 12], especially as a function of subband population.

Recently, we reported the direct observation of one-dimensional (1-D) subbands in the electrical transfer characteristics of long-channel (L~8 μm) InAs NW field-effect transistors (FETs) [13]. Given the large Bohr radius of InAs (~34 nm) [14], strong quantization with prominent subband spacing is readily observed for sub-50

[3] Reprinted with permission from Steven Chuang et al., Nano Letters, 13, 555−558, 2013. Copyright 2013 American Chemical Society.

nm diameter NWs. The devices were passivated by a ZrO_2 dielectric which resulted in the lowering of surface disorder, and thereby allowing for the direct mapping of the transport in individual 1-D subbands. Given that for a ballistic NW, each 1-D subband contributes a quantum unit of conductance of $G_o=2e^2/h$ [15], the transmission probability and thereby λ can be directly assessed from electrical measurements. Here, by fabricating InAs NW FETs with different channel lengths down to ~60 nm, we experimentally extract λ~150 nm for electron transport in the 1st and 2nd subbands. The experimental results are consistent with the theoretical calculations of the momentum relaxation times associated with surface roughness (SR) scattering mechanisms. Given the relatively long mean free path in InAs NWs, ultrashort channel FETs with L~60 nm are shown to exhibit a conductance of ~$0.8G_o$ for the 1st subband, suggesting electron transport at ~80% of the ballistic limit, independent of temperature.

3.2 Nanowire FET Fabrication

InAs NWs used in this study were grown by a vapor transport technique described previously [16]. The NWs were suspended in anhydrous ethanol and drop casted over a Si/SiO_2 substrate. Multiple Ni (~40 nm thick) source/drain (S/D) contact electrodes of varying spacing (L~510 nm to 60 nm) were defined on each NW by electron-beam lithography, metallization and lift-off. The sample was then annealed at 185 ºC under vacuum in order to reduce the contact resistance at the Ni/InAs interface. Previous studies have shown that annealed Ni contacts to InAs NWs exhibit ohmic properties without parasitic resistances [17]. A 15nm ZrO_2 gate dielectric was deposited at 130 ºC via atomic layer deposition (ALD), followed by a 130 ºC forming gas anneal for 30 minutes to improve the dielectric/InAs interface quality [18]. Finally, a single Ni/Au (20/30 nm) top-gate electrode overlapping the S/D contacts was defined via photolithography. Figure 3.1 shows a cross-sectional schematic, optical image and scanning electron micrograph (SEM) of the fabricated devices.

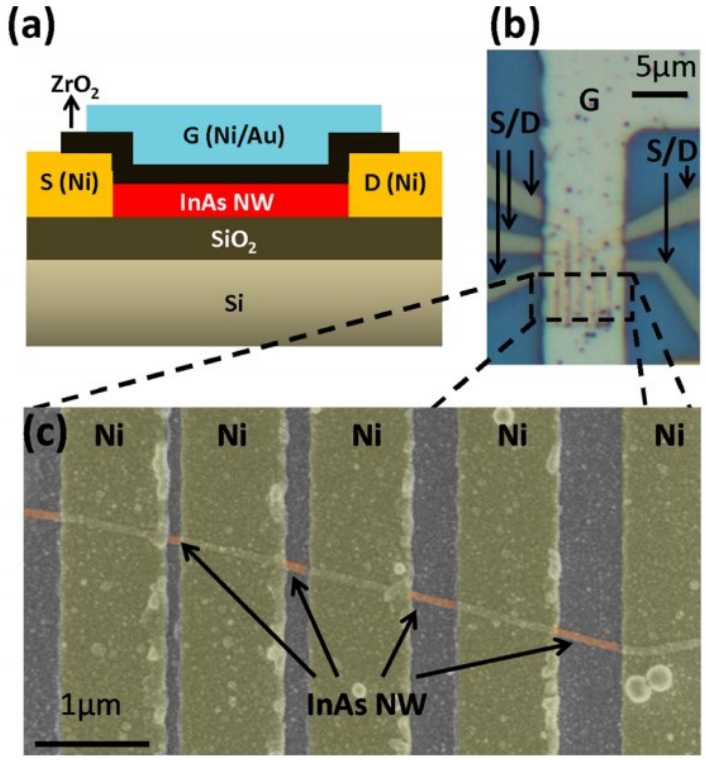

Figure 3.1. (a) Cross-sectional schematic of a top-gated InAs NW device explored in this study. (b) Optical image and (c) false color SEM image of the fabricated devices, featuring one nanowire contacted by multiple source/drain fingers for length dependent measurements.

3.3 Low Temperature Electrical Characteristics

Low-field transfer characteristics of InAs NW FETs with L~60, 150, 340, and 510 nm at 120 K are shown in Figure 3.2. All devices are fabricated on a single NW. The diameter of the NW was measured by atomic force microscopy (AFM) as ~31 nm, which corresponds to an actual InAs diameter of ~26 nm considering the ~2.5 nm thick native oxide previously observed under TEM for NWs grown by the same method [19]. Conductance was obtained by dividing the measured drain current by the applied drain voltage (V_{DS}=10 mV) and plotted in units of G_o. Distinct step-like features are observed in each conductance plot, which are due to quantization of the channel density of states, with each step attributed to the population of a single 1-D subband. Importantly, the conductance value for each subband can be easily extracted from the plateaus of the G-V_{GS} plots. Note that as we previously reported, the height of the 2nd subband plateau is approximately

twice that of the 1st subband for long channel devices where the transport is largely diffusive [13], as evident in the L~510 nm device (Fig. 3.2). This phenomenon is due to the two-fold degeneracy of the 2nd subband arising from the structural symmetry of cylindrical NWs. The conductance ratio of the 2nd to 1st plateaus decreases as the channel length is reduced. This observation can be attributed to the difference in parasitic contact resistance R_c of the two subbands.

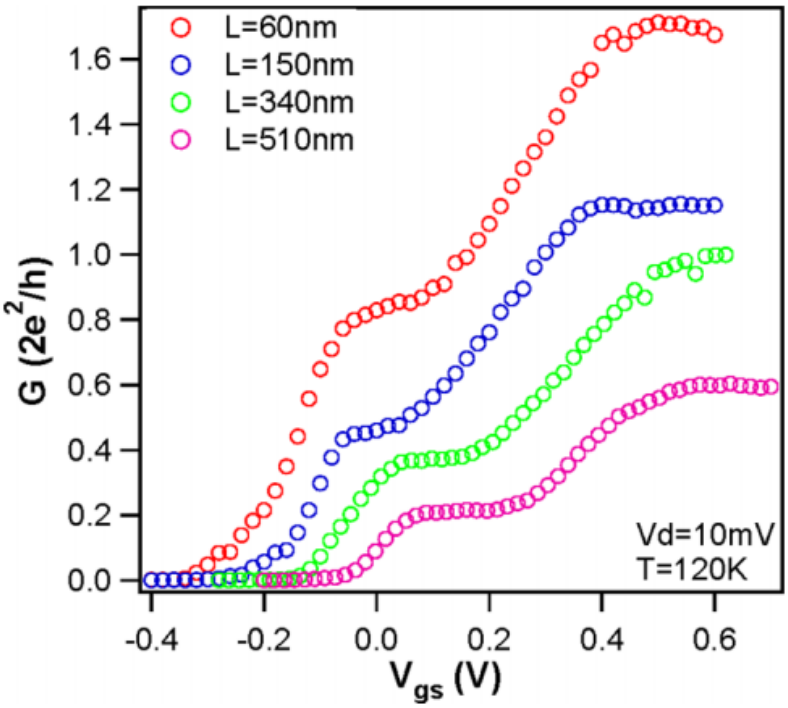

Figure 3.2. (a) G-V_{GS} plots for 26 nm diameter InAs NW FETs with varying channel lengths. The plots have been shifted in V_{GS} for presentation clarity.

3.4 Contact Resistance and Mean Free Path Extraction

The total resistance of each subband plateau can be analytically expressed as [20]:

$$R = R_c + R_q(1+L/\lambda)$$

where R_q is the quantum resistance, which is $1/G_o$ for the 1st subband and $1/2G_o$ for the 2nd subband due to degeneracy. By plotting R vs L for each subband plateau, λ can be extracted from the inverse of the slope, and R_c can be extracted from the y-intercept (Fig. 3.3a-b, inset). The extracted R_c values are ~0 and $0.3/G_o$ for the 1st

and 2nd subbands, respectively. The absence of contact resistance for the 1st subband is expected given the negative Schottky barrier heights previously reported for bulk InAs/metal interfaces [21]. The presence of a contact resistance for the 2nd subband is indicative of a small Schottky barrier height to the higher energy subbands. As noted later in the manuscript, the device resistance is independent of temperature, suggesting that the Schottky barrier height and width must be small and thin, respectively, with electron tunneling at the metal interface being the primary source of carrier injection. Given that the barrier heights to the first two subbands are either negative or very small [13], the V_{GS} dependence of R_c is assumed to be negligible.

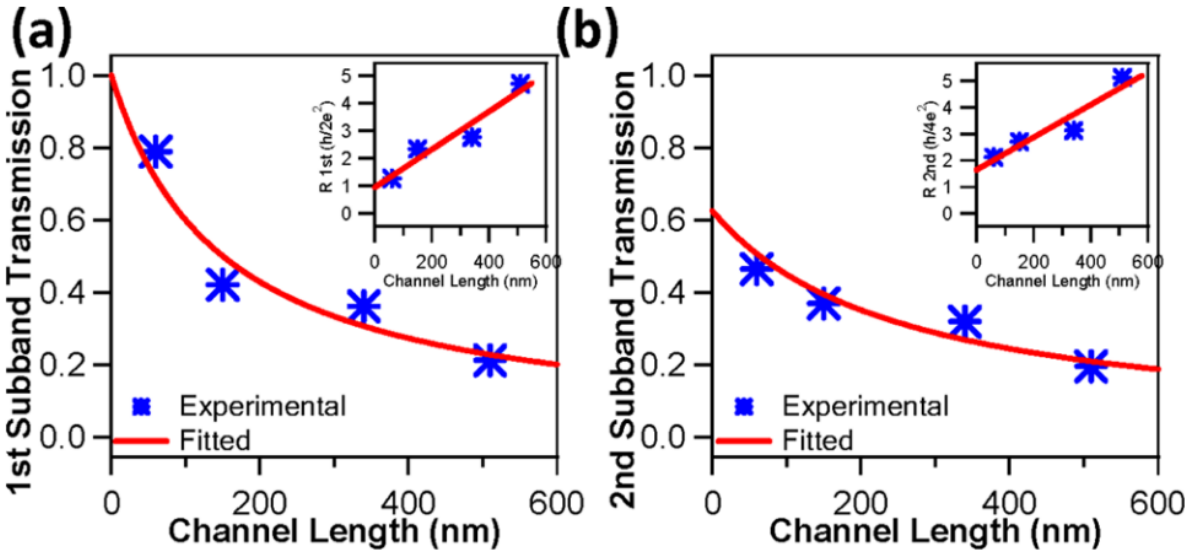

Figure 3.3. Experimental and fitted transmission probability vs channel length plots for the (a) 1st and (b) 2nd subbands. Resistance vs length plots are shown in the insets.

From the inverse slope of R vs L (Fig. 3.3a-b inset), the electron mean free paths for the 1st and 2nd subbands are extracted as $\lambda_{n=1}$ ~150±40 nm and $\lambda_{n=2}$ ~160±50 nm, respectively, which is in well agreement with previously extracted values using other techniques [11, 12]. Plots of G vs L for the experimental and fitted λ and R_c values are also shown in Fig. 3.3a-b, with each being in good agreement with one another. In addition, by normalizing the observed G of each subband by G_o, we can obtain the transmission coefficient T of carriers traversing our devices, which gauges how close the subband conductance of our devices is to the theoretical limit of scaling. The shortest device (L~60 nm) in our study exhibits a T of ~80%, which

is the highest value reported for inorganic semiconductors to date. The results highlight the near ballistic transport in InAs NWs when L< λ.

3.5 Temperature Dependent Electrical Characteristics

Next, we focus on the temperature-dependent transport of InAs NWs. Figure 3.4 shows the transfer characteristics for L~60 nm (Fig. 3.4a) and L~510 nm (Fig. 3.4b) NW devices as a function of temperature (120-300K).

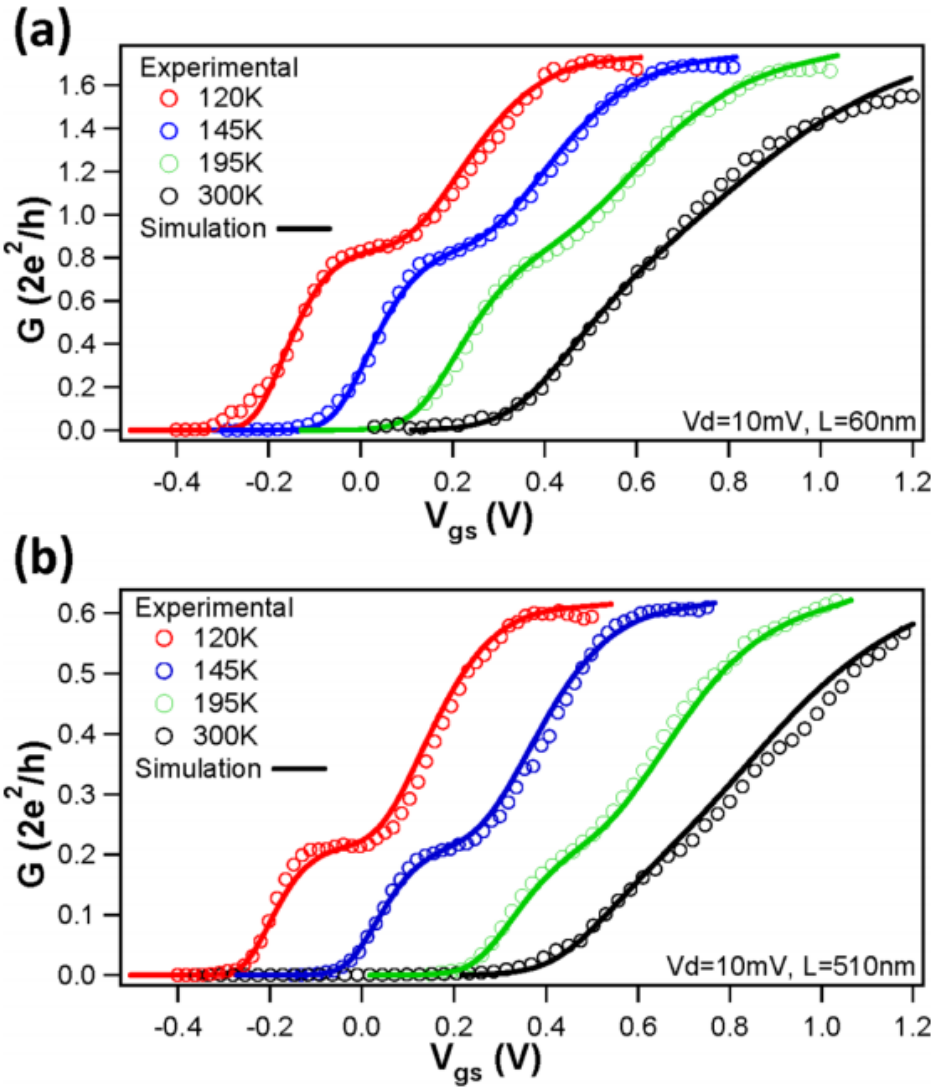

Figure 3.4. Temperature dependent G-V_{GS} plots for (a) L=60nm and (b) L=510 nm InAs nanowire devices. Both experiment (open circles) and modeling (solid lines) data are presented. The plots have been shifted in V_{GS} for presentation clarity.

For both channel lengths, increasing the temperature only causes the broadening of the subbands population (i.e., conductance steps), without a change in the overall conductance of the device.

Modeling was performed to shed light on the temperature dependency of the transfer characteristics [13]. Briefly, the subband density vs energy for a NW was obtained by analytically solving Schrodinger's equation for the device. The energy axis was converted to gate voltage by the relationship: $V_{GS}=E/e-(Q/C_{ins})$, where E is electron energy, Q is the total charge in the NW, and C_{ins} is the gate capacitance. The gate capacitance was obtained by a Poisson simulation as $2.57\text{x}10^{-10}$ F/m [22]. The following term, $\Delta V_g = \frac{\Delta Q_{it}}{C_{ins}}$, was added to the previous calculations to account for a density of interface traps (D_{it}) of 3×10^{12} states/cm^2 eV as previously reported for InAs/ZrO_2 interfaces [23], with $\Delta Q_{it}=\Delta E\times D_{it}$. A gate coupling factor of 0.8 was applied to C_{ins} to fit the data for the L=60nm device, justified by the reduction of gate coupling in short channel devices. Each step in the subband density was multiplied by its corresponding experimental transmission probability to convert the y-axis to conductance. The resulting curve was then broadened with the Fermi function. The curves from this model agree well with the experimental results, indicating that the transfer characteristics of these devices can be described by focusing on the available states for conduction, as opposed to the well-known diffusive transport MOSFET equations.

Importantly, note that the transmission probability and gate coupling fitting parameters were kept constant over all temperatures. It can easily be seen that the experimental current levels do not drop below the model, indicating that transmission through the NWs does not degrade with temperature. Two deductions can be made from this temperature dependency observation. First, the λ extracted from the transmission probability values does not depend on temperature, implying that the dominant scattering mechanism is temperature independent SR scattering. A similar conclusion was previously made from the mobility analysis of long-channel InAs NW FETs [19]. Second, the transmission values extracted at 120K can be extended to room temperature, implying that the L~60 nm device is ~80% ballistic at room temperature.

3.6 Modeling InAs Nanowire Surface Roughness Scattering

In order to better understand the observed transport characteristics, λ values due to surface roughness (SR) scattering were assessed theoretically by a method that combines the Fermi's golden rule and a numerical Schrödinger-Poisson simulation to determine the SR scattering potential. SR scattering was assumed to be the dominant scattering mechanism according to previous InAs NW and thin film mobility studies [14, 19] and the lack of temperature dependence in transmission probability (shown in chapter 3.5). The SR is described statistically by an exponentially decaying autocorrelation function with the parameters Δ_m (the RMS SR magnitude), and L_c (the correlation length along the axis direction). Only SR in the axial direction of the NW is considered. From the calculated momentum relaxation time τ_{sr}, λ is calculated as $\lambda=v_F\times\tau_{sr}$, where v_F is the initial Fermi velocity of the carrier. The details of this simulation approach are described below. The results indicate that the SR parameters of $\Delta_m \approx 0.3$ nm, and $L_c \approx 6$nm, result in λ~ 175 nm and 138 nm for the 1st and 2nd subband at ~25meV above the subband edge, in which 25meV is about 1/2 of the spacing between the 1st and 2nd subbands. These theoretical values are consistent with the extracted experimental values. The low density-of-states (DOS) of scattering final states arising from the quasi-1D structure and low effective mass of InAs contributes to the long λ. Furthermore, the calculated λ of the 1st subband is slightly larger than that of the 2nd subband due to the following reason. The scattering potential matrix element square of the 2nd intrasubband scattering is about a factor of ~1.27 larger than that of the 1st subband, as calculated by Schrödinger-Poisson simulations, because the charge centroid of the 2nd subband is closer to the surface. The experimentally extracted values for the 1st and 2nd subbands, however, are nearly identical most likely due to the uncertainty in the experimental values.

The theoretical model of SR scattering is based on the Born approximation and self-consistent solutions of the Schrodinger and Poisson equations [24]. By describing the SR statistically using an exponentially decaying autocorrelation function, the rate due to SR scattering is expressed as [25, 26],

$$\frac{1}{\tau_{SR}(E)}=\frac{2\pi e^2 M_S D_f(E)}{\hbar}\sqrt{2}\Delta_m^2 L_c\left(1+\frac{L_c^2 q^2}{2}\right)^{-1}(1-\cos\phi)$$

where $D_f(E)$ is the density of states for the scattering final states, L_c is the correlation length along axial direction, Δ_m is the RMS SR magnitude, q is the

axial wavevector along the z-direction, and $\phi = \pi$ for backscattering in 1D transport. Only SR in the axial direction of the NW is considered and the SR in the azimuthal direction is neglected [26]. The validity of this assumption will be discussed later. The expression is different from the equation of the SR scattering rate in planar MOSFETs because the autocorrelation is related to its spectral function through a one-dimensional rather than two-dimensional Fourier transform for a NW with SR only along the axial direction.

The matrix element square of perturbing potential M_s is defined as

$$M_{snn} = \left| \int \Psi_n \left[\frac{\Delta V_m}{\Delta} \right] \Psi_n dr \right|^2$$

where Ψ_n is the envelope function for n^{th} subband and ΔV_m is the SR perturbing potential which is calculated as the electrostatic potential variation by perturbing the NW radius by Δ using a numerical self-consistent Schrödinger-Poisson simulation of the NW cross section [24]. From the momentum relaxation scattering rate, the mean free path is obtained by using $\lambda(E) = v_F(E)\tau_{SR}(E)$, where v_F is the initial Fermi velocity of the carrier.

Using numerical self-consistent Schrodinger-Poisson calculations [13], the matrix element squares are calculated as [24] $M_{S11} \approx (17\ \mathrm{mV/nm})^2$, and $M_{S22}/M_{S11} \approx 1.27$. λ is calculated for a NW radius $R_{NW} \approx 13$nm at the energies of $E\text{-}E_{C1} \approx 25$meV and $E\text{-}E_{C2} \approx 25$meV for the 1st and 2nd subbands, in which E_{ci} is the ith subband edge. The values of $\lambda_{n=1} \sim 175$nm and $\lambda_{n=2} \sim 138$nm are obtained by using $\Delta_m \approx 0.3$nm and $L_c \approx 6$ nm as fitting parameters.

3.7 Conclusions

In summary, the mean free path for carrier scattering in InAs NW FETs is directly extracted for electron transport in the 1st and 2nd subbands by examining resistance as a function of channel length. Due to the observation of discrete subband transport in the transfer characteristics, direct analysis of the ballistic transport can be deduced, with L~60 nm devices exhibiting near-ballistic transport (~80% ballistic) independent of temperature. This represents one of the most ballistic device systems reported to-date at room temperature, owing to the relatively long mean free path of ~150 nm for the 1st subband transport. Surface roughness scattering is shown to be the dominant scattering mechanism. In the future, further improvement of the surface properties and reducing the SR could potentially enhance the mean free path of the experimental NW FETs. Most importantly, this work provides a platform for the study of ultra-scaled, non-planar devices based on III-V material systems where quantization plays a major role in determining the electrical properties, given their relatively large Bohr radius.

References

1. Dayeh, S. A.; Aplin, D. P. R.; Zhou, X.; Yu, P. K. L.; Yu, E. T.; Wang , D. High Electron Mobility InAs Nanowire Field-Effect Transistors. *Small* **2007**, 3, 326-332.

2. Alam, K. Transport and Performance of a Gate All Around InAs Nanowire Transistor. *Semidond. Sci. Technol.* **2009**, 24, 085003

3. Thelander ,C.; Froberg, L. E.; Rehnstedt, C.; Samuelson, L.; Wernersson, L. E. Vertical Enhancement-Mode InAs Nanowire Field Effect Transistor with 50-nm Wrap Gate. *IEEE Electron Dev. Lett.* **2008**, 29 206–208.

4. Thelander, C.; Rehnstedt, C.; Froberg, L. E.; Lind, E.; Martensson, T.; Caroff, P.; Lowgren, T.; Ohlsson, B. J.; Samuelson, L.; Wernersson, L. E. Development of a Vertical Wrap-Gated InAs FET. *IEEE Trans. Electron Devices* **2008**, 55, 3030–3036.

5. Bessire, C. D.; Björk, M. T.; Schmid, H.; Schenk, A.; Reuter, K. B.; Riel, H. Trap-Assisted Tunneling in Si-InAs Nanowire Heterojunction Tunnel Diodes. *Nano. Lett.* **2011**, 11, 4159-4199.

6. Lu, W.; Xiang, J.; Timko, B. P.; Wu, Y.; Lieber, C. M. One-dimensional hole gas in germanium/silicon nanowire heterostructures. *PNAS* **2005**, 102, 10046.

7. Biercuk, M. J.; Mason, N.; Martin, J.; Yacoby, A.; Marcus, C. M. Anomalous Conductance Quantization in Carbon Nanotubes. *Phys. Rev. Lett.* **2005** 95, 069902.

8. Xiang, J.; Vidan, A.; Tinkham, M.; Westervelt, R. M.; Lieber, C. M. Ge/Si nanowire mesoscopic Josephson junctions. *Nature Nanotech.* **2006** 1, 208.

9. Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. Ballistic Carbon Nanotube Transistors. *Nature* **2003**, 424, 654-657.

10. Inoue, K.; Takayanagi, H. Local Tunneling Spectroscopy of a Nb/InAs/Nb Superconducting Proximity System with a Scanning Tunneling Microscope. *Phys. Rev. B* **1991**, 43 6214-6215.

11. Zhou, X.; Dayeh, S. A.; Aplin, D.; Wang, D.; Yu, E. T. Scanned Electrical Probe Characterization of Carrier Transport Behavior in InAs Nanowires. *J. Vac. Sci. Technol. B* **2006,** 24, 2036.

12. Zhou, X.; Dayeh, S. A.; Aplin, D.; Wang, D.; Yu, E. T. Direct Observation of Ballistic and Drift Carrier Transport Regimes in InAs Nanowires. *Appl. Phys. Lett.* **2006,** 89, 053113.

13. Ford, A. C.; Kumar, S. B.; Kapadia, R.; Guo, J.; Javey, A. Observation of Degenerate One-Dimensional Sub-Bands in Cylindrical InAs Nanowires. *Nano. Lett.* **2012**, 12, 1340-1343.

14. Takei, K.; Fang, H.; Kumar, S. B.; Kapadia, R.; Gao, Q.; Madsen, M.; Kim, H. S.; Liu, C.-H.; Chueh, Y.-L.; Plis, etc. Quantum Confinement Effects in Nanoscale-Thickness InAs Membranes. *Nano. Lett.* **2011**, 11, 5008–5012.

15. Datta, S. *Quantum Transport: Atom to Transistor*; Cambridge University Press: New York, **2005**.

16. Ford, A. C.; Ho, J. C.; Fan, Z.; Ergen, O.; Altoe, V.; Aloni, S.; Razavi, H.; Javey, A. Synthesis, Contact Printing, and Device Characterization of Ni-Catalyzed, Crystalline InAs Nanowires. *Nano. Res.* **2008**, 1, 32-39.

17. Chueh, Y.-L.; Ford, A. C.; Ho, J. C.; Jacobson, Z. A.; Fan, Z.; Chen, C.-Y.; Chou, L.-J.; Javey, A. Formation and Characterization of Ni_xInAs/InAs Nanowire Heterostructures by Solid Source Reaction. *Nano. Lett.* **2008**, 8, 4528-4533.

18. Takei, K.; Chuang, S.; Fang, H.; Kapadia, R.; Liu, C.-H.; Nah, J.; Kim, H. S.; Plis, E.; Krishna, S.; Chueh, Y.-L *et al*. Benchmarking the Performance of Ultrathin Body InAs-On-Insulator Transistors as a Function of Body Thickness. *Appl. Phys. Lett.* **2011**, 99, 103507.

19. Ford, A. C.; Ho, J. C.; Chueh, Y.-L.; Tseng, Y.-C.; Fan, Z.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano. Lett.* **2009**, 9, 360-365.

20. Datta, S. *Electronic Transport in Mesoscopic systems*; Cambridge University Press: New York, **1997**.

21. Wieder, H. H. Surface and Interface Barriers of $In_xGa_{1-x}As$ Binary and Ternary Alloys. *J. Vac. Sci. Technol. B* **2003**, 21, 1915-1919.

22. Nextnano^3. Available on-line: http://www.nextnano.de.

23. Ko, H.; Takei, K.; Kapadia, R.; Chuang, S.; Fang, H.; Leu, P. W.; Ganapathi, K.; Plis, E.; Kim, H. S.; Chen, S.-Y. *et al.* Ultrathin Compound Semiconductor on Insulator Layers for High Performance Nanoscale Transistors. *Nature* **2010**, 468, 286-289.

24. Gámiz, F.; Roldán, J. B.; Cartujo-Cassinello, P.; López-Villanueva, J. A.; Cartujo, P. J. Role of Surface-Roughness Scattering in Double Gate Silicon-On-Insulator Inversion layers. *Appl. Phys.* **2001**, 89, 1764-1770.

25. Goodnick, S. M.; Ferry, D. K.; Wilmsen, C. W.; Liliental, Z.; Fathy, D.; Krivanek, O. L. Surface Roughness at the Si(100)-SiO_2 Interface. *Phys. Rev. B* **1985**, 32, 8171-8186.

26. Lenzi, M.; Gnudi, A; Reggiani, S.; Gnani, E.; Rudan, M.; Baccarani, G. Semiclassical Transport in Silicon Nanowire FETs Including Surface Roughness. Journal of Computational Electronics, **2008**, 7, 355-358.

Chapter 4

[4]MoO_x Contacts to Transition Metal Dichalcogenides

4.1 Introduction

Transition metal dichalcogenides (TMDCs) offer ultra-thin, uniform channel thicknesses for unparalleled gate control, and are a strong candidate for future electronics [1] [2] [3] [4] [5]. In order to apply TMDCs to low-power, high-performance complementary logic applications, both *n*- and *p*-type field effect transistors (NFETs and PFETs) must be developed. The polarity of a FET is determined by the type of charge carriers that can be injected from the source contact into the semiconductor channel. In a conventional metal-oxide-semiconductor FET (MOSFET), this is achieved by heavily doping the source/drain contacts to either *p*+ or *n*+ for *p* and *n*-type transistors respectively. Similarly, in a Schottky MOSFET, where metal contacts are directly fabricated on the semiconductor, the device polarity is determined by the Schottky barrier (SB) heights for electrons and holes at the source contact. A small SB height to the conduction or valence band leads to *n* or *p*-type FETs, respectively. SB heights, in principle, can be controlled by the work function potential of metal contacts. To date, most reported TMDC FETs have been based on the Schottky device architecture given its ease of fabrication. While TMDC NFETs have been

[4] Reprinted with permission from Steven Chuang et al., Nano Letters, 14 (3), 1337–1342, 2014. Copyright 2014 American Chemical Society.

relatively well studied [3] [4] [5] [6], there has been difficulty fabricating high-performance TMDC PFETs, largely limited by hole injection at the source/drain (S/D) contacts due to large SB heights to the valence band. Traditionally, the high work function metal palladium (Pd) has been used as the most popular contact material to the valence band of various nanostructures, including nanotubes, graphene, and organics [7] [8] [9] [10]. However Pd alone has proven insufficient as a hole contact for TMDC devices. With a workfunction of 5.1 eV [11], the Fermi level of ultra-clean Pd lies slightly above the valence band maximum of MoS_2 [12] [13]. However, most previously reported Pd-contacted MoS_2 devices exhibit *n*-type behavior with high contact resistance instead of *p*-type behavior, which is commonly ascribed to Fermi-level pinning at the MoS_2 contact interface [6] [14]. A recent study has shown that limited hole injection can be observed in Pd-contacted MoS_2 devices, but only in the limit of large gate fields when the SBs are sufficient thinned by the electrostatic fields [15]. On the other hand Pd-contacted WSe_2 PFETs show high contact resistances and require surface charge transfer doping to thin the SBs and allow tunneling of holes at the contacts [2].

4.2 MoO_x Material Characterization

Here we explore substoichiometric molybdenum trioxide (MoO_x, $x<3$) as a promising material for hole injection into TMDCs without doping the semiconductor body. MoO_x exhibits a high work function potential of up to ~6.6 eV (see Fig. 4.1a) [16] exceeding those of elemental metals [11]. While MoO_x has been previously used as hole contacts in organic electronics [17] [18], its application to inorganic semiconductors was extended only recently [16] [19]. Here we demonstrate a series of TMDC devices with MoO_x contacts that highlight unambiguously the advantages of MoO_x hole contacts over conventionally explored elemental metal contacts. MoS_2 FETs with MoO_x contacts present *p*-type behavior despite the notorious Fermi level pinning to the conduction band previously observed [6]. MoS_2 Schottky diodes with asymmetric MoO_x and Ni contacts clearly display rectifying behavior. Finally, WSe_2 PFETs with MoO_x contacts show an order of magnitude increase in on-current when compared to Pd-contacted WSe_2 PFETs.

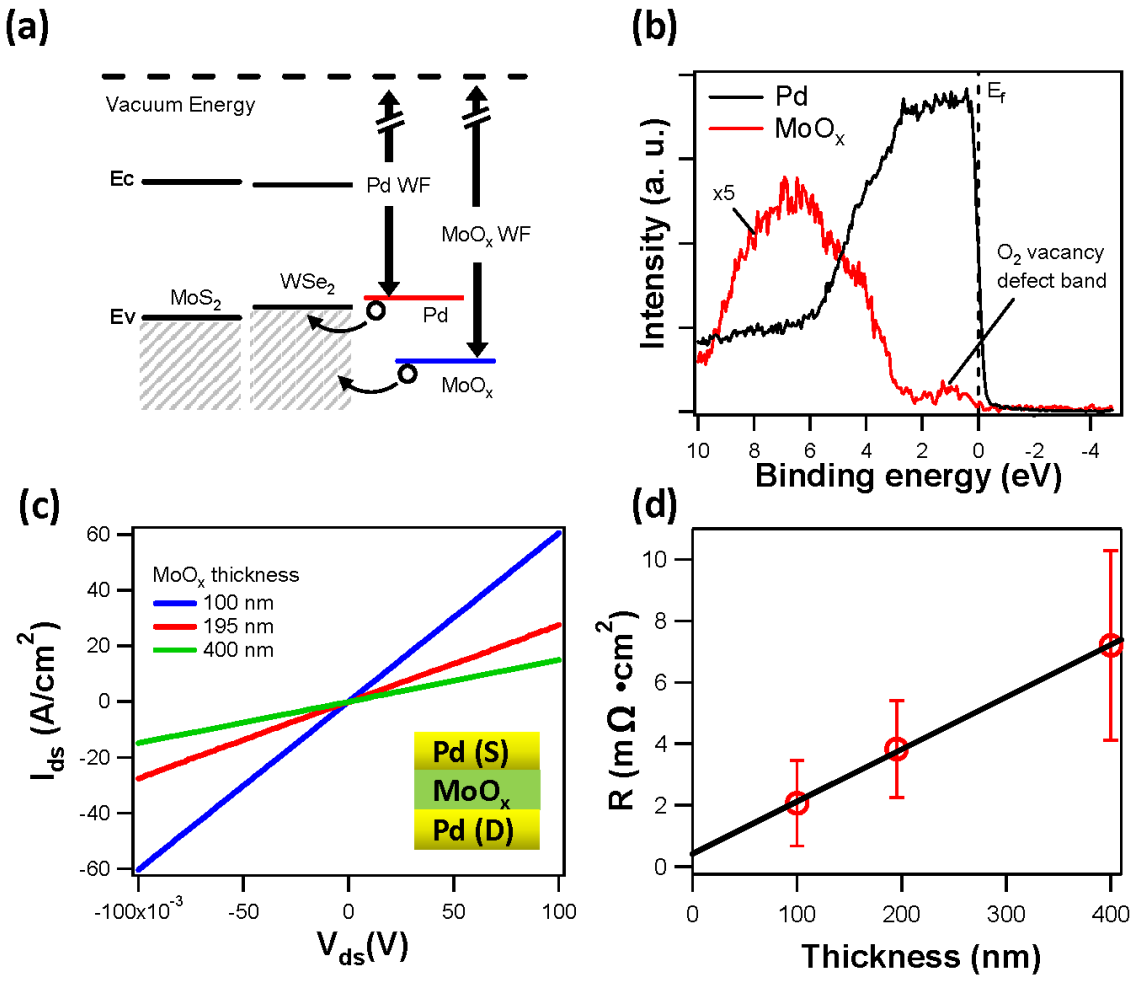

Figure 4.1. (a) Valence and conduction band positions with respect to vacuum level for MoS_2, WSe_2, Pd and MoO_x. (b) Valence band photoelectron spectra for MoO_x and Pd films evaporated in ultra-high vacuum conditions using monochromatized Al K_α radiation. (c) Current-voltage characteristics across $Pd/MoO_x/Pd$ stacks indicating good Ohmic contact with a schematic of the test structure in the inset. (d) Resistance of $Pd/MoO_x/Pd$ stacks as a function of MoO_x thickness.

Fig. 4.1b compares monochromatic x-ray photoelectron spectra (XPS) of the valence band region of MoO_x and Pd films [20]. While Pd shows a strong photoelectron signal below the Fermi energy (E_F) with a clear metallic Fermi-Dirac step centered at E_F, the valence band of thermally evaporated MoO_x possesses a weak characteristic defect band in the band gap derived from oxygen vacancies,

whose tail reaches all the way up to E_F. Consequently MoO_x can be classified as a semiconducting oxide with a metallic defect band. Its workfunction can exceed 6.6 eV, but is known to strongly depend on carbon contamination [16]. For practical applications, MoO_x can thus be considered to act as a high workfunction metal with a low density of states at the Fermi level. Consequently most metals should form ohmic contacts with MoO_x.

In order to confirm ohmic contact between MoO_x and Pd, the current-voltage characteristics across Pd/MoO_x/Pd stacks were measured. Stacks of 20nm Pd/ MoO_x/ 40nm Pd were fabricated by photolithography, evaporation and lift-off. The MoO_x thickness was varied from 100 nm to 400 nm. Fig. 4.1c shows the clearly linear current-voltage characteristics of the stacks which confirm ohmic behavior between MoO_x and Pd. Fig. 4.1d shows the total resistance of these devices as a function of MoO_x thickness. The resistance of a single contact is extracted from half the y-intercept of the linear fit as ~200 $\mu\Omega\bullet cm^2$. The resistivity extracted from the slope of the linear fit of the plot is ~200 $\Omega\bullet$cm. Although this resistivity is high, keeping the MoO_x layer thin enough (i.e., sub-50 nm) guarantees efficient carrier transport.

4.3 MoS_2 PFETs with MoO_x Contacts

4.3.1 Fabrication Process

We now turn to the fabrication of MoS_2 PFETs with MoO_x contacts. MoS_2 flakes were first exfoliated mechanically onto a 260 nm SiO_2/Si substrate. A 1 hour acetone bath was used to clean any organic residues from the chip after exfoliation. Symmetrical 30 nm MoO_x/ 30 nm Pd contacts were defined on the MoS_2 flakes via photolithography, evaporation and lift-off. The channel length between the contacts is ~7 μm. In order to minimize workfunction lowering due to carbon contamination of MoO_x, several precautions were taken. Thermal evaporation of MoO_x was carried out after ~12 hours of pumping at a base pressure of $\sim 8\times10^{-7}$ Torr at a rate of 0.5 Å/s. MoO_3 powder (99.9995% purity, Alfa Aesar) was used as the MoO_x evaporation source throughout this study. Electron-beam evaporation of Pd was performed right after MoO_x deposition without breaking vacuum.

4.3.2 I_{ds} vs V_{gs} Characteristics

A schematic and optical microscope image of a representative MoS_2 PFET with MoO_x contacts are shown in figure 4.2a. Corresponding I_{ds} vs V_{gs} characteristics are shown in figure 4.2b. All TMDC devices in this study were measured in vacuum in order to isolate effects from exposure to ambient, such as the adsorption of oxygen and water [4]. The thickness of the MoS_2 flake was measured as 40 nm with atomic force microscopy (AFM). Clear *p*-type characteristics with I_{on}/I_{off}~10^4 are obtained, indicating hole contact to the valence band.

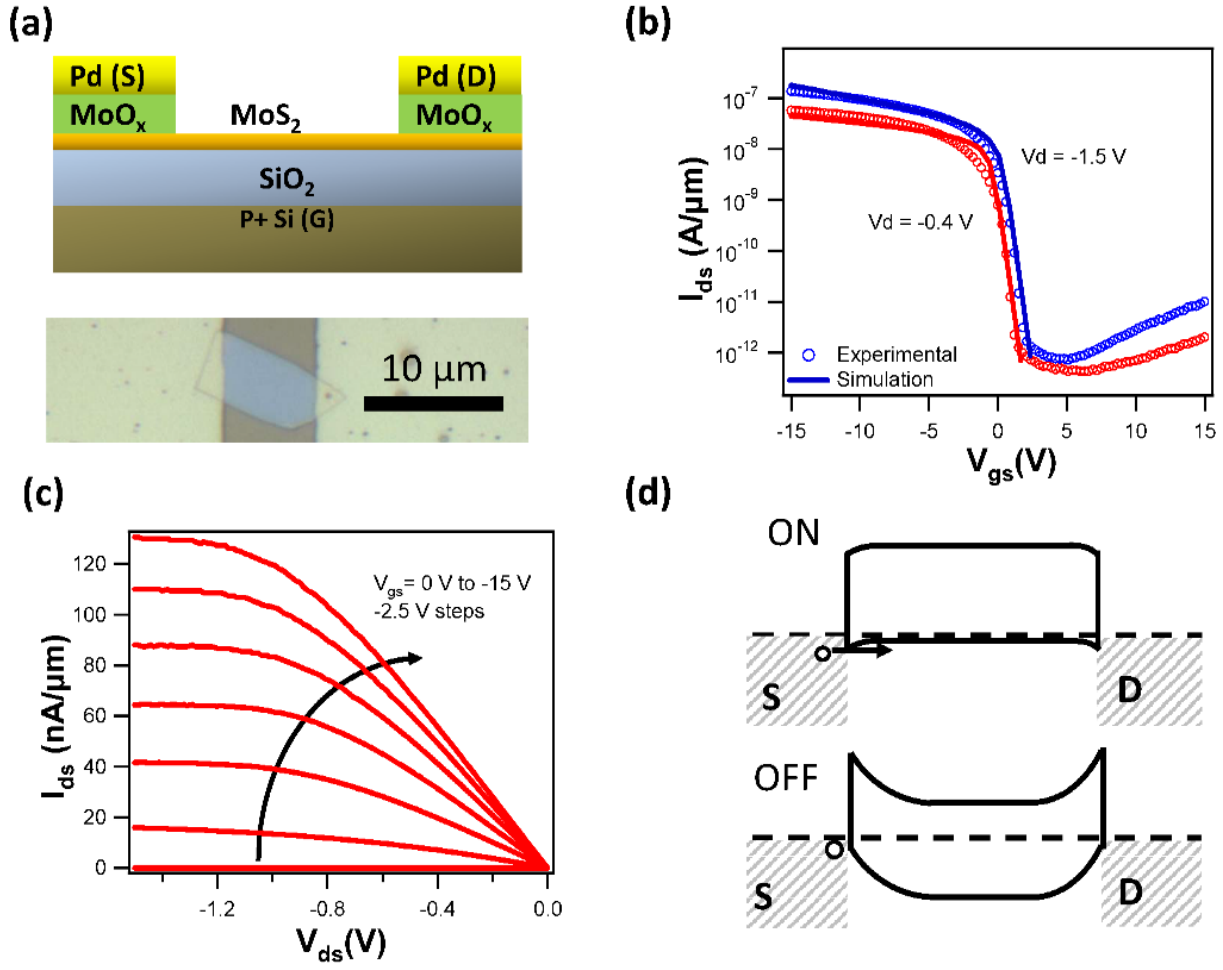

Figure 4.2. (a) Schematic and optical microscope image, (b) I_{ds} vs V_{gs} and (c) I_{ds} vs V_{ds} characteristics for a representative MoS_2 PFET with MoO_x contacts. (d) Qualitative band diagrams for the ON (top panel) and OFF (bottom panel) states of the MoS_2 PFET.

4.3.3 Device Simulations

2D simulations coupling drift-diffusion and Poisson relations were performed with TCAD Sentaurus to extract the SB heights from the experimental I_{ds} vs V_{gs} results. An in-plane effective mass of 0.45 m_0 for electrons and 0.43 m_0 for holes were assumed [21]. An electron mobility of 200 $cm^2/V\bullet s$ and hole mobility of 86 $cm^2/V\bullet s$ were assumed [22] [5]. The subthreshold slope (SS) of 410 mV/dec was fit with a uniform density of interface traps D_{it} of 6×10^{11} $cm^{-2}eV^{-1}$ across the MoS_2 bandgap at the MoS_2/SiO_2 interface. This value of SS is reasonable given we have multi-layer flakes on a thick (260 nm) backgate oxide. Threshold voltage shifts were applied to match each simulated curve with its respective experimental data. From the qualitative band diagram in figure 4.2d it is evident that with the non-negligible barrier to the valence band, we expect tunneling and thermionic emission to dominate the on-current characteristics. Thus a nonlocal tunneling model based on the Wentzel-Kramers-Brillouin (WKB) formalism was implemented at the contacts. An out-of-plane effective mass of 1.0 m_0 was used as the hole tunneling mass [21]. A hole SB height of 0.31 eV was used to fit the on-current to the experimental results. Such a low barrier height is surprising given that elemental metals have been shown to be Fermi level pinned ~1.1-1.2eV from the valence band of MoS_2 [14]. A good fit is obtained to the I_{ds} vs V_{gs} curve in the subthreshold, linear and saturation regimes of the device as shown in figure 4.2b.

4.3.4 I_{ds} vs V_{ds} Characteristics

I_{ds} vs V_{ds} characteristics are shown in figure 4.2c. Clear linear and saturation regimes are exhibited, indicating standard MOSFET device operation. The saturation current of typical long channel FETs is proportional to $(V_g-V_t)^2$, however in our device we observe that saturation current is proportional to V_g-V_t instead. This observation suggests that the device has non-negligible series resistance, most likely from the SB barrier height at the contacts [23].

4.3.5 Control MoS_2 Devices with Pd Contacts

In contrast, control devices fabricated with Pd contacts (without MoO_x) exhibit clear *n*-type characteristics (Figure 4.3). Figure 4.3 shows I_{ds} -V_{gs} electrical

characteristics of MoS_2 FETs with symmetrical a) Pd and b) Ni contacts. The fabrication procedures were the same as the MoO_x/MoS_2 PFETs, other than the different contact metal used. Specifically, all MoS_2 flakes in this study came from the same source crystal. Clear *n*-type characteristics with $I_{on}/I_{off} > 10^3$ are exhibited, consistent with literature [6, 14].

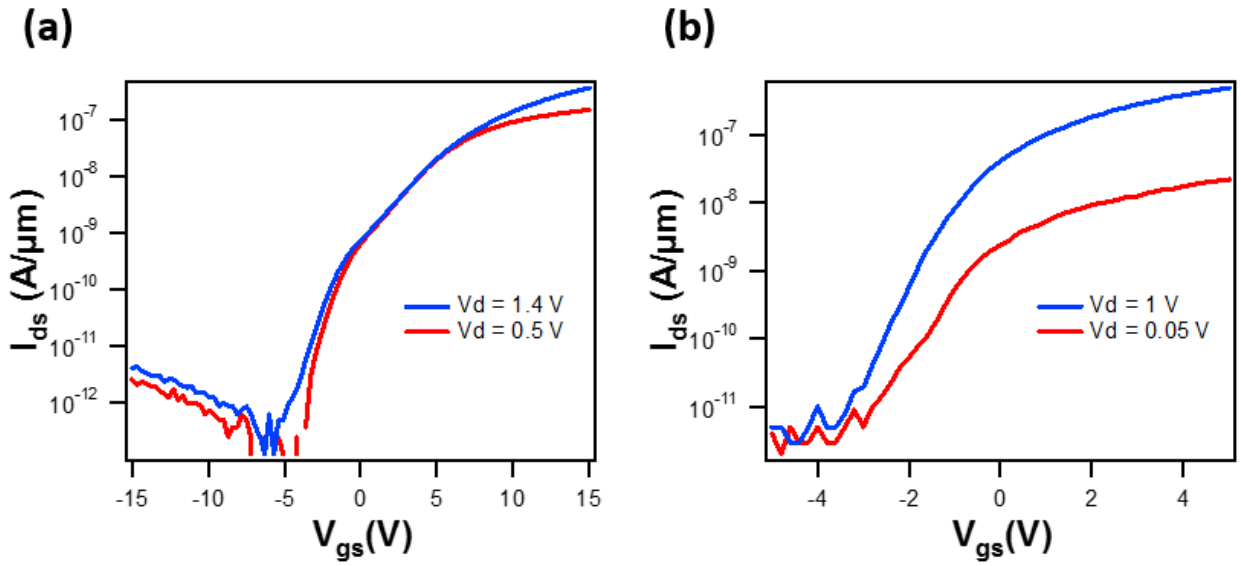

Figure 4.3. I_{ds} vs V_{gs} electrical characteristics of MoS_2 PFETs with symmetrical a) Pd and b) Ni contacts.

4.4 Origin of MoO_x Hole Injection Improvement

Next we investigate the origin of the hole injection improvement in MoO_x contacts as compared to elemental metals. An interface Fermi-level pinning parameter $S = \frac{\partial \Phi_p}{\partial \psi_c} = -\frac{\partial \Phi_n}{\partial \psi_c} = -0.1$ ($\Phi_{n/p}$=electron/hole SB height, ψ_c= contact workfunction) was previously extracted for elemental metal contacts [14]. Using this pinning parameter and the highest work function ψ_c = 6.6 eV we observed for MoO_x, we expect a lower bound SB height of Φ_p~ 1 eV for MoO_x/MoS_2 contacts. This value is significantly larger than our experimental observations and suggests a lower degree of Fermi-level pinning at MoO_x/MoS_2 contacts as compared to elemental contacts. This may be expected given the difference in the nature of the interface chemical bonding and the density of states at the Fermi level for MoO_x. Specifically, due to the low density of states at the Fermi level (see again Fig. 4.1b)

and the localized nature of the defect states in MoO_x, its tendency to form metal induced gap states is possibly less pronounced than that of elemental metals such as Pd [24] [25]. Alternatively interface states could originate from native defects of the MoS_2 surface or from surface damage caused by metal evaporation. If so, MoO_x possibly passivates and reduces the number of such states. Further experimental and theoretical investigations are necessary to understand the contact/TMDC interface for both MoO_x and elemental metals. Nevertheless, the work here clearly suggests that the advantage of MoO_x contacts for hole injection is not only due to its high work function, but also due to its better interface properties (i.e., lower degree of interface Fermi-level pinning) with TMDCs.

4.5 MoS_2 Schottky Diodes with MoO_x Contacts

4.5.1 Fabrication Process

MoS_2 Schottky diodes were studied in order to further demonstrate the utility of MoO_x as an effective hole contact to MoS_2. The process flow was identical to that for the MoS_2 PFETs, other than the fact that two photolithography steps were used to pattern Ni and MoO_x/Pd asymmetric contacts to the same MoS_2 flake. A device schematic and qualitative band diagram are shown in figures 4.4a and b. Specifically, Ni is used as an electron contact with a small SB height ($\Phi_{n,Ni}$) to the conduction band of MoS_2 according to previous reports [3] [6] and our control experiments reported in chapter 4.3.5. On the other hand, MoO_x is used as the hole contact with a small SB height (Φ_{p,MoO_x}) to the valence band of MoS_2 as previously discussed.

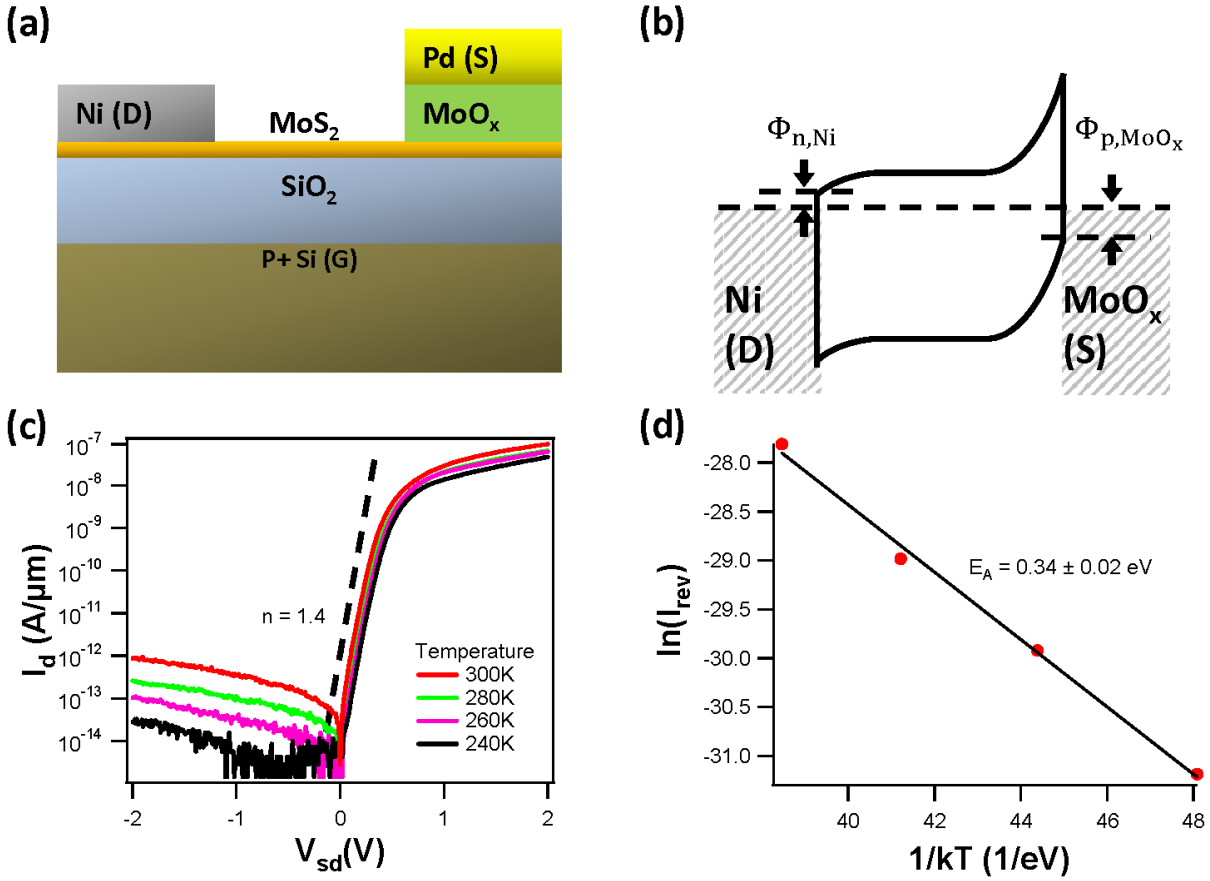

Figure 4.4. (a) Schematic for a representative MoS_2 Schottky diode made with asymmetric metal contacts. (b) Qualitative band structure of the device with asymmetric Ni and MoO_x electrodes used as electron and hole contacts, respectively. (c) Temperature dependent I_d vs V_{sd} electrical characteristics of the diode. (d) Barrier height extraction of the reverse bias current (I_{rev}) at V_{sd} = -2V from temperature dependent measurements.

4.5.2 Electrical Characteristics

The resulting electrical measurements with a grounded Si substrate for a 24 nm thick MoS_2 flake are shown in figure 4.4c. Clear rectification is shown with a forward/reverse bias current ratio of up to ~10^5. The direction of the rectification is consistent with that originating from the two asymmetric contacts discussed above (see band diagram in Fig. 4.4b). An ideality factor n of 1.4 at room temperature is extracted from the ideal diode region. The ideality factor of a diode typically varies

between 1 and 2 depending on the relative contribution of current from diffusion and recombination, respectively, assuming mid-gap trap states. The low value extracted for the ideality factor indicates a low contribution of recombination current and a low density of trap states at the MoO_x/MoS_2 junction and in the unintentionally doped MoS_2 [26].

4.5.3 Reverse Bias Analysis

By plotting the natural log of the reverse bias current I_{rev} at $V_{sd} = -2$ V as a function of 1/kT, the activation energy E_A of the reverse bias was extracted as 0.34 ± 0.02 eV (Fig. 4.4d), which most likely corresponds to phonon assisted tunneling mechanisms commonly observed in reverse biased Schottky diodes [27]. A small temperature dependence is observed in the $V_{sd} > 1$ V forward biased region of the diode. Assuming that this region is dominated by series resistance from the MoS_2 flake, this observation can be attributed to the small temperature dependence of the shallow dopants (i.e., un-intentional impurities) in MoS_2 in this temperature range.

4.6 WSe_2 PFETs with MoO_x Contacts

4.6.1 Fabrication Process and Electrical Characteristics

Given the success in contacting the valence band of MoS_2, we next fabricated PFETs using WSe_2, a promising *p*-type TMDC [2]. Unlike MoS_2, WSe_2 has been shown to exhibit a surface Fermi level pinning closer to the valence band edge, thereby, making it easier to obtain PFETs by using various metals. The fabrication process was analogous to the MoS_2 PFET other than the different flake exfoliated. A schematic of the device is shown in figure 4.5a. WSe_2 devices with 30 nm MoO_x/ 30 nm Pd contacts as well as a reference device with 30 nm Pd contacts were fabricated and compared to each other. The thicknesses of the WSe_2 flakes were 32 nm and 29 nm for the MoO_x and Pd contacted flakes, respectively.

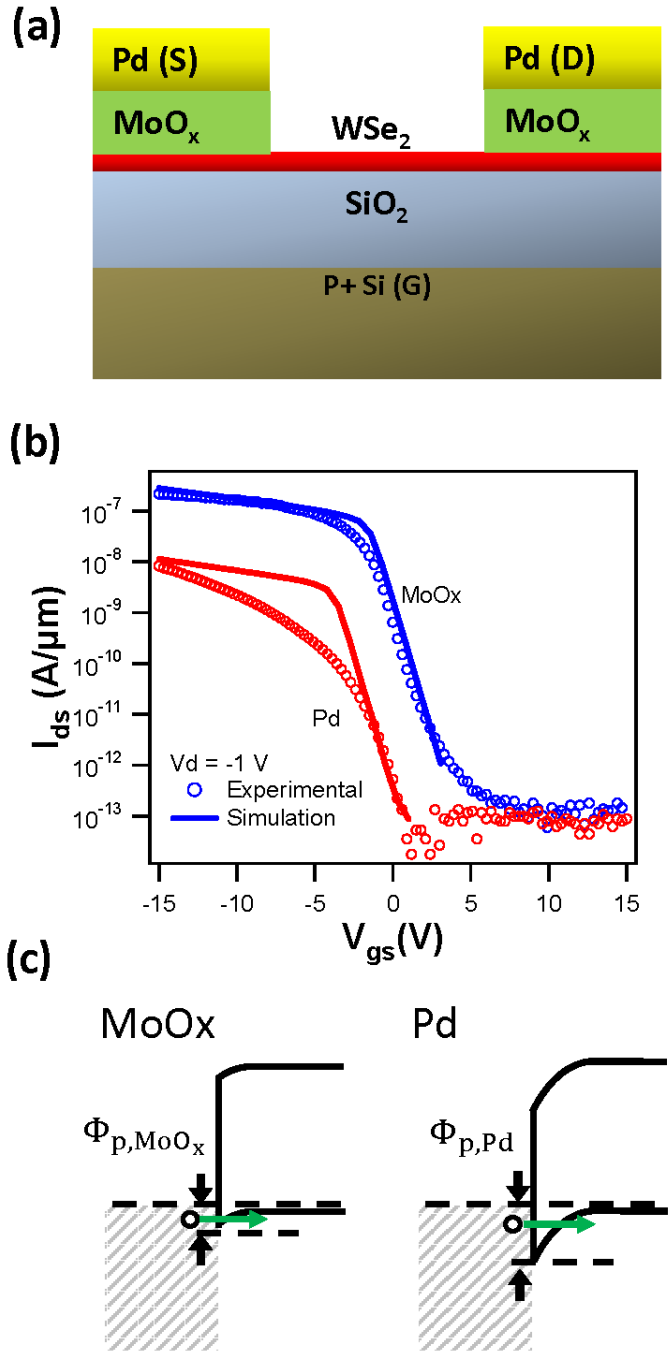

Figure 4.5. (a) Schematic, (b) I_{ds} vs V_{gs} characteristics and (c) qualitative band diagrams for WSe_2 devices contacted with MoO_x (left panel) and Pd alone (right panel). The hole barrier heights are indicated as Φ_{p,MoO_x} and $\Phi_{p,Pd}$ for the MoO_x and Pd contacted devices, respectively.

The resulting I_d vs V_{gs} characteristics measured in vacuum are shown in figure 4.5b. More than one order of magnitude improvement in ON current is observed in the MoO_x contacted WSe_2 device compared to the Pd contacted device.

4.6.2 Device Simulations

Sentaurus simulations were performed to investigate the origin of this improvement. A uniform D_{it} of $1.2x10^{12}$ $cm^{-2}eV^{-1}$ across the WSe_2 bandgap was used to fit the SS of 970 mV/dec. We assumed 0.3 m_0 for the in-plane effective mass of holes m_h [28]. Given the WSe_2 reduced electron-hole mass m_r = 0.24 m_0, the effective mass of electrons was assumed to be $m_e = (\frac{1}{m_r} - \frac{1}{m_h})^{-1}$= 1.2 m_0 [29]. An electron mobility of 200 $cm^2/V{\cdot}s$ and hole mobility of 329 $cm^2/V{\cdot}s$ were used [30] [31]. Again a non-local WKB model was used to simulate the contacts, with a 0.9 m_0 out-of-plane effective mass used as the hole tunneling mass parameter [32]. Hole SB heights of 0.29 eV and 0.37 eV were used to fit the on current of the MoO_x and Pd contacted devices, respectively. From the qualitative band diagrams in figure 4.5c, we see the lower hole barrier height in the MoO_x contacted devices facilitates improved hole injection, resulting in higher on currents. The simulated curves match the experimental results well. The overestimation of the simulation current for the Pd contacted device in the subthreshold region could be ascribed to the oversimplification of the WSe_2/contact and dielectric interfaces. Atomic simulations are needed in the future to better account for the WSe_2/contact interfaces.

4.7 Air Stability of MoO_x

We also characterized the stability of devices in air. The PFETs measured are highly stable over time, showing minimal change in I-V characteristics over the course of >2 weeks exposure to air (Fig. 4.6a). However when measured in air instead of vacuum, all MoO_x devices show a reversible lowering of on-current (Fig. 4.6b). Original device characteristics are restored upon placement in vacuum. This observation can be attributed to the sensitivity of the MoO_x work function to ambient gas exposure [16]. This behavior is similar to elemental metal contacts to devices, which also show barrier height modulation due to gas exposure, and can be remedied by encapsulating the device [7] [9].

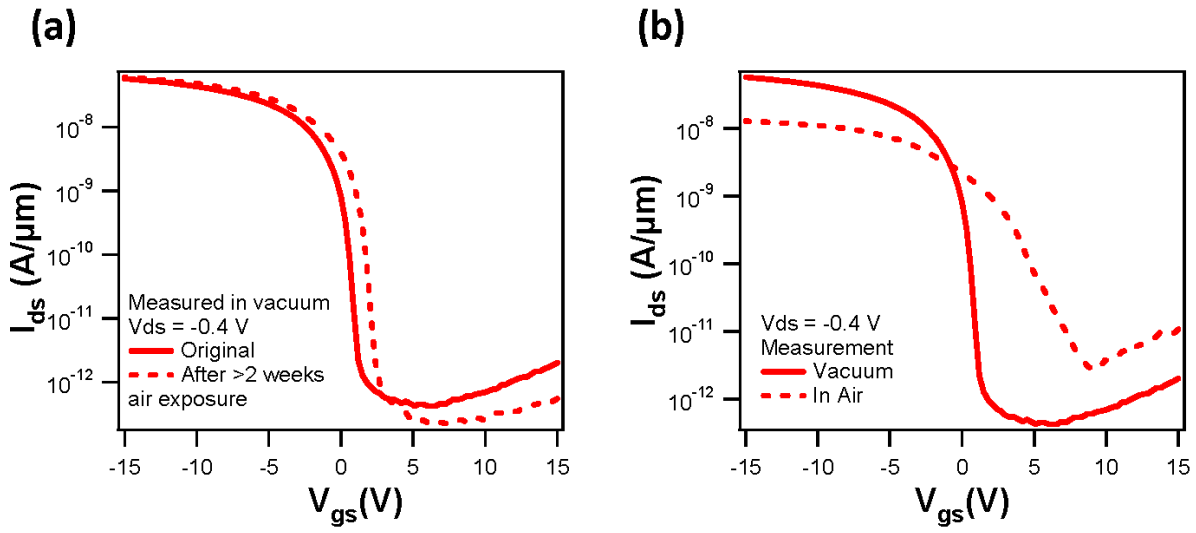

Figure 4.6. I_{ds} - V_{gs} characteristics of a MoS_2 PFET with MoO_x contacts a) before and after 2 weeks exposure in air, and b) measured in air and in vacuum.

4.8 Conclusions

In conclusion, this study explores high work function MoO_x contacts to the valence band of TMDCs for efficient hole injection, addressing a key challenge for obtaining high performance *p*-type and complementary logic components. MoO_x contacts to MoS_2 enables fabrication of PFETs with I_{on}/I_{off}~10^4 despite previous studies showing metals being Fermi level pinned near the conduction band edge of MoS_2 [14]. MoS_2 Schottky diodes with asymmetric MoO_x and Ni contacts exhibit rectifying behavior. Finally, WSe_2 PFETs with MoO_x contacts exhibit an order of magnitude improvement in I_{on} over Pd contacted WSe_2 PFETs. The observed FET behavior could be captured well by 2D simulations. Overall this study is an invitation to explore transition metal oxides with extreme work functions as selective carrier contacts to TMDCs for realization of high performance devices.

References

[1] Liu, L.-T.; Kumar, B. B.; Ouyang, Y.; Guo, J. *IEEE Trans. Electron Devices* **2011**, 58,3042-3047.

[2] Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. *Nano Lett.* **2012**, 12, 3788−92.

[3] Liu, H.; Neal, A. T.; Ye, P. D. *ACS Nano* **2012**, 6, 8563-8569.

[4] Qiu, H.; Pan, L.; Yao, Z.; Li, J.; Shi, Y.; Wang, X. *Appl. Phys. Lett.* **2012**, 100, 123104.

[5] Kim, S.; Konar, A.; Hwang, W.-S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.-B.; Choi, J.-Y.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. *Nat. Commun.* **2012**, 3, 1011.

[6] Neal, A.; Liu, H.; Gu, J.; Ye, P.; *IEEE Device Research Conf.* , **2012**, 65-66.

[7] Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. *Nature*, **2003**, 424, 654-657.

[8] Fan, Z.; Ho, J. C.; Jacobson, Z. A.; Yerushalmi, R.; Alley, R. L.; Razavi, H.; Javey, A. *Nano Letters* **2008** 8, 20-25.

[9] Skucha, K.; Fan, Z.; Jeon, K.; Javey, A.; Boser, B. *Sens. Actuators, B*, **2010,** 145, 232-238.

[10] Li, X.; Zhang, G.; Bai, X.; Sun, X.; Wang, X.; Wang E.; Dai, H. *Nat. Nanotechnol.* **2008,** 3, 538-542.

[11] Michaelson, H. B. *J. Appl. Phys.* **1977**, 48, 4729.

[12] Lee, K.; Kim, H.-Y.; Lotya, M.; Coleman, J. N.; Kim, G.-T.; Duesberg, G. S. *Adv. Mater.* 2011, 23, 4178–4182.

[13] Gmelin Handbook of Inorganic and Organometallic Chemistry, 8th ed.; Springer-Verlag: Berlin, 1995; Vol. B7.

[14] Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. *Nano Lett.* **2013**, 13, 100-105.

[15] Fontana, M.; Deppe, T.; Boyd, A. K.; Rinzan, M.; Liu, A. Y.; Paranjape, M.; Barbara, P. *Sci. Rep.* 2013, 3, 1634.

[16] Battaglia, C.; Yin, X.; Zheng, M.; Sharp, I. D.; Chen, T.; McDonnell, S.; Azcatl, A.; Carraro, C.; Maboudian, R.; Wallace, R. M.; Javey. *Nano Lett.*, in press.

[17] Kröger, M.; Hamwi, S.; Meyer, J.; Riedl, T.; Kowalsky, W.; Kahn, A. *Appl. Phys. Lett.* **2009**, 95, 123301.

[18] Zilberberg, K.; Gharbi, H.; Behrendt, A.; Trost, S.; Riedl, T. *ACS Appl. Mater. Interfaces* **2012,** 4, 1164-1168.

[19] Lin, H.; Irfan; Xia, W.; Wu, H. N.; Gao, Y.; Tang, C. W. *Sol. Energy Mater. Sol. Cells* **2012**, 99, 349-355.

[20] Wallace, R. M. *ECS Trans.* **2008**, 16, 255-271.

[21] Peelaers, H.; VandeWalle, C. G. *Phys. Rev. B: Condens. Matter Mater. Phys*. **2012**, 86, 241401.

[22] Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y. *Nano Letters* **2012** *12* (3), 1136-1140.

[23] Hu, C. MOS Transistor. *Modern Semiconductor Devices for Integrated Circuits*, 1st Edition; Prentice Hall: New Jersey, 2010.

[24] Heine, V. *Phys. Rev.* **1965**, 138, 1689.

[25] Louie, S. G.; Chelikowsky, J. R.; Cohen, M. L. *J. Vac. Sci. Technol.* **1976**, 13, 790-797.

[26] Chuang, S.; Kapadia, R.; Fang, H.; Chang, T. C.; Yen, W.-C.; Chueh, Y.-L.; Javey, A. *Appl. Phys. Lett.* **2013**, 102, 242101.

[27] Pipinys, P.; Pipiniene, A.; Rimeika, A. *J. Appl. Phys.* **1999***,* 86, 6875-6878.

[28] Klein, A.; Dolatzoglou, P.; Lux-Steiner, M.; Bucher, E. *Sol. Energy Mater. Sol. Cells* **1997**, 46, 175-186.

[29] Consadori, F.; Frindt, R. F. *Phys. Rev. B* **1970**, 2, 4893-4896.

[30] Solanki, G. K.; Gujarathi, D. N.; Deshpande, M. P.; Lakshminarayana, D.; Agarwal, M. K. *Cryst. Res. Technol.* **2008**, 43, 179–185.

[31] Fivaz, R. C.; Schmid, Ph. E. Transport Properties of Layered Semiconductors in *Physics and chemistry of materials with layered structures*; P. A. Lee. Eds.; D. Reidel Publishing Company: Massachusetts, 1976; Vol. 4, pp 343-383.

[32] Coehoorn, R.; Haas, C.; de Groot, R. A. *Phys. Rev. B* **1987**, 35, 6203–6206.

Chapter 5

[5]InAs/WSe_2 Heterojunctions

5.1 Introduction

The development of heterojunctions has led to numerous high impact discoveries and applications [1-5]. Heterostructures are typically grown with epitaxial methods to ensure the high quality and crystallinity of the participating material layers. However in order to obtain high quality interfaces with traditional epitaxial methods, the lattice constant and crystal structure of each participating material must be similar. This severely limits the possible material pairs that could be utilized in heterostructures. Many research efforts have focused on resolving this issue [6-14]. One path to overcome this limitation would be to form a heterostructure by layer transfer of its components. The key advantage of this method is that it would theoretically allow for the complete freedom of material choice in the hetero-stacks. In addition, there would be no interdiffusion of atoms at the interface, given that the transfer is conducted at room temperature. It remains unclear whether high quality interfaces without large density of trap states and with near-ideal electrical characteristics can be obtained with this method. So far, van der Waals heterojunctions have not been thoroughly explored for materials other than carbon nanotubes, graphene, boron nitride, and tungsten disulphide [10-14].

[5] Reprinted with permission from Steven Chuang et al., Applied Physics Letters, 102, 242101, 2013. Copyright 2013, AIP Publishing LLC.

Here, we fabricate InAs/WSe_2 thin film diodes by transferring their respective quantum membranes (QM) upon one another. Notably, this heterostructure consists of two materials with completely different crystal structures (figure 5.1b). An ideality factor of ~1.1 and low reverse bias currents were measured, suggesting a clean interface between the two materials. Simulations were used to investigate the band structure and I-V characteristics of the diode.

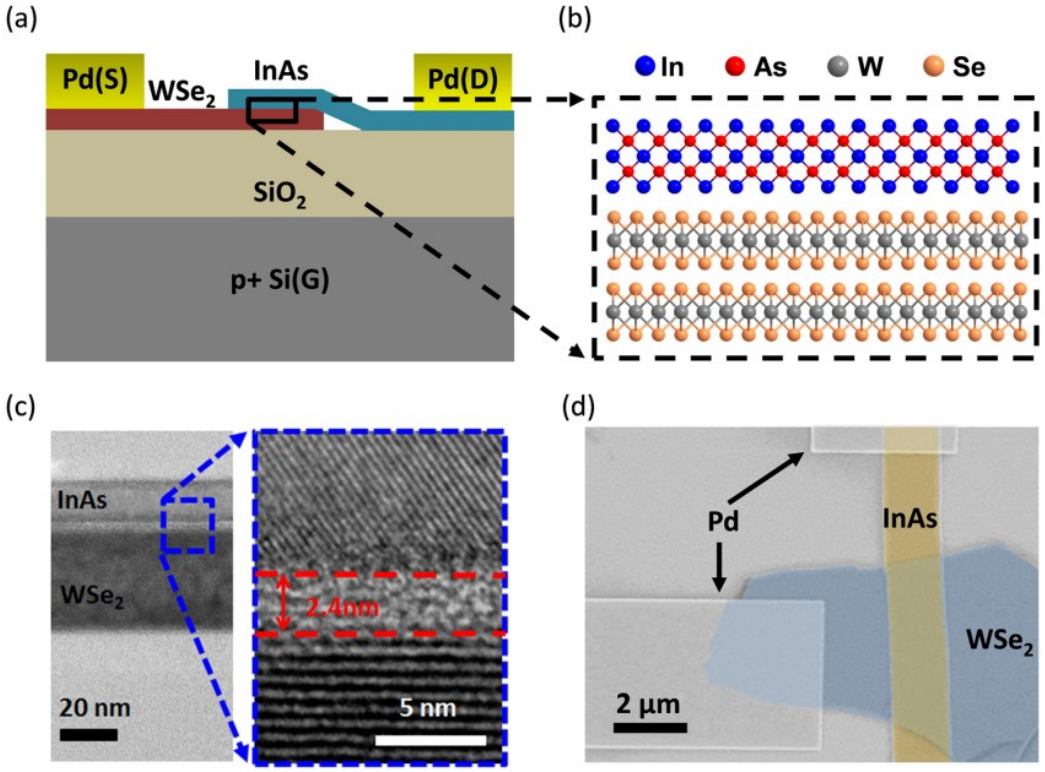

Figure 5.1. (a)Cross-sectional schematic of an InAs/WSe_2 device explored in this study. (b)Ideal atomic cross-sectional view of InAs/WSe_2 interface, depicting 2 different crystal structures. (c)HRTEM image of fabricated InAs/WSe_2 heterostructure. (d)False color SEM image of fabricated InAs/WSe_2 device.

The InAs/WSe_2 system was chosen to demonstrate the viability of this layer transfer heterostructure method since previously we have shown layer transferred InAs and WSe_2 membranes exhibiting low density of interface traps. The transfer of ultra-thin, high quality single crystalline InAs QMs has been thoroughly explored [15-23]. High performance WSe_2 devices have been demonstrated with the mechanical exfoliation technique [24]. In particular, WSe_2 is an ideal bottom layer for the heterostructure because it provides a freshly cleaved, pristine top

surface, as demonstrated by the 60mV/decade subthreshold slope exhibited by its MOSFETs [24]. Given that InAs and WSe_2 layers are intrinsically n-type and p-type, respectively, their combined structure will form a diode for electrical analysis of the interface. It is particularly important to reduce the Schottky barriers to each semiconductor, as Schottky diodes might mask the pn-junction diode performance. Low resistance metal contacts are readily formed to InAs as previously reported due to its low conduction band edge [25]. On the other hand it is hard to form ohmic metal contacts with WSe_2 due to its large bandgap. Previous studies by our group have shown that the Schottky barrier to WSe_2 can be significantly thinned by NO_2 doping [24], thereby enabling formation of low resistance contacts for hole injection.

5.2 Fabrication Process

The fabrication process of the InAs/WSe_2 van der Waals stack is as follows. WSe_2 QMs were first mechanically exfoliated onto a Si/SiO_2 (270 nm) substrate as previously described [24]. InAs QMs were then transferred from an epitaxial substrate onto the WSe_2 QMs [15]. The InAs QMs were dipped in 1%HF for ~1min to clean its surface right before being transferred onto the WSe_2 QMs. Pd contacts (~40nm thick) were defined on the InAs and WSe_2 QMs by electron beam lithography, metallization and lift-off. The Si substrate is heavily doped and serves as the global back gate. Figure 5.1a shows a cross-sectional diagram of the fabricated devices.

5.3 Electron Microscopy Characterizations

Figure 5.1c shows a transmission electron microscopy (TEM) image of an InAs/WSe_2 stack. From the TEM image we see a distinct InAs single-crystal membrane stacked on a layered WSe_2 crystal with a ~2.4 nm thick intermediate layer in-between. Previous InAs QM studies suggest that the intermediate layer is the native oxide of InAs [15]. WSe_2 is a 2D crystal that perfectly terminates on its surface, and does not form native oxides under ambient conditions. The InAs/WSe_2 stack appears conformal, with no voids formed between the layers at least within the area examined by TEM. Through device simulations later in this paper, we demonstrate that this system can be treated as though the InAs was stacked directly on top of WSe_2, and the effect of the ultra-thin intermediate oxide on the diode characteristics is negligible. A scanning electron microscopy (SEM) image of an

InAs/WSe_2 diode is depicted in figure 5.1d, depicting well defined junction areas and contacts.

5.4 Electrical Characterization

The electrical characterization of a representative device (junction area ~2.5μm^2) is shown in figure 5.2. Without any post-fabrication treatment (i.e., no surface doping of WSe_2), the device exhibits clear rectifying behavior (Fig. 5.2a). The reverse bias current was below the noise floor of the measurement. The relatively low forward bias current can be ascribed to the large contact resistance from the WSe_2/Pd junction. By grounding the WSe_2 electrode and increasing V_{SG}, we observe an increase in forward bias current caused by the modulation of the WSe_2/Pd Schottky junction contact resistance (Fig. 5.2a). The lack of gate dependence of the ideal diode region suggests that V_{SG} has a negligible effect on the InAs/WSe_2 junction and its band alignments. An ideality factor of ~1.1 is obtained, indicating a clean interface between the InAs and WSe_2 QMs.

In order to reduce the WSe_2/Pd contact resistance, we exposed the devices to NO_2 gas (Fig. 5.2b). As previously reported, NO_2 molecules cause strong *p*-doping of WSe_2, and result in near ohmic Pd contacts to the valence band of WSe_2. On the other hand, NO_2 treatment does not affect the InAs conductivity and InAs/Pd junction. Previous studies have shown that InAs conduction changes <2x under exposure to NO_2 gas [26]. The 15nm thick InAs membrane which is the top layer of the junction should prevent NO_2 from reaching the InAs/WSe_2 junction. After exposure to NO_2, the diode exhibited ~10^3 higher forward bias currents while maintaining an ideality factor of ~1.1 and a reverse bias current below the noise floor. In total, the diode exhibits a forward/reverse current ratio >10^6 for an applied voltage range of 2V to -2V. The slight gate dependence of the forward bias current indicates the change in the band-offset between the semiconductors by the gate potential.

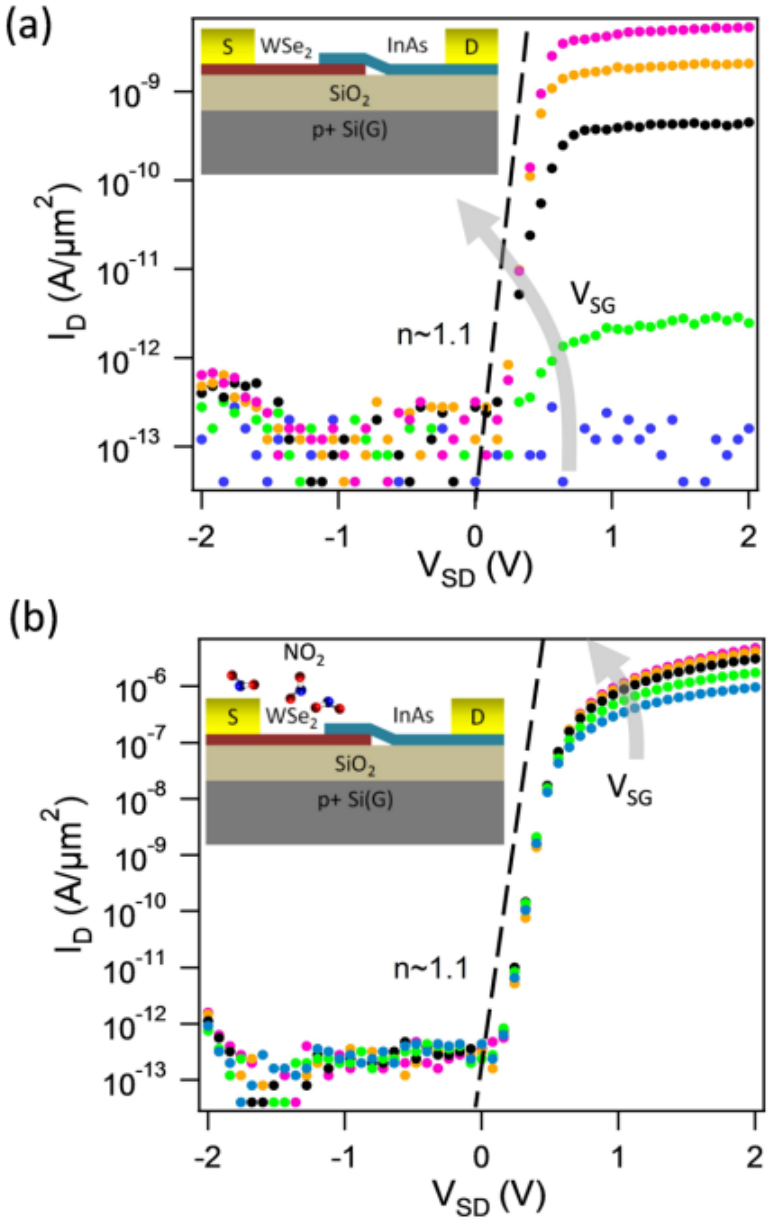

Figure 5.2. I_D vs V_{SD} plots for an InAs/WSe_2 diode device with a [-4:2:4] V_{SG} bias (a) without NO_2 gas doping and (b) with NO_2 gas doping. The insets show the cross sectional schematics of the measured devices.

5.5 Band Structure Simulation

In order to better understand the I-V characteristics, electrostatic simulations were performed with TCAD Sentaurus 2012 to simulate the band structure of the

InAs/WSe_2 diode with and without NO_2 doping. Hole and electron concentrations of $5x10^{15}cm^{-3}$ and $1.5x10^{18}cm^{-3}$ were used for WSe_2 and InAs, respectively, in the absence of NO_2 doping, as suggested by reports of their respective undoped thin films [20,27]. The WSe_2/Pd Schottky barrier height was determined by the difference between the semiconductor electron affinity and metal work function. The InAs/Pd Schottky barrier to the conduction band was assumed to be pinned at -0.15 eV as suggested by literature [28]. The simulation results without doping (Fig. 5.3a) suggest that the WSe_2/InAs p-n junction dominates the behavior at low forward biases, while a significant Schottky barrier to the WSe_2 valence band (i.e., a large parasitic resistance) will dominate at higher forward biases as observed experimentally. This is expected for any given diode in that the parasitic resistances lead to current saturation under large forward bias. From the band bending we see that the majority of the depletion region lies in WSe_2.

In order to simulate the band structure under NO_2 doping, a highly doped WSe_2 layer ($Na=1x10^{19}cm^{-3}$) [24] was introduced as shown in the inset of figure 5.3b. As discussed previously, it is assumed that the NO_2 has no effects on the InAs, InAs/Pd contact and InAs/WSe_2 junction (since InAs is on top of WSe_2 and protects it from exposure to NO_2 in the junction area). The resulting band structure (Fig. 5.3b) shows dramatic thinning of the WSe_2 Schottky barrier, thus promoting hole tunneling through the barrier and reducing the WSe_2/Pd contact resistance. This finding is consistent with the experimental I-V curves (Fig. 5.2b), where the forward bias current is drastically enhanced by ~3 orders of magnitude upon NO_2 exposure.

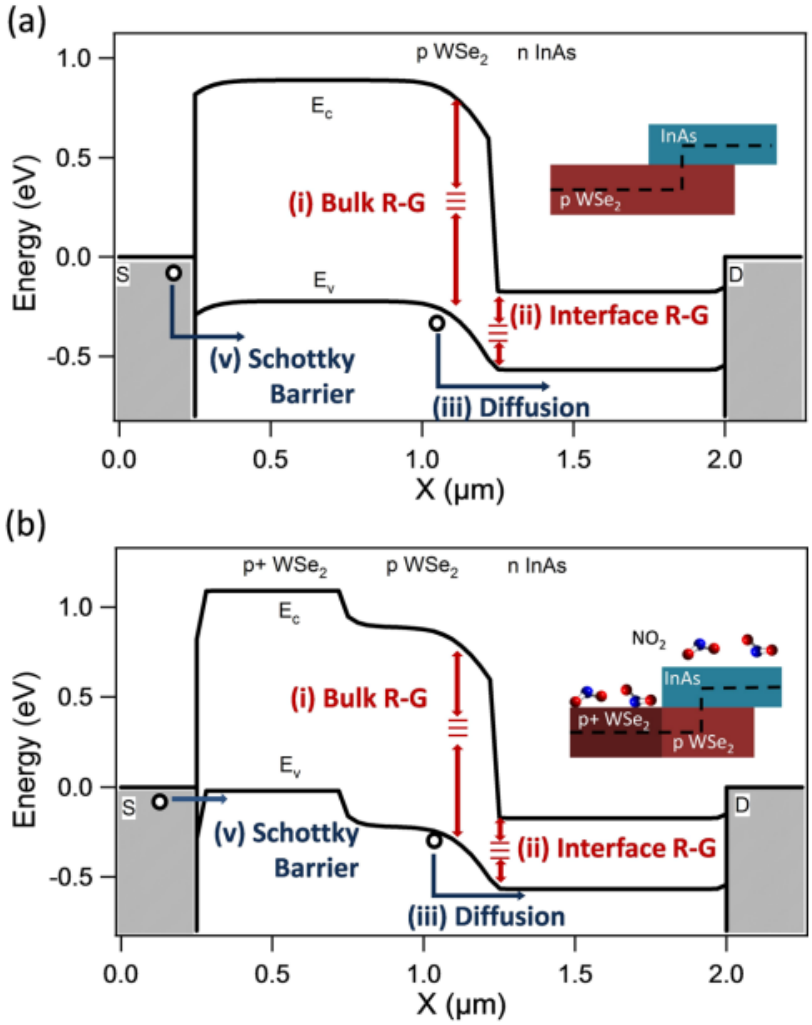

Figure 5.3. Electrostatic band structure simulation results for an InAs/WSe_2 stack (a) without NO_2 gas doping and (b) with NO_2 gas doping. The insets show cross sectional schematics of the simulated structures. Important current processes are also shown.

5.6 Analysis of I-V Characteristics

In addition to a quantitative simulation of the diode band diagram, we analyze the heterodiode I-V characteristics to further understand the effect of each junction. Specifically, a standard diode's I-V characteristics can be described by five different regimes[29]: (i) reverse-bias, dominated by recombination-generation (R-G) current as well as drift current; (ii) low-voltage forward-bias, governed by R-G

current; (iii) forward-bias, described by the ideal diode equations; (iv) high-injection forward-bias region, where diffusion current levels become so great that the injected minority carrier concentration equals the majority carrier concentration; and (v) series-resistance forward-bias region, where current is limited by parasitic resistances. The processes that drive these regimes in our device are depicted in figure 5.3: specifically, R-G mechanisms (i, ii), diffusion over the p-n junction barrier (iii), and the parasitic resistance due to the Schottky barrier of the Pd/WSe_2 junction (v).

First, the reverse-bias current and low-voltage forward-bias current of the heterodiode will be considered. It should be noted that the measured current in reverse-bias is extremely low, below the 10^{-12} A/μm^2 noise floor of the measurement setup, and no R-G current dominated forward-bias regime is observed, suggesting that the RG current is nearly negligible in our devices. Such low RG current values can be ascribed to: firstly, the depletion region occurring entirely in the higher bandgap WSe_2 due to the higher carrier concentration in InAs; secondly, the small volume of the depletion region due to the relatively thin body of the WSe_2; and thirdly, it is hypothesized that the density of interface traps existing at the InAs/WSe_2 interface must be low. Electron concentration levels previously extracted from similar InAs membranes without intentional doping [20] indicate that the InAs is doped high enough such that the depletion region is pushed mostly into the WSe_2, as shown in the band diagram simulations. Furthermore, WSe_2 Schottky FETs previously fabricated also show extremely low off currents, suggesting that WSe_2 R-G currents are below the noise floor of our measurements [24].

Next, we discuss the ideal diode region. This region is often described by the ideality factor, η, which ranges from $\eta = 1$ for an ideal diode to $\eta = 2$ for an R-G current dominated diode. Our device exhibits $\eta = 1.1$, further supporting the conclusion that the device has R-G current levels significantly lower than the diffusion current. Finally, the high forward bias region is dominated by the WSe_2 /Pd Schottky barrier, which ultimately limits the forward-bias current. Note that the series resistance and high injection regimes cannot be clearly distinguished here given the relatively large resistance arising from the WSe_2/Pd Schottky contacts. In summary, our device exhibits an extremely low reverse bias RG current region, a nearly ideal diode region and a high forward bias region dominated by the WSe_2/Pd Schottky barrier, also supported by the experimental and simulation results shown next.

5.7 Device Simulation

2D simulations coupling Poisson's and drift diffusion relations were performed with TCAD Sentaurus 2012 to analyze the electrical characteristics of the heterostructure diode after NO_2 doping (Fig. 5.4). Ohmic contacts were assumed for the InAs/Pd and WSe_2/Pd junctions [24, 25]. The forward current was fit with a series resistance of 5kΩ/μm to account for parasitic resistances and the residual WSe_2/Pd Schottky barrier resistance, even after doping. The same doping concentrations mentioned previously were used. A low field minority carrier lifetime of $3x10^{-8}$s and 10^{-9}s was assumed for InAs and WSe_2, respectively [30, 31]. A uniform density of traps across the InAs bandgap at the InAs/WSe_2 interface with $10^{-15}cm^2$ capture cross sections was assumed [32]. A density of interface traps of $10^{11}cm^{-2}eV^{-1}$ was used as a fitting parameter. The reasonable fit between simulation and experimental results indicates that the InAs/WSe_2 diode electrical behavior can be described well by standard diode theory.

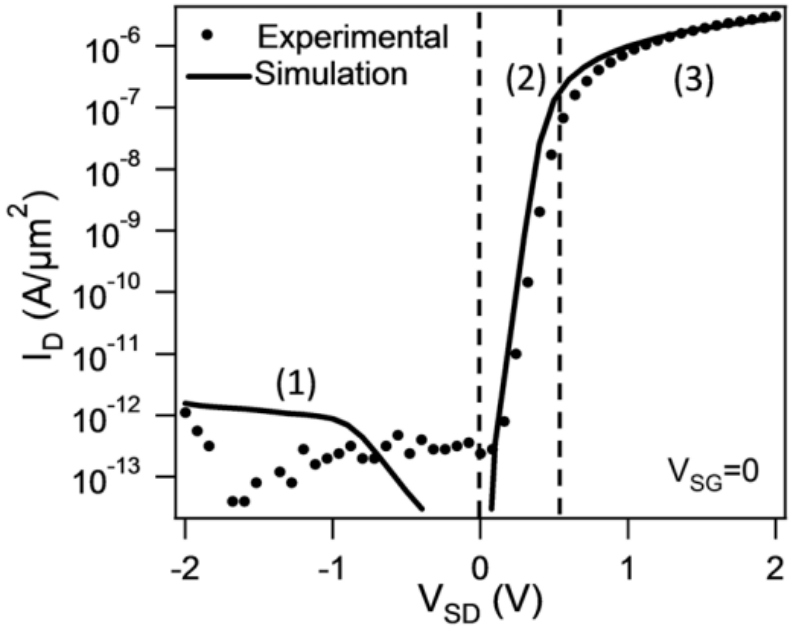

Figure 5.4. Experimental and simulation results for an InAs/WSe_2 diode under NO_2 gas doping, depicting 3 areas of operation dominated by different processes: (1) recombination-generation, (2) ideal diode, and (3) parasitic resistances.

5.8 Conclusions

In summary, a novel InAs/WSe_2 heterostructure, inconceivable by traditional epitaxial techniques alone, was fabricated by the layer transfer of each material. It exhibits an on/off current ratio $>10^6$ after reducing the WSe_2/Pd contact resistance with NO_2 doping, a clear indication of rectification from the InAs/WSe_2 junction. An ideality factor of ~1.1 was observed, indicating a clean interface between the two materials. Simulations of the observed I-V characteristics indicate that its behavior can be explained by standard diode theory. This study paves way for the electrical analysis and understanding of a whole new avenue of heterojunctions previously thought impossible.

References

1. H. Kroemer and J. Heber, Nat. Materials **9**, 372 (2010).

2. L. Wang, E. Yu, Y. Taur, P. Asbeck, IEEE Electron Device Lett. **31**, 431 (2010).

3. R.-T. Huang, Y.-Y. Tu, D. Kasemset, N. Nouri, C. Colvard, and D. Ackley, Appl. Phys. Lett. **67**, 550 (1990)

4. R. Dingle, H. L. Störmer, A. C. Gossard, and W. Wiegmann , Appl. Phys. Lett. **33**, 665 (1978)

5. M. Wolf, Proc. Of IRE **48**, 1246 (1960).

6. A. Koma , Thin Solid Films **216**, 72 (1992)

7. K. Saikia, K. Uenoa, T. Shimadaa, A. Komaa, J. of Crystal Growth **95**, 603 (1989)

8. M. P. Levendorf, C.-J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. A. Muller and J. Park, Nature **48**, 627 (2012)

9. L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, Science **335**, 947 (2012)

10. W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang and X. Duan, Nature Mat. **12**, 246 (2012)

11. L. A. Ponomarenko, A. K. Geim, A. A. Zhukov, R. Jalil, S. V. Morozov, K. S. Novoselov, I. V. Grigorieva, E. H. Hill, V. V. Cheianov, V. I. Fal'ko, K. Watanabe, T. Taniguchi and R. V. Gorbachev, Nature Physics **7**, 958 (2011)

12. A. S. Mayorov , R. V. Gorbachev , S. V. Morozov , L. Britnell , R. Jalil, L. A. Ponomarenko , P. Blake , K. S. Novoselov , K. Watanabe , T. Taniguchi , and A. K. Geim, Nano Lett. **11**, 2396 (2011).

13. C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard and J. Hone, Nature Nano. **5**, 722 (2010)

14. T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov and A. Mishchenko, Nature Nano. **8**, 100 (2013)

15. H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, Nature **468**, 286, (2010)

16. H. Fang, M. Madsen, C. Carraro, K. Takei, H. S. Kim, E. Plis, S.-Y. Chen, S. Krishna, Y.-L. Chueh, R. Maboudian and A. Javey. , Appl. Phys. Lett. **98**, 012111, (2011)

17. A. C. Ford, C. W. Yeung, S. Chuang, H. S. Kim, E. Plis, S. Krishna, C. Hu and A. Javey, Appl. Phys. Lett. **98**, 113105 (2011)

18. M. Madsen, K. Takei, R. Kapadia, H. Fang, H. Ko, T. Takahashi, A. C. Ford, M. H. Lee and A. Javey, Adv. Mater. **23**, 3115 (2011).

19. K. Takei, S. Chuang, H. Fang, R. Kapadia, C.-H. Liu, J. Nah, H. S. Kim, E. Plis, S. Krishna, Y.-L. Chueh and A. Javey, Appl. Phys. Lett. **99**, 103507 (2011).

20. K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C.-H. Liu, Y.-L. Chueh, E. Plis, S. Krishna, H. A. Bechtel, J. Guo and A. Javey, Nano Lett. **11**, 5008 (2011)

21. J. Nah, S. B. Kumar, H. Fang, Y.-Z. Chen, E. Plis, Y.-L. Chueh, S. Krishna, J. Guo and A. Javey, J. of Phys. Chem. C **116**, 9750 (2012)

22. J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna and A. Javey, Nano Lett. **12**, 3592 (2012).

23. C. Wang, J.-C. Chien, H. Fang, K. Takei, J. Nah, E. Plis, S. Krishna, A. M. Niknejad and A. Javey, Nano Lett. **12**, 4140 (2012).

24. H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi and A. Javey, Nano Lett. **12**, 3788 (2012)

25. C. K. Peng, J. Chen, J. Chyi, and H. Morkoç, J. Appl. Phys. **64**, 429 (1988)

26. P.Offermans, M. Crego-Calama and S.t H. Brongersma, Nano Lett. **10**, 2412 (2010)

27. A. Jäger-Waldau and E. Bucher, Thin Solid Films **200**, 157 (1991)

28. N. Li, E. S. Harmon, J. Hyland, D. B. Salzman, T. P. Ma, Y. Xuan, and P. D. Ye, Appl. Phys. Lett. **92**, 143507 (2008)

29. S. M Tze and K. K. Ng. *Physics of Semiconductor Devices Third Edition*; John Wiley & Sons: New Jersey, 2007.

30. A. Kleina, Y. Tomma, R. Schlafa, C. Pettenkofera, W. Jaegermanna, M. Lux-Steinerb, and E. Bucherc, Solar Energy Mater. **51**, 181 (1998)

31. V. Tetyorkin , A. Sukach and A. Tkachuk, Advances in Photodiodes, pp. 432 (InTech, 2011)

32. C.J. Park, H.B. Kim, Y.H. Lee, D.Y. Kim, T.W. Kang, C.Y. Hong, H.Y. Cho and M.D. Kim, J. of Crystal Growth **227-228**, 1057 (2001)

Chapter 6

Conclusions

The continued development of low dimensional channel transistors is inevitable. Device simulations show that scaling cannot continue with the bulk paradigm [1]. Currently industry is already implementing 2D thin film channels in high-performance logic devices. As industry continues to reap the benefit of scaling, it will require device and material innovations at the nanoscopic scale. This necessity motivates my work at Berkeley. At the end of this thesis, it is useful to place everything in context, focus on key findings and plan for the future.

Quasi-2D InAsSb thin film n-FETs were explored in chapter 2. III-V semiconductors exhibit outstanding transport properties, and their thin film manifestations offer promising electrostatics for highly scaled transistors. This work was part of a series of III-V thin-film on insulator studies that overcame many key challenges of the field [2] [3] [4]: integration on industry friendly silicon; dramatic reduction of leakage currents; simplification of device structure for lucid transport studies; etc. While early works focused entirely on InAs, this study was one of the first to utilize a different channel material. The resulting ~2x boost in transistor effective mobility demonstrates the viability and effectiveness of channel material engineering with this platform. However, the InAsSb devices suffered from poor gate control due to interface states in the gate stack. For future devices, detailed studies and engineering of the InAsSb surface states are needed to address this problem. This work also encourages further exploration of different channel materials for III-V on insulator transistors.

1D InAs nanowire (NW) n-FETs were explored in chapter 3. In particular we studied ballistic transport, the highest current density regime of all transistors, achievable only with ultra-short channel lengths on the order of the carrier mean free path. By using a quantized system, we isolated transport within single subbands and were capable of gauging how close the electron transport was to the ballistic limit. We achieved one of the most ballistic inorganic devices (~80% theoretical limit) and extracted a mean free path of ~150nm. Temperature dependent transport studies revealed that the dominating scattering mechanism was surface roughness scattering. This revelation highlights a conundrum for III-V FETs: although its low effective mass enables high carrier velocities, at small length scales quantization magnifies band edge roughness from channel width/diameter variations. In the long term, the viability of III-V nanomaterials for highly scaled FETs requires further study. In the short term, III-V materials are one of the few platforms that allow exploration and optimization of ballistic transport.

2D transition metal dichalcogenide (TMDC) p-FETs were explored in chapter 4. As a 2D crystal, TMDCs offer the physical limit of channel thickness scaling and pristine surfaces for unparalleled gate control. However TMDC p-FETs have been difficult to achieve, and without it complementary TMDC logic circuits cannot be realized. In this study we used high work function MoO_x as a hole injection layer to MoS_2 and WSe_2, 2 model TMDCs. One of the first MoS_2 p-FETs was demonstrated, and WSe_2 p-FETs with MoO_x contacts exhibited ~10x improved on-current over devices with Pd contacts. Further analysis revealed that MoO_x exhibits a better pinning factor than elemental metals. This observation encourages the future study of other transition metal oxide contacts for TMDCs.

Layer transfer III-V/TMDC heterojunctions were explored in chapter 5. Semiconductor heterojunctions offer an additional degree of freedom in designing the band structure of transistors. However traditionally they are grown by epitaxial techniques, where lattice matching constraints severely limit possible material combinations. By physically transferring one material upon another, we overcame this limitation. The InAs/WSe_2 diodes fabricated demonstrated an ideality factor of 1.1 and forward/reverse current ratio $>10^6$. These results indicate a negligible recombination-generation (R-G) current component, which is reasonable given the small device volume. Furthermore the depletion region, in which R-G events contribute to a current, is almost completely pushed by the highly doped InAs into the near intrinsic WSe_2. Overall, this study enables heterojunctions unachievable by traditional epitaxial techniques, allowing novel physics studies and applications.

References

[1] N. Arora, *MOSFET Modeling For VLSI Simulation: Theory And Practice*; World Scientific: Singapore, 2007.

[2] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature* Vol. 468, 2010, pp. 286-289.

[3] K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C.-H. Liu, Y.-L. Chueh, E. Plis, S. Krishna, H. A. Bechtel, J. Guo, A. Javey. "Quantum Confinement Effects in Nanoscale-Thickness InAs Membranes", Nano Letters, 2011, ASAP, doi: 10.1021/nl2030322.

[4] K. Takei, S. Chuang, H. Fang, R. Kapadia, C.-H. Liu, J. Nah, H. S. Kim, E. Plis, S Krishna, Y.-L. Chueh, and A. Javey, "Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Appl. Phys. Lett.* Vol. 99, 2011, pp. 103507-1–1035073.