Room temperature approach to fully transparent, all-oxide thin-film transistors

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Low temperature approach to fully transparent, all-oxide, flexible ZnO transistors

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Research Project

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Chapter 1 – Introduction and Motivation

The exploration and understanding of electronic material properties and how they can be implemented into a usable form for electronics is the driving force behind developing new types of devices and electronic systems. Within these new types of electronic systems, transparent and flexible electronics represent two emerging fields that have gathered much attention.[1,2] For example, transparent electronics have applications in the area of fully transparent displays. While there are separate research efforts on the development of light-emitting materials needed for displays,[3] there is still a need to develop the underlying electronics to make the system entirely transparent—namely, the pixel-driving transistors and the digital circuits needed for pixel addressing and additional logic. Development of the latter, digital logic circuits, can lead to large scale logic and digital processors that can be integrated into almost any transparent electronic system and maintain full transparency. In the realm of flexible electronics, the focus is on the ability to integrate electronics into existing flexible systems. The application area for this technology quite diverse, ranging from conformal coverage of contoured shapes, such as prosthetic hands, to wearable or implantable health monitoring sensors.[4–7] In order to realize these types of devices, effort must be put into developing mechanically robust electronic materials whose device performance is immune to bending and stretching. Additionally, any fabrication steps involving the flexible substrate material need to be done at a temperature low enough to not damage the substrate, which greatly limits the deposition temperatures for polymer-based substrates. Alternatively, devices can be

fabricated on a rigid substrate then mechanically transferred to a flexible substrate to avoid temperature incompatibility. While each of these areas currently has their own areas of utilization, integrating these two areas of transparent and flexible electronics will lead to even more applications that were previously unable to be realized by the two areas alone. Unfortunately, many of these complex systems cannot be realized without one of the basic building blocks—in this case, the thin-film transistor (TFT).

Original development of the TFT was achieved over thirty years ago using silicon.[8,9] Due to its understood electrical characteristics, deposition, and fabrication processes, silicon-based TFTs using amorphous silicon and polysilicon were first demonstrated.[8,9] However, as our discovery and understanding of new material systems and deposition methods have progressed, the development of TFTs has grown to include alternative thin-film materials, each with their tradeoffs amongst the other material systems. The most widely explored TFT materials after silicon include organic semiconductors and carbon nanotubes (CNTs). Tremendous effort has been put into these material systems, enabling the realization of large-scale flexible circuits for display and sensor applications.[8–15] Organic semiconductors are excellent TFT candidates due to their inherent mechanical flexibility and low deposition temperature.[11,12] Unfortunately, these organic semiconductors are usually extremely air-sensitive, causing rapid device performance degradation.[11] However, organic semiconductors continually prove to be a viable TFT system as advancements have been made in device air stability.[16] CNTs are also an excellent TFT material platform due to their mechanical flexibility, low deposition temperature, and high mobility.[13–15]

While CNTs exhibit excellent scaling properties towards large digital circuits in the form of nanotube growth and solution drop-casting,[13,14] these devices are entirely p-type. While much effort has been put into type conversion in CNT systems,[17,18] there is still no reliable method creating n-type CNT devices, and thus CMOS logic, on a large scale. However, despite the challenges in type conversion, CNTs have proven to be an extremely promising material for future digital circuit applications. Additionally, both organic semiconductors and CNTs can be readily dispersed into solutions, which shows promise for ink-jet and roll-to-roll printing of electronic systems.[19–21]

More recently, research efforts have increased in the TFT material of semiconducting metal oxides. The family of semiconducting post-transition metal oxides (ZnO, In_2O_3, InZnO, InGaZnO, etc.) offers an additional platform with wide energy band gaps for optical transparency over the full visible range, room temperature deposition (both solution-based and physical vapor deposition techniques) for plastic compatibility, and electrical properties suitable for TFTs for transparent, flexible, and bio-related applications.[7,22–25] However, many existing fabrication techniques for these oxide TFTs, while they are being deposited at room temperature, require higher temperature annealing steps to prime the oxide (i.e., improve crystallinity, improve stoichiometry, or calcination of solutions) for TFT use or to improve the device performance to an acceptable level.[25–29] Unfortunately, the use of higher temperatures for processing and device improvement can severely limit substrate compatibility and present challenges for integration with other components.

In order to retain a wide range of substrate choices without sacrificing device performance, a low temperature approach to fabrication is needed. In this work, we demonstrate fully transparent all-oxide based ZnO TFTs with low operation voltages fabricated using a room temperature plasma deposition method with no post-processing annealing and a maximum device processing temperature of 110 ºC.

Chapter 2 – Experimental Results

As previously stated, this work consists of transparent all-oxide based ZnO TFTs fabricated on flexible substrates using a room temperature plasma deposition method. With the fabrication techniques and deposition process presented in this report, we seek to propose a new method for low temperature fabrication of flexible oxide-based devices and reaffirm that ZnO is a viable metal oxide material to use for future transparent and flexible electronic systems.

2.1 – Fabrication Process and Cathodic Arc Deposition

The schematic process flow for the fabrication of top-gated ZnO TFTs is shown in Fig. 1a. ZnO TFTs are fabricated on three different substrates: i) a reference silicon wafer substrate with a 50 nm thick thermal oxide (Fig. 1b), ii) transparent alkali-free borosilicate glass (Fig. 1c), iii) flexible polyimide foil (Fig. 1d).

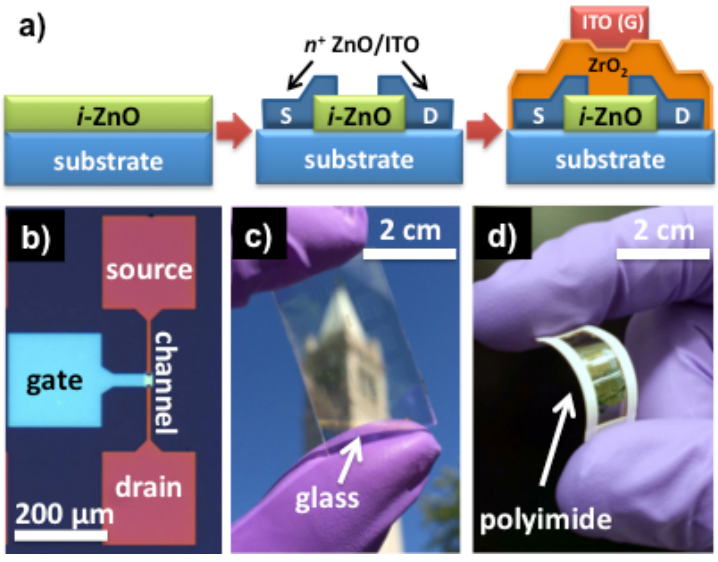

Fig. 1: Process Flow and Images of Devices (a) Process schematics of ZnO TFT fabrication. (b) Optical microscope image of finished device on silicon. (c)

Photograph of finished device array on glass slide. (d) Photograph of finished devices on freestanding polyimide foil bent between fingers.

Substrates are cleaned with acetone and isopropyl alcohol and blown dry with nitrogen. Substrates are then loaded into a cathodic arc vacuum deposition chamber and pumped down to ~5×10^{-6} Torr for ZnO deposition. The filtered cathodic arc deposition for zinc oxide has originally been developed for the deposition of transparent conducing oxide films.[30] It has been shown that this deposition technology is similar to pulsed laser deposition (PLD) as it produced a flux of energetic ions. The typical Zn ion energy is 36 eV[31] which leads to atomic scale heat right at the film growth region without imposing a large heat load to the substrate. Additionally, in contrast to magnetron sputtering, negative oxygen ions are not accelerated to very high energies of several 100 eV because the arc operates at low arc voltage (the potential difference between anode and cathode is less than 40 V).

The arc deposition system can be described as follows. Cathodic arc deposition (Fig. 2a) uses a relatively low DC voltage to trigger and sustain a metal arc plasma, where the discharge current of about 100 A is concentrated in non-stationary cathode spots.[32] In contrast to the former work on AZO, here we use a pure (undoped) zinc (99.99%) cathode. It is surrounded by an annular grounded anode body. A permanent ring magnet is placed at the bottom part of the cathode cone: its purpose is to steer the moving arc spots around the cathode, enabling efficient material use and spreading of the heat load on the cathode. The zinc plasma generated at cathode spots streams

away from the cathode into the macroparticle filter coil. The purpose of the coil is to guide the plasma to the substrate, which is not in line-of-sight with the cathode. In doing so, the plasma particles (electrons and ions) are separated from the microscopic but relatively massive zinc droplets, also known as "macroparticles." The coil is made of hollow, water-cooled copper tubing. It operates at a constant current of 400 A, producing a magnetic field of the order of 100 mT (more about plasma guiding and macroparticle removal can be found in Ref. 32. Zn ions react with oxygen to form a ZnO film on the near-room-temperature substrate surface. 30 nm of ZnO is deposited as the active TFT channel material onto the substrates placed 12.5 cm away from the exit of the plasma macroparticle filter coil in a 5 mTorr O_2/Ar ambient (O_2 60 sccm, Ar 20 sccm unless otherwise stated).

Photolithography is used to define patterns for the source and drain electrodes via lift-off. Source and drain pads consist of 40 nm thick degenerately doped ZnO deposited at lower O_2 partial pressure partial pressure than the TFT channel ZnO (5 mTorr, O_2 20 sccm, Ar 20 sccm, room temperature), followed by 30 nm of indium tin oxide (ITO) sputtered in a 7 mTorr Ar ambient also at room temperature. A second photolithography step is performed to define the ZnO channel region of the transistors by etching in hydrochloric acid (HCl 1% for 1 s). In this process, the top ITO film on the source and drain serves as an etch stop barrier for the underlying ZnO, as the etch rate for ITO in HCl is much lower than that of ZnO.[33] A 20 nm thick ZrO_2 top gate oxide is deposited by atomic layer deposition (ALD) at a maximum temperature of 110 ºC, and subsequently patterned by photolithography. The same ITO sputtering

and lift-off process is then used to define the top gate contact. Fig. 1b, c, and d show optical images of the devices completed on silicon, alkali-free glass, and free-standing polyimide foils, respectively.

2.2 – ZnO Film Characterization

We first explore the material properties of ZnO thin films deposited by cathodic arc. X-ray diffraction spectra (XRD) of the ZnO films as function of O_2 flow rate are shown in Fig. 2b. All films exhibit a polycrystalline hexagonal wurtzite structure and {0002} texture in agreement with literature.[34] The c-axis lattice constant extracted from the 0002 peak at 34.8° is 5.2 Å in good agreement with values for sputtered ZnO films.[35] No peaks corresponding to metallic Zn inclusions are detected. Estimating the grain size from the 0002 peak positions 2Θ and full-with half-max widths β using the Scherrer equation, $D(2\Theta) = K\cdot\lambda/\beta\cdot\cos 2\Theta$, assuming a crystallite shape factor $K = 0.9$ and substituting $\lambda = 0.154$ nm for Cu Kα radiation, yield grain sizes between ~17-23 nm.[36]

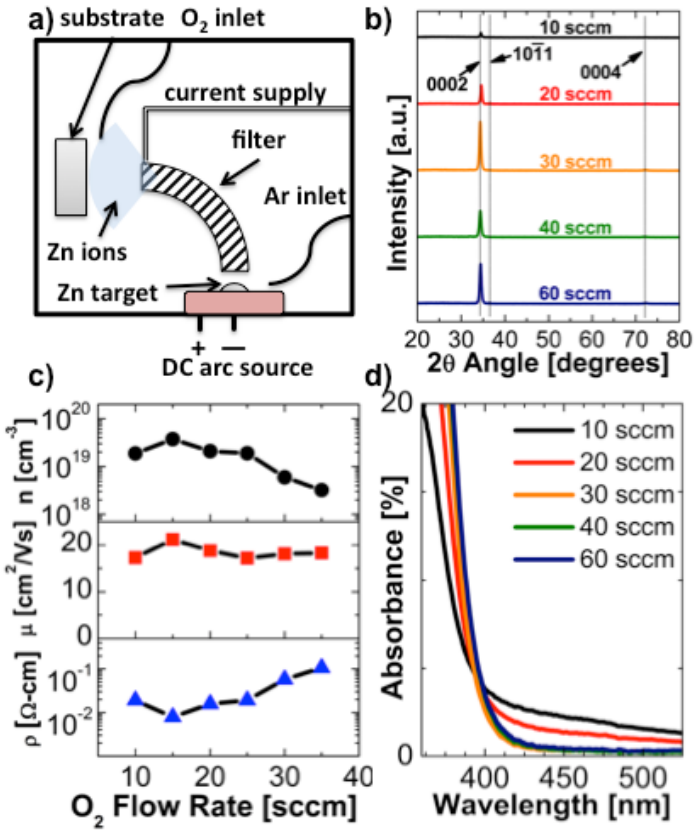

Fig. 2: Cathodic Arc Setup and ZnO Film Characterization (a) Schematic of cathodic arc deposition chamber. The permanent magnet is denoted in red. (b) XRD pattern for ZnO film and varying O_2 flow rates. (c) Electron concentration (n), Hall mobility (μ), and resistivity (ρ) as a function of O_2 flow rate. (d) Dependence of optical absorption with O_2 flow rate.

For transistor application, it is important to precisely control the conductivity of the ZnO channel to enable gate control. The carrier concentration in the ZnO film can be tuned by adjusting the O_2 flow rate during deposition as the carrier concentration of intrinsic ZnO films directly correlates with the number of oxygen vacancies.[34,37] We choose to keep the Ar flow rate and the total deposition pressure constant (20 sccm and 5 mTorr, respectively) and vary the O_2 flow rate from 10 sccm to 35 sccm

to modulate the electron concentration in the ZnO. As the O_2 flow rate is increased from 15 sccm to 35 sccm, the electron concentration drops from the mid 10^{19} cm^{-3} to the low 10^{18} cm^{-3} (Fig. 2c), while the Hall mobility (second panel in Fig. 2c) essentially remains constant between 17.3-21.2 $cm^2V^{-1}s^{-1}$, with the highest recorded mobility of 21.1 $cm^2V^{-1}s^{-1}$ being deposited at an O_2 flow rate of 15 sccm. For the higher O_2 flow rates above 35 sccm, the resistivity of the films (third panel in Fig. 2c) increases too rapidly, rendering Hall mobility determination unreliable. However, the ZnO mobilities reported here appear to be some of the highest Hall mobilities reported for room-temperature-deposited thin film oxides for TFTs reported in literature, showing that cathodic arc deposition is reliable for producing high quality ZnO films.[7,23–25,38,39]

Fig. 2d shows the optical absorption of the ZnO films as a function of wavelength and O_2 flow rate. As the O_2 flow rate increases from 10 to 30 sccm, the sub bandgap absorption at wavelengths longer than 400 nm caused by metallic Zn clusters embedded in the film decreases significantly and the films become more transparent. The absorbance of 30 nm ZnO films in this spectral range drops below 2%. In parallel, the absorption edge at wavelength shorter than 400 nm shifts longer wavelengths for increasing O_2 flow rates due to a reduction of the Burstein-Moss shift with decreasing electron concentration consistent with our Hall measurement results. Absorbance data at 60 sccm O_2, which is the O_2 flow rate used for the ZnO TFT channel, is practically identical to the data at 40 sccm although film resistivity further increases.

2.3 – TFT Performance

We now focus on ZnO TFT device performance. The TFT device architecture implemented is a top gate structure consisting entirely of transparent oxides. We fabricated the all-oxide fully transparent devices on alkali-free glass substrates. Fig. 3a shows the I_{DS}-V_{GS} transfer curve of a TFT device on alkali-free glass with channel width and length of 100 μm, operated at V_{GS} = ±3 V and V_{DS} = 3 V, resulting in an on/off current ratio of ~10^5. The subthreshold slope (SS) is calculated from a linear fit (dotted line) to be SS = 204 mV/dec. The threshold voltage of V_t = 0.36 V was extracted from a linear fit of $I_{DS}^{1/2}$ vs. V_{GS}. The saturation mobility was determined to be μ_{sat} = 4.5 $cm^2V^{-1}s^{-1}$, calculated using the peak value of the slope of the $I_{DS}^{1/2}$ vs. V_{GS} plot under V_{DS} = 3 V saturation operation, assuming a relative permittivity (ε_r) of our ALD ZrO_2 of ε_r = 12. Fig. 3b shows the I_{DS}-V_{DS} characteristic of the device, exhibiting typical square-law behavior and reaching an on-current of almost 40 nA/μm. These values compare well with the best reported oxide low temperature TFTs in literature with SS typically in the range of one hundred to a few hundreds of mV/dec and V_t less than 1 V.[29,40–45]

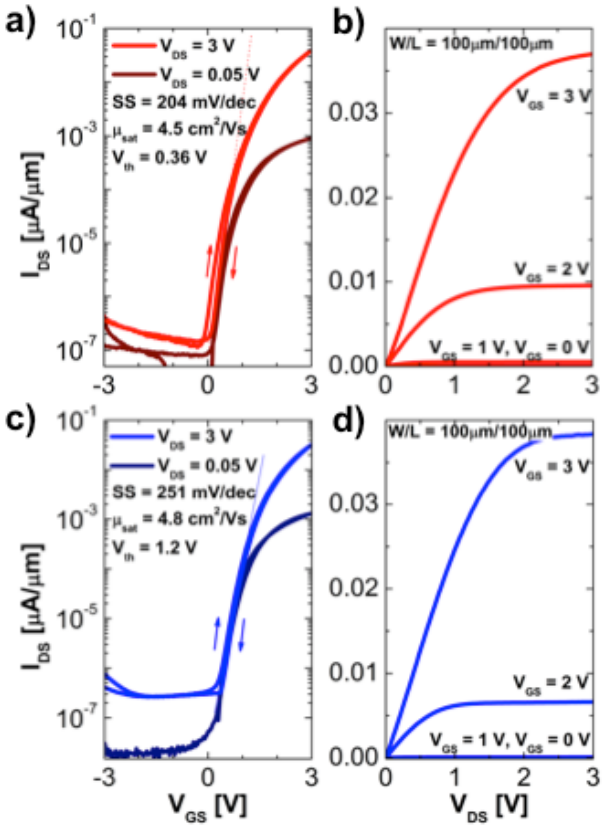

Fig. 3: TFT Performance I_{DS}-V_{GS} and I_{DS}-V_{GS} curves for W/L = 100 μm/100 μm device on (a, b) alkali-free glass and (c, d) polyimide. The arrows on the transfer curves indicate the direction of the double sweep measurement.

It should be noted that alkali-free glass is chosen due to impurities in other glasses, such as microscopy slides. We found that charged ions in the glass were causing a threshold voltage shift of our devices, so alkali-free glass was used to avoid this issue. Additionally, the off-current of our devices is comparable to those reported in literature, showing that the room-temperature process is able to produce devices with just as low of an off-current as compared to those with higher temperature processes. In terms of the saturation mobility, our lower values as compared to literature can be associated with interface states between the ZrO_2 gate oxide and ZnO channel overlap

capacitances between the gate and source/drain, which would cause some of the applied gate field to contribute to state filling and source/drain charges rather than channel inversion, as well as contact resistance effects. These effects can be combatted by annealing or plasma treatments for the oxide interfaces and improved alignment during fabrication for the overlap capacitances. Again, seeing that we are avoiding any higher temperature or post-annealing to improve the gate-channel interface, our future work will look into plasma treatment to enhance the ZrO_2-ZnO interface.

The process was then ported to flexible polyimide foils. Polyimide resin was spun on a temporary silicon handling wafer and cured at 300˚C for an hour before device fabrication. Fig. 3c shows the I_{DS}-V_{GS} transfer curve of the ZnO TFT on polyimide with channel width and length of 100 μm operated at $V_{GS} = \pm 3$ V, exhibiting an on/off current ratio of almost 10^5, with extracted subthreshold slope, threshold voltage, and saturation mobility of SS = 251 mV/dec, V_t = 1.2 V, and μ_{sat} = 4.8 $cm^2V^{-1}s^{-1}$, respectively. Fig. 3d shows the I_{DS}-V_{DS} curves indicating expected square-law behavior with an on-current of again almost 40 nA/μm, thus reaching identical performance characteristics to the device on glass and with those reported in literature.

For each of the I_{DS}-V_{GS} curves on the two substrates, the increase in off-current at low V_{GS} operation can be attributed to gate leakage resulting from both the thin 20 nm gate oxide and the source/drain to gate overlap. The value of the subthreshold slope

can also be restricted by trap states in the channel-oxide interface and series resistance effects from our ITO contacts to our ZnO channel. In this study, we choose to avoid higher temperature annealing steps to potentially reduce these effects, and the result is still acceptable TFT performance. The on/off ratio is 10^5, whereas other studies report ratios as high as 10^8.[40,41] This is because the devices are being operated at high operation voltages (V_{GS} and V_{DS} $\geq$10 V). While this on/off ratio is beneficial for display applications, our focus is on scalable TFTs for digital circuits, which would focus more on decreasing power consumption, requiring low voltage operation. Overall, the devices made on glass and polyimide show consistent, transferrable and reproducible behavior, suggesting this method to be a universally applicable technique for creating fully-transparent ZnO TFTs on a variety of substrates. Table I summarizes our results for the ZnO TFT on polyimide and compares this device to other high-performance oxide TFTs reported in literature.

Material	ZnO*	IGZO[40]	IGZO[41]	IGZO[42]
Dep. Method	CAD	sputtering	sol-gel	sputtering
On/off ratio	10^5	$<10^7$	10^8	$<10^8$
V_{op} [V]	±3 V	±20 V	±10 V	±3 V
SS [mV/dec]	251	200	95.8	60
V_t [V]	1.2	2	2.7	0.5
μ_{sat} [cm^2/Vs]	3.1	11	<10.5	10
W/L	100/100	400/100	100/10	1000/5
Max T [˚C]	110	RT	150	325
Transparent?	yes	yes	no	no
Flexible?	yes	no	yes	no

Material	ZnO*	ZnO[29]	ZnO[43]	ZnO[44]	ZnO[45]
Dep. Method	CAD	PLD	sol-gel	sputtering	solution
On/off ratio	10^5	$>10^4$	10^4	$>10^4$	$>10^4$
V_{op} [V]	±3 V	-1 – 4 V	0 V – 3V	±1.5 V	-1 V – 3 V
SS [mV/dec]	251	250	≈300 (est.)	180	250
V_t [V]	1.2	2	0.7 V	0.1	0.1
μ_{sat} [cm^2/Vs]	3.1	0.024	3.4	0.45	22.1
W/L	100/100	2000/50	1500/100	500/50	N/A
Max T [ºC]	110	200	280	200	150
Transparent?	yes	yes	no	no	no
Flexible?	yes	no	yes	yes	no

Table I Comparison of this work to previous oxide TFTs. The upper portion compares this work to existing IGZO devices, and the lower portion compares this work to existing ZnO devices. V_{op} and W/L denote the operation voltage and size of the published device, respectively. Max T refers to the maximum temperature used during device processing, excluding substrate preparations. V_{op} refers to the gate

voltage range in which the device was reported, with the accompanying V_{DS} voltage being the highest of the reported V_{op} value. It should be noted that transparency is defined as all components of the transistor, including the gate and source/drain contacts, and the substrate altogether be transparent.

2.4 – TFT Bending

With the focus of these TFTs being on applications in flexible electronics, bending studies are performed to get an idea of the mechanical robustness and its effect on the electrical performance of the device. To remove the polyimide from the handle wafer, the polyimide was cut around the edges and then submerged into DI water for twenty minutes. Putting the sample in water promotes self-delamination of the polymer from the substrate. This process prevents the polyimide from needing to be manually peeled off, which induces strain on the polymer, potentially cracking the fabricated devices. Once the polyimide has delaminated, the polyimide foil is laid flat, and the devices are measured to quantify possible effects from internal strain relaxation during delamination. Bending tests are then performed by wrapping the polyimide around a test tube with r = 8 mm and measuring the device performance while bent.

Fig. 4 shows the I_{DS}-V_{GS} and I_{DS}-V_{DS} curves for the W/L = 200 μm/25 μm device before peeling off the handle wafer, after peeling off but before bending, and while bent. This device geometry is chosen for its higher output current values.

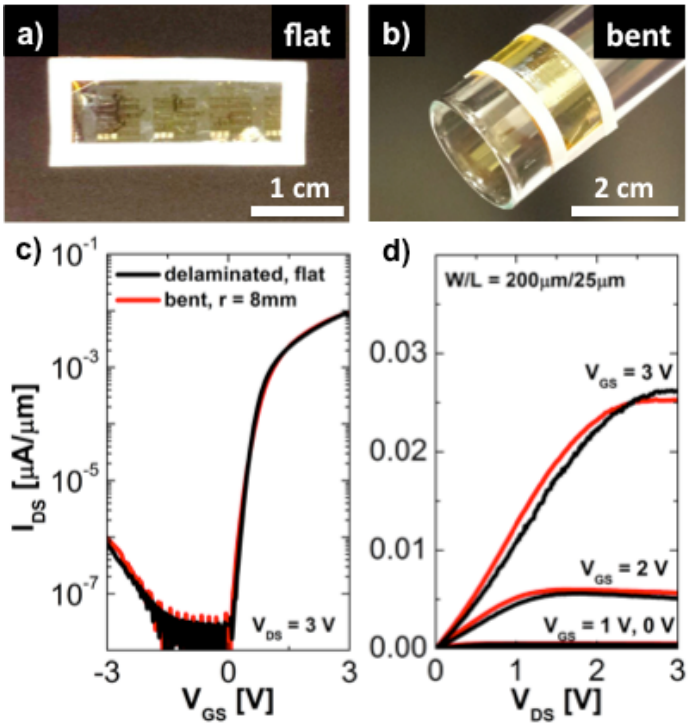

Fig. 4: Flexible TFT Bending Tests Images of the substrate while (a) flat and (b) bent around a test tube with r = 8 mm. (c) I_{DS}-V_{GS} and (d) I_{DS}-V_{DS} curves for a device on free-standing polyimide with W/L = 200 µm/25 µm while flat (black) and bent at r = 8 mm (red).

The on-current of the device drops almost one order of magnitude, which may be attributed to defects created in the device during strain relaxation of the polyimide film upon delamination. However, while bent at r = 8 mm, there seems to be minimal change in device performance, proving that our ZnO TFT process is not only universally applicable to various substrates but also mechanically robust for flexible electronics.

2.5 – NMOS Inverter

Furthermore, to demonstrate the applicability of this process to integrated logic systems, we have fabricated an inverter gate. Due to these devices being solely NMOS, the inverter was constructed with a depletion-mode transistor load rather than a PMOS device or resistor. Henceforth, the transistor in which the input (V_{IN}) is passed is referred to as the "switching transistor," whearas the depletion-mode transistor, whose gate terminal is connected to the inverter output node (V_{OUT}), is referred to as the "load transistor." The switching voltage of the inverter only depends on the V_t of the switching transistor since the load transistor is acting as the resistive load, so the supply voltage to the inverter (V_{DD}) was chosen to maximize the inverter noise margin. At an input voltage of $V_{IN} = 0$ V, the switching transistor is off and has a much greater resistance than the load transistor. Thus, V_{OUT} tends toward V_{DD}, logic 1. Upon the onset of inversion, the switching transistor changes from the off-state to the on-state. As the switching transistor turns on, the resistance of the switching transistor becomes comparable to and then much less than that of the load transistor, causing V_{OUT} to be pulled to ground, logic 0. Fig. 5 shows the transfer characteristics of the inverter at $V_{DD} = 2$ V as well as an optical image and circuit schematic of the device. The contact pads have been labeled for convenience.

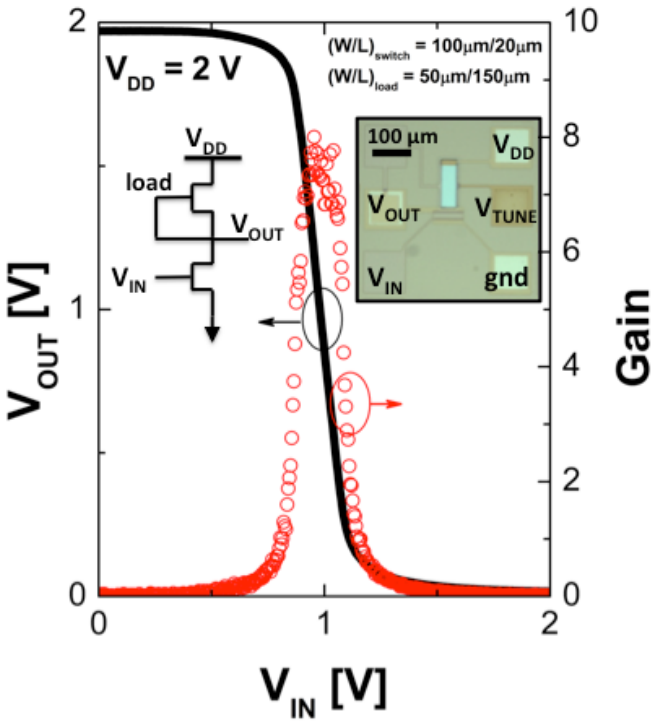

Fig. 5: NMOS Inverter Characteristics Voltage transfer curve (V_{OUT} vs. V_{IN}) and dc gain ($|\partial V_{OUT}/\partial V_{IN}|$) of the all-oxide NMOS inverter on polyimide under an operation voltage V_{DD} = 2 V. The switching transistor has a W/L = 100 μm/20 μm, and the depletion-mode load transistor has a W/L = 50 μm/150 μm. Inset is a schematic representing the device layout as well as the corresponding optical image of the device with labeled contacts.

It should be noted that the V_{TUNE} pad is available for V_t tuning of the load transistor but was not needed and therefore unused in this device. Also plotted is the dc gain of the inverter, defined as $|\partial V_{OUT}/\partial V_{IN}|$, which is shown to be ~8. Additionally, the noise margins of the inverter were extracted from the transfer curve by taking the maximum low input voltage (V_{LI}) and the minimum high input voltage (V_{HI}), corresponding to the input voltages at unity gain, and the corresponding output values of those inputs,

V_{HO} and V_{LO}, respectively. The high and low input noise margins are then defined as $NM_H = V_{HO} - V_{HI}$ and $NM_L = V_{LO} - V_{LI}$, respectively. The noise margin values were calculated as $NM_H = 0.36V_{DD}$ and $NM_L = 0.33V_{DD}$.

Chapter 3 – Conclusion and Future Work

In conclusion, we have implemented a cathodic arc deposition technique for room temperature deposition of intrinsic ZnO with electrical and optical quality suitable for transparent transistor applications. Additionally, we have shown this method of ZnO deposition to be usable in the fabrication of all-oxide fully transparent transistors on alkalki-free glass and polyimide with comparable or better electrical performance to alternative TFT platforms and existing oxide TFTs. We performed bending studies to show the mechanical robustness of our device structure to confirm its potential use on flexible substrates. Overall, we have demonstrated a low temperature fabrication process for ZnO TFTs enabling use in both fully transparent and flexible electronic applications.

In future work, we plan to port our process to other flexible plastics, such as PET or PEN. In doing so, we plan to improve device performance by creating better channel-oxide interfaces and decrease series resistance issues, which will help with the gate control of the device and boost device mobility and on/off ratio. Additionally, lower temperature gate oxides via ALD or solution processing will be explored to lower the processing temperature to its lowest limit of 90 ºC, as determined by photolithography. Our group has been noted for its development of an e-skin platform based on carbon nanotubes[5,6,14], which requires uniform TFTs for pixel backplane addressing as well as large-scale digital circuits for on-chip pixel addressing and simple data manipulation. We plan to continue developing our new ZnO platform for

future e-skin applications as an emerging flexible, large-scale circuit systems for backplanes and circuits on various flexible substrates.

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