Transistor circuits for MEMS based transceiver

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Final Report

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I. Project Description

In recent years, the push for low power wireless sensor networks has called for the introduction of RF-MEMS transceiver devices capable of operating on scavenged power. The design of ultra-low power MEMS based transceivers stands to revolutionize the fields of industrial monitoring, environmental monitoring, and biomedical imaging.

This report demonstrates a MEMS based transceiver capable of supporting these low power applications. Included are design and simulation results using transistor circuits implemented with a commercial TSMC 180nm technology. The entire system is estimated to consume 57.8uW of power at a Vdd=1.8V, duty cycled at 50%. The transceiver system implements a modified OOK modulation scheme and utilizes a MEMS resonator, an oscillator, an envelope detector, a comparator, a power amplifier, and an output buffer. The system is currently optimized for data rates of 5kHz, but can easily support much higher data rates. This design demonstrates operation at 60MHz VHF, but the tunable nature of the MEMS device allows for use of frequencies up to UHF.

The remainder of this report is organized as follows. Section II explains the current state of the industry that the transceiver is to be commercialized in. This section also uses that information to propose a viable go-to-market strategy for a startup seeking to commercialize this technology. Section III presents a detailed description of my individual contributions toward the capstone project. Section IV is a consolidated paper with brief descriptions of the performance of each individual block in the transceiver architecture. It also includes simulation results showing the performance of the transceiver as a whole after all individual work was integrated together. Section V finishes with concluding reflections on the progress of the capstone project and potential directions for future work.

II. Industry Analysis and Proposed Market Strategy

This paper provides a detailed industry analysis of our MEMS transceiver chip by first comparing against other competing technologies already present in the market and then proposing a viable go-to-market strategy with our technology. The biggest competitors to our MEMS-based wireless transceiver technology are WiFi, Zigbee, and Bluetooth. Therefore, we begin by proving our transceiver technology as a viable competitor against these existing technologies due to lower cost and lower power consumption. Despite this fact, our analysis of the wireless semiconductor industry using Porter's five forces will show that barriers to entry into this industry are extremely high. We identify an alternate strategy to bring our technology to market; we plan to vertically integrate our technology into an electrical sensing system for agriculture. We will show that we can not only exploit the weak forces in the agricultural sensing systems market, we can also capture most of the value chain by having exclusive access to our MEMS technology. By entering the agricultural sensing market, our strategy is to dominate the market by being both a chip designer and a systems manufacturer.

The objective of our capstone team is to build a fully-functional low power transceiver chip that successfully integrates a microelectromechanical system (MEMS) resonator. We accomplish this by creating a strict power budget of 60 micro watts for the entire system and using block-level design methodology to implement the CMOS transistors in the transceiver chain. We conduct this process in three steps. First, we create a schematic of our transceiver circuit and verify its functionality in simulation. Next, we implement the layout that corresponds to our schematic by designating the locations of connections, wires, doped wells, and metal layers. Finally, once the chip has been fabricated, we need to use PCB boards to conduct the final tests needed to verify its operation. These steps will allow us to achieve a low-power MEMS transceiver chip that is ready for commercial use at the end of the year.

Before discussing about specific competing technologies to MEMS, it is important to appreciate the context of how transceivers operate and what are some design metrics for a good transceiver. This paper will first distinguish the power advantages of our MEMS transceiver chip from other conventional transceivers. We will then show why these advantages are relevant by illustrating the need for minimizing power use in today's transceiver applications.

Transceivers allow for wireless communications by transmitting and receiving wireless signals. To avoid interference, signals traveling in the air must travel in different frequency channels. This often requires them to be converted into higher frequencies in a process called modulation. When the signal then reaches its destination, the receiver then needs to recover the original signal from the modulated signal in a process called demodulation. It is the job of the transceiver to modulate and demodulate signals being sent and received; it does this by using a resonator to generate a reference frequency that is tuned to the desired sending or receiving frequency of the signal.

When designing a transceiver chain, the most difficult problem is isolating the desired signal from other unwanted signals that are received from the antenna. Engineers define the Q factor of a resonator as its ability to resonate at a specific frequency. Resonators with a low Q factor are less selective; they resonate not only at the tuned frequency, but also at other nearby frequencies. For smaller channels, the Q of the resonator needs to be high in order to minimize insertion loss, or loss of signal strength (Nguyen, 2013, p. 112). Most conventional transceivers implement resonators that need additional filtering to isolate the signal. This costs power. Although we would like to fit many channels into our band, smaller channel bandwidths require stronger filtering and consume more power.

Herein lies the advantage of MEMS technology. Mechanical resonators generate larger Q factors than purely electrical resonators. MEMS resonators provide record on-chip Q factors operating at gigahertz frequencies while still maintaining excellent thermal and aging stability (Nguyen, 2013, p. 110). In particular, the capacitive-gap RF MEMS resonator that we use for

our MEMS transceiver circuit produces exceptionally high Q around 100,000 and can be tuned to select 1kHz-wide channels over a 80kHz range (Rocheleau, Naing, Nilchi, & Nguyen, 2014, p. 83). The high Q factors of MEMS resonators eliminates any steps involving additional filtering and takes away the power consumption overhead required for reducing insertion loss from the resonator. Eliminating the filtering step also results in a simpler design for the system as a whole.

Next, this paper provides examples of applications using our low-power MEMS-based transceiver to show its relevance in the market today. The main interests of our technology will come from wireless sensor node markets, where low power and simplicity are much more important than data transmission rate (Rocheleau, Naing, Nilchi, & Nguyen, 2014, p. 83). Since the wireless sensor market is wide and diverse, this paper uses body area network (BAN) sensors and environmental sensor networks (ESNs) as case studies to illustrate the needs for simple, low-power transceivers.

BAN sensors are used to collect information directly from the person's body. Designers integrate BAN sensors into smart textiles to detect the wearer's heart rate, stress, motion, and energy expenditure (Peiris, 2013, p. 1). A transceiver chip will then enable the sensors to send this physiological information to an interface where either the person or a medical professional can view it and form educated decisions. The biggest challenge with these devices is miniaturizing the BAN node and keeping it low power while maintaining a broad range of applications. A full on-chip application-specific implementation for BAN has already been designed using the wireless protocol Zigbee and consumes approximately 4mW of power when transmitting and receiving. A tiny lithium coin-cell battery can easily provide enough power for this radio. Although current implementations of BAN are functional, an approach to combine MEMS technology with ICs has already been discussed as the next step to further miniaturize the features of the BAN project (Peiris, 2013, p. 2). If we decreased power consumption from

the milliwatt range to the microwatt range using MEMS, the battery life will increase by several orders of magnitude.

ESNs are another area where we can employ low-power transceivers. These sensors constantly monitor the natural environment to study how they work and detect natural hazards such as floods and earthquakes. The transceiver allows for communication between the sensors and a Sensor Network Server, where it can be viewed at a base station (Hart, Martinez, 2006, p. 178). The biggest advantage of ESNs is that they allow us to monitor remote or dangerous areas that have long been inaccessible to study (Hart, Martinez, 2006, p. 177). The designer of these sensors needs to satisfy both low power and low maintenance constraints; these will ensure that the system will operate with minimum intervention for sensor maintenance or changing batteries. MEMS technology can provide the low power and simplicity needed for these sensor nodes. An approach to build tiny cubic millimeter sensor nodes called Smart Dust using MEMS technology has already been proposed, although environmental robustness is an additional design constraint for this particular application (Hart, Martinez, 2006, p. 180).

We have shown that some wireless sensor applications such as BANs and ESNs need ultra-low power transceivers. To show that MEMS is a feasible technology, we now require a closer examination of the major competitors in wireless sensor applications. The most recognizable competing technology in wireless communications is WiFi. WiFi is the biggest threat to our technology because of its wide use in applications from cell phones to computers. Because it is supported across many platforms, WiFi is even used extensively for smart wearable and connected medical device applications. Thus, WiFi takes a sizeable chunk of the market that we hope to apply our technology. The cost per WiFi chip is moderately expensive at a bulk price of $3 for 1000 chips (Smith, 2011). Although this cost is slightly inflated, WiFi's biggest strength is that it is the fastest means of wireless communications in the industry. Supporting up to 11 to 54Mbps (megabits per second), WiFi takes a commanding lead over the second fastest wireless method, which is Bluetooth at 1Mbps (Smith, 2011). This means that

WiFi transfers data up to 54 times faster than Bluetooth. Our transceiver can be configured for high data rates but at the expense of additional power consumption. Therefore, to secure a special niche for low power and low cost, our design is not optimized for speed. We operate at speeds of 200kbps, which is much lower than WiFi. However, the relaxed speed constraint allows us to design our transceiver architecture to be much simpler than typical WiFi chips and less costly as a result (Dye, 2001). By using a simple design, our MEMS-based chip is expected to be less costly at about $2.5 for 1000 chips.This is another strength of our MEMS transceiver in addition to the aforementioned low-power advantages from using a high-Q MEMS resonator. Although WiFi is a major competitor in the wireless communications field, low power applications that do not require excessively high data rates should favor our transceiver over WiFi.

Zigbee is another wireless communication method that is less recognizable because it does not directly target the consumer market. However, Zigbee is widely used in some battery powered systems such as home networks, and smart watches that require moderately long distance communications (Lawson, 2014). Zigbee accomplishes long distance travel with intellectual property known as mesh networking. Mesh networking is a method of having all the devices in a given area working together to transmit your information. For example, in city of 100 smart phones spread out evenly, information can be transmitted across the entire region by having phones send information to each other and successively passing data forward one phone at a time until the data reaches its the final destination. This type of networking is analogous to a relay run where runners pass the baton to subsequent runners until the finish line is reached. By utilizing this type of IP, Zigbee is able to serve information across very long distances and therefore commands the market of long distance communications.

Our technology can also achieve long distance travel by using low frequency techniques. High frequency networks that do not use mesh techniques cannot travel far because higher frequency signals have a larger probability of disappearing when coming into contact with

obstructions like buildings. In comparison, lower frequency signals can wrap around obstructions without losing data. Therefore, implementing low frequency signals in our design allows us to compete with Zigbee's long distance travel. A weakness of using Zigbee chips is that they need to always be powered on in order to accurately pass information through. In networks of battery powered cell phones, Zigbee will drain batteries very rapidly. Our transceiver chip easily beats Zigbee in power consumption because our chip does not need to be powered on at all times to achieve long distance travel. Furthermore, as a result of the mesh network design, Zigbee requires complicated circuitry and this makes their bulk price very costly at $3.2 for 1000 chips (Smith, 2011). The clear advantage that Zigbee has is in addition to long range is that their data rates are higher at 500kbps. However, much like the argument against WiFi, our design relaxes the speed constraint for optimizing cost and power consumption. Our chip has the competitive advantage in markets that require low cost, low power chips for long-distance, battery-operated devices that can tolerate producing moderate data rates.

So far, we have discussed Zigbee and WiFi as two major competitors of our technology. These two standards currently dominate the long distance travel market and the wearables market, respectively. Our transceiver chip hopes to steal some of the market share by offering low power alternatives with comparable long distance capability for battery powered devices. However, it should be said that Zigbee and WiFi are not the only two competitors. The wireless communications industry is a saturated field and there are several other standards that dominate some other markets we hope to enter.

The final competing wireless technology discussed in this paper is Bluetooth. Bluetooth is a global wireless technology standard that enables convenient, secure connectivity for an expanding range of devices and services. This is a widely used communication channel for sharing voice, data, music and other information wirelessly between paired devices such as cars, medical devices, computers, and even toothbrushes. Its wide use poses a threat to our MEMS technology. Bluetooth runs at a high frequency carrier of 2.5GHz but is suitable for

sending information only up to a range of 100 meters. As we have discussed in the case of Zigbee, we can configure our system to communicate information over long ranges by choosing to operate at lower frequencies. Furthermore, the cost of Bluetooth is about 2.7$ for 1000 chip-sets and we expect to operate at roughly the same cost due to our simpler design methodology.

In the area of low power, Bluetooth low energy (BTLE), a new version of Bluetooth developed in 2011, could put our technology at great risk. BTLE ranks number one in the market list for lowest energy consumption. Known as Bluetooth smart, this wireless standard extends the use of Bluetooth wireless technology to devices that are powered by small coin cell batteries such watches and toys. BTLE transceivers can allow these devices to runs for years on a small battery. Although BTLE is currently the industry leader in low power transceivers, this technology still operates at power levels in the milliwatt range (Siekkinen, 2012). Our MEMS transceiver is designed to operate with microwatts of power, which will provide a significant power improvement to BTLE at roughly the same cost per chip.

This paper will next identify both primary and potential end-user stakeholders of our project. Our primary stakeholders are our advisors and sponsors. These include Professor Clark Nyugen, his post-doc assistant Tristen Rocheleau, and PhD. student Thura Naing. They have written journal papers on the theory of our MEMS-based wireless transceiver and have built the initial draft circuits that prove the operation of the high-Q MEMS resonator alone. Professor Nyugen, who is the co-director of Berkeley Sensor & Actuator Center (BSAC), is also our primary sponsor for the project. Since our design is still developing, it is possible future designs can operate at higher frequency and data rate. If that is the case, it will draw more attention and interest from different industries. We currently do not have any issue with budgets since BSAC fully sponsors the project. However, collaborating with top companies like Apple and Samsung would be a reasonable choice if we need to look for other sources of budgets in the future.

Since this project is still in progress, we currently have no actual end-users using our transceiver chip. However, we use market analysis to identify potential consumers and applications that require wireless transceivers with low power consumption. Since we have already discussed several case studies of potential applications, this section focuses more on potential consumers. From the consumer's point of view, our low power chip means that consumers would no longer need to replace their battery very often. People using sensors implanted in the human body will find our technology very necessary. Implantable medical electrical devices gradually become feasible as an assisted medical treatment, especially for detecting biological signals that doctors can use to monitor the condition of the patient. These implantable devices need extremely low power to prevent any potential harm to the body. If the device consumes a low enough amount of power, the energy provided to the device can be acquired from the body itself through energy harvesting, allowing the device to operate for an indefinitely long period of time. For this reason, companies specialized in biomedical imaging may also be interested in our product.

Besides applications in the medical field, the market of our product can also be expanded to other broad fields. Wearable electronic devices have recreational, scientific research and even military uses. These devices need low power transceivers because they often cannot be charged frequently or conveniently while in use. For example, in environmental science, it is necessary for scientists to tag the animal to track their migration and living habit. The longevity of the tagging device is important to maximize the time the device is continuously transmitting signals back to the research center without any battery replacement. Moreover, there are some situations that the battery life is critical. For military applications, the wearable device should have a long life to work in any emergency situation, since it would be terrible if the device was running out of power in a critical moment. This simple consumer-focused analysis, together with the application-focused analysis presented at the beginning of this paper, shows a

strong likelihood of a potential market for our technology centered around wireless applications that specifically require low power.

Although market analysis presents many exciting possibilities for our technology, it does not produce a feasible go-to-market strategy for our technology. We have already alluded to abiding by a strategy to vertically integrate ourselves forward into producing an agricultural sensor for end-users. We will conduct a detailed industry analysis using Porter's five forces to justify this decision (Porter, 2008). More specifically, we will compare the barriers to entry between the precision agriculture industry and the semiconductor industry to show the infeasibility of selling our transceiver as a standalone chip in a startup company. In comparison, we discuss how we as a company in the precision agriculture industry will manage the threat of new entrants to ingrain our success in this industry. We will then analyze the other forces in the context of the precision agriculture industry to further show why it is a more appealing alternative to our startup strategy.

To understand how it is possible to vertically integrate, we first introduce the typical value chain for a sensor product. GTQ, a company that produces sensors, identifies five major sectors in this value chain: fabricating the chip inside the sensor, integrating the chip into a sensor, creation of a probe, adding additional electronics to create a measurement system, and adding software to develop the instrument for a specific application (Sensors Value Chain). Companies selling individual, general-purpose sensors like GTQ occupy the first two sectors while instrumentation companies would occupy the other sectors by customizing for a specific application. We envision ourselves as an instrumentation company. However, while a typical environmental sensing company would purchase all of its components, our strategy is to do the same for everything except for the wireless transceiver chip, which is the final product of our capstone project and will be further developed as part of our company's IP.

There are two reasons why we have chosen to vertically integrate forward. The first reason is related to where the value lies in this value chain. The sensor instrument marketed to

the end user costs much more than the general components a company like QTR would sell to instrumentational companies. Two of our competitors in the agricultural sensing industry - ConnectSense and Twine - sells environmental sensors at costs of $149.99 per unit and $214.99 per unit. On the other hand, individual sensors supplied by the circuit board & global electronic parts manufacturing industry average to about 10 USD per module. By choosing to go into instrumentation, we will position ourselves to obtain most of the wealth in this value chain.

The more important reason is that barriers to entry in the industry of circuit manufacturing are very high. IBIS, a provider of industry-based research, describes this industry of selling “widely available general purpose chips” as being dominated by existing major players. IBIS states that “the size of existing participants in the industry means new entrants need to spend more on marketing to establish industry links and gain market presence” (Ulama). In Porter’s words, the incumbents in this industry can access distribution channels that newer entrants cannot (Porter). There is also the issue of brand name; IBIS argues that companies are reluctant to “risk the quality of their own products” by purchasing from startups in this space (Ulama). Furthermore, Porter argues that intense price competition occurs when different companies sell undifferentiated products, which applies in this industry (Porter). The production of semiconductors at reduced costs favors larger companies that have larger “production throughput” and “plant technology” (Ulama). These situations are unfavorable for startups, who would get quickly outscaled and outcompeted in response even if they developed a novel technology that allowed them to temporarily penetrate the market.

In comparison, the barriers to entry in the industry of precision agriculture are less intense. IBIS states that the main issue is finding highly skilled workers who know how to “incorporate several communications protocols, from GPS to Wi-Fi…” (Antayle). However, as electrical engineers who have developed a transceiver chip, we are well-versed in this knowledge and are therefore in a good position to enter the industry. IBIS also states that “almost two-thirds of revenue (is) up for grabs among many small players”, which further

supports why we should enter this particular industry (Antayle). Furthermore, IRIS rates competition as being low in this industry since firms can “compete on the basis of enhanced functionality or widened application” rather than on price alone (Antayle). Therefore, we will not receive much retaliation if we entered this industry as compared to the circuit manufacturing industry.

A key issue to address is how we as incumbents of the precision farming industry will address the threat of new entrants. It is true that the absence of big players in this industry may allure other competitors into this space. However, as was presented in the value chain analysis, most instrumental companies purchase their components rather than manufacture their own. Our company would have exclusive access to MEMS-based transceiver technology, which based on our previous paper on competitive analysis will outcompete existing transceiver technologies in both cost and low power. Herein lies our competitive advantage. IBIS argues that one of the key success factors in this industry, in addition to having the aforementioned highly trained technical labor, is the “protection of intellectual property/copyrighting of output” (Antayle). New entrants that plan on purchasing components will not have access to this technology; therefore, we can inherently build the better sensor instrument just from having better transceiver technology for this application.

This paper will now present the rest of Porter’s five forces solely in the context of the agricultural sensing industry to further strengthen our identification of this as the industry where our technology can flourish. Since this paper has now shifted its focus specifically to the agricultural sensor industry, we begin by briefly introducing the need for sensors in agriculture. We then begin discussing the remainder of Porter’s five forces by presenting an analysis of the rivalry within the industry and how our technology will leverage low power consumption in order to differentiate ourselves and mitigate rivalry. This paper will draw from information previously presented regarding competing technologies – Zigbee, WiFi, and Bluetooth – in order to study our rivals in the context of the technology they apply in their sensors. Additionally, this paper

will identify how our technology, in a market with several competitors, can better serve the consumers in this industry.

There is an immense need for smart connected sensors in the agricultural industry. In 2014, IBM composed a report which stated that 40% of food produced by developed nations is thrown away. The IBM study also found that weather damages and destroys 90% of crops grown by farmers [Gerson 2014]. This statistic is disheartening considering the amount of people on this planet that can benefit from food. On top of that, farmers are dedicating precious natural resources such as water and land to grow the wasted food. Our capstone team believes we can help. Specifically, our project can provide farmers with the sensors and wireless monitoring tools they need to improve crop yield and reduce food waste. Pursuing the sensor and wireless monitoring application can disrupt the agriculture industry and the market is ready for technologies that can gather soil and other weather information. Market researcher BCC expects the environmental sensing and monitoring technology business to grow from $13.2 billion in 2014 to $17.6 billion in 2019 [BCC Research, 2014].

Wireless agricultural sensors gradually play an important role in agriculture. The use of sensors mainly helps to monitor the environment data, including the weather change, soil quality, temperature, and water quality. By collecting these data, farmers can better control the cultivate process and cut costs by reducing the waste of water and chemicals. Sensors can apply to livestock farms as well. Farmers can tag individual animals with sensors to accurately monitor their behavior, health, and body temperature. From the consumer's point of view, we are positioning our MEMS transceiver chip, and thus our sensors, to be a long-lasting system. This feature is very attractive for U.S. farms; since the average farm size today is 441 acres (Agriculture Council of America, 2014) , it is very time-consuming for farmers to manually set sensors on their farmland and then replace batteries at a later time.

In an industry study conducted by IBISWorld, the precision agriculture market is currently fragmented by players that provide farmers with surveying, agriculture construction,

and asset management services [Neville 2014]. In fact, many of the companies are described as distributors, rather than developers, of third-party sensor systems. By entering this market, we will be providing farmers with a unique hardware solution rather than a service. There are very few companies in direct competition with us, and many of the rivals in this emerging market appear to be startup companies. According to Michael Porter's "The Five Competitive Forces That Shape Strategy," the intensity of rivalry among competitors can drive profits down [Porter 2008]. Our industry analysis identifies the agricultural sensor industry as having weak rivalry because most of our competitors are of equal size and power. There are no clear leaders in the market and thus, each rival exerts equal forces that are weak.

To show that most start-ups are still in the development phase, this paper re-identifies two rivals with products in the market – ConnectSense and Twine. The former company offers environmental sensors with batteries that last 3 years at a cost of $149.99 per unit while the latter offers comparable sensors that last 2-3 months and cost $214.99. The battery life of these rival products are lacking when considering their application. In a large farm where several of these sensors are used to monitor the environment, frequent battery changing or charging can become tedious. As discussed earlier in this paper, WiFi is one direct competitor to our transceiver technology. Therefore, it should come as no surprise that both ConnectSense and Twine employ WiFi technology in their units. There are also many systems proposed or in development that take advantage of other competitors such as Zigbee. For example, a Zigbee based agriculture system to monitor soil, temperature, and humidity was described in the Institute for Electrical and Electronics Engineers (IEEE) Journal [Xialei 2010]. However, we had concluded that our transceiver technology enables us to create systems that consume less power than comparable WiFi or Zigbee systems. Taking advantage of our edge, we can position ourselves to offer a longer lasting system to solve an unmet need. Also according to Porter, price competition is likely to occur with rivalry when competitors offer similar products where price is the only differentiating factor. Because our technology allows us to have low power as

the differentiating factor, our capstone team does not expect an impending price war by entering the agricultural industry.

Porter also stated that rivalry can cause a company to specialize and this creates a high exit barrier. The exit barrier for environmental sensors are low because our products have applications in many industries such as home, health, and telecommunications. Therefore, if exiting the agriculture industry becomes our only option, our resources and technology can easily pivot for applications in other markets.

This paper next analyzes the threats from our customers in the context of the industry they operate in. The agriculture market is an industry with low market share concentration. The top four companies in the Agribusiness industry account for less than 10.0% of industry revenue (Neville, 2014). The reason for the low concentration is due to the naturally fragmented feature of this industry, since the farms are never big enough to dominate the market. In the domestic market, about 97% of U.S. farms are operated by families, individuals or family corporations (American Farm Bureau Federation, 2014). The agriculture companies are generally segmented by their locations and their different agricultural products. As a result, the force from our customers are generally weak since there are a large number of companies with similar size.

Next, we present a detailed analysis of the power of our potential suppliers and how we will overcome this force. In addition to our transceiver chip, the final sensor module will consist of various components like humidity, pressure and temperature sensors supplied by the circuit board & global electronic parts manufacturing industry. As stated before, the cost of these components averaged over a 1000 modules is expected to be less than 10 USD per module. These electronic parts/component suppliers don't impose serious switching costs as they can be easily replaced due to their low cost, variety of substitutes, and negligible cycle time [Sensors Value Chain. (2012)]. Therefore, these particular suppliers are weak.

Our transistor level designs of the MEMS transceiver chip itself will need to be fabricated on a wafer before it can be used as a part of a sensor module. Our current supplier of choice for

this chipset is a semiconductor foundry called Taiwan Semiconductor Manufacturing Company Limited (TSMC). Our advisors have chosen TSMC to be our foundry as TSMC offers a variety of product lines on MEMS and is best known for its strength in advanced low-power processes [IHS Technology. 2012]. TSMC also has a production capability of 16,423,625 wafers/year, which is more than all the other major foundries combined [foundry-ranking-capacity-2013-2014]. The production capacity of the foundry clearly defines the time taken by the foundry to fabricate a design. By choosing to work with the leader in production capabilities, we minimize the time we spend waiting for the chip to come back after sending off our design.

We acknowledge that the component and sensor manufacturing industries are less powerful when compared to the chipset fabrication industry due to two main reasons. Firstly, the transceiver is the most vital component in our module, and the fabs are ultimately the ones providing us with the chip. The significance in ensuring the operation of our transceiver is represented by its huge cost. The chipset costs about 60~70 USD per module, which is more than 6 times the cost of components [IBIS World Industry Report, Sarah Kahn - January 2015]. We as chip designers are obligated to work with the best in the industry - namely, TSMC - to mitigate risks of imperfect chips both immediately upon fabrication and during the lifetime of the sensor. Secondly, the choice of supplier for the chipset is evaluated and integrated into the design process right at the beginning of a project, which considerably affects the cost of switching from one supplier to another. The entire design of semiconductors is done with technology files provided by the foundry to dramatically reduce the risk of failed chips during the manufacturing step. As a result, the layout provided by the semiconductor designer to the foundry is a significant representation of sunk costs and engineering efforts. Switching foundries will require redesigning from the very start and translates to wasted time, engineering effort, money, and product quality.

These two reasons identify our supplier as a strong force, which according to Porter endangers our profits in this industry. The best we can do to accommodate this powerful force is

to formulate all of the problems in the early stages of the project and select the best supplier for us in terms of cost and performance. Additionally it is important to understand that, given that the nature of our capstone project is to design a working transceiver chip that would eventually require fabrication, avoiding business deals with the strong chip fabrication industry was not an option for us.

Finally, we will discuss the effect of substitute technologies outside of competing wireless transceiver technologies, which we have already analyzed. For the application of agricultural and agronomical sensors, wireless technology itself may not be necessary. Instead, farmers can choose to use actual wires to transmit data. By contrast with wireless transmission, wire transmission has advantages in speed, reliability and security. Not only does it allow faster and almost lossless data transmission, it also has full control of who and what gets online. It keeps away all unauthorized visitors, therefore securing the confidentiality of the collected data. However, the disadvantages far outweigh the advantages. To build a wire infrastructure, cost is a fundamental barrier. Our target application is not restricted to an office. Instead, it might cover tens or even hundreds of acres of farmland. In this case, the wire cost is tremendous. For instance, prices for copper wires is about $100 per 1000 ft. (Southwire 2015). If we used wires to surround an acre of land, we need about 850 feet which will cost $85 with copper wires. This does not take into account the complications of the actual infrastructure, which will further increase the actual price beyond this estimation. In contrast, the price for semiconductors that constitute our wireless transceivers is steadily decreasing (IBISWorld Business 2015). Therefore, wireless technologies provide a more cost-efficient option than wired technologies.

Based on this analysis, our strongest threats are other wireless solutions. If customers are already using a wireless transceiver like WiFi or Bluetooth, our MEMS-based wireless transceiver is not the only possible low energy alternate. Energy harvesting is another viable options. This technology aims to convert ambient energy (i.e. motion, solar and thermal energy) into electrical energy. The danger of this technology against our position as a energy efficient

solution is that customers may choose to integrate energy harvesting technology to their pre-existing WiFi or Bluetooth transceivers. Since this technology has already been successfully implanted into some watches, the technical barrier to combine energy harvesting and existing wireless transceivers is small. However, their main weakness is still cost. If our customer has no existing agricultural sensors, then our product is definitely cheaper than the combination of a WiFi or Bluetooth based sensor with additional circuitry for energy harvesting. In general, the threat of substitutes for our product as an agricultural sensor is weak.

This paper now concludes by summarizing the points made regarding the viability of our go-to-market strategy and the competitive advantages of our MEMS transceiver technology compared to other existing wireless technologies. We have analyzed the agricultural sensor industry using Porter's five forces to show that, apart from the inevitably strong supplier force, the other forces are weak enough to justify our decision to vertically integrate into this industry. This is a strategy made in contrast to directly entering the semiconductor industry as a startup and handling its high barriers to entry. We have also shown that our simple design architecture for our transceiver results in competitive advantages of low power and low cost for our MEMS-based wireless transceiver relative to the existing technologies WiFi, Zigbee, and Bluetooth. Although advantages exist for using MEMS technology, it has the danger of being overshadowed by these three commonly-used and widely-trusted technologies. Our go-to-market strategy will ensure that our MEMS technology can successfully outcompete in metrics that are very relevant to the agricultural industry (cost and power) without being overshadowed by the brand names of these existing technologies.

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III. Individual Technical Contribution

Section I: Project Statement

Our team's task was to build a transceiver based on a Mems device. The main idea was to build individual blocks that consummate to make a transceiver. The transceiver would eventually be fabricated into a chipset that could be used in various modules for applications like, wireless communication, livestock monitoring, environmental sensors and medical devices etc. These tasks were split equally among all of our team members and called 'design blocks'. Each of these design blocks had a precise functionality and specification to meet. Subdividing the transceiver into blocks was based on individual interests and relevant technical skills needed for the design. Following are the various blocks assigned to each of us by our advisors.

Yuehan Xu	Kelvin Liang	Keli Hui	Darryl Yu	Soumya Mantha
Oscillator	Detector	Comparator	Buffer	Power Amplifier

TABLE1: Division of project

My part of the project was the design of a Power amplifier for the transmitter part of the system. This block was needed to establish connections and send information from the system to the external world. The design involved many considerations with respect to the block itself as well as the interfacing with the external world.

Following this section is section II on the literature review, which emphasizes on the different architectures available in theory and the choice of using a particular architecture for this application. Next is section III, that shows the procedure for construction of this block in detail along with the sizes of components used and their numerical derivations for classes A, D an E power amplifiers .This section also showcases the simulation tests, performs and the results obtained for each of the classes followed by section V with conclusions.

Section II: Literature Review

As emphasized above, my goal in this project is to design and layout and carry out the entire validation of a power amplifier with the given specifications.

Given the fact that reducing the power consumption is the overall goal of this project, the power consumed by individual blocks must also be minimized. This translates to the concept of power efficiency, meaning 'the amount of power used to generate and transmit a decodable burst of data from the system'.

In past architectures and research it is apparent that the Power amplifier is the dominant power-consuming block in the entire transceiver. There are various literature segments and architectures proposed on improving the performance of a power amplifier along with their respective trade-offs.

The major trade off for efficiency is a characteristic called Linearity. Linearity defines 'the relationship between the output and the input, and the change in output for a given change in the input level'. As we increase the input signal level, the output stops following the input after a particular value of input is reached, and this point decides if the block can be used for particular applications. As we move towards systems that are highly efficient, we need to give up on linearity in most of the prevailing architectures.

However, there are a few architectures that switch between two different Power amplifiers –one with good linearity and the other offering good efficiency. Depending on the requirement for a particular mode, the efficient or linear amplifier is picked.

Based on the performance and particular ways in which its input is controlled, this general Power Amplifiers are sectioned into different classes –A, B, AB, C, D, E and F.

Below is a table of the performance statistics of each of the above classes.

CLASS	A	B	AB	C	D	E
Theoretical efficiency	50%	78.5%	60%	80%	100%	100%
Linearity	Linear	Non-linear	Linear	Non-linear	Non-linear	Non-linear

TABLE2: Power Amplifier Class Trade-off

DESIGN 1 : CLASS D

Since efficiency is our major consideration in this system, I chose to build the Amplifier in a class D configuration. This choice was made after surveying highly efficient PA's in papers written by N.O.Sokal [Nathan.O.Sokal(1981)] and Prof. Ali Niknejad . The other requirements needed for proper operation of the block like current bias generation, voltage bias at the input, inclusion of passives like inductors, capacitors and resistors etc. need to be taken into consideration.

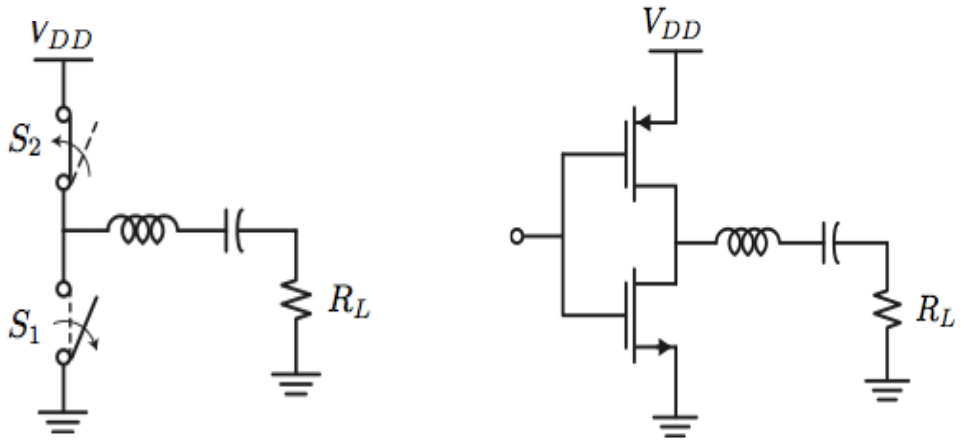

Fig1: Class D Amplifier models [Ali.M.Niknejad (2014)]

From the above table, class D and class E amplifiers can be theoretically characterized as having an efficiency of 100%[Ali.M.Niknejad (2014)], this is because they don't allow for any

dissipation of energy within the system, thus translating all of its energy to the required output load, which is an antenna used for transmission in most cases.

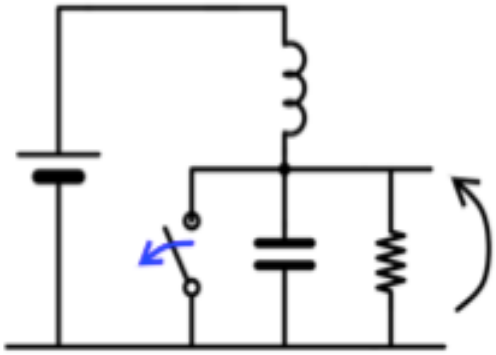

Fig2: Class E power Amplifier model [Ali.M.Niknejad (2014)]

Although, the linearity of this block can be a drawback, it does not play an important role in this particular application as, the input signal is of a Frequency shift-keying (FSK) format and has constant amplitude. Linearity is mostly a concern for inputs with variable amplitudes.

Both class D and class E use the same concept of using the transistor as a switch for low dissipation of energy in the Metal oxide semiconductor field effect transistor (MOSFET), class E requires the supply to be connected to a inductor choke of a large value, which directly translates to large area utilization. Also, the voltage swings for a class E is much higher than the supply voltage, and it offers low power gain [Ali.M.Niknejad (2014)]. Whereas, a class D amplifier needs the supply to be connected to a MOSFET used as a switch again, thus decreasing the area requirement substantially.

Consequently, the choice is using a class D amplifier was discussed upon and voted for by the team.

ARCHITECTURE:

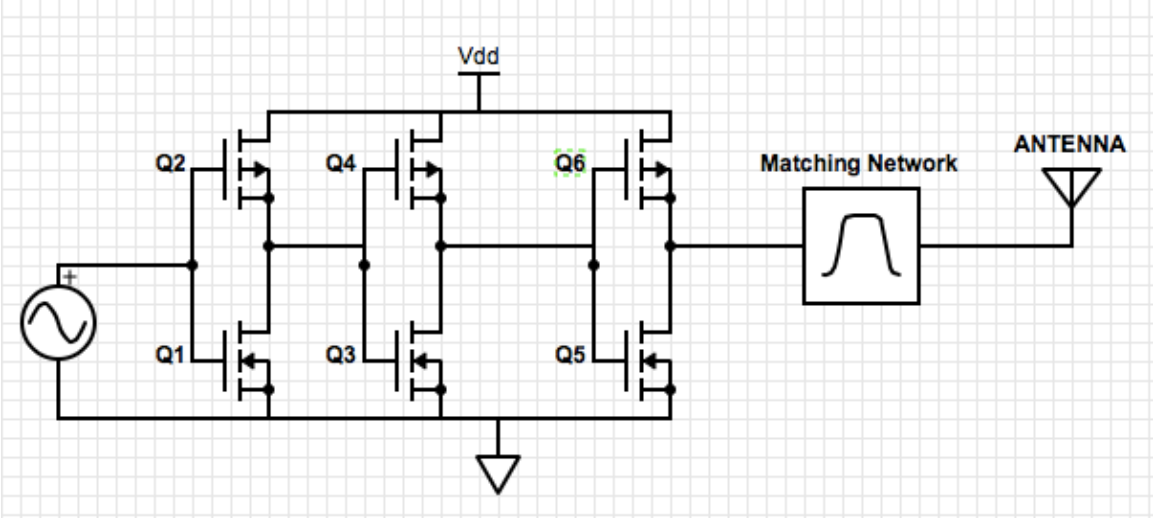

Fig3: Architecture of the Power Amplifier

The control over power transmitted to the load depends on the impedance (resistance) of the load seen by the output node of the amplifier. To illustrate, if the drain node were connected to the antenna directly with a conductor or wire, it would see the impedance of the antenna, this impedance would draw a certain amount of power from the supply or source based on a few analytical energy equations. In our case, the output load is an antenna, which has a standard impedance of 50 ohms. In order to meet the specification of the power drawn by the load precisely, this load seen by the output node has to be transformed to a different value with respect to the energy relations, while keeping the antenna impedance constant. This process of transforming the load can be done by using a network called 'matching network' to match the output node to the impedance it wants to see.

There are various architectures used for serving the purpose of translating the impedance seen by the output and some of the most generic such networks used in the past are T-match, L-match, pi-match or a combination of the three. The matching networks are mostly designed

using passives like inductors and capacitors and the quality of the match is defined by a term called “Quality factor”. The quality factor of a match defines its ability to filter out spurious signals, which are not of our interest. Quality factor can also be defined for individual components like inductors and capacitors, for which it means the parasitic resistance that exists in the component that deviates the component value from ideal also causing dissipation of energy.

MATCHING NETWORK:

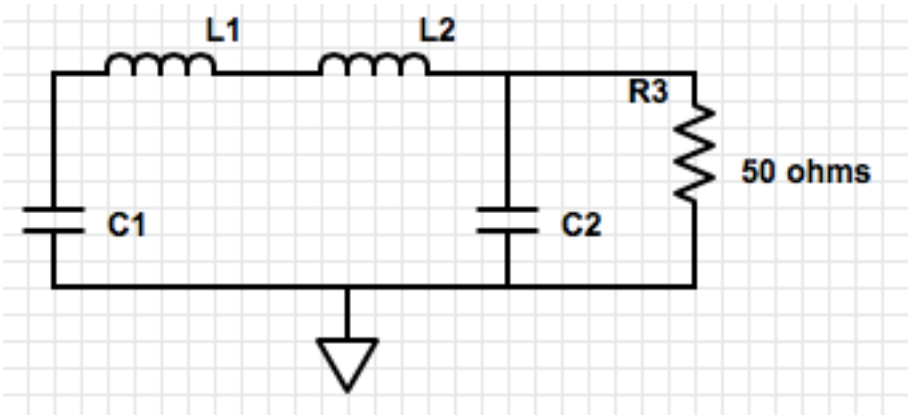

Fig 4: pi-match

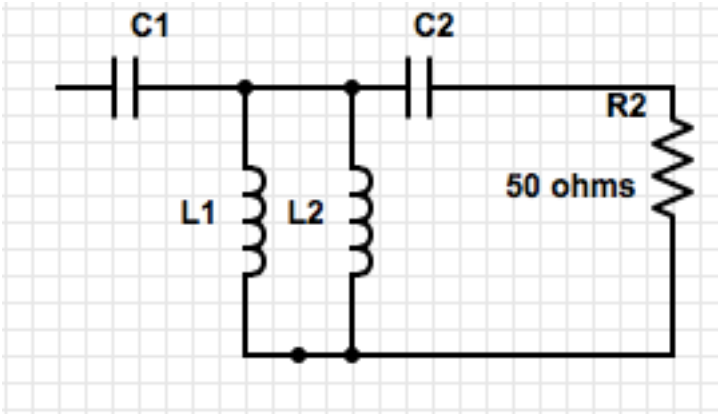

Fig 5: T-match

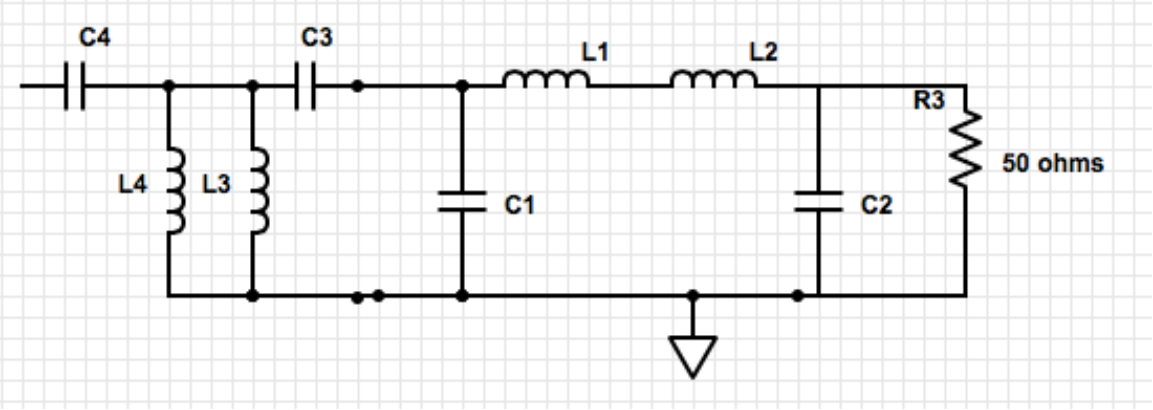

Fig 6: Pi-match plus T-match

For this power amplifier a T-match was employed, mainly because it isolates the DC component and the AC component –which is of our interest at the output node and also provides the impedance transformation that we need for achieving the required functionality the block.

Section III: Methods and Materials

The process of IC design follows a path where the first step is picking a 'process', which defines the minimum area possible for a MOSFET device, For this application our advisors have chosen a 180nm process. Secondly, the foundry with an available process close to our choice was chosen which is TSMC located in Taiwan. TSMC is also known for its good performance and is a key market player in the semiconductor industry [Foundry-ranking-capacity-2013-2014]. Next, the suppliers for the passives in the printed circuit board were chosen according to the quality factor presented by each supplier. DigiKey and Coil craft offer a very good quality factor and therefore, we have opted for these suppliers.

We procured all the models needed for the active and passive devices used in the design from TSMC –the foundry that would be fabricating out chipset. Having chosen the class D amplifier

architecture for this project, the next step would be to begin the design using a tool for developing schematics called 'cadence' using its version 5.0 GUI.

The design methodology was carried out in the following steps:

STEP1: Derive the load impedance value that needs to be seen by the output node to draw a power of 100uW from the supply.

$$power = \frac{VI}{2} = \frac{V^2}{2R} = I^2R$$

$$\frac{V^2}{2R} = \frac{0.9 * 0.9}{2R} = 100u\,W \Longrightarrow R = 4.05K\,ohms$$

STEP2: Derive the values of the passives in the T-match and pi-match for the matching network. Using the equations:

$$\frac{1}{2 * pi * f} = L * C$$

Where, f=60Mhz, pi= 3.141, substituting these values we get,

$$LC = 6.9 * 10^{-18}$$

For a T/pi-match we first transform the impedance 50 Ohms to a impedance higher than a required impedance of 4.05K. We can select this impedance to be 8K ohms. A T/pi-match can be divided into two L-matches for the purpose of extracting the values of the components.

For the first L-match from the right [fig 6],

$$Rint = \frac{Rs * jwL2 + \frac{L2}{C2}}{\frac{1 - w^2 * L2 * C2}{JwC2} + Rs}$$

Where; Rint is the intermediate resistance between the two L–match stages.

at resonance or at 60MHz,

$$Re\{Rint\} = \frac{L2}{C2 * Rs}$$

Using the above values of {L*C}, we can derive the values of L2 and C2.

Similarly, the values other half of the L-match can be derived as L1 and C1.

component	L1(uH)	C1(pF)	L2(uH)	C2(pF)
value	11.75	0.6	1.314	5.365

STEP3: Derive the size of the mosfets:

Amplifier: Width and length needed to keep the ON-resistance low to avoid dissipation through the switch when it is 'ON' and at the same time minimize the loss due to the gate caps.

Using Matlab, both, the $\boldsymbol{Ron} \propto \frac{\mathbf{1}}{\boldsymbol{ratio}}$ & $\boldsymbol{cap} \propto \boldsymbol{ratio}(\boldsymbol{L} = \boldsymbol{const})$ are plotted on y-axis with the aspect ratio defined on the x-axis.

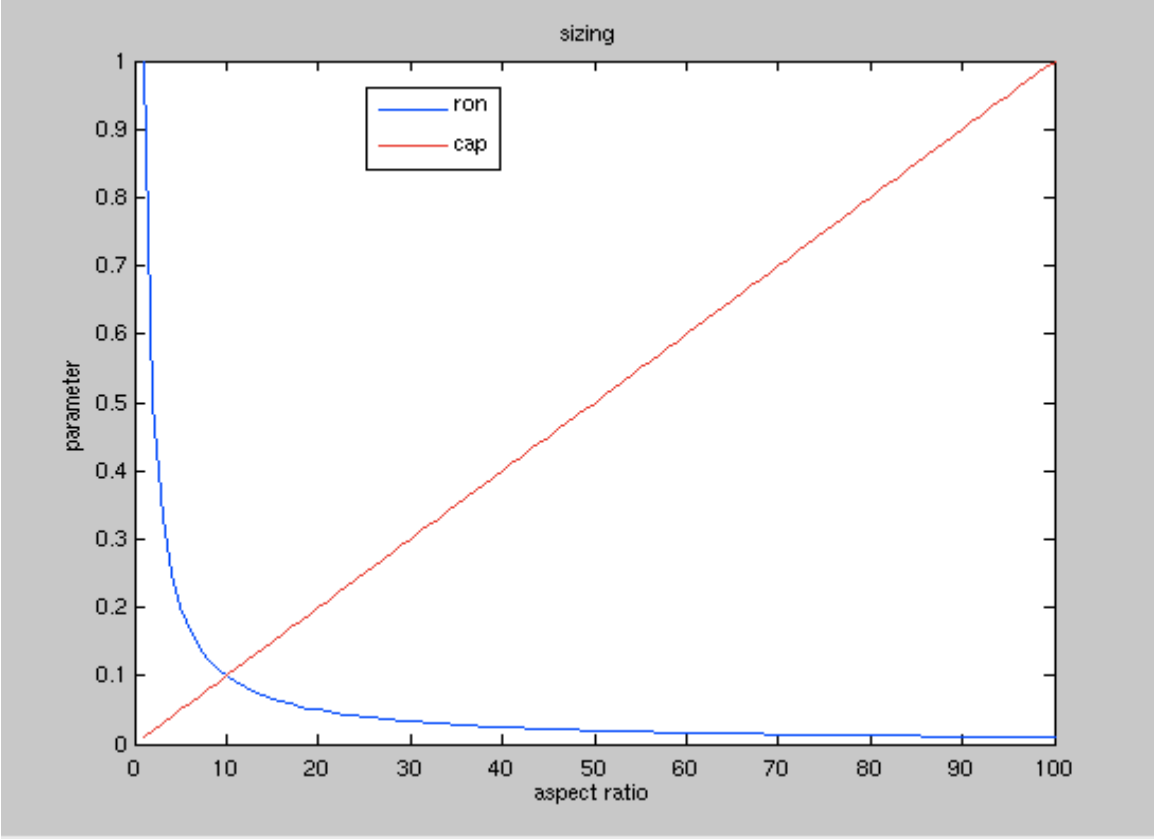

Fig7: Sizing the devices

An aspect ratio of 50 was used from the above plot.

Keeping length=180nm, Width =9u for the NMOS and 18u for the PMOS.

Driver: The driver stage must provide an input square wave with a good step response to the amplifier. This can be accomplished by increasing the strength of the driver (sizing it up), but in turn increases the $C * V^2 * f$ losses. Therefore a minimum is picked which establishes the best size for optimal drive strength as well as low loss. This is mainly to reduce the time for which both the mosfets (PMOS and NMOS) are turned 'ON'. In an event of both the transistors turning on, there will be short-circuit current flowing through the inverter from supply to ground, with a value defined by the on-resistance of the mosfets in saturation region. The chosen sizes were; W=0.36u m and L=0.18 um for the NMOS and, W=0.72 um and L=0.18 um for the PMOS.

STEP4: Derive the value of the impedances provided by the T-match at harmonics/ multiples of the fundamental frequency-60MHz.

As discussed above the impedance seen by the output node after using a T-match and Pi-match can be evaluated from the equations below:

$$\boldsymbol{R(T)} = \frac{\mathbf{1}}{\boldsymbol{jwC1}} + \frac{\boldsymbol{Rs} * \boldsymbol{jwL2} + \frac{\boldsymbol{L2}}{\boldsymbol{C2}} * \boldsymbol{jwL1}}{\frac{\mathbf{1} - \boldsymbol{w^2} * \boldsymbol{L2} * \boldsymbol{C2}}{\boldsymbol{jwC2}} + \boldsymbol{Rs} * \boldsymbol{jwL1} + \frac{\boldsymbol{L2}}{\boldsymbol{C2}} + \boldsymbol{Rs} * \boldsymbol{jwL2}}$$

$$\boldsymbol{R(pi)} = \frac{\boldsymbol{Rs} * \left(\mathbf{1} - \boldsymbol{w^2} * \boldsymbol{L1} * \boldsymbol{C1}\right) + \boldsymbol{jw}(\boldsymbol{L1} + \boldsymbol{L2}) - \boldsymbol{w^2} * \boldsymbol{L2} * \boldsymbol{C1} * \boldsymbol{Rs}}{(\mathbf{1} + \boldsymbol{jwC1} * \boldsymbol{Rs}) * (\mathbf{1} - \boldsymbol{w^2} * \boldsymbol{L2} * \boldsymbol{C2}) + \boldsymbol{jwC2}[(\mathbf{1} - \boldsymbol{w^2} * \boldsymbol{L1} * \boldsymbol{C1}) * \boldsymbol{Rs} + \boldsymbol{jwL1}]}$$

Using matlab we get the following values of impedances at higher frequencies.

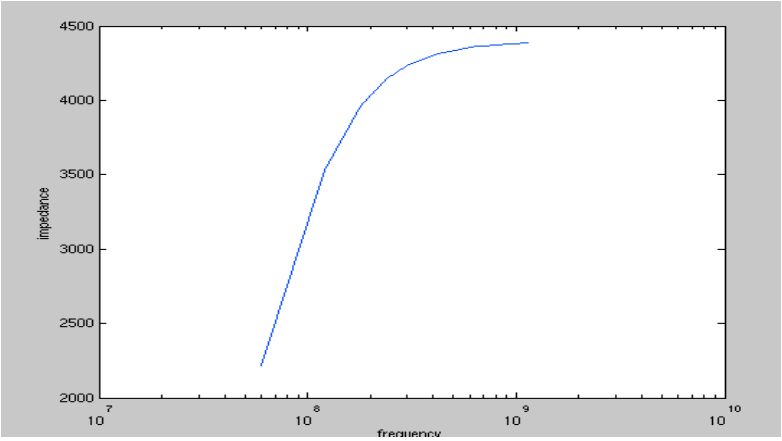

Fig 8: Impedances for T match

STEP 5: Estimate the efficiency using the ideal waveform models.

For an ideal switch the drain voltage follows the Fourier series form [Ali.M.Niknejad (2014)]:

$$\boldsymbol{Vd = \frac{VDD}{2} * (1 + s(wt))}$$

$$\boldsymbol{S(\theta) = sign(sine\theta) = \frac{4}{\pi} * (sin\theta + \frac{1}{3} * sin3\theta + \frac{1}{5} * sin5\theta + \cdots)}$$

The load current is ;

$$\boldsymbol{iL = \frac{4}{\pi} * \frac{VDD}{2 * R} * sin\theta = \frac{2VDD}{\pi * RL} * sin\theta}$$

Thus, the load power is

$$\boldsymbol{PL = \frac{iL^2 * RL}{2} = \frac{2}{\pi^2} * \frac{VDD^2}{RL} = \frac{0.2 * VDD^2}{RL}}$$

The average DC current drawn from the supply is

$$\boldsymbol{\frac{Ip}{\pi} = \frac{2}{\pi^2} * \frac{VDD}{RL} = PL}$$

This implies that the efficiency is $\boldsymbol{\eta = 100\%}$.

STEP 6: Design of schematic with the above derived values for the MOSFET s' aspect ratio and the matching network. Figure 9 shows a version of the schematic drawn in cadence version 5.0.

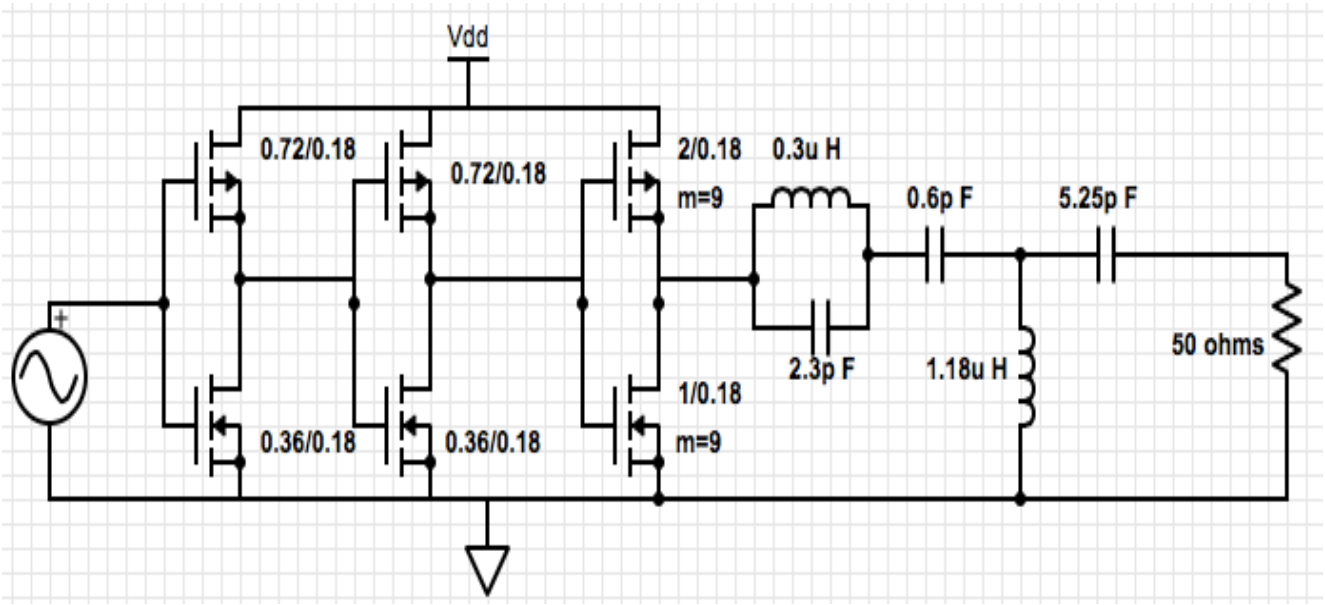

Fig 9: Schematic with final values

STEP 7: Once the expected results as estimated in the above steps were derived from the schematic, a layout of matching the schematic was drawn using the 7 metal layers given by TSMC [fig. 10]. Below is the layout of the power amplifier.

Floorplan:

The floor plan of the layout was decided by estimating the pin positions of the input and output. The output is especially crucial, as any resistance due to long routes could cause the power to dissipate at these nodes.

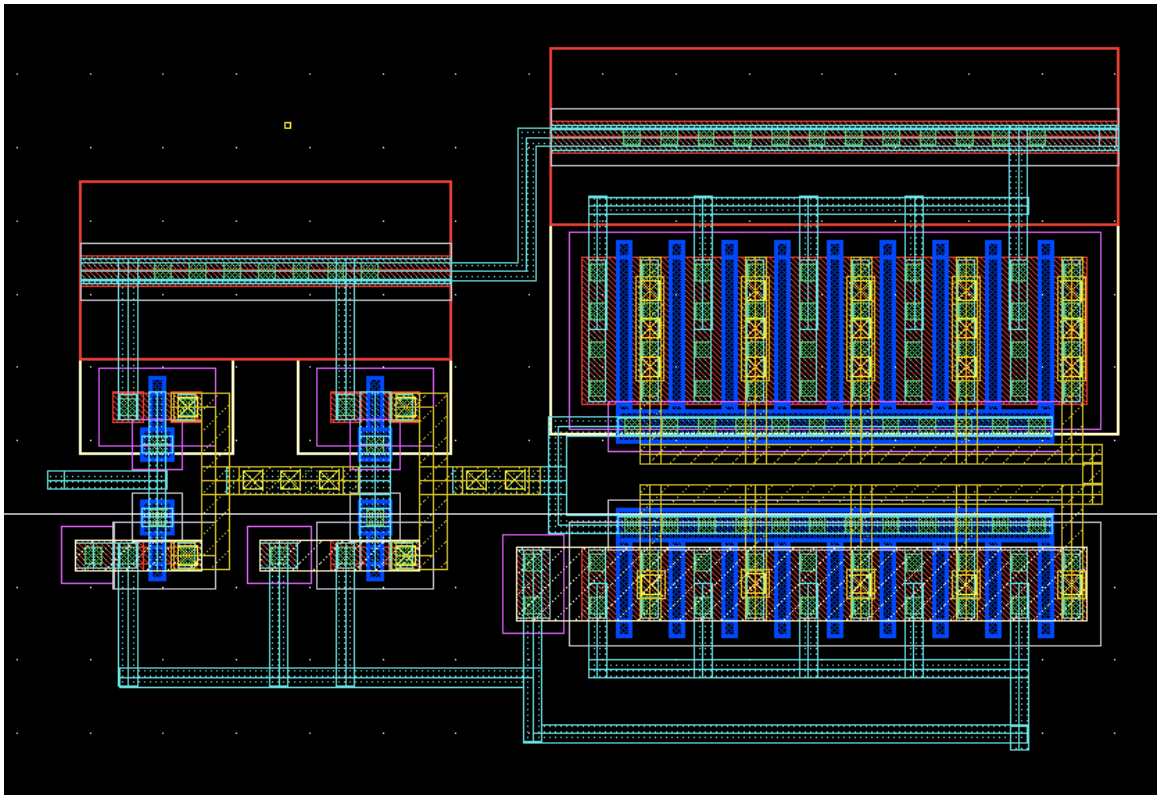

Fig 10: first cut Layout

Routing:

The connections between the inverter stages are done using metal 1, as it provides low capacitance and keeps the drive strength intact. The supply and ground rails have been routed

with metal 1, with the ide that the top level routing will be carried on with higher metals that can be staked upon these layers.

RESULTS AND DISCUSSION

Following waveforms show the simulated results for the various performance metrics.

POWER-GAIN:

Below is a plot showing the power gain of the amplifier. The reported power gain is 47 dB at the fundamental frequency.

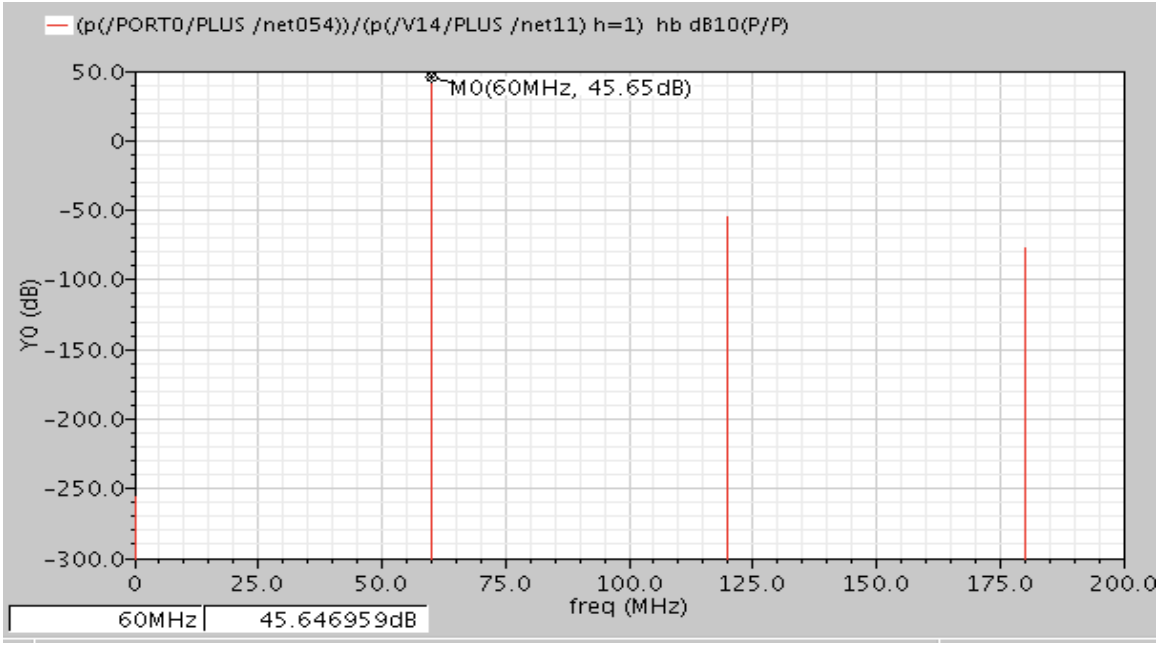

Fig 11: measured power gain

OUTPUT WAVEFORMS:

The following waveforms depict the voltage and current waveforms at the port or the virtual antenna. We can see that the waveforms are purely sinusoidal.

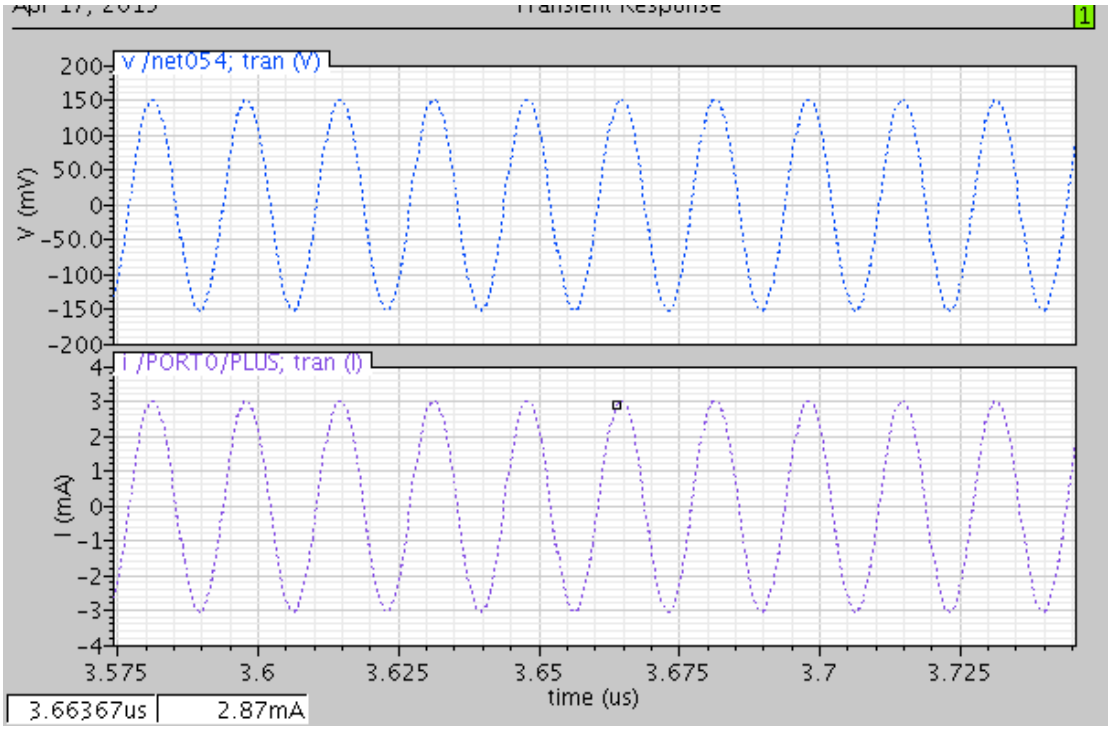

Fig 12: simulated output waveforms

POWER:

Below are two plots showing the power levels of the power amplifier at different harmonics up to the 19th harmonic of the fundamental frequency. The first plot shows the power levels without the L–match filtering at the port and the 3rd harmonic filtering at the drain.

The second plot depicts the power levels with both the L-match filtering at the port and the 3rd harmonic filtering at the drain. Both the results are at a typical temperature and corner. Refer to the discussion section for further details.

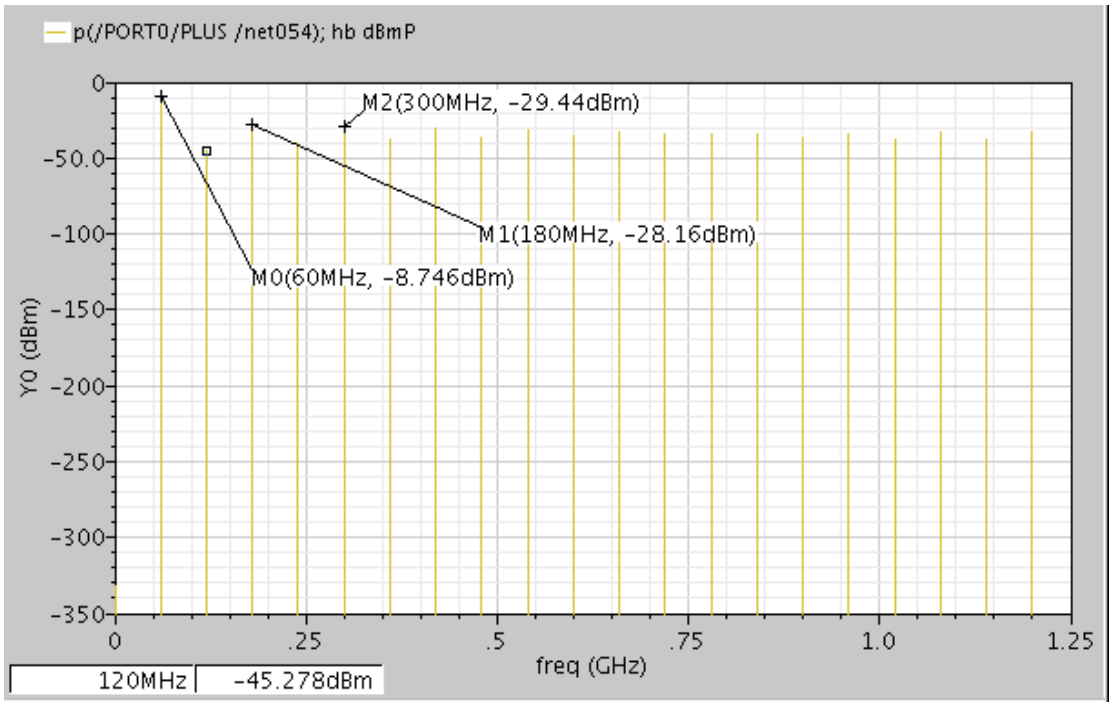

Fig 13: Power without the L- match filtering

We can see that, the harmonic power is high and can affect the efficiency significantly.

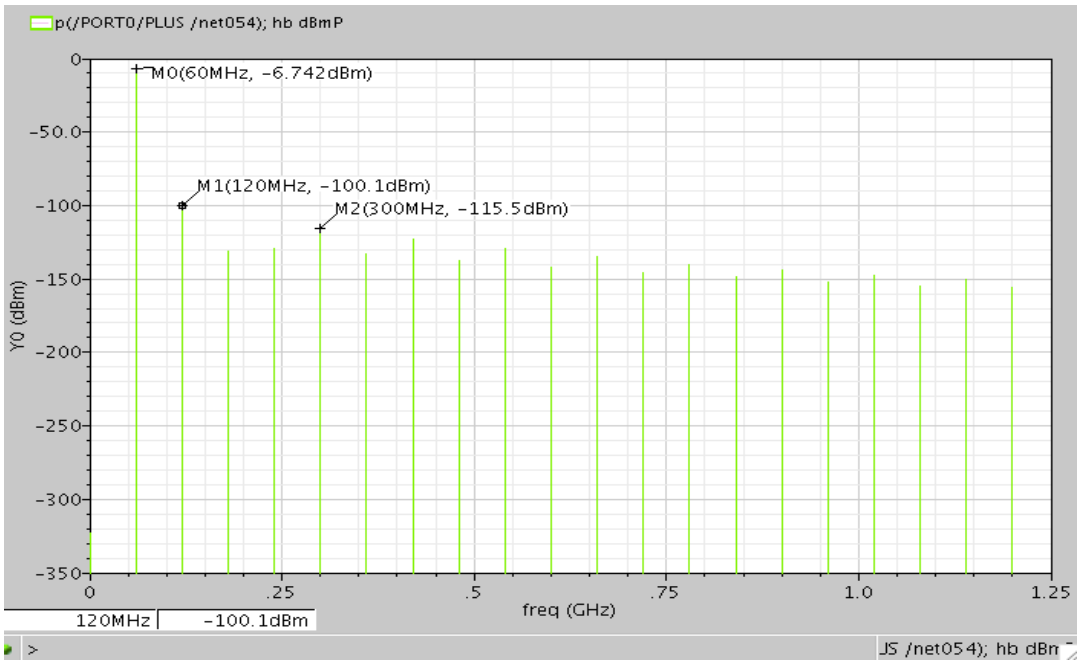

Fig 13:Power with the L- match filtering

ISSUE:

We observe from the power plots above that the power at the odd order harmonics; especially the third order harmonic (3w0) or 180MHz is rather high, implying that the T-match provides low impedance at these frequencies. In order to fix this issue, a network resonating at 180MHz was added before the matching network to block the 3rd order harmonic from passing through to the load.

Following plot shows the improved efficiency after adding the “block network” and the resultant power at the 180MHz and other odd order frequencies.

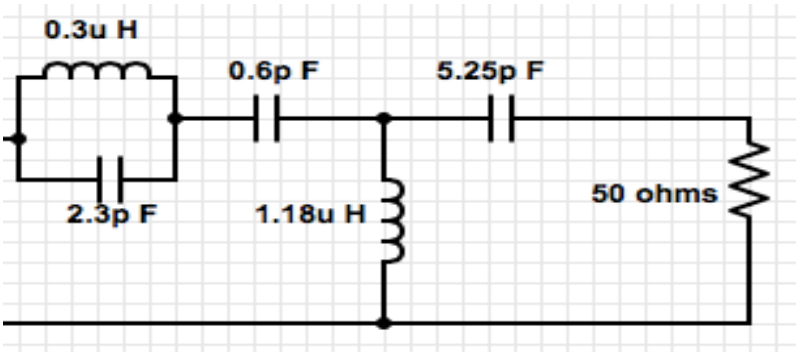

Fig 14: Third harmonic Filtering +T match

Match type	L (nH)	C1 (pF)	C2 (pF)	Block-cap (pF)	Max efficiency	Power (dBm)	Drawback
pi	582	13.13	117	0.8	82.5%	-10	Needs dc-block
pi	184	41.5pF	371	1.2	84%	-9.5	Needs dc-block
T+3wo filter	1180	0.587	5.25	-	79.5%	-8.2	
Pi+T + filtering	1180	0.587	5.25		89%	-6.72	needs 3 inductors

TABLE3: Impedance calculated for different matches

EFFCIENCY:

Setup: A simulation was setup with the “Harmonic balance analysis”, with 19 harmonics, and a fundamental frequency of 60MHz. The reported efficiency is 86.35%.

Below is a plot showing the efficiency of the Power amplifier at a typical temperature and typical corner.

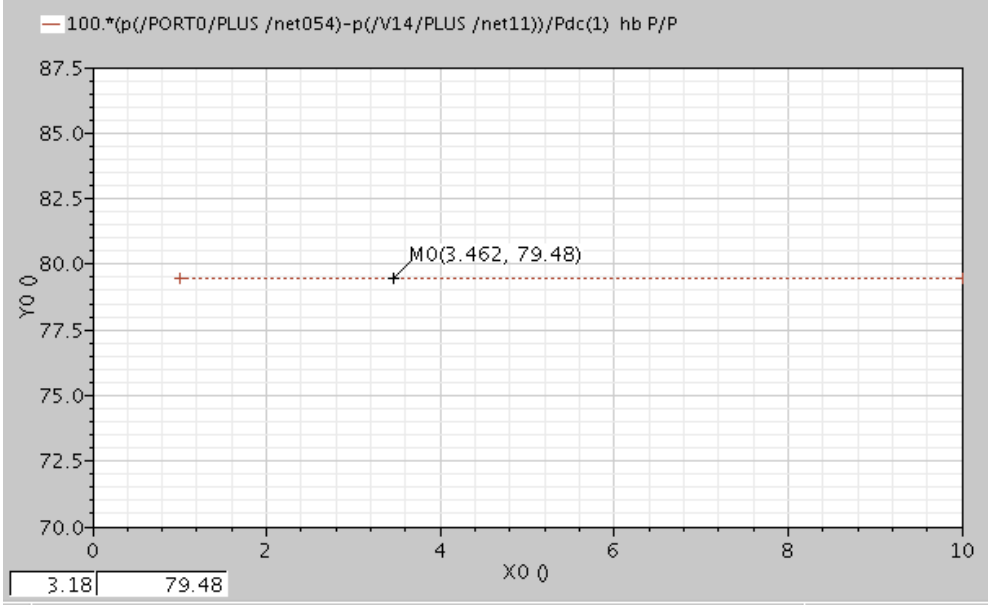

Fig 15: Measured efficiency with filtering

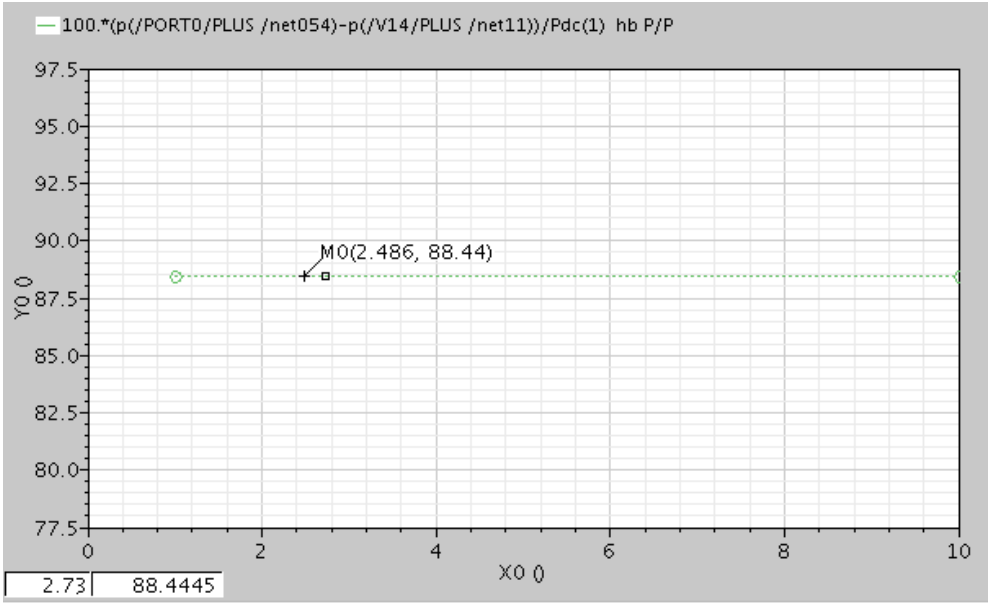

Fig 16: measured efficiency before harmonic “block network”

As efficiency is our key parameter, presented here is a list of the contributors to degrading efficiency away from a theoretical ideal of 100%. From the above plots it is evident that the efficiency improves by 16% just by adding a third harmonic block network at the drain of the amplifier.

The critical contributor to the efficiency degradation now is the short circuit current in the drain, while the voltage is non-zero.

In theory the ideal voltage and current waveforms for 100% efficiency follow that the voltage is zero when the current in non-zero and vice versa. This concept ensures that there is no power dissipation in the circuit itself and all of the power sourced from the supply is transferred to the load efficiently.

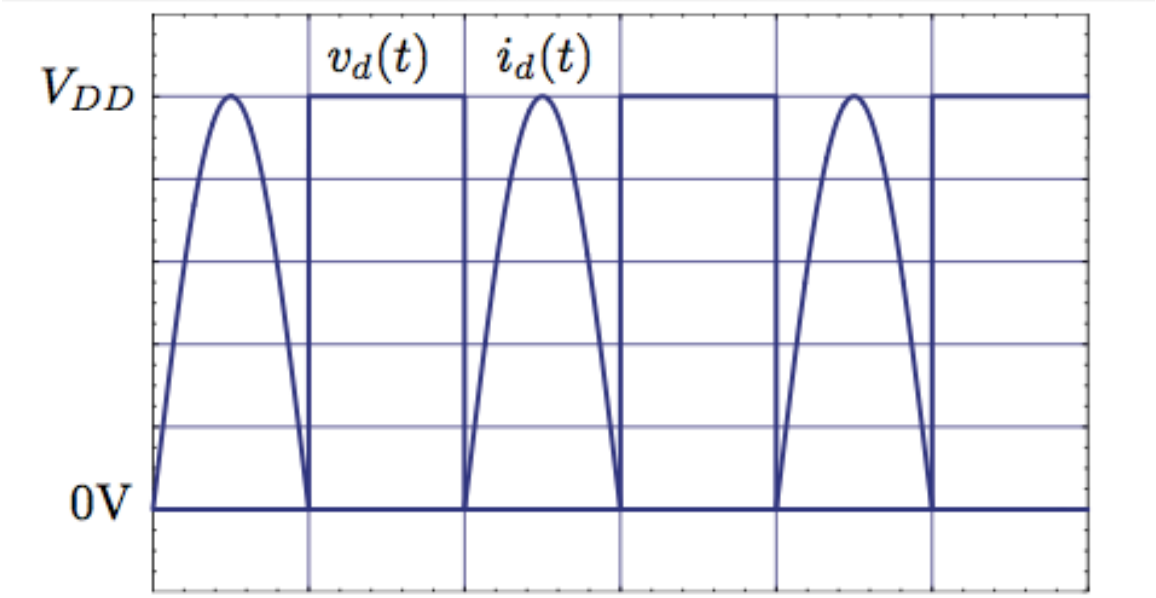

Fig 17: Ideal class D output waveforms [Ali.M.Niknejad (2014)]

DRAIN WAVEFORMS:

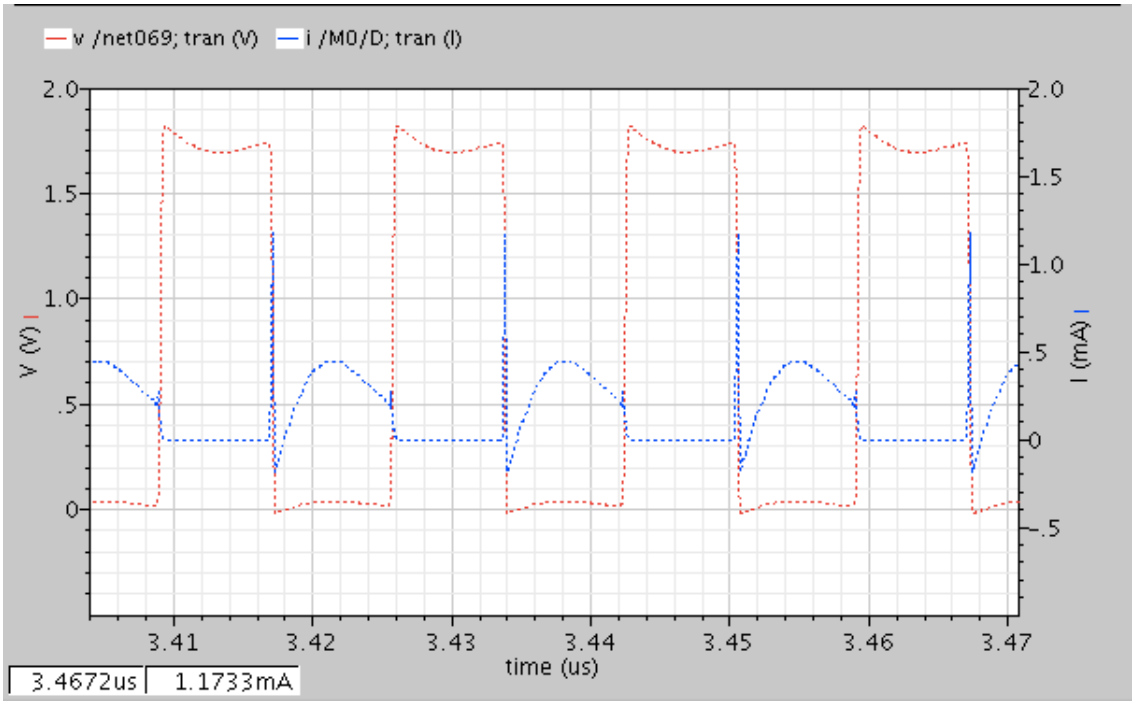

Fig 18: Simulated Drain waveforms

Power loss due to short circuit current when both the devices are turned on:

As we can see from the above plot, the degradation due to the glitch in the current waveform when the voltage goes to zero is high.

Calculating the power lost due to this glitch is:

$$\boldsymbol{Pglitch = \frac{1}{T} * \int_{0}^{\frac{t}{10}} Iglitch * Vglitch * dt}$$

After exporting the .csv file from the above plot into matlab we estimate that Pglitch =13u W ➔ 6.4% efficiency loss.

The peak value of Iglitch goes by the equation:

$$\boldsymbol{Iglitch = \frac{VDD}{2 * Rsat} = \frac{1.8\,(V)}{2 * 6k(ohms)} = 1.5mA}$$

Unfortunately, this issue needs low aspect ratio (W/L) for the transistors for Rsat to be higher. However, this is not possible as the size decides the 'ron' when the transistor operates as a switch, and this needs be <50 ohms to maintain a good quality factor for the overall network.

Other Contributors for efficiency degradation:

1- Harmonic dissipation:

   Using the harmonic balance analysis, we see that the total harmonic power added from the second to 19th harmonic sums upto 1.2% after adding the 3rd harmonic filter at the drain node.

2- Parasitic losses:

   The passive devices have a quality factor of 20.Therefore, the internal resistances of the components adds upto a loss of 2.4% .

3- Driver stage $C * V\text{^}2 * f$ losses:

   The input gate capacitance of the inverters is 1.5f F each and the amplification stage offers a gate cap of 31f F.

   This produces a loss of 6.722uW = 3.4 %

	Short circuit current	Harmonics	Passive parasitics	Driver $C * V\text{^}2 * f$	Total loss
loss	6.4%	1.2%	2.4%	3.4%	13.4%

TABLE 4: loss contributors

DESIGN 2 : CLASS A

As a part of the project I was also to design a class A power amplifier for comparison with the class D PA and also for having an option of eliminating the off chip matching networks as a simplistic approach.

ARCHITECTURE:

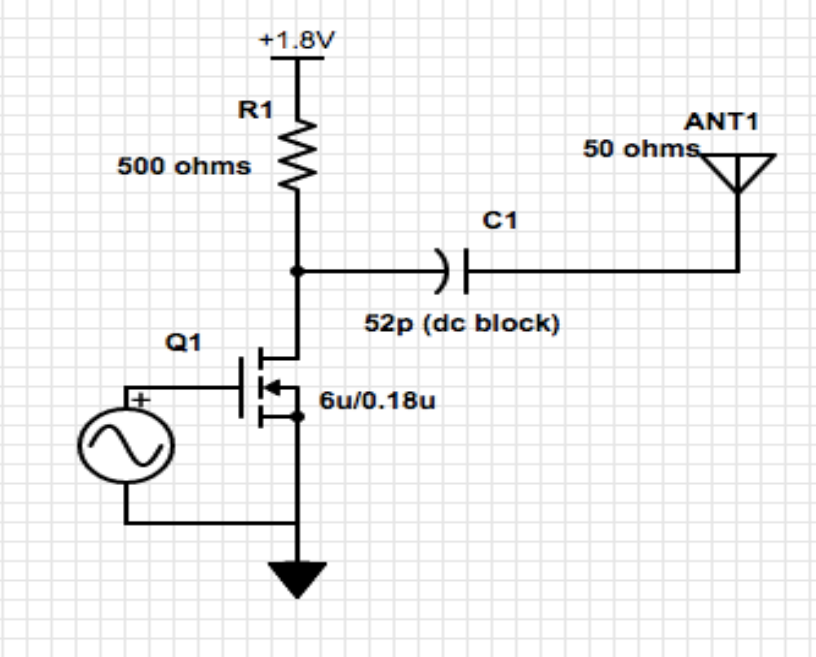

Fig 19: Class A schematic-NO MATCH

DESIGN METHODOLOGY

STEP 1: The given specification to be met for the output power is

100uW = -10dBm.

$$\frac{V^2}{2R} = 100u$$

STEP 2: since we plan to terminate the PA without any matching network with just an antenna→ we have a output impedance of 50 ohms.

$$V^2 = 0.01 \rightarrow V = 0.1V = 100mV$$

$$Iload = \frac{V}{R} = \frac{100mV\text{Ʊ}}{50} = 2mA$$

STEP 3: Efficiency estimation→ Assuming we use all the current in driving the load resistance and have no power dissipated in the system, we get:

$$\frac{Pload}{Pdc} = \frac{100mV * 2mA}{1.8V * 2mA} = 0.05 = 5\%$$

STEP 4: It is evident from the above calculation that it is not possible to get a highly efficient PA for the given specification of output power without a matching network; in order to derive maximum efficiency from this system we see that following:

$$\frac{V^2}{2R} = 100uW \rightarrow Rmax = \frac{V(max - achieveable)^2}{2 * 100uW}$$

$$\rightarrow Rmax = \frac{1.8 * 1.8}{200uW} = 16K\ Ohms$$

The maximum achievable **V-load =1.8**, assuming we have an inductive choke that swings from **0 to 2*VDD**

$$Efficiency = \frac{Pload}{Pdc} = \frac{100uW}{1.8V * 111uA} = 50\%$$

This calculation explicitly tells us that the load has to be transformed in order to get maximum efficiency.

STEP 5: choke inductor design; the choke needs to have an **impedance of 10 times the load impedance** for transferring most of the power to the load since it has a lower impedance by the current division theorem.

$$XChoke = 10 * 50 = 500 \rightarrow BFL = \frac{500}{2 * pi * freq} = 1.32uH$$

STEP 6: The output voltage we need is 100mV in amplitude; the load impedance is 50 ohms. This implies that if we provide a input swing of amplitude 0.9V

Designing the T-match for transformation of 50 ohms→16K ohms

STEP7: Derive the values of Ls' and Cs' for the T-match as following:

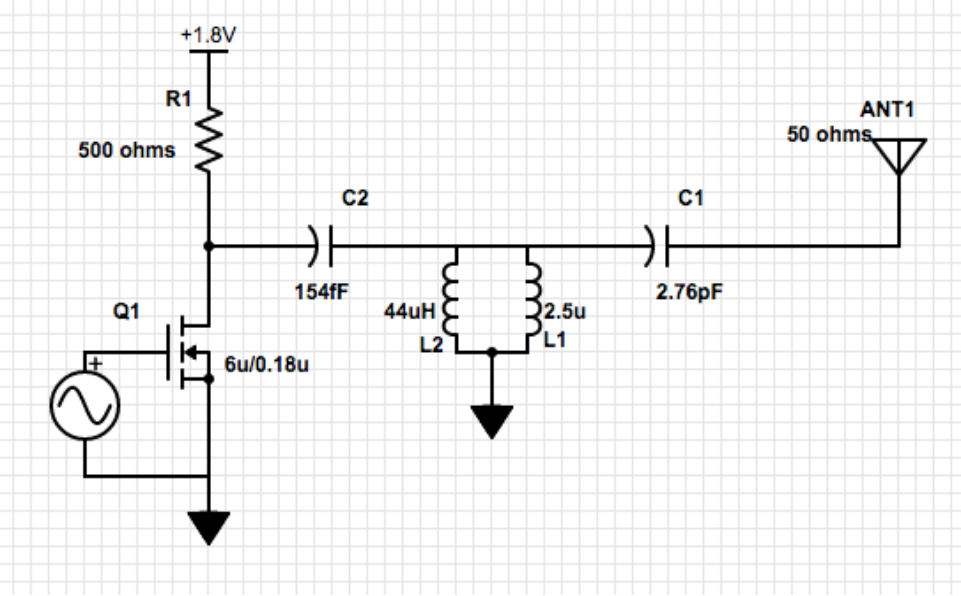

Fig 20: class A schematic with T-match for impedance transformation

$$XChoke = 10 * 16K = 160K \rightarrow BFL = \frac{160K}{2 * pi * freq} = 424\,uH$$

$$\omega^2 = \frac{1}{2 * pi * L * C} \rightarrow L * C = 6.9 * 10^{-18}$$

$$Rp * Rs = \frac{L}{C} \rightarrow 16K * 18K = \frac{6.9 * 10^{-18}}{c^2} \rightarrow C1 = 2.76pF$$

$$L1 = 2.5uH, C2 = 154fF, L2 = 44.8uH$$

RESULTS AND DISCUSSION

Power gain:

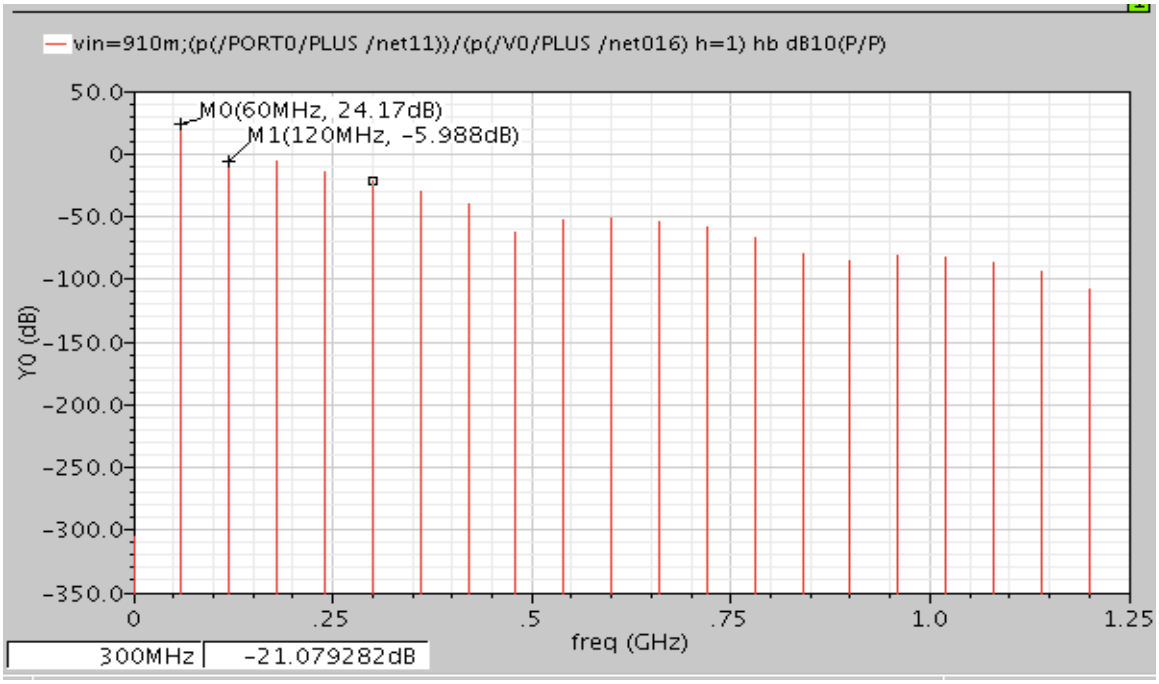

Fig 21: Power gain for class A

Output power: As expected from the hand design, the **output power = -10dBm** for an input voltage amplitude of 0.9V.

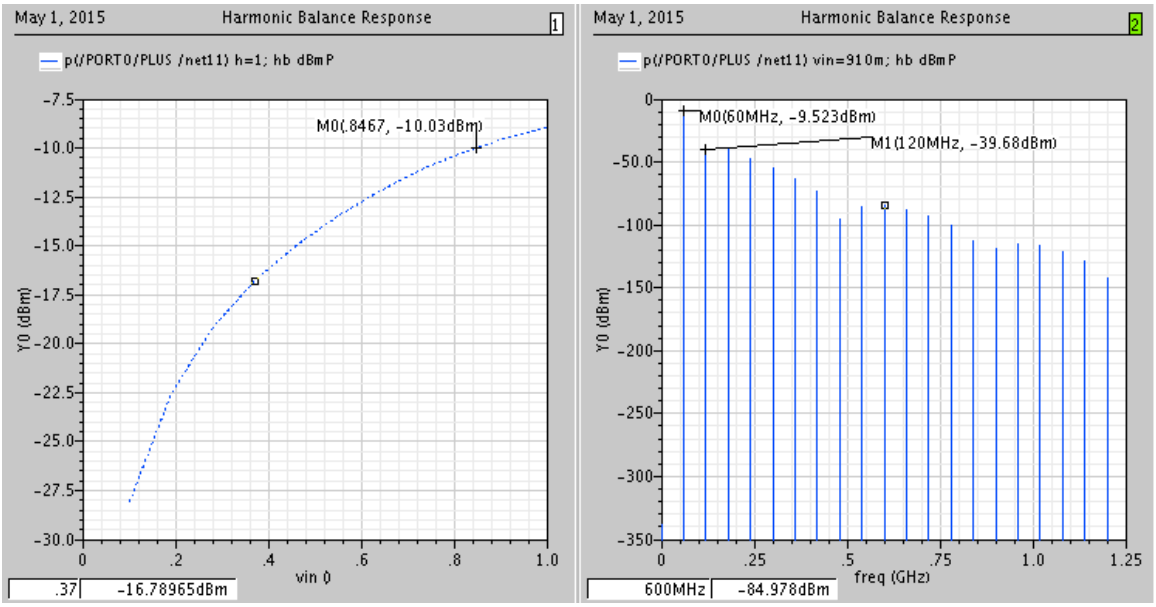

Fig 22: output power with variable vin and at vin=0.9 resp.

Efficiency:

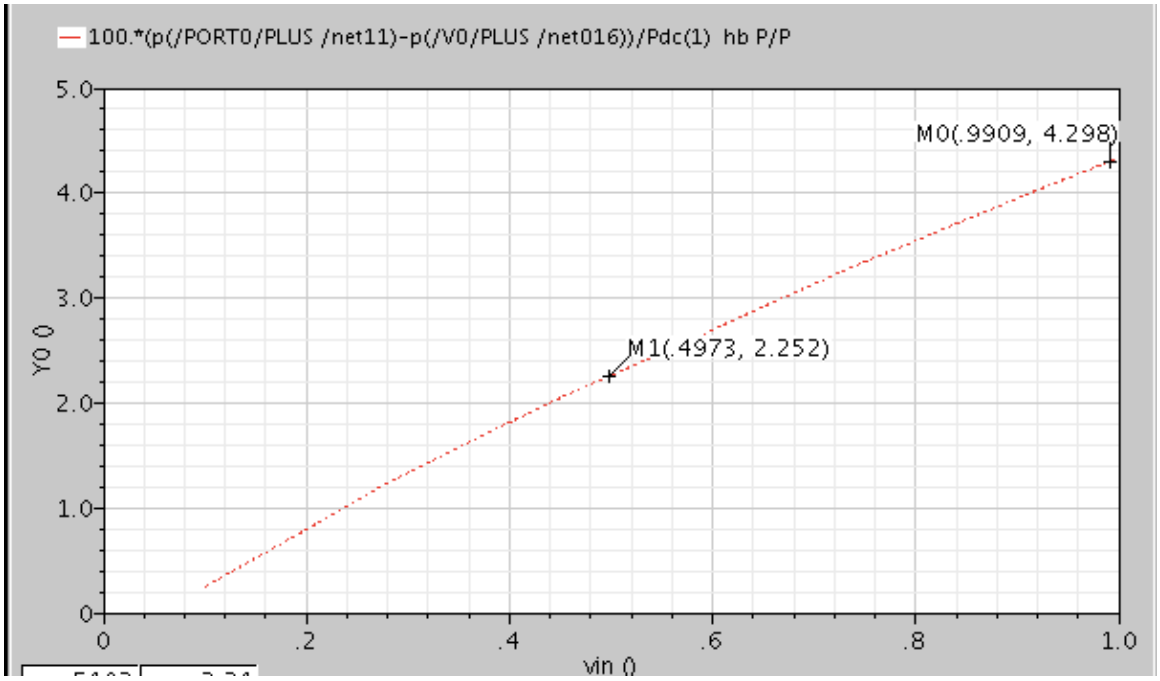

Fig 23:Efficiency with variable vin = 4%(vin max)

Output voltage:

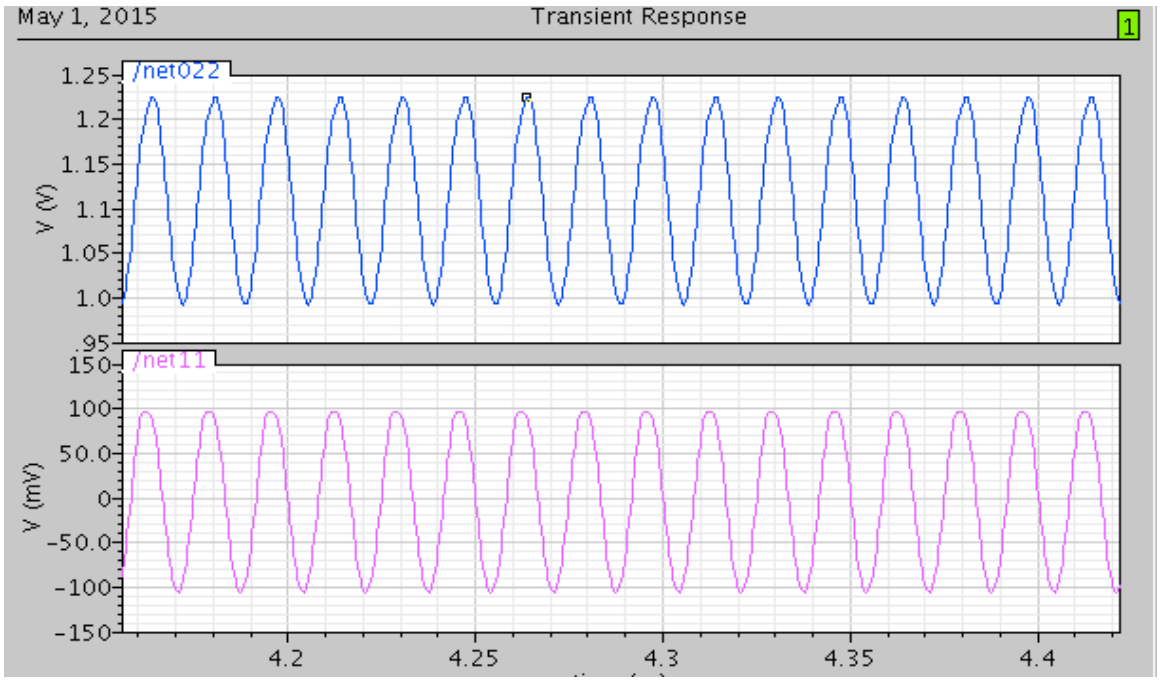

Fig 23: filtered V & I waveforms at the output port

CLASS A WITH T - MATCH

Output power: As expected from the hand design, the **output power = -10dBm** for an input voltage amplitude of 0.9V.

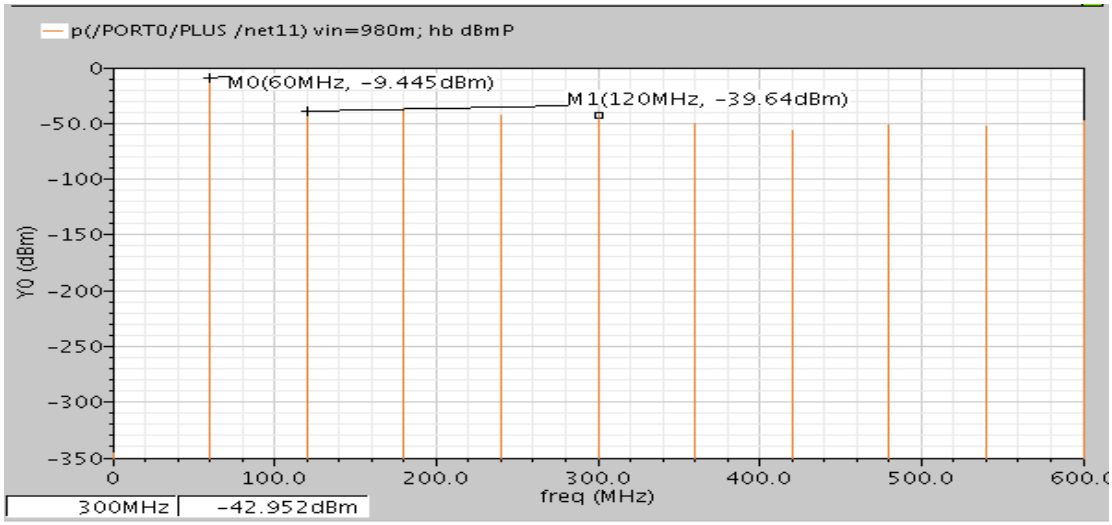

Fig 24: output power with harmonics

Efficiency:

We can see that the efficiency depends on the output impedance as derived in the hand calculations. The efficiency is 42% with the ideal load.

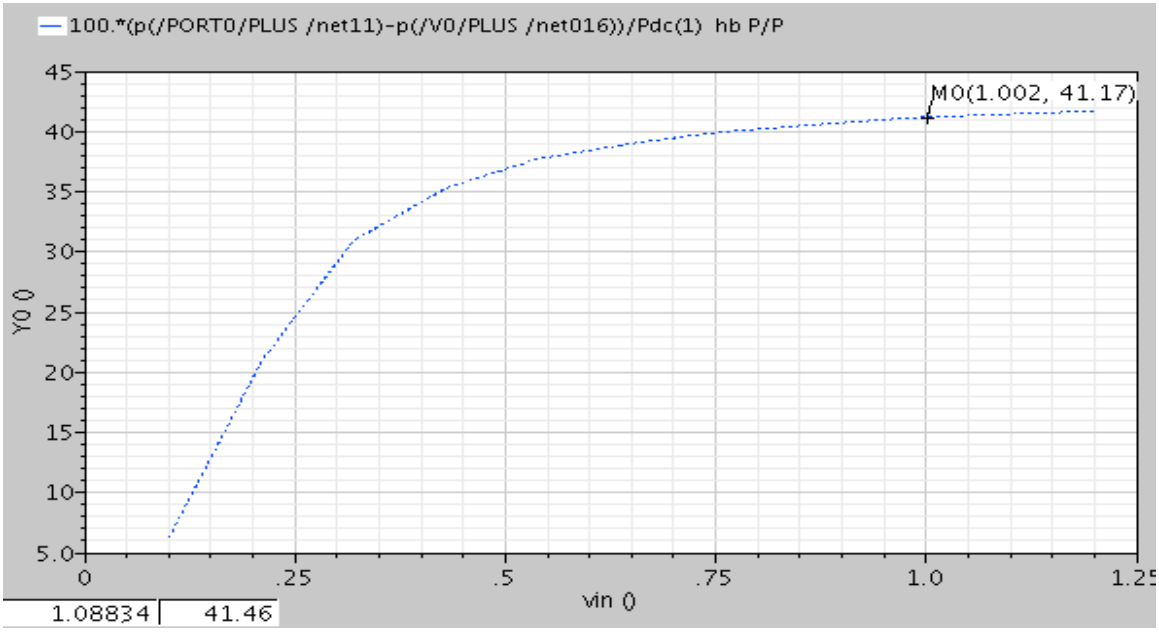

Fig 25: Efficiency with added T-match = 41%

DESIGN 3 : CLASS E

As the efficiency achieved for the class D PA is not sufficient and since we can do better at a frequency of 60MHz, a decision to design a class E power amplifier for comparison was made. Following is the architecture and design procedure for a class E PA..

ARCHITECTURE:

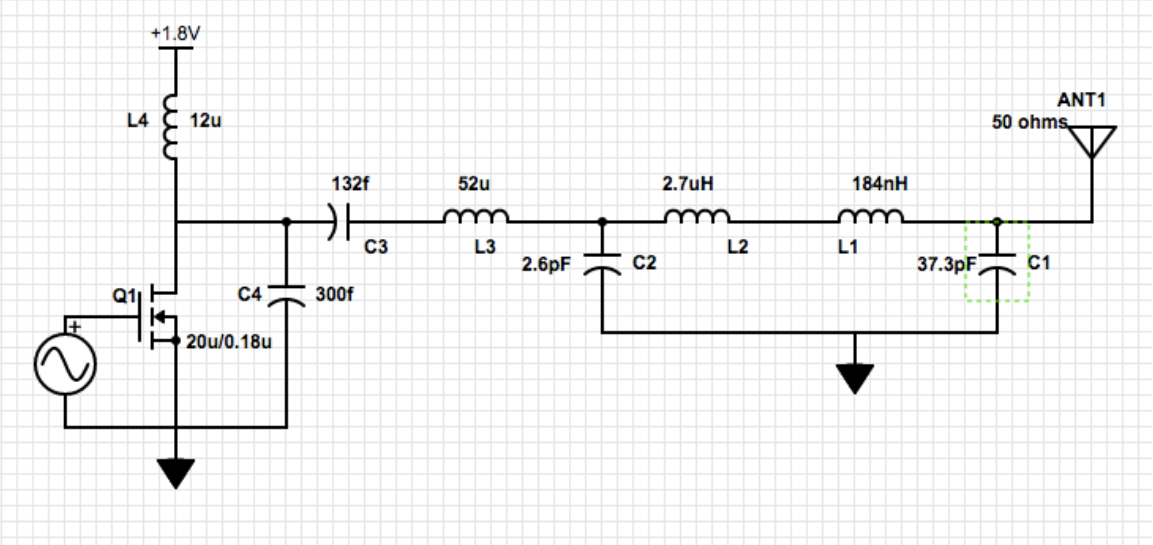

Fig 26: Class E schematic and derived values

DESIGN METHODOLOGY

STEP 1: The given specification to be met for the output power is

100uW = -10dBm.

$$\frac{V^2}{2R} = 100u$$

STEP 2: A class E PA has an inductive choke as a load, which allows a **swing from 0→3VDD**.

$$\frac{V^2}{2R} = \frac{\left(\frac{5.4}{2}\right)^2}{2R} = 100uW \rightarrow R = 36K\ Ohms$$

STEP 3: Using the table below; we can derive L3, C3 and C4, which are responsible for getting the perfect output waveform.

Q_L	$PR/(V_{CC} - V_o)^2$	$C_1 2\pi fR$	$C_2 2\pi fR$
infinite	0.576801	0.18360	0
20	0.56402	0.19111	0.05313
10	0.54974	0.19790	0.11375
5	0.51659	0.20907	0.26924
3	0.46453	0.21834	0.63467
2.5	0.43550	0.22036	1.01219
2	0.38888	0.21994	3.05212
1.7879	0.35969	0.21770	infinite

Fig 27: class E design methodology [N.O.Sokal]

The above values are derived from the equations:[Nathan .O.Sokal]

Picking a QL=20

$$C3 = \left[\frac{1}{2 * pi * f * R} * \left(\frac{(pi)^2}{4} + 1\right)\left(\frac{pi}{2}\right)\right]\left[0.9988 + \frac{0.914}{Ql} - \frac{1.03}{(Ql)^2}\right]$$

$$+ \left[\frac{0.6}{(2 * pi * f)^2} * L1\right] = 300fF$$

$$C4 = \left[\frac{1}{34.22 * f * R}\right]\left[0.9988 + \frac{0.914}{Ql} - \frac{1.03}{(Ql)^2}\right] + \left[\frac{0.6}{(2 * pi * f)^2} * L1\right] = 132fF$$

$$L3 = Ql * \frac{R}{(2 * pi * f)} = 52u$$

we derive the values for the passive elements that model the waveforms of current and voltage to be purely non overlapping.

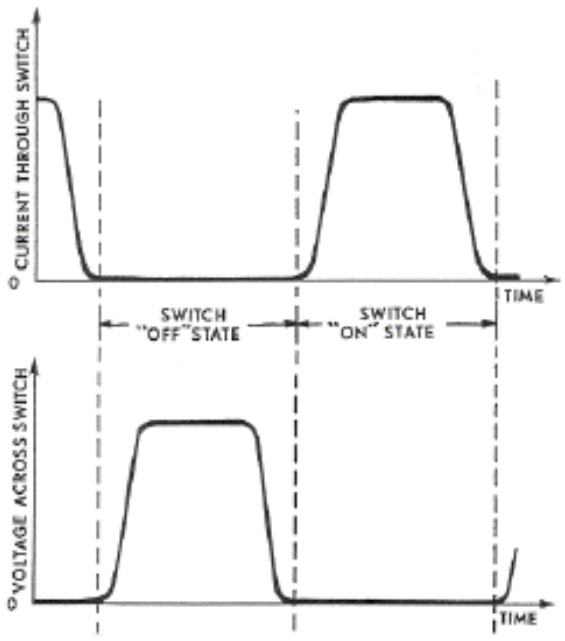

Fig 28: Expected waveforms

STEP 4: The transistor sizes are determined to keep the Ron low and at the same time support the equations in deriving the non-overlapping circuits.

An low Ron is picked to satisfy the QL requirement

$$\boldsymbol{Rs = \frac{Rp}{1+Q^2} \rightarrow Rs < 200\ ohms}$$

With minimum channel length of 180 nm, a width of 30u gives us a on-resistance of 170 Ohms.

STEP 5: A pi- match is used to convert the antenna impedance of 50 ohms to 36K at the output of the class E stage. This is achieved using a Pi-match.

We Derive the values of Ls' and Cs' for the Pi-match as following:

$$\boldsymbol{XChoke = 16K \rightarrow BFL(L4) = \frac{16K}{2 * pi * freq} = 12\ uH}$$

$$\boldsymbol{\omega^2 = \frac{1}{2 * pi * L * C} \rightarrow L * C = 6.9 * 10^{-18}}$$

$$\boldsymbol{Rp * Rs = \frac{L}{C} \rightarrow 50 * 25 = \frac{6.9 * 10^{-18}}{c^2} \rightarrow C1 = 37.3pF}$$

$$\boldsymbol{L1 = 0.184uH, C2 = 2.6pF, L2 = 2.7uH}$$

Observed waveforms:

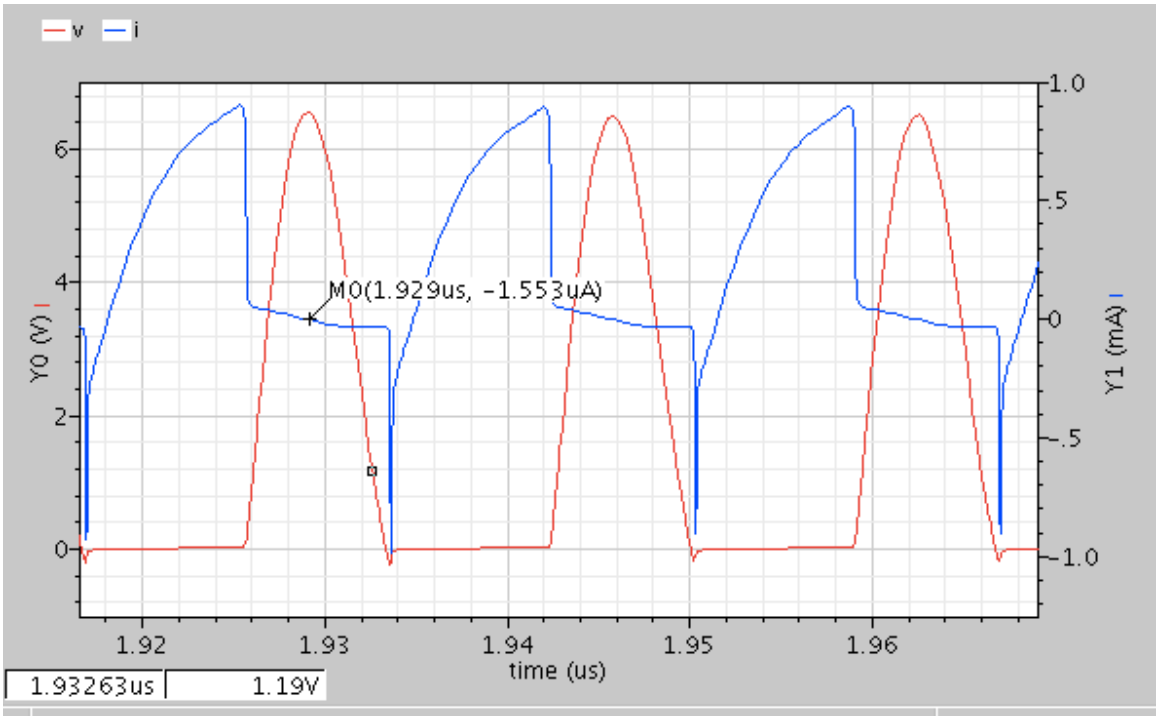

Fig 29: V & I non-overlap waveforms for class E

Voltage and current waveforms at the Drain of the FET

As expected, we see very small overlap between the current and the voltage waveforms at the drain, and changing the values of L3, C3 and C4 can control the waveform shape.

NOTE: It looks like the waveform above has an over lap part, but that is just due to the negative current glitch. The current is 0 when the voltage is positive and vice versa.

RESULTS AND DISCUSSION

Power gain:

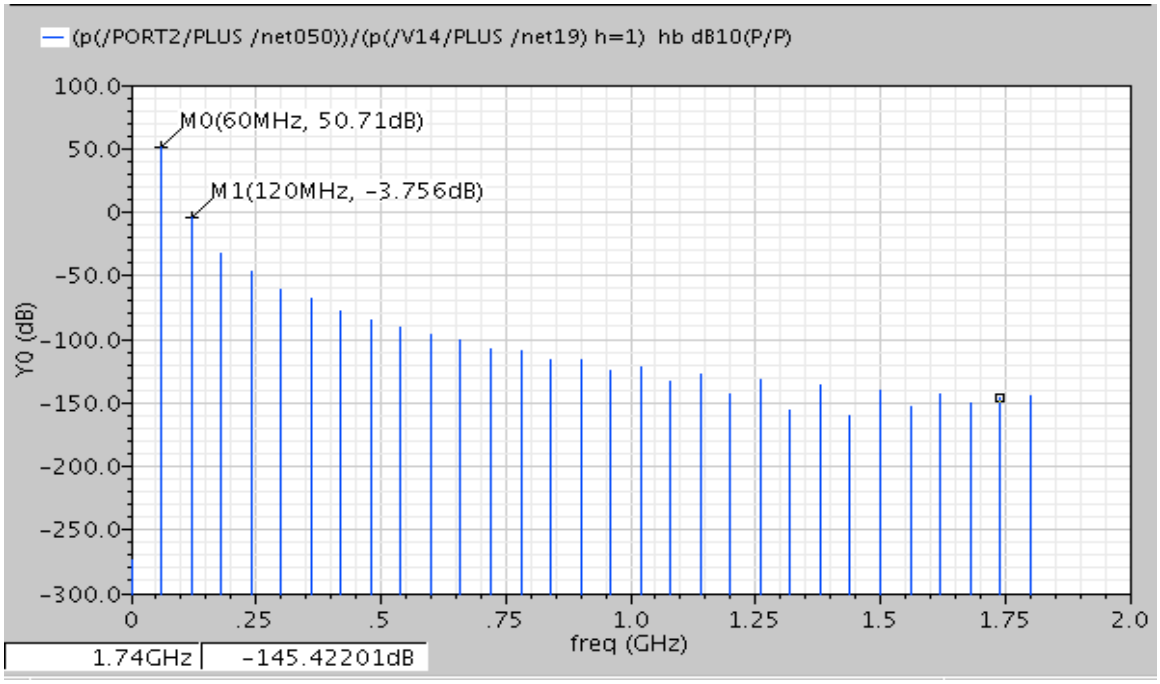

Fig30: Power gain for class A

Output power: As expected from the hand design, the **output power = -5dBm**

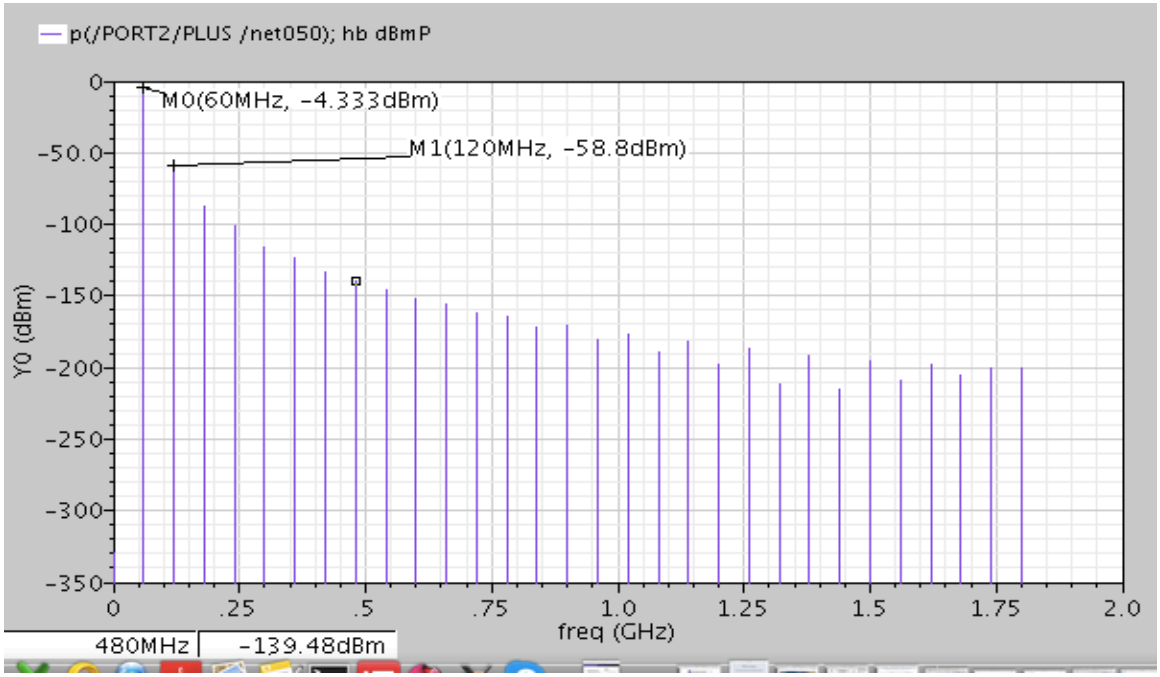

Fig 31: output power levels

Efficiency:

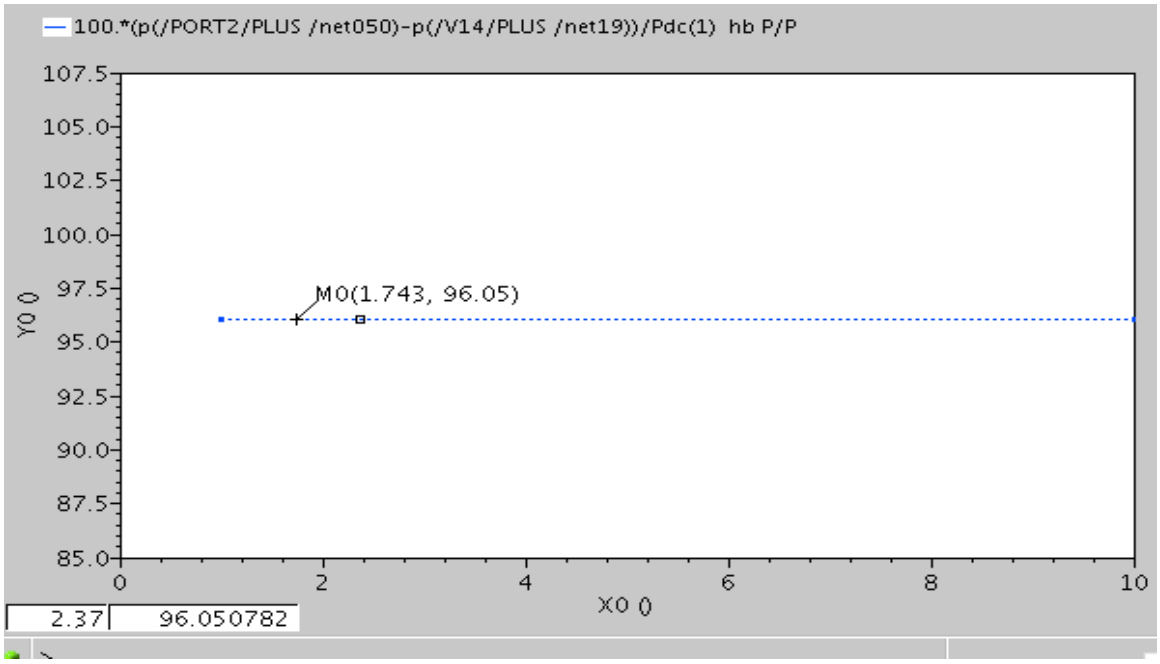

Fig 32:Efficiency of the PA

THE OBSERVED EFFICIENCY IS 96%, close to the ideal 100%

Output voltage:

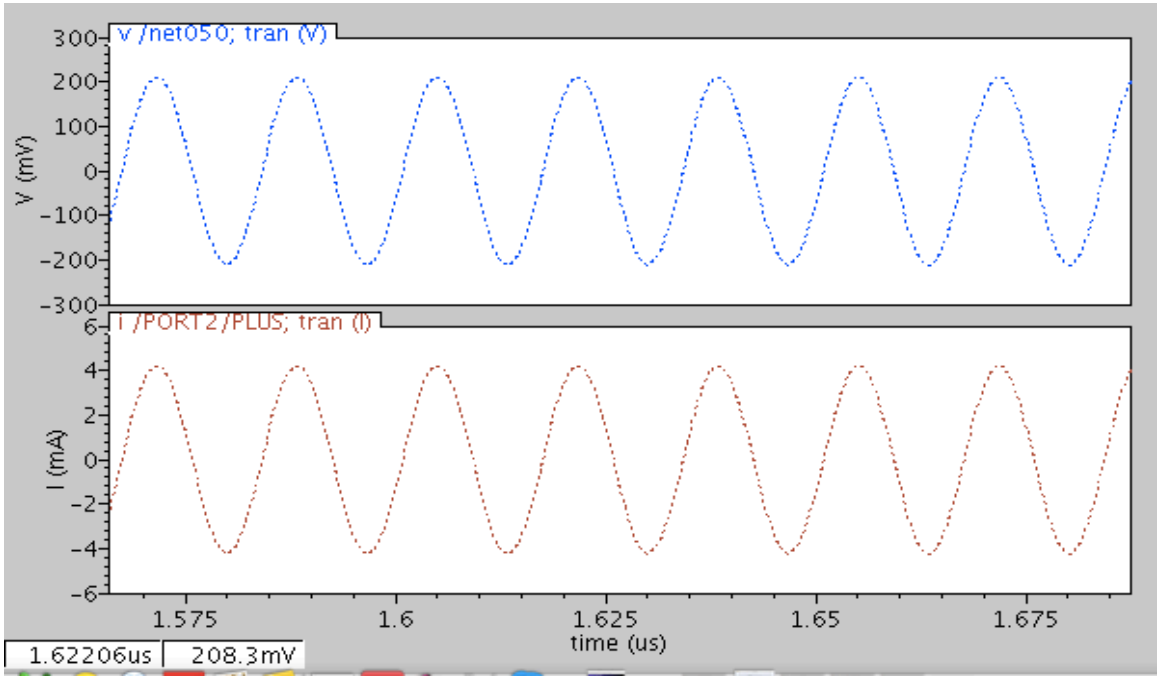

Fig 33:V & I waveforms at the output port

NOTE:

The values of inductors used in this design are fairly large, mainly due to the low frequency of operation. The passives are all designed assuming a quality factor of 20. Thus class D proves to be a more plausible design to be integrated on chip.

Section IV: Conclusion

CLASS	Efficiency	Output power (dBm)	SFDR (dB)	Power-Gain(dB)
A	5%	-10	29	24
D	89%	-7	93	45
E	96%	-5	54	50

TABLE: Achieved results for classes A,D & E power amplifiers

From the derivations and design constraints, a class D & E power amplifiers are a fair choice and prove efficient operation .It can be observed that the hand analysis mostly agrees with the simulated results. Further, this block is to be integrated with signal processing unit that outputs an FSK signal into the Power amplifier, which transmits data through the antenna with minimal loss. The next steps for this block would be top-level integration on a schematic and a layout level, followed by simulating the schematic and the layout of the entire chain of blocks. This validated design will then be taped-out /sent to the foundry for fabrication.

Works Cited

[1] Nathan O. Sokal (1981) IEEE life fellow design automation, inc: "*Class-e high-efficiency rf/microwave power amplifiers: principles of operation, design procedures, and experimental verification*" retrieved February 1981 from: http://www.cs.berkeley.edu/~culler/AIIT/papers/radio/Sokal%20AACD5-poweramps.pdf

[2] N.O.Sokal and A.D.Sokal (1975),"Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 168–176, Jun. 1975. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1050582

[3] Ali.M.Niknejad (2014): RFIC, UC Berkeley; EE242B, retrieved fall 2014 from: http://rfic.eecs.berkeley.edu/ee242/lectures.html

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[6] King-Chun Tsai(2007 February), Ph.d. dissertation "*cmos power amplifiers for wireless communication*" retrieved February 2007 from: http://www.eecs.berkeley.edu/Pubs/TechRpts/2007/EECS-2007-161.html

IV. Consolidated Paper: System Summary

This chapter of the report will provide the summary of the system level integration and performance of the receiver and transmitter. This chapter will provide a summary of the oscillator, comparator, power amplifier, and buffer blocks.

Oscillator

The function of oscillator in a transceiver system is to create a constant high frequency signal to carry the information signal. In a transmitter system, the oscillator output modulates the information signal, and the power amplifier amplifies the signal to be transmitted afterwards. In the receiver chain, the oscillator and envelope detector demodulates the transmitted signal and then sends it to comparator for decoding. The oscillator in this system is designed as a MEMS-based oscillator, where the MEMS device is used as a resonator to replace the crystal that is used in traditional oscillators. The advantage of the MEMS-based oscillator is that it provides high Q to have a more accurate channel selection, and the simple design also contributes to low power consumption.

Oscillators typically consume the majority of power in the receive chain. Therefore, the topology of the oscillator determines the power consumption of whole system at some degree. Based on the low power consumption specification, the Pierce oscillator schematic, which consumes relatively low power, is being used. The schematic is shown below in Figure 1:

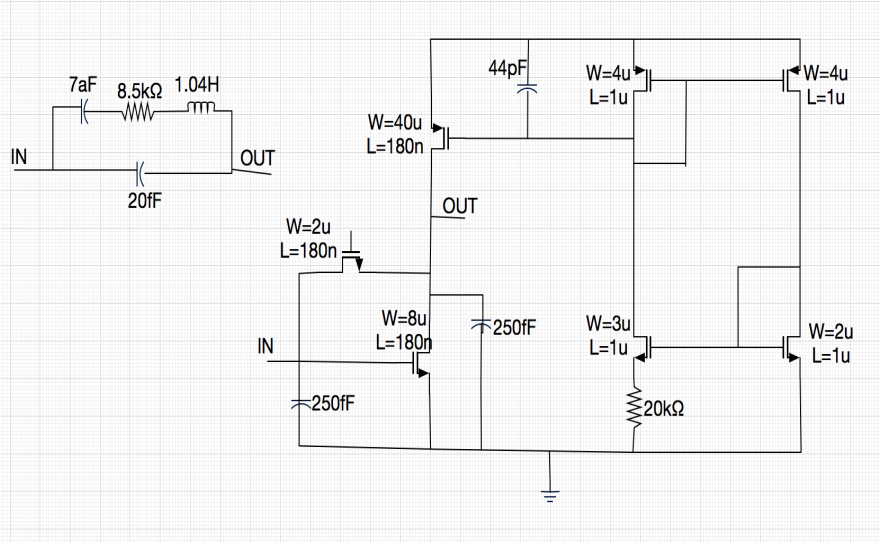


Figure 1: Pierce Oscillator

The feedback loop of this oscillator has a phase shift of 360°, and in order to make it oscillate, we also need to design for a negative resistance greater than 8.5kΩ looking into two ports of resonator. Since positive resistance consumes power, we can regard negative resistance as an energy source. If this "energy source" provides energy larger than the power consumption of resistor in the resonator, then this oscillator can work well.

According to the equation of negative resistance:

$$\mathrm{Re}(Z_c) = -\frac{g_m C_1 C_2}{(g_m C_3)^2 + w^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2}$$

In the circuit shown in Figure 1, the nodes "IN" and "OUT" link with the MEMS device by bond pad connection, and we assume the parasitic capacitance on the bond pad is around 250fF. The trans conductance of the common source amplifier is 165.68uA/V, and the value of negative resistance is 13.66kΩ.

The output waveform and power consumption is shown below in Figure 2 and Figure 3.

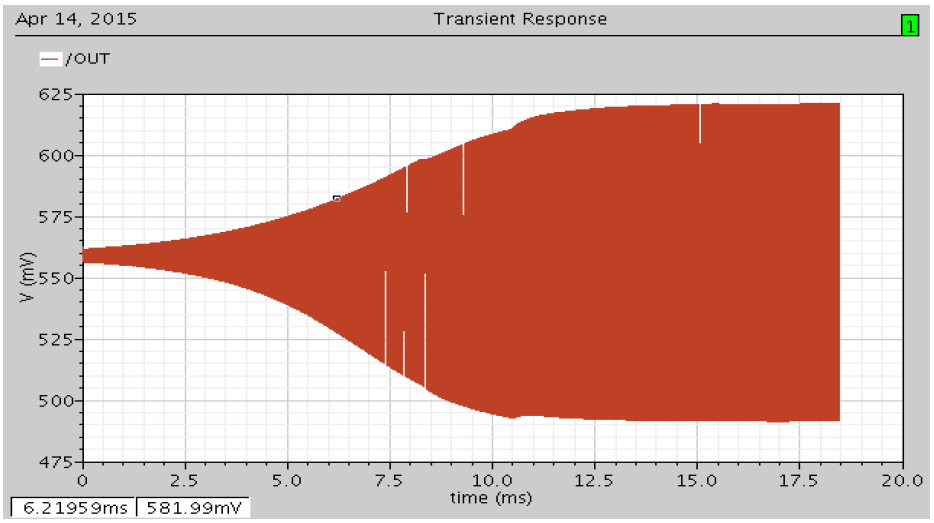


Figure 2: Growing Waveform Of The Oscillator

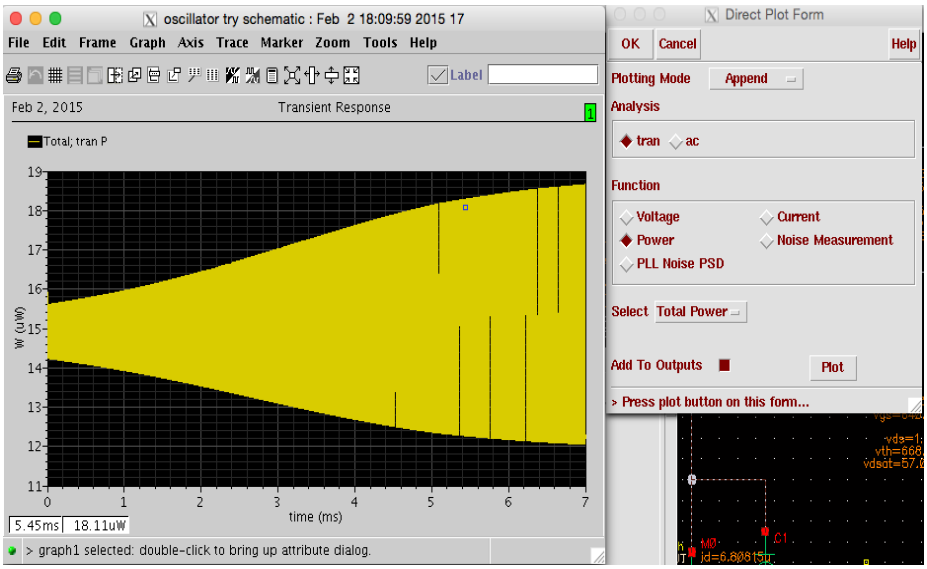


Figure 3: Power Consumption Of The Oscillator

The resonance frequency of 58.98MHz, and the amplitude is 128mV. The power consumption is 15uW.

The amplitude of the oscillator output in each period differentiates ‘1’ and ‘0’. The simulation required different stimulating signals to generate the different growing speed. Further, the oscillator required a reset to toggle a ‘0’ in simulation .The reset to the oscillator was generated

by switching the resonator resistance to a much higher resistance to destroy the quality factor. The stimulating circuit with a reset is shown in Figure 4.

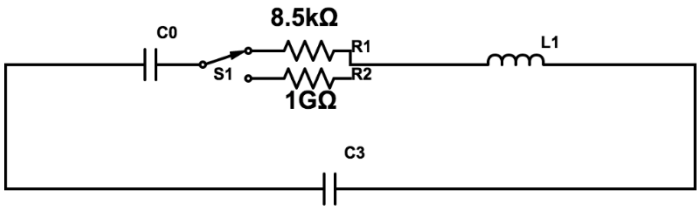


Figure 4. Stimulating Circuit

R1 corresponds to the working state, and R2 corresponds to resetting state. When the circuit switches to R2, the high resistance destroys the quality factor so that the oscillator can no longer work. The switch S1 is set to be periodically switches between R1 and R2. The output waveform is shown below in Figure 5.

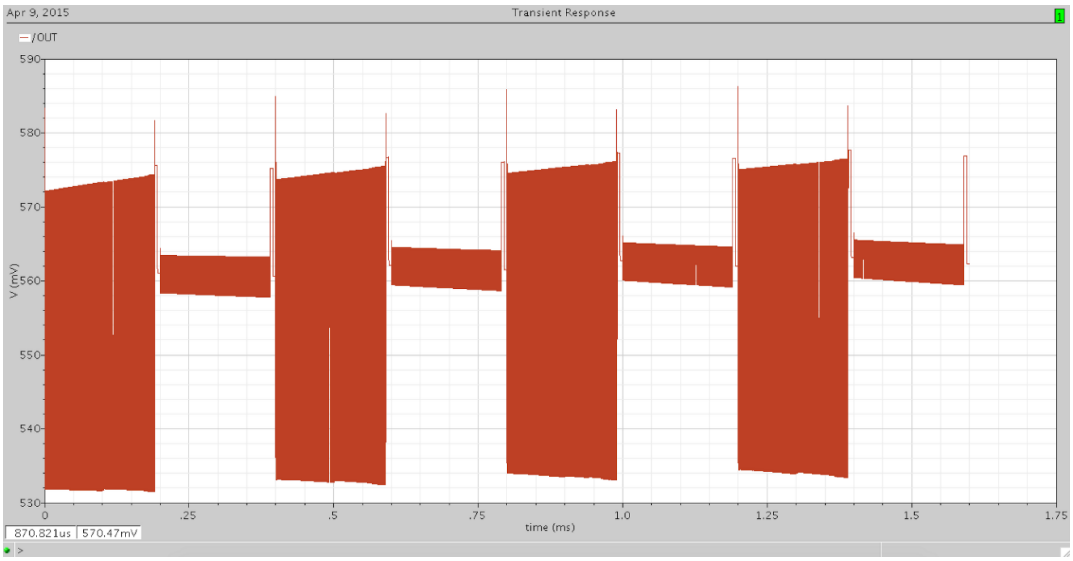


Figure 5. Output Waveform of Oscillator

In addition, an FSK signal is needed on the transmitter side. The method to generate an FSK signal is to switch the value of capacitance between two values. 7aF capacitance was used to generate 59MHz signal, and 6.5aF capacitance to generate 61MHz signal. The MEMS resonator model is shown below in Figure 6:

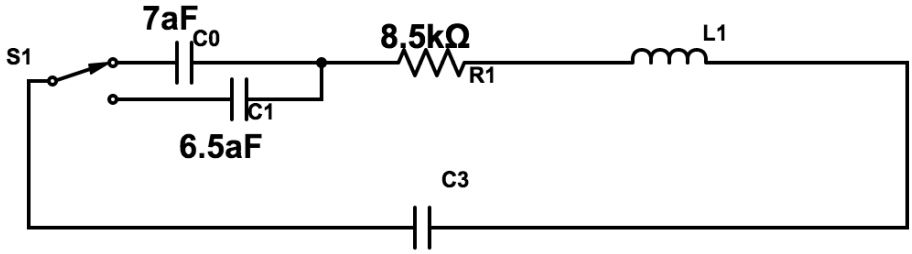


Figure 6. MEMS Resonator Model

Design Specification	Value
Resonance frequency	58.9MHz
Power Consumption	15uW

Envelope Detector

The envelope detector designed is a key piece of the transceiver system because it serves to detect the information stored in the envelope of wireless signals. In order to bias the envelope detector circuit into a temperature stable state of operation, a temperature independent current source was implemented. This temperature independent current source was also taken advantage of by the oscillator and the buffer circuits.

The design of the envelope detector had several key specifications. The consumption of the envelope detector was limited to several nW. Second, the envelope detector needed to be able to measure amplitude variations as small as several microvolts with good carrier rejection. Lastly, the envelope detector needed to be temperature independent because any variation to the bias level of the circuit will affect the threshold level of the comparator block.

Classic envelope detectors are simple to design because they require a basic diode and low pass filter circuit. However, to meet the specifications laid out above, the envelope detector used in this system needed to be based off an entirely different architecture. The main issue

with using the classic diode detector with low pass filter circuit configuration, as highlighted in [2], is the need for a significant amount of gain to bring the radio frequency amplitude above the turn on voltage of the diode. The high gain required in the classic diode detector is not suitable for our low power design. Many of the alternative envelope detector architectures capable of receiving low radio signals consumed far too much power. In [3], an operational trans conductance amplifier (OTA) based envelope detector can demodulate signals as low as 257mV while consuming 6.3mW of power. In [4], [5] and [6], differential envelope detectors capable of receiving RF as low as 5mV consumed 20μW, 10μW and 1μW respectively.

The envelope detector implemented in this transceiver was designed with 180nm TSMC process. The design implemented a single ended source follower stage with low bandwidth to filter out the carrier. A PMOS biased in the triode region is used in the output stage for capacitive low pass filtering. A copy of the input branch is also used to supply the DC bias voltage as a reference voltage for the comparator. The final envelope detector, shown in Figure 22, is capable of recovering signals with amplitudes as low as 2mVpp. Overall, the envelope detector consumed 167.1nW of power.

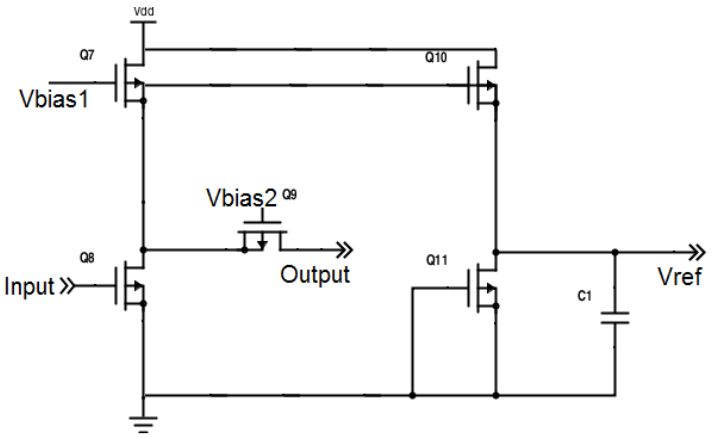


Figure 7. Single Ended Source Follower Envelope Detector

The noise equivalent circuit used for the hand calculations is shown in Figure 8. The noise simulation plots verifying the hand calculation is shown in Figure 9. From the equation below,

the minimum detectable signal with a nominal noise figure (NF) and signal-to-noise ratio (SNR) requirement is

$$Min\ Det.\ Signal = Noise\ Floor + 10log(BW) + NF + SNR$$

$$Min\ Det.\ Signal = -53.9dBm$$

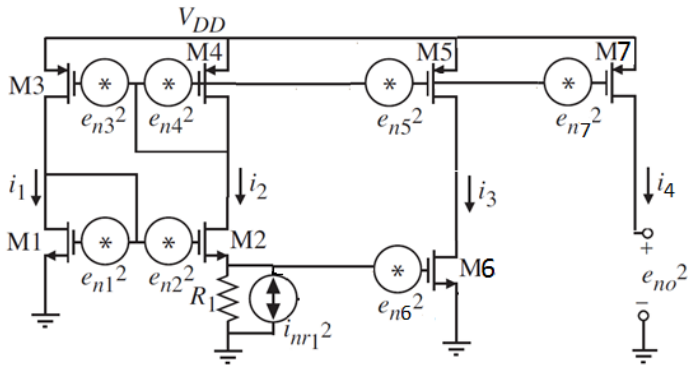


Figure 8. Noise Equivalent Circuit

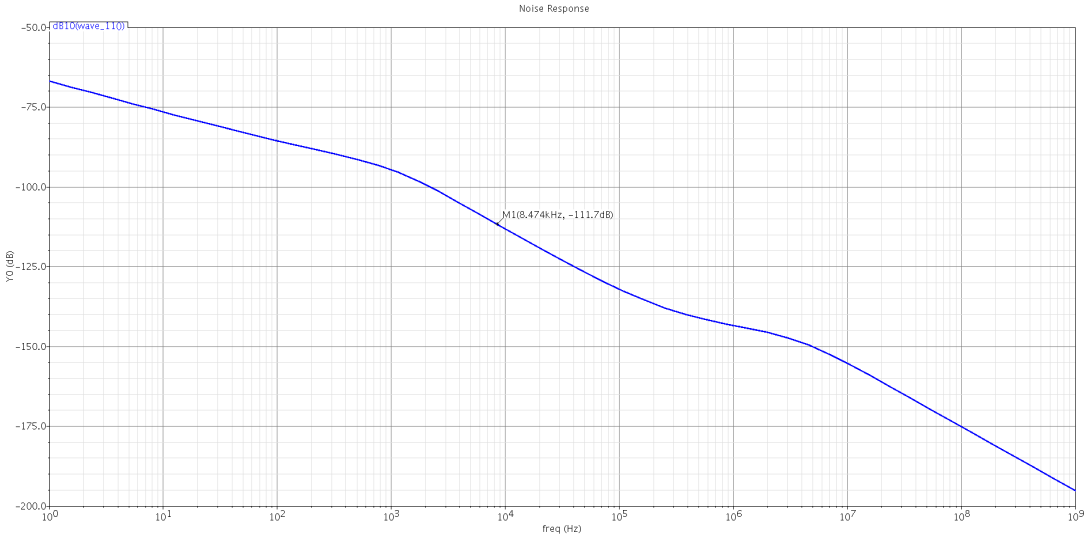


Figure 9. Noise Plot

Therefore, the minimum detectable is 2mVpp. The simulation proving the ability to demodulate signals with 2mVpp amplitude is shown in Figure 10. On the other end of the spectrum, the maximum amplitude the envelope detector can detect before clipping is simulated to be 1V. Therefore, the dynamic range of this block is

$$0dBm - (-53.9dBM) = 53.9dB.$$

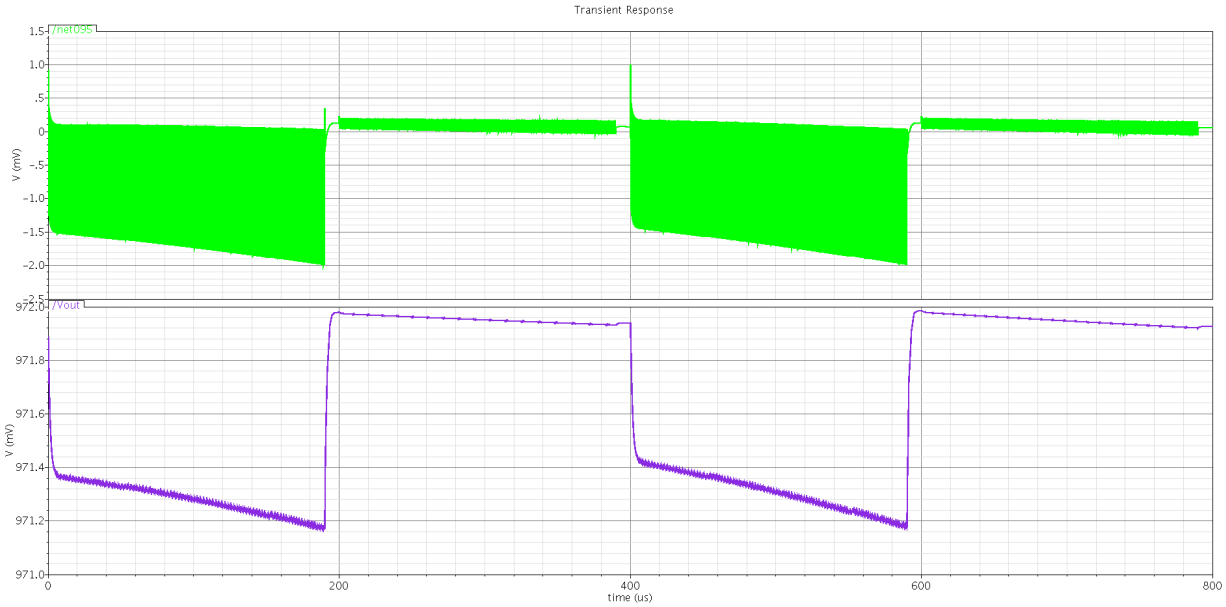


Figure 10. Minimum Detectable Signal

The envelope detector discussed was biased with 83nA of current and required stable reference supply. The design of the reference followed the methodology proposed in [7], which discusses a stable bandgap reference. The final design of the current reference is shown in Figure 11 and is capable of supplying 83nA of current with a 0.3% variation across the 0°C to 70°C temperature range. This stability was achieved by cancelling the temperature dependence of the resistor in the circuit with a diode connected NMOS transistor in parallel. The low current supply was achieved using maximum long channel devices in 180nm TSMC transistors.

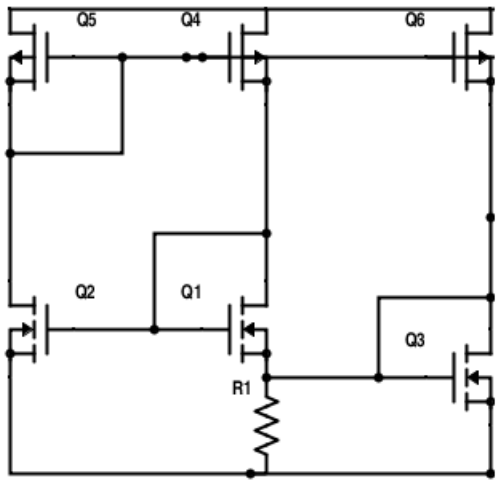


Figure 11. Temperature Independent Current Reference

The final design of the envelope detector with current reference is shown in Figure 12.

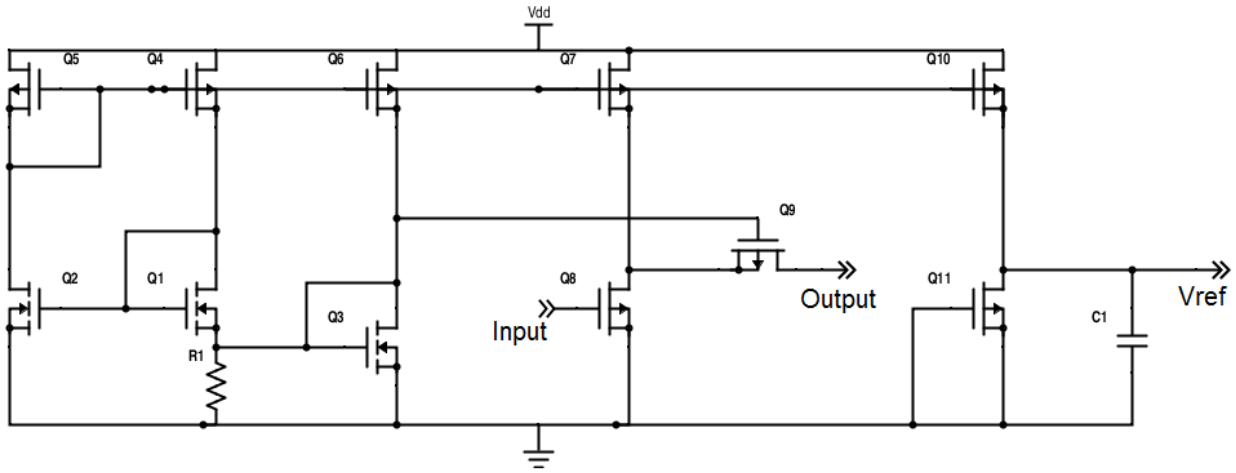


Figure 12. Envelope Detector and Current Reference

As part of the integration process, the layout of the envelope detector, current reference and the oscillator was designed. The layout is shown in Figure 7 with a die area of 750um^2.

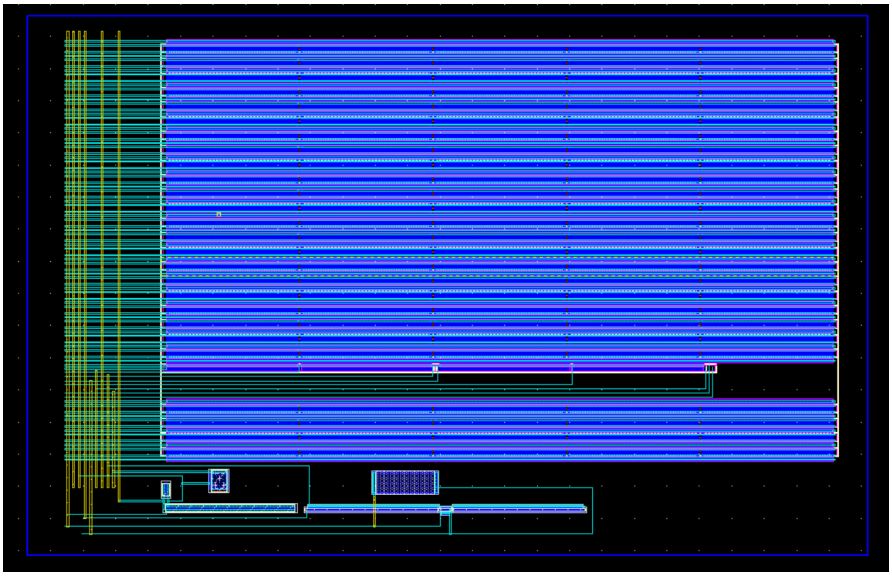


Figure 13. Layout of Oscillator, Current Supply, and Envelope Detector

Block Summary	
Envelope Detector	
Minimum Detectable Signal	2mVpp
Dynamic Range	53.9dB
Envelope Delay	.5us
Envelope Bandwidth	1MHz
Carrier Bandwidth	500MHz
Total Power Consumption	167.1nW
Current Reference	
DC Current 0°C	83.21nA
DC Current 25°C	83.55nA
DC Current 70°C	83.89nA
Total Power Consumption	250.6nW
Layout	
Die Size (Oscillator, Envelope Detector, Current Source)	750um^2

Comparator

When Frequency Shift Keying (FSK) modulated signals enter the transceiver, they give rise to the periodically restarted oscillations [1]. When the oscillation envelope is detected, the comparator should be able to discriminate “0”s and “1”s [1].

The schematic for the comparator is shown below in Figure 14.

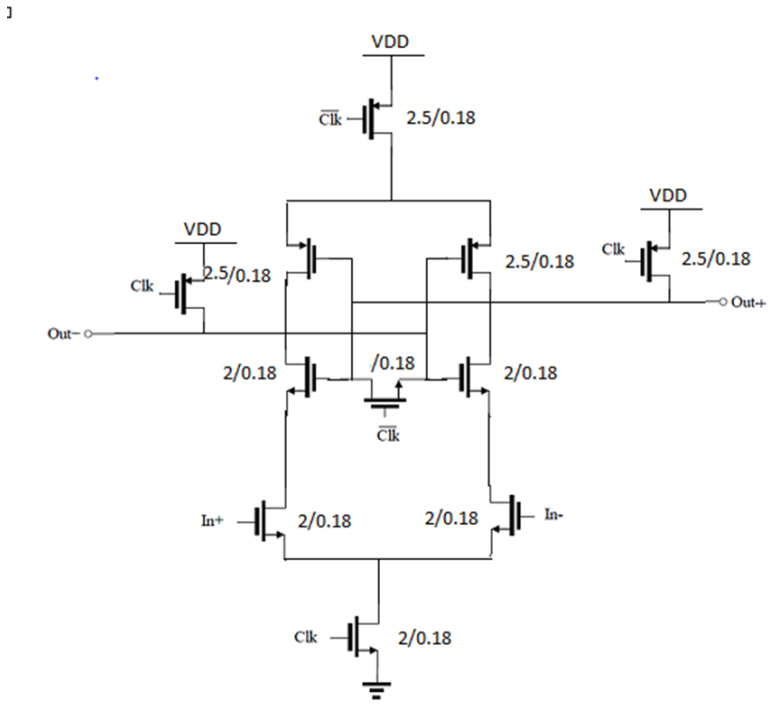


Figure 14. Comparator Schematic

The benefit of this design is that in the reset phase, when the clock signal is low, voltage supply and ground are disconnected from the latch. Therefore, no power consumption occurs in this phase. Since digital circuits normally only accept supply voltage and ground voltage as “1”s and “0”s, a PMOS pair was added to pull the output to supply voltage. During the evaluation phase, when the clock signal is high, the comparator is powered and starts to compare the input signals at the “In+” and “In-” terminals. The latch circuit grows the input difference and finally reflects either “1” or “0” at the output terminal.

The functionality of the comparator is confirmed with Figure 15. The first plot is the input signal, the second one is the clock signal and the third one is the output signal. The test signal was a sinusoidal wave with 1mV amplitude at 800mV DC level. The reference voltage used to

discriminate the “0” and “1” was 800mV. From the output signal plot, it is shown that when the clock is on, if the input signal is above 800mV, the output is “1”; vice versa.

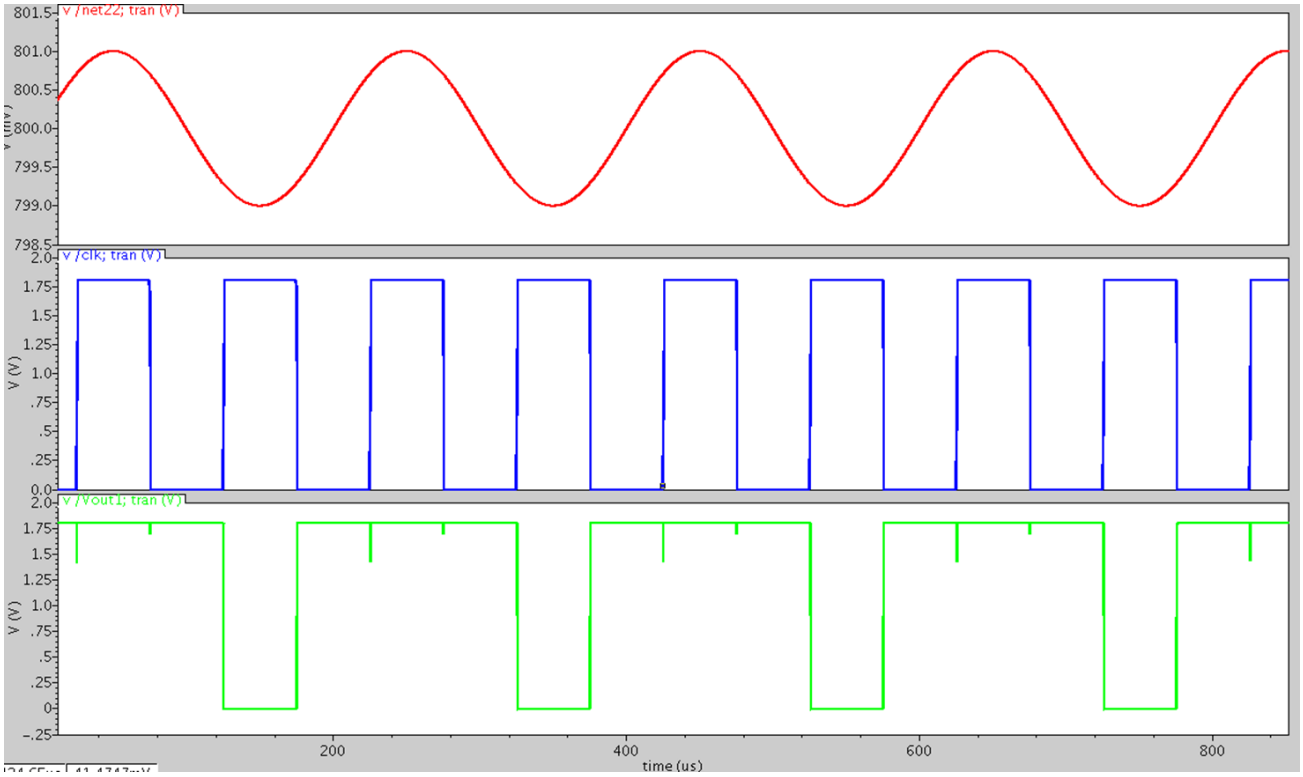


Figure 15. Comparator Functionality

This comparator circuit consumes 237nW of power, which fits our team’s purpose of building an ultra-low power transceiver.

Complete Receiver Chain

The schematic for the complete receiver chain, which consists of the oscillator, the envelope detector, and the comparator, is shown in Figure 16.

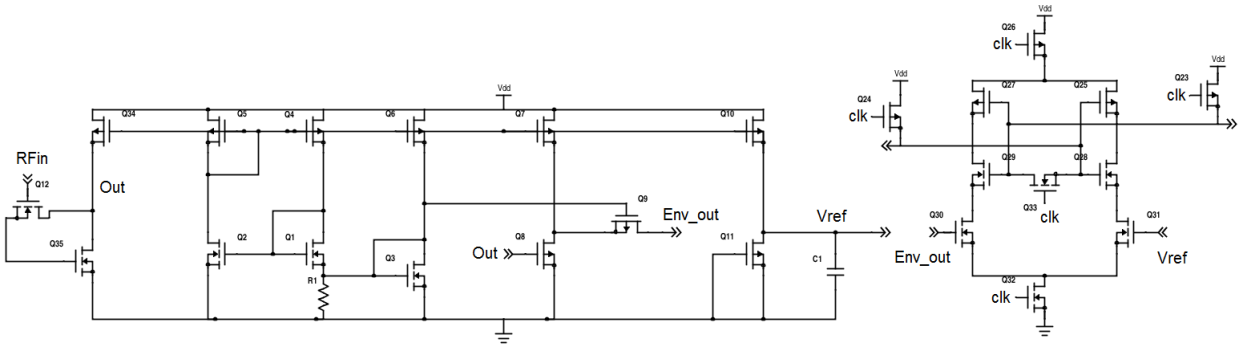


Figure 16. Receiver Chain

The capstone team verified the functionality of the receiver chain by inputting a test 1010 signal that is generated by the oscillator. The results of the simulation are shown in Figure 17. As shown, the green signal is the generated 1010 signal from the oscillator. The purple square wave is the output of the envelope detector and as expected, it is the negative envelope of the input oscillator signal. The dc purple signal represents the reference voltage that the comparator uses to determine the received bits. For envelope amplitudes below the reference level, the comparator will clock a 1 and for envelope amplitudes above the reference level, the comparator will clock a 0. The red signal represents the clock signal. The blue signal represents the output of the comparator. An output synchronous flip flop that is edge triggered by the clock shown will latch a 1010, as expected.

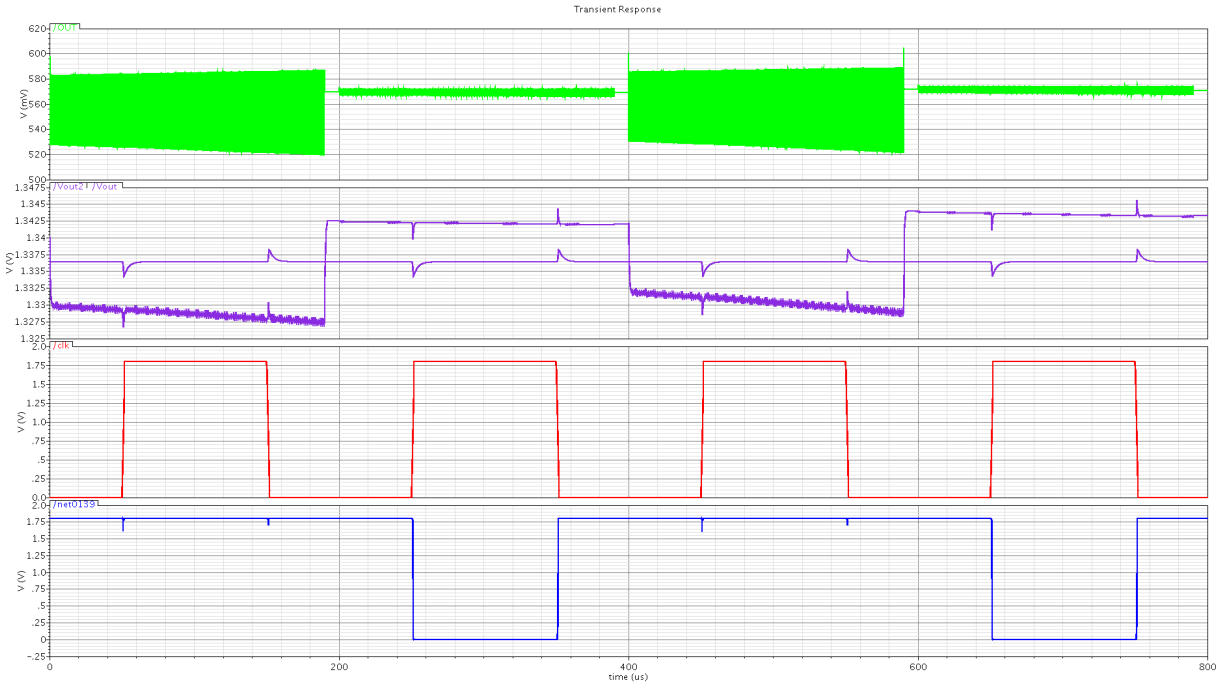


Figure 17. Verification of Receiver

Power Amplifier

This part of the paper summarizes the design of a Power amplifier (PA) for the transmitter part of the system. This block functions to establish connections and send information from the digital system to the external world.

Given the fact that reducing the power consumption is the overall goal of this project, the power consumed by the individual blocks must also be minimized. This translates to the concept of power efficiency, meaning 'the amount of power used to generate and transmit a decodable burst of data from the system'. The major trade off for efficiency is a characteristic called linearity. Linearity defines 'the relationship between the output and the input, and the change in output for a given change in the input level'. Below is a table of the performance statistics of each of the power amplifier classes available.

CLASS	A	B	C	D	E
Theoretical efficiency	50%	78.5%	80%	100%	100%
Linearity	Linear	Non-linear	Non-linear	Non-linear	Non-linear

Since efficiency is our major consideration in this system, a class D amplifier was used. This choice was made after surveying highly efficient PA's in papers written in [8] and [9]. The other requirements needed for proper operation of the PA block include current bias generation, voltage bias at the input, and inclusion of passives.

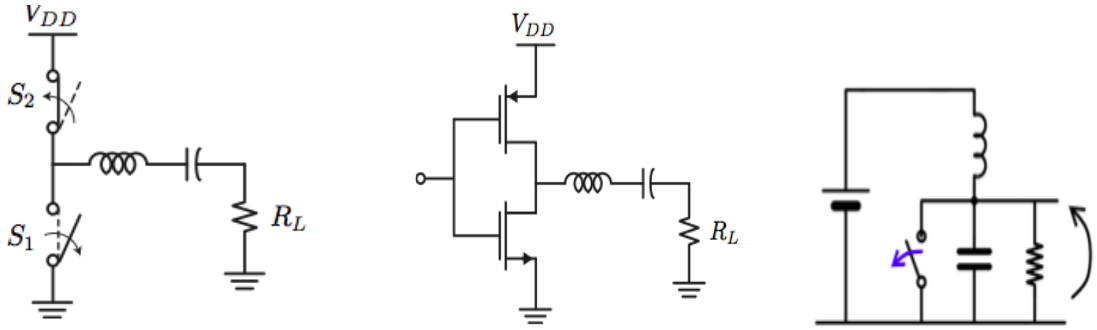


Figure 18. Class D & E Amplifier models [10]

From the above table, class D and class E amplifiers can be theoretically characterized as having an efficiency of 100% [10], this is because they don't allow for any dissipation of energy within the system, thus translating all of its energy to the required output load, which is an antenna used for transmission in most cases.

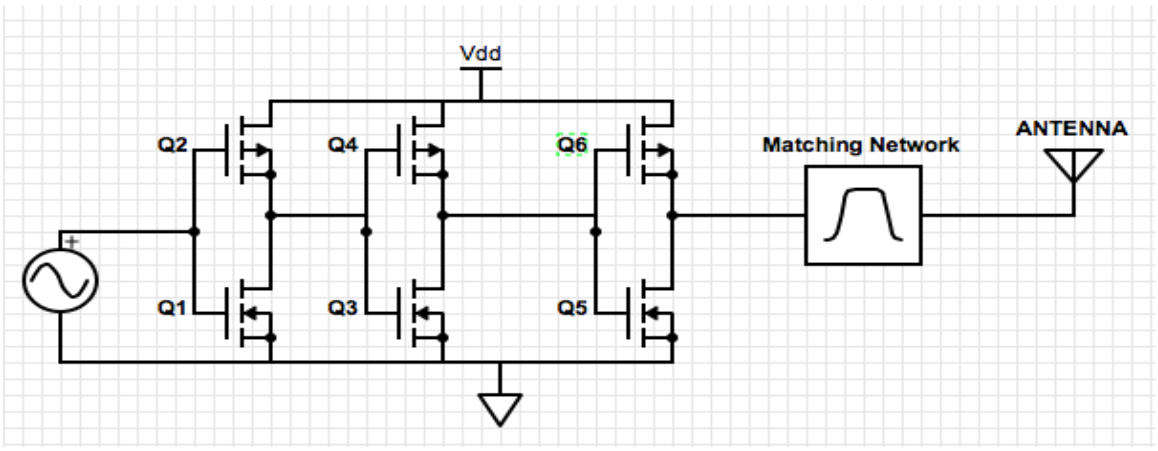


Figure 19. Architecture of the Power Amplifier

The control over power transmitted to the load depends on the impedance (resistance) of the load seen by the output node of the amplifier. In order to meet the specification of the power drawn by the load precisely, this load seen by the output node has to be transformed to a different value. This process of transforming the load can be done by using a network called 'matching network' to match the output node to the impedance needed for maximum power transfer. For this power amplifier, a T-match was employed because it isolates the DC component and the AC component – which is of our interest at the output node and also provides the impedance transformation needed. The final schematic of the power amplifier is shown in Figure 20.

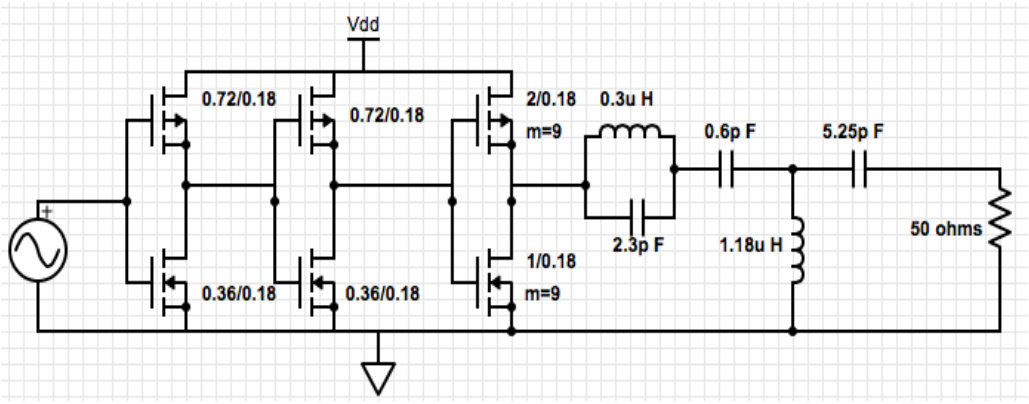


Figure 20. Power Amplifier Schematic

The layout of the power amplifier is shown in Figure 21.

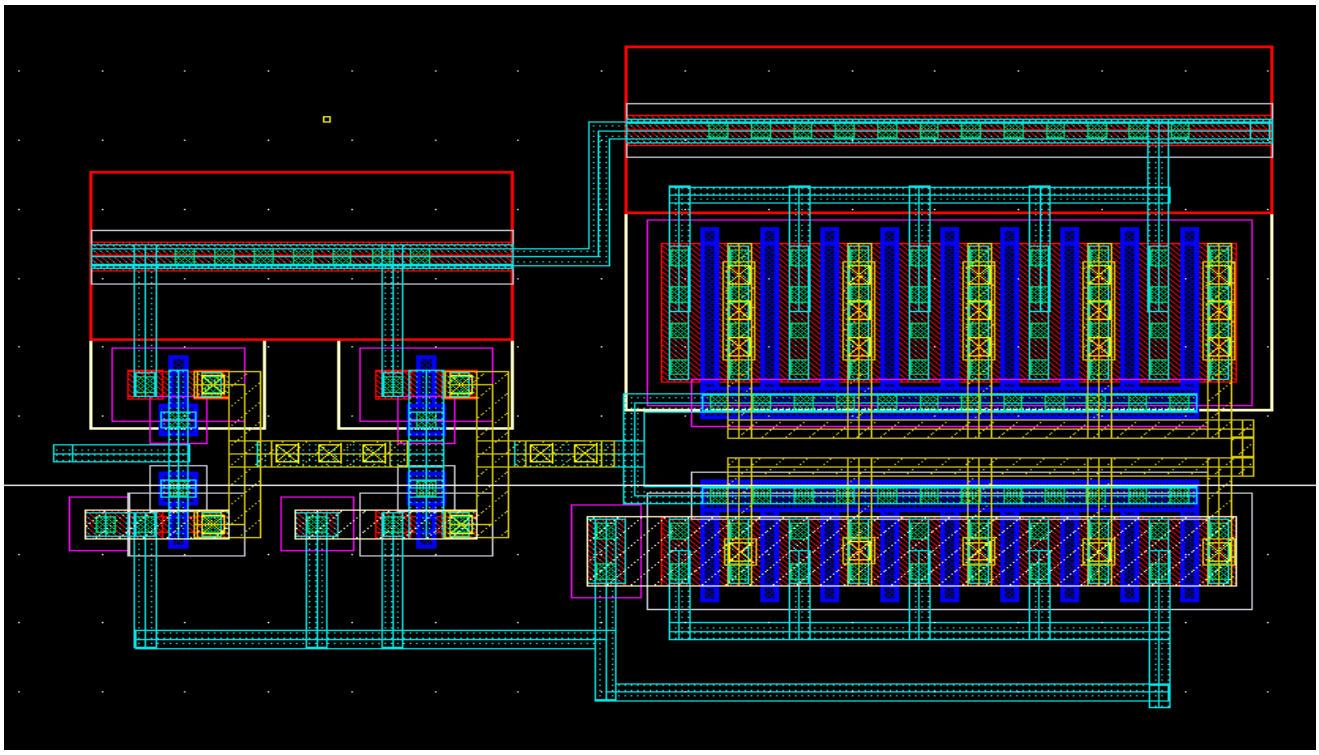


Figure 21. Power Amplifier Layout

Following waveforms show the simulated results for the various performance metrics.

POWER-GAIN & OUTPUT WAVEFORMS: The reported power gain is 47 dB at the fundamental frequency. Waveforms below depict the voltage and current waveforms at the port or the virtual antenna. We can see that the waveforms are purely sinusoidal.

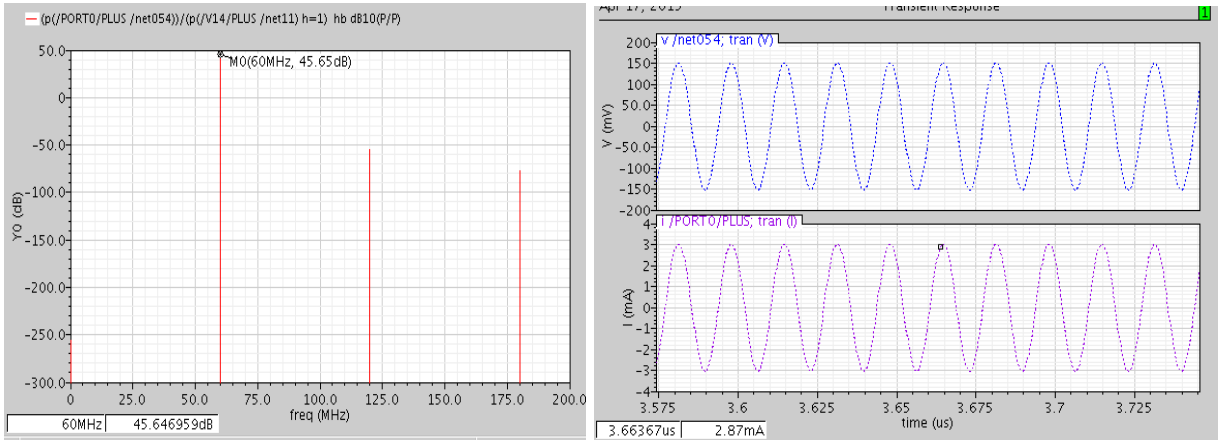


Figure 22: measured power gain & simulated output waveforms

POWER: The first plot shows the power levels without the L–match filtering at the port. The second plot shows the power levels with both the L-match filtering at the port and 3rd harmonic filtering. We see that harmonic power is high and can affect the efficiency.

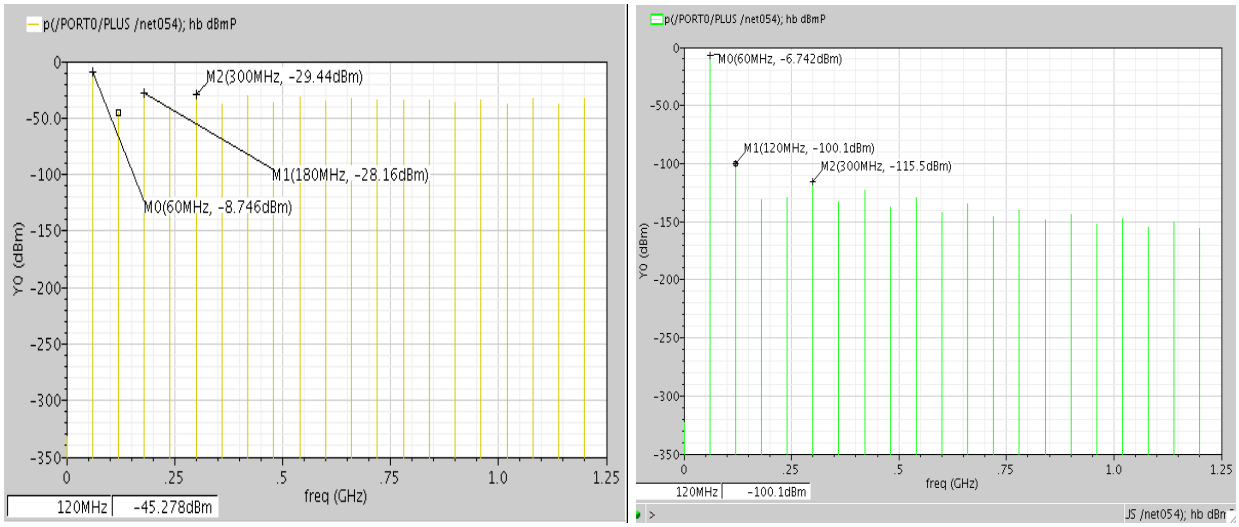


Figure 23: Power without the L- match filtering

Match type	L(uH)	C1(pF)	C2 (pF)	C-Block	Max eff	Power (dBm)	Drawback
pi	0.184	41.5	371	1.2pF	89%	-3.5	Needs dc-block
T+3wo filter	1.18	0.587	5.25	-	86.5%	-7	No dc block needed
Pi+T filtering	1.18	0.587	5.25		89%	-7.2	Needs 3 inductors

Figure 24: Impedance calculated for different matches

EFFICIENCY: The reported efficiency is 88.35%.

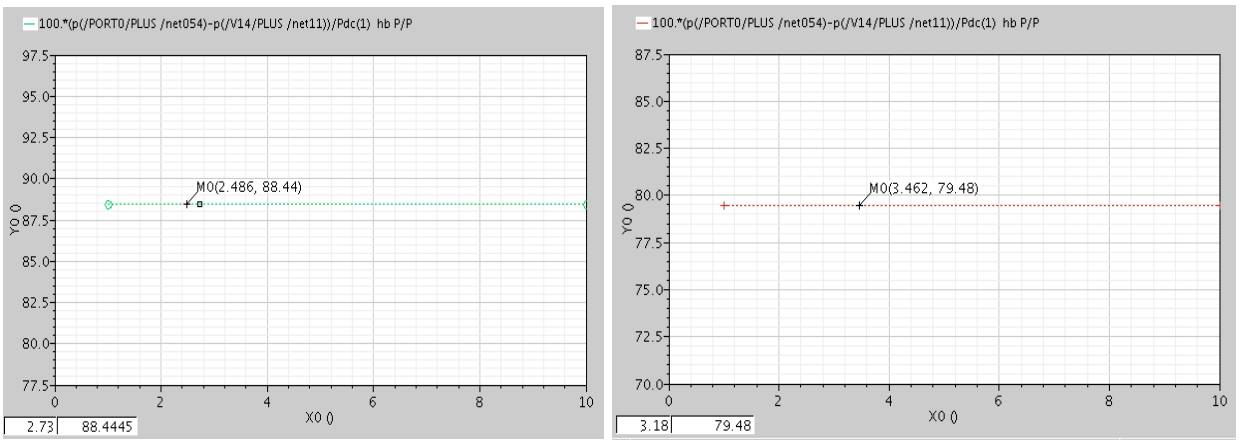


Figure 25: Measured efficiency with filtering & before harmonic "block network"

It is evident that the efficiency improves by 16%, by adding a third harmonic block.

DRAIN WAVEFORMS:

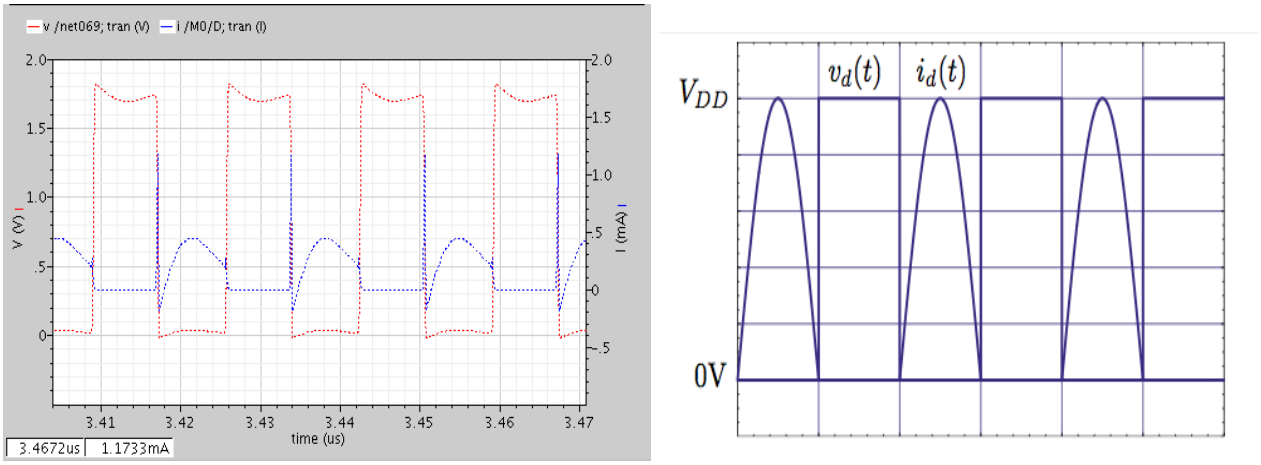


Figure 26: Drain waveforms Ideal class D output waveforms

The contributors for efficiency degradation are:

1- Harmonic dissipation: we see that the total harmonic power added from the second to 19th harmonic sums up to 1.2% after adding the 3rd harmonic filter.

2- Parasitic losses: The passive devices have a quality factor of 20.Therefore, the internal resistance of the components adds up to a loss of 2.4%.

3- $C * V\text{^}2 * f$ Losses: The input gate capacitance of the inverters is 1.5f F each and the amplification stage offers a gate cap of 31f F. This produces a loss of 6.722uW = 3.4 %

	Short circuit current	Harmonics	Passive parasitics	Driver $C * V\text{^}2 * f$	Total loss
loss	6.4%	1.2%	2.4%	3.4%	13.4%

Figure 27: Loss contributors

Transmit Chain

The oscillator is integrated with the Power amplifier by connecting the output of the oscillator to the input of the PA. An input FSK is generated by the oscillator and given to the PA.

The plot below in Figure 28 shows how an input data stream is modulated and transmitted by the power amplifier into the antenna.

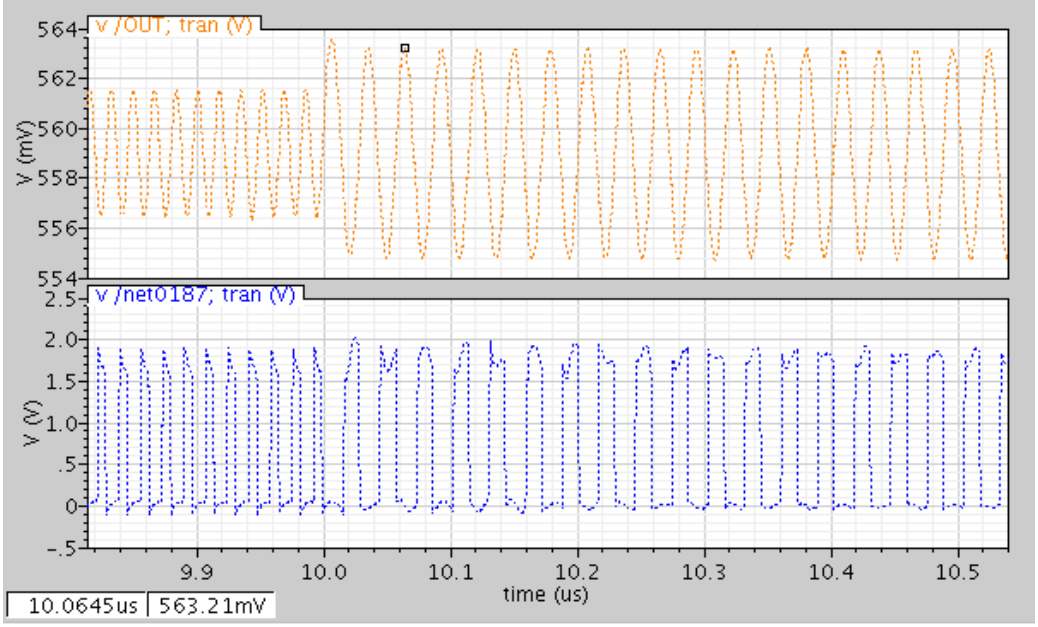


Figure 28. Transmit Waveform

Voltage Buffer

We require a voltage buffer to interface with the 50Ω transmission line required to test our chip. This voltage buffer has several design requirements. The most important is a voltage gain of 1 to accurately represent the input signal. Impedance matching at the output is necessary to ensure that the maximum available power from the input signal is delivered to the load. The buffer also requires high enough bandwidth, output voltage swing, and linearity to send signals to the output negligible distortion. The input signals of interest are the output signals of each block in the transceiver chain except the power amplifier; in general, these are a 60Mhz signal with 0.8V peak to peak (pk-pk) and a 5khz signal with 1.8Vpk-pk. A bandwidth requirement of 600Mhz is necessary to capture harmonics of the 60Mhz signal. Die area and power consumption will not be considered as primary design constraints. Since our project is currently focused on verifying functionality, cost and commercialization details are not concerns. Additionally, the buffer will connect a separate power rail from the rest of the transceiver to negate its power contribution during normal operation of the MEMS transceiver.

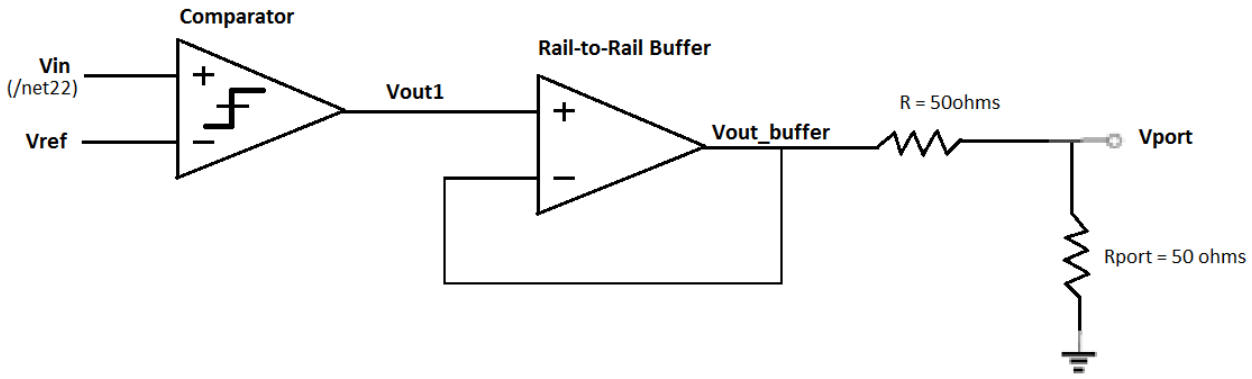
Given the design requirements presented, two different buffer topologies were implemented. A wideband buffer was designed for 60Mhz while a rail-to-rail buffer was designed for 5khz. For the purposes of this paper, which is to discuss the integration of the voltage buffer into the transceiver system, we encourage the reader to briefly refer to the summary of the performance of both buffers as given in the “Individual Technical Contributions” report for the voltage buffer. Details on the topologies, transistor sizes, design methodology, and test results of the buffers is discussed in more detail in that report.

The integration of the voltage buffer to the transceiver system required proper modeling of the interface between the buffer and the block being measured. The additional capacitance that would be added after attaching the buffer must be taken into consideration during design time for the measured block. The input PMOS device of the wideband buffers were sized to be

20um/180nm, which resulted in an input loading of ~10fF. Since the functionality of both the envelope detector and the oscillator already required large capacitances on the order of ~100fF at their outputs, this additional loading was not a concern. The integration of the comparator with the rail-to-rail buffer was more challenging; the input of this buffer had a PMOS device with size 36u/180nm in parallel with a NMOS device with size 12u/180nm, which summed to a significant capacitance. A redesign of the transistor sizes in the comparator was necessary. Figure 29 shows the schematic and resulting plots of a rail-to-rail buffer integrated with the redesigned comparator. As shown in part (b) of the figure, the output of the buffer follows the comparator's output up to its maximum voltage swing of 1.67V, which is the expected performance.

A different issue that needed to be resolved for the wideband buffers was being able to take in the input signal and display it accurately at the output. The ability for the buffer to do depended on its maximum input common mode range and the voltage range of the signal being monitored. Refer back to Figure 17 in the "Complete Receiver Chain" section for the the output signal of the oscillator and the envelope detector. The wideband buffer with a PMOS input pair can accept voltages between 200mV and 1V. This was acceptable for the oscillator, which after integration yielded a signal centered around 600mV and stayed within this range. However, another wideband buffer with an NMOS input pair needed to be implemented to monitor the output of the envelope detector. The new buffer with an common mode input range between 600mV and 1.4V can accept the signal at the envelope detector's output, which is centered around 1.2V. The resolution of the two issues described above allowed us to successfully integrate the voltage buffers with the blocks we are interested in measuring: the oscillator, the envelope detector, and the comparator.

(a)



(b)

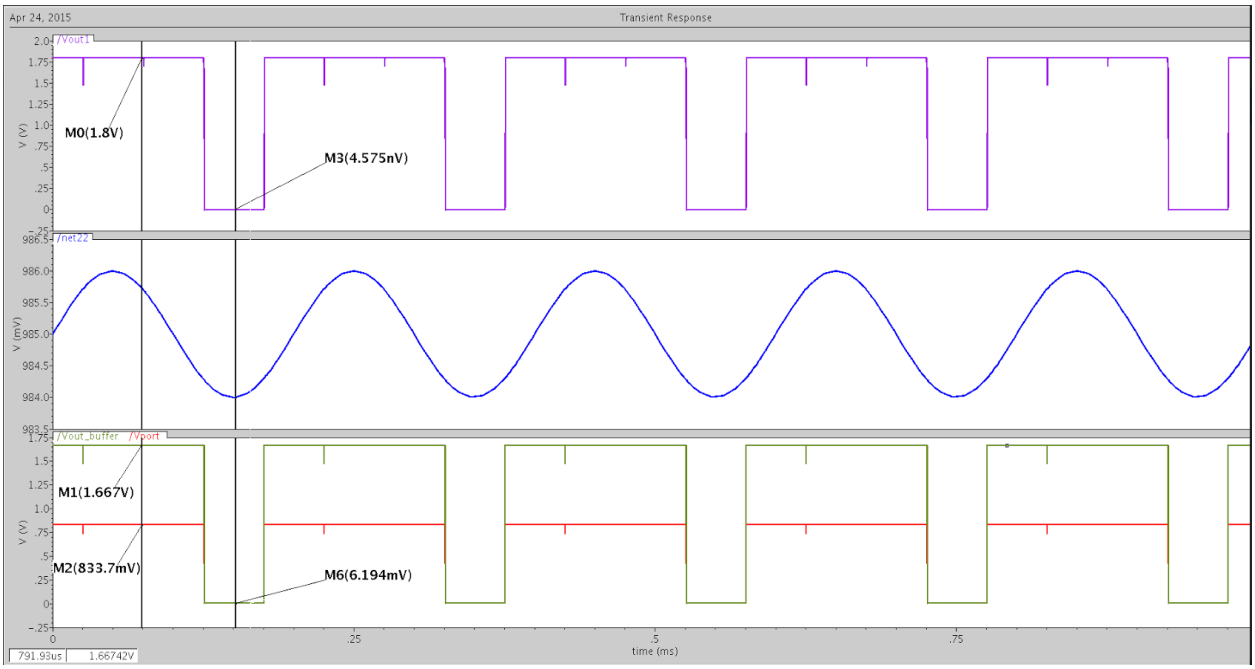


Figure 29: Test Setup (part a) and Transient Response (part b) for comparator and rail-to-rail buffer. Blue trace is the test signal (output of envelope detector), purple trace shows output of the comparator, green trace shows the output of the voltage buffer, and red signal shows the signal being sent to the load after matching.

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V. Concluding Reflections

This project on the whole was very insightful. The final aim of the project was to complete the design, layout and finish all test cases for the design with top-level integration of the system as a whole. The Entire system was chosen to follow a top down approach, where each block would go through several phases before being tagged complete. The phases would be listed as:

Schematic ➔ Pre layout simulations➔ Layout➔ Post Layout simulations➔ GDS

In the past I have always worked on the receiver part of the system which was one of the key reasons for me to pick the design of a power amplifier .It is the most crucial block in the transmit part of the system. Designing power Amplifiers was one of my goals that I had set for myself before I had joined as a graduate student ay UC. During the course of this project, I have designed three classes of power amplifiers, and compared them for their performance metrics. This experience is invaluable and I have gained confidence in designing power amplifiers and integrating them with the system.

Although we were supposed to complete all the phases from design, layout and post layout leading to a tape out with the foundry, we were able to complete our designs only till the layout phase. The main reasons for not accomplishing the initial goals we had set as a team include time management and technical knowledge. Most of the group didn't have the technical skills required to design their blocks and this led to slow progress throughout the first semester.

However, to compensate for the effort required by this project I have designed 3 classes of power amplifiers and simulated them for all the functional metrics. The layout was also completed for the class D power amplifier with successful passing of LVS and DRC rules. The class D power amplifier was also integrated with the oscillator to obtain an FSK output as required by the top level system.

The next step for this project would be to check the performance across PVT variations and freeze the GDS for a tape out with TSMC. If, the system works as expected on silicon, we could improve the data rate of the system so it could compete with high data rate technologies like Zigbee, Bluetooth and Wi-fi.