Efficient Switching Power Amplifiers using the Distributed Switch Architecture

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by Siva V Thyagarajan

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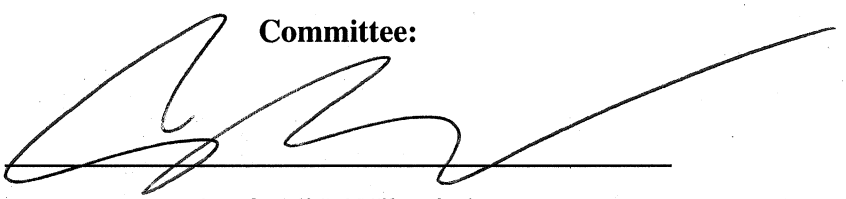

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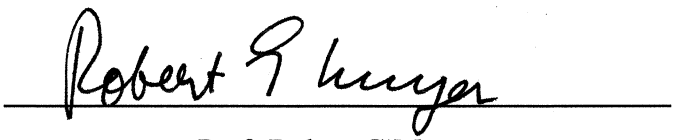

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Chapter 1

Introduction

Research in wireless communication systems have focussed on achieving low cost, fully integrable power efficient solutions. The efficiency of wireless transmitters is mainly affected by the design of the power amplifier block. In CMOS technologies, the rapid scaling of the power supply and low breakdown voltages have severly limited the peak efficiencies of power amplifiers. Also, with complex modulation schemes which have a very high peak to average ratio (typically $7-8$ dB for OFDM systems), the power amplifier operates mainly in the backoff regime and hence its average efficiency is even lower.

Linear power amplifiers such as Class A/B/AB [1] can be used with complex modulation schemes but have poor average efficiencies. Various techniques such as dynamic load modulation, envelope tracking [2], Doherty [3] have been proposed to boost the efficiencies of these amplifers. Non-linear switching amplifiers namely Class D, D^{-1}, E, F, E/F and its variants [4]-[8] achieve very high efficiencies but can be used only for constant envelope modulation schemes. By using advanced transmitter architectures such as Outphasing LINC [9], Polar modulation (Envelope Elimination and Reconstruction (EER)) [2], Pulse Width Modulation (PWM) [10] and recent Digital Power Amplifier [11] approach, these switching amplifiers can be used for advanced modulation schemes. The achievable output power and efficiency numbers for switching power amplifiers is mainly governed by two factors i.e. the switch size and its transition frequency. With the scaling of CMOS technology in the last decade, the transition frequencies of the transistors are in the hundreds of GHz range and hence these switching power amplifiers are a popular choice at RF [12].

However, achieving very high output power typically in the Watt regime with high efficiency and linearity is still an active area of research. In mm-wave systems, the relatively lower transition frequencies severely limits the performance of these topologies and hence these architectures have become popular only recently [13][14]. Another popular architecture, the Distributed Amplifier and its variants [15][16] achieve reasonable output power with very high bandwidths. These are broadband linear amplifiers that use transmission lines to boost the overall gain of the amplifier without any bandwidth penalty. However, the overall gain of these amplifiers is restricted as the distributed transconductance adds up linearly. Hence, they are not very efficient. The idea of distribution has also been applied to Transmit/Receive (T/R) switch design [17] where, by using a transmission line, a relatively large switch can be obtained to achieve low insertion loss and high isolation between the transmit and receive chains. However, these switches operate at a single frequency and under static conditions i.e. either in Transmit mode or Receive mode.

In this report [18], we introduce a new architecture - the Distributed Switching Power Amplifier (DSPA), that enhances the output power and efficiency metrics of a switching power amplifier by improving the overall realizable switch size. The transistors in a DSPA architecture are distributed along a transmission line but operate as switches unlike the case of a distributed amplifier. Hence, the effective switch transition frequency is improved which increases the overall output power and efficiency. As this involves a non-linear switching circuit with transmission lines, the theoretical framework of the distributed amplifier and the switching amplifier is no longer valid and optimum design parameters need to be calculated to maximize the performance. The report is organized as follows. Chapter 2 introduces the DSPA architecture and discusses how to choose the various design parameters. Chapter 3 gives the time domain analysis of the architecture and describes other concepts and tradeoffs associated with the design. Chapter 4 gives the complete frequency domain analysis of the DSPA architecture considering transmission line attenuation. Finally, in Chapter 5, the developed theoretical framework is compared against simulation results and concluding remarks are provided in Chapter 6.

Chapter 2

The Distributed Switching Power Amplifier (DSPA) Architecture

In this section, we introduce the basic concept of the DSPA architecture. For discussion purposes, we will restrict ourselves to the Inverse Class-D power amplifier based DSPA architecture. However, the idea can be very easily extended to other switching amplifier topologies namely Class E and F.

2.1 Conventional Inverse Class-D Power Amplifier

Fig. 2.1 (a) shows the circuit diagram of the Inverse Class-D power amplifier. It consists of two switches driven by square wave input signals operating in a complementary fashion. The switching action causes the constant current I_{DC} in the chokes to alternate across the output tank network. Hence, the current through the output resonator is square wave in nature with an amplitude I_{DC}. The LC tank circuit filters this current to yield a sinusoidal waveform across the load R_L at the fundamental frequency. Fig. 2.1 (b) shows the ideal Inverse Class-D waveforms. Since the switches are driven using ideal square wave inputs, the currents through the switches are also square wave in nature but are phase shifted by π. The voltage on the nodes v_{outp} and v_{outn} are rectified sinusoids and thus the differential waveform gives the required sinusoidal output. We should note that

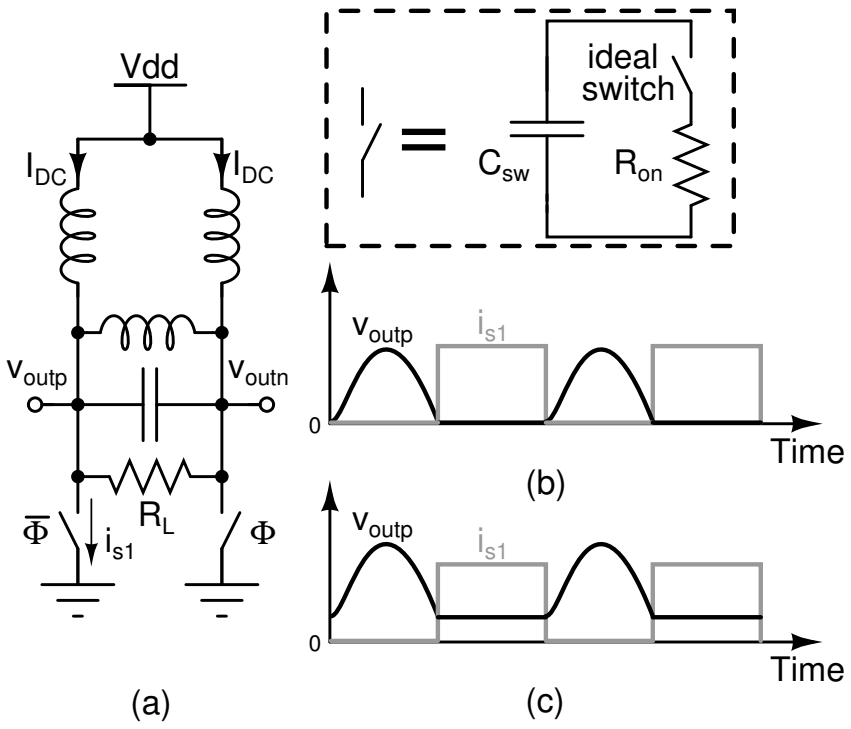

Figure 2.1: Conventional Inverse Class-D Switching Power Amplifier (a) Circuit diagram (b) Ideal switch waveforms (c) Switch waveform considering finite switch resistance

there is no overlap between the current and the voltage waveforms (zero-voltage switching or ZVS condition) and hence the power dissipation in the switch under ideal conditions is zero, thereby yielding a 100% theoretical efficiency for the amplifier.

In the design of this amplifier, the switch can be modeled using a switch resistance R_{on} and a switch parasitic capacitance C_{sw} as shown. The effect of R_{on} can be seen in the waveform shown in Fig. 2.1 (c). Compared to the ideal waveform, there is a DC shift which is proportional to the switch resistance. With regard to the switch capacitance C_{sw}, most of it is absorbed into the design of the output tank network. However, this capacitance still contributes to the amplifier loss. This is because the output tank capacitance acts like an open circuit for even harmonics whereas the switch capacitance provides a finite reactance to ground at these frequencies. This causes a change in the ZVS conditions and hence results in loss due to the switch resistance R_{on}. Assuming that most of C_{sw} is designed as part of the output resonator, we can assume that the output voltage waveform is purely sinusoidal with an amplitude A. Therefore, the DC voltage at v_{outp} can be

related to the DC current I_{DC} as

$$2I_{DC}R_{on} + A/\pi = Vdd \tag{2.1}$$

The output voltage can be related to the DC current as

$$A = 4I_{DC}R_L/\pi \tag{2.2}$$

Combining (2.1) and (2.2), we can compute the output amplitude, output power P_{out} and efficiency η as

$$A = \frac{2Vdd/\pi}{R_{on}/R_L + 2/\pi^2} \tag{2.3}$$

$$P_{out} = R_L \frac{2Vdd^2/\pi^2}{(R_{on} + 2R_L/\pi^2)^2} \tag{2.4}$$

$$\eta = \frac{1}{1 + \pi^2 R_{on}/(2R_L)} \tag{2.5}$$

From (2.4) and (2.5), it is clear that the only way to increase the output power and efficiency is to reduce R_{on} or equivalently increase the switch size. As the switch size is increased, the switch capacitance C_{sw} also increases. The output tank network is typically implemented using a transformer or an explicit inductor (if differential output is required) and this inductance must resonate with the combination of the tank and switch capacitance. The minimum realizable inductance therefore puts an upper bound on the maximum realizable switch size. This effect is more pronounced when one wishes to design a power amplifier at mm-wave or W-band frequencies. This is because the maximum allowed switch size scales inversely with the square of the operating frequency. In order to break this upper bound on the switch size, we introduce the DSPA architecture which allows one to realize a larger switch size and thereby helps achieve higher output power and efficiency.

2.2 The DSPA architecture switching network

Fig. 2.2 (a) shows the switch network of the DSPA architecture. The basic idea is to replace the switch in the conventional Inverse Class-D power amplifier using a distributed switch network. This distributed switch network would allow one to realize a much larger switch size without being limited by the minimum inductance constraint as in the case of a conventional amplifier. The

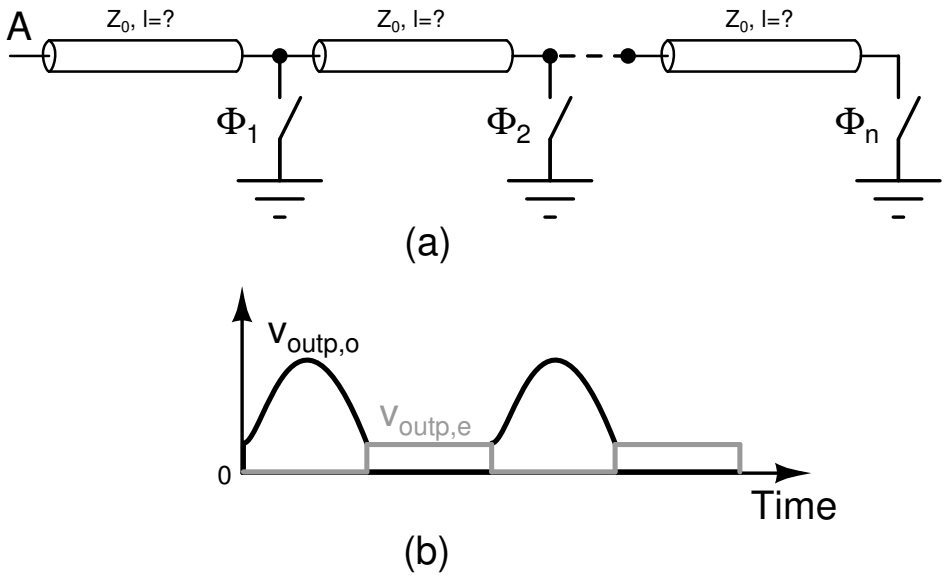

Figure 2.2: Distributed Switching Power Amplifier (DSPA) architecture switch network

distribution is also performed for the driving circuit where the gate capacitances of the switches are also distributed along a transmission line. This reduces the matching network quality factor and hence its insertion loss. Unlike a Distributed Amplifier which operates at a single frequency, a switching amplifier is highly non-linear and thus contains the fundamental frequency and all its harmonics. Therefore, the clocking scheme and the transmission line length play a crucial role in its operation. Hence, we need to find l and Φ_1, Φ_2, ... Φ_n, so that the effective switch size is increased thereby increasing output power and efficiency.

In order to determine the transmission line length, we refer to the Inverse Class-D waveforms shown in Fig. 2.1 (c). For the proper functioning of the DSPA, the output waveforms must maintain the same characteristics as this waveform i.e. it should be a half-sinusoid in one half-cycle and should be constant during the other. Hence, this waveform can be decomposed for all time as a half-wave rectified sinusoid in the odd cycle ($v_{outp,o}$) and a shifted square wave in the even cycle ($v_{out,e}$) as shown in Fig. 2.2 (b). If the single switch in the conventional amplifier is replaced by the distributed switch of Fig. 2.2 (a), the waveform injected into the transmission line will be a linear combination of $v_{outp,o}$ and $v_{out,e}$ with some appropriate scaling factors for the forward and reflected waves. Now to determine the transmission line length, we must note that the waveform $v_{out,e}$ is determined by the effective switch resistance of the distributed switches similar to a conventional power amplifier. Let us assume that only one switch namely the one clocked by Φ_1 exists. If a

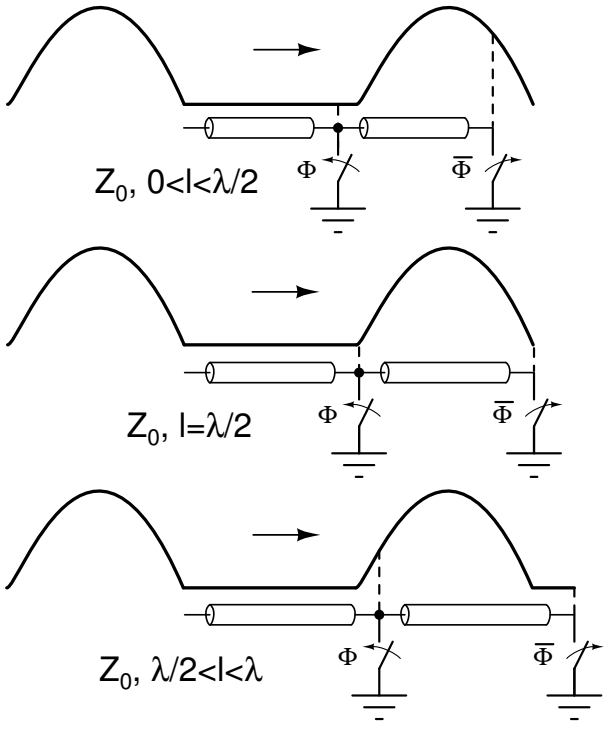

Figure 2.3: Conceptual diagram showing the effect of transmission line length mismatch

waveform proportional to $v_{out,e}$ is injected into the transmission line at node A, the impedance seen from A must always equal the switch resistance in the even cycle. From transmission line theory, we know that the impedance repeats itself for every one cycle around the Smith chart or for a line length of $\lambda/2$, where λ corresponds to the fundamental frequency of operation f_0 . Further, if the impedance seen at f_0 is the switch resistance, then this is true for all the harmonics of f_0 too. Hence, as far as the switch resistance is concerned, the minimum line length that satisfies this condition is $\lambda/2$. If we now consider the odd cycle, we must make sure that as $v_{out,o}$ passes through the transmission line, none of the switches are turned on as this would distort the waveform. Therefore, when one of the switches is turned on say Φ_1, the incident wave comprising of $v_{out,o}$ must be travelling towards Φ_2. This means that the half sinusoid wave which spans a cycle of π must be contained by the transmission line, before the next switch (in this case Φ_2) turns off and the wave can pass through. This would also require a minimum line length of $\lambda/2$ and to preserve the waveform the clocking should be complementary i.e. $\Phi_1 = \Phi_3 = \cdots = \Phi$ and $\Phi_2 = \Phi_4 = \cdots = \overline{\Phi}$. Since the transmission lines have a length which is an integer multiple of half-a-wavelength and the clocking mechanisms are complementary, this type of an architecture could be used only when the duty cycle is 50%. The effect of incorrect transmission line lengths with clocking is shown in

Fig. 2.3. As can be seen for the cases $0 < l < \lambda/2$ and $\lambda/2 < l < \lambda$, incorrect transmission line lengths causes switching during the sinusoidal phase of the waveform thereby violating the ZVS condition. We will now describe the time domain analysis of the DSPA architecture which will explain this concept in detail.

Chapter 3

The DSPA architecture : Analysis and Design Concepts

3.1 Time domain analysis

In order to understand the DSPA architecture, we employ a time domain approach, as it gives us a better insight into the operation of the amplifier. Consider the power amplifier topology shown in Fig. 3.1 where the switch in a conventional power amplifier is replaced with a single transmission line followed by a switch.

Let the characteristic impedance of the line be Z_0 with a length $\lambda/2$, where λ is the wavelength corresponding to the fundamental frequency of operation. The switches are assumed to be ideal and operate in a complementary fashion with 50% duty cycle. Assuming the quality factor of the tank to be high (typically $Q \geq 2$) [6], we can write the the voltage across the tank as

$$v_{outp} - v_{outn} = A\sin(\theta) \tag{3.1}$$

Here A is the output amplitude and $\theta = 2\pi f_0 t + \Phi$, where f_0 is the frequency of operation and Φ some arbitrary output phase. In terms of the forward and reflected waves of the transmission line (${v_p}^+, {v_p}^-, {v_n}^+, {v_n}^-$), we can write the node voltages v_{outp} and v_{outn} as

$$v_{outp} = {v_p}^+ + {v_p}^- \tag{3.2}$$

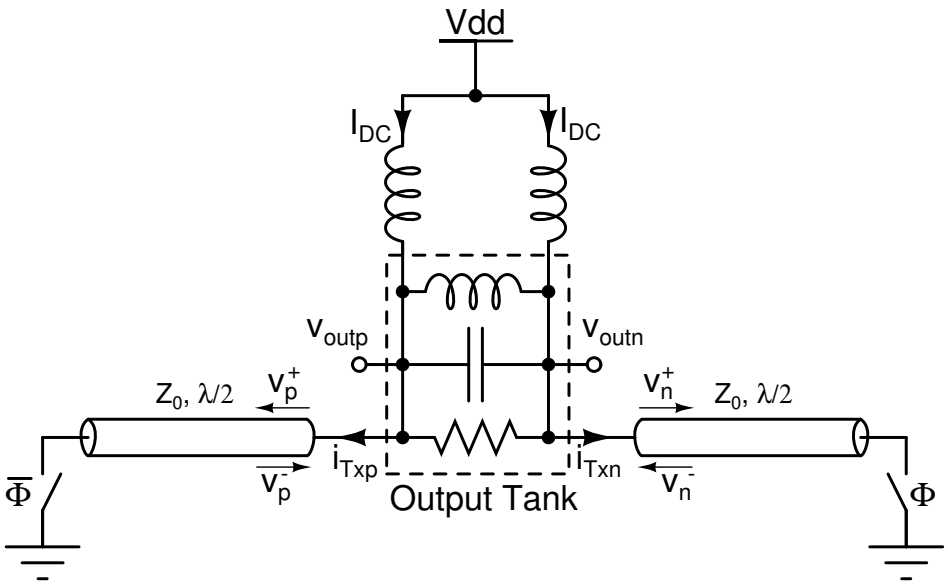

Figure 3.1: Circuit diagram of single stage DSPA architecture

$$v_{outn} = {v_n}^+ + {v_n}^- geqn : tda3 \tag{3.3}$$

The currents i_{Txp} and i_{Txn} flowing into the transmission line are given as

$$i_{Txp} = \frac{{v_p}^+ - {v_p}^-}{Z_0} \tag{3.4}$$

$$i_{Txn} = \frac{{v_n}^+ - {v_n}^-}{Z_0} \tag{3.5}$$

and satisfy the relation $i_{Txp} + i_{Txn} = 2I_{DC}$, where I_{DC} is the DC current flowing through the chokes. Combining (3.1)-(3.5), we obtain the simplified equations

$${v_p}^+ - {v_n}^- = I_{DC}Z_0 + 0.5A\sin(\theta) \tag{3.6}$$

$${v_n}^+ - {v_p}^- = I_{DC}Z_0 - 0.5A\sin(\theta) \tag{3.7}$$

We can now proceed with the analysis by considering the waveforms at a particular half-cycle number 'i' (a half-cyle corresponds to a time difference of $T_0/2$, where T_0 is the time period corresponding to f_0). Since the switches operate in a complementary fashion, the waveforms in the differential legs of the circuit under steady state condition must satisfy

$${v_p}^+(i) = {v_n}^+(i-1) = v_p^+(i-2) = {v_n}^+(i-3)\ldots \tag{3.8}$$

$${v_p}^-(i) = {v_n}^-(i-1) = v_p^-(i-2) = {v_n}^-(i-3)\ldots \tag{3.9}$$

Here the term in the paranthesis indicates the half-cycle number. Using (3.8) and (3.9), we can combine (3.6) and (3.7) into one equation as

$$v_p{}^+(i) - v_p{}^-(i-1) = I_{DC}Z_0 + (-1)^i\, 0.5A\text{sin}(\theta) \tag{3.10}$$

Now consider the left half of the circuit shown in Fig. 3.1. Assume that the switch turns ON at the end of every even cycle i.e. $i = 2k$. Note that this choice is arbitrary and only results in a final phase change at the output v_{outp}. Hence, with an ideal switch which results in the reflection coefficient $\Gamma = -1$, we get

$$v_p{}^-(2k+1) = -v_p{}^+(2k-1) \tag{3.11}$$

Note that there is a two half-cycle gap (or one cycle) in the relation and this equals the round-trip delay of the transmission line. During the OFF state which is every odd cycle, the reflection coefficient is unity and therefore

$$v_p{}^-(2k+2) = v_p{}^+(2k) \tag{3.12}$$

Combining (3.8)-(3.12), we obtain the forward and reflected waves at the even and odd cycles as

$$v_p{}^+(2k) = v_n{}^+(2k-1) = v_p{}^-(2k) = \quad v_n{}^-(2k-1) = 0.5A\text{sin}(\theta) \tag{3.13}$$

$$v_p{}^+(2k-1) = v_n{}^+(2k) = I_{DC}Z_0 \tag{3.14}$$

$$v_p{}^-(2k-1) = v_n{}^-(2k) = -I_{DC}Z_0 \tag{3.15}$$

Therefore, from (3.13), (3.14) and (3.15), during the even cycle

$$v_{outp} = v_p{}^+(2k) + v_p{}^-(2k) = A\text{sin}(\theta)$$
$$v_{outn} = v_n{}^+(2k) + v_n{}^-(2k) = 0$$

and the reverse holds true in the odd cycle. The waveforms at the output nodes v_{outp} and v_{outn} are thus identical to that of an Inverse Class-D Switching Power Amplifier architecture except for the fact that a transmission line now precedes the switch. The forward and reflected waves on the transmission line for a single cycle is shown in Fig. 3.2 (a). We observe that the forward wave $v_p{}^+$ and reflected wave $v_p{}^-$ are identical in one half cycle and add up in phase to generate part of the output sinusoid. In the other half-cycle, they add up to provide a short circuit at v_{outp}. The other transmission operates in a complementary fashion.

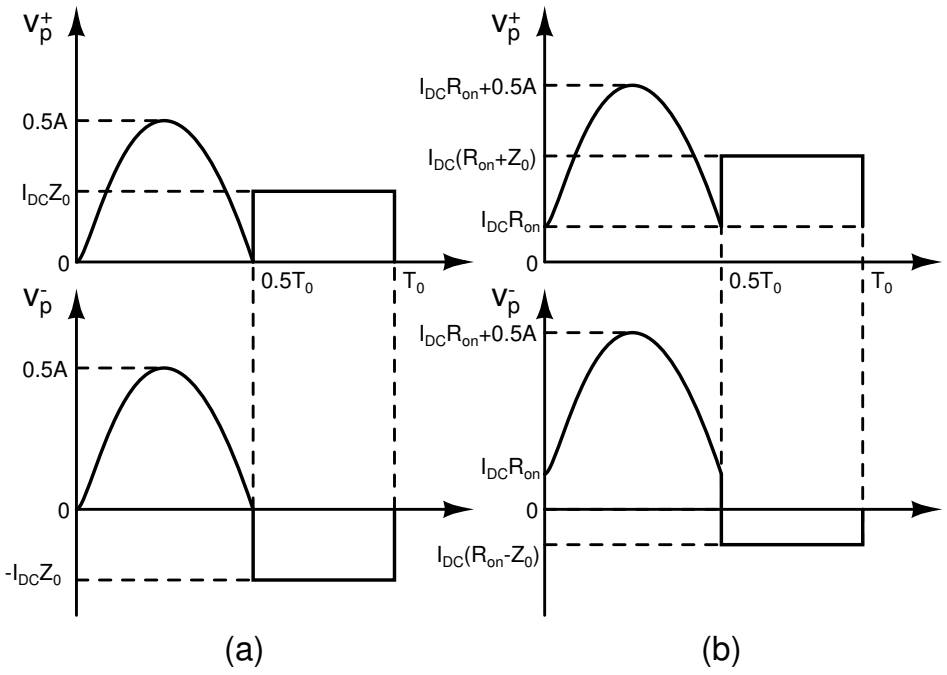

Figure 3.2: Single stage DSPA architecture: Forward and Reflected waves (a) with ideal switches (b) with switches having a finite resistance R_{on}

Now let us consider the case where the switches have a finite resistance R_{on}. Under these conditions, only (3.11) changes and is replaced as

$$v_p{}^-(2k+1) = \Gamma v_p{}^+(2k-1) \tag{3.16}$$

where Γ is the reflection coefficient given by $\Gamma = (R_{on} - Z_0)/(R_{on} + Z_0)$. Using a similar analysis as before, we obtain the forward and reflected waves as

$$\begin{aligned} v_p{}^+(2k) &= v_n{}^+(2k-1) = v_p{}^-(2k) = v_n{}^-(2k-1) \\ &= \left(\frac{1+\Gamma}{1-\Gamma}\right) I_{DC}Z_0 + 0.5A\text{sin}(\theta) \end{aligned} \tag{3.17}$$

$$v_p{}^+(2k-1) = v_n{}^+(2k) = \left(\frac{2}{1-\Gamma}\right) I_{DC}Z_0 \tag{3.18}$$

$$v_p{}^-(2k-1) = v_n{}^-(2k) = \left(\frac{2\Gamma}{1-\Gamma}\right) I_{DC}Z_0 \tag{3.19}$$

Therefore, from (3.17), (3.18), (3.19) and substituting for the reflection coefficient Γ, the even cycle waveforms can be simplified as

$$v_{outp} = v_p{}^+(2k) + v_p{}^-(2k) = 2I_{DC}R_{on} + A\text{sin}(\theta)$$

$$v_{outn} = v_n{}^+(2k) + v_n{}^-(2k) = 2I_{DC}R_{on}$$

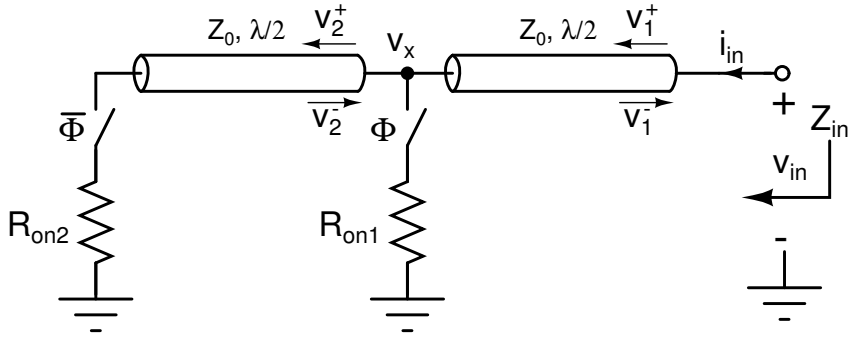

Figure 3.3: Two stage distributed switch

We observe that even in this case the output waveforms are exactly identical to that of a Class-D^{-1} Power Amplifier. The forward and reflected waves are shown in Fig. 3.2 (b). Compared to Fig. 3.2 (a), the waveforms are now offset by a DC shift $I_{DC}R_{on}$. Hence, neglecting the parasitic switch capacitances, if the switches in a conventional Inverse Class-D Power Amplifier topology are replaced with a transmission line based switch as discussed above, the performance and operation of the amplifier stays the same.

3.2 Effect of Distributed Switching

In the previous section, we discussed the working of an Inverse Class-D Power Amplifier with a transmission line based switch. However, using just a single switch does not give us any benefit compared to a conventional architecture. By distributing the switch beyond a single stage, one can take advantage of the DSPA architecture. In order to understand the effect of distribution, we consider a two stage distributed switch as shown in Fig. 3.3. In this case the switches have resistances R_{on1} and R_{on2} and the transmission lines have a characteristic impedance of Z_0 with a line length of $\lambda/2$ as before. The switches on this transmission line operate in a complementary fashion. For the analysis part, we will only consider the waveforms in the odd cycle (i.e when the switches are closed). The waveforms in the even cycle are immaterial as far as the effective resistance of the switch is concerned. We denote the forward and reflected waves in the odd cycle as ${v_1}^+$, ${v_1}^-$, ${v_2}^+$ and ${v_2}^-$. The input voltage v_{in} thus satisfies the relation

$$v_{in} = {v_1}^+ + {v_1}^- = {v_2}^+ + {v_2}^- \tag{3.20}$$

Our goal now is to find the net resistance looking into the transmission line under these conditions in the odd cycle. For the second transmission line, it is clear that the reflected wave is related to the forward wave through the reflection coefficient i.e.

$$v_2{}^- = \Gamma_2 v_2{}^+ \tag{3.21}$$

where Γ_2 is the reflection coefficient given by $\Gamma_2 = (R_{on2} - Z_0)/(R_{on2} + Z_0)$. Using (3.20) and (3.21), we get

$$v_{in} = (1 + \Gamma_2) v_2{}^+ \tag{3.22}$$

At the intermediate node v_x, using Kirchoff's current law we have

$$\frac{v_2{}^+ - v_2{}^-}{Z_0} + \frac{v_2{}^+ + v_2{}^-}{R_{on1}} = \frac{v_1{}^+ - v_1{}^-}{Z_0} = i_{in} \tag{3.23}$$

Using (3.21) and (3.23), we get the input current i_{in} as

$$i_{in} = (\frac{1 - \Gamma_2}{Z_0} + \frac{1 + \Gamma_2}{R_{on1}}) v_2{}^+ \tag{3.24}$$

Combining (3.22) and (3.24), the net impedance looking into the transmission line can be simplified as $Z_{in} = v_{in}/i_{in} = R_1 || R_2$ ("||" denotes resistances in parallel operation). Hence, we see that the effective resistance under this mode of operation is reduced, thereby allowing an equivalently larger switch size which results in higher output power and better efficiency. The forward and reflected waves with a two stage distribution (as in Fig. 3.3), is shown in Fig. 3.4. The half-sinusoid waveforms (marked as A, B, C and D) pass through the transmission line without being affected. The square waves on the other hand are altered by the switching action and this gives rise to an effectively lower resistance or equivalently larger switch. The parasitic capacitances of the switches can now be absorbed into the transmission line design and thus do not contribute to the loss or affect the output matching network design.

3.3 Switch size

In the previous section, we described the DSPA architecture where an effectively larger switch can be utilized thereby achieving high output power and high efficiency. However, the switch size cannot be increased arbitrarily. In practice, the switch has a finite transition frequency and therefore

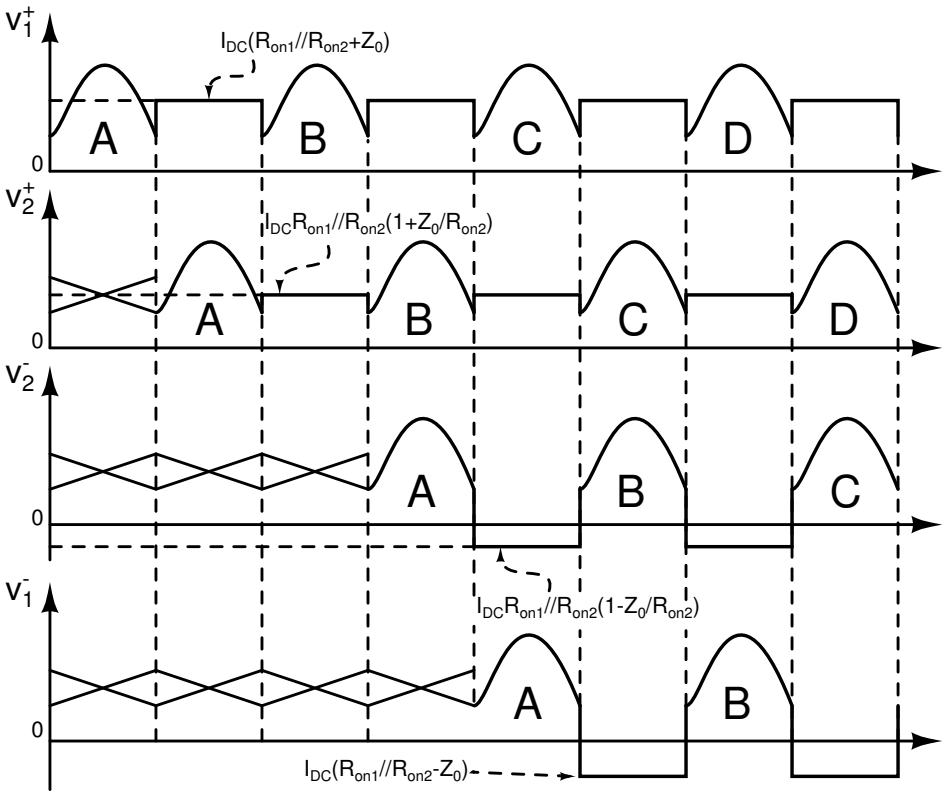

Figure 3.4: Two stage DSPA architecture: Forward and Reflected waves with switches having finite resistances R_{on1} and R_{on2}

an associated parasitic capacitance. Due to the distributed nature of the composite switch, most of this capacitance can be absorbed into the transmission line design. As the switch size is increased, the parasitic capacitance also increases. This changes the cut-off frequency of the transmission line and places an upper bound on the switch size. In order to understand this, consider the distributed switch network shown in Fig. 3.5. Here, we consider one section of the transmission line with length l and characteristic impedance Z_0. The switches have a capacitance C_{sw} each. If the inductance per unit length is L' and capacitance per unit length C', the characteristic impedance of the transmission line $Z_0 = \sqrt{L'/C'}$ and its cutoff frequency is infinity. When the transmission line is loaded with the switch capacitance C_{sw}, the new characteristic impedance and cutoff frequency can be approximated using lumped elements. The section can then be treated as a two port network using ABCD parameters [19]. The new characteristic impedance Z_{loaded} is given as $Z_{loaded} = Z_0/(\sqrt{1 + (2C_{sw})/(C'l)})$ and the cutoff frequency ω_c is given as

$$\omega_c = \frac{2}{l\sqrt{L'C'[1 + (2C_{sw})/(C'l)]}} \tag{3.25}$$

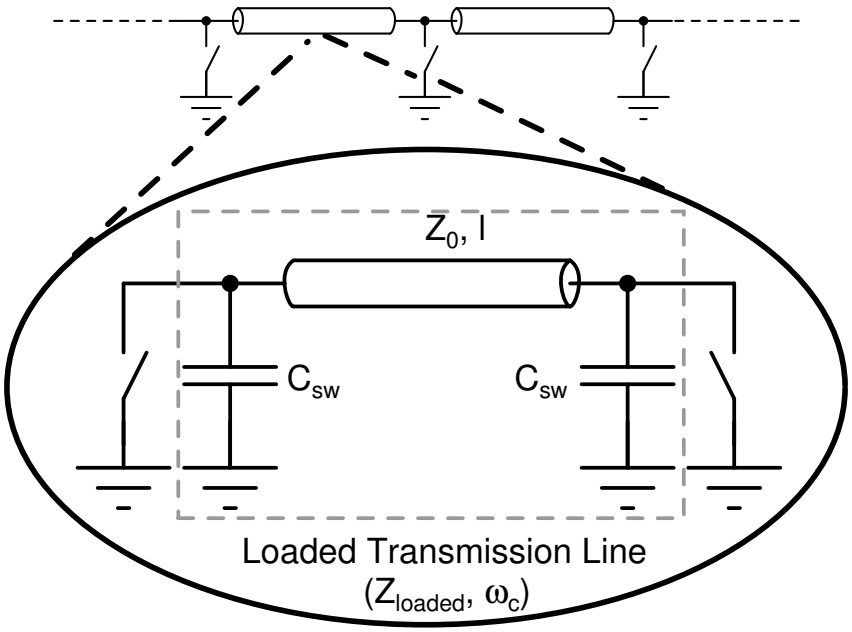

Figure 3.5: Distributed switch network (loaded transmission line)

Equation (3.25) indicates that the cutoff frequency of the transmission line is a strong function of the switch size. For the proper functioning of the DSPA, the cutoff frequency of the transmission line must be chosen such that most of the harmonic content of the signal is propagated through. This is a function of the operating frequency of the PA, loss of the passives and the process technology node. In this report, we discuss the system level aspects of the design and practical issues as these will be covered in future work as part of a design. A minimum cutoff frequency places an upper bound on the switch size and hence there is a maximum switch size which can be added per distribution level. If the effective switch size needs to be increased, the number of levels of distribution must be increased. The optimum number of levels is again a function of technology but qualitatively one can understand the tradeoff as follows. By adding multiple levels of distribution, the effective switch size is increased and the efficiency increases. However, the transmission line structure is itself lossy and after a particular number of stages, the loss in the transmission line offsets the benefit gained by distributing the switch. All the above factors must be considered while designing a power efficient DSPA.

3.4 Startup Conditions

The time domain analysis shown in the previous section gave the steady state solution of the DSPA architecture. However, the startup condition of the amplifier is instrumental in the complete understanding of the architecture. In order to analyze the startup condition, consider the single stage distributed amplifier shown in Fig. 3.1. For simplicity, we will not consider the transient behaviour of the chokes and will assume that they carry a constant current I_{DC} when the circuit is turned on (say at $t = -T_0/2$, where T_0 is the time period of the switching waveform). At this point we assume that $\phi = 0$. This results in a wave of amplitude $I_{DC}Z_0$ being launched on each of the transmission lines and reflected waves of $-I_{DC}Z_0$ and $I_{DC}Z_0$ being generated at $t = 0$. Let the switching action start at $t = T_0/2$ i.e. $\phi = 1$ at $t = T_0/2$. At the start of the half cycle i.e. when $t = T_0/2$, we have

$$v_p{}^+\Big|_{t=T_0/2} = (2+\Gamma)(I_{DC}Z_0) \tag{3.26}$$

Proceeding in a similar way, at $t = 3T_0/2$,

$$v_p{}^+\Big|_{t=3T_0/2} = [2+\Gamma(2+\Gamma)](I_{DC}Z_0) \tag{3.27}$$

Extending this analysis, at $t = nT_0/2, n \to \infty$

$$v_p{}^+\Big|_{\substack{t=nT_0/2\\ n\to\infty}} = [2+\Gamma(2+\Gamma(2+\Gamma(\dots))](2I_{DC}Z_0) \tag{3.28}$$

Equation (3.28) can be rewritten as

$$v_p{}^+\Big|_{\substack{t=nT_0/2\\ n\to\infty}} = 2I_{DC}Z_0 + \Gamma v_p{}^+\Big|_{\substack{t=nT_0/2\\ n\to\infty}} \tag{3.29}$$

Solving (3.29), at $t = nT_0/2$ with $n \to \infty$, $v_p{}^+ = I_{DC}(R_{on} + Z_0)$ and therefore $v_p{}^- = I_{DC}(R_{on} - Z_0)$ which is the same steady state solution which we obtained in the time domain analysis. During the cycle when $t = T_0, 2T_0, 3T_0, \dots$ we can perform a similar analysis starting with the recurrence relation

$$v_p{}^+\Big|_{t=nT_0} = I_{DC}\left(\frac{Z_0Z_T}{Z_0+Z_T}\right) + \Gamma v_p{}^+\Big|_{t=(n-1)T_0} \tag{3.30}$$

Here Z_T is the impedance of the tank circuit and $\Gamma = (Z_T - Z_0)/(Z_T + Z_0)$. At $t = T_0$, the DC current from the choke sees the transmission line Z_0 in parallel with the tank impedance Z_T, so that $v_p{}^+ = I_{DC}(Z_TZ_0)/(Z_T + Z_0)$. Using this initial condition, we can solve (3.30). Therefore, at $t = nT_0$ with $n \to \infty$, $v_p{}^+ = v_p{}^- = 0.5I_{DC}Z_T$. We must note that this waveform represents the

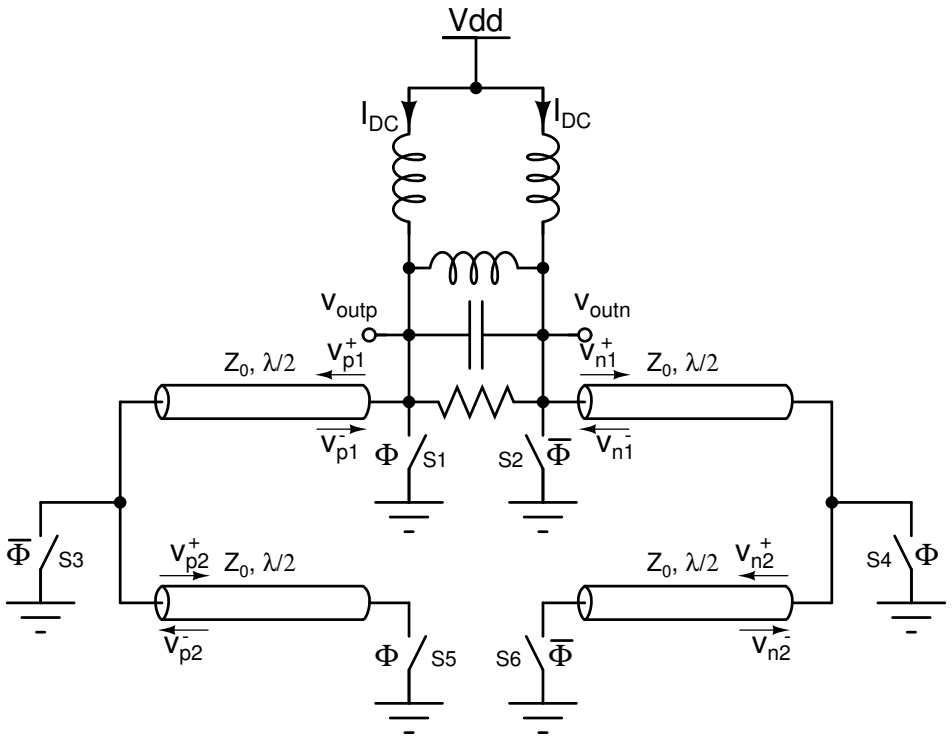

Figure 3.6: Two stage modified DSPA architecture

output during the OFF state and is valid during every alternate cycle. Moreover as Z_T is a resonant tank with a bandpass filter transfer function, the amplitude will be a filtered version of the square wave i.e. a half sinusoidal waveform as expected.

3.5 The modified DSPA architecture

By using the conventional Inverse Class-D power amplifier as the core, we could construct the modified DSPA architecture as shown in Fig. 3.6. In the case of the conventional and the DSPA architecture, the chokes and the output tank inductance are typically implemented using a transformer which performs an impedance transformation as well acts like a BALUN to drive the single ended antenna. We therefore get the benefit of adding additional switches whose capacitances are tuned at the fundamental frequency by the tank inductance. In the circuit diagram shown, if we denote the size of switch S5 i.e. W_{S5} as the maximum switch size tolerable by the transmission line, then $W_{S3} = 2W_{S5}$ as we have two transmission lines and twice the capacitance can be tolerated at

the middle node. The size of switch S1, $W_{S1} = W_{S5} + W_{conv}$, where W_{conv} is the switch size in a conventional Class-D^{-1} power amplifier. Hence, the effective switch size $W_{Seff} = 4W_{S5} + W_{conv}$. The switches operate in a complementary fashion as shown. In order to compare the performance of this amplifier with the conventional one, one must know the frequency of operation and the attenuation of the transmission line which is a function of the chosen technology node. However, one could argue that if the line attenuation is small, the number of stages in the DSPA can be increased and hence the effective switch size also increases. As an example, let us consider the two stage modified DSPA architecture. In order for most of the harmonic content to pass through the transmission line, the cutoff frequency must be atleast higher than twice the operating frequency (3.25). As the output tank circuit is realized using a transformer structure, the minimum realizable transformer inductance would be larger than the one used in the transmission line design (a very small transformer has a lower coupling factor [20]). Also, some part of the transformer inductance is always required for tuning out the secondary pad capacitances and this decreases the value of W_{conv}. Neglecting these effects and assuming the minimum realizable inductances to be the same in both the transformer and transmission line design, the unit switch size $W_{S5} = W_{conv}/4$. Hence, in this DSPA architecture, the increase in switch size can be factor of 2 compared to a conventional one.

3.6 Comparison with state-of-art High Power Architectures

Supply voltage scaling and low transistor breakdown voltages (especially in CMOS) have severely restricted the maximum achievable output power in power amplifiers. Hence, the design of high power amplifiers typically involves some form of combining such as transformer combining, "figure-8" structure [21] or the popular Distributed Active Transformer (DAT) [22]. In all these topologies, the efficiency of the core amplifier along with the combining efficiency determines the overall performance of the amplifier. By using a cascode device, one can increase the supply voltage further to obtain higher output power. Employing the DSPA architecture allows for obtaining a lower effective switch resistance than typical high-power architectures, thus simultaneously achieving high output power and improved efficiency. Since the impact of switch resistance is more pronounced at higher frequencies, the DSPA architecture becomes an attractive solution. The output power can be further increased by using one of the above power combining techniques with a DSPA-core.

Chapter 4

Frequency Domain Analysis of the DSPA architecture

In the previous sections, we introduced the DSPA architecture and explained the ideal operation scenario using time domain analysis. However, for practical purposes, the performance of the DSPA will be a function of the attenuation of the transmission line. The analysis of the DSPA architecture for a given number of stages considering transmission line attenuation and switch resistances is very complicated and it is almost impossible to obtain accurate closed form analytical solutions. In this section, we derive expressions for the output power and drain efficiency of a single stage distributed architecture and extend it to a given number of stages using simple approximations. This gives us a first cut estimate of the expected efficiency and output power given a particular switch resistance and transmission line attenuation. The attenuation of the transmission line typically increases with frequency. At microwave and mm-wave frequencies, the loss comprises of both conduction losses due to skin effect (proportional to the square root of frequency in dB) and dielectric losses in the substrate (proportional to frequency). With the scaling of CMOS technology the overall stack height is reduced and hence the top metal layers are now much closer to the substrate. Thus, these dielectric losses become significant at finer technology nodes. However, for the purpose of analysis and simulation, we neglect the dielectric losses to keep things simple. This does not change the analysis in any manner and these losses can be easily incorporated into the developed analytical framework. The attenuation in the transmission line considering

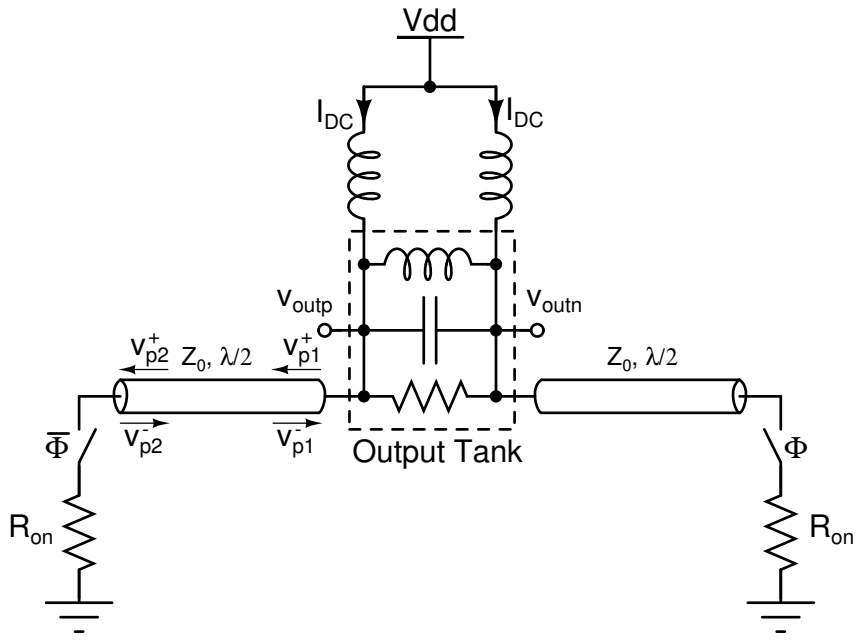

Figure 4.1: Circuit diagram of single stage DSPA architecture with switches having finite resistance R_{on}

conduction losses can be modeled as a function of frequency and is given as

$$A(f) = A_0\sqrt{\frac{f}{F}} \tag{4.1}$$

where $A(f)$ is the attenuation in dB/m and f the frequency under consideration. Let us assume a transmission line of length l and a fundamental operating frequency of f_0. The attenuation of the transmission line at frequencies nf_0 is α_n, $n = 1, 2, \ldots$. Let the injected periodic signal be given as

$$v^+ = a_0 + \sum_{n=1}^{\infty}[a_n\text{cos}(2\pi n f_0 t + \phi_n)]$$

Then the function Ψ computes the received signal at the other end of the transmission line and is given as

$$\Psi[v^+] = a_0 + \sum_{n=1}^{\infty}[\alpha_n a_n\text{cos}(2\pi n f_0 t + \phi_n - \delta_n)]$$

where δ_n represents the phase shift through the transmission line at the particular frequency. We can similarly define the inverse transformation Ψ^{-1}.

We will now analyze the single stage DSPA architecture shown in Fig. 4.1. Here, the switches have a resistance R_{on} and their capacitances are absorbed into the transmission line which has a

characteristic impedance of Z_0. The attenuation of the transmission line at the operating frequency and its harmonics are given by the coefficients α_n as defined above. It must be noted that for a transmission line of a given length, the phase shift at the fundamental frequency and its harmonics and the characteristic impedance are itself functions of the attenuation of the line. However, when the line attenuation is not very significant the characteristic impedance can be assumed to be the same as in the case with no attenuation. In order to calculate the output power and efficiency of the DSPA, a harmonic analysis technique is required visavis the time domain approach for the ideal case. This is because the line attenuation can be represented much more easily in the frequency domain. To perform a harmonic analysis technique, we will assume a finite number of harmonics (up to third) for the output node voltages and carefully select the unkowns in order to minimize calculations. From the time domain analysis waveforms in Fig. 3.2 (b), we observe that the single ended output waveform consists only of the first and the second harmonics. In fact the second harmonic term has only a cosine component. Since the attenuation is small, and because the second harmonic term is smaller than the fundamental, we will assume that the output single ended waveform has only cosine terms for the second harmonics even with attenuation. Hence, we can write

$$v_{p1}{}^{+} + v_{p1}{}^{-} = Vdd + 0.5p\cos(\theta) + 0.5q\sin(\theta) + a_2\cos(2\theta) \tag{4.2}$$

where $\theta = 2\pi f_0 t$ with f_0 being the fundamental frequency of operation. The DC output voltage is set to Vdd by the choke. Here, we assume an output tank with a high quality factor (typically $Q \geq 2$) so that the output differential voltage can be assumed to be purely sinusoidal and given as $p\cos(\theta) + q\sin(\theta)$. Observing the time domain waveforms for the current through the transmission line in the ideal case, we find that it consists only of the fundamental and odd harmonics, with the sinusoidal component of the third harmonic being dominant. Hence, we can write

$$v_{p1}{}^{+} - v_{p1}{}^{-} = I_{DC}Z_0 + c_1\cos(\theta) + d_1\sin(\theta) + d_3\sin(3\theta) \tag{4.3}$$

where I_{DC} is the DC current through the chokes. Our goal now is to find the coefficients p, q, a_2, c_1, d_1, d_3 and get an analytical expression for the output power and drain efficiency. Combining (4.2) and (4.3), we can write

$$\begin{aligned} v_{p1}{}^{+} = 0.5(Vdd + I_{DC}Z_0) + (0.25p + 0.5c_1)\cos(\theta) + (0.25q + 0.5d_1)\sin(\theta) \\ +0.5a_2\cos(2\theta) + 0.5d_3\sin(3\theta) \end{aligned} \tag{4.4}$$

$$v_{p1}{}^{-} = 0.5(Vdd - I_{DC}Z_0) + (0.25p - 0.5c_1)\cos(\theta) + (0.25q - 0.5d_1)\sin(\theta) + 0.5a_2\cos(2\theta) - 0.5d_3\sin(3\theta) \quad (4.5)$$

By using the notation of Ψ and Ψ^{-1}, we can write the forward and reflected waves from the switch as

$$v_{p2}{}^{+} = 0.5(Vdd + I_{DC}Z_0) + (0.25p + 0.5c_1)\Psi[\cos(\theta)] + (0.25q + 0.5d_1)\Psi[\sin(\theta)] + 0.5a_2\Psi[\cos(2\theta)] + 0.5d_3\Psi[\sin(3\theta)] \quad (4.6)$$

$$v_{p2}{}^{-} = 0.5(Vdd - I_{DC}Z_0) + (0.25p - 0.5c_1)\Psi^{-1}[\cos(\theta)] + (0.25q - 0.5d_1)\Psi^{-1}[\sin(\theta)] + 0.5a_2\Psi^{-1}[\cos(2\theta)] - 0.5d_3\Psi^{-1}[\sin(3\theta)] \quad (4.7)$$

The current through the switch can be related to the voltage across it using the switching voltage waveform ($\overline{\Phi} = s(\theta)$) and is given by

$$\frac{v_{p2}{}^{+} - v_{p2}{}^{-}}{Z_0} = \left(\frac{v_{p2}{}^{+} + v_{p2}{}^{-}}{R_{on}}\right) s(\theta) \quad (4.8)$$

where $s(\theta)$ is a DC shifted square wave with Fourier series given as

$$s(\theta) = 0.5 + \frac{2}{\pi}\sum_{k=1,3,\ldots}\frac{\sin(k\theta)}{k}$$

Since the line length is $\lambda/2$, $\Psi(v_{p2}{}^{+})$ has a phase shift $\delta_n = -n\pi$ and coefficient α_n with respect to $v_{p1}{}^{+}$ whereas $\Psi^{-1}(v_{p2}{}^{-})$ has a phase shift $\delta_n = n\pi$ and coefficient $1/\alpha_n$ compared to $v_{p1}{}^{-}$, $n = 1, 2, \ldots$. By using (4.6) and (4.7) in (4.8) and comparing the harmonic components, we get the following relations. For the DC term,

$$2I_{DC}R_{on} = Vdd - \frac{0.5q(1/\alpha_1 + \alpha_1)}{\pi} + \frac{d_1(1/\alpha_1 - \alpha_1)}{\pi} + \frac{d_3(1/\alpha_3 - \alpha_3)}{3\pi} \quad (4.9)$$

For the different harmonic frequencies nf_0, let us denote $\gamma_n = 1/\alpha_n + \alpha_n$ and $\beta_n = 1/\alpha_n - \alpha_n$, so that (4.9) becomes

$$2I_{DC}R_{on} = Vdd - \frac{0.5q\gamma_1}{\pi} + \frac{d_1\beta_1}{\pi} + \frac{d_3\beta_3}{3\pi} \quad (4.10)$$

The magnitude of the sinusoidal component of the current through the load is given by the fundamental component of the current through the transmission line and hence

$$(v_{p1}{}^{+} - v_{p1}{}^{-})|_{f_0} = -\frac{Z_0}{R_L}(p\cos(\theta) + q\sin(\theta)) \quad (4.11)$$

From (4.3), this results in $c_1 = -pZ_0/R_L$ and $d_1 = -qZ_0/R_L$. Combining (4.11) with the relation for the fundamental component from (4.8), we obtain $p = 0$ and $c_1 = 0$. This shows that when the attenuation is low enough, the cosine terms in the fundamental frequency can also be ignored. Comparing the fundamental sinusoidal term, the second harmonic and third harmonic from (4.8), we obtain the output voltage q as

$$q = \frac{2Vdd/\pi}{\frac{\beta_1}{4}\left(\frac{R_{on}}{Z_0} + \frac{Z_0}{R_L}\right) + \frac{\gamma_1}{2}\left(\frac{R_{on}}{R_L} + 0.25\right) - \frac{2\gamma_2}{9\pi^2}\left(\frac{\gamma_1 + 2\beta_1 Z_0/R_L}{\gamma_2 + 2\beta_2 R_{on}/Z_0}\right)} \tag{4.12}$$

When we consider the case of an ideal transmission line, $\alpha_1 = \alpha_2 = 1$ and hence $\beta_1 = \beta_2 = 0$ and $\gamma_1 = \gamma_2 = 2$, evaluating (4.12) results in an output amplitude

$$q = \frac{2Vdd/\pi}{R_{on}/R_L + 0.25 - 4/(9\pi^2)} \approx \frac{2Vdd/\pi}{R_{on}/R_L + 2/\pi^2}$$

which is the same for the case of an ideal Inverse Class-D power amplifier as in (2.3). The harmonic coefficients a_2, d_1 and d_3 are given as

$$a_2 = -\frac{2q}{3\pi}\left(\frac{\gamma_1 + 2\beta_1 Z_0/R_L}{\gamma_2 + 2\beta_2 R_{on}/Z_0}\right) \tag{4.13}$$

$$d_1 = \frac{-\frac{Z_0}{R_L}(2Vdd/\pi)}{\frac{\beta_1}{4}\left(\frac{R_{on}}{Z_0} + \frac{Z_0}{R_L}\right) + \frac{\gamma_1}{2}\left(\frac{R_{on}}{R_L} + 0.25\right) - \frac{2\gamma_2}{9\pi^2}\left(\frac{\gamma_1 + 2\beta_1 Z_0/R_L}{\gamma_2 + 2\beta_2 R_{on}/Z_0}\right)} \tag{4.14}$$

$$d_3 = -\frac{4Vdd/3 + a_2\gamma_2}{\pi(0.5\beta_3 + \gamma_3 R_{on}/Z_0)} \tag{4.15}$$

By using (4.12)-(4.15) in (4.10), we can obtain the DC power consumption for the single stage DSPA.

The next step in this analysis is to find the output power and efficiency numbers for a multi stage DSPA. In order to generalize this result for an n-stage distribution, it is convenient to map the DSPA to a simplified architecture. For this consider the circuit diagram shown in Fig. 4.2. For any n-stage DSPA/modified DSPA architecture we can combine the entire distributed switch network as shown here. Considering the attenuation of the transmission line, the switches do not behave as perfect shorts or perfect open circuits as compared to the ideal case. Hence, part of the DC current always leaks into the transmission line structure. For example, consider the ideal waveform shown in Fig. 3.2 (a). When the transmission line is ideal, the two half sinusoids in the forward and reflected wave are equal in amplitude and hence no current flows through the transmission line during that cycle. With finite attenuation in the transmission line, the reflected

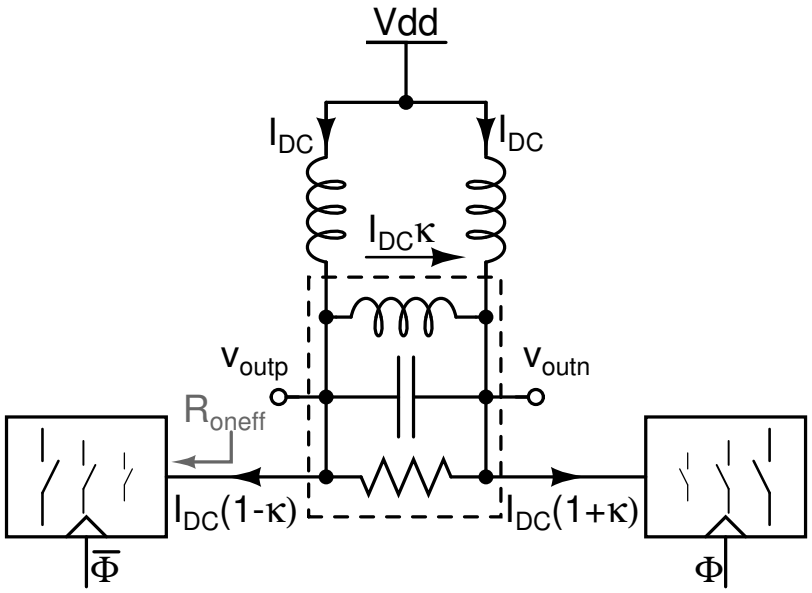

Figure 4.2: Equivalent circuit for an n-stage DSPA

wave will be a damped version of the forward wave and hence even during the OFF cycle some current would leak into the transmission line. These effects can be modeled using a fractional parameter κ and an effective switch resistance R_{oneff}. κ can be visualized as a single attenuation parameter which multiplies with the output waveform to model the loss. This is because the output is obtained from the individual waveforms at nodes v_{outp} and v_{outn}, both of which are half-wave rectified sinusoids. These waveforms pass through the transmission lines in an n-stage DSPA (see Fig. 3.4) and thus encounter the complete loss of all the lines. R_{oneff} on the other hand is the effective switch resistance of the distributed switch network and its value is affected both by the attenuation of the line and the number of stages of distribution. Using this model we analyze the circuit in Fig. 4.2 in the same manner as we analyzed the conventional Class-D^{-1} power amplifier in Section 2. We can write the DC current and output amplitude relation by considering the DC voltage at node v_{outp}. This gives

$$I_{DC}(1+\kappa)R_{oneff} + A/\pi = Vdd \tag{4.16}$$

where I_{DC} is the DC current through the chokes, A is the output amplitude and Vdd the supply voltage. With an attenuation parameter κ, we can write the output amplitude as

$$A = \kappa(4I_{DC}R_L/\pi) \tag{4.17}$$

Combining (4.16) and (4.17), we obtain the output power P_{out} and DC power consumption P_{DC} as

$$P_{out} = \kappa^2 R_L \frac{2Vdd^2/\pi^2}{\left[0.5(1+\kappa)R_{oneff} + \kappa(2R_L/\pi^2)\right]^2} \tag{4.18}$$

and

$$P_{DC} = \frac{Vdd^2}{0.5(1+\kappa)R_{oneff} + \kappa(2R_L/\pi^2)} \tag{4.19}$$

Given P_{out} and P_{DC}, using (4.18) and (4.19), we can compute the attenuation parameter and the effective switch resistance as

$$\kappa = \sqrt{\left(\frac{P_{out}}{{P_{DC}}^2}\right)\frac{\pi^2 Vdd^2}{2R_L}} \tag{4.20}$$

$$R_{oneff} = \frac{2Vdd^2/P_{DC} - 4\kappa R_L/\pi^2}{1+\kappa} \tag{4.21}$$

These set of equations from (4.18)-(4.21) can be used to map any n-stage DSPA architecture using appropriate κ and R_{oneff} values.

In order to understand this, consider the circuit diagram shown in Fig. 4.3 (a). Here we have the switch network of a three stage modified DSPA architecture. Our goal now is to map this architecture to Fig. 4.2 i.e. to find the effective parameters R_{oneff} and κ (shown in circles) and then calculate its output power and efficiency. The attenuation parameter κ for a three stage modified DSPA will be almost the same as that of a single stage DSPA operating with a transmission line of length $3\lambda/2$. This is because in both cases the output waveform sees the loss in the three $\lambda/2$ lines or equivalently a single $3\lambda/2$ line. Hence, in order to find κ, we employ the theory of a single stage DSPA developed in the previous section. As shown in Fig.4.3 (b), we solve the single stage DSPA with a $3\lambda/2$ line instead of a $\lambda/2$ line. Note that the phase change for both the cases is the same except for the fact that the attenuation in the $3\lambda/2$ line case is higher. This must be taken into account while performing the analysis. We calculate the P_{out} and P_{DC} for this case with the theoretical framework (4.10)-(4.15) and using (4.20), we compute the effective κ which we denote as κ_3.

The computation of R_{oneff} involves a few more steps. The first thing to notice is that the distributed network in Fig. 4.3 (a) is a composition of various single stage $\lambda/2$ lines. Hence, we first need to find the effective switch resistance $R_{on,stage}$ for a single stage DSPA. For this we again employ the theory developed for the single stage DSPA. We calculate the output power P_{out} and

DC power consumption P_{DC} considering a $\lambda/2$ line (Fig. 4.3 (c)). Then using (4.20) and (4.21), we calculate $R_{on,stage}$. As one can comprehend, the resistance $R_{on,stage}$ models the effective resistance looking into the transmission line from the output side. This resistance takes into account all the losses due to attenuation in the $\lambda/2$ transmission line and hence can be visualized as an average resistance. In order to compute the effective resistance of the three stage DSPA which has different resistance terminations namely R_{on1}, R_{on2}, R_{on3} and R_{on4}, we need to find an effective (average) transmission line transformation parameter ζ, which performs the impedance change. We illustrate this in Fig. 4.3 (d) where one end of the transmission line with characteristic impedance Z_0 is terminated with R_{on1} and on the other end we observe an impedance $R_{on,stage}$. Note that the values of both $R_{on,stage}$ and R_{on1} are known. Using transmission line theory, we can write $R_{on,stage}$ as

$$R_{on,stage} = Z_0 \left(\frac{R_{on1}(1+\zeta^2) + Z_0(1-\zeta^2)}{R_{on1}(1-\zeta^2) + Z_0(1+\zeta^2)} \right) \tag{4.22}$$

Equation (4.22) can be rearranged to give ζ as

$$\zeta = \sqrt{\frac{(R_{on,stage} - Z_0)(R_{on1} + Z_0)}{(R_{on,stage} + Z_0)(R_{on1} - Z_0)}} \tag{4.23}$$

Using (4.22) and knowing the value of $R_{on,stage}$ and R_{on1} from previous calculations, one can find the effective transmission line transformation parameter ζ for a $\lambda/2$ line which transforms R_{on1} to $R_{on,stage}$. We are now all set to find the effective resistance R_{oneff} of the three stage modified DSPA. Referring back to Fig. 4.3 (a), starting from the left-most transmission line we can calculate R_{oneff3} using (4.22) where R_{on1} is replaced by R_{on4} and we use the value of the calculated ζ to carry out the transformation. This resistance R_{oneff3} is now in parallel with R_{on3} and the combination serves as the terminating resistance for the second transmission line. Following a similar procedure, we can find the effective resistance R_{oneff}. If we denote Υ as the impedance transformation as given by (4.22), then

$$R_{oneff} = R_{on1}|||[\Upsilon(R_{on2}|||[\Upsilon(R_{on3}|||[\Upsilon(R_{on4})])])] \tag{4.24}$$

We will illustrate this procedure using a numerical example for clarity. Let us consider a three stage modified DSPA architecture operating at 60 GHz with the switch network as shown in Fig. 4.3 (a). Let $Vdd = 1$ V, $Z_0 = 50\,\Omega$ and $R_L = 50\,\Omega$. With a process $f_T = 200$ GHz and a reasonable switch size of $50\,\mu$m at these frequencies, the switch ON resistance is $R_{on} = 10\,\Omega$ with a capacitance density of $1.5\,\text{fF}/\mu\text{m}$. Hence, we assume $R_{on1} = R_{on2} = R_{on3} = 10\,\Omega$ and $R_{on4} = 20\,\Omega$.

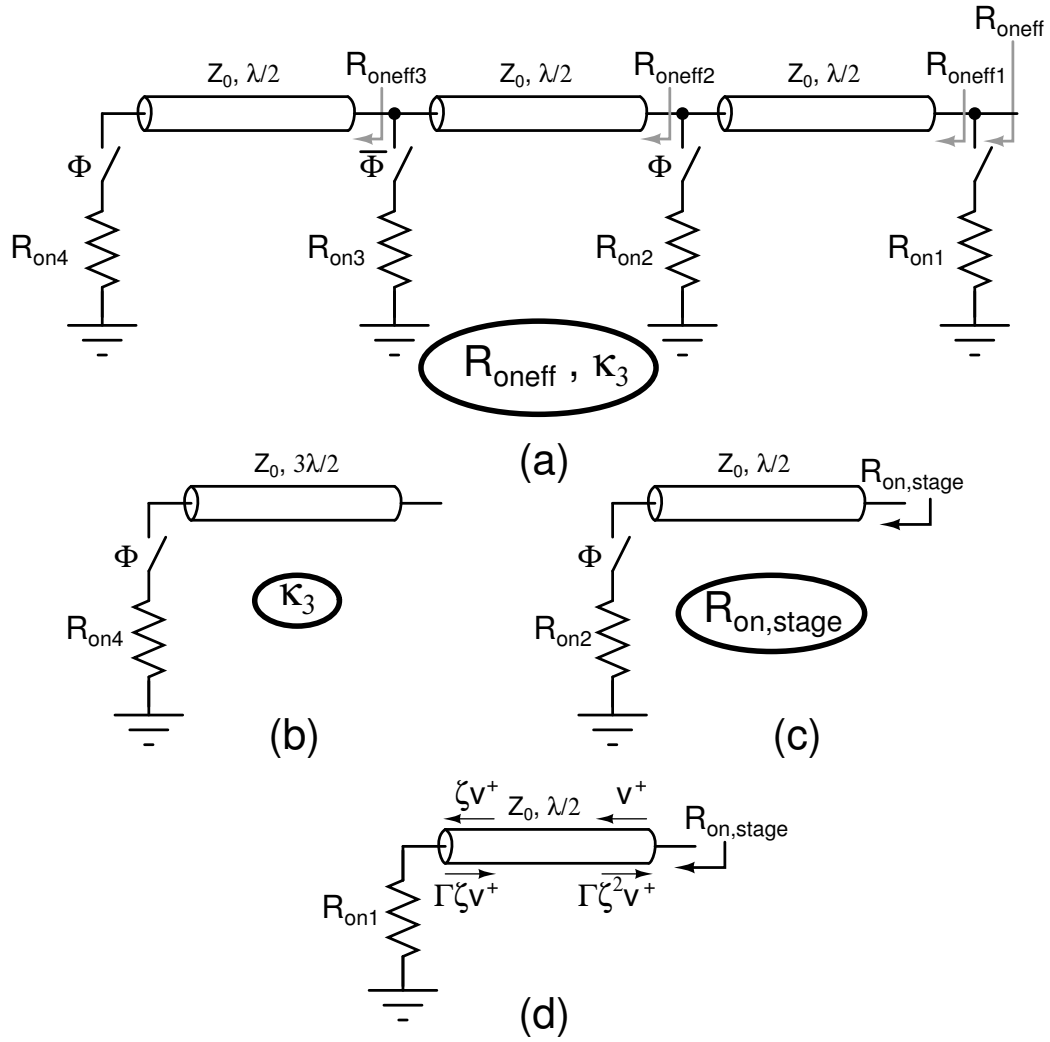

Figure 4.3: Calculation of effective switch resistance for a multi stage DSPA

This is considering the difference between the minimum realizable inductances for the transformer and transmission line as stated earlier. Assuming a medium with dielectric constant $\epsilon_r = 4$, the wavelength $\lambda = 2.5$ mm. Also, let the attenuation of the transmission line be 0.5 dB/mm, so that the line loss for a $\lambda/2$ line at the fundamental, second and third harmonic frequencies are 0.625 dB, 0.884 dB and 1.083 dB respectively. Note that we have used (4.1) to model the transmission line attenuation. Our goal is to find the output power and efficiency of the three stage modified DSPA. The calculation steps are given below with the respective equation references.

1. To find κ_3 using single stage DSPA with $3\lambda/2$ line, $R_{on} = 20\,\Omega$

   - $\alpha_1 = 0.806$, $\gamma_1 = 2.047$, $\beta_1 = 0.435$, $\alpha_2 = 0.737$, $\gamma_2 = 2.094$, $\beta_2 = 0.620$, $\alpha_3 =$

0.688, $\gamma_3 = 2.142$, $\beta_3 = 0.766$

- $q = 0.833\,\text{V}$, $a_2 = -0.199$, $d_1 = -0.833$, $d_3 = -0.235$, $P_{out} = 6.939\,\text{mW}$, $P_{DC} = 29.711\,\text{mW} \rightarrow$ (4.10)-(4.15)
- $\kappa_3 = 0.881 \rightarrow$ (4.20)

2. To find $R_{on,stage}$ using single stage DSPA with $\lambda/2$ line, $R_{on} = 10\,\Omega$
   - $\alpha_1 = 0.931$, $\gamma_1 = 2.005$, $\beta_1 = 0.144$, $\alpha_2 = 0.903$, $\gamma_2 = 2.010$, $\beta_2 = 0.204$, $\alpha_3 = 0.883$, $\gamma_3 = 2.016$, $\beta_3 = 0.250$
   - $q = 1.431\,\text{V}$, $a_2 = -0.333$, $d_1 = -1.431$, $d_3 = -0.400$, $P_{out} = 20.489\,\text{mW}$, $P_{DC} = 46.695\,\text{mW} \rightarrow$ (4.10)-(4.15)
   - $\kappa = 0.963$, $R_{on,stage} = 11.878\,\Omega \rightarrow$ (4.20), (4.21)
3. To find transmission line transformation parameter ζ
   - $R_{on,stage} = 11.878\,\Omega$, $R_{on1} = 10\,\Omega$
   - $\zeta = 0.961 \rightarrow$ (4.23)
4. To find R_{oneff} of the three stage distributed switch using $\zeta = 0.961 \rightarrow$ (4.22), Fig. 4.3 (a)
   - $R_{on4} = 20\,\Omega$, $R_{oneff3} = 21.630\,\Omega$
   - $R_{on3} = 10\,\Omega$, $R_{oneff2} = 8.763\,\Omega$
   - $R_{on2} = 10\,\Omega$, $R_{oneff1} = 6.618\,\Omega$
   - $R_{on1} = 10\,\Omega$, $R_{oneff} = 3.982\,\Omega$
5. To find P_{out}, P_{DC} and η of the three stage DSPA
   - $R_{oneff} = 3.982\,\Omega$, $\kappa_3 = 0.881$
   - $P_{out} = 48.978\,\text{mW}$, $P_{DC} = 78.917\,\text{mW}$, $\eta = 62.063\% \rightarrow$ (4.18), (4.19)

One must note that in Step 4, the effective resistance $R_{oneff} = 3.982\,\Omega$ which is slightly larger than the case when all switches are connected together without transmission lines (in that case $R_{oneff} = 2.857\,\Omega$). This is due to the finite attenuation of the transmission line that causes the effective switch resistance to increase ($\eta \neq 1$ in (4.22)). However, the effective resistance is still lesser than what could have been achieved using a conventional architecture which is around $10\,\Omega$.

Chapter 5

Verification with Simulation Results

In order to verify the theory of the DSPA architecture, the power amplifier was simulated using Agilent's Advanced Design System (ADS). The operating frequency was chosen to be $60\,\text{GHz}$. The output tank network quality factor was around 2.2 corresponding to a minimum realizable inductance of $60\,\text{pH}$ and a load resistance of $50\,\Omega$. The transmission line was modeled using ADS internal model TLINP4. Harmonic balance simulations were used to characterize the power amplifier.

To verify the time domain analysis of the DSPA, a two stage DSPA with a distributed switch network similar to the one shown in Fig. 3.3 was used. R_{on1} was chosen to be $10\,\Omega$ and R_{on2} to be $20\,\Omega$. The characteristic impedance of the transmission line was $50\,\Omega$. Fig. 5.1 shows the simulated switch current waveforms. The total DC current divides in a manner proportional to the switch conductances. Hence, the switch distribution indeed achieves a lower resistance. In order to determine the forward and reflected waves for the circuit shown in Fig. 3.3 i.e. ${v_1}^+$, ${v_1}^-$, ${v_2}^+$ and ${v_2}^-$, a transformer based directional coupler is used. Fig. 5.2 shows the simulated forward and reflected waves for the two stage DSPA. Note that the magnitude of the waveforms is $1/100$th of the actual voltage waveform which is due to a coupling factor of $1{:}100$. Comparing this with the waveforms shown in Fig. 3.4, we find a good match between simulation and theory.

In order to verify the frequency domain analysis for a single stage DSPA, the circuit in Fig. 4.1 was simulated for different values of R_{on} and transmission line attenuation parameters. Fig. 5.3

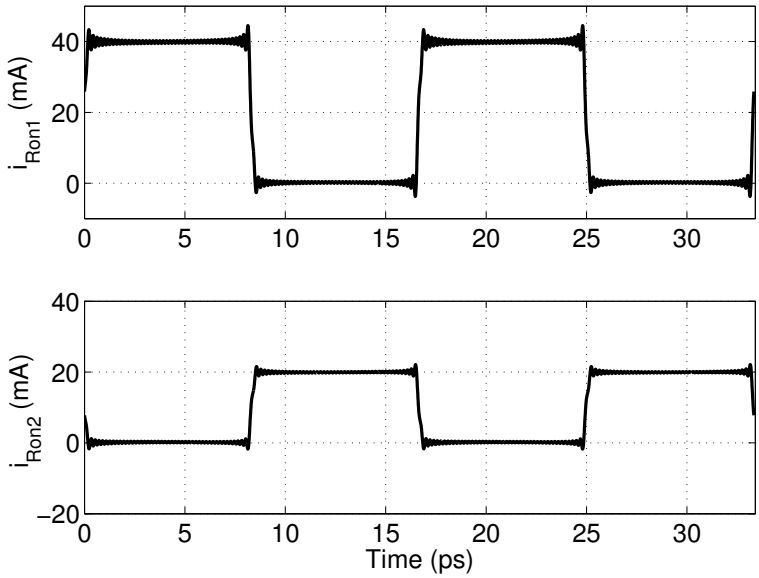

Figure 5.1: Simulated switch currents for a two stage DSPA

shows the variation of output power with attenuation for $R_{on} = 5\,\Omega$, $R_{on} = 10\,\Omega$ and $R_{on} = 20\,\Omega$. The simulated values are compared against the developed theory and the error increases as R_{on} reduces and the attenuation increases. Note that in our analysis, we have assumed Z_0 to be a constant. However, with attenuation the characteristic impedance of a transmission line is no longer real and the error increases as the attenuation increases. This also causes the phase change across the line to be altered from the required shift of π at the fundamental frequency. Fig. 5.4 compares the derived efficiency from theory with the simulated value. We find a good correlation between the two indicating that the DC power consumption is also accurately predicted. As expected the efficiency of the power amplifier drops as the attenuation of the transmission line increases.

The theory of the single stage architecture was extended to an n-stage DSPA using the equivalent circuit model shown in Fig. 4.2. The calculated values were compared as a function of the transmission line attenuation for the two stage modified DSPA shown in Fig. 3.6. In this case, the resistance of S1 and S3 was chosen to be R_{on} and that of S5 was $2R_{on}$. Fig. 5.5 and Fig. 5.6 compare the theoretical and simulated output power and efficiency of the DSPA. We find that the theoretical analysis predicts the trend in the output power and efficiency accurately. Comparing the efficiency numbes for the single stage DSPA in Fig. 5.4 with that of the two stage modified DSPA, we find that there is an efficiency boost of almost $17 - 18\%$. This is because the effective switch

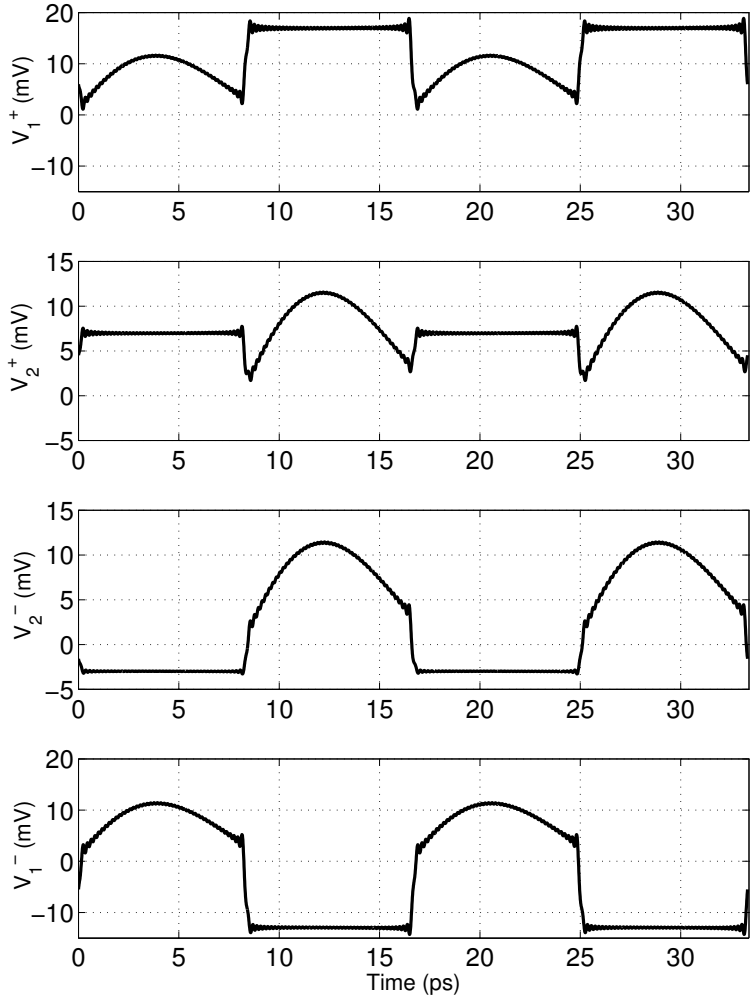

Figure 5.2: Simulated forward and reflected waves for a two stage DSPA

resistance in the modified DSPA case is much lower.

In order to verify the theoretical analysis for an n-stage DSPA, the variation of the output power and efficiency were compared as the number of stages of the power amplifier was varied. Fig. 5.7 shows the variation of the output power as a function of the number of stages for different attenuation numbers. The value of zero for the number of stages in the x-axis indicates a conventional amplifier with $R_{on} = 10\,\Omega$. The distributed switches also have an $R_{on} = 10\,\Omega$ for any switch flanked by two transmission lines and $R_{on} = 20\,\Omega$ for the switch at the very end, as was the case in the two stage modified DSPA. The output power in the case of an ideal transmission line (0 dB/mm)

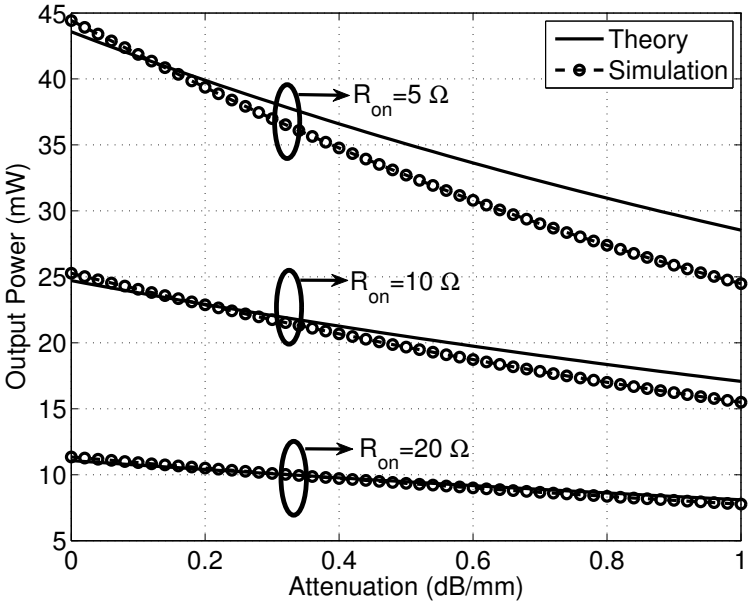

Figure 5.3: Variation of Output Power with Attenuation (for different R_{on}) for a single stage DSPA

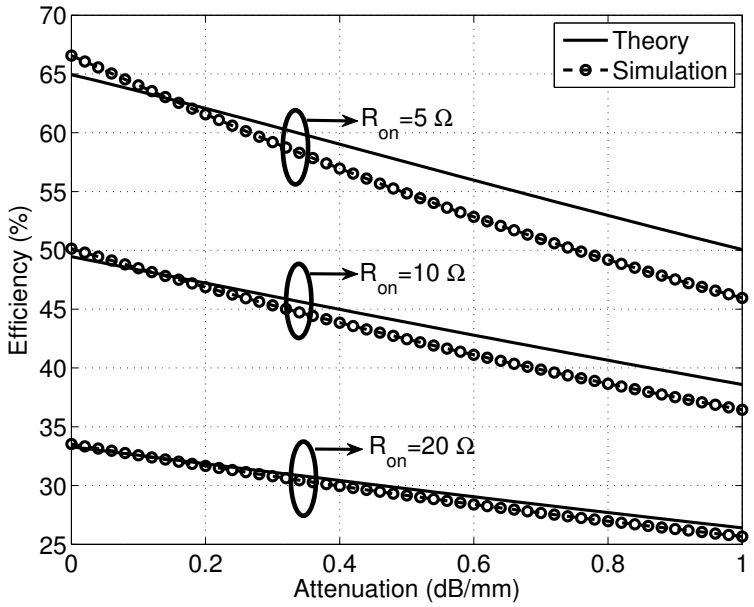

Figure 5.4: Variation of Drain Efficiency with Attenuation (for different R_{on}) for a single stage DSPA

increases as the number of stages increases. This is because the effective switch resistance keeps decreasing. The efficiency also follows a similar trend as shown in Fig. 5.8. Once the attenuation

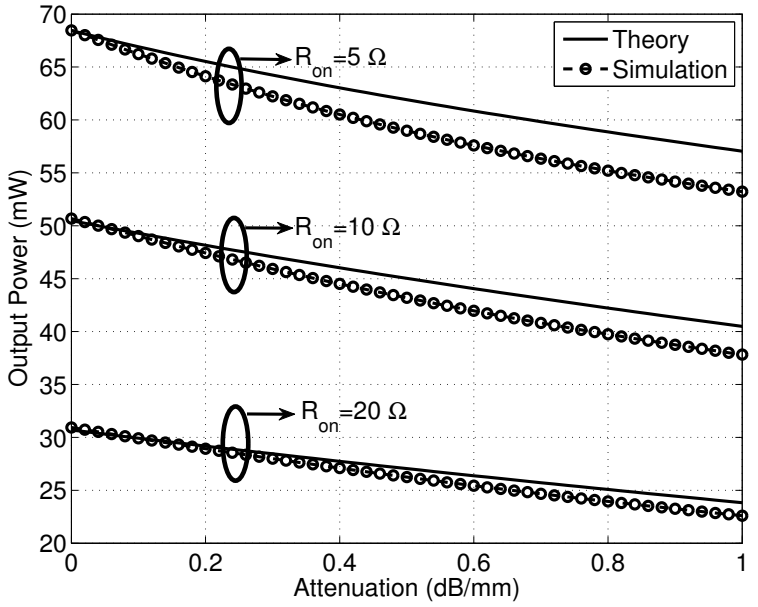

Figure 5.5: Variation of Output Power with Attenuation (for different R_{on}) for a two stage modified DSPA

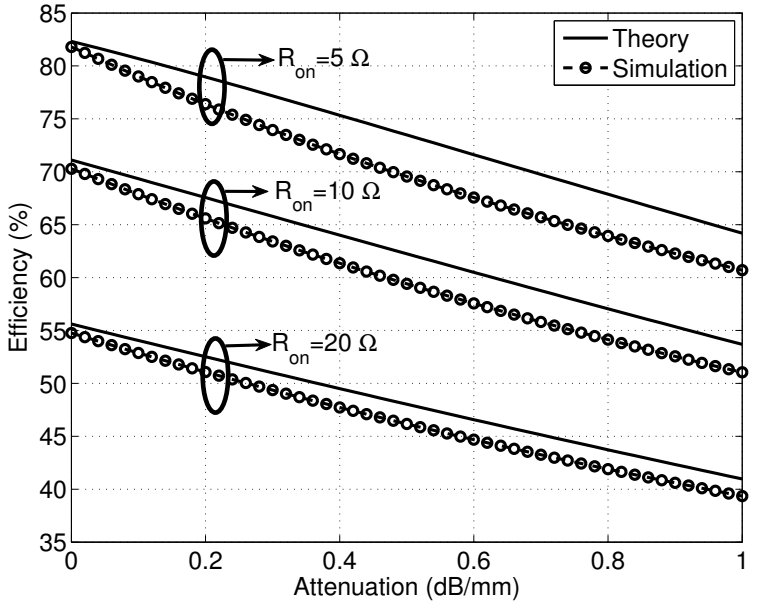

Figure 5.6: Variation of Drain Efficiency with Attenuation (for different R_{on}) for a two stage modified DSPA

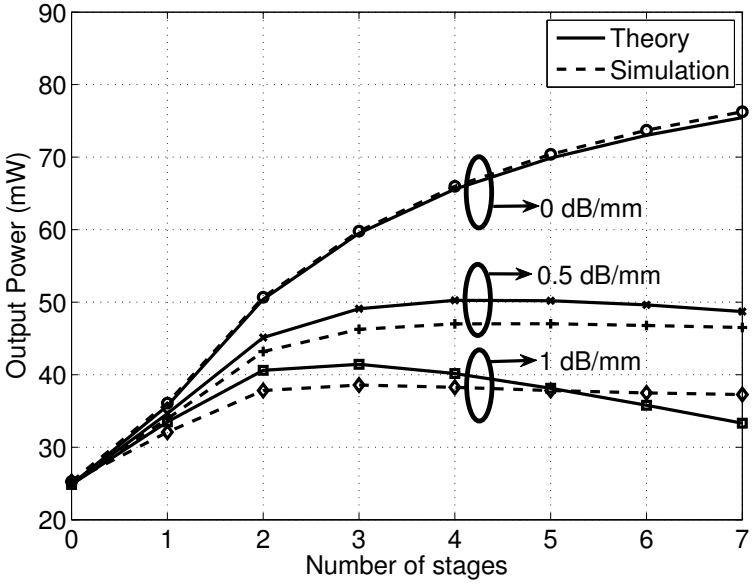

Figure 5.7: Variation of Output Power with Number of stages for an n-stage DSPA with $R_{on} = 10\,\Omega$

for the transmission line is included, we find that there exists an optimum number of stages for which the output power and efficiency is maximized. The performance of the power amplifier is affected by two factors namely the attenuation of the transmission line and the reduction in the effective switch resistance. As the number of stages is increased, the effective switch size increases and this boosts the efficiency and output power of the amplifier. Beyond a particular number of stages, the attenuation of the transmission line outweights the benefit gained by the decrease in the effective switch resistance and at this point the output power and efficiency start to reduce. For example, for an attenuation of 1 dB/mm the efficiency boost is minimal over that of a conventional amplifier ($n = 0$). However, the output power increases significantly. For an attenuation of 0.5 dB/mm, there is marked improvement over the conventional architecture. As can be seen from the plots, the theoretical analysis predicts the trend and the optimum points accurately.

Another factor which needs to be considered in the design of the DSPA is the mismatch in the length of the transmission lines. Typically, metal traces in CMOS processes are controlled pretty accurately and the tolerances are well within $\pm 10\%$. Fig. 5.9 and Fig. 5.10 show the variation of the output power and efficiency respectively as a function of the line length with a variation of $\pm 10\%$. As can be seen from the plots, the variation is high in cases where the resistance is lower. However,

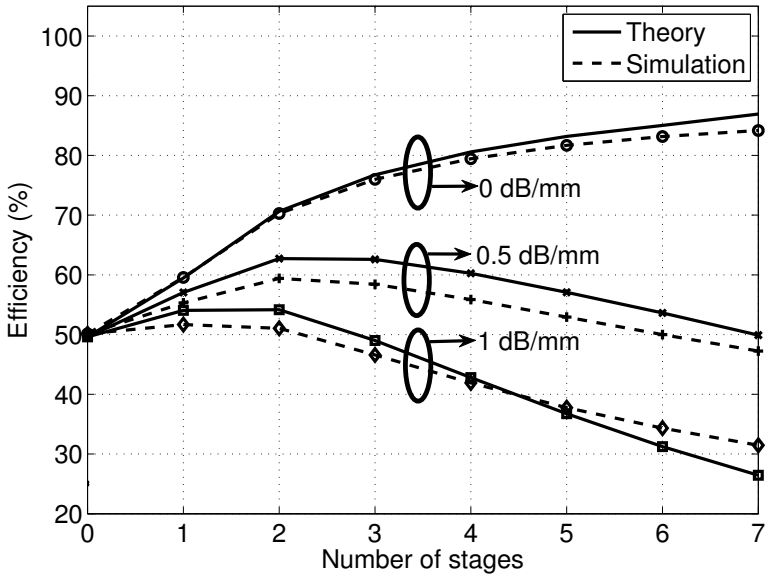

Figure 5.8: Variation of Efficiency with Number of stages for an n-stage DSPA with $R_{on} = 10\,\Omega$

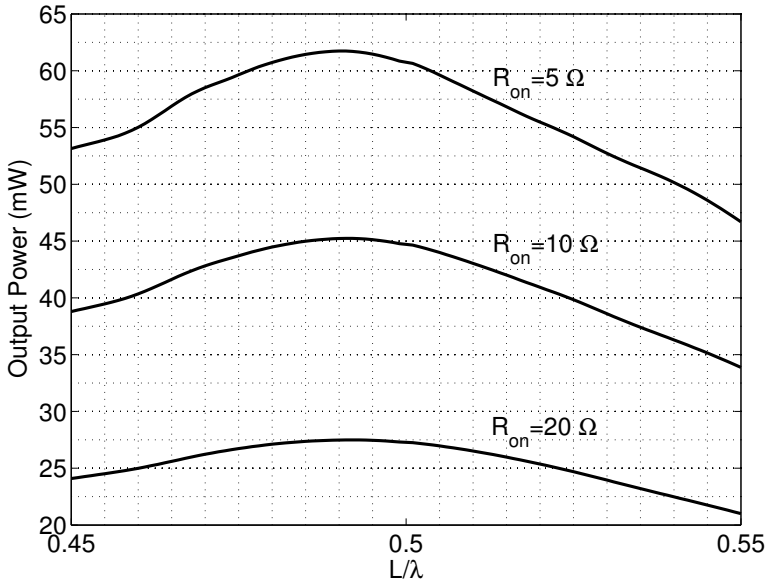

Figure 5.9: Variation of Outptut Power with the transmission line length mismatch for a two stage modified DSPA. Here the attenuation is 0.5 dB/mm

in such cases the switch size is already large and there isn't much incentive in using the DSPA architecture. The variation can also be mitigated by implementing the transmission line using lumped components but the discussion involves practical aspects and is beyond the scope of this

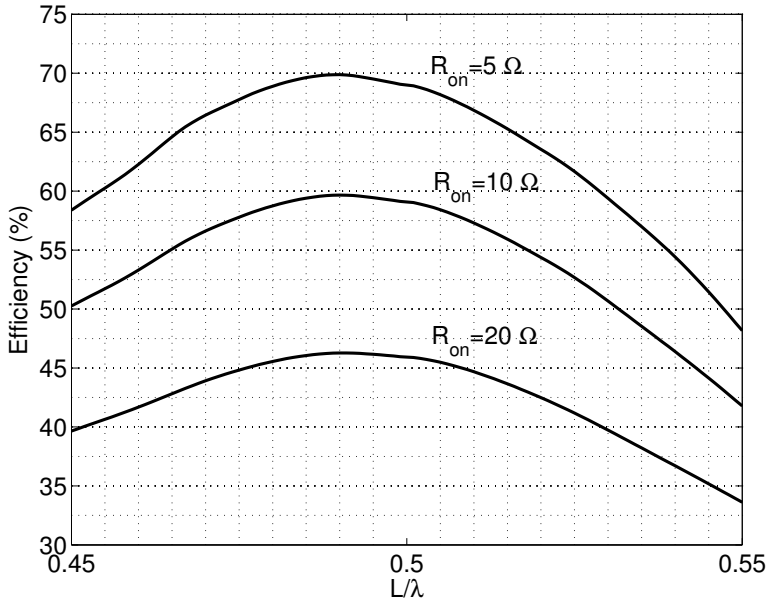

Figure 5.10: Variation of Efficiency with the transmission line length mismatch for a two stage modified DSPA. Here the attenuation is 0.5 dB/mm

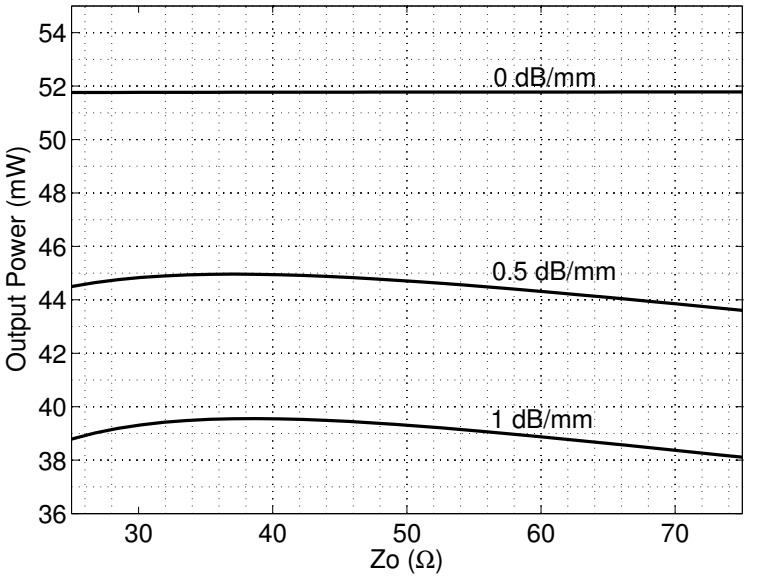

Figure 5.11: Variation of Output Power with the transmission line length characteristic impedance for a two stage modified DSPA with $R_{on} = 10\,\Omega$

report. Fig. 5.11 and Fig. 5.12 show the variation of the output power and efficiency respectively as a function of the transmission line characteristic impedance. When the line is ideal, the output

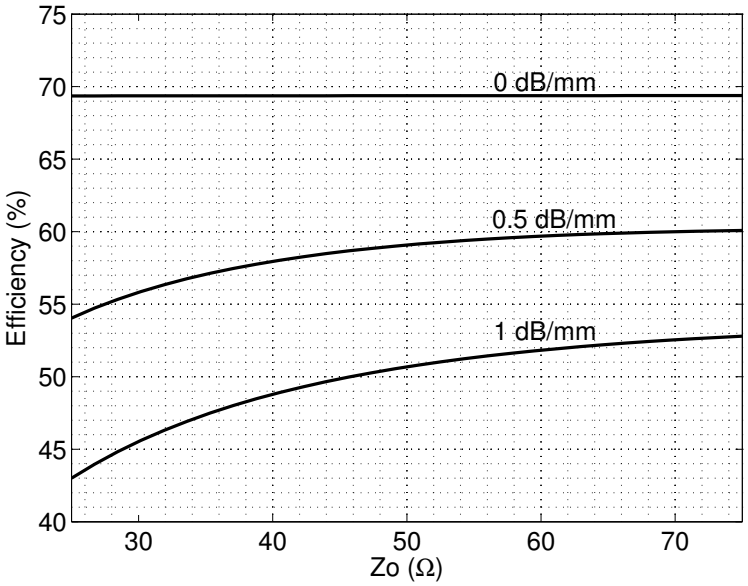

Figure 5.12: Variation of Efficiency with the transmission line characteristic impedance for a two stage modified DSPA with $R_{on} = 10\,\Omega$

power and efficiency are independent of the line characteristic impedance as was evident from the time domain analysis theory. When the transmission line has a finite attenuation, the efficiency varies slightly with the characterisitic impedance of the line (about 5% for 0.5 dB/mm and 10% for 1 dB/mm) as shown in the simulated waveform in Fig. 5.12.

Chapter 6

Conclusion

In this report, we introduced a new architecture, the Distributed Switching Power Amplifier (DSPA) that achieves higher output power and efficiency than conventional switching power amplifiers. The efficiency of a switching power amplifier is determined mainly by the realizable switch size and one always desires a larger switch size to achieve lower on-resistance. However, the parasitic capacitances of the transistor also affect the performance of the amplifier. These parasitic capacitances can be tuned out by using on-chip inductors and hence the switch size is mainly determined by the minimum realizable on-chip inductance. Also, using a larger switch size (without distribution) results in a higher quality factor for the tank which makes the design more sensitive to process variations. In this topology, the large switch is distributed across a transmission line using appropriate line lengths and clocking mechanisms. We have shown that the line length must be an integer number of the half wavelength ($n\lambda/2$) and the clocking scheme must be complementary with 50% duty cycle. A comprehensive analytical framework analyzing the power amplifier in both time and frequency domain has been developed and these were verified using system level simulation results. We also showed that the practical achievable switch size (at high frequencies) for a DSPA can be a factor of 2 compared to a conventional architecture thereby significantly boosting its efficiency.

The Digital power amplifier architecture would be an ideal candidate for the DSPA. As the efficiency of this architecture is determined mainly by the efficiency of the core unit cell, this topology would be particularly effective in boosting the overall performance of the PA. As this

architecture allows one to increase the overall implementable switch size, combining this with a cascode switch (which has high resistance) would help increase the overall output power by increasing the supply voltage. The DSPA can also serve as the core cell in a Distributed Active Transformer combined PA to simultaneously achieve high output power and efficiency. This report discusses the architecture mainly with regard to high frequency operation of the power amplifier. However, these switching amplifiers could also be used in ISM band applications where high output power is desired.

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