Low Noise Integrated CMOS Direct Conversion RF Receiver Front-End

Kai Yiu Tam

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2016-102
http://www.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-102.html

May 13, 2016

Low Noise Integrated CMOS Direct Conversion RF Receiver Front-End

by Kai Yiu Tam

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Advanced Study in Integrated Circuits, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Professor Ali Niknejad
Research Advisor

5/13/2016

(Date)

* * * * * * *

Professor Jan Rabaey
Second Reader

5/13/2016

(Date)

Abstract

Low Noise Integrated CMOS Direct Conversion RF Receiver Front-End

By

Kai Yiu Tam

Master of Advanced Study in Integrated Circuits

Electrical Engineering and Computer Science

University of California, Berkeley

Professor Ali Niknejad

A low noise direct-conversion receiver front-end has been designed in a commercial foundry 65nm CMOS process. Direct-conversion receivers (DCR) have obvious advantages over the heterodyne counterpart. The image problem has been eliminated in DCR since the intermediate frequency (IF) is zero and the image to the desired channel is the channel itself, therefore, no image reject filter is required at the front-end and the channel selection filter becomes a low-pass filter, which makes on-chip system integration easier. However, DCR suffers from several drawbacks such as performance degradation due to DC offsets, LO self-mixing, 1/f noise, even-order distortion and I/Q mismatch. A DCR front-end consists of RF band-select filter, low-noise amplifier (LNA), I/Q mixer, variable gain amplifier (VGA), low-pass filter (LPF), and an analog-to-digital converter (ADC). Main components such as LNA, I/Q mixer, and VGA have been designed and simulated with power consumption of < 2mW, programmable gain from 20dB to 80dB, input return loss of < -20 dB, overall noise figure (NF) of < 5 dB integrated from bandwidth of 1kHz to 5MHz, overall input-referred third-order intercept point (IIP_3) of > -20dBm and input-referred second-order intercept point (IIP_2) of > 10 dBm.

Contents

CONTENTS **2**

LIST OF FIGURES **4**

LIST OF TABLES **6**

1 INTRODUCTION **7**

1.1 MOTIVATION 7
1.2 OBJECTIVES 7

2 DIRECT CONVERSION RECEIVERS **8**

2.1 ARCHITECTURE AND PROCESS TECHNOLOGY 8
2.2 DC OFFSETS 11
2.3 LO SELF-MIXING 12
2.4 DISTORTION 13
2.5 1/F NOISE 14
2.6 I/Q MISMATCH 14
2.7 IMAGE REJECTION 15

3 PERFORMANCE SPECIFICATIONS **16**

3.1 PERFORMANCE PARAMETERS 16
3.2 OVERALL SPECIFICATIONS 17
3.3 NOISE/LINEARITY BUDGET 18
3.4 LNA SPECIFICATIONS 19
3.5 MIXER SPECIFICATIONS 20
3.6 VGA SPECIFICATIONS 21

4 LNA DESIGN **22**

4.1 CIRCUIT TOPOLOGY 22
4.2 INPUT MATCHING 23
4.3 NOISE FIGURE ANALYSIS 24
4.4 LINEARITY ANALYSIS 25
4.5 SIMULATIONS 26
4.6 LNA PERFORMANCE SUMMARY 33

5 MIXER DESIGN **34**

5.1 CIRCUIT TOPOLOGY 34
5.2 LO BUFFER AND I/Q GENERATION 35
5.3 IF AMPLIFIER MODELING 36
5.4 MIXER NOISE ANALYSIS 37
5.4 MIXER SIMULATIONS 39
5.5 MIXER PERFORMANCE SUMMARY 46
5.6 LNA+MIXER SIMULATIONS 46

6 VGA MODELING **53**

6.1 VGA VERILOG-A MODEL 53
6.2 SIMULATIONS 54

7 SYSTEM PERFORMANCE AND RESULTS 58

7.1 FRONT END TOP LEVEL BEHAVIORAL SIMULATIONS 58
7.2 FRONT END TOP LEVEL SIMULATIONS 59
7.3 OVERALL FRONT END PERFORMANCE 67

8 CONCLUSION 68

BIBLIOGRAPHY 69

List of Figures

Figure 1: Direct Conversion Receiver Block Diagram
Figure 2: Image problem of non-zero IF receiver
Figure 3: Simulated NMOS device characteristic
Figure 4: Effect of DC offset in Direct Conversion Receiver
Figure 5: High-level implementation of the filter for DC offset cancellation
Figure 6: LO self-mixing in frequency domain
Figure 7: High-level illustration of LO self-mixing
Figure 8: Effect of distortion in direct conversion receiver
Figure 9: Effect of I/Q mismatch on constellation
Figure 10: Double sideband noise figure
Figure 11: Intermodulation products
Figure 12: Intercept Point
Figure 13: Schematic of an inductively source degenerated cascode LNA
Figure 14: LNA Testbench
Figure 15: LNA Schematic
Figure 16: LNA Load Stability and Gain Circle
Figure 17: LNA Source Stability Circle
Figure 18: LNA operating points and performance
Figure 19: LNA noise figure versus input frequency
Figure 20: LNA power gain, max. gain, and max. stable gain versus input frequency
Figure 21: LNA S_{11} versus input frequency
Figure 22: LNA stability factor versus input frequency
Figure 23: LNA IIP_3 performance
Figure 24: LNA $P_{-1dB,i}$ performance
Figure 25: LNA IIP_2 performance
Figure 26: Current commutating passive mixer
Figure 27: CMOS LO buffer with linear amplifier and limiting amplifier
Figure 28: I/Q generation using frequency dividers with input running at double rate
Figure 29: LO switching waveforms with DC bias
Figure 30: Mixer testbench in Cadence
Figure 31: I/Q mixer core with ideal op-amp in Verilog-A
Figure 32: passive mixer core with dc gate bias
Figure 33: LO buffer operating at 2.4GHz after the I/Q generation
Figure 34: LO buffer operating at 4.8GHz for amplifying input LO to square wave
Figure 35: I/Q generation using static CMOS logic frequency dividers in 65nm
Figure 36: Simulated LO and I/Q transient waveform
Figure 37: Simulated mixer input transient waveform

Figure 38: Simulated mixer voltage conversion gain
Figure 39: Simulated mixer double-sideband noise figure
Figure 40: Simulated large signal mixer input impedance
Figure 41: Simulated mixer IIP3
Figure 42: Simulated mixer IIP2
Figure 43: Simulation testbench of LNA with mixer
Figure 44: Simulated voltage conversion gain of LNA cascading mixer
Figure 45: Simulated double-sideband noise figure of LNA cascading mixer
Figure 46: Simulated large signal S11 of LNA cascading mixer
Figure 47: Simulated large signal input impedance of LNA cascading mixer
Figure 48: Simulated IIP3 of LNA cascading mixer
Figure 49: Simulated IIP2 of LNA cascading mixer
Figure 50: Simulated input P1dB of LNA cascading mixer
Figure 51: Simulated VGA gain of 0dB at minimum gain mode
Figure 52: Simulated VGA gain of 60dB at maximum gain mode
Figure 53: Simulated VGA noise figure
Figure 54: Simulated VGA IIP3 at minimum gain mode (0dB)
Figure 55: Simulated VGA IIP3 at maximum gain mode (60dB)
Figure 56: Front End Top Level Behavioral Testbench in ADS
Figure 57: Simulated performance of the behavioral front end
Figure 58: Top level design schematic of the RF front end
Figure 59: Simulated RF front end gain at minimum gain mode
Figure 60: Simulated RF front end gain at maximum gain mode
Figure 61: Simulated RF front end double-sideband noise figure at minimum gain mode
Figure 62: Simulated RF front end double-sideband noise figure at maximum gain mode
Figure 63: Simulated RF front end S11
Figure 64: Simulated RF front end input impedance
Figure 65: Simulated RF front end LO-RF feedthrough
Figure 66: Simulated RF front end IIP3 at minimum gain mode
Figure 67: Simulated RF front end IIP3 at maximum gain mode
Figure 68: Simulated RF front end IIP2
Figure 69: Image rejection ratio (IIR) versus gain and phase imbalance

List of Tables

Table I: LNA block design constraints

Table II: Mixer block design constraints

Table III: VGA block design constraints

Table IV: LNA block design component values

Table V: LNA block design performance summary

Table VI: Mixer Design Performance Summary

Table VII: LNA+Mixer Design Performance Summary

Table VIII: RF Front End Design Performance Summary

1 Introduction

1.1 Motivation

For RF Narrowband applications, there are three possible RF receiver architectures: high-IF, low-IF and zero-IF. A zero-IF receiver has also been referred as a homodyne or direct conversion receiver (DCR) and has attracted a lot of attention lately because of possibility to integrate the complete RF receiver on a single chip.

Unlike high-IF or low-IF receivers requiring the need of very high-Q electromechanical off-chip filters for good image rejection and frequency selectivity, the DCR simply needs a low-pass filter for frequency select after down-conversion, and does not require a high speed Analog-Digital Converter (ADC) to quantize the received signal to digital domain. However, the DCR suffers from LO self-mixing, DC offset and low-frequency flicker noise, even-order distortion and I/Q mismatch. However, it is still a widely used architecture depending on application specifications.

1.2 Objectives

The objective of this study is to design a LNA, I/Q passive mixer, and VGA for a 2.4GHz RF direct conversion receiver in a commercial foundry 65nm CMOS process with a total current consumption of less than 2mW in a 1V supply, along with a set of specifications such as noise figure and linearity.

In this study, the IF amplifier employed for the passive mixer and the VGA will be designed based on behavioral models in Verilog-A. Inductors are modeled with a quality factor (Q) of 10, and capacitors are modeled with a Q of 50. The required LO voltage swing will be simulated and the LO port power consumption will be included as part of the total power consumption.

2 Direct Conversion Receivers

2.1 Architecture and Process Technology

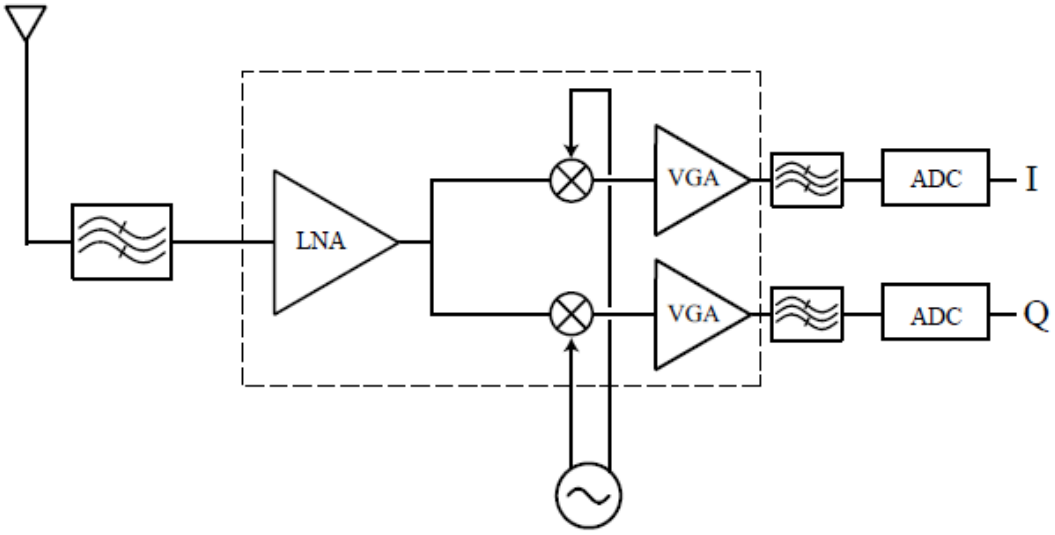

Figure 1: Direct Conversion Receiver Block Diagram

The architecture follows a direct conversion (zero-IF) topology. High level of integration , low power consumption , low cost, small form factor and the absence of image suggest that the zero-IF architecture as the best choice for the receiver. However, the problems with the zero-IF architecture i.e. DC offset, sensitivity to I/Q mismatch and flicker noise, back radiation through antenna needs to be addressed carefully. The receiver block diagram is shown in Figure 1.

Based on the system requirements, the budget analysis is performed using Excel spreadsheets. The design of the front-end involves the mapping of the specifications from the standard into relevant system-level parameters such as gain, noise-figure (NF) and the input third intercept point (IIP3). SNR is calculated at every stage in the receiver to derive the receiver noise figure requirement.

The direct conversion receiver chain is generally preceded by a TDD switch and by either a surface acoustic wave (SAW) or an on-chip LC filter in order to remove out-of-band blockers. These two components have typically a combined loss of 2dB. For the simplicity of this study, they are not included in the budget analysis because they have minimum effects on the system noise and linearity.

The filtered signal from the SAW propagates through a single ended LNA then feeds into passive mixers in the I/Q path. Local oscillator (LO) buffers and I/Q generator are designed to provide the in-phase (I) and quadrature-phase (Q) of LO signals with shape rise and fall time. The mixer is then followed by a VGA with programmable gain from

0dB to 60dB with a low-pass filter before the analog to digital converter (ADC) to ensure a constant input at the input of the ADC.

As mentioned above, the image problem has been eliminated in DCR since the intermediate frequency (IF) is zero and the image to the desired channel is the channel itself. Figure 2 shows the image problem for a non-zero IF receiver. One can observe that the positive image frequency locating at f_o-Δf gets down-converted to baseband at -Δf and the negative image frequency locating at -f_o+Δf gets up-converted to baseband at Δf. Due to this problem that the receiver cannot distinguish between desired and image signal after mixing, they are sitting on the same channel and the image signal can possibly overwhelm the desired signal or even saturate the receiver. The frequency spacing between the desired signal and image signal is 2IF, therefore impose difficulty to filter it before mixing depending on the targeted IF frequency, and cannot be filtered at the IF output.

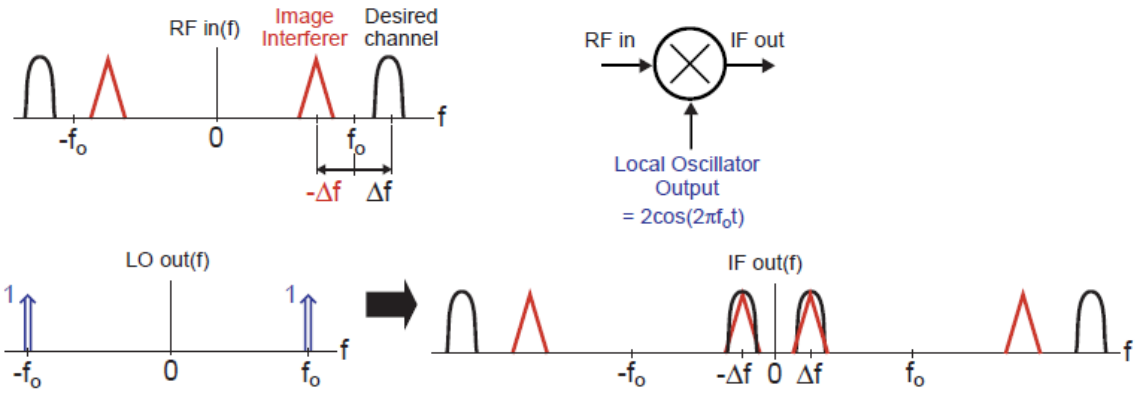

Figure 2: Image problem of non-zero IF receiver [4]

The objective of this study is to design the LNA, I/Q mixer in a commercial foundry 65nm CMOS process, while using behavioral Verilog-A models for the IF amplifier in the passive mixer, as well as the VGA. The NMOS device in this process is characterized in DC sweeping V_{gs} from 0V to V_{dd} with W/L = 10µm/0.07µm with V_{ds}=V_{dd}/2. Figure 3 shows the simulation plots of the device characteristic normalizing to 1µm. The optimum point of g_m/i_d*f_t occurs at V_{gs} of 0.4V as the bias point of the best current efficiency and speed. The simulated f_t at V_{gs} of 0.4V is 155 GHz with g_m/i_d of 9.8. Current density is 63µA/µm.

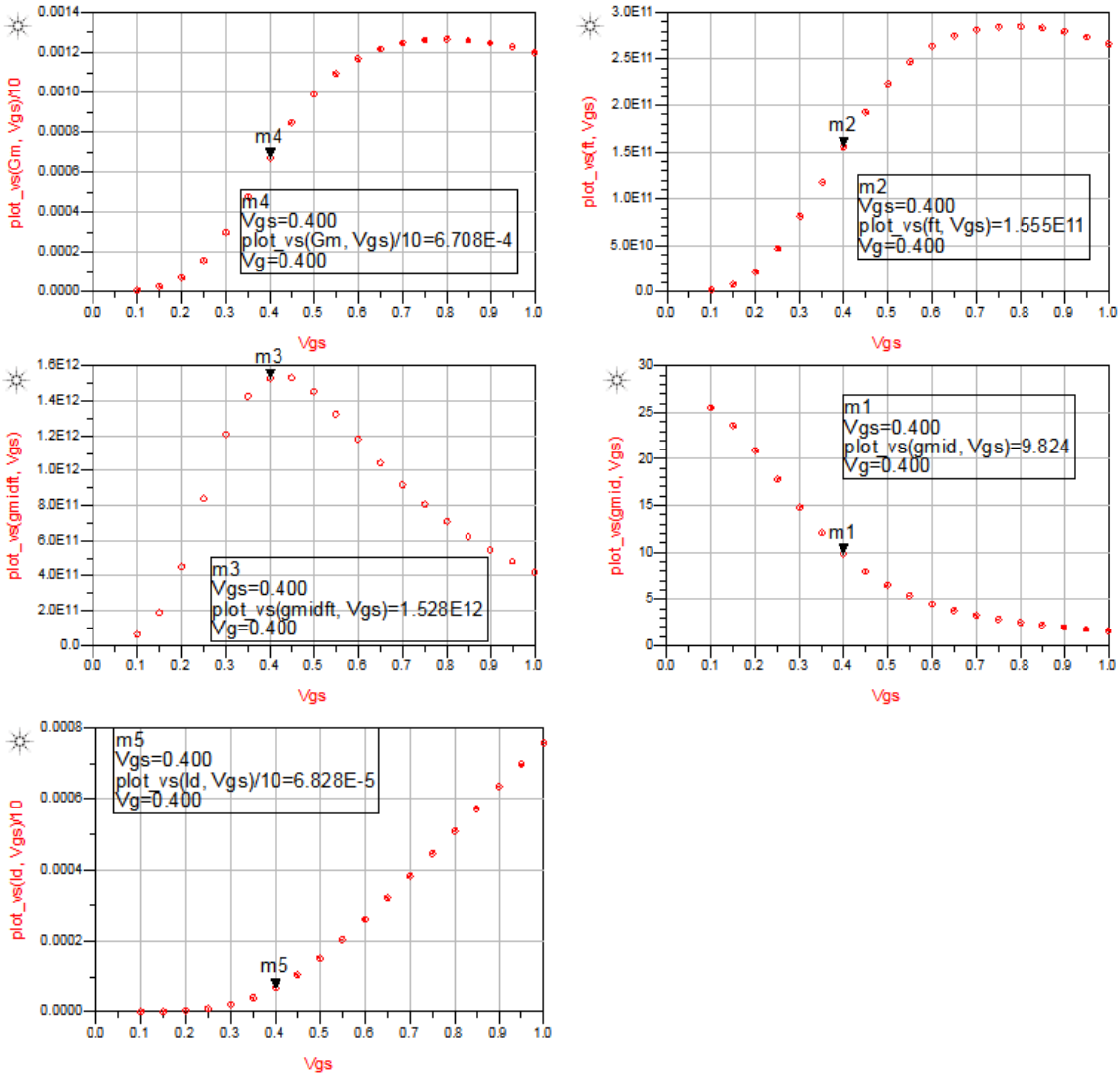

Figure 3: Simulated NMOS device characteristic

2.2 DC Offsets

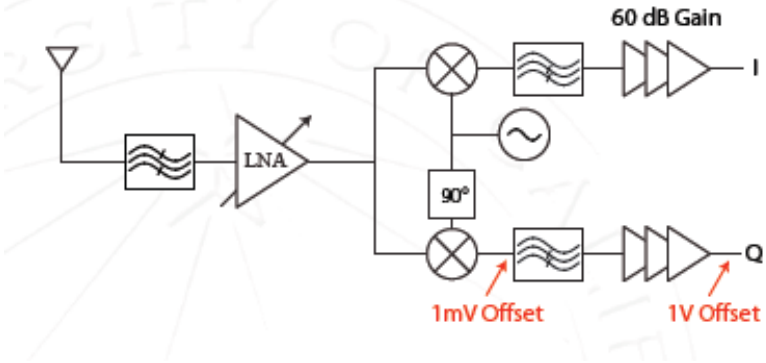

Figure 4: Effect of DC offset in Direct Conversion Receiver [3]

Figure 4 shows the effect of DC offsets in DCR. DC offsets that appear at the baseband experience a large gain from the VGA and thus can easily saturate the receiver. A large AC coupling capacitor or a programmable DC offset cancellation loop is therefore required to minimize the DC offset.

DC Offset is a key issue with zero-IF receivers. Usually DC offset is removed by high pass filtering the signal. The HPF corner should be low in the order of few kHz, which requires a large capacitor and causes any transients a large settling time as a consequence. Figure 5 shows the high-level implementation of the filter for DC offset cancellation. A G_mC filter can be used to extract the DC offset and subtract it from the output of the mixer.

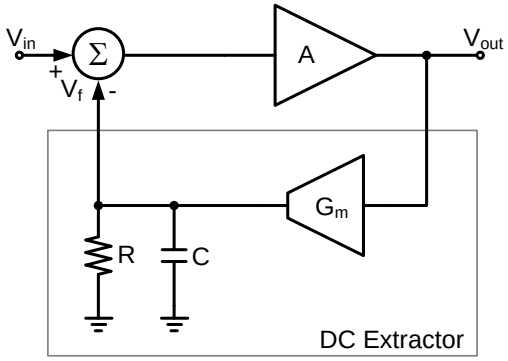

Figure 5: High-level implementation of the filter for DC offset cancellation

2.3 LO Self-mixing

LO self-mixing, also referred as self-mixing of reverse LO feedthrough can occur from the LO port to RF input port due to parasitic capacitance coupling. The LO energy can leak out of antenna and violate emission standards for radio if the isolation to antenna is inadequate due to large coupling. Moreover, LO component leaked to the mixer input, the LNA input, or the worst case back to the antenna can propagate through the mixer again and be modulated by the LO signal, therefore generating tones at DC and $2f_o$ after down-conversion at the IF output. The tone at DC due to self-mixing can cause problem and degrade the signal-to-noise ratio (SNR) for the desired output signal of DCR because their frequency contents are now combined. Figure 6 shows the consequence of LO self-mixing in the frequency spectrum and figure 7 shows a high-level illustration of LO self-mixing.

In the worst case scenario, the DC-Offset caused by LO self-mixing can be time varying if the LO signal leaks all the way back to the antenna due to insufficient isolation. The voltage standing wave ratio (VSWR) of the antenna can change if the reflected signal varies in time. Therefore we must provide high isolation from the Mixer to the antenna to prevent time-varying DC-offset.

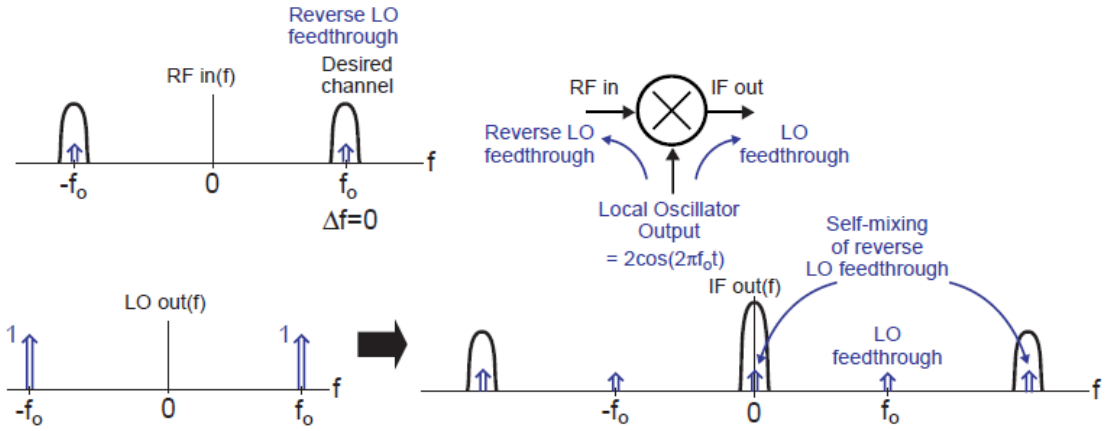

Figure 6: LO self-mixing in frequency domain [4]

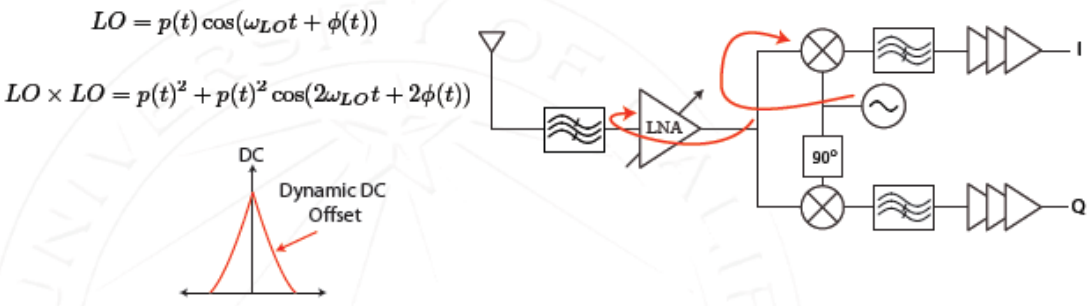

Figure 7: High-level illustration of LO self-mixing [3]

2.4 Distortion

Normally we concern more about odd-order intermodulation effects in RF receivers because they are located near the desired signal and cannot be filtered out easily. For superheterodyne receivers, they occur at RF input frequencies where RF ± LO = IF, while for the DCR they occur where RF - LO = 0. When a blocking signal carrier frequency falls on one of these spurious frequencies, the signal is then converted to baseband and degrades the linearity.

Due to the second-order nonlinearity of the mixer, a DC tone can be produced at the mixer output and amplified by the baseband stages. This can be further characterized by the second-order intercept point (IP2) and can be minimized by extremely well-balanced circuit design. However, the antenna and the RF band-select filter are usually single-ended, and thus requiring either the LNA or mixer to be singled-ended, or with an additional balun to convert from single-ended to differential which will introduce an additional loss at the input of approximately 2 to 3 dB.

Moreover, large blocking signals can also generate a DC tone in DCR, whether on a spurious frequency or not. Assume two jammers have a frequency separation of Δω: The two produce distortions at DC as show in the derivation below [3]. The modulation of the jammers gets doubled in bandwidth and then their intermodulation product can also fall into the band of the receiver and possibly saturate the receiver if the jammers are close together, even if they are out of band. Figure 8 shows the illustration of low frequency tone generated at the RF input by the nonlinearity of the LNA due to the two interferers S_1 and S_2.

$$s_1 = m_1(t)\cos(\omega_1 t)$$

$$s_2 = m_2(t)\cos(\omega_1 t + \Delta\omega t)$$

$$(s_1 + s_2)^2 = (m_1(t)\cos\omega_1 t)^2 + (m_2(t)\cos\omega_2 t)^2 + 2m_1(t)m_2(t)\cos(\omega_1 t)\cos(\omega_1 + \Delta\omega)t$$

$$\mathrm{LPF}\{(s_1 + s_2)^2\} = m_1(t)^2 + m_2(t)^2 + m_1(t)m_2(t)\cos(\Delta\omega)t$$

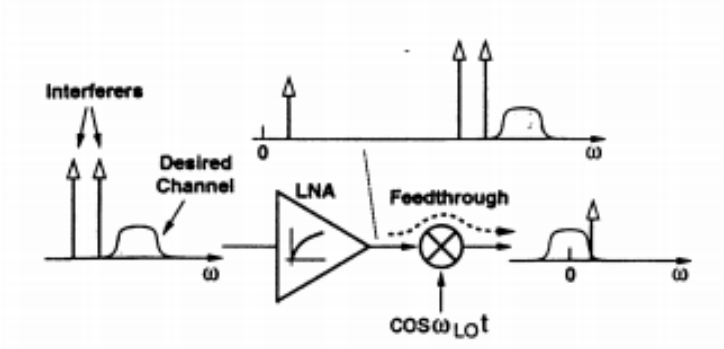

Figure 8: Effect of distortion in direct conversion receiver [1]

2.5 1/f Noise

Since the IF is at DC, any low frequency noise, such as flicker (1/f) noise can dramatically impact the overall noise figure of the receiver. Compared to Bipolar device, CMOS has much higher 1/f noise and requires careful device sizing (e.g. large device size after down-conversion for low 1/f noise while achieving required speed) and sometimes additional circuit design techniques (e.g. periodic offset cancellation techniques [1]) to ensure low 1/f noise contribution.

2.6 I/Q Mismatch

A DCR uses two channels to form the I/Q components of the received signal respectively. Each channel consists of a mixer, VGA, LPF and ADC. The mismatch between the LPF and the mismatch between the LO in I and Q paths can corrupt the received signal and severely distort the SNR. As seen in figure 9 constellation diagram, the I/Q gain imbalance appears as a non-unity scale factor in the amplitude while the I/Q phase imbalance corrupts one channel with a fraction of data pulses in the other channel.

Due to the LO operating at relatively high frequency, it is not possible to implement a I/Q demodulator digitally for good I/Q matching. An analog IQ demodulator exhibits gain and phase imbalances between the two branches, corrupts the downconverted signal constellation and thus raising the bit error rate. In DCR systems, I/Q matching is not as critical as in image-rejection architectures. A 5˚ phase imbalance results in 1 dB of SNR degradation in DCR while only 27 dB of image rejection in image rejection architectures. [1]

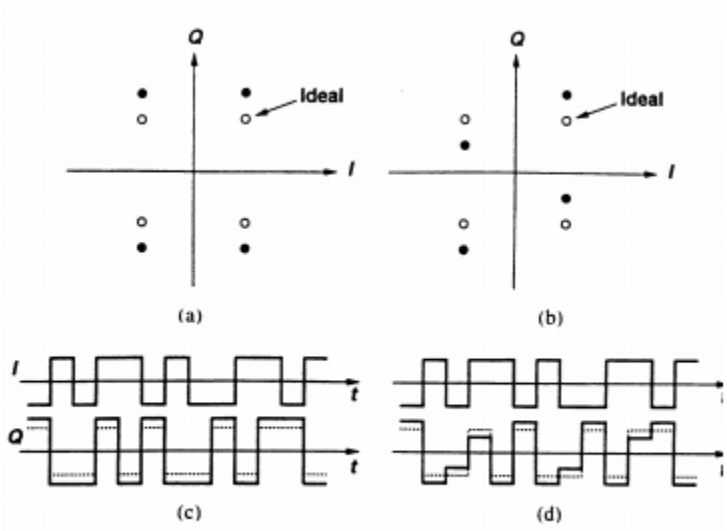

Fig. 7. Effect of I/Q mismatch. Constellation (a) with gain error.; (b) with phase error. Time-domain waveforms (c) with gain error; (d) with phase error.

Figure 9: Effect of I/Q mismatch on constellation [1]

2.7 Image Rejection

In a DCR, the image is the desired signal itself after downconversion. However, DCR also needs image reject because we may sometimes want to send different data in positive and negative frequency. Such rejection coming from the I+jQ calculation in BB, and how good of the IRR depends on I/Q mismatch. Based on the typical DCR architecture, we can write the quadrature signals with gain and phase mismatch on I/Q as:

$$\mathrm{LO_I}(t) = A_{LO}\cos(\omega_{LO}t)$$

$$\mathrm{LO_Q}(t) = -(A_{LO} + \Delta A_{LO})\sin(\omega_{LO}t + \theta)$$

Consider input as RF(t) feeding into the mixer in both I and Q channel, we can write the receiver output I+jQ as:

$$\mathrm{I + jQ} = \mathrm{RF(t)}[A_{LO}\cos(\omega_{LO}t) - j(A_{LO} + \Delta A_{LO})\sin(\omega_{LO}t + \theta)]$$

$$= \mathrm{A_{LO}}RF(t)[\cos(\omega_{LO}t) - j\varepsilon\sin(\omega_{LO}t + \theta)] \text{ where } \varepsilon = \frac{A_{LO}+\Delta A_{LO}}{A_{LO}}$$

$$\mathbf{I + jQ} = \frac{\mathbf{RF(t)A_{LO}}}{\mathbf{2}}[(\mathbf{1} - \boldsymbol{\varepsilon}\cdot\boldsymbol{e}^{j\theta})\boldsymbol{e}^{j\omega_{LO}t} + (\mathbf{1} + \boldsymbol{\varepsilon}\cdot\boldsymbol{e}^{-j\theta})\boldsymbol{e}^{-j\omega_{LO}t}]$$

Therefore, we can express image rejection ratio IRR as:

$$\mathrm{IRR_{dB}} = 10\log_{10}\left(\frac{|1 + \varepsilon\cdot e^{-j\theta}|}{|1 - \varepsilon\cdot e^{j\theta}|}\right) = 10\log_{10}\left(\frac{\varepsilon^2 + 1 - 2\varepsilon cos\theta}{\varepsilon^2 + 1 + 2\varepsilon cos\theta}\right)$$

Normally, if DCR does not require very high IRR, for example: IRR between 30 and 40-dB, meaning that there is a possible combination of 0.2 to 0.6-dB gain mismatch and 5˚ to 15˚ of phase imbalance. [8] Layout matching and circuit parasitics are therefore critical make sure layout symmetry between I/Q and thus minimize I/Q mismatch.

3 Performance Specifications

3.1 Performance Parameters

Based on the system requirements, the budget analysis is performed using Excel spreadsheets. The design of the front-end involves the mapping of the specifications from the standard into relevant system-level parameters such as gain, noise-figure (NF) and the input third intercept point (IIP3). SNR is calculated at every stage in the receiver to derive the receiver noise figure requirement.

In DCR, there is no image band and therefore the noise from positive and negative frequencies combine at zero IF, as well as the signal itself. Double-sideband (DSB) noise figure is therefore used to capture the actual SNR because of the contribution from both sidebands. Figure 10 shows a graphical representation of how signal and noise from both sidebands get converted to the same zero IF.

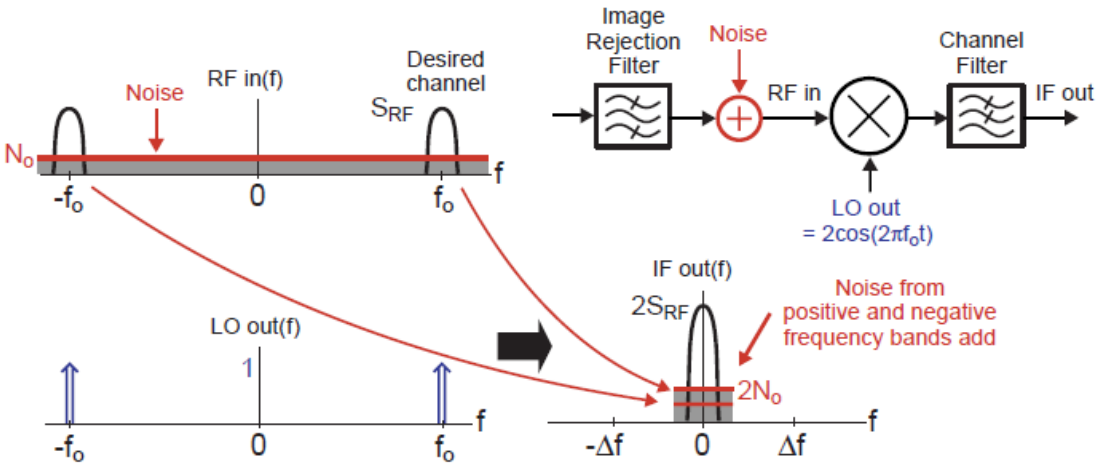

Figure 10: Double sideband noise figure [4]

Due to the nonlinearity of the circuit, we can describe a function y(t) = f(x(t)) where f(x) is:

$$f(x) = a_1 x + a_2 x^2 + a_3 x^3 + \cdots$$

,and therefore one can see that y(t) has frequency components not present in input due to the nonlinearity of the circuit. In DCR, we are more concern about nonlinearity due to intermodulation products from two closely-spaced tones. Figure 11 shows a simple illustration of the location in frequency of intermodulation products we concern the most: IM_2 and IM_3. In DCR, IM_2 products fall at much lower (DC, important due to DC content of baseband signal) and higher frequencies ($2\omega_o$). The IM_2 at $2\omega_o$ appear as interference to others but can be attenuated by filtering, while IM_3 products cannot be filtered for two close tones due to too close to the RF input tone. Figure 12 shows the curve of fundamental tone, IM_2 and IM_3 versus input strength. The metric IIP_2 and IIP_3 are defined as the input strength when IM_2 and IM_3 are 0 dBc respectively.

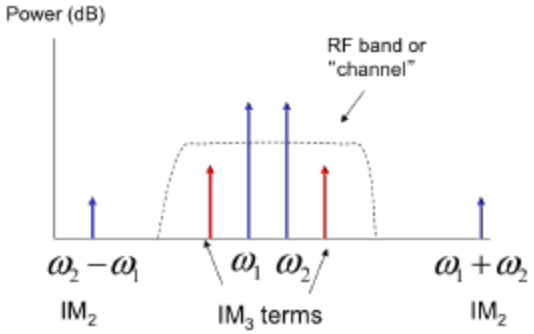

Figure 11: Intermodulation products [3]

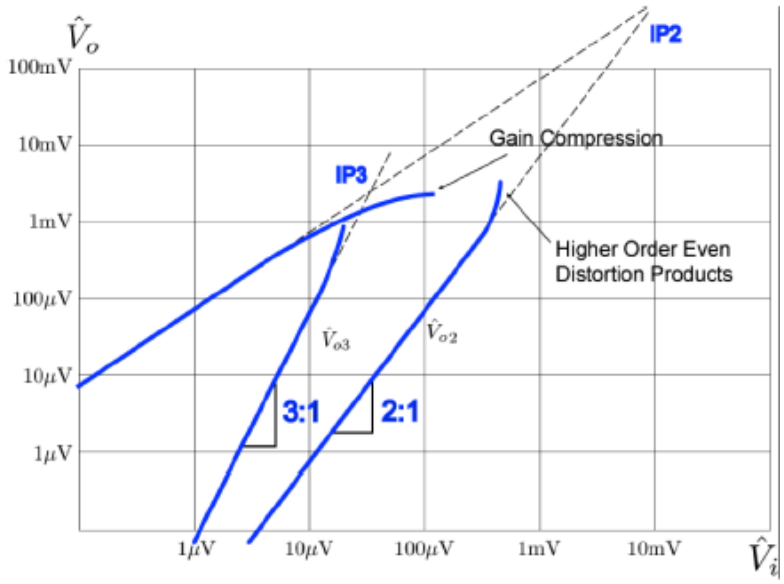

Figure 12: Intercept Point [3]

3.2 Overall Specifications

This integrated CMOS direct conversion receiver front-end operates in the 2.4 GHz band with 5 MHz channel bandwidth and is designed and simulated in a commercial foundry 65nm CMOS process. The specifications for the design are summarized below:

- Total current consumption of less than 2mW in a 1V supply.
- Power gain programmable from 20dB to 80dB.
- System noise figure of 5 dB (highest gain). Integrate the noise figure from 1 kHz to 5 MHz.
- Input match better than 20 dB, Zin = 50Ω. Drive a load capacitance of 1pF.
- A third-order linearity better than IIP3 > -20 dBm.
- Second order linearity IIP2 > +10 dBm.

- LO leakage at the LNA input: -100 dBm max.
- Image rejection 40 dB.

3.3 Noise/Linearity Budget

System noise figure specification = 5 dB (highest gain = 80dB)

- $G_{LNA} = 15dB$
- $G_{MIXER} = 5dB$
- G_{VGA} = 60dB

$$F = F_{LNA} + \frac{F_{MIXER} - 1}{G_{LNA}} + \frac{F_{VGA} - 1}{G_{LNA}G_{MIXER}}$$

Assume the RF filter and BB filter have zero insertion loss for simplicity, therefore their noise figures are both 0 dB.

We know that system noise figure will be mainly dominated by LNA. Assume mixer has a noise figure of 10dB and VGA has a noise figure of 20dB:

$$10^{\frac{NF}{10}} = 10^{\frac{NF_{LNA}}{10}} + \frac{10^{\frac{NF_{MIXER}}{10}} - 1}{G_{LNA}} + \frac{10^{\frac{NF_{VGA}}{10}} - 1}{G_{LNA}G_{MIXER}}$$

$$10^{\frac{5}{10}} = 10^{\frac{NF_{LNA}}{10}} + \frac{10^{\frac{10}{10}} - 1}{10^{\frac{15}{10}}} + \frac{10^{\frac{20}{10}} - 1}{10^{\frac{15}{10}}10^{\frac{5}{10}}}$$

$$3.16 = 10^{\frac{NF_{LNA}}{10}} + \frac{10 - 1}{31.62} + \frac{100 - 1}{31.62 * 3.16}$$

$$\mathbf{NF_{LNA} < 2.76\ dB}$$

We know that the corresponding input voltage for P1dB,i of VGA is 100mV$_{rms}$, therefore we can find that

$$V_{IIP3,VGA} = \frac{100mV}{\sqrt{0.11}} = 301.5mV_{rms}$$

$$\mathbf{IIP3_{VGA} = 10\log\left(\frac{301.5mV^2}{50} * 1000\right) = 2.6\ dBm\ (50ohm)}$$

$$\mathbf{IIP3_{VGA} = 10\log\left(\frac{301.5mV^2}{10k\Omega} * 1000\right) = -20.4\ dBm\ (10kohm)}$$

From spec. we know that the overall IIP3 must be > -20 dBm:

$$V_{IIP3,TOT} = \sqrt{P_{IIP3} * R} = \sqrt{10^{-\frac{20}{10}} * 1mW * 50} = 22.4\ mV_{rms}$$

We can specify the IIP3 of LNA and mixer with the following equation:

$$\frac{1}{\mathrm{V}_{\mathrm{IIP3,TOT}}^2} = \frac{1}{V_{IIP3,LNA}^2} + \frac{G_{LNA}}{V_{IIP3,MIXER}^2} + \frac{G_{LNA}G_{MIXER}}{V_{IIP3,VGA}^2}$$

$$\frac{1}{22.4\mathrm{mV}^2} = \frac{1}{V_{IIP3,LNA}^2} + \frac{10^{\frac{15}{10}}}{V_{IIP3,MIXER}^2} + \frac{10^{\frac{15}{10}}10^{\frac{5}{10}}}{301.5mV^2}$$

The input of the mixer will have a larger input swing than the input of the LNA, to make sure both blocks are linear:

Assume $\frac{1}{V_{IIP3,LNA}^2} = \frac{G_{LNA}}{V_{IIP3,MIXER}^2}$

$$\frac{1}{\mathrm{V}_{\mathrm{IIP3,TOT}}^2} = \frac{2}{V_{IIP3,LNA}^2} + \frac{G_{LNA}G_{MIXER}}{V_{IIP3,VGA}^2}$$

$$\frac{1}{22.4\mathrm{mV}^2} = \frac{2}{V_{IIP3,LNA}^2} + \frac{10^{\frac{15}{10}}10^{\frac{5}{10}}}{301.5mV^2}$$

$$V_{IIP3,LNA} = 47.3\mathrm{mV}_{\mathrm{rms}}$$

$$\mathbf{IIP3_{LNA}} = \mathbf{10}\boldsymbol{log}\left(\frac{\mathbf{47.3}\boldsymbol{mV^2}}{\mathbf{50}} * \mathbf{1000}\right) = \mathbf{-13.5\ dBm}$$

$$\mathrm{V}_{\mathrm{IIP3,MIXER}} = \sqrt{G_{LNA}} * V_{IIP3,LNA} = \sqrt{10^{\frac{15}{10}}} * 47.3mV = 266mV_{rms}$$

$$\mathbf{IIP3_{MIXER}} = \mathbf{10}\boldsymbol{log}\left(\frac{\mathbf{266}\boldsymbol{mV^2}}{\mathbf{50}} * \mathbf{1000}\right) = \mathbf{1.51}\ \boldsymbol{dBm}$$

3.4 LNA Specifications

LNA Design Intro and Challenges

To establish a starting point of the design, DC device characteristic was simulated by sweeping V_{gs} with W=10µm, L=L_{min}=70nm and V_{ds}=V_{dd}/2=0.5V as shown in figure 3 before. For both low power and high speed, it was found that the peak of $g_m/i_d * f_t$ occurs at V_{gs}=0.4V. However, we will need to confirm whether this bias condition can satisfy the noise figure and linearity requirement, and can achieve input matching with reasonable component values (e.g. realizable on-chip inductors with Q_L=10 and capacitors with Q_C=50), due to tradeoffs between power, linearity and noise. Due to the total power consumption budget of 2 mW, 800 µA is set as the target current consumption of the LNA. Table I shows the LNA block design constraints.

LNA Design constraints:

Parameter	Value
V_{DD}	1 V
I_{DD}	< 800 µA
Operating Frequency	2.4GHz ± 5MHz
Gain (S_{21})	~ 15 dB
NF	< 2.76 dB
IIP3	> -13.5 dBm
IIP2	> +10 dBm (for the overall system)
P_1dB,i	> -23.1 dBm
S_{11}	< -20 dB
K	> 1 (unconditionally stable)

3.5 Mixer Specifications

In this study, a 4.8GHz LO is used for generating I/Q signals conveniently with CMOS frequency dividers. LO buffers operating at 4.8GHz are also designed to amplifier the input LO signals to CMOS-level full swing. The IF amplifier for converting current into voltage of the passive mixer will be designed based on an ideal behavioral model of a fully differential op-amp in Verilog-A. The current consumption budget for this block is targeted to be < 1 mA. Table II shows the mixer design constraints.

Mixer Design constraints:

Parameter	Value
V_{DD}	1 V
$I_{DD,AVG}$	< 1 mA (including LO buffer, IQ generator)
LO port power consumption	< 200 µA
$I_{tot,avg}$	< 1.2 mA
Load	10 kohm
RF Input Frequency	2.4GHz ± 5MHz
LO Input Frequency	4.8 GHz
I/Q LO Input	2.4 GHz
IF Output Frequency	0 Hz – 5 MHz
Voltage Conversion Gain	5 dB
NF	< 10 dB
IIP3	> 1.51 dBm
IIP2	> +10 dBm (for the overall system)

3.6 VGA Specifications

The VGA which provides programmable gain from 0dB to 60dB will be designed based on behavioral models in Verilog-A, including accurate models on noise figure and IIP_3 linearity. Table III shows the VGA design constraints.

VGA Design constraints:

Parameter	Value
Input Frequency (IF)	0 Hz – 5 MHz
Gain	0 dB to 60 dB progammable
NF	20 dB
V_{IIP3}	301.5 mVrms
Input impedance	10 kohm
Output impedance	10 kohm // 1 pF

4 LNA Design

4.1 Circuit Topology

Since the Noise Figure (NF) of total receiver chain highly depends on Low Noise Amplifier (LNA), LNA is one of the most important parts of the front end of RF receiver. The inductively source degenerated cascode LNA which is shown in Figure 13, is most commonly used tuned amplifier for narrowband. Our receiver can be regarded as a narrow band (2.4GHz ± 5MHz), which is one of the reason why this topology is chosen.

Input impedance is matched 50 ohm antenna, but the output impedance is matched to a load value depending on the LNA design with gain circle.

The purpose of putting an LNA as the first stage in the receiver architecture is to reduce the noise figure of the entire system by having a large gain as can be seen from Friis noise equation. In typical receivers, it is common to use a single-ended LNA because the antenna and the RF band select filter are also single-ended, and it consumes half the power while being able to meet the noise and linearity specification.

There are many topologies of LNA in literatures. For example, a simple common source amplifier can provide high enough gain to minimize the overall noise figure. However, the resistor at the load is noisy and would therefore contribute noise to the LNA output. In order to solve this problem, one approach is to inductively load the common source to provide better noise performance. The disadvantage of this approach is mainly area because inductors are large and are difficult to achieve high qualify factor on-chip. The other approach is to choose a common-gate–common-source topology in which the noise of the common gate transistor can be canceled. [10] However, this approach will consume high power and provides wideband amplification which is not necessary in a narrowband receiver.

The LNA in this study was designed using an inductively degenerated common source with inductive load to achieve the required noise and linearity. The amplifier is also cascoded to provide higher reverse isolation (amplifier is more unilaterial) to minimize LO self-mixing due to feedthrough from device and layout parasitics.

4.2 Input Matching

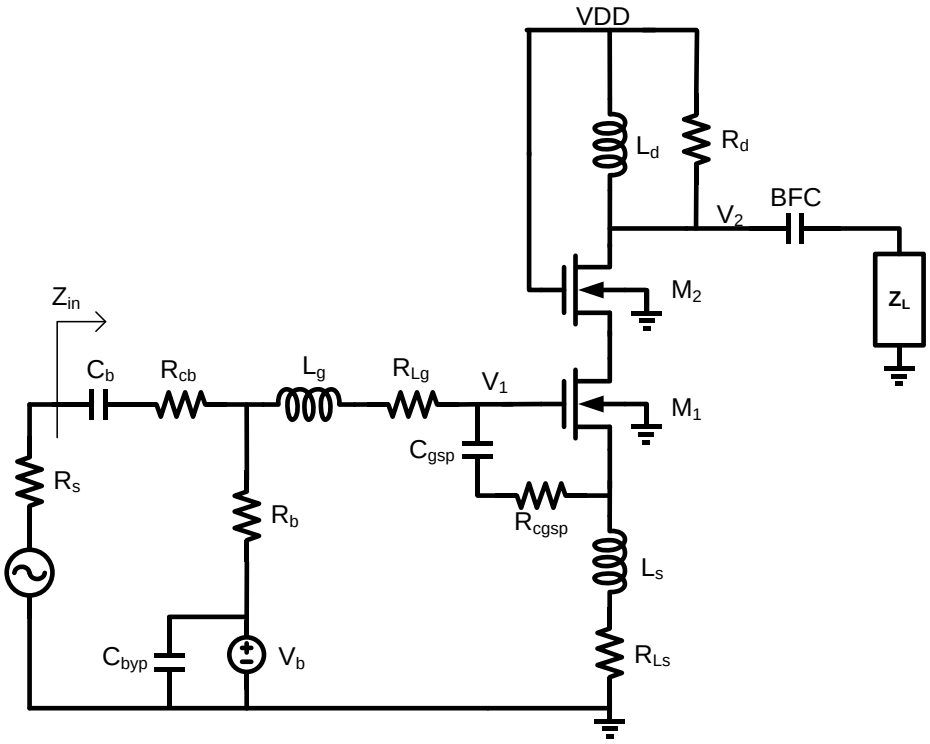

Figure 13: Schematic of an inductively source degenerated cascode LNA

The schematic of the designed LNA is shown above. A common source configuration is chosen to achieve lower NF_{min} compared to a common gate configuration, and a cascode device M_2 is added to make the 2 port more unilateral. Inductor L_s acts as inductive degeneration on M_1 to provide a broadband programmable real input impedance to simplify the input matching. Capacitors C_{gsp} is placed in parallel with C_{gs} to intentionally de-Q the input network so that the input matching bandwidth is wider, less sensitive to component variations, and easier for inductor L_s to be integrated on chip.

For this design, output matching to 50ohm is not necessary as the next stage is mixer. As a result, the load is kept ideal in the simulation and will match the conjugate of the input impedance of the mixer to this value to preserve the gain of LNA. The load is also chosen to be relatively low Q and reasonable values for ease of matching.

The bias tee is designed by AC coupling the input with a large resistor to provide the DC bias to the LNA. Knowing that the AC coupling capacitor C_b and its associated loss can be negligible by design at 2.4GHz, the input impedance Z_{in} can be written as the following: (C_{gd} ignored)

$$Z_{in} \cong \left[j\omega\left(L_s + L_g\right) + \frac{1}{j\omega\left(C_{gs} + C_{gsp}\right)} + \frac{\omega_T R_{LS}}{j\omega} + \omega_T L_s + R_{LS} + R_{Lg} + R_g \right] // R_b$$

Where $R_{LS} = \frac{\omega L_s}{Q_L}$, $R_{Lg} = \frac{\omega L_g}{Q_L}$, $R_g = \frac{1}{5g_m}$

We can observe that the resonance occurs when $j\omega(L_s + L_g) - j\frac{1}{\omega}\left(\frac{1}{C_{gs}+C_{gsp}} + \omega_T R_{LS}\right) = 0$ and can design $(\boldsymbol{\omega_T L_s + R_{LS} + R_{Lg} + R_g)//R_b = R_s = 50\ ohms}$

4.3 Noise Figure Analysis

We can derive the noise figure of the LNA, making simplification on cascade contributes no noise to output, ignoring C_{gd}, body effect, loss from capacitors C_b, C_{gsp} and loss from L_s.

$$F = 1 + \frac{R_g}{R_s} + \frac{R_{Lg}}{R_s} + \frac{\frac{4kT}{R_b}\left(\frac{R_s}{R_{Lg}+R_g+\omega_T L_s+R_s}\right)^2\left(\frac{1}{\omega(C_{gs}+C_{gsp})}\right)^2 (g_m R_d)^2}{4kTR_s(G_m R_d)^2} + \frac{\frac{1}{4}4kT\gamma g_m}{4kTR_s G_m^2} + \frac{4kTR_d}{4kTR_s(G_m R_d)^2}$$

$$F = 1 + \frac{1}{5g_m R_s} + \frac{R_{Lg}}{R_s} + \frac{4R_s^3}{R_b\left(R_{Lg}+R_g+\omega_T L_s+R_s\right)^2} + \gamma g_m R_s\left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_d}\left(\frac{\omega_o}{\omega_T}\right)^2$$

$$\boldsymbol{F = 1 + \frac{1}{5g_m R_s} + \frac{R_{Lg}}{R_s} + \frac{4R_s^3}{R_b\left(R_{Lg}+R_g+\omega_T L_s+R_s\right)^2} + \gamma g_m R_s\left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_d}\left(\frac{\omega_o}{\omega_T}\right)^2}$$

Where, $R_{Lg} = \frac{\omega_o L_g}{Q_L}$, $R_d = \omega_o L_d Q_L$, $G_m = Q g_m = \frac{g_m}{\omega_o 2R_s(C_{gs}+C_{gsp})}$

At V_{gs}=0.4V, the transistor has g_m/i_d = 9.8 from the characteristic simulation, yielding g_m of 4.9mS for i_d of 500µA. If we allow maximum inductor size of 15nH (j226Ω at 2.4GHz), we will constraint degrading f_T to a minimum of 5.3GHz.

With $\gamma = \frac{2}{3}$, L_g=L_d=15nH, L_s=500pH and R_s=50Ω F = 2.328 => NF = 3.67 dB which is greater than the required spec of 2.76dB

In order to meet all specifications, it is found that the optimum bias point for highest $g_m/i_d * f_t$ cannot achieve low enough noise figure for the LNA (NF < 2.76dB), which agrees with above analysis due to insufficient transconductance g_m.

In order to boost up transconductance for lower NF while keeping the current consumption low, the design is then revised and the input transistor of LNA is pushed to subthreshold with V_{gs}=0.25V, allowing g_m/i_d = 21.6, with f_T of 5.8GHz and g_m of 12.46mS as showing on the operating point simulation below, while keeping low current consumption of 577µA.

With $\gamma = \frac{2}{3}$, the new design is calculated to have F = 1.867 => NF of 2.71dB, which agrees reasonably well with the simulated NF of 2.4dB and met the LNA NF requirement.

4.4 Linearity Analysis

Lastly, we need to meet the specification of linearity, i.e. IIP_3. Since the input transistor M_1 is now biased at subthreshold, we expect the I-V characteristic of M_1 behaves like a bipolar device.

To analyze the IM_3 product of two closely-spaced tones, we can simplify the LNA with an equivalent circuit in the passband of the matching network and assume the amplifier is memoryless for analysis simplification, however we will need to neglect the load in the analysis since it is not pure resistive at the operating frequency due to the choice of loading from gain circle.

In subthreshold, we have: (channel length modulation ignored)

$$i_d = I_{DS}\left(e^{\frac{qv_{gs}}{nkT}} - 1\right) = I_{DS}\left(\frac{v_{gs}}{nV_T} + \frac{1}{2n^2V_T^2}v_{gs}^2 + \frac{1}{6n^3V_T^3}v_{gs}^3 + \cdots\right)$$

where $v_s = Qv_{gs},\ Q \cong \frac{1}{2R_s\omega_o(C_{gs}+C_{gsp})} = \frac{\omega_T}{2R_s\omega_o g_m}$

$$i_d = I_{DS}\left(e^{\frac{qv_{s/Q}}{nkT}} - 1\right) = I_{DS}\left(\frac{v_s}{QnV_T} + \frac{1}{2Q^2n^2V_T^2}v_s^2 + \frac{1}{6Q^3n^3V_T^3}v_s^3 + \cdots\right)$$

Where I_{DS} is the designed quiescent current (i.e. at V_{gs}=0.25V), $V_T = kT/q$

$$a_1 = \frac{I_{DS}}{QnV_T} = \frac{I_{DS}}{nV_T}\frac{\omega_T}{2R_s\omega_o g_m}$$

$$a_2 = \frac{1}{2}\frac{I_{DS}}{(QnV_T)^2} = \frac{1}{2}\frac{I_{DS}}{n^2V_T^2}\left(\frac{\omega_T}{2R_s\omega_o g_m}\right)^2$$

$$a_3 = \frac{1}{6}\frac{I_{DS}}{(QnV_T)^3} = \frac{1}{6}\frac{I_{DS}}{n^3V_T^3}\left(\frac{\omega_T}{2R_s\omega_o g_m}\right)^3$$

$$\boldsymbol{IIP_3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} = \frac{\sqrt{32}nV_T g_m R_s\omega_o}{\omega_T} = \frac{\sqrt{32}I_{DS}R_s\omega_o}{\omega_T}}$$

With the design of subthreshold with V_{gs}=0.25V, allowing g_m/i_d = 21.6, with f_T of 5.8GHz and g_m of 12.46mS while keeping low current consumption of 577µA. IIP_3 is computed to be 91.2mVrms, which corresponds to -10.4dBm referring to 50Ω, matches pretty close to the simulation. However, we cannot analyze IIP_2 with above setup since IM_2 product is not in the passband of the matching network. Volterra series will have to

be used to capture memory effects for an accurate analysis outside of the passband frequency.

Input 1-dB compression point (P1dB) can also be analyzed based on the relationship of: (assuming 3rd order nonlinearity is the dominating odd-order nonlinearity at input strength of IIP3)

$$\boldsymbol{P1dB_i = IIP_3 - 9.6dB}$$

Then, input P1dB is calculated to be -21.5dBm, matches close to simulation of -19.5dBm. The discrepancy can be due to neglecting higher order nonlinearities, therefore underestimating the input P1dB.

4.5 Simulations

The LNA is designed in ADS with the NMOS model card from the commercial foundry 65nm CMOS process. Table IV shows the design component values. Figure 14 shows the LNA testbench in ADS.

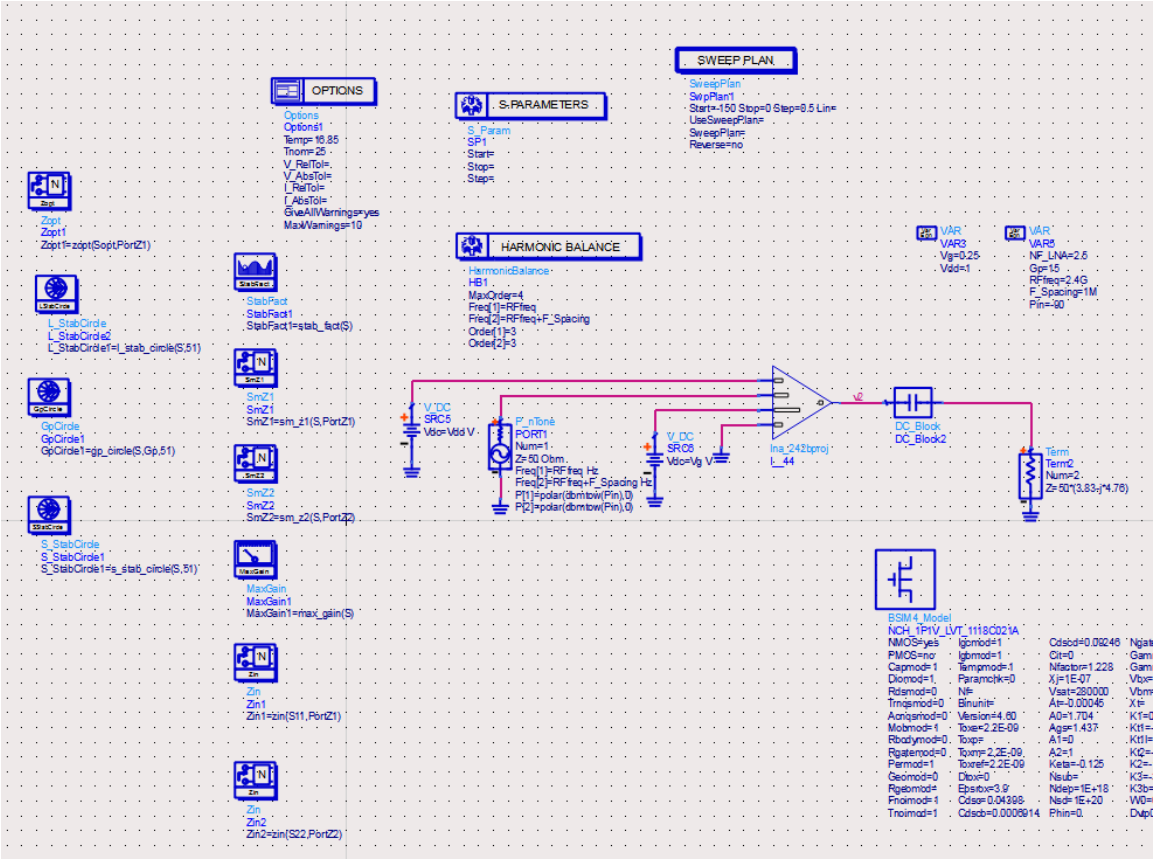

Figure 14: LNA Testbench

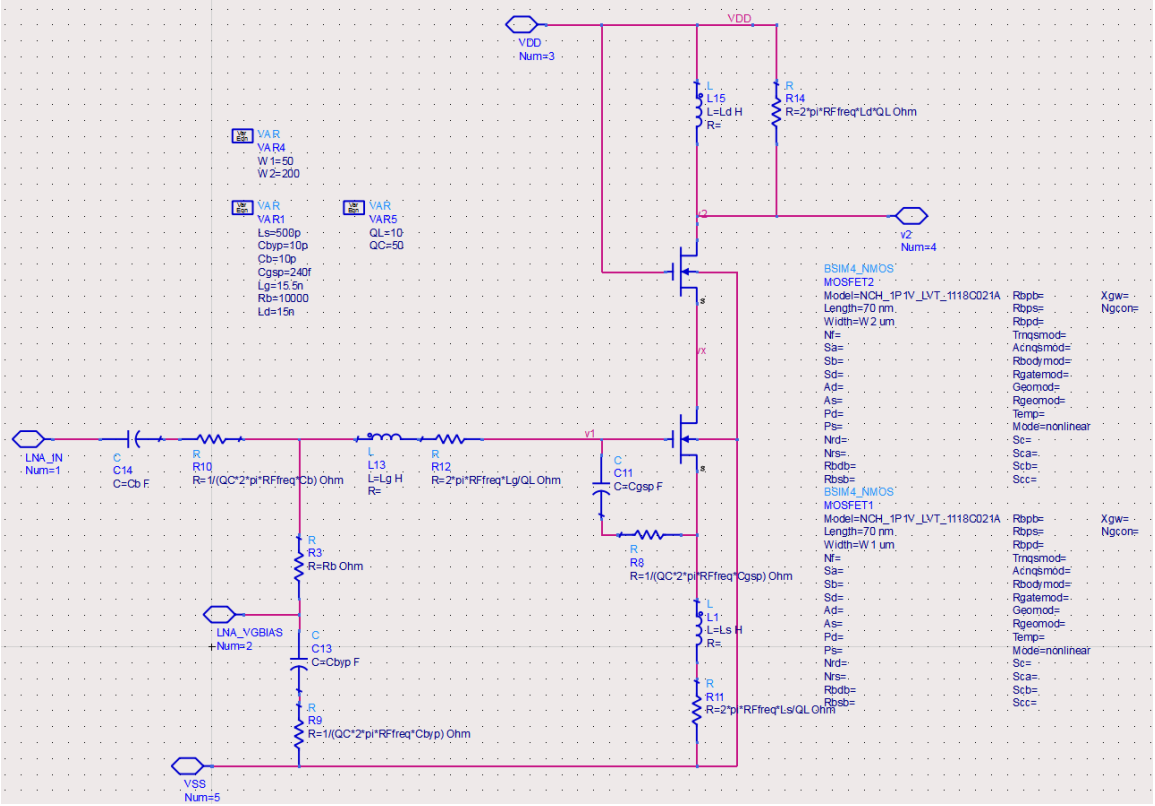

Figure 15: LNA Schematic

TABLE IV
DESIGN COMPONENT VALUES OF LNA

Component	Values	Units
M_1	50/0.07	µm/µm
M_2	200/0.07	µm/µm
L_g	15.5	nH
C_{gsp}	240	fF
L_S	500	pH
L_d	15	nH
C_b	10	pF
C_{byp}	10	pF
R_b	10	kΩ

Power Gain and Load Stability Circles

Load of 192-j238 (Q=1.24) is chosen to be the farthest point away from load instability. Below diagram showing gain of 15dB (spec) once input is matched. Load instability region is outside of the unit circle

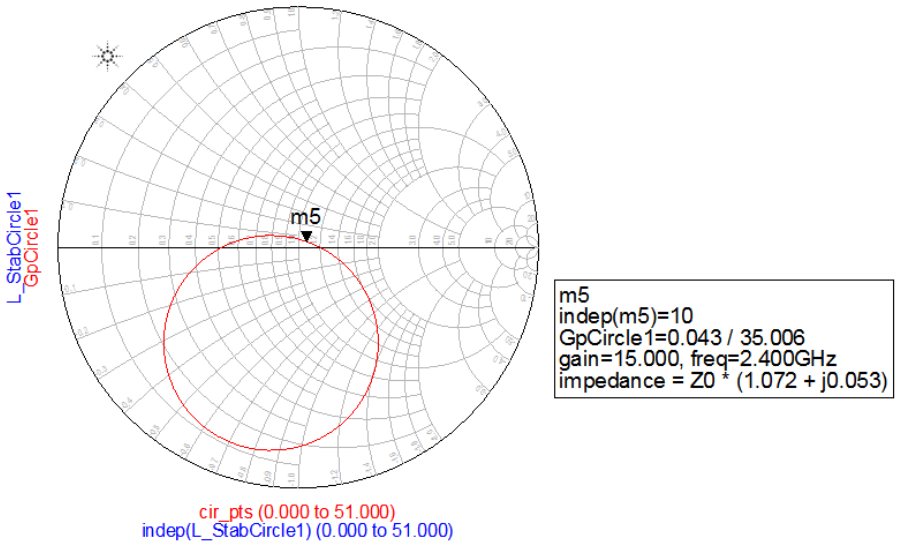

Figure 16: LNA Load Stability and Gain Circle

Source Stability Circle

S11 is inside the stable region and showing matched to source (50Ω). Source instability region is outside of the unit circle

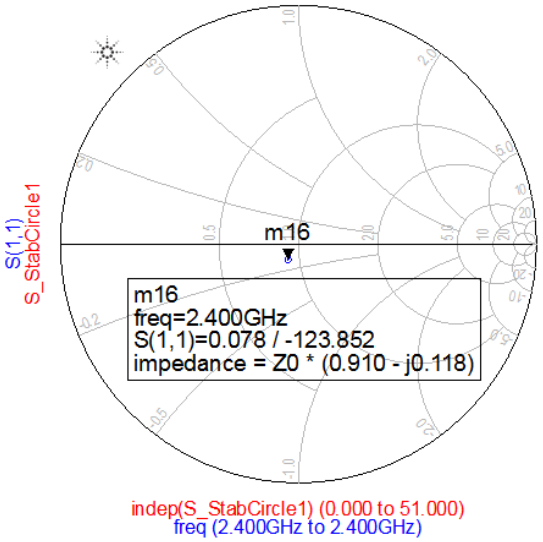

Figure 17: LNA Source Stability Circle

Operating Point

freq	real(Zopt1)	imag(Zopt1)	real(Zin1)	imag(Zin1)	real(Zin2)	imag(Zin2)
2.400 GHz	59.284	-42.293	45.496	-5.895	81.204	364.316

index	Id*1000	Gm*1000	dQg_dVgb	ft/1e9	Gm/Id	Vdsat
1	0.579	12.508	1.023E-13	5.816	21.598	0.045
2	0.579	9.928	2.717E-14	5.914	17.142	0.046

freq	MaxGain1	GMSG	nf(2)	dB(S(2,1))	StabFact1	dB(S(1,1))
2.400 GHz	16.775	27.215	2.358	15.142	5.578	-22.210

Eqn GMSG=10*log(mag(S21)/mag(S12))
Eqn ft=Gm/(2*pi*(dQg_dVgb+240e-15))

Eqn iip3=0.5*(dB(mix(v2,{1,0}))-dB(mix(v2,{2,-1})))-90
Eqn iip2=1*(dB(mix(v2,{1,0}))-dB(mix(v2,{1,-1})))-90

freq	iip3	iip2
<invalid>Hz	-11.755	52.806

Figure 18: LNA operating points and performance

Noise figure (spec. < 2.76dB)

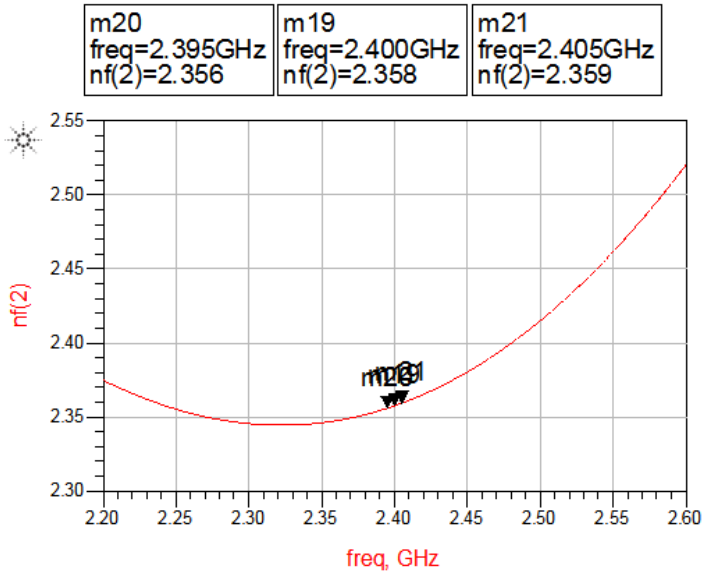

Figure 19: LNA noise figure versus input frequency

Max gain, GMSG, and S21 (spec. S21 = 15dB)

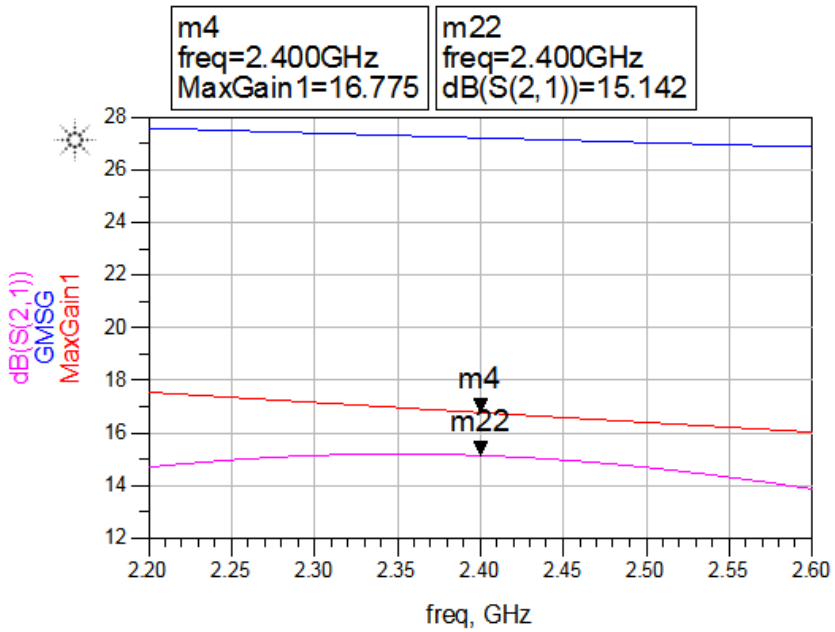

Figure 20: LNA power gain, max. gain, and max. stable gain versus input frequency

S11 (spec. < -20dB)

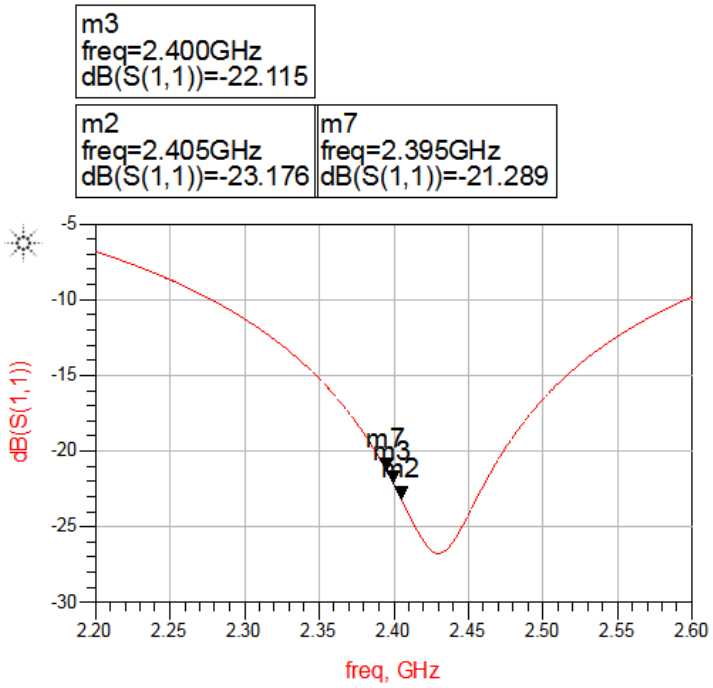

Figure 21: LNA S_{11} versus input frequency

Stability factor (spec. K > 1 across all frequencies)

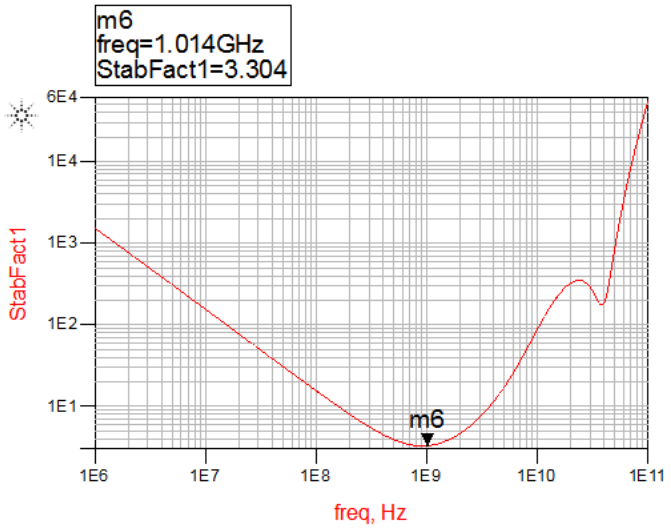

Figure 22: LNA stability factor versus input frequency

Simulated IIP3 of -11.7 dBm, matches with hand analysis (spec. of > -13.5dBm). Two tone simulation at 2.4GHz and 2.401GHz.

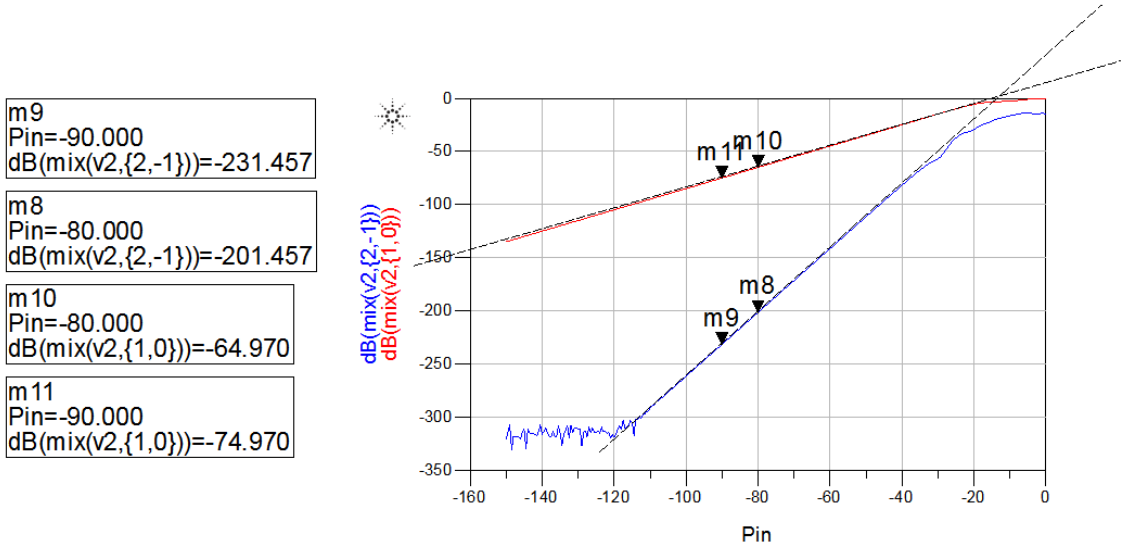

Figure 23: LNA IIP_3 performance

Simulated P1dB,i of -19 dBm (spec. of > -23.1 dBm)

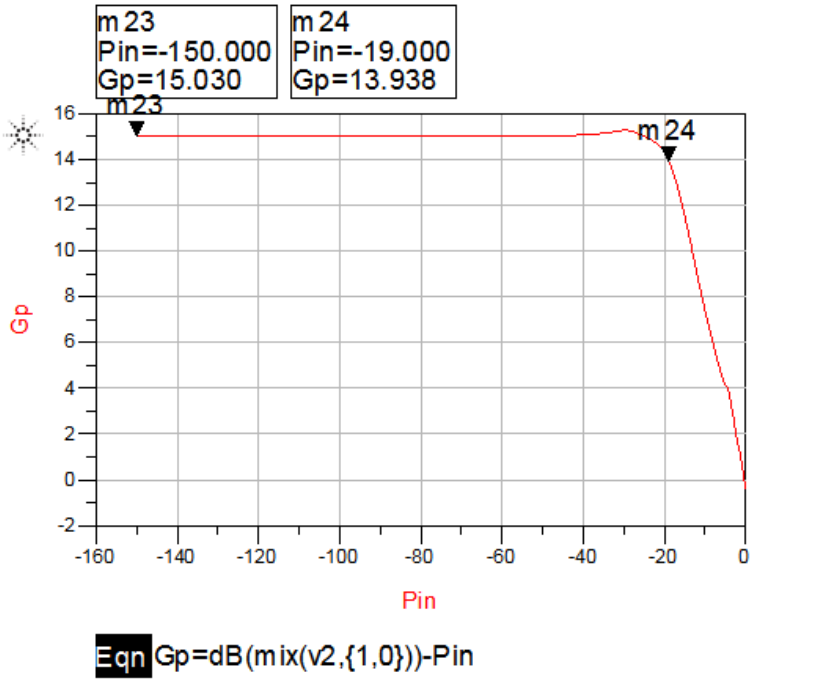

Figure 24: LNA $P_{-1dB,i}$ performance

Simulated IIP2 of +52.8 dBm, (spec. of > +10dBm for the overall system). Two tone simulation at 2.4GHz and 2.401GHz.

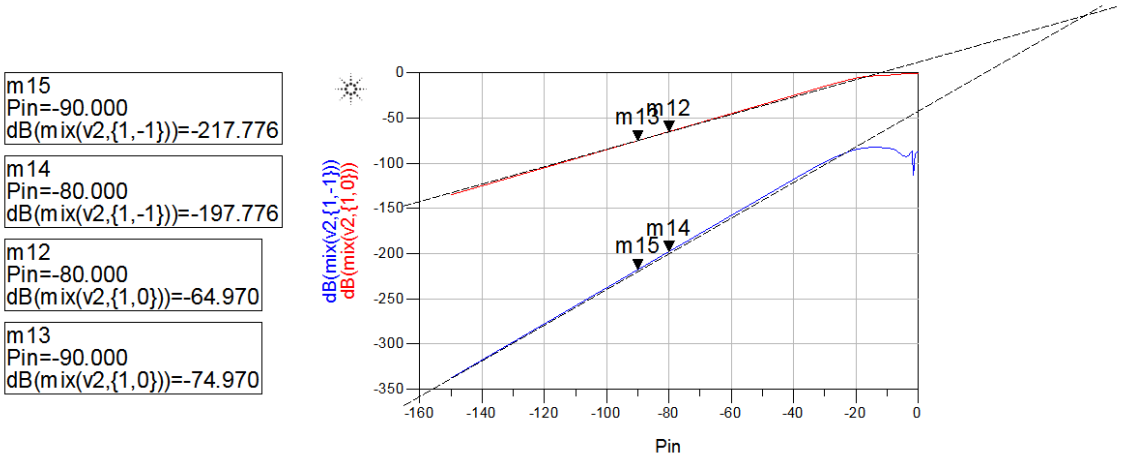

Figure 25: LNA IIP_2 performance

4.6 LNA Performance Summary

TABLE V
LNA DESIGN PERFORMANCE SUMMARY

Parameter	Specification	Simulation Results
V_{DD}	1 V	1 V
I_{DD}	< 1 mA	579 µA
Operating Frequency	2.4GHz ± 5MHz	2.4GHz ± 5MHz
Gain (S_{21})	~ 15 dB	15.142 dB
NF	< 2.76 dB	2.358 dB
P_1dB,i	> -23.1 dBm	-19 dBm
IIP_3	> -13.5 dBm	-11.75 dBm
IIP_2	> +10 dBm (for the overall system)	+52.8 dBm
S_{11}	< -20 dB	< -22.1 dB
K	> 1 (unconditionally stable)	> 1 (unconditionally stable)

The LNA amplifier meets all specifications.

5 Mixer Design

5.1 Circuit Topology

In a typical receiver, it is common to use a single-ended LNA because the antenna and the RF band select filter are also single-ended, therefore the mixer will also be a single-balanced mixer to prevent the need of a balun between LNA to mixer. Ideally, a double balanced mixer topology will prevent LO and RF leakage by creating a virtual ground between the positive and negative LO and RF signals. Typically we are only concerned with LO leakage since it can leak back to the mixer input, LNA input or even the antenna input and cause LO self-mixing in DCR.

Mixer is one of the important building blocks in RF receiver design. The CMOS active mixer and CMOS passive mixer have been widely used in the RF receivers. In this study, a passive mixer is used for the receiver as the best candidate for the given specification requirement.

With the limited power consumption budget we are targeting, it is difficult to design a low power active mixer while meeting the noise and linearity requirement. In a passive mixer as shown in figure 25, LNA output RF current is fed into the passive mixer and the switching pair is performing the current commutating for mixing the RF tone and LO tone. Because the switch pair is just commutating current and the virtual ground of the IF amplifier prevents large swing at that node, we can achieve very high linearity with zero DC current because of the DC blocking capacitor at the switching pair input, also with very low 1/f mixer noise due to zero DC current flowing to the switching pair. The n-path filtering effect due to baseband filter response is itself frequency translated and converted to a high Q bandpass characteristic at the RF port also helps to achieve high IIP3. [3] The disadvantage is that we require some budget of power consumption on the LO buffer to generate a CMOS full swing with sharp transitions for the switching pair input. In a 65nm technology, we can survive with a reasonable power consumption of the LO buffer operating at 2.4GHz with CMOS inverters as limiting amplifiers.

In this study, the LNA acts as the g_m stage as shown in figure 26 and its output directly drives the DC blocking capacitor for saving power consumption and avoids additional linearity degradation from an additional gm stage. Recall that the LNA was designed with gain circle to achieve the required power gain, therefore the large signal mixer input impedance due to the switching action of the LO has to be designed as the desired load that LNA would like to see.

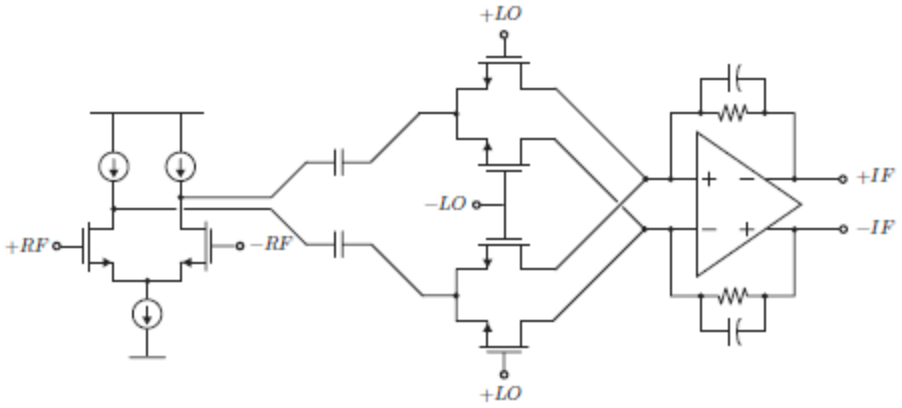

Figure 26: Current commutating passive mixer [3]

5.2 LO Buffer and I/Q Generation

In a typical receiver architecture, there are multiple ways to generate I/Q signals with sharp transitions for the mixer to minimize the noise transfer from input of the mixer switching pair to the IF output. One way is to design a differential quadrature ring oscillator operating at f_o to get CMOS full swing I/Q signals, the drawback is ring oscillator suffers from poor phase noise performance which can degrade the receiver overall noise performance.

The other way to get I/Q signals is to design a quadrature LC oscillator by coupling two LC oscillators with switches to obtain I/Q signals with much better phase noise performance compared to ring oscillator, however additional amplifiers are needed to get CMOS full swing with sharp transitions.

Finally the last common approach is to operate the LO at 2X the frequency and switches one output on the rising edge, and one of the falling edge to achieve quadrature relationship of the two outputs. The amplitude and phase balance of this structure is very good due to its low complexity and operating by digital flip-flops. The drawback of this approach is that the LO at 2X has to be operating at CMOS full swing in order for the flip-flop to function properly, which costs power. Any duty cycle distortion at the input will also result in phase mismatch between I/Q due to the fact that I and Q are generated by rising edge and falling edge respectively. [9] In this study, this approach is used in the design to generate I/Q signals from a LO running at 2X the frequency.

A full swing LO input operating at 4.8GHz is achieved by a CMOS inverter with resistive feedback as a linear amplifier, following by an inverter chain as limiting amplifier. Figure 25 shows the implementation of the CMOS LO buffer and figure 26 shows the typical implementation of the I/Q generation using frequency dividers. [9]

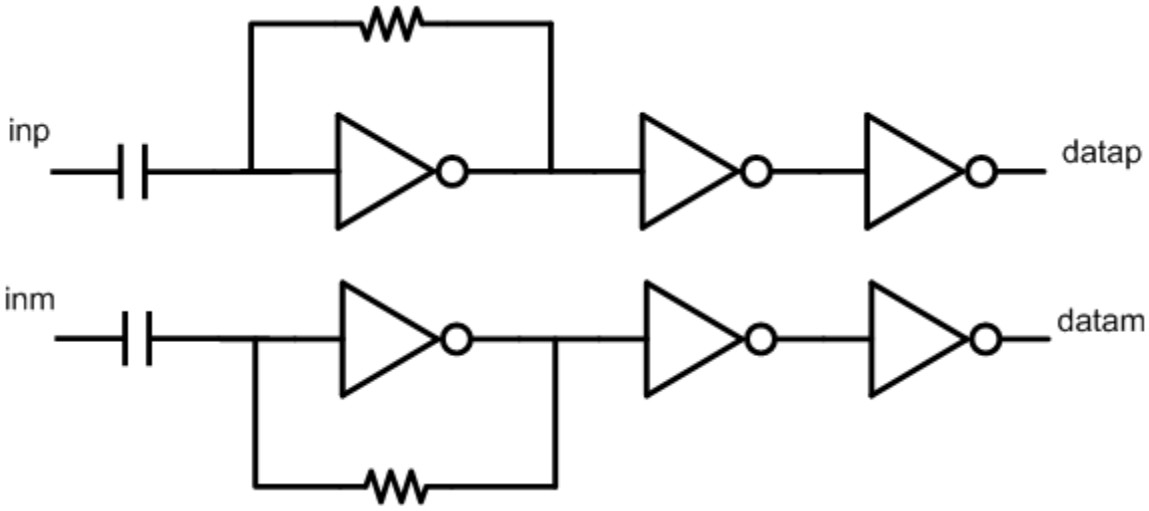

Figure 27: CMOS LO buffer with linear amplifier and limiting amplifier

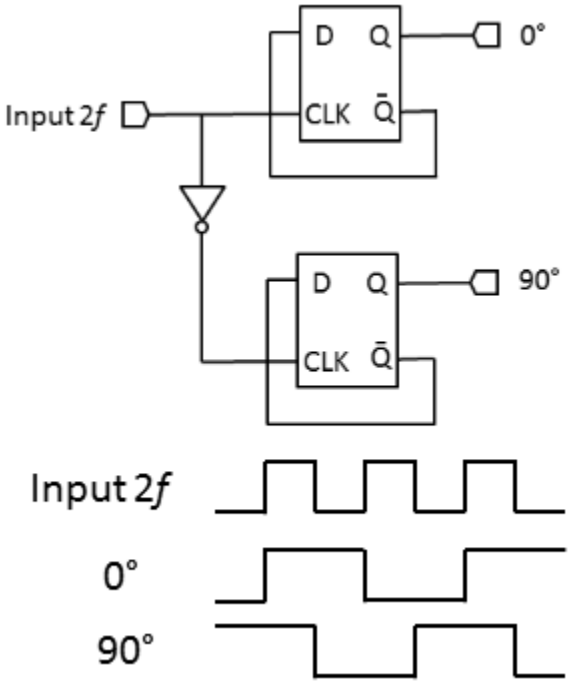

Figure 28: I/Q generation using frequency dividers with input running at double rate [9]

5.3 IF Amplifier Modeling

As shown in figure 26 of the passive mixer architecture, an IF amplifier with resistive feedback is configured as a transimpedance amplifier to convert the IF current to IF

voltage. However, the parasitic capacitor at the mixer input due to the mixer, LNA, and layout parasitics, is inversely proportional to an effective switched-capacitor resistor R_{par} due to the mixer switching action. The input-referred noise of the amplifier is therefore gained up to the IF amplifier output by:

$$v_{n,o} = \left(1 + \frac{R_f}{R_{par}}\right) v_{n,i}$$

, where R_f is the feedback resistance of the IF amplifier.

To minimize the noise amplification (minimize the ratio of R_f/R_{par}), the inductor load at the LNA output must be tuned to resonate with all parasitic capacitors at the mixer input to provide essentially infinite R_{par}, which can be realized in a narrowband receiver similar to matching. [3]

In this study, an ideal fully-differential op-amp is used with open-loop gain of 100V/V and unity gain frequency of 200MHz. The model is written in Verilog-A with non-ideality such as headroom limit. A common mode feedback voltage of 0.3V is defined in the Verilog-A source code. However the parasitic capacitor at the mixer input cannot be tuned out because this architecture does not have an additional gm stage to isolate the LNA and the mixer switching pair. Also the LNA requires a specific load (not purely real in this study) to deliver a certain amount of power based on the gain circle design.

5.4 Mixer Noise Analysis

To analysis the noise of the passive mixer in this study, we will take the noise contribution from the switching pair, as well as the op-amp amplification noise. The noise contribution of the g_m stage was already captured in the LNA noise figure analysis.

The switch is basically operating in triode region when it is ON and square law equation is sufficient to model the conductance. Additional DC bias is provided to the gate and source of the switch to properly shift the levels of the LO input for an effectively 50% duty cycle as shown in figure 29. The source DC bias (V_B) of the switch can be biased directly by the common mode feedback of the IF amplifier once the gate is properly biased to have zero DC current. S represents the ramp rate of the LO transition which is given by A_{LO}/t_{rise}.

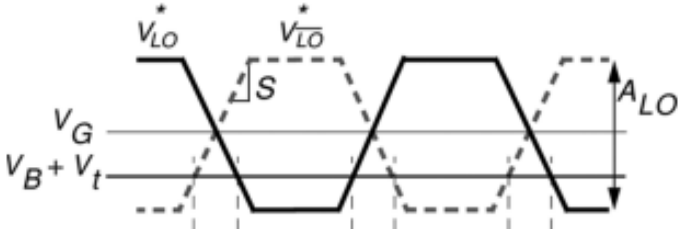

Figure 29: LO switching waveforms with DC bias [5]

To begin the analysis, assume the LO input port has an input referred noise that is white:

$$S_{n,LO}(f) = 4kT(2R_n)\overline{G^2}\left(1+\frac{R_F}{R_{par}}\right)^2$$

, where the factor of 2 comes from the fact that we have two switches (single-balanced) and G is the noise transfer function from the LO port to the switch output.

Define V_{LO} as the max. amplitude of the LO swing (V_{DD} in CMOS output), we can express the conductance of both LO+ and LO- switch respectively as:

$$g_{LO+} = \frac{k'W}{L}(V_G + V_{LO} - V_B - V_{TH})$$

$$g_{LO-} = \frac{k'W}{L}(V_G - V_{LO} - V_B - V_{TH})$$

The noise transfer function G can be obtained by averaging the cyclostationary noise from the switching pair of the mixer over a small bandwidth. [5] First, we will find the cyclostationary noise from the switching pair at the differential output:

$$S_{i,n,diff} = \frac{4kTR_n(g_{LO+}^2 + g_{LO-}^2)}{g_o^2}\left(1+\frac{R_F}{R_{par}}\right)^2 = \frac{4kTR_n(g_{LO+}^2 + g_{LO-}^2)}{\frac{k'W}{L}(V_G - V_B - V_{TH})}\left(1+\frac{R_F}{R_{par}}\right)^2$$
$$= 4kTR_n\left(2+\frac{2V_{LO}^2}{(V_G - V_B - V_{TH})^2}\right)\left(1+\frac{R_F}{R_{par}}\right)^2$$

Next, we can observe the cyclostationary noise over a small bandwidth to obtain the stationary noise at the output due to the LO input referred noise:

$$S_{n,LO}(f) = \overline{S_{i,n,diff}(f,t)}$$
$$= \frac{1}{T_{LO}}\int_{-\frac{V_G - V_B - V_{TH}}{S}}^{\frac{V_G - V_B - V_{TH}}{S}} 4kTR_n\left(2+\frac{2V_{LO}^2}{(V_G - V_B - V_{TH})^2}\right)\left(1+\frac{R_F}{R_{par}}\right)^2 dV_{LO}$$
$$\cong \frac{8kTR_n(V_G - V_B - V_{TH})}{ST_{LO}}\left(1+\frac{R_F}{R_{par}}\right)^2$$

With the assumption that the op-amp is ideal, the only noise contribution is from the input-referred noise of the LO being amplified by the op-amp. From this equation, we would like to dc bias the switch pair to minimize the LO input-referred noise transferring to the output.

5.4 Mixer Simulations

In this section, the mixer is simulated in spectreRF with the testbench consists of LO buffers (operating at 1X and 2X of LO), I/Q generation, and I/Q mixers. Ideal baluns at the output are used for probing the differential IF output. A load of 10kohm is used at the IF output to emulate the input impedance of the VGA. The input RF port impedance is set to be the output impedance of the LNA to maintain the block performance after they are connected.

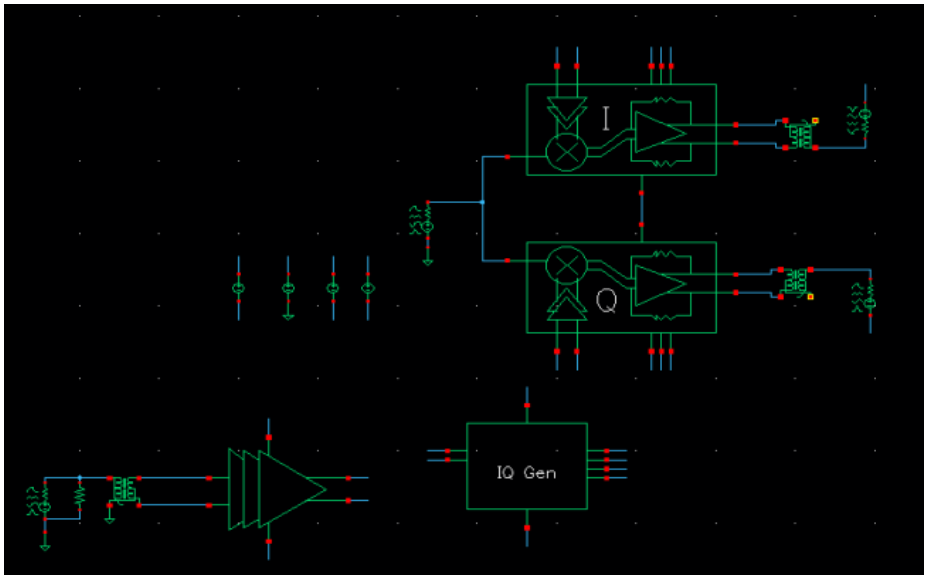

Figure 30: Mixer testbench in Cadence

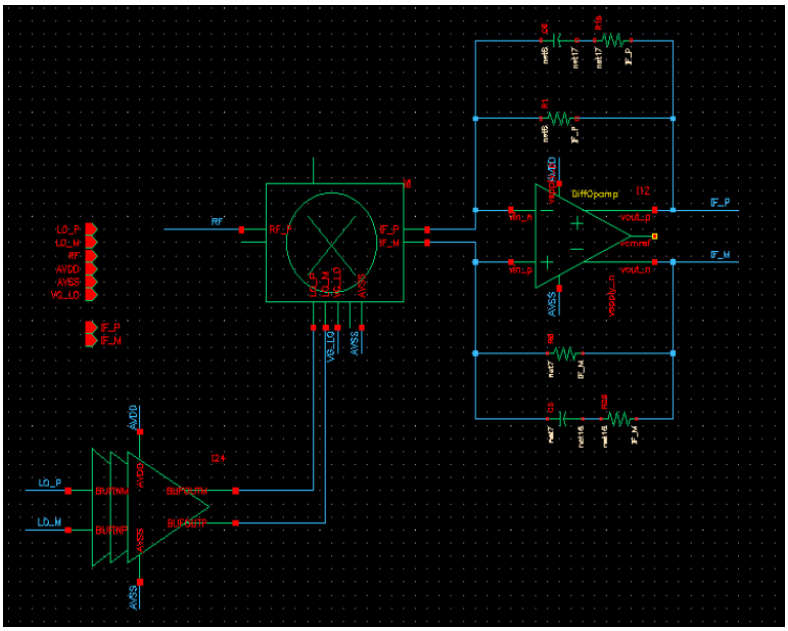

Figure 31: I/Q mixer core with ideal op-amp in Verilog-A

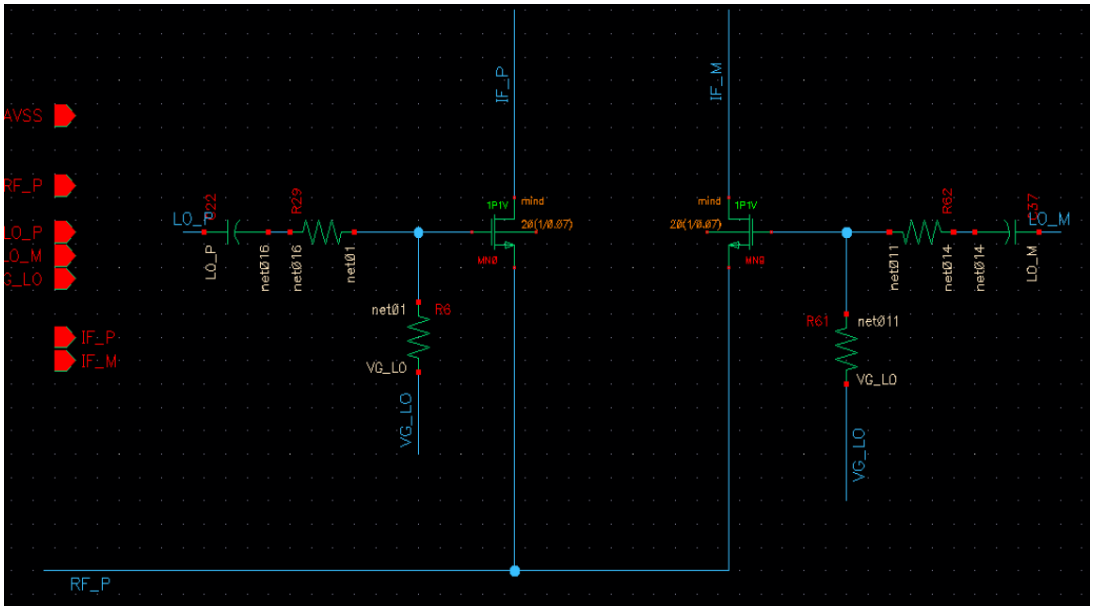

Figure 32: passive mixer core with dc gate bias

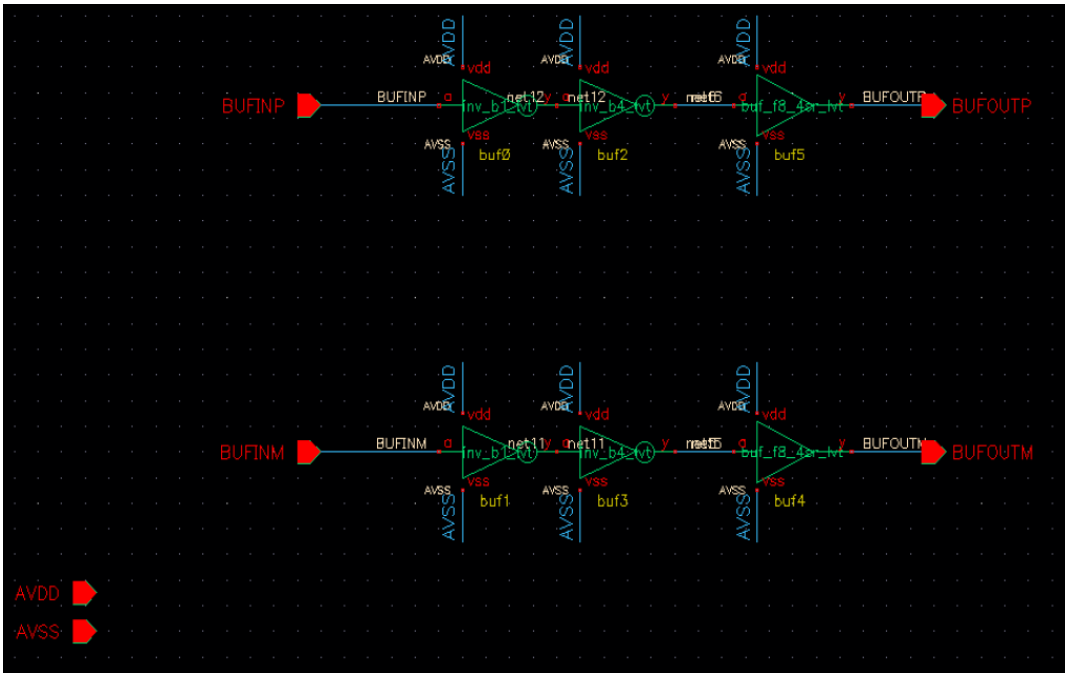

Figure 33: LO buffer operating at 2.4GHz after the I/Q generation

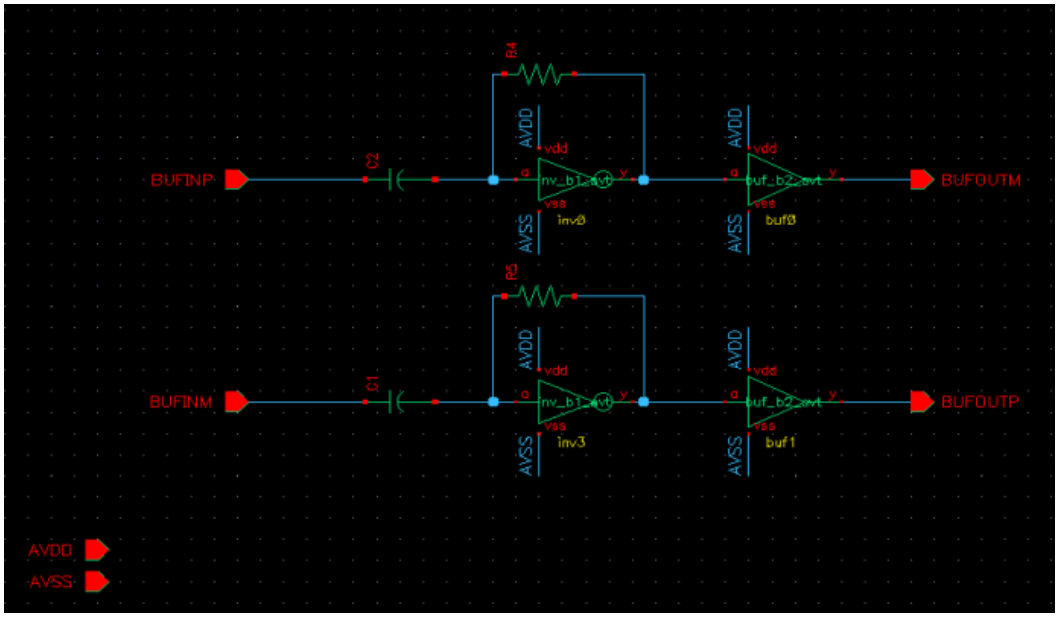

Figure 34: LO buffer operating at 4.8GHz for amplifying input LO to square wave

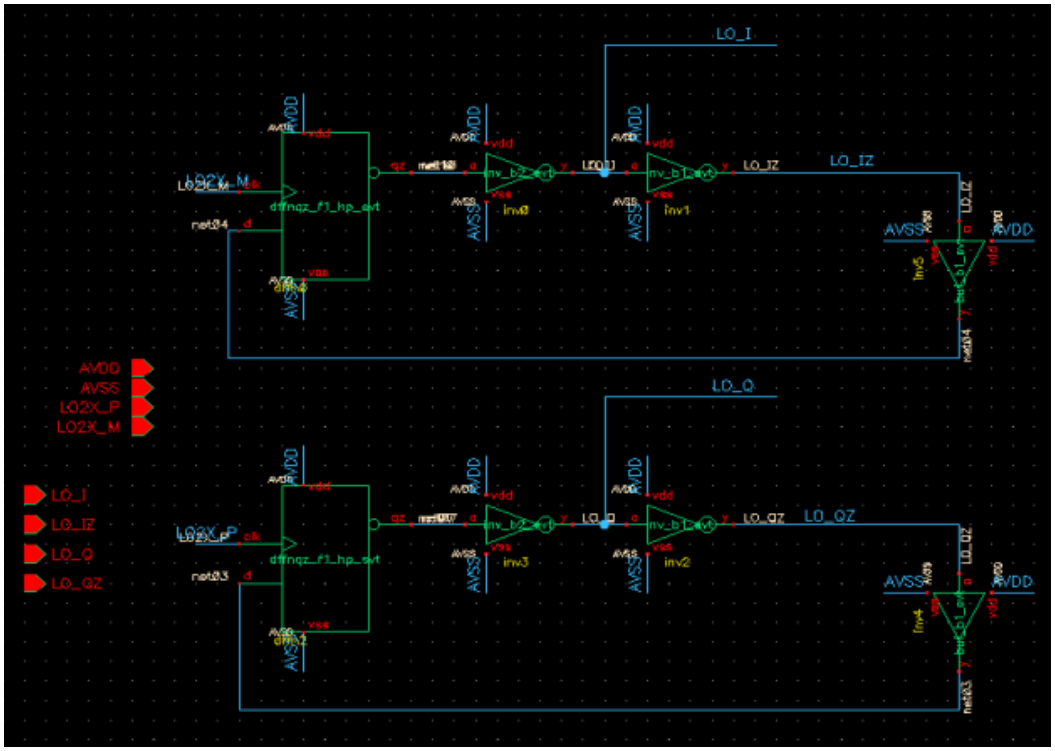

Figure 35: I/Q generation using static CMOS logic frequency dividers in 65nm

Figure 36 shows the transient waveform of LO running at 4.8GHz and the I/Q signal at 2.4GHz from PSS. The I/Q rise/fall time to the mixer before the dc bias of the switch pair is approximately 12ps. The LO port output power is set to -15dBm referring to 200 ohm.

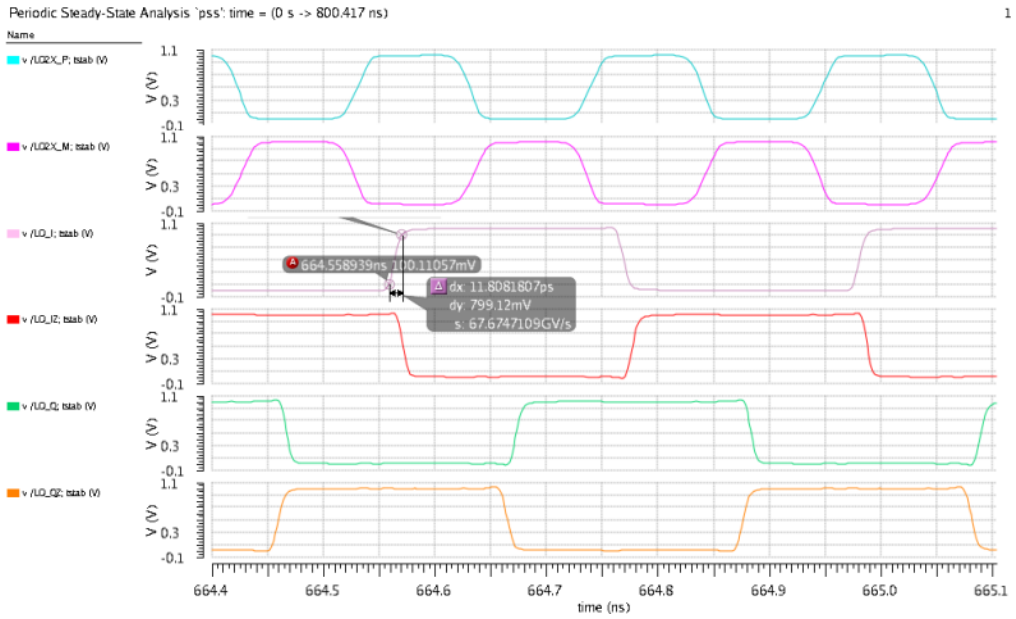

Figure 36: Simulated LO and I/Q transient waveform

Figure 37 shows the transient waveform probed at the mixer's Vgs after the dc bias. As shown in the figure, the dc point of Vgs is biased at approximately Vt (0.35V) in order to optimize the LO switching, with rise time of 20ps for fast switching. The LO gate is biased at 0.65V while the drain of the switched is biased at 0.3V by the common mode feedback of the IF amplifier, therefore a Vgs bias of 0.35V across the switch.

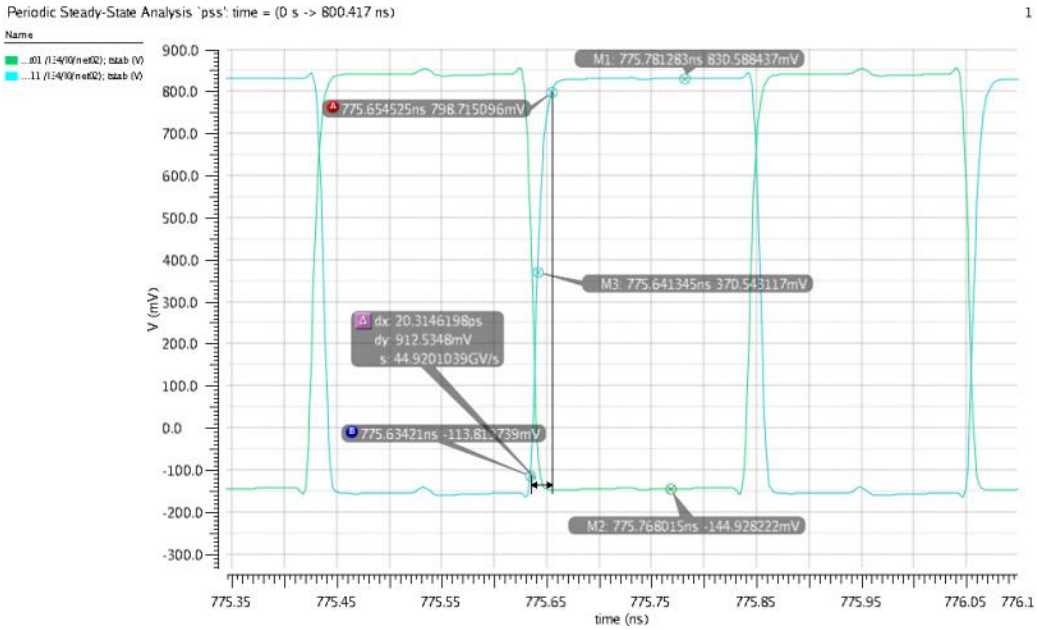

Figure 37: Simulated mixer input transient waveform

PAC simulation is performed to simulate the voltage conversion gain of the mixer with IF from 0Hz to 5MHz. In this setup, LO is the only large signal and RF is the small signal. Simulated voltage conversion gain is 5dB.

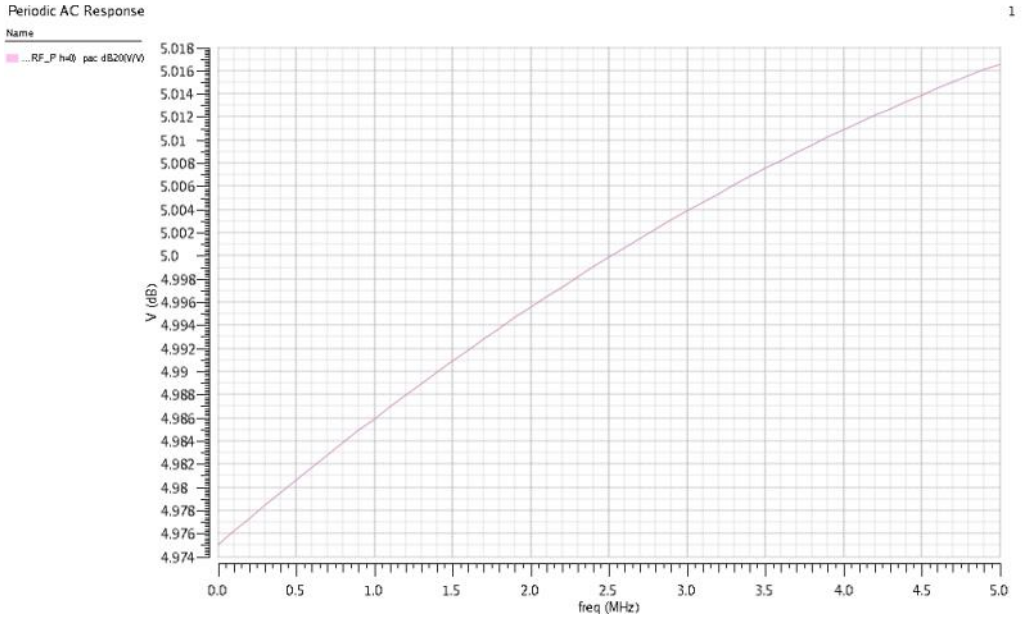

Figure 38: Simulated mixer voltage conversion gain

Pnoise simulation is performed to simulate the double-sideband noise figure of the mixer with IF from 1kHz to 5MHz. The simulated integrated DSB noise figure from 1kHz to 5MHz is 9dB.

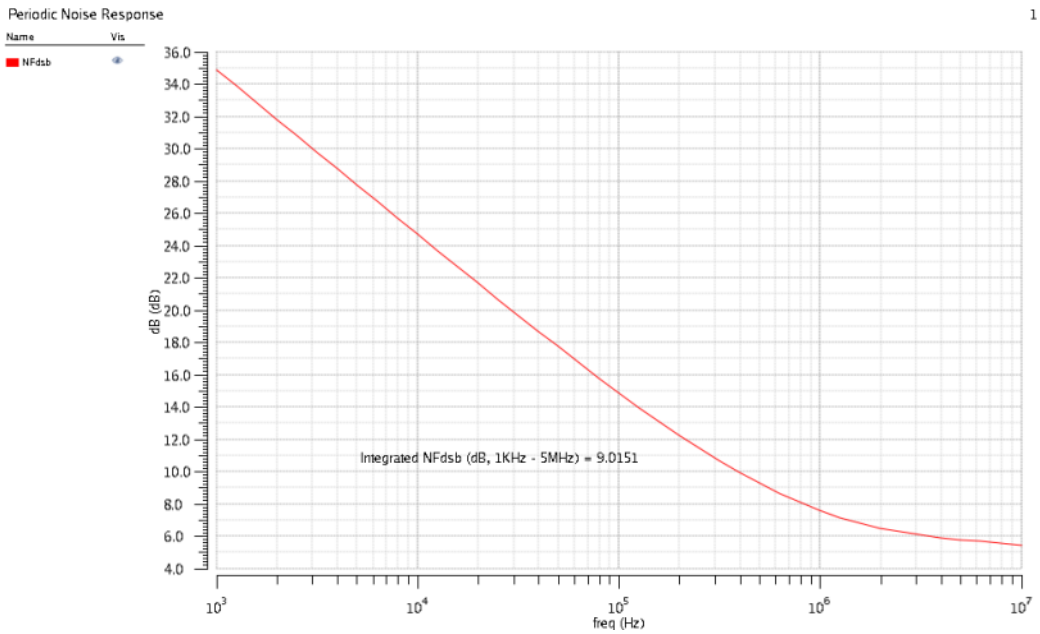

Figure 39: Simulated mixer double-sideband noise figure

PSP is performed to to simulate the large signal s-parameter of the mixer. The input impedance of one mixer at RF is found to be 87 – j*81 ohm. With both I/Q mixer, the LNA is expected to see approximately 44 – j*40 ohm.

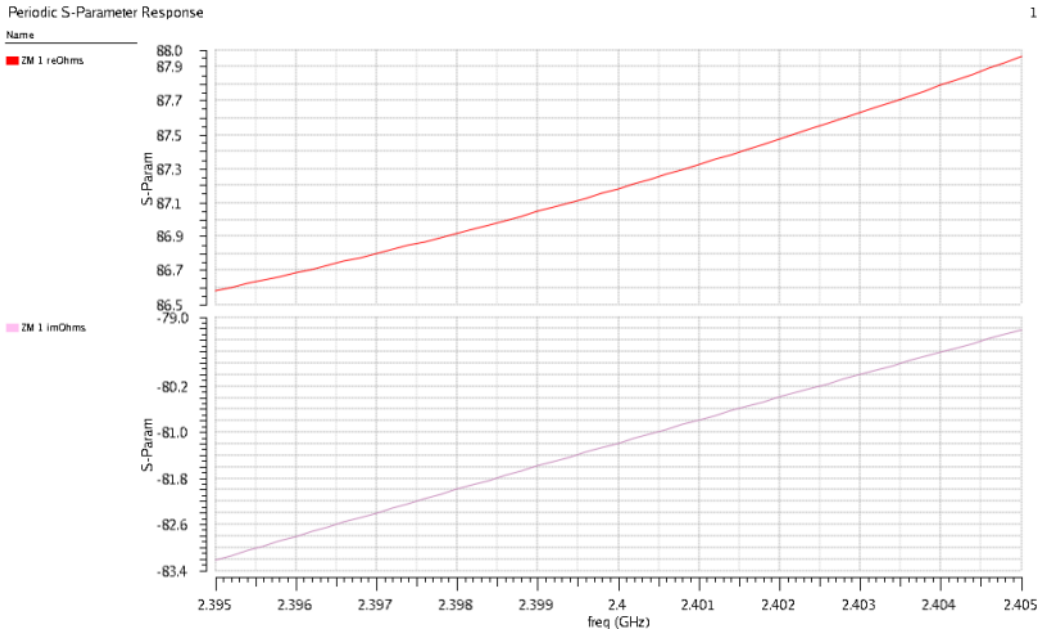

Figure 40: Simulated large signal mixer input impedance

QPSS along with QPAC is used to perform the linearity simulation. The simulation setup can be referred to [11]. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV). The simulated IIP3 is +13 dBm which is much higher than the required specification. It can be seen that the conversion gain is 5dB from the fundamental curve. (input of -90dBm is equivalent to -100dBV, and output gives -95dBV). The linearity at the Q channel output is also analyzed and it gives the same result.

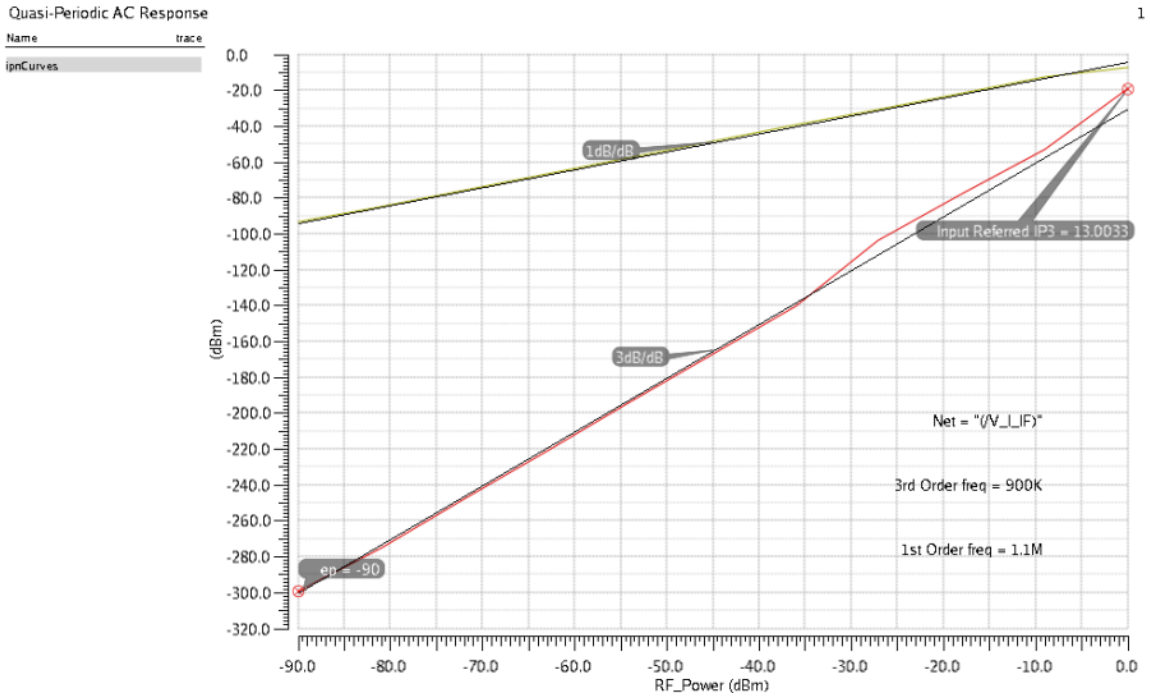

Figure 41: Simulated mixer IIP3

Similarly, we can plot IM2 and find IIP2. Because the load does not have any mismatch and the duty cycle is 50%, we observe a very high IIP2 of 170dBm. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV).

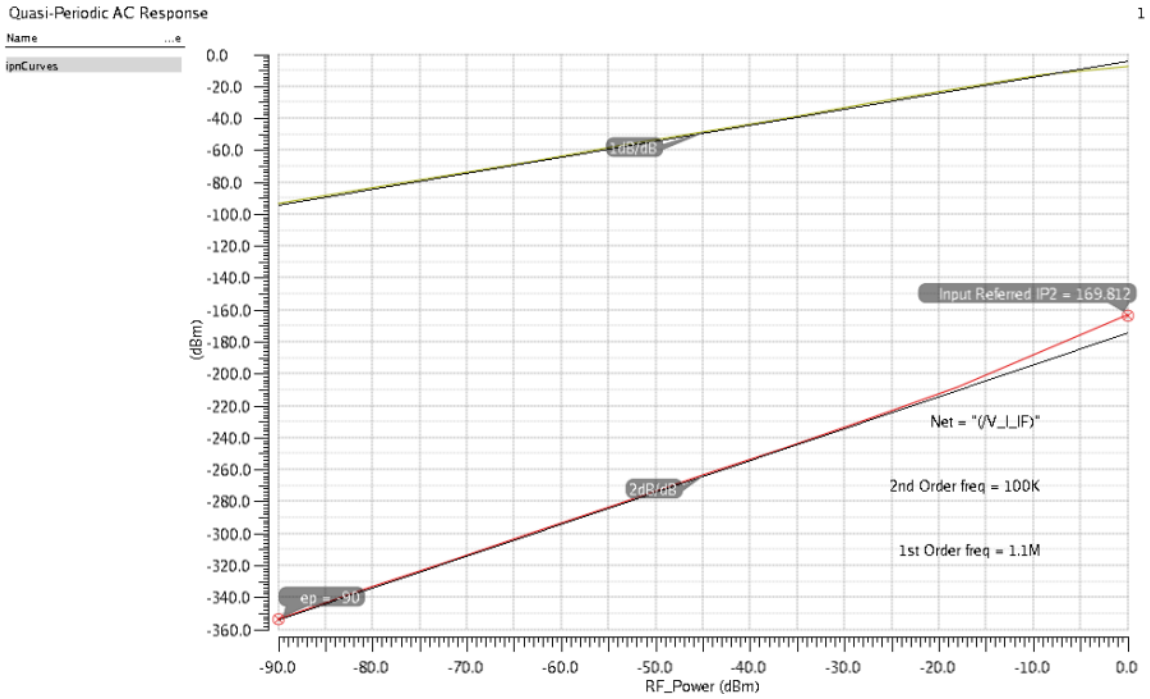

Figure 42: Simulated mixer IIP2

5.5 Mixer Performance Summary

TABLE VI
MIXER DESIGN PERFORMANCE SUMMARY

Parameter	Specification	Simulated
V_{DD}	1 V	1 V
$I_{DD,AVG}$	< 1 mA (including LO buffer, IQ generator)	890 µA
LO port power consumption	< 200 µA	64 uA (@-15dBm,200Ω) Multiplied by 2 to consider differential LO
$I_{tot,avg}$	< 1.2 mA	954 µA
Load	10 kohm	10 kohm
RF Input Frequency	2.4GHz ± 5MHz	2.4GHz ± 5MHz
LO Input Frequency	4.8 GHz	4.8 GHz
I/Q mixer LO	2.4 GHz	2.4 GHz
IF Output Frequency	0 Hz – 5 MHz	0 Hz – 5 MHz
Voltage Conversion Gain	5 dB	5 dB
NF_{DSB}	< 10 dB	9 dB
IIP3	> 1.51 dBm	13.1 dBm
IIP2	> +10 dBm (for the overall system)	170 dBm (no mismatch)

LO gate bias = 0.65V
LO drain bias = IF amplifier common mode feedback = 0.3V
Ideal op-amp with gain = 100 and unity-gain frequency of 200MHz

The mixer meets all specifications.

5.6 LNA+Mixer Simulations

The LNA and mixers are combined to ensure the matching between the interfaces is designed correctly, with the expected performance based on the budget hand analysis. Figure 42 shows the testbench of LNA with mixer. A DC blocking capacitor of 250fF is added between the LNA and mixer for AC coupling, as well as adjusting the impedance such that LNA sees the desired load based on its design in gain circle.

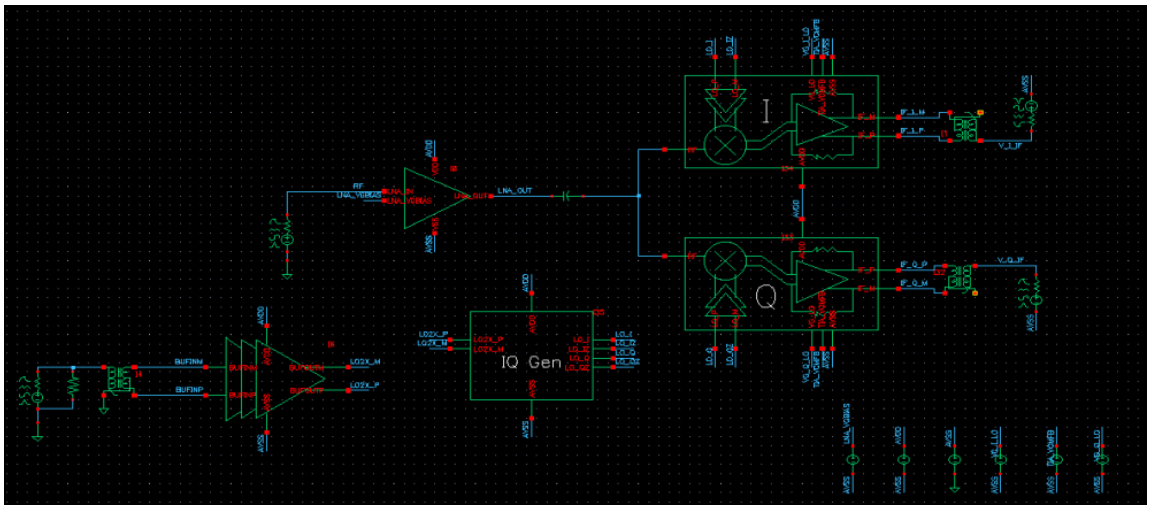

Figure 43: Simulation testbench of LNA with mixer

Similar to the mixer simulation, PAC simulation is performed to simulate the voltage conversion gain of the LNA+mixer with IF from 0Hz to 5MHz. In this setup, LO is the only large signal and RF is the small signal. Simulated voltage conversion gain is 20dB, agrees with adding both the LNA gain of 15dB and mixer gain of 5 dB.

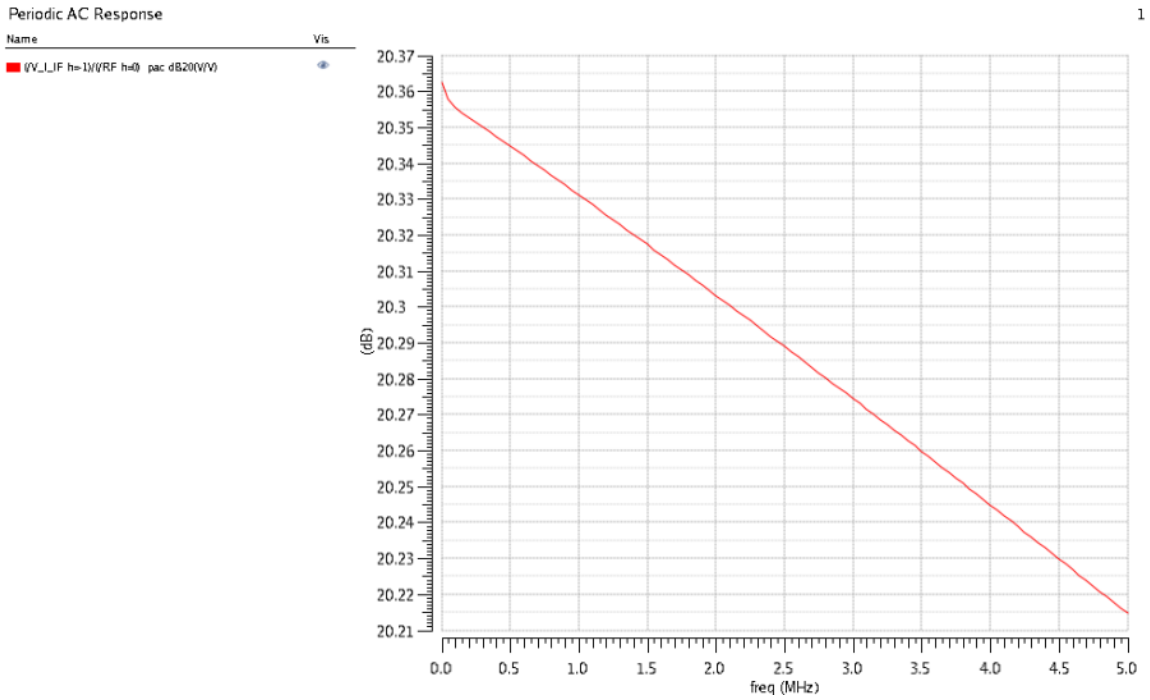

Figure 44: Simulated voltage conversion gain of LNA cascading mixer

Pnoise simulation is also performed to simulate the double-sideband noise figure of the mixer with IF from 1kHz to 5MHz. From the noise equation with the simulation data, we expect the noise figure at high frequency region where flicker noise is negligible to be:

$$\mathrm{NF_{LNA+MIXER}} = 10 * \log\left(10^{\frac{NF_{LNA}}{10}} + \frac{10^{\frac{NF_{MIXER}}{10}} - 1}{G_{LNA}}\right) = 2.88\ dB$$

The simulated integrated DSB noise figure cascading LNA and mixer from 1kHz to 5MHz is 3.22dB.

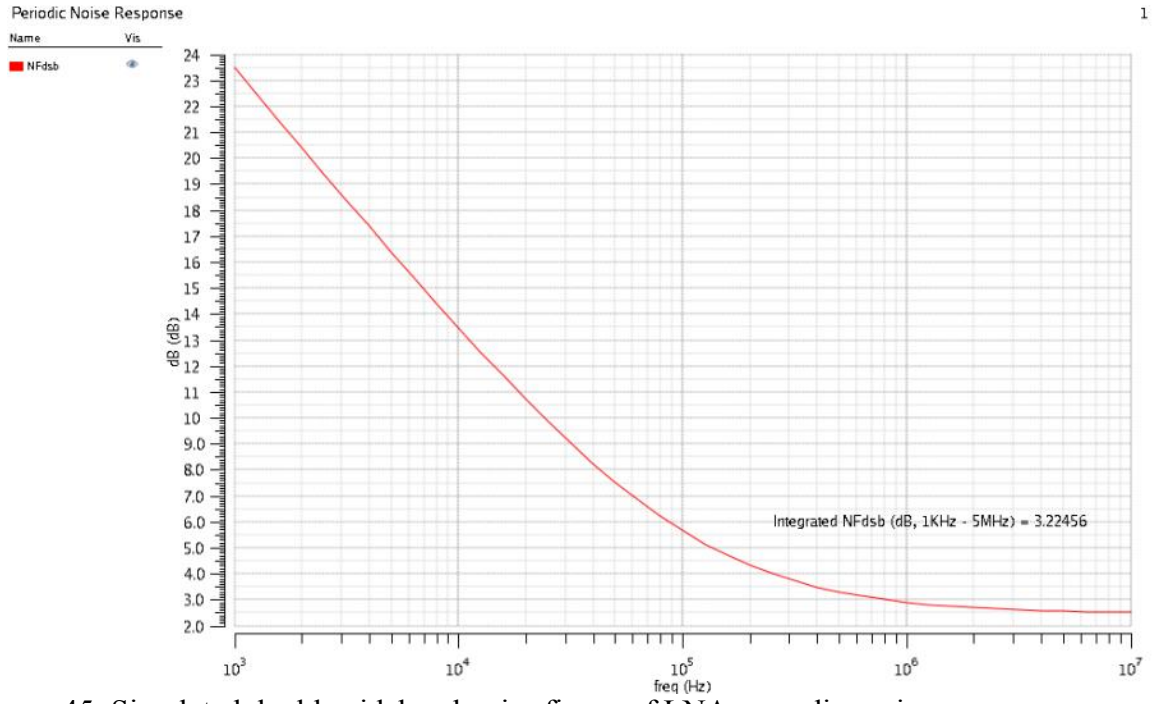

Figure 45: Simulated double-sideband noise figure of LNA cascading mixer

PSP is also performed to simulate the large signal s-parameter of LNA+mixer. Simulation in figure 46 and figure 47 shows S11 is well-matched to 50Ω with about 200MHz of bandwidth for S11 < -20 dB.

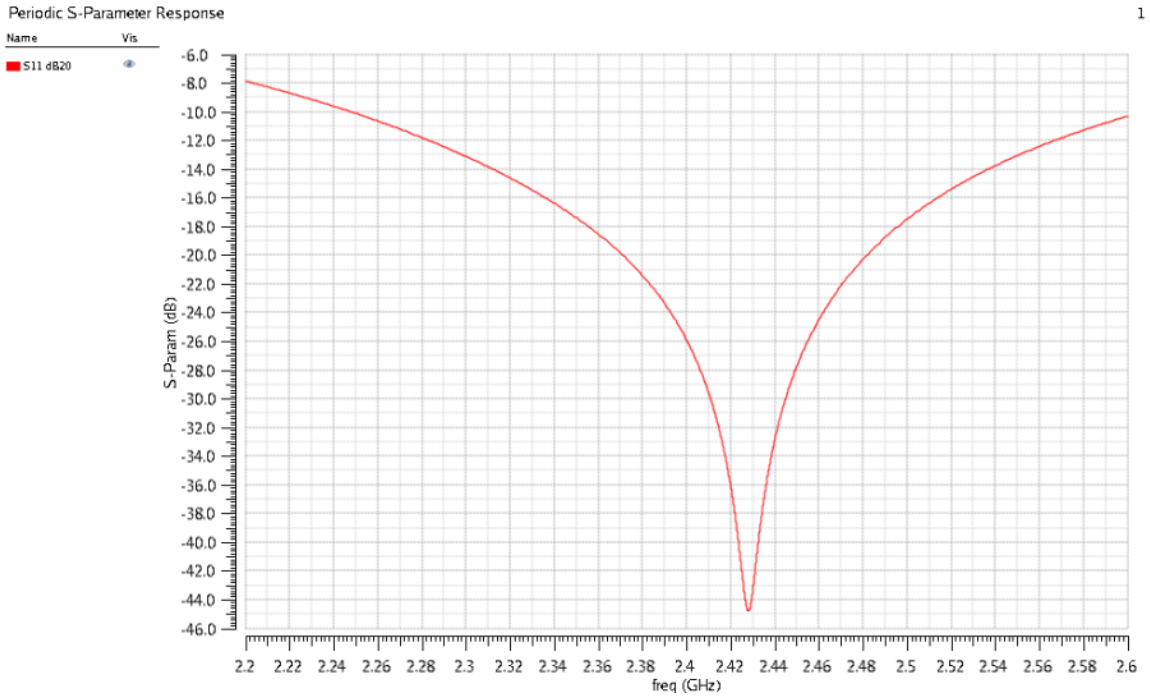

Figure 46: Simulated large signal S11 of LNA cascading mixer

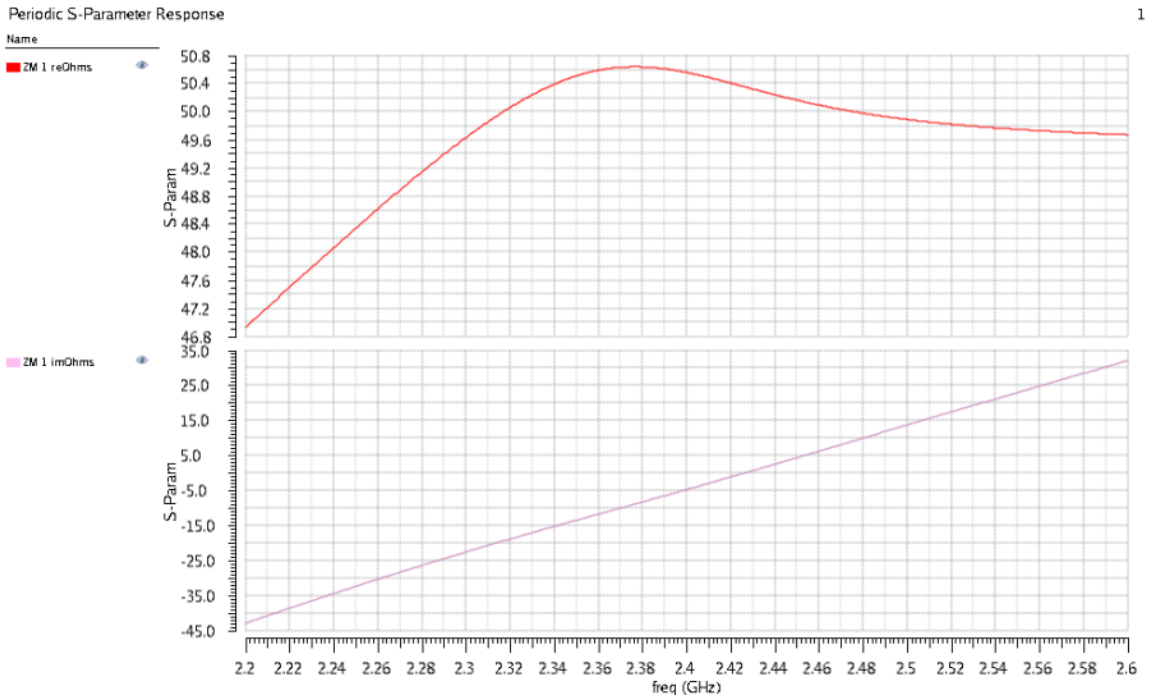

Figure 47: Simulated large signal input impedance of LNA cascading mixer

QPSS along with QPAC is again used to perform the linearity simulation. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV). Since the mixer has a very high IIP3, it is expected the overall IIP3 of LNA cascading with mixer to be close to the LNA linearity. The simulated IIP3 is -15.245 dBm which is higher than the required specification. It can be seen that the voltage gain is 20dB for LNA+mixer from the fundamental curve. (input of -90dBm is equivalent to -100dBV, and output gives -80dBV). The linearity at the Q channel output is also analyzed and it gives the same result.

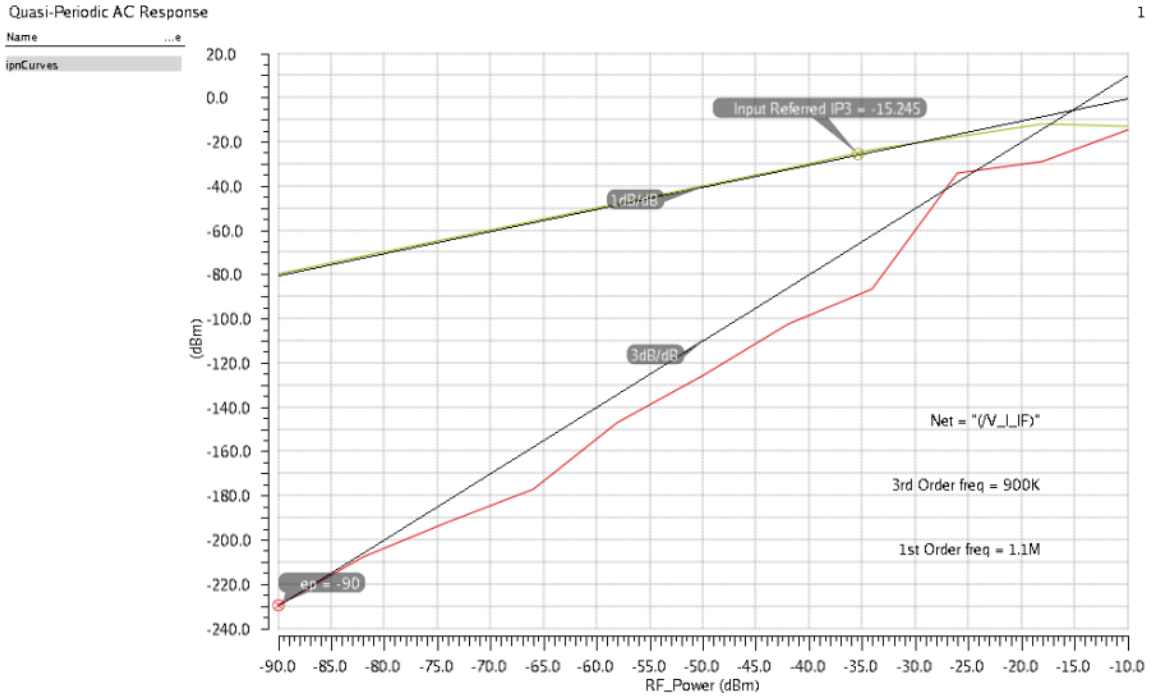

Figure 48: Simulated IIP3 of LNA cascading mixer

Similarly, we can plot IM2 and find IIP2. IIP2 will be limited by the LNA because the IIP2 of mixer is closed to ideal due to no mismatch. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV).

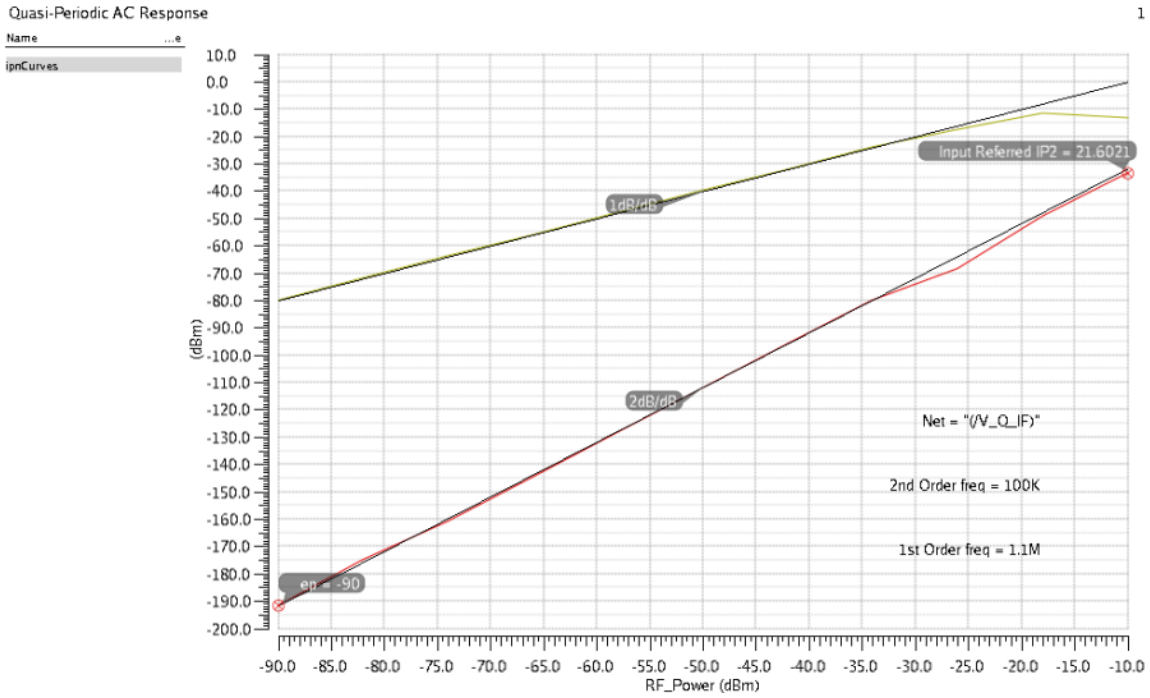

Figure 49: Simulated IIP2 of LNA cascading mixer

Input P1dB of LNA cascading mixer is also simulated in PSS. From the budget analysis, the required input P1dB is -27dBm at the LNA input because the required input P1dB at VGA input is -7dBm. Figure 50 shows that it is still within specification.

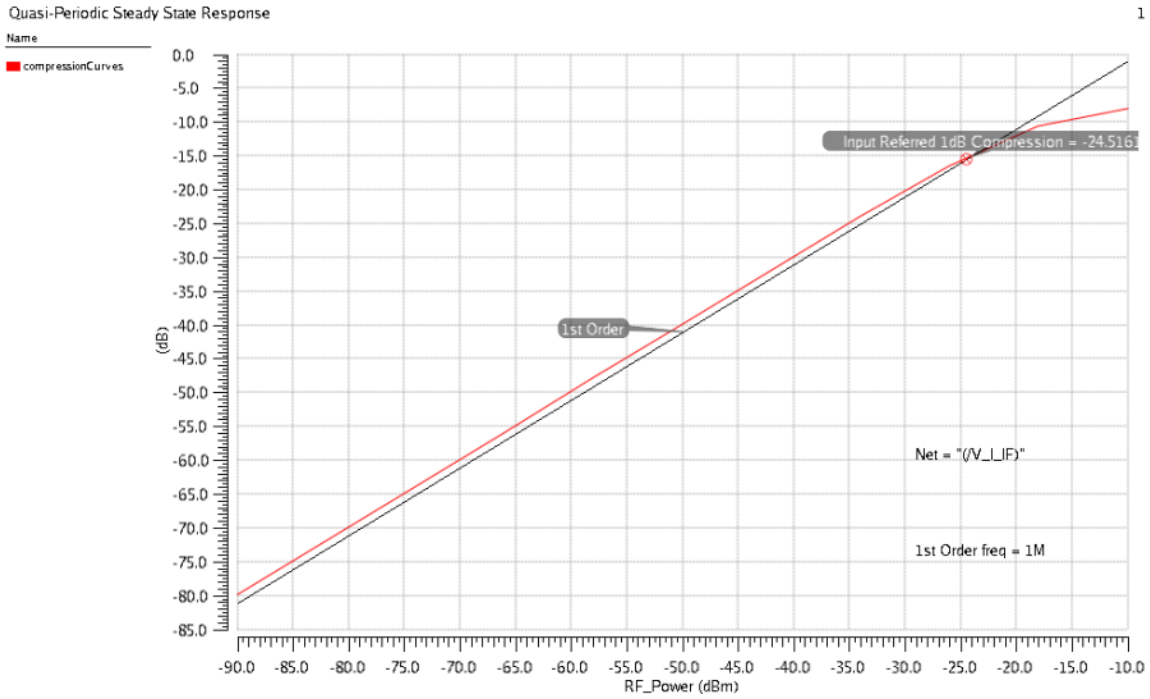

Figure 50: Simulated input P1dB of LNA cascading mixer

TABLE VII
LNA+MIXER DESIGN PERFORMANCE SUMMARY

Parameter	Specification	Simulated
V_{DD}	1 V	1 V
$I_{DD,AVG}$	< 1.8 mA (including LO buffer, IQ generator)	1.47 mA
LO port power consumption	< 200 µA	64 uA (@-15dBm,200Ω) Multiplied by 2 to consider differential LO
$I_{tot,avg}$	< 2 mA	1.53 mA
Load	10 kohm	10 kohm
RF Input Frequency	2.4GHz ± 5MHz	2.4GHz ± 5MHz
LO Input Frequency	4.8 GHz	4.8 GHz
I/Q mixer LO	2.4 GHz	2.4 GHz
IF Output Frequency	0 Hz – 5 MHz	0 Hz – 5 MHz
Voltage Gain	20 dB	20 dB
NF_{DSB}	< 3.36 dB	3.22 dB
P1dB,i	> -27 dBm	-24.5 dBm
IIP3	> -16.5 dBm	-15.245 dBm
IIP2	> +10 dBm (for the overall system)	21.6 dBm

- LO gate bias = 0.65V
- LO drain bias = IF amplifier common mode feedback = 0.3V
- Ideal op-amp with gain = 100 and unity-gain frequency of 200MHz
- NF and IIP3 specifications are calculated based on the cascade equations with only LNA and mixer in the chain.

6 VGA Modeling

6.1 VGA Verilog-A Model

A Verilog-A behavioral model is used for the VGA with IIP3 and noise figure accurately modeled. Below is the modified source code from [7]. Modifications are done for correctly referring the impedance to convert the noise contribution and linearity from dBm to voltage. In this study, the noise contribution of VGA should refer to the LNA input which is 50 ohm, while the linearity in dBm should refer to the input impedance which is 10kohm. The gain programmability can be done by modifying the gain variable in the Verilog-A block.

```
 //  VerilogA baseband behavioral model of a power amplifier.
//  Copyright (c) 2000
//  by Cadence Design Systems, Inc.  All rights reserved.

// 1/5/99

/* PARAMETER DEFINITIONS:
======================
gain      = voltage gain in dB.
IP3       = input referenced IP3(dBm)
nf        = noise figure [dB]
rin       = input resistance
rout      = output resistance
======================
*/

`include "constants.h"
`include "discipline.h"

`define PI 3.14159265358979323846264433
module LNA_PB(in, out);
inout in;
electrical in;
inout out;
electrical out;

parameter real gain = 60 from [0:inf);
parameter real ip3 = -20.4;
parameter real rin = 10k from (0:inf);
parameter real rout = 10k from (0:inf);
parameter real nf = 20 from [0:inf];

real a;
real b;
real ip;
real rho;
real rhooutmax;
real rhoinmax;
real rhoout;
```

```
real tmp;
real cp;
real noise_current;
real rnf;

analog begin

// The initial block converts the input parameters from engineering
// units to implementation units.
   @(initial_step) begin
     a = sqrt(pow(10,gain/10)*rout/rin);
     ip = sqrt(pow(10,ip3/10)*2*rin*0.001);
     rnf = pow(10,nf/10);
     b = a/(ip*ip)*4/3;
     rhoinmax = sqrt(a/(3*b));
     rhooutmax = (2*a/3)*rhoinmax;
     noise_current = sqrt(4*(rnf-1)*1.380620e-23*$temperature/50);

   end

  rho = V(in);

// Apply the third order non-linearity. Clamp the
// output for extreme inputs.
  if (abs(rho) < rhoinmax ) rhoout = (a - b*rho*rho)*rho;
  else if (rho >0) rhoout = rhooutmax;
  else  rhoout = -rhooutmax;

  I(in) <+ V(in)/rin;
  I(out) <+ (-2*(rhoout) + V(out))/rout;

  I(in) <+ white_noise(noise_current*noise_current, "LNA_PB");

end
endmodule
```

6.2 Simulations

Simulations in spectreRF are performed to verify the functionality of the model and performance of the VGA. The desired VGA should have a NF of 20dB, V_{IIP3} of 301.5mVrms (-20.4dBm referring to 10kohm is applied in the setup) and programmable gain from 0dB to 60dB.

PSS with PAC, Pnoise are again used to verify the performance of the VGA. PSS is performed with a single input tone at 1kHz for gain and noise simulation. A two tone simulation in PSS at 1kHz and 1.1kHz are applied to verify IIP3 of the VGA.

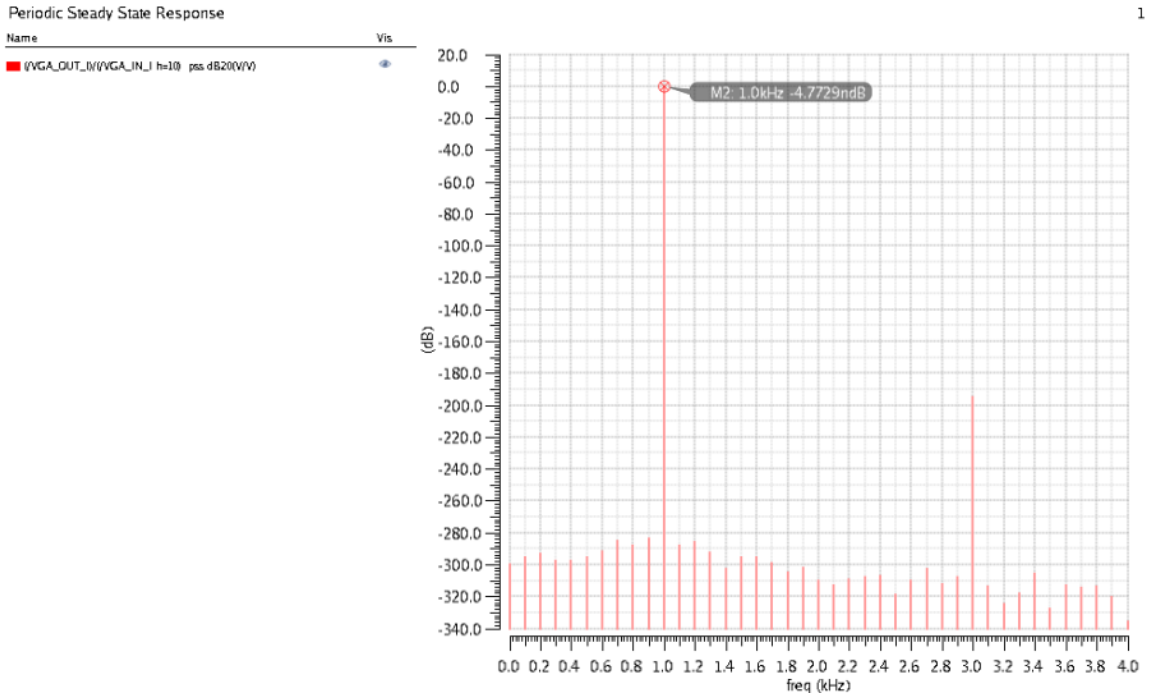

Figure 51: Simulated VGA gain of 0dB at minimum gain mode

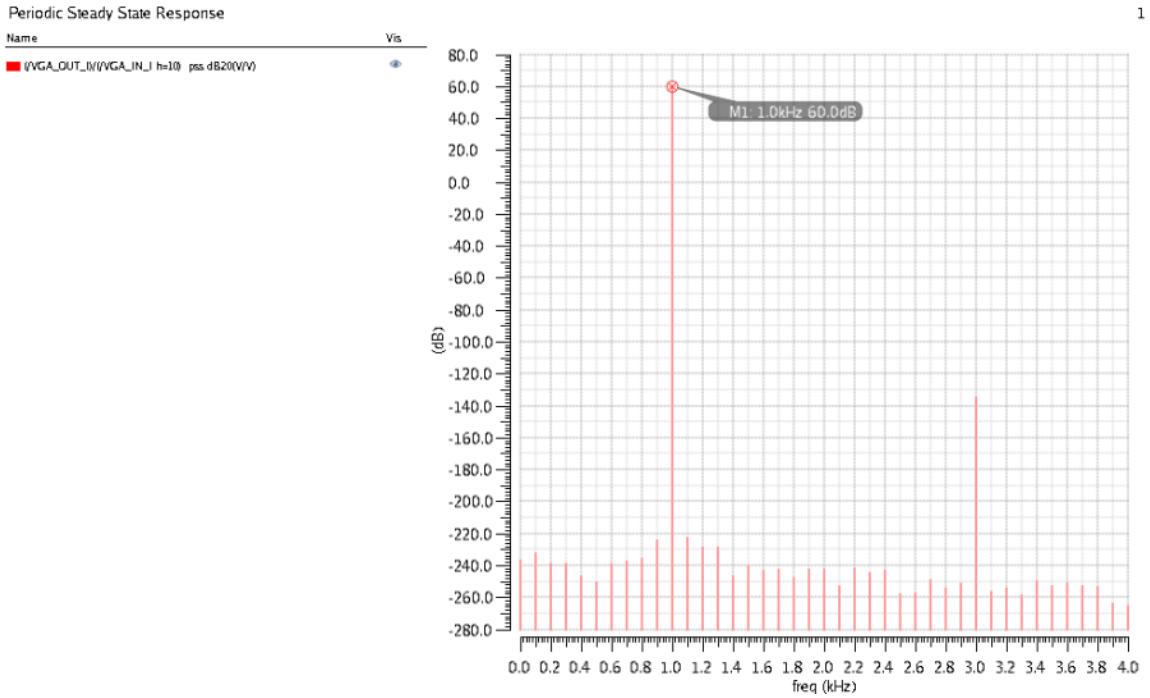

Figure 52: Simulated VGA gain of 60dB at maximum gain mode

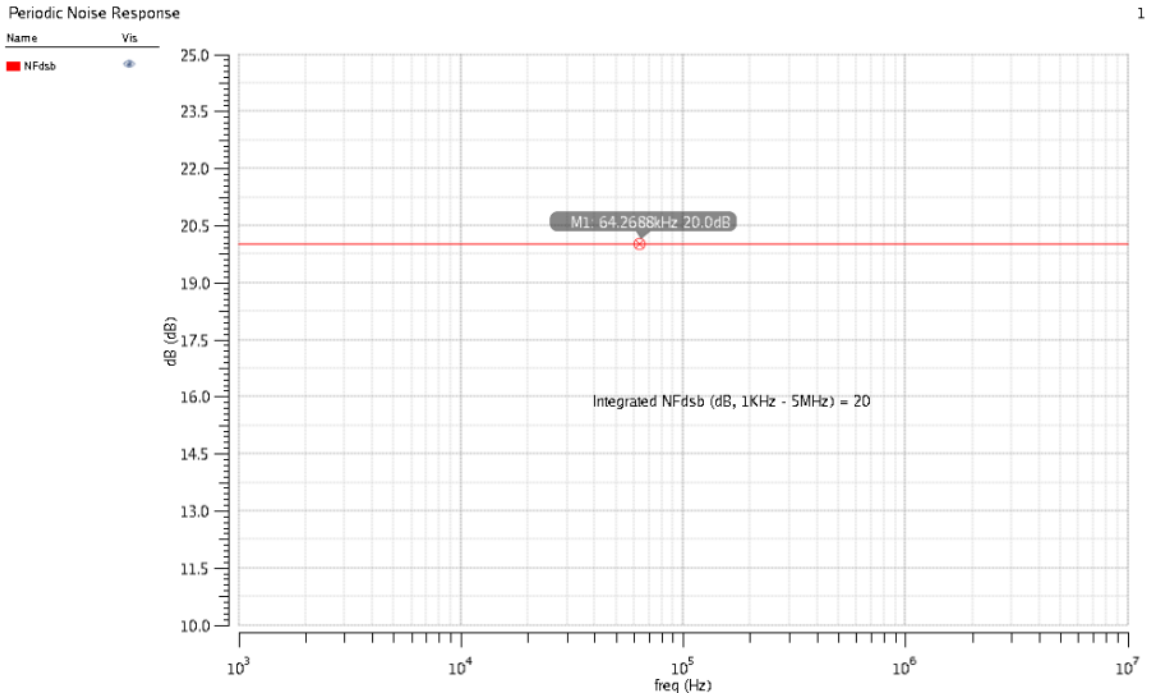

Figure 53: Simulated VGA noise figure

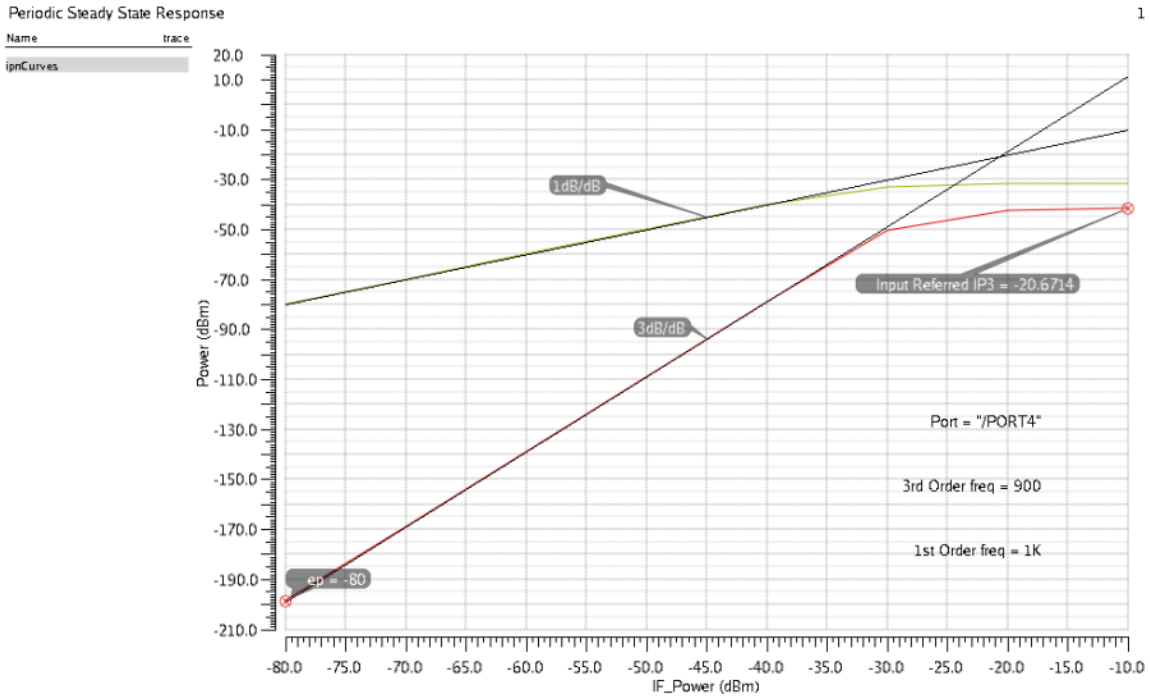

Figure 54: Simulated VGA IIP3 at minimum gain mode (0dB)

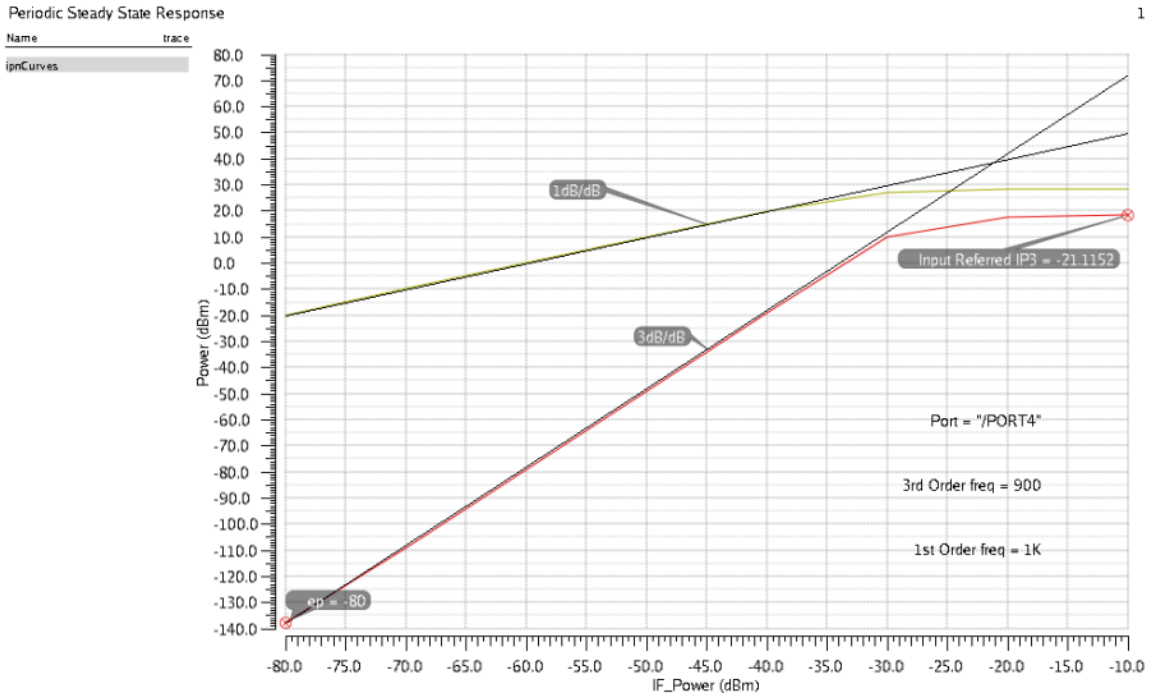

Figure 55: Simulated VGA IIP3 at maximum gain mode (60dB)

7 System Performance and Results

7.1 Front End Top Level Behavioral Simulations

Test bench of the system-level verification with budget simulation. The IF of the test bench is nonzero due to error message from ADS, however it does not affect the result since power gain and noise figure of each blocks are not frequency dependent in this setup.

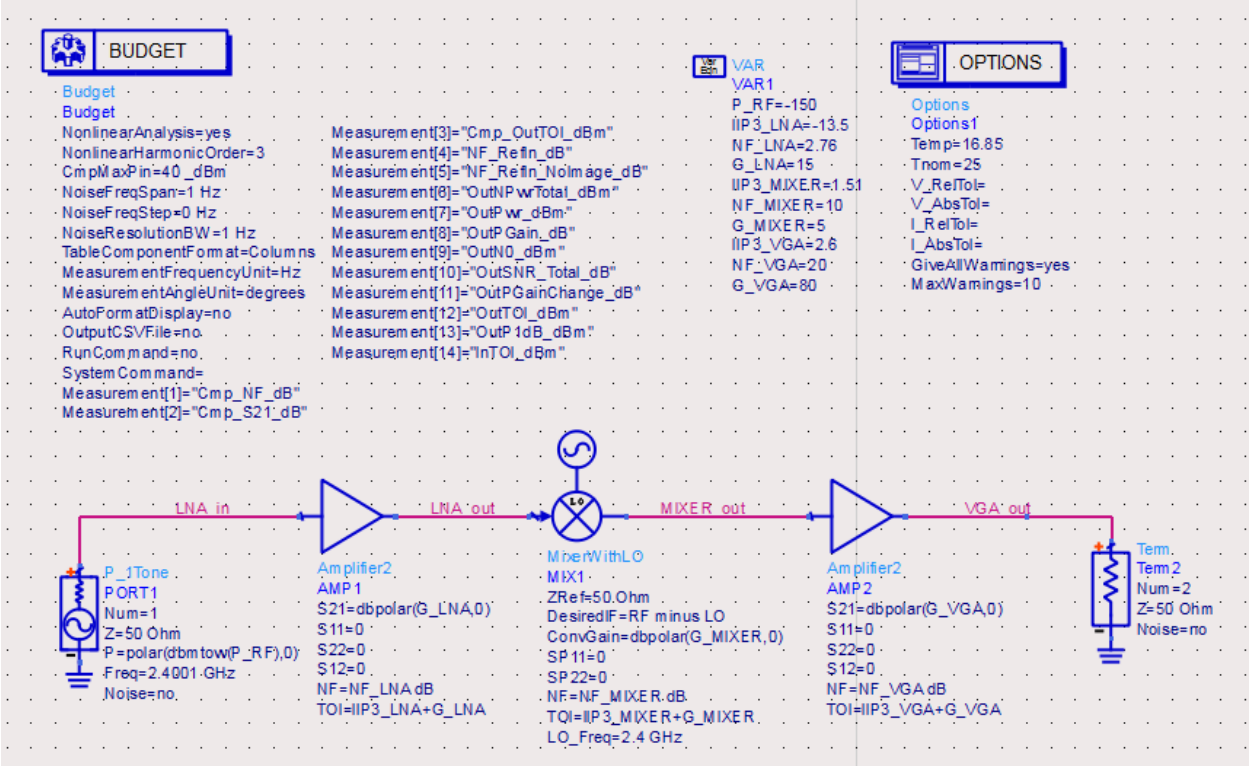

Figure 56: Front End Top Level Behavioral Testbench in ADS

Simulation results verifying the overall NF_{dsb} and the overall IIP3:
Overall NF_{dsb} showing 5dB and overall IIP3 showing -19.986 dBm -> match with calculations
Cmp_index:

0- LNA
1- MIXER
2- VGA

Cmp_Index	Cmp_S21_dB	Cmp_NF_dB	InTOI_dBm	NF_RefIn_NoImage_dB
0	15.000	2.760	-19.986	2.760
1	5.000	10.000	-3.881	3.370
2	80.000	20.000	2.600	5.000

Figure 57: Simulated performance of the behavioral front end

7.2 Front End Top Level Simulations

Finally, the LNA, I/Q mixers and VGAs are cascaded to simulate the overall front end performance. The interface between LNA and mixer has been verified in section 5. The interface between mixer and VGA can be easily configured with a 10kohm shunt resistor to model the input impedance of the VGA. Ideal baluns at the mixer output are used for connecting the differential IF to VGA. This can be eliminated by modifying the VGA source code to accept differential input. Figure 58 shows the top level of the front end. The DC blocking capacitor of 250fF between the LNA and mixer is lumped into the LNA symbol. Besides the final VGA output driving a 1pF, a 10kohm port is also placed in parallel for probing simulation results, as well as defining the output resistance for the behavioral VGA block. Simulations are performed with PSS+PAC+PNOISE to extract the performance of the RF receiver front end.

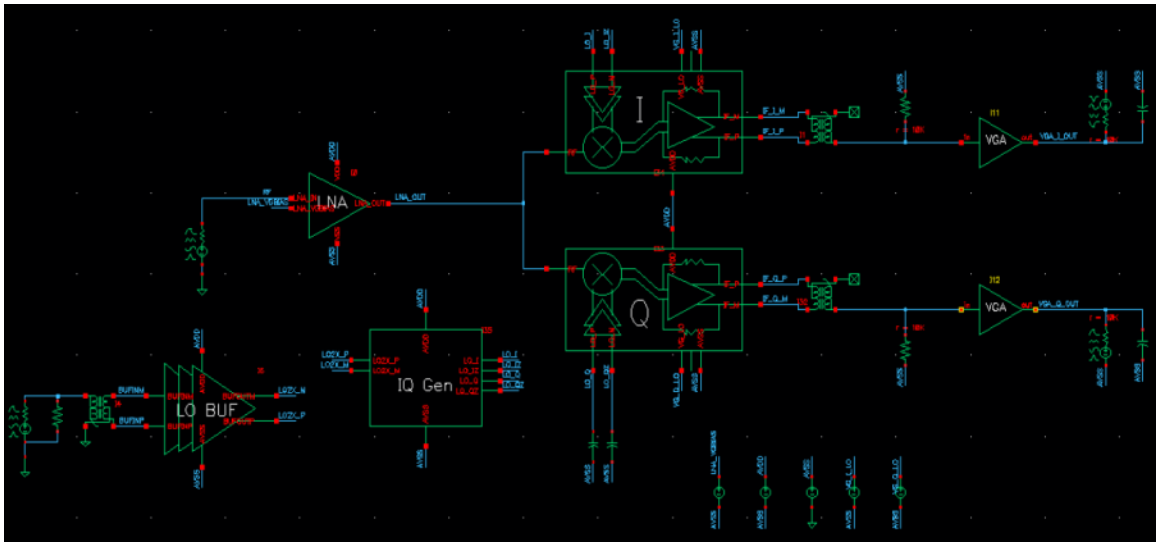

Figure 58: Top level design schematic of the RF front end

Similar to the other sub-block simulations, PAC simulation is performed to simulate the voltage conversion gain of the RF front end with IF from 0Hz to 5MHz. In this setup, LO is the only large signal and RF is the small signal. Simulated voltage conversion gain

at minimum and maximum gain mode are 20dB and 80dB respectively, agrees with adding both the gain of sub-blocks in dB.

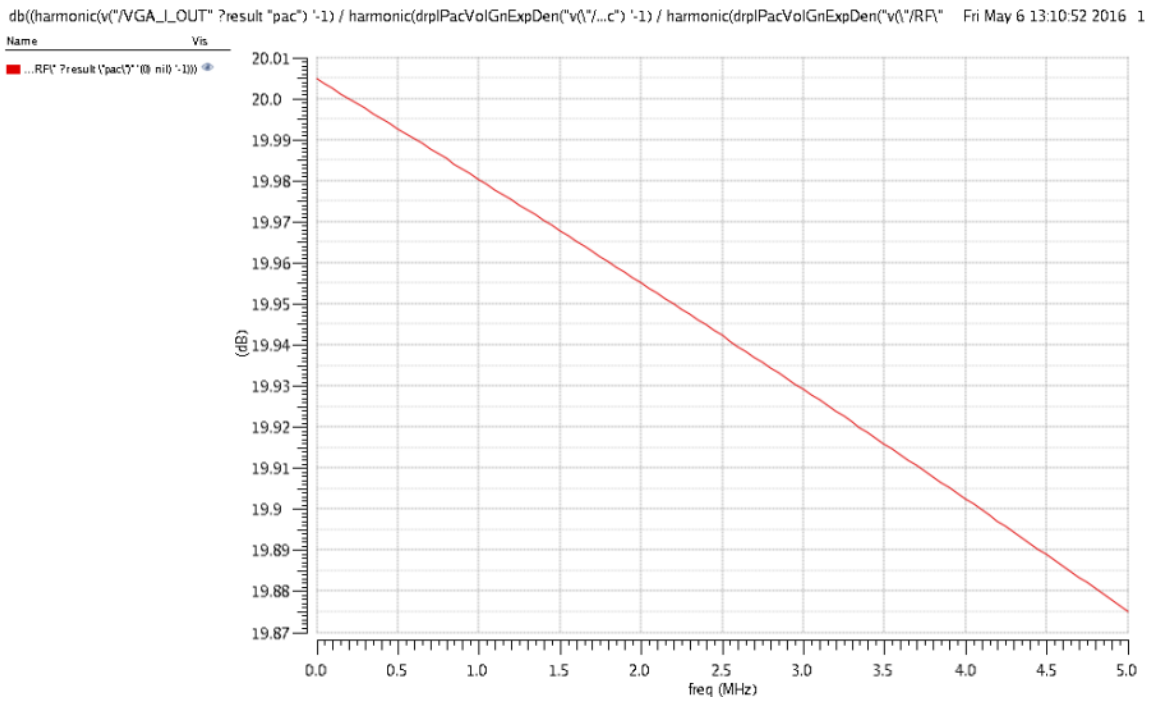

Figure 59: Simulated RF front end gain at minimum gain mode

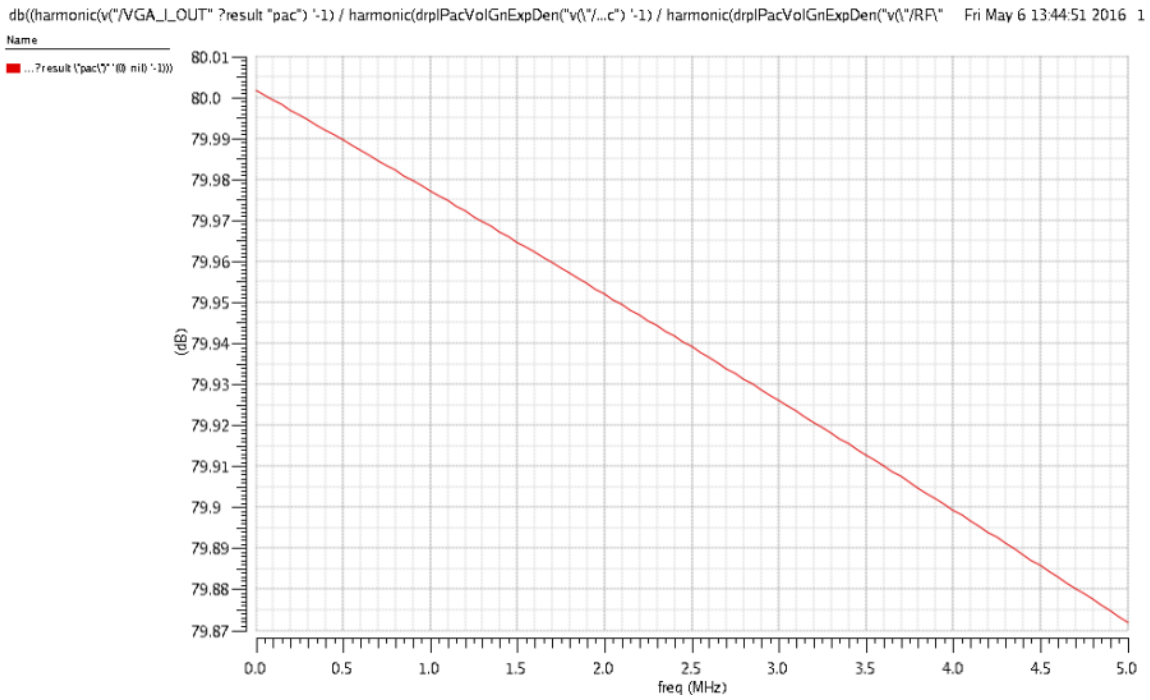

Figure 60: Simulated RF front end gain at maximum gain mode

Pnoise simulation is also performed to simulate the double-sideband noise figure of the mixer with IF from 1kHz to 5MHz. From the noise equation with the simulation data, we expect the noise figure at high frequency region where flicker noise is negligible to be:

$$\mathrm{NF}_{\mathrm{LNA+MIXER}} = 10 * \log\left(10^{\frac{NF_{LNA}}{10}} + \frac{10^{\frac{NF_{MIXER}}{10}} - 1}{G_{LNA}} + \frac{10^{\frac{NF_{VGA}}{10}} - 1}{G_{LNA}G_{MIXER}}\right) = 4.67\ dB$$

, matches closely with the simulated NF at 5MHz of 4.76 dB.

The simulated integrated DSB noise figure cascading LNA and mixer from 1kHz to 5MHz is 5dB for both minimum and maximum gain setting.

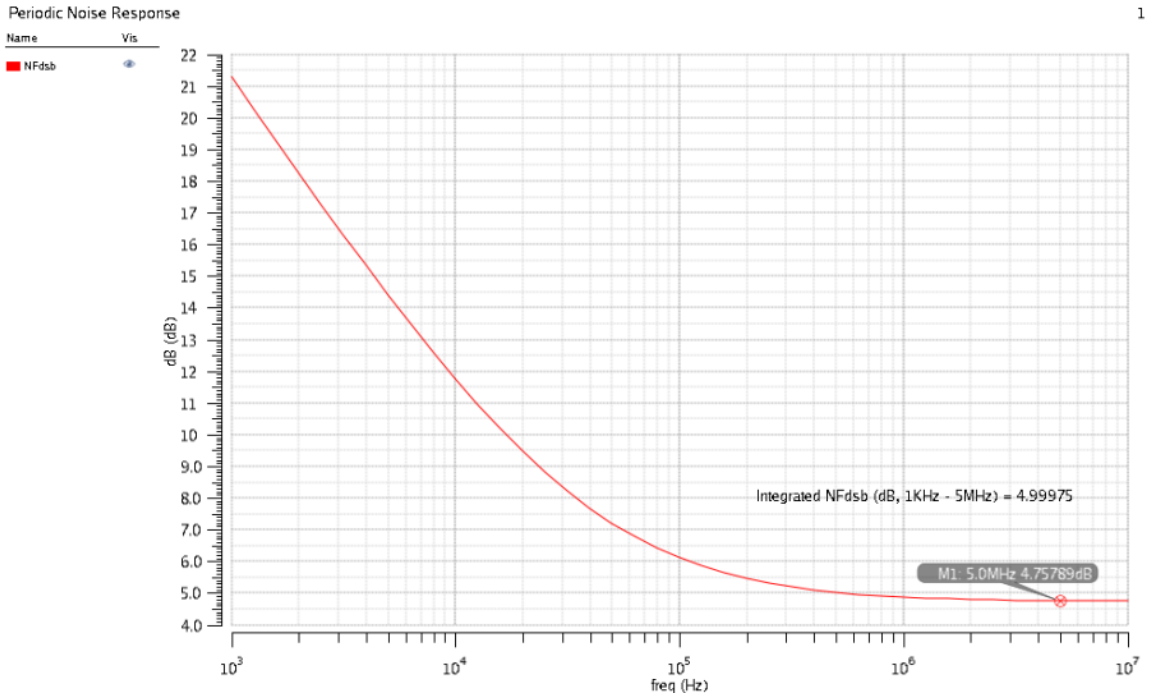

Figure 61: Simulated RF front end double-sideband noise figure at minimum gain mode

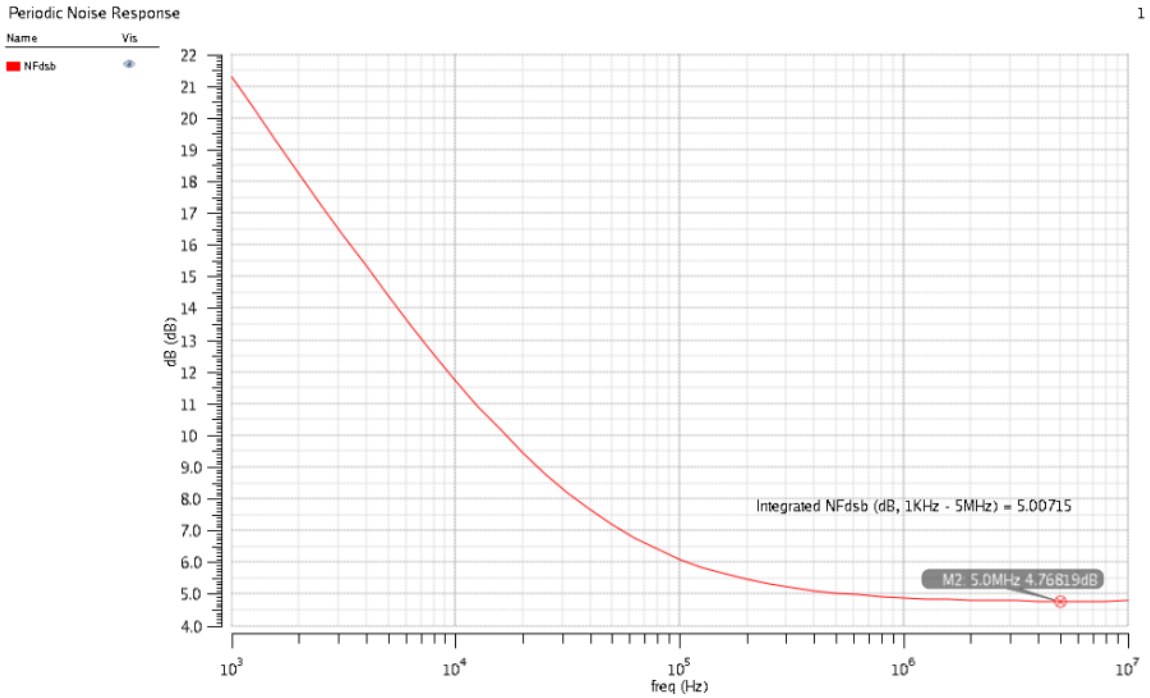

Figure 62: Simulated RF front end double-sideband noise figure at maximum gain mode

PSP is performed to confirm that input matching is still within the specification of < -20dB in the RF bandwidth of 2.4GHz +/- 5MHz.

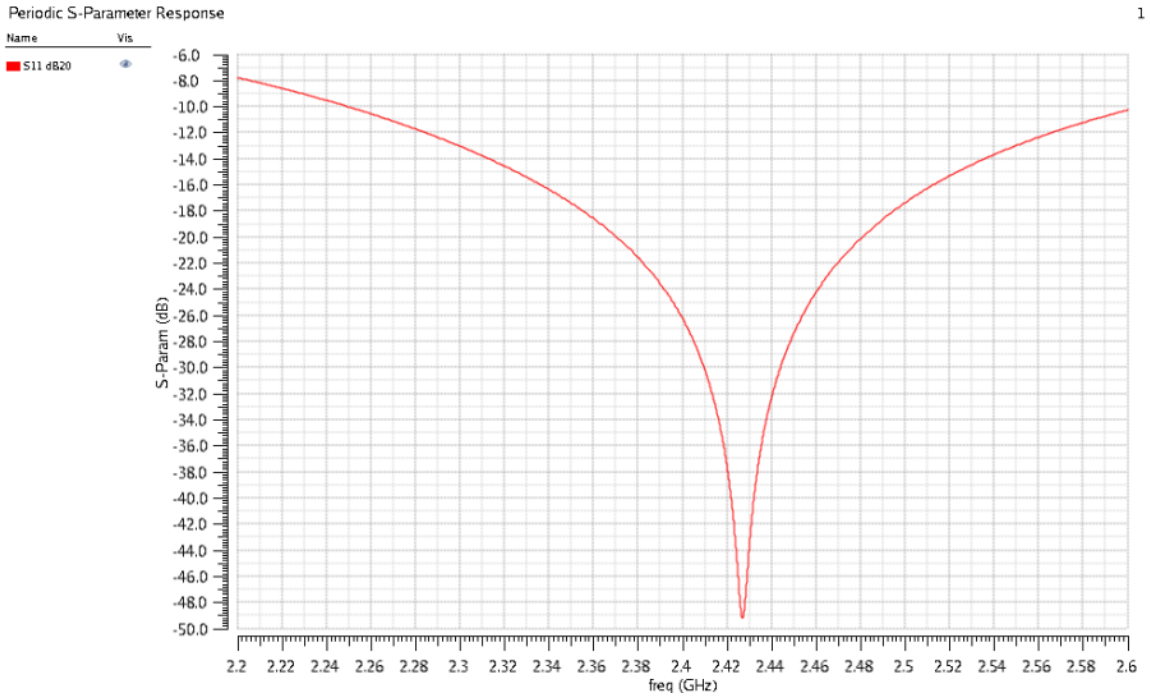

Figure 63: Simulated RF front end S_{11}

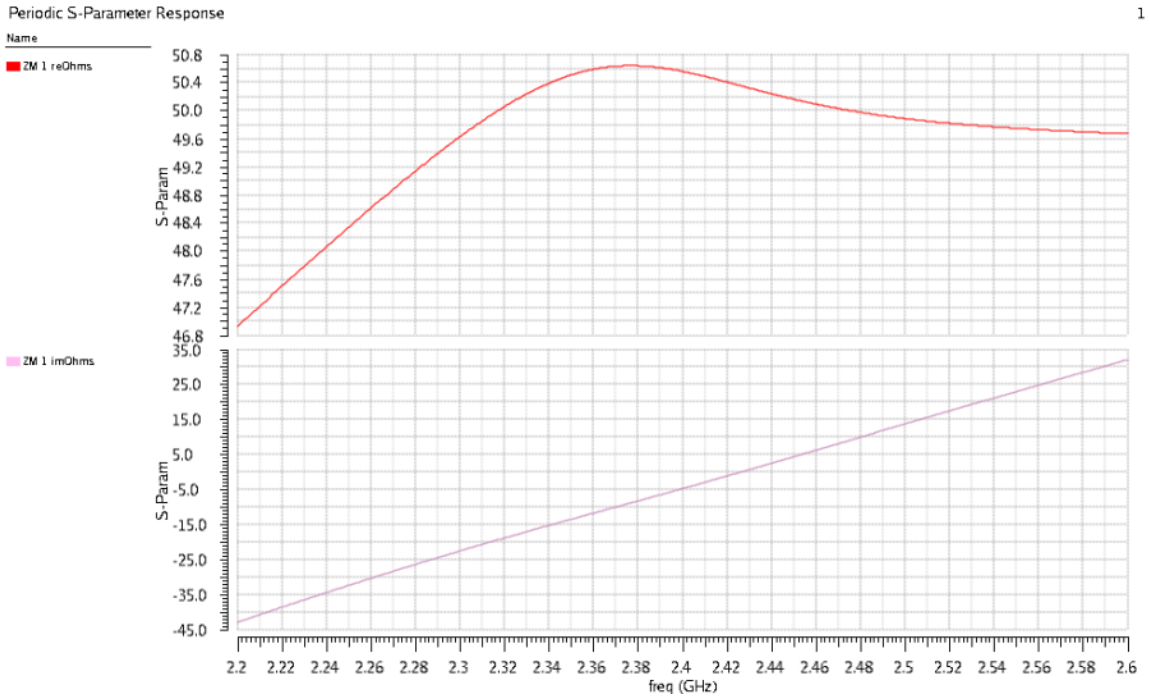

Figure 64: Simulated RF front end input impedance

LO-RF feedthrough is an important metric in DCR and should be minimized to reduce the amount of LO self-mixing which creates additional DC offsets to the DCR. The LO is probed at the output of the I/Q generator (2.4GHz).

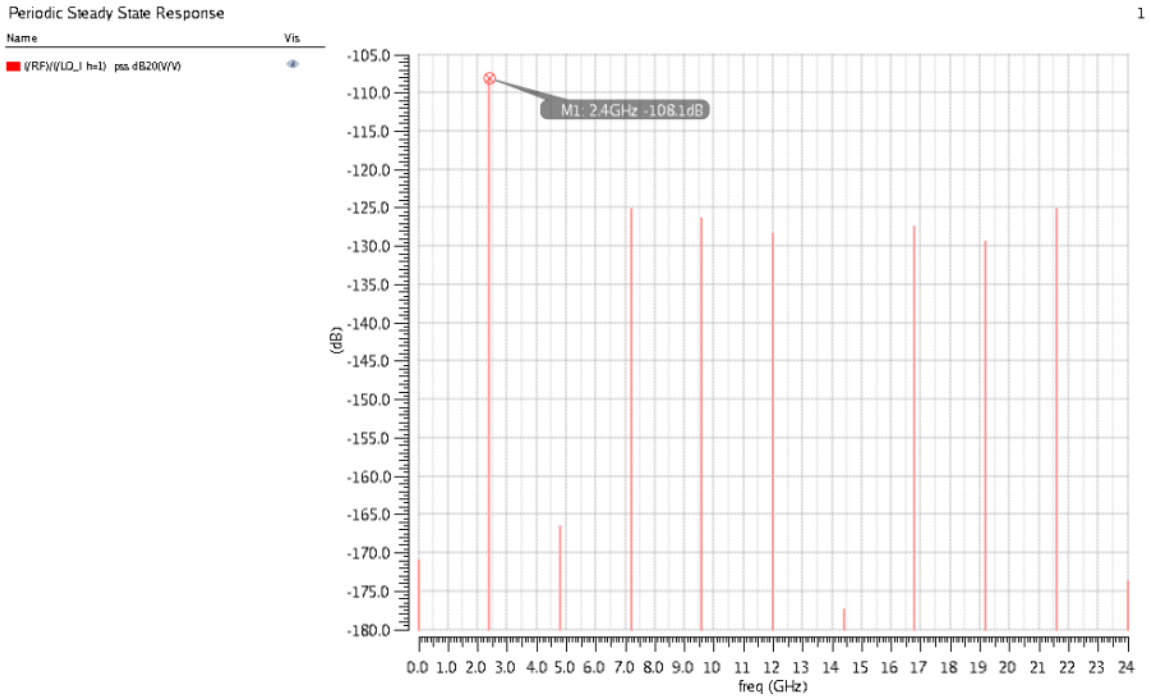

Figure 65: Simulated RF front end LO-RF feedthrough

QPSS along with QPAC is used to perform the linearity simulation. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV). The simulated IIP3 is < -19 dBm in both min. and max. gain setting, which is within the required specification. The simulation errors of IM3 at medium RF power can be ignored due to interpolation occurs at the RF power of -90dBm as shown in the figure, and IM3 exhibits a slope of 3dB/dB around that RF power region. The inaccuracy is caused by compact MOSFET models with a singularity at Vds=0 (particularly valid in a passive mixer), therefore not able to model distortion properly. [6]

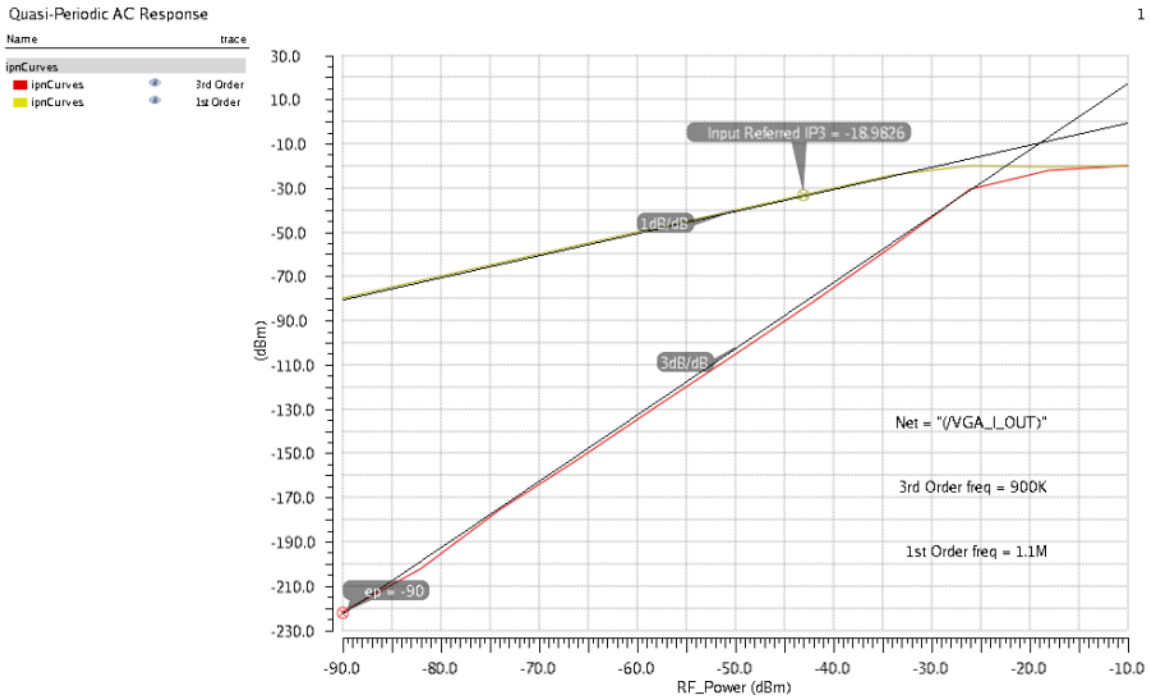

Figure 66: Simulated RF front end IIP3 at minimum gain mode

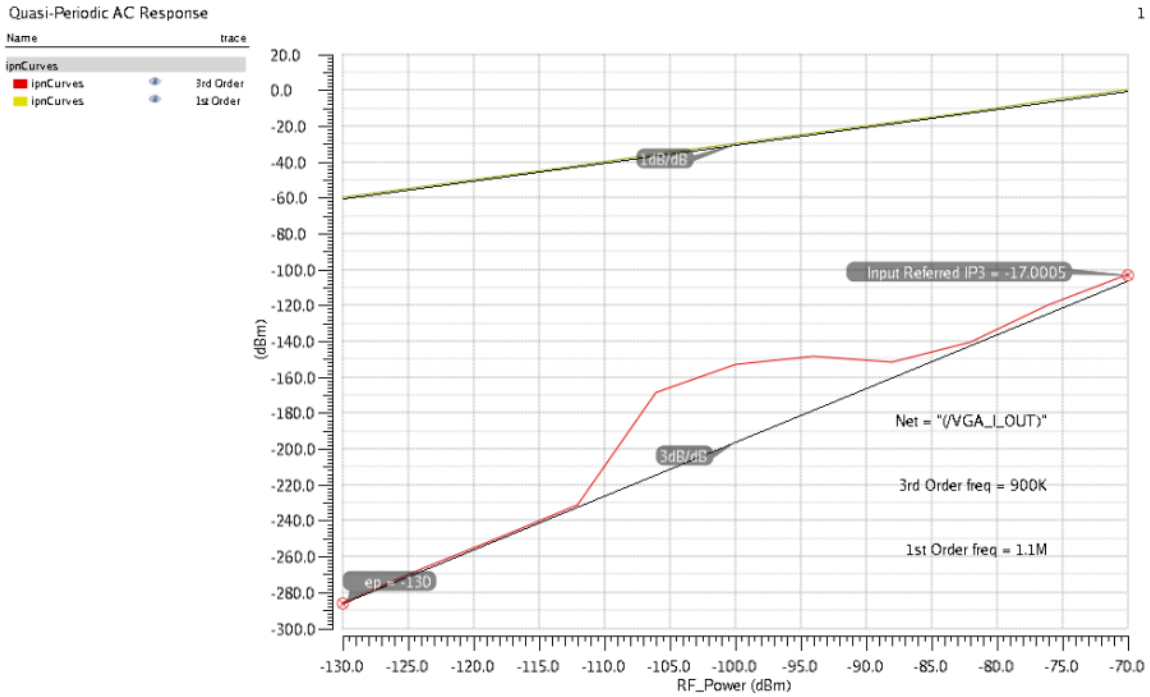

Figure 67: Simulated RF front end IIP3 at maximum gain mode

Similarly, IM2 is simulated and find IIP2. Note that y-axis is actually plotted with voltage with 1ohm reference (dBV). Simulated IIP2 for the front end is 14dBm, which is within the specification.

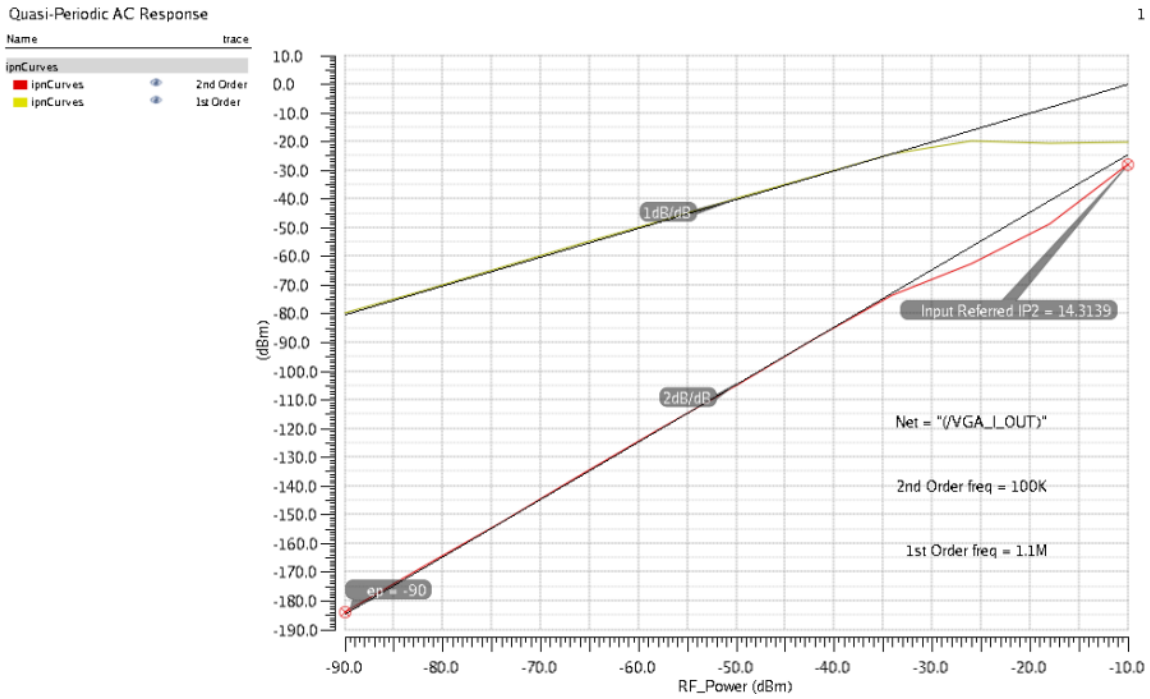

Figure 68: Simulated RF front end IIP2

In the simulation, I/Q is nearly ideal in term of matching, therefore the achievable IIR really depends on the process mismatch and layout parasitics mismatch. Figure 69 shows the achievable IIR versus gain and phase imbalance [8]. In this study, LO buffers and I/Q generator are operating from the same supply and signals are at CMOS full swing. We can therefore assume the main contribution of mismatch is coming from phase imbalance. With a 0dB of gain imbalance, we can tolerate up to 1˚ of phase imbalance to achieve 40dB image rejection.

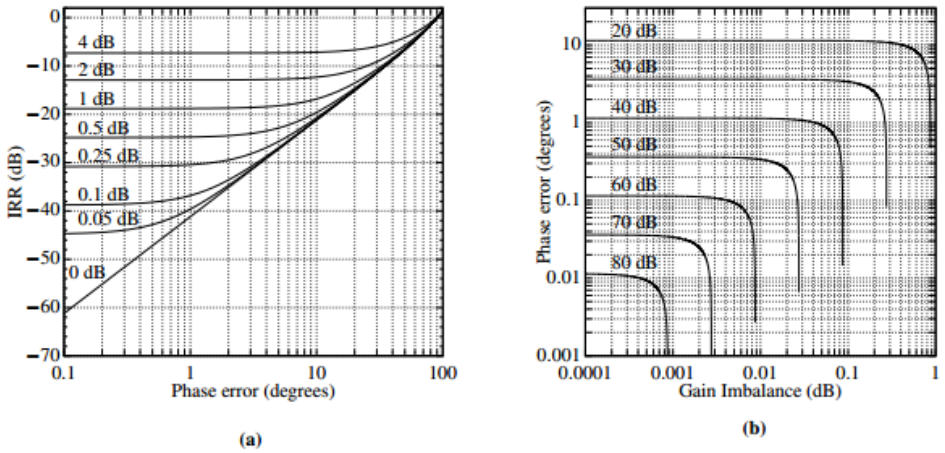

Figure 69: Image rejection ratio (IIR) versus gain and phase imbalance [8]

7.3 Overall Front End Performance

TABLE VIII
RF FRONT END DESIGN PERFORMANCE SUMMARY

Parameter	Specification	Simulated
V_{DD}	1 V	1 V
$I_{DD,AVG}$	< 1.8 mA (including LO buffer, IQ generator)	1.47 mA
LO port power consumption	< 200 µA	64 uA (@-15dBm,200Ω) Multiplied by 2 to consider differential LO
$I_{tot,avg}$	< 2 mA	1.53 mA
Load	10 kohm // 1pF	10 kohm // 1pF
RF Input Frequency	2.4GHz ± 5MHz	2.4GHz ± 5MHz
LO Input Frequency	4.8 GHz	4.8 GHz
I/Q mixer LO	2.4 GHz	2.4 GHz
IF Output Frequency	0 Hz – 5 MHz	0 Hz – 5 MHz
Voltage Gain (minimum)	20 dB	20 dB
Voltage Gain (maximum)	80 dB	80 dB
NF_{DSB}	< 5 dB	5 dB
IIP_3	> -20 dBm	-19 dBm
IIP_2	> +10 dBm	14.3 dBm
S_{11}	< -20 dB	< -26 dB
LO-RF feedthrough	< -100 dBc	-108 dBc
I/Q Phase imbalance for 40dB IRR	< 1˚	0.077˚ (no mismatch)

8 Conclusion

The theme of this Master's research project was the design of a low noise RF direct conversion receiver front end. The goal was to minimize the power consumption while achieving a set of specifications such as noise figure, linearity, input return loss, LO-RF feedthrough, etc…

The front end was designed and simulated in a commercial 65nm CMOS process, and has met all the required specifications. The total power consumption is 1.53mW, which is 24% lower than the required specification. It achieves an integrated noise figure of 5dB from 1kHz to 5MHz with programmable gain from 20dB to 80dB. It also has an IIP3 linearity of -19dBm and IIP2 linearity of 14dBm.

Main design blocks such as LNA, I/Q mixer, and VGA are all analyzed, simulated and verified by itself first, then going with step-by-step to eventually cascade all blocks to form a functional RF front-end.

In the front end design, LO buffers and I/Q generation circuits are also designed to incorporate more non-linearities of the front end. Flicker noise and thermal noise contributions from these blocks are included and they can significantly affect the noise performance due to operating the receiver at zero-IF. Although the VGA is a Verilog-A behavioral model, it has included all the non-ideal effects such as noise figure and nonlinearity. The only ideality in this design is the op-amp used for the IF amplifier in the passive mixer, which can contribute additional noise to the system.

LO-RF feedthrough is also minimized to reduce LO self-mixing for DCR by incorporating cascode device in the LNA to provide extra reverse isolation from LO input of the mixer to the RF port.

Besides the design work done in this project, detailed hand analysis of noise figure and linearity of the LNA, as well as noise analysis of the mixer are also included to provide a better understanding on the design optimization and tradeoffs.

Bibliography

[1] B. Razavi, "Design Considerations for Direct Conversion Receivers, "IEEE Transactions on Circuits and Systems – II Analog and Digital Signal Processing, vol. 44, No. 6, June 2007, pp. 428-435.

[2] A. Mashhour, W. Domino, N. Beamish, On the Direct Conversion Receiver -- A Tutorial http://www.microwavejournal.com/articles/3226-on-the-direct-conversion-receiver-a-tutorial

[3] A. Niknejad, UC Berkeley EE242B lecture notes, http://rfic.eecs.berkeley.edu/~niknejad/ee242/

[4] M. Perrott, MIT 6.976 lecture 10 notes, http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-976-high-speed-communication-circuits-and-systems-spring-2003/lecture-notes/lec10.pdf

[5] S. Chehrazi, A. Mirzaei, A. Abidi, Noise in Current-Commutating Passive FET Mixers, IEEE TCAS-I, Vol. 57, No. 2, Feb. 2010

[6] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C. C. McAndrew, X. Gu, and G. Gildenblat, "RF distortion analysis with compact MOSFET models," in Proc. CICC, Oct. 2004, pp. 9–12.

[7] Chen, J. E. Modeling RF Systems. http://designersguide.org/Modeling/modeling-rf-systems.pdf

[8] Luís Filipe da Costa Malheiro, Polyphase Filter with Parametric Tuning, University of Porto Master's thesis

[9] Top 7 Ways to Create a Quadrature (90˚) Phase Shift http://www.markimicrowave.com/blog/2015/04/top-7-ways-to-create-a-quadrature-90-phase-shift/

[10] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1341-1350, 2008
.
[11] R. Ramzan, (Tutorial) Gilbert Mixer Simulation (Cadence SpectreRF), Linköping University, Sweden