Ultra-low Power Wake-up Radio for Low Activity Wireless System

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By

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Fall 2014

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Abstract

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Recent advances in low power radio design have enabled a broad range of low activity applications such as smart utilities, health monitoring, building and industry automation, automotive control and monitoring, wireless control and etc. The key challenge to implement these applications is to reduce the average power consumption spent on wireless communications. A traditional way to solve this is to implement protocol based duty cycling which leads to a tradeoff between reduced average power consumption and increased system latency. A smarter solution is to use a dedicated wake-up receiver continuously monitoring the channel and activating the main receiver upon detection of a wake-up signal. The use of a wake-up receiver helps to improve the overall power performance while keeping the system latency bounded.

This dissertation addresses challenges and concerns of designing an ultra-low power high performance wake-up radio. It proposes a two-step wake-up architecture including energy detection mode and address detection mode to reduce the active power dissipation meanwhile improving the robustness and reliability of the system. Design metrics has been provided to serve as a guideline for detailed circuit implementations. Based on that, a wake-up radio prototype has been built in TSMC 65nm standard CMOS targeting 915MHz band for IEEE 802.15.4g. This prototype focuses on improving the sensitivity performance at an ultra-low power level. It consumes only 45μW in energy detection mode. With 20μs detection time, it is able to achieve a sensitivity of -90dBm at 10^{-2} error rates. In address detection mode, it consumes 300 μW and is able to achieve a sensitivity of -74.5dBm at 10^{-3} BER.

To my beloved parents and husband

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Chapter 1

Introduction

1.1 Motivation

Recent advances in low-power radio design have enabled a broad range of new applications, such as wireless senor networks (WSNs) [Rabaey02], wireless body area networks (WBANs) [IEEE12-1], wireless personal area networks (WPANs) [IEEE03] and etc. In many of these applications, the wireless nodes are used to monitor certain events which occur at low activity rate. The radio link remains inactive until events occurs and then information is gathered, processed and exchanged among nodes or between nodes and central hub with limited protocol overhead and communication delay. Such scenarios can be found in smart utilities, health monitoring, building and industry automation, automotive control and monitoring, wireless control, and many other applications. All these applications require extremely low power wireless nodes so as to last for years without battery recharge or replacement. Some applications require usage of energy harvesters to supplement or completely replace the battery, yet state-of-the-art energy harvesters, for example, sub-mm solar cells under moderate illumination can only provide up to 100μW power [Ingram11] for a wireless node. Therefore the key challenge to implement these low activity applications remains in designing a wireless node consuming the lowest amount of energy possible.

A classic wireless node implementation includes radios, sensing interfaces, memory, a processor and power management. Among all the functions, the dominant component is the wireless communication energy which is usually spent on data exchanging, idle monitoring, collision avoidance, control packet overhead, overhearing [Lin05]. For a typical low activity application, communications are sparse, in other words, the packet traffic load is usually light and packets are usually short. With such traffic characteristics, nodes will spend most of the time idle monitoring the channel. Therefore, the high-level goal of this research is to reduce the energy dedicated to the idle monitoring.

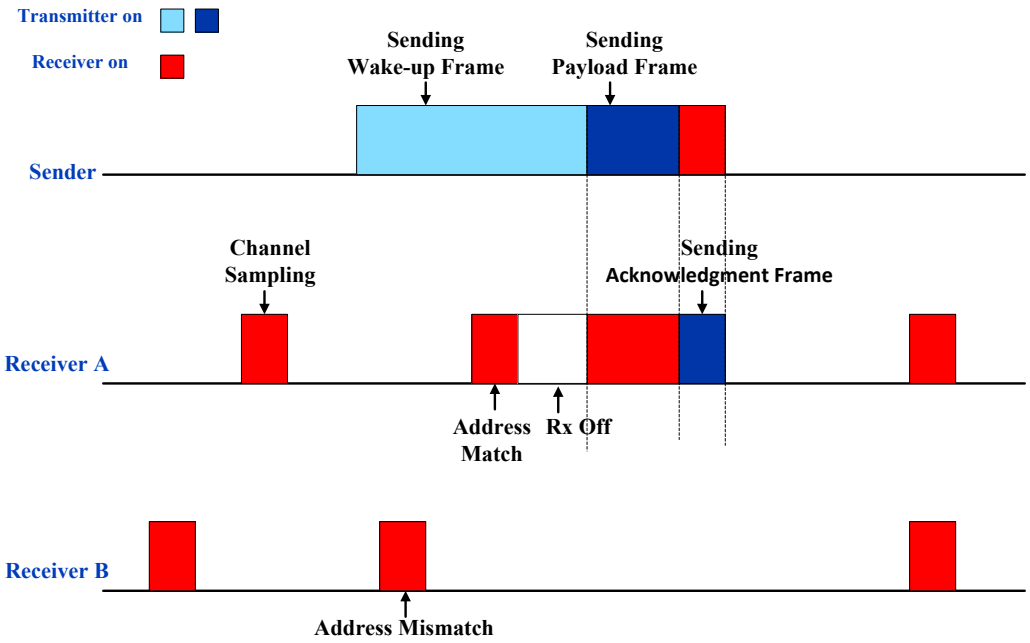

Figure 1.1 Protocol Based Duty-Cycling Example: CSL for 802.15.4e

1.2 Protocol Based Duty-Cycling Vs Reactive Wake-up Receiver

A traditional way to reduce the energy for idle monitoring is to implement protocol-based duty-cycling. Depending on the protocol, communication could be initiated by either the transmitting device or the receiving one. Taking 802.15.4e as an example, it provides two low-energy mechanisms: coordinated sampled listening (CSL) and receiver initiated transmission (RIT) [IEEE12-2].

Figure 1.1 shows an example of CSL. It allows the receiving device to periodically sample the channel for incoming transmissions at low duty cycles. If the channel sample does not detect energy on the channel, CSL disables the receiving device until the next channel sample. If the channel sample receives a wake-up frame, CSL checks the destination address in the wake-up frame. If it does not match, CSL disables receiver until the next channel sample. Otherwise, CSL disables receiving devices until the Rendezvous Time in the wake-up frame from now and then enables receiving device to receive the payload frame, send back a secure acknowledgment frame and return back to periodical channel sampling.

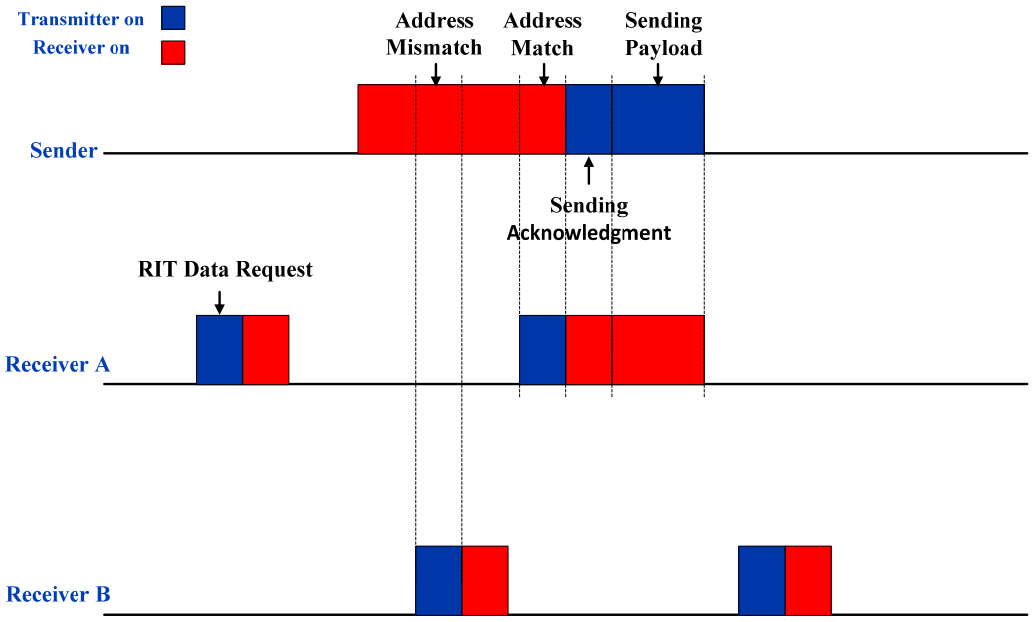

Figure 1.2 Protocol Based Duty-Cycling Example: RIT for 802.15.4e

Figure 1.2 shows another example of RIT. In RIT mode, a receiving device periodically transmits a RIT data request command and then listens to the channel for a while for an incoming frame at low duty cycles. If no incoming frame is detected, the device goes back to idle state till the next periodic transmission of RIT data request command. If an acknowledgment frame is received, the device stops periodic transmission and prepares to receive the payload frame. The transmitting device stays awake until it receives a RIT data request packet from the destination, and then sends out a secure acknowledgment and payload frames.

Both CSL and RIT utilize low duty-cycling of receiving node to reduce the energy dedicated to idle monitoring so as to reduce the total energy consumed by each node. CSL and RIT are used under different latency requirements. CSL is suitable for applications with a relatively low latency requirement, e.g., less than 1 second while RIT is suitable for applications with a high latency tolerance, e.g., tens of seconds. Although CSL and RIT are low energy mechanisms, significant energy may still be wasted on sender's side by sending long wake-up sequence or monitoring the channel long time for data request and on receiver's side by periodic channel sampling or sending data request. More importantly, there exists an inherent trade-off between average power consumption and average network latency. For many low latency applications, the protocol must be adjusted to increase duty-cycling of receiving node, thus increasing average power consumption.

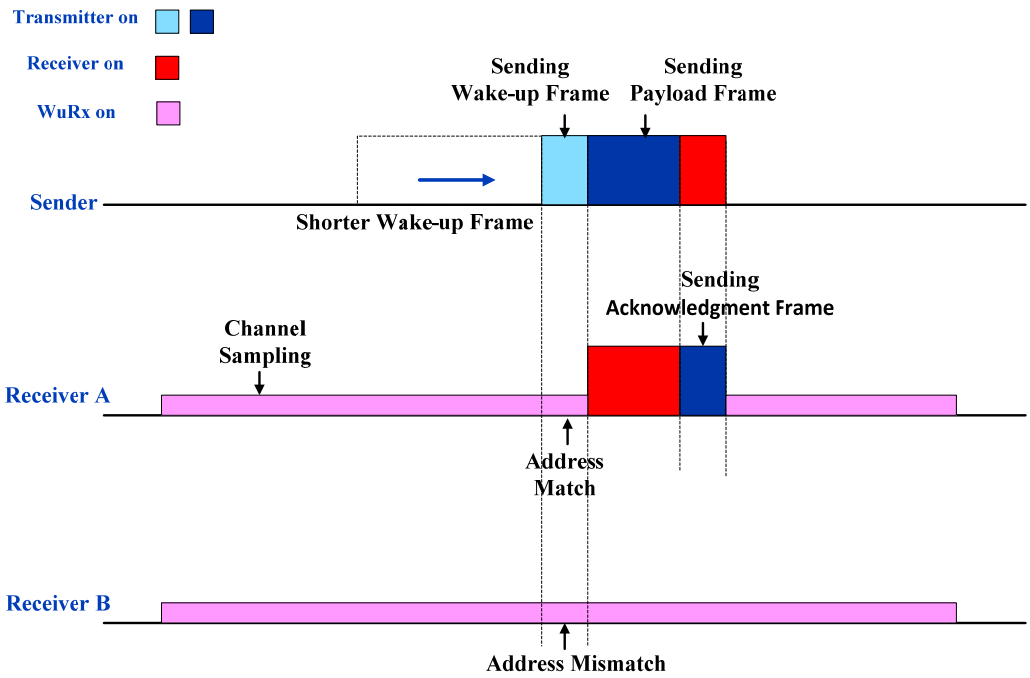

Figure 1.3 Communication with Reactive Wake-up Receiver

An alternative to protocol-based duty-cycling is to add an auxiliary receiver called wake-up receiver (WuRx) to each node. As shown in figure 1.3, during idle monitoring, the main transceiver is off and only WuRx is on. It continuously monitors the channel for incoming transmissions. When it detects a wake-up sequence, it will wake up the main receiver for data communication immediately. Figure 1.4 compares the performance of average power consumption and average network latency between protocol-based duty-cycling (CSL mechanism) and reactive wake-up receiver by using the power numbers from WuRx literature [Pletcher09] and Atmel AT86RF233 [Atmel14]. It assumes the control packets (ACK, Wake-up Frame) are 40 bits long and the data packet is 200 bits long, all with an 18bit preamble. The transceiver data rate is 50k bits per second and each device has 5 neighbors. It can be clearly seen from the figure that the use of a wake-up receiver breaks the trade-off between network latency and average power consumption. It can help to effectively reduce the average power consumption of each node while keeping the latency bounded. However, when traffic load (network activity) becomes low, the power consumption of WuRx starts to dominate the energy consumed by each node. Therefore, it is crucial to keep the power budget of WuRx at really low level.

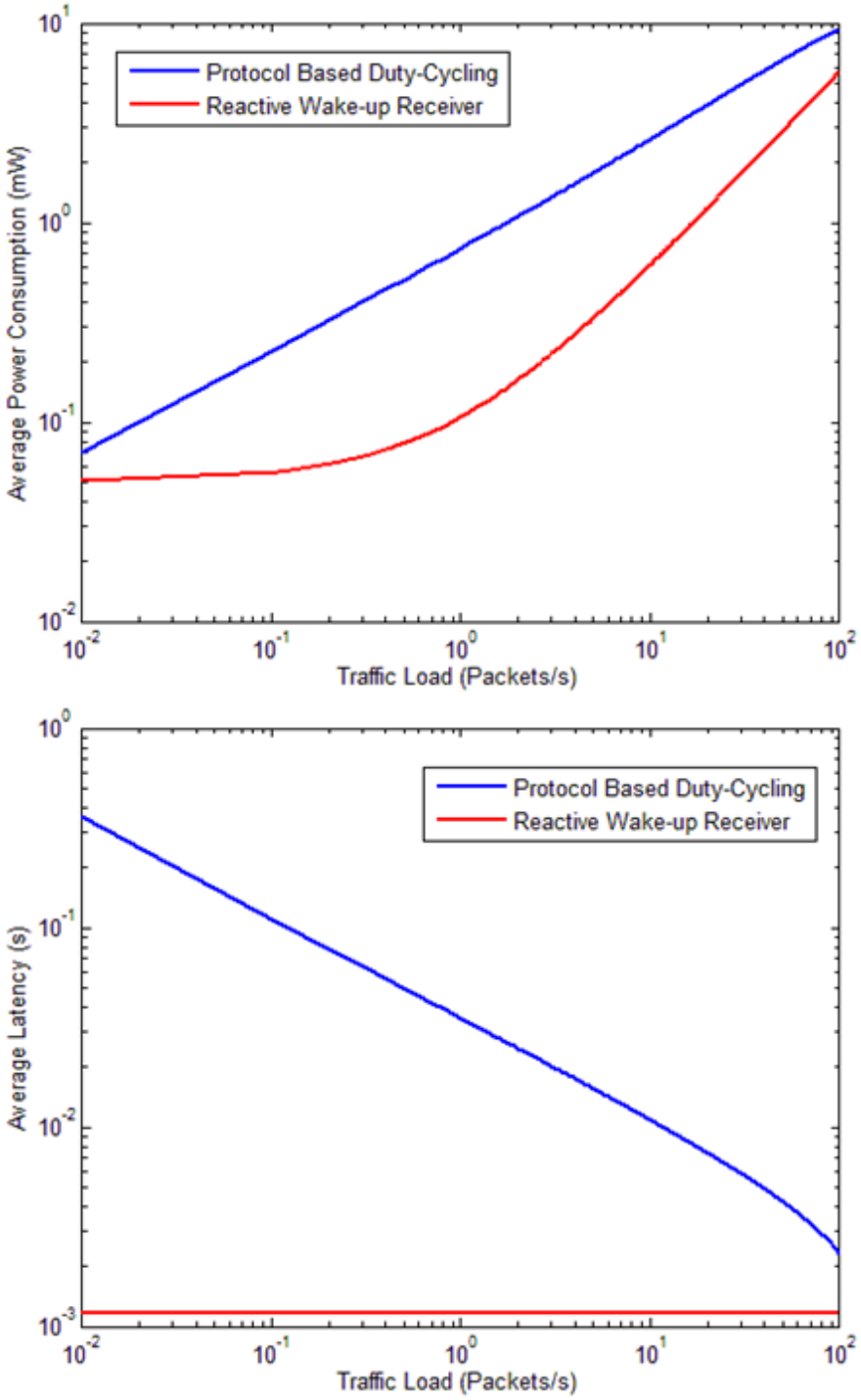

Figure 1.4 Performance Comparison between Protocol Based Duty-Cycling and Reactive Wake-up Receiver

1.3 Dissertation Outline

This dissertation investigates the possibility of designing an ultra-low power, low latency receiver for low activity wireless links. It provides system level analysis methodology as well as circuit level design techniques for implementation of a practical wake-up receiver. It is organized in six chapters. After this introduction, Chapter 2 presents a high level overview of the design considerations and functional specifications for the wake-up receiver. It also proposes a two-step wake-up architecture including energy detection mode and addressing mode for the wake-up receiver and discusses its system level design metrics in details. Chapter 3 describes the design and implementation of energy detection mode. It proposes an effective technique to achieve high sensitivity with limited power budget. Following that, Chapter 4 details the design and implementation of addressing mode. Chapter 5 presents the measurement results. Finally, Chapter 6 concludes with a brief summary of this dissertation and discussion of future research directions. A bibliography is included in the appendix.

Chapter 2

System Level Design

2.1 Design Consideration

The specifications and implementation of the wake-up receiver rely heavily on the intended applications. In this research, our goal is to design a wake-up receiver for low activity wireless network and to build a prototype compatible with 802.15.4g [IEEE10].

2.1.1 System Integration

At the system level, the wake-up receiver must integrate conveniently with the main transceiver. The overall system architecture together with WuRx is shown in figure 2.1. The WuRx shares the same antenna with the main transceiver for minimum size and easy integration. To reduce hardware cost, it is desirable for the WuRx to receiver signals from the same transmitter used for data communications, such that no additional wake-up transmitter is required. Therefore, the implementation of WuRx will use the same carrier frequency, modulation scheme and data rate as the main transceiver. In 802.15.4g, it specifies nine different frequency bands for narrow band operation including 450 MHz, 470 MHz, 863 MHz, 896/901 MHz, 901/902 MHz, 915 MHz, 928/960 MHz, 1427/1518 MHz and 2450 MHz as well as ultra-wideband (UWB) operation; It also specifies three different modulation schemes including FSK, OFDM and QPSK and various data rate ranging from 10kbps up to 200kbps. In this research, we target to build a WuRX prototype for 915MHz ISM band with FSK modulation scheme and 50kbps data rate. When implementing the WuRx, compatibility with 802.15.4g at the MAC layer is not necessary. A dedicated wake-up command or sequence can be designed and used, as it only add one additional instruction set to DSP or one additional state to the state machine. Its power overhead is negligible.

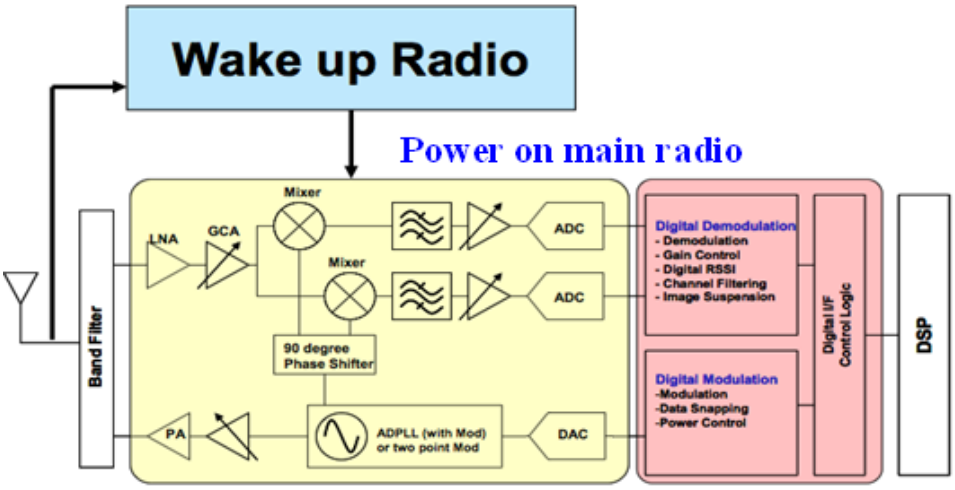

Figure 2.1 System Integration with WuRx

2.1.2 Active Power Oriented

For a general purpose low power transceiver design, the energy efficiency is usually the most important metric it targets for, as it is typically used in data driven applications where energy per transferred bit is more closely tied to the battery life of a wireless device. During its communication, protocol-based duty cycling is implemented. As previously mentioned, with extremely low duty cycling, high active power consumption can be tolerated as long as the data rate is high enough to result in an overall low energy per bit. However, a WuRx is essentially an event driven receiver that detects whether there is communication in the channel and asserts a signal to wake up the main data receiver. At the most basic level, it is just a one bit RF energy detector. Therefore, energy per bit is meaningless to WuRx and active power consumption is the most critical metric for WuRx design. Moreover the WuRx needs to listen to the channel continuously and cannot take advantage of duty-cycling. This means that transceiver architecture such as UWB is not suitable for WuRx since it depends on heavy duty-cycling and synchronization to achieve low energy per pit.

The active power consumption specification depends heavily on the application. Energy harvesters instead of battery become more attractive for recent applications, yet state-of-the-art energy harvesters, for example, sub-mm solar cells under moderate illumination can only provide up to 100μW power [Ingram11] for a wireless device. From the previous simulation shown in figure 1.4, considering the overall wireless system has an activity rate as low as one packet per second, the power consumption of WuRx needs to be less than 50μW so as to meet the total 100μW power budget.

2.1.3 Performance Metrics

Another important difference between a general purpose low power transceiver and a WuRx is the performance metrics. For a general purpose receiver, bit error rate (BER) performance is the most important as they are mainly used in data communications. However, BER is not a proper metric to measure the WuRx from its functional perspective. Instead, the performance metrics of interest are probability of miss detection and probability of false alarm. These two errors have strong relationship with the power dissipation. Miss detection means that the WuRx misses the current wake-up request and the transmitter must re-transmit the request which increases both the power and the system latency. False alarm means that the WuRx wakes up the main data receiver unnecessarily which also costs additional power consumption. Detailed analysis for the specification of miss detection rate and false alarm rate will be discussed in a later section.

2.1.4 Sensitivity

The sensitivity requirement is typically related to communication distance, transmitted power and antenna gain. As discussed previously, the WuRx and the main transceiver will share the same antenna and use the same transmitter. Besides, the WuRx should be able to communicate over the same distance as the main transceiver. Therefore, for WuRx design, it is desirable to achieve sensitivity comparable to that of the main data transceiver. Otherwise, it may either decrease the communication range which limits the applications or require an additional power amplifier at the transmitter side to increase the transmitted power which costs extra power consumption. In 802.15.4g protocol [IEEE10] it specifies the receiver sensitivity to be at least -90dBm, therefore in this research our target receiver sensitivity should be better than -90dBm.

From the above discussion, the overall WuRx specifications are summarized in table 2.1.

Table 2. 1 Specification of WuRx Prototype

Parameter	Specification
Architecture	Narrow Band
Carrier Frequency	915MHz
Modulation Scheme	FSK
Data Rate	50k
Sensitivity	-90dBm
Active Power Consumption	< 50μW

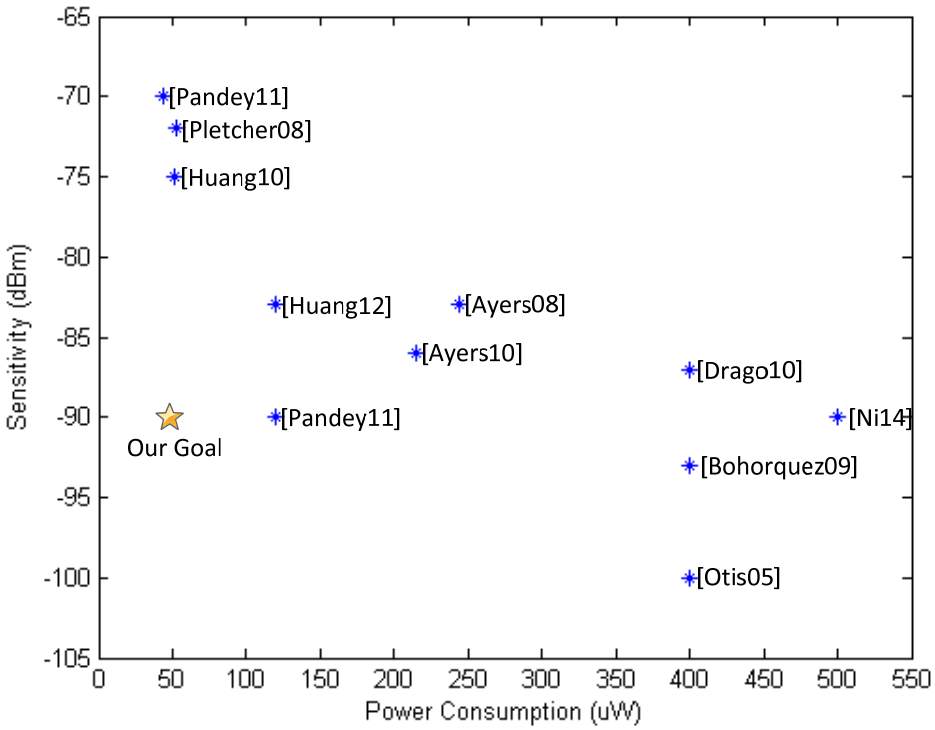

Figure 2.2 Performance of Recently Published Low Power Receivers

Figure 2.2 shows the performance comparison of previously published low power receivers. Although several implementations achieve high level of sensitivity, their power consumption is more than 2 to 10 times higher than the power budget for the WuRx. On the other hand, some implementations are able to consume within the power budget, yet their achievable sensitivity is more than 15dBm away from the sensitivity requirement for the WuRx. Obviously, the feasibility of implementing a high sensitivity receiver with less than 50μW of power consumption represents the most critical challenge for the WuRx design.

2.2 Proposed Two-Step WuRx

The most basic way to design a WuRx is to build a simple RF energy detector. However from reliability and power saving purpose, a more sophisticate practical implementation should be considered. Figure 2.3 shows an example wake-up scheme with only simple energy detection. In this example, the sender wants to communicate with device A. As A and B are neighboring devices, both WuRx A and WuRx B can detect energy from the wake-up frame transmitted by the sender and will wake up the data receiver of A and B simultaneously. This means that the data receiver B is unnecessarily activated which results in an additional energy waste. Therefore to avoid false alarms triggered by regular

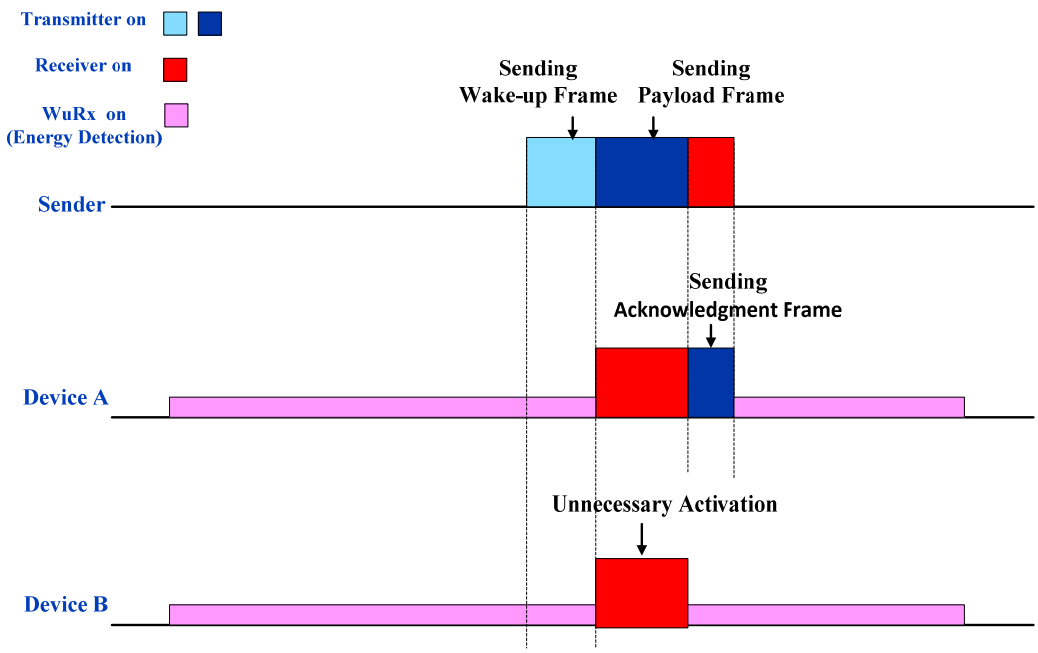

Figure 2.3 Wake-up Scheme with Simple Energy Detection

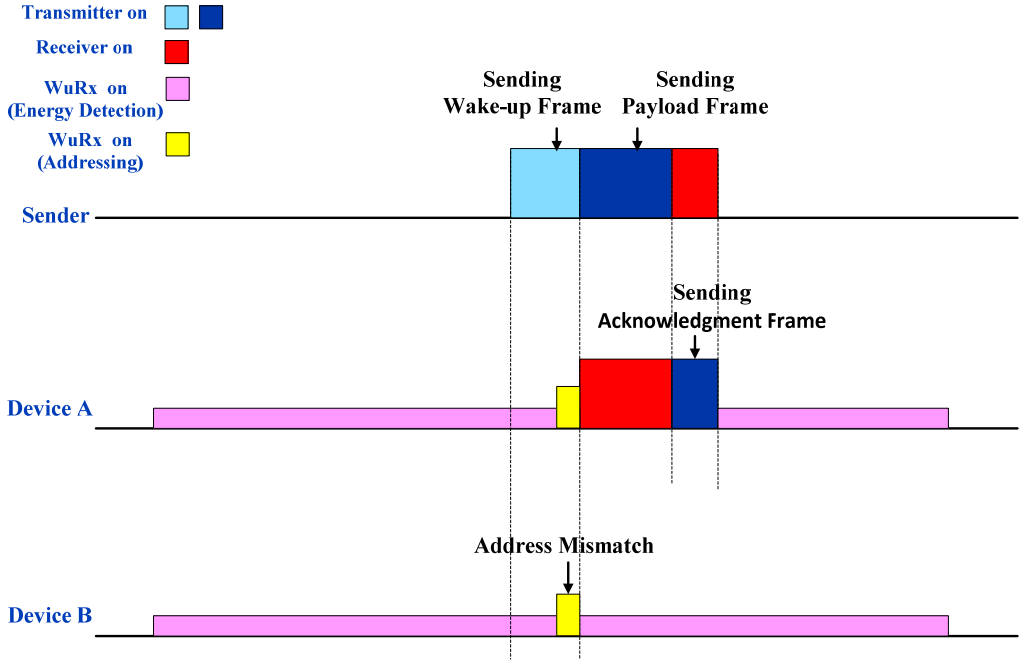

Figure 2.4 Wake-up Scheme with Proposed Two-Step WuRx

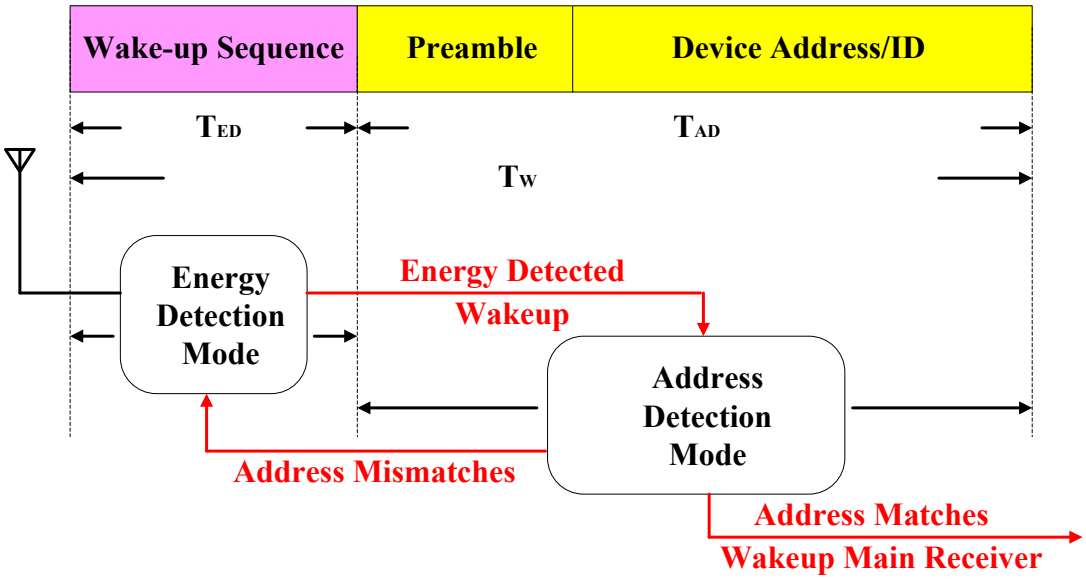

Figure 2.5 Wake-up Frame for Proposed Two-Step WuRx

data communication between neighboring devices, the WuRx design should contain the functionality of selective wake-up among different devices which means unique device ID/address detection should be included. Upon this principle, we propose a two-step WuRx architecture. The wake-up strategy and corresponding wake-up frame design is shown in figure 2.4 and figure 2.5. The WuRx has two operation modes: energy detection mode and address detection mode. Most of time, it is in energy detection mode monitoring whether there is communication energy in the channel. After it detects energy, it switches to address detection mode checking whether the address required in the wake-up frame matches the device address. If matches, it will wake up the main data receiver for data communication, otherwise it switches back to energy detection mode for channel monitoring. Obviously, due to the function complexity, the power dissipation in energy detection mode is smaller than in address detection mode. According to some previous literature, an RF energy detector dissipates tens of microwatts [Pletcher07], while an FSK demodulator dissipates hundreds of microwatts [Lont12]. Yet both of them consume much less power than the main data receiver whose typical power consumption is a few milliwatts. Therefore, by using the two-step wake up strategy, the unnecessary wake-up of main data receiver due to the communication initiated by neighboring devices has been avoided. Commands destination checking has been released from main data receiver to the WuRx which results in a huge amount of power saving. The average power consumption of the proposed WuRx is mainly dominated by the power dissipated in energy detection mode, yet it is also related to the power consumption of address detection mode and probabilities of error rates. Detailed analysis will be described in next section.

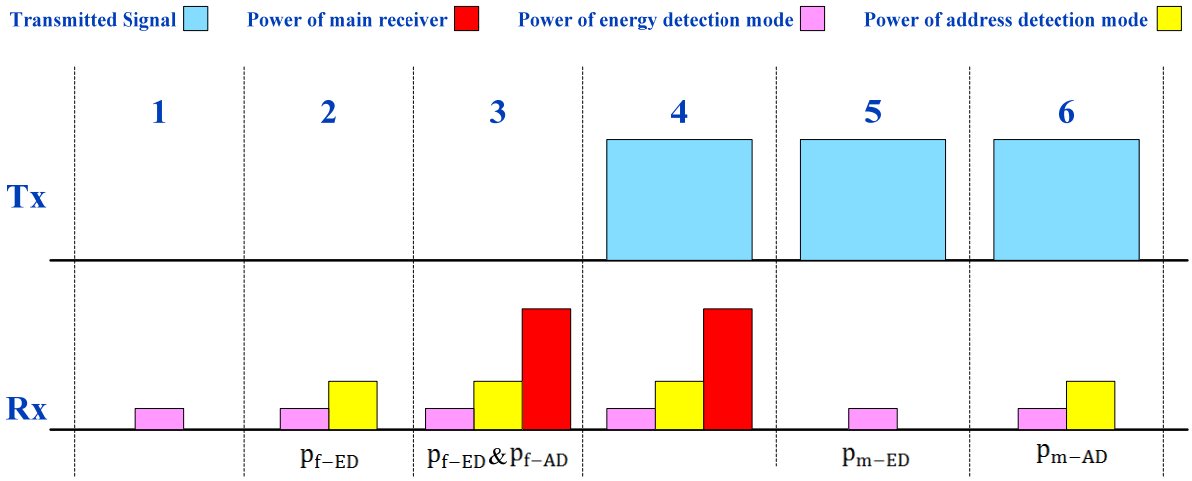

Figure 2.6 Six Different Working Categories for WuRx

2.3 Design Metrics

As mentioned in chapter 1, there are two major design metrics when comparing the WuRx aided wireless system with the traditional protocol-based duty-cycling system: average power consumption and average latency. These two metrics are not only related to the power consumption in different modes and the length of wake-up frame, but also related to the probabilities of errors. Before going through details of the design metrics, we first list the main notations that are used in the analysis.

- P_{ED}: power consumption in energy detection mode
- p_{f-ED}: probability of false alarm in energy detection mode
- p_{m-ED}: probability of miss detection in energy detection mode
- T_{ED}: total time in energy detection mode
- P_{AD}: power consumption in address detection mode
- p_{f-AD}: probability of false alarm in address detection mode
- p_{m-AD}: probability of miss detection in address detection mode
- T_{AD}: total time in address detection mode
- P_{MAIN}: power consumption of main data receiver
- α : receiver wake-up activity rate.
- T_W: total time of the wake-up frame

As shown in the figure 2.6, the working scheme of a WuRx can be divided into six categories. 1, 2, 3 refer to the scenario where no data communication exists in the channel. 1 is the normal operation. 2 stands for false alarm in energy detection mode which costs extra power for waking up address detection mode. 3 represents false alarm in both modes which triggers an unnecessary wake up of the main data receiver. 4, 5, 6 refer to the scenario where a wake-up frame is sent by the transmitter. 4 is the normal operation. 5 indicates miss detection in energy detection mode and the transmitter needs to resent the wake-up frame which costs additional latency. 6 means miss detection in address detection mode which results in not only additional latency but also additional power dissipation to operate in address detection mode once more. Combining all six of the above categories together, the average power consumption and the average latency of the WuRx can be derived as

$$\begin{aligned}\text{Power} &= P_{ED} + (1-\alpha)(P_{AD}\cdot p_{f-ED} + P_{MAIN}\cdot p_{f-ED}\cdot p_{f-AD}) \\ &\quad +\alpha\cdot P_{AD}(1 + p_{m-AD} + {p_{m-AD}}^2 + {p_{m-AD}}^3 \dots\dots) \\ &= P_{ED} + (1-\alpha)(P_{AD}\cdot p_{f-ED} + P_{MAIN}\cdot p_{f-ED}\cdot p_{f-AD}) + \frac{\alpha\cdot P_{AD}}{1-p_{m-AD}} \qquad (2.1)\end{aligned}$$

$$\begin{aligned}\text{Latency} &= T_W(1-p_{m-ED})(1-p_{m-AD})\times \\ &\quad (1 + 2p_{m-ED} + 2p_{m-AD} + 3({p_{m-ED}}^2 + p_{m-ED}\cdot p_{m-ED} + {p_{m-AD}}^2) \\ &= \frac{T_W(1-p_{m-ED}\cdot p_{m-AD})}{(1-p_{m-ED})(1-p_{m-AD})} \qquad (2.2)\end{aligned}$$

From (2.1) and (2.2), one can figure out that both the average power consumption and the average latency are proportional to the probability of error rates. The higher the error rates, the larger the power dissipation and latency are. As the wake-up activity α is low, the power consumption is mainly dominated by false alarm errors while the latency is determined by miss detection errors. Therefore, to satisfy the desired power budget and meanwhile to keep the latency bounded, it is important to set the specification of false alarm rate and miss detection rates in both operation modes.

In address detection mode, the WuRx performs as an ultra-low power FSK receiver. It should be able to correctly demodulate N bits in a wake-up frame used for address/ID matching. In this prototype, N is designed to be 50bits with 16bits of preamble for data synchronization purpose, 32 bits representing device unique address and 2 bits indicating the end of the wake-up frame. As the required FSK data rate (f_{data}) is 50kbps, the total time spent on address detection mode is

$$T_{AD} = N\times\frac{1}{f_{data}} = 1\text{ms} \qquad (2.3)$$

Its probability of false alarm and miss detection are related to the number of bits (N) and its bit error rate (BER).

$$p_{f-AD} = BER_{AD}{}^{N} \tag{2.4}$$

$$p_{m-AD} = 1 - (1 - BER_{AD})^{N} \approx N \cdot BER_{AD} \tag{2.5}$$

Considering a typical BER requirement for wireless receiver as 10^{-3},

$$p_{f-AD} = (10^{-3})^{50} = 10^{-150} \tag{2.6}$$

$$p_{m-AD} \approx 50 \times 10^{-3} = 0.02 \tag{2.7}$$

Obviously, p_{f-AD} is such a small number that it can be neglected. Therefore, the average power consumption of the WuRx heavily depends on the performance of energy detection mode, not only on its power dissipation but also on its probability of false alarm. Figure 2.7 and 2.8 plots the power and the latency performance based on probability of errors. We assume 45uW for energy detection mode, 400uW for address detection mode and 30mW for main receiver. It can be clearly seen from the graph that when p_{f-ED} becomes smaller, the average power consumption is dominated by the power dissipation in energy detection mode and would not be further reduced by decreasing p_{f-ED}. Therefore it is unnecessary to require a low p_{f-ED}. Rather 10^{-2} roughly the corner probability of the graph is a reasonable requirement for our prototype design to satisfy 50μW power budget. Similarly, p_{m-ED} also targets for 10^{-2}, which results in extra 4% average latency. For T_{ED} requirement, it is at least 1 bit long (20us) for energy detection as the transmitter can only send out data based on a fixed data rate. Yet analysis in chapter 3 will prove that T_{ED} has a strong relationship with the achievable sensitivity. The longer the T_{ED}, the higher the sensitivity that can be achieved. Therefore, considering a reasonable overhead to the whole wake –up frame, $T_{ED}$is designed to be 1/10 of T_{AD} which is about 5 bits length (100us).

Based on the previous discussion of design metrics, table 2.2 summarizes the specification of WuRx in different modes.

Table 2. 2 Specification of Proposed WuRx in Different Modes

Modes	Energy Detection Mode	Address Detection Mode
Power	< 45μW	< 400μW
Frame Length	< 5bits (100us)	50bits (1ms)
Probability of False Alarm	10^{-2}	10^{-150}
Probability of Miss Detection	10^{-2}	0.02
BER	N/A	10^{-3}

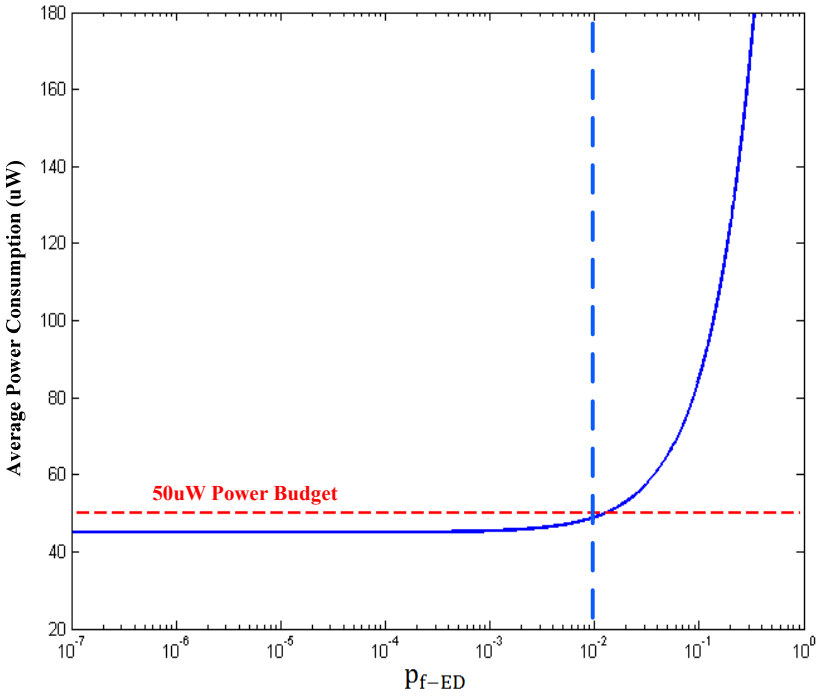

Figure 2.7 Six Different Working Categories for WuRx

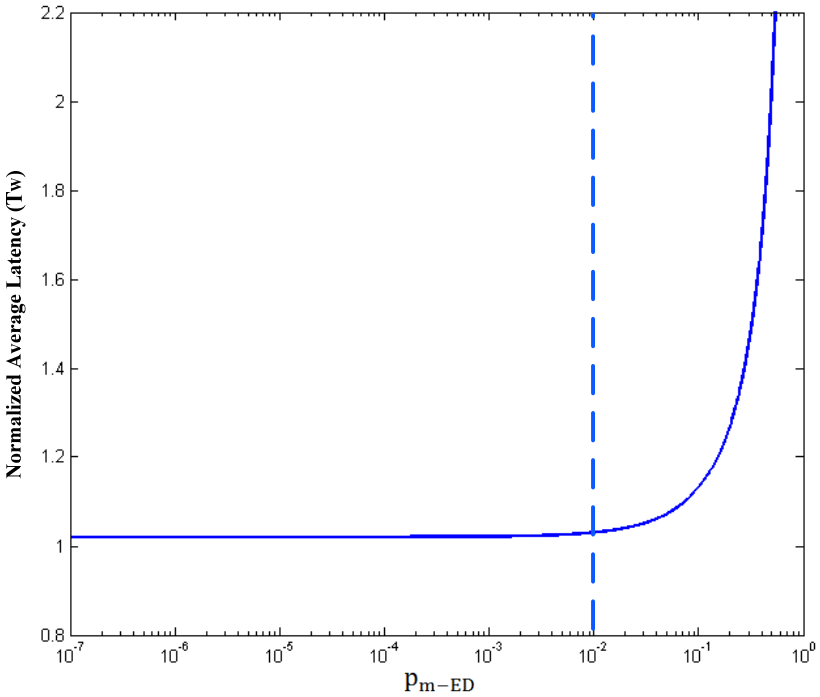

Figure 2.8 Six Different Working Categories for WuRx

2.4 Summary

This chapter presents a system level design for the wake-up receiver. It has proposed a two-step wake-up architecture to avoid the unnecessary activation of main data receiver to achieve an ultra-low power budget. It also provides design metrics in terms of power and latency performance optimization. Based on that, wake-up receiver specifications have been discussed in details for both working modes which can be served as a guideline for circuit designs in later chapters.

Chapter 3

Receiver for Energy Detection Mode

3.1 Architecture Development

As described in Chapter 2, in energy detection mode, the main function of receiver is to perform a simple energy detection of the input RF signal. The major performance specification of the receiver remains to be ultra-low power consumption (45μW) and high sensitivity (-90dBm). There are a wide variety of ways to implement the energy detection receiver ranging from simple passive rectifier to complex super-heterodyne receiver. Before developing a suitable architecture, it is worth to make a performance comparison among different receiver architectures in terms of power consumption and sensitivity.

3.1.1 Passive Rectifier

The passive rectifier is a typical circuit used in AC to DC conversion and is able to derive power from the incoming RF waveform. This performs exactly the desired functionality of the receiver in energy detection mode. Therefore, passive rectifier based receiver is the simplest and lowest power architecture. As shown in figure 3.1, the input RF signal passes through the frontend filter and the rectifier and is then compared with a given threshold to decide whether there is enough energy received in the channel. Since frontend filter and rectifier do not consume power and comparator operates at really low frequency, the power consumption of rectifier based receiver is extremely low, typically less than 1μW. However due to the nature of rectifier, the sensitivity of this receiver is very poor. [Roberts12] reports a 98nW wake-up receiver with only -41dBm sensitivity. In [Oh13], the authors add a 31-bit correlator after comparator for better interference rejection and sensitivity boosting. With 116nW power consumption, it is able to achieve -45dBm sensitivity. Although the active power consumption of the passive rectifier based receiver is well below our power budget, its achievable RF sensitivity is far away from the

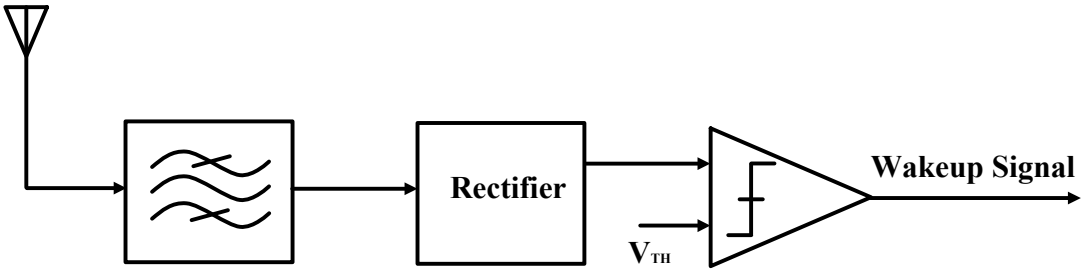

Figure 3.1 Passive Rectifier Based Receiver

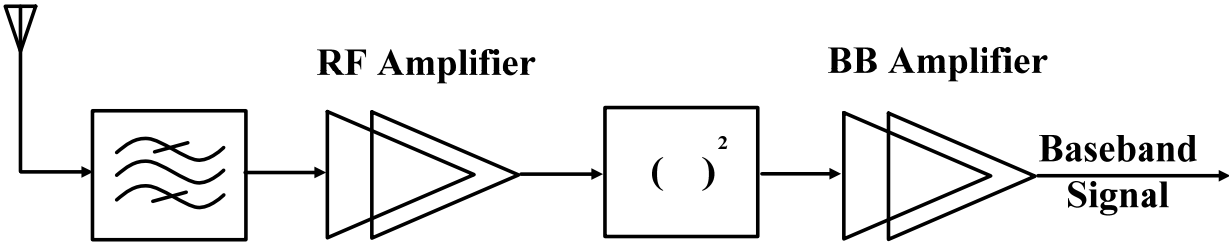

Figure 3.2 Tuned Radio Frequency (TRF) Receiver

desired specification. This architecture is not suitable to build the receiver for energy detection mode.

3.1.2 Tuned Radio Frequency (TRF) Receiver

The tuned radio frequency (TRF) receiver is another type of simple receiver which was invented and commonly used in the early nineteen century. As shown in figure 3.2, it is implemented with a frontend filter, RF amplification stages, a nonlinear envelop detector and baseband amplifiers. As implied by the name, the envelope detection process discards all frequency and phase content of the input signal and simply detects the amplitude of the RF carrier which implies the energy of the RF input. The TRF receiver is actually an enhanced version of the passive rectifier based receiver which is shown earlier to have poor sensitivity. It includes high frequency gain stages which are expensive from power perspective to improve the receiver sensitivity, thus it suffers from the tradeoff between power consumption and sensitivity performance. In [Pletcher08], the author proves that within a certain power budget, it is beneficial to increase gain in the front-end of a TRF receiver to achieve better sensitivity, even if the increase in gain results in degraded front-end noise performance. With this principle, the author builds a receiver with 65μW power consumption, 75% of which is spent on RF amplification and achieves a sensitivity of -

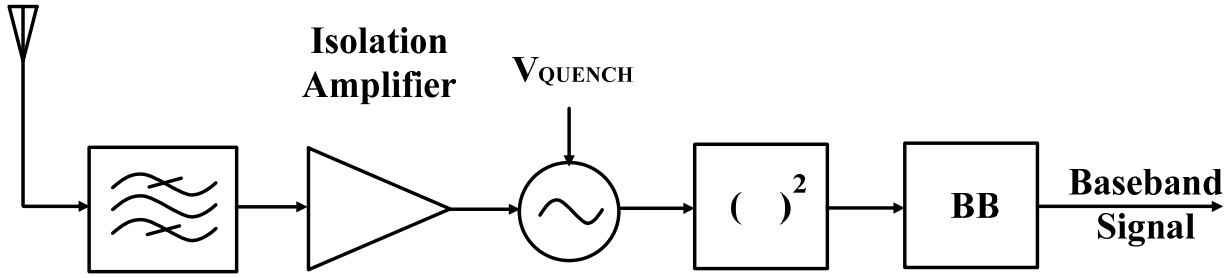

Figure 3. 3 Super-Regenerative Receiver

50dBm. Some following up researches have tried different techniques to improve the sensitivity without increasing the power consumption of RF amplification. [Huang10] has adopted double sampling technique applied to the down-converting envelope detector to suppress the offset and 1/f noise, although it means that the receiver is sensitive to the RF signal only half of the time. By flattening out the output noise floor, the receiver is able to achieve an improved sensitivity of -75dBm with 51μW power consumption, 58% of which is burnt on RF amplifiers. [Cheng12] implements a ΣΔADC after the baseband amplifier. This first-order low-pass ΣΔADC oversamples the wake-up request to enhance SNR and lessen the false detection, thus the receiver is able to achieve a sensitivity of -65dBm. Although all different techniques have been tried, yet limited sensitivity can be improved for a TRF receiver. The fundamental problem to use TRF architecture lies in providing sufficient gain at RF requires large amount of power. It limits the achievable sensitivity of a TRF receiver within a certain budget of power consumption.

3.1.3 Super-Regenerative Receiver

One technique to enhance RF gain so as to improve sensitivity is the use of positive feedback, or regeneration, in the amplifier. This super-regenerative concept was first introduced by Armstrong in the 1920s and was used in the early days of wireless communication due to its ability to reach a high RF gain from active devices (vacuum electron tubes) and to operate at high RF frequencies above the f_T of RF devices [Whitehead50]. Figure 3.3 shows the typical architecture of a super-regenerative receiver. The frontend consists of a passive matching network, an isolation amplifier, a quenched oscillator, a RF envelop detector and a baseband demodulator. The oscillator is periodically turned on and off by a quenched signal. The start-up time of the oscillator is exponentially dependent upon the initial voltage of the oscillator tank and this dependency provides a large amount of gain achievable by a single stage. The resulting high RF gain in front of the envelope detector improves the receiver sensitivity substantially, to better than -99dBm

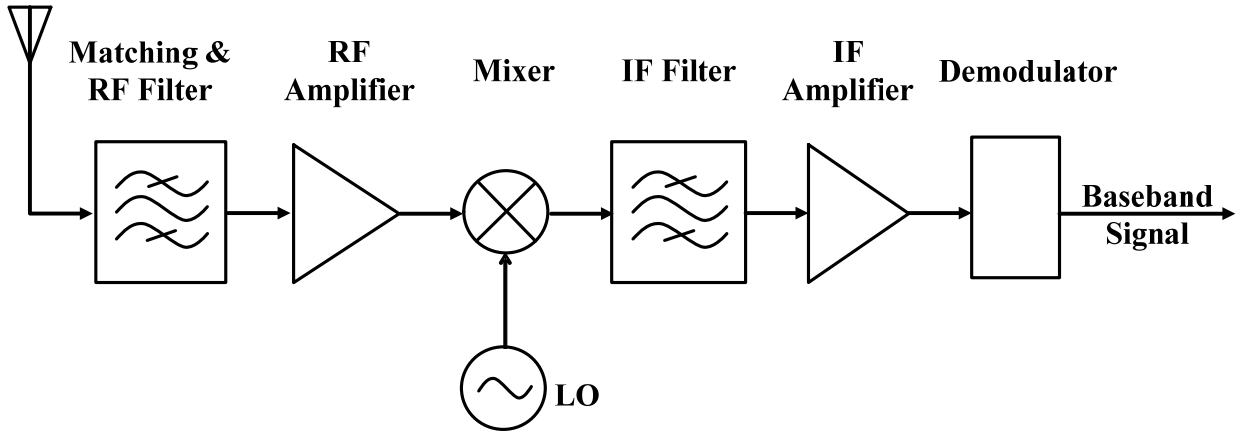

Figure 3.4 Single Conversion Superheterodyne Receiver

[Bohorquez09], [Otis05]. The super-regenerative receiver is fundamentally a TRF architecture using the quenched oscillator as a super-regenerative amplifier to achieve large RF gain and impressive performance. The drawback of this architecture is that a high accuracy local oscillator (LO) is now required. This stringent frequency accuracy typically requires a resonant LC oscillator, yet the limited quality factor (Q) of the integrated passive elements leads to a power floor of a few hundred microwatts. For example, in [Bohorquez09] the LC oscillator consumes 315μW which is more than 78% of the total receiver power. Thus for super-regenerative architecture, the high power consumption of accurate LO generation makes it difficult to meet the power budget of the wake-up receiver.

3.1.4 Superheterodyne Receiver

The superheterodyne receiver was first invented by Edwin Armstrong in 1918 during World War I. It is the most widely used architecture in nowadays wireless communication and almost all modern radio receivers use the superheterodyne principle. The basic idea of superheterodyne is to use frequency mixing to convert a received signal to an intermediate frequency (IF) which can be more conveniently processed than the original radio carrier frequency. At the cost of an extra frequency converter stage, the superheterodyne receiver provides superior selectivity and sensitivity compared with simpler designs described previously. Figure 3.4 shows an example of a single-conversion superheterodyne receiver design. The input RF signal passes through the matching network and is amplified by a low noise amplifier (LNA) so as to relax the noise requirement of the rest of the receiver chain. Then, the RF signal is down-converted to IF with a high-accuracy LO. The resulting IF signal is amplified and filtered to remove the image and interferers. Finally, the demodulator uses

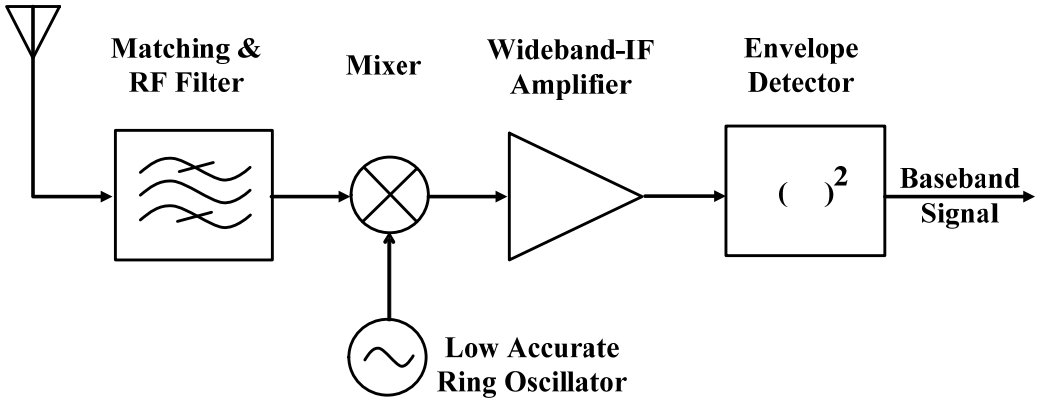

Figure 3. 5 Wideband-IF Receiver

the IF signal to recreate a copy of the original data information. In the superheterodyne architecture, an RF LO with high frequency accuracy and spectral purity is required to drive the mixer. Similar to previous super-regenerative receiver, it almost invariably requires an LC oscillator embedded in a phase-locked loop and it is difficult to design a low power LC oscillator with on-chip low Q integrated components. Thus, the power consumption of this architecture is often limited by the power consumption of the LO.

Recently researchers have adopted different techniques to reduce the power consumption of LO generation. One technique is to apply duty-cycling either on LO blocks or on the whole receiver. For example, in [Drago10] the author duty-cycles the digital control oscillator (DCO) based PLL (DCPLL) at 10% (turned on 100ns every 1us) and the DCPLL still draws an average current of 180uA from a 1.2V supply. In [Milosiu13], the whole receiver is duty-cycled heavily to as low as 0.8% (turned-on 4×250ns every 125us). In this way, the power consumption of the receiver is brought down to 217μW and can be reduced further with even more duty-cycling (e.g. 27μW with 0.1% duty-cycling). Duty-cycling helps to reduce the power of a receiver, yet it either requires a novel design of fast settling oscillator/amplifier so as to decrease the minimum turned-on time or suffers from a tradeoff between detection rate and average power consumption.

Another technique is to replace the LC oscillator with a CMOS ring oscillator whose power would be 20X smaller than its LC counterpart [Pletcher09]. The drawback of this replacement is that the frequency accuracy and phase noise of the ring oscillator is pretty poor, usually prohibit its use as the LO. Yet, in [Pletcher09], the author has overcome this fundamental disadvantage at the architectural level by proposing a superheterodyne receiver with wideband-IF as shown in figure 3.5. Due to the frequency inaccuracy of the ring oscillator, the RF input signal is converted down to a wideband IF instead of a fixed IF

and this wideband IF signal could be further converted to baseband by an envelope detector which is similarly used in a TRF receiver. Compared to a TRF receiver, this wideband-IF receiver utilizes a low quality ring oscillator to generate the LO so as to bring the gain amplification before the envelope detector from RF side to IF side which results in a major power saving. The proposed receiver is able to achieve a sensitivity of -72dBm with 52μW power consumption.

3.1.5 Proposed Architecture

From previous architecture reviewing, the TRF receiver and the superheterodyne receiver with wideband-IF could be two potential choices for designing a receiver for energy detection mode. Both of them eliminate the power hungry and high precision timing element which make it possible to bring the total power of receiver down within our tight budget, yet the published achievable sensitivity of these two type receivers is still far away from our target, with the best performance around -75dBm [Huang10]. For a TRF receiver, the bottleneck of performance improvement remains in the tradeoff between achievable sensitivity and expensive power spent on the front-end RF gain stages. For example, in [Huang14] the TRF receiver is able to reach a sensitivity of -61dBm with 64μW power consumption and can be improved to -86.5dBm with extra 82μW spent on the RF amplification. For a wideband-IF receiver, the dominant noise contribution comes from the noise folding from wideband IF to baseband when performing envelope detection [Pletcher09]. As the bandwidth of IF is several orders larger than that of baseband, by envelope detection, this wideband IF noise will be superposed on top of the baseband signal which largely degrades the achievable SNR at the receiver output. Therefore, to improve the sensitivity performance of a wideband-IF receiver, one need to find an effective way to eliminate the contribution from wideband IF noise.

True circuit noise is a random process following Gaussian distribution and is still a random process following a certain distribution after a square operation. If a random process is averaged for sufficient time, it converges to its mean value which can be estimated depending on its distribution. Based on this principle, we propose a receiver architecture for energy detection mode based on “wideband-IF” and “noise averaging”. Figure 3.6 shows the proposed receiver architecture and its frequency planning. The input RF signal first passes through a matching network which contains a FBAR resonator to simultaneously filter the input with a sharp band-pass response. With the MEMS resonator embedded, the frontend network provides a high selectivity and helps to eliminate interfering signals that lie close to the desired channel. Then the RF signal is down-converted to the wideband IF with a mixer and a low power ring oscillator which can be calibrated within 30MHz of the desired frequency. The resulting IF signal is amplified with gain blocks that cover the entire IF bandwidth (BW_{IF}) and is further down-converted to baseband through energy detection

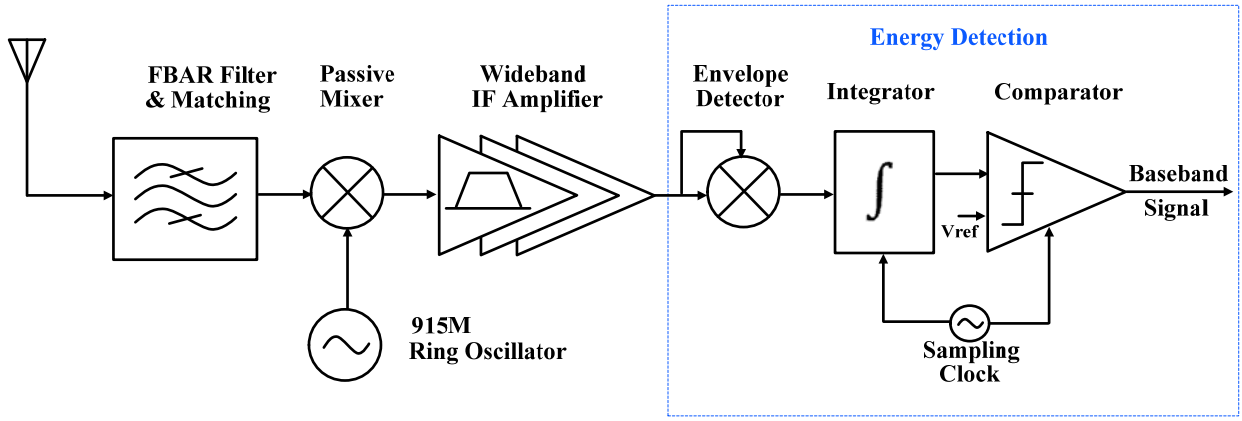

Figure 3.6 Proposed Receiver Architecture in Energy Detection Mode

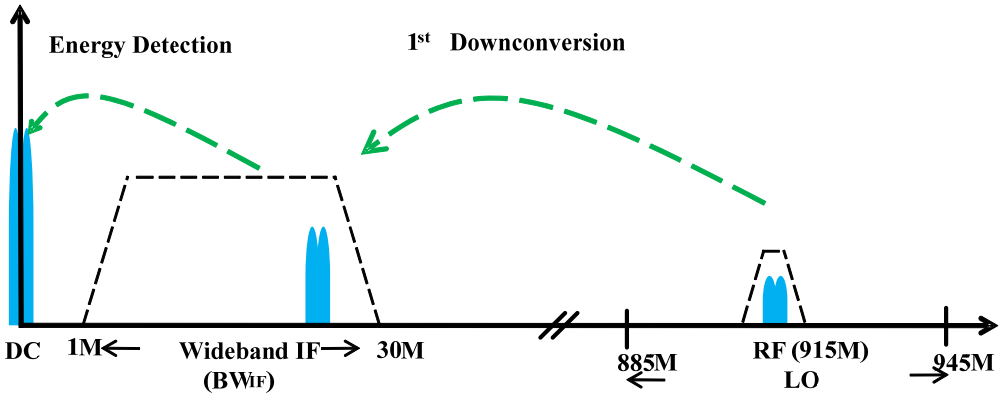

Figure 3.7 Frequency Planning for Receiver in Energy Detection Mode

which consists of a self-driven mixer (envelope detector), an integrator and a comparator. As the integrator performs averaging functionality, it also helps to shape the wideband noise to its mean value which can be effectively eliminated by turning the threshold at the comparator. The proposed receiver architecture adopts the "wideband-IF" concept to utilize a low power ring oscillator instead of a LC oscillator for LO generation which results in huge power saving to satisfy the power budget. Meanwhile, it also adopts the "noise averaging" concept to eliminate the effect of wideband noise caused by "wideband-IF" so as to improve the sensitivity to the desired number. Detailed sensitivity analysis is provided in next section.

3.2 Sensitivity Analysis

Traditionally, the sensitivity of a receiver is calculated as:

$$\text{Sens} = -174\text{dBm} + 10\log\text{BW} + \text{NF} + \text{SNR}_{\text{MIN}} \tag{3.1}$$

where SNR_{MIN} is the minimum required signal to noise ratio for a certain detection. Typically, energy detection performed by using envelope detector needs around 11 dB SNR_{MIN} for a decent error rate [Proakis01]. NF is the noise figure of the whole receiver which is typically proportional to the bias current and could not be easily reduced without increasing the power budget significantly. BW is the noise bandwidth in Hz, usually comparable to the bandwidth of baseband data. Yet, due to the nonlinear nature of the envelope detector, it is not straightforward to analyze the noise figure directly. Therefore we modify the sensitivity equation from (3.1) to

$$\text{Sens} = -174\text{dBm} + 10\log\text{BW}_{\text{IF}} + \text{NF}_{\text{FE}} + \text{SWNR}_{\text{MIN}} \tag{3.2}$$

where BW_{IF} is the noise bandwidth of wideband IF. NF_{FE} is the linear noise figure of the receiver frontend including matching network, mixer and IF gain stages. SWNR_{MIN} is the minimum required signal to wideband noise ratio needed for energy detection to achieve a certain error rate. In this calculation, the noise generated by energy detection circuitry itself is neglected as the frontend gain stages can easily achieve 60~70 dB of gain. This makes the noise contribution of energy detection a trivial factor of the total noise performance [Gambini08]. In this section, we will build a theoretical model for energy detection so as to analyze SWNR_{MIN} it needs to achieve a certain error rate. Then we use this SWNR_{MIN} together with NF_{FE} and BW_{IF} to calculate the sensitivity of receiver.

3.2.1 Theoretical Model for Energy Detection

Before calculate SWNR_{MIN}, we first list the main notations that are used to describe the theoretical model for energy detection shown in Figure 3.8.

- x(t): input waveform of energy detection
- y: integrator output
- s(t): IF signal waveform
- n(t): noise waveform which is modeled as zero-mean, white Gaussian random process with variance σ_N^2.
- B: noise bandwidth which is equal to BW_{IF}

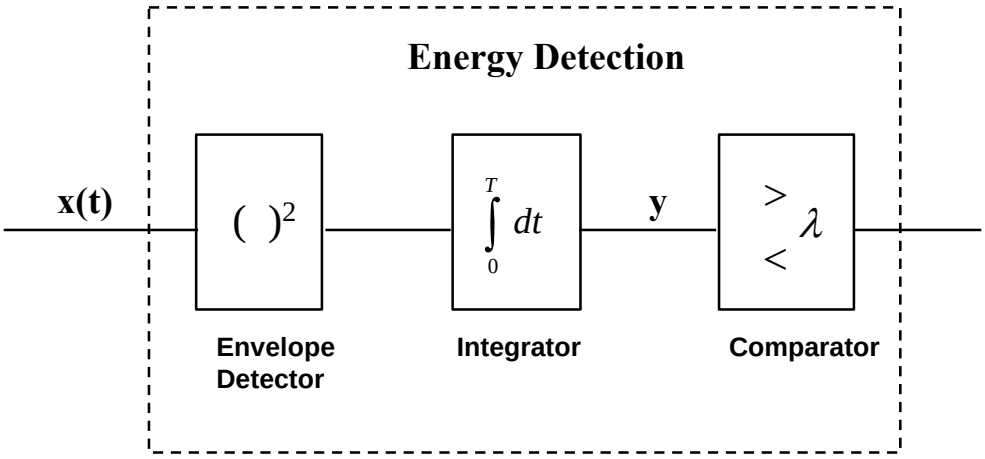

Figure 3. 8 Theoretical Model for Energy Detection

- N_0: noise power spectrum density
- SWNR: signal to wideband noise ratio at the input of energy detection
- T: integration time also the energy detection latency.
- λ: energy threshold used by comparator
- H_0: hypothesis corresponding to no signal transmitted.
- H_1: hypothesis corresponding to signal transmitted.
- Pf: probability of false alarm
- Pm: probability of miss detection
- Fn(x): cdf of normalized chi-squared distribution with n degree of freedom
- Fn,s(x): cdf of non-central chi-squared distribution with n degree of freedom and a non-central parameter of s.

The input signal of energy detection takes the form

$$x(t) = h \times s(t) + n(t) \qquad (3.4)$$

where h = 0 or 1 under hypotheses H_0 or H_1 respectively. The output of the integrator y_0 and y_1 will act as the test statistic to test the two hypotheses H_0 or H_1 respectively.

Let us first start with hypotheses H_0 when there is no signal transmitted

$$x_0(t) = n(t) \tag{3.4}$$

$$y_0 = \int_0^T x_0^2(t)dt = \int_0^T n^2(t)dt \tag{3.5}$$

As the noise signal has bandwidth B, according to the sampling theorem [Shannon49], it can be expressed as

$$n(t) = \sum_{i=-\infty}^{\infty} a_i \text{sinc}(2Bt - i) \tag{3.6}$$

where

$$\text{sinc} = \frac{\sin(\pi x)}{\pi x}, a_i = n\left(\frac{i}{2B}\right)$$

Clearly, each a_i is the sample of zero-mean white Gaussian random process n(t), so it is a Gaussian random variable with zero mean and with the same variance σ_N^2, which is the variance of n(t).

$$\sigma_N^2 = N_0 B \tag{3.7}$$

$$a_i \sim N(0, N_0 B) \tag{3.8}$$

$$\frac{a_i}{\sqrt{N_0 B}} \sim N(0,1) \tag{3.9}$$

Using the fact that

$$\int_{-\infty}^{\infty} \text{sinc}(2Bt - i)\text{sinc}(2Bt - j)dt = \begin{cases} \frac{1}{2B} & (i = j) \\ 0 & (i \neq j) \end{cases} \tag{3.10}$$

We may write

$$\int_{-\infty}^{\infty} n^2(t)dt = \frac{1}{2B} \sum_{i=-\infty}^{\infty} a_i^2 \tag{3.11}$$

[Urkowitz67] has proved that if 1/T is small enough compared to B, on the interval (0, T), signal can be approximated by a finite sum of 2BT. This assumption is exactly true for our energy detection, since the noise bandwidth B is much larger than the desired data bandwidth 1/T. It also means the integration time T needs to be long enough to make the assumption work. Therefore

$$y_0 = \int_0^T n^2(t)dt = \frac{1}{2B}\sum_{i=0}^{2BT} a_i^2 \tag{3.12}$$

According to (3.9) and (3.12), the test statistic y_0 can be rewritten as

$$\frac{2y_0}{N_0} = \sum_{i=i}^{2BT}\left(\frac{a_i}{\sqrt{N_0 B}}\right)^2 \tag{3.13}$$

$\frac{2y_0}{N_0}$ is a sum of the squares of 2BT Gaussian variables with zero mean and unit variance, thus following central chi-squared distribution with 2BT degree of freedom.

Next, let us focus on with hypotheses H_1 when there is signal present.

$$x_1(t) = s(t) + n(t) \tag{3.14}$$

$$y_1 = \int_0^T x_1^2(t)dt = \int_0^T (s(t) + n(t))^2 dt \tag{3.15}$$

As signal bandwidth is much smaller than noise bandwidth, according to the sampling theorem [Shannon49], the signal can be expressed as

$$s(t) = \sum_{i=-\infty}^{\infty} b_i \mathrm{sinc}(2Bt - i) \tag{3.16}$$

$$x_1(t) = \sum_{i=-\infty}^{\infty} (a_i + b_i)\mathrm{sinc}(2Bt - i) \tag{3.17}$$

where

$$\mathrm{sinc} = \frac{\sin(\pi x)}{\pi x}, b_i = s\left(\frac{i}{2B}\right)$$

By using the fact (3.10)

$$\int_{-\infty}^{\infty} s^2(t)dt = \frac{1}{2B}\sum_{i=-\infty}^{\infty} b_i^2 \tag{3.18}$$

$$\int_{-\infty}^{\infty} x_1^2(t)dt = \frac{1}{2B}\sum_{i=-\infty}^{\infty} (a_i + b_i)^2 \tag{3.19}$$

Similarly, on the interval (0, T), signal can be approximated by a finite sum of 2BT.

$$\int_{0}^{T} s^2(t)dt = \frac{1}{2B}\sum_{i=0}^{2BT} b_i^2 \tag{3.20}$$

$$y_1 = \int_{0}^{T} x_1^2(t)dt = \frac{1}{2B}\sum_{i=0}^{2BT} (a_i + b_i)^2 \tag{3.21}$$

According to (3.9), (3.20) and (3.21), the test statistic y_1 can be rewritten as

$$\frac{2y_1}{N_0} = \sum_{i=i}^{2BT}\left(\frac{a_i + b_i}{\sqrt{N_0 B}}\right)^2 \tag{3.22}$$

$$\sum_{i=i}^{2BT}\left(\frac{b_i}{\sqrt{N_0 B}}\right)^2 = \frac{2BT \cdot \frac{1}{T}\int_0^T s^2(t)dt}{N_0 B} = 2BT \cdot SWNR \tag{3.23}$$

Similar to $\frac{2y_0}{N_0}$, $\frac{2y_1}{N_0}$ follows non-central chi-squared distribution with 2BT degree of freedom and a non-central parameter of $2BT \cdot SWNR$.

The probability of miss detection (P_m) and false alarm (P_f) can be generated by

$$P_m = P(y < \lambda | H_1) = P\left(\frac{2y_1}{N_0} < \frac{2\lambda}{N_0}\right) \tag{3.24}$$

$$P_f = P(y > \lambda | H_0) = P\left(\frac{2y_0}{N_0} > \frac{2\lambda}{N_0}\right) \tag{3.25}$$

where λ is the decision threshold and it is reasonable to assume that λ is proportional to noise power BN_0 and integration time T

$$\lambda = \beta \cdot BN_0 \cdot T \tag{3.26}$$

where β is the normalized factor. Using (3.13), (3.22) and (3.26) to evaluate (3.24) and (3.25) yields

$$P_m = F_{2BT,2BT\cdot SWNR}(2BT \cdot \beta) \tag{3.27}$$

$$P_f = 1 - F_{2BT}(2BT \cdot \beta) \tag{3.28}$$

From the above analysis, we can figure out that the probability of miss detection (P_m) of the proposed energy detection is related to the cumulative distribution function (cdf) of non-central chi-squared distribution while the probability of false alarm (P_f) is related to the cdf of chi-squared distribution. They are determined by four parameters: 1) Decision threshold (β) 2) Noise bandwidth (B) 3) Integration time (T) 4) Signal to wideband noise ratio (SWNR). Noise bandwidth, integration time and decision threshold together determine the amount of noise reduction that can be achieved by "noise averaging" and the effect of each parameter will be explored further in the next section.

3.2.2 Simulation Result

Simulations based on (3.27) and (3.28) are done in matlab to verify the performance of the proposed energy detection. Effects of different design parameters - decision threshold β, noise bandwidth B and integration time T will be discussed respectively and an estimation of receiver sensitivity will also be provided.

Decision Threshold

Figure 3.9 plots the probability of detection errors (P_m and P_f) versus SWNR with fixed noise bandwidth, fixed integration time and various decision threshold. It can be clearly viewed from the figure that P_f is always flat with different SWNR as it is only related to hypothesis H_0 when there is no signal presented while P_m is effected by SWNR and could be improved with an increasing of SWNR. It is also obvious that when decision threshold is low, one can get better miss detection rate. On the contrast, when the decision threshold is high, one can achieve better false alarm rate. To take both P_m and P_f into account, we define energy detection error rate (DER) as

$$DER = \alpha \cdot P_m + (1 - \alpha) \cdot P_f \tag{3.29}$$

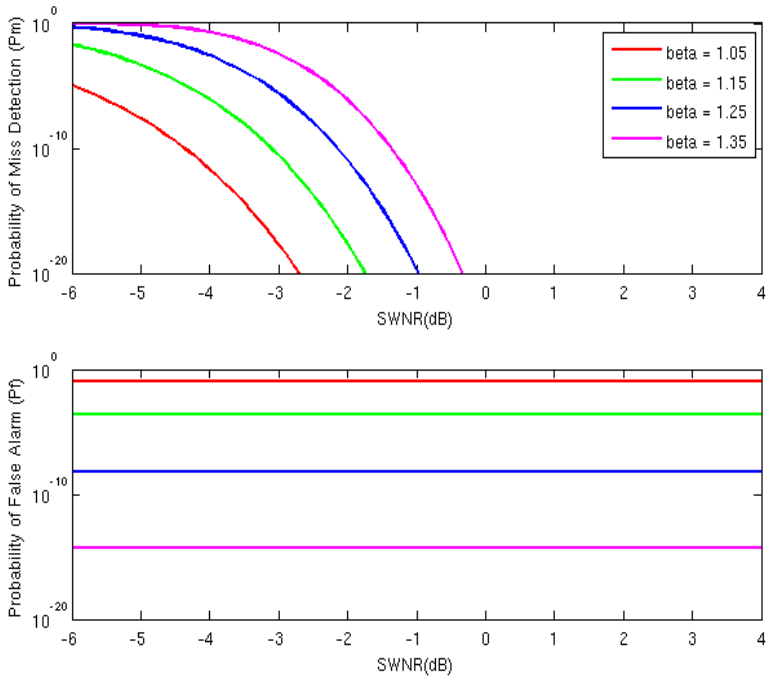

Figure 3.9 Probability of Miss Detection (P_m) and Probability of False Alarm (P_f) Vs SWNR for Various Threshold Factor β with 30MHz Noise Bandwidth and 10us Integration Time.

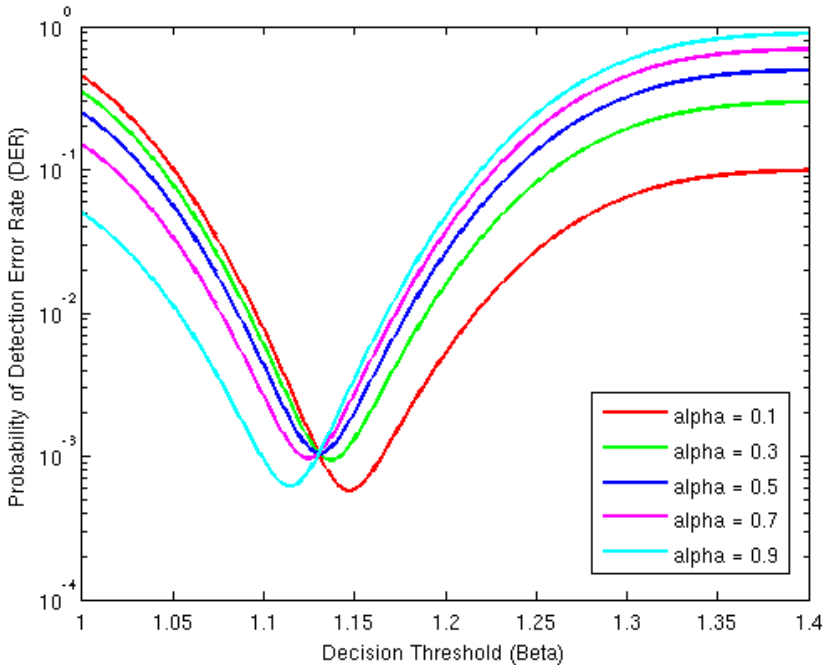

Figure 3.10 Detection Error Rate (DER) Vs Decision Threshold Factor β for Various Wake-up Activity Rate α with 30MHz noise bandwidth, 10us integration time and -5.5dB SWNR

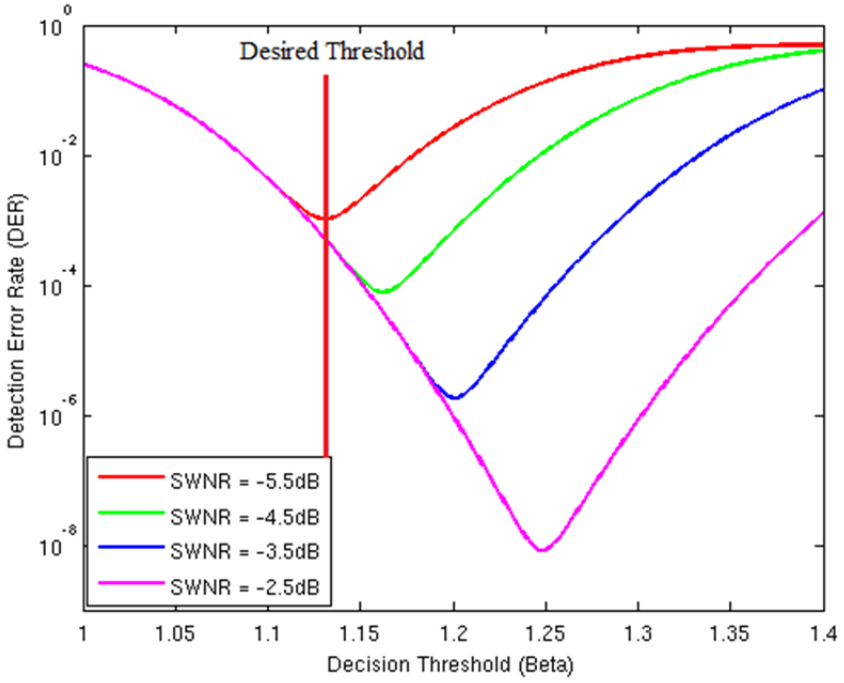

Figure 3.11 Detection Error Rate Vs Decision Threshold Factor β for Various SWNR with 30MHz noise bandwidth and 10us integration time

where α is receiver wake-up activity rate. As by varying decision threshold β, P_m and P_f are varied accordingly, the most effective way to achieve minimum DER is to set β at the point where $\alpha \cdot P_m$ and $(1 - \alpha) \cdot P_f$ equal to each other. Figure 3.10 plots detection error rate versus decision threshold with various wake-up activity rate, fixed noise bandwidth, fixed integration time and fixed SWNR. It shows that with different α one can always achieve an optimum DER by changing β and the worst optimum DER occurs at the point when α equals 0.5. Therefore in later simulations we only consider the worst case scenario when α equals 0.5. One thing to notice is that when α equals 0.5, DER has the same definition as bit error rate (BER) for OOK demodulation. Thus our energy detector could also be used as OOK demodulator for an ultra-low power receiver.

Figure 3.11 plots the detection error rate versus decision threshold for different SWNR with fixed noise bandwidth and fixed integration time. Obviously, for each SWNR, there always exists a different optimum β to achieve the minimum DER and when SWNR is increased, the optimum β shifts to a larger value which helps to reduce the probability of false alarm and yields a lower DER. In our design, for a desired setting of noise bandwidth and integration time, we only choose a fixed β located at the optimum point (as shown in the red straight line) where with $SWNR_{MIN}$, it can achieve a DER less than 10^{-3}. Thus for any SWNR larger than $SWNR_{MIN}$, a better DER can always be guaranteed.

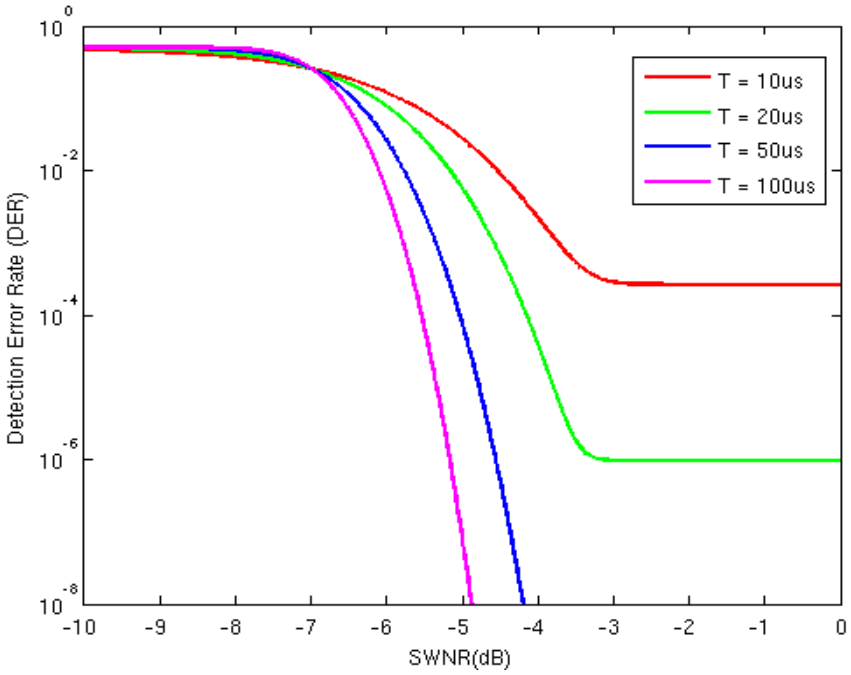

Figure 3.12 Detection Error Rate Vs SWNR for Various Integration Time with Fixed Decision Threshold Factor β = 1.2 and 30MHz noise bandwidth

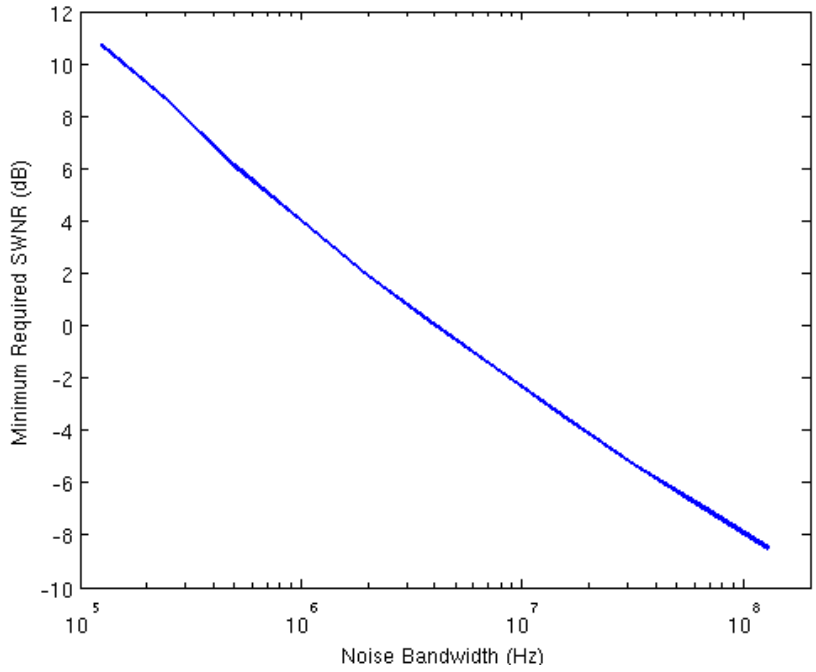

Figure 3.13 Minimum Required SWNR Vs Noise Bandwidth for 0.1% DER with 20us Integration Time and Optimum Decision Threshold

Integration Time

Figure 3.12 plots the detection error rate versus SWNR for different integration time with a fixed decision threshold. It demonstrates the effect of integration time that the system performance can always be improved by increasing the time of integration, yet this also leads to an increase in wake-up latency. For example, the minimum required SWNR for 10^{-3} DER can be reduced by more than 2dB when increasing integration time from 10us to 100us. This presents a tradeoff between achievable sensitivity and system latency. Another noticeable thing is that when SWNR increases to a certain level, DER saturates and could no longer be improved. This is because the decision threshold is fixed and the probability of false alarm starts to dominate DER with higher SWNR.

Noise Bandwidth

From the definition of P_m (3.27) and P_f (3.28), we can figure out that the noise bandwidth has the same effect as the integration time. This means that the larger the noise bandwidth, the lower the required $SWNR_{MIN}$ to achieve a certain DER as shown in figure 3.13. Yet this does not imply that by increasing the noise bandwidth a better sensitivity can be achieve as the sensitivity needs to take noise power into account. When the noise bandwidth is increased, although $SWNR_{MIN}$ is reduced, the noise power is increased much faster which leads to an even worse performance. Figure 3.13 actually demonstrates the effectiveness of wideband noise reduction by performing "noise averaging". For example, for 30MHz noise bandwidth, with 20us integration time, it only requires a SWNR of -4dB to achieve 0.1% DER. Compared with theoretical 11dB SNR for non-coherent energy detection [Proakis01], our proposed strategy helps to remove more than 15dB excess noise power, thus it improves the sensitivity performance substantially. However when noise bandwidth decreases, "noise averaging" becomes less effective in noise reduction because more portion of noise is correlated with desired signal and could not be removed by average function. Especially, when noise bandwidth is close to data bandwidth (1/T), $SWNR_{MIN}$ reaches its theoretical value and "noise averaging" is no longer useful.

Receiver Sensitivity

Combining (3.2), (3.27), (3.28) and previously discussed design parameter together, figure 3.14 shows the simulation result for receiver sensitivity versus noise bandwidth with an estimated 13dB frontend noise figure. Considering IF bandwidth of 30 MHz to provide an adequate level of precision for a low power ring oscillator, the receiver could achieve better than -91.2dBm sensitivity with 20us integration time (one bit period) and sensitivity could be improved to around -96dBm with 180us integration time (nine bits period). One could also reduce the noise bandwidth to get better performance, yet this requires a more precisely controlled ring oscillator that may lead to a high power budget. This result

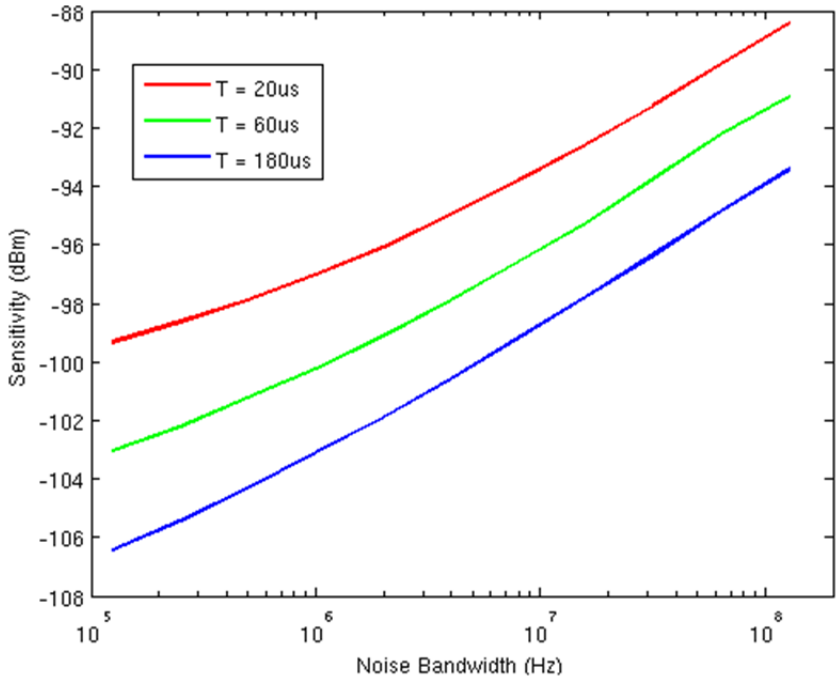

Figure 3.14 Receiver Sensitivity@ 0.1% DER Vs Noise Bandwidth for Various Integration Time

presents a tradeoff among achievable receiver sensitivity, latency (integration time) and power consumption.

3.2.3 Performance Boundary

It has been observed that by either increasing integration time T or decreasing noise bandwidth B, the sensitivity of the proposed energy detection receiver can be improved. In this section, we will prove this observation theoretically and quantify the performance improvement in terms of various design parameters.

Firstly, recall the definition of false alarm rate from (3.28), P_f is related to chi-squared distribution with n degree of freedom (χ_n^2) where n = 2BT. Let us define random variables Y_i which follows chi-squared distribution with one degree of freedom (χ_1^2)

$$Y_i \sim \chi_1^2 \qquad (i = 1, 2, \dots\dots, n) \tag{3.30}$$

$$\sum_{i=1}^{n} Y_i \sim \chi_n^2 \tag{3.31}$$

According to the central limit theorems [Billingsley95]

$$\sum_{i=1}^{n} Y_i \xrightarrow{d} N(n \cdot E(Y_i), n \cdot Var(Y_i)) \quad (n \to \infty) \tag{3.32}$$

where $N(\mu, \sigma^2)$ represents normal distribution, $E(Y_i)$ and $Var(Y_i)$ represent mean and variance of random variable Yi respectively. Using the fact that

$$E(\chi_1^2) = 1, \quad Var(\chi_1^2) = 2 \tag{3.33}$$

Yields

$$\chi_n^2 \xrightarrow{d} N(n, 2n) \quad (n \to \infty) \tag{3.34}$$

Therefore

$$P_f = 1 - F_{2BT}(2BT \cdot \beta) = Q\left(\frac{n \cdot \beta - n}{\sqrt{2n}}\right) \quad (n \to \infty) \tag{3.35}$$

where $Q(\cdot)$ is the Q function of standard normal distribution.

Next, recall the definition of miss detection rate from (3.27), P_m is related to non-central chi-squared distribution with n degree of freedom and a non-central parameter of s ($\chi_{n,s}^2$) where n = 2BT, s = 2BT·SWNR, similar to previous discussion

$$\chi_n^2 \xrightarrow{d} N(n + s, 2(n + 2s)) \quad (n \to \infty) \tag{3.36}$$

Therefore

$$P_m = F_{2BT,2BT\cdot SWNR}(2BT \cdot \beta) = Q\left(\frac{n(1 + SWNR - \beta)}{\sqrt{2n(1 + 2 \cdot SWNR)}}\right) \quad (n \to \infty) \tag{3.37}$$

Consider both of P_m and P_f smaller than 10^{-3} and use the fact that

$$Q(3.1) < 10^{-3} \tag{3.38}$$

Yields

$$\frac{n \cdot \beta - n}{\sqrt{2n}} > 3.1 \tag{3.39}$$

$$\frac{n(1+SWNR-\beta)}{\sqrt{2n(1+2\cdot SWNR)}} > 3.1 \tag{3.40}$$

Combining (3.39) and (3.40) together to cancel β

$$SWNR > \frac{6.2\sqrt{2n}+4\cdot(3.1)^2}{n} \approx \frac{6.2\sqrt{2}}{\sqrt{n}} \qquad (n = 2BT \rightarrow \infty) \tag{3.41}$$

Using sensitivity equation (3.2) and minimum SWNR (3.41)

$$Sens = -166dBm + NF_{FE} + 5\log(B) - 5\log(T) \tag{3.42}$$

(3.42) illustrates the relation among receiver sensitivity, frontend noise figure, noise bandwidth and integration time. With 13dB NF_{FE}, 30MHz noise bandwidth and 20us integration time, the receiver is estimated to achieve a sensitivity of -92dBm which is pretty close to the simulation results. The sensitivity can be further improved by 5dB when increasing integration time or decreasing noise bandwidth by 10 times and this leads to a tradeoff among achievable sensitivity, system latency and power consumption.

3.3 Circuit Design

This section presents the detailed design of receiver circuitry shown in figure 3.6. For power considerations, the entire receiver is optimized for sub-threshold operation from a single 0.5V supply.

3.3.1 Input Matching Network

The input matching network mainly serves two purposes. First, it must provide a stable impedance match to the 50 ohm input source within the operation frequency range. Second, the network should also provide a narrow RF filter to reject out-of-band noise and interfering signals. Instead of using on chip LC elements in matching network, in this research we take advantage of mature MEMS technology, utilizing the Film Bulk Acoustic Resonator (FBAR) manufactured by Avago Technologies. From a filtering perspective, the high quality factor of FBAR is attractive. Compared to the quality factor of an on-chip inductor, usually less than 20, the quality factor of FBAR resonator could be more than several thousand which makes the bandwidth of RF frontend filter only a few MHz. From a matching perspective, the matching network transforms the 50 ohm source impedance to the high parallel impedance of FBAR resonator which also serves as the input impedance of

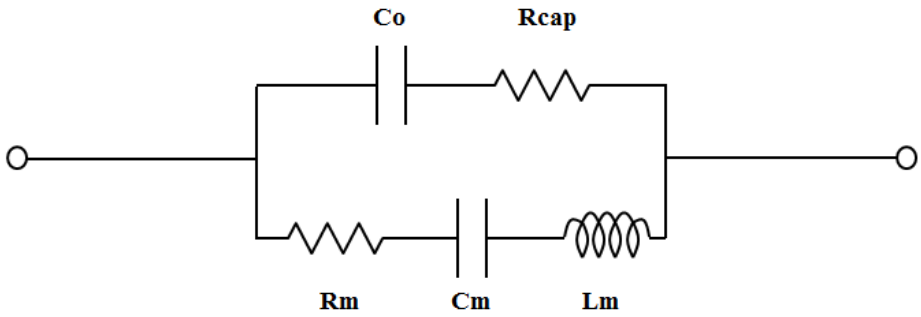

Figure 3.15 FBAR Resonator Circuit Equivalent Model

Table 3.1 Typical Parameter Values for a 920MHz FBAR Resonator

Model Parameter	Value
Rm	3 ohm
Lm	947.78nH
Cm	32.25fF
Co	1.98p
Rcap	0.8 ohm

the next stage. As noise figure of circuitry is typically reverse proportional to input impedance [Cook05], the high parallel impedance of FBAR resonator helps to reduce the required current consumption to achieve a certain noise performance.

3.3.1.1 FBAR Characteristics

Figure 3.15 depicts the circuit schematic equivalent model of a FBAR resonator. The model contains a series resonant branch including motional resistance Rm, inductance Lm and capacitance Cm and a large shunt capacitance Co. Table 3.1 gives some typical values for the model parameters. The example model parameters are for a 920MHz FBAR resonator. Figure 3.16 plots the impedance of the example resonator versus frequency. Though most of the frequency range, the response is determined by the response of shunt capacitor Co. However when frequency increases, the series resonance first occurs at a frequency fs which is determined by Lm and Cm and the impedance reaches its minimum value Zs. Soon after the series resonance, the series branch performs inductively and resonates with the shunt capacitor Co which provides the parallel resonance fp and impedance reaches its peak value Zp. If the resonator is used in series resonance as a short circuit, Co still allows signal to feed through away from resonance. For this reason, if only a single resonator is to be used, it is better to use the parallel resonant mode to build a filter. More detailed expressions for fs, fp, Zs, Zp are derived in following.

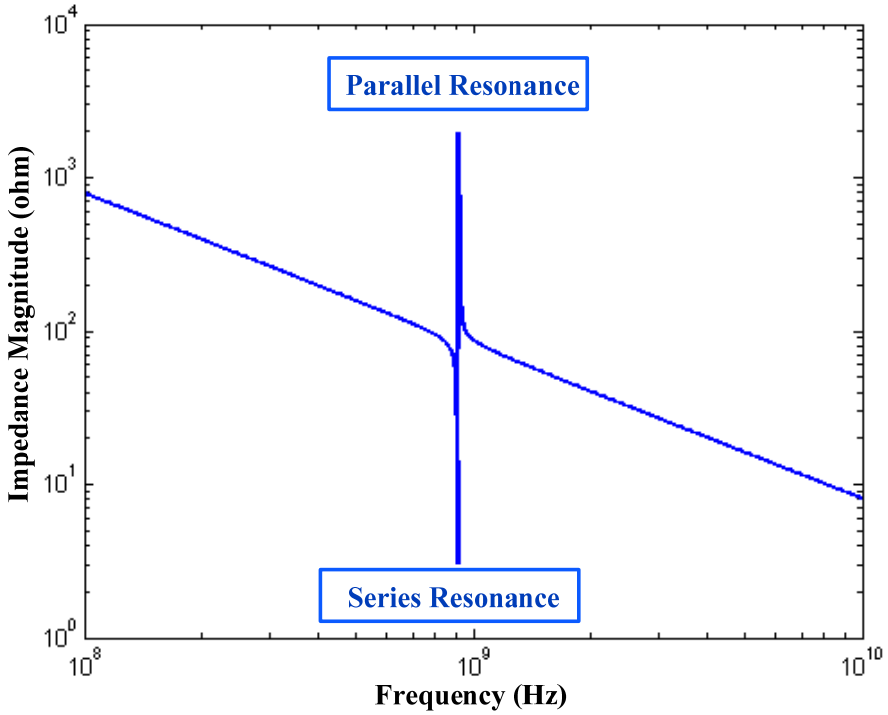

Figure 3.16 Impedance Response of a FBAR Resonator

Series Resonance:

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{3.43}$$

$$Q_s = \frac{\omega_s L_m}{R_m} \tag{3.44}$$

$$Z_s = R_m // \left(\frac{1}{sC_o} + R_{cap}\right) \approx R_m \tag{3.45}$$

Parallel Resonance:

$$f_p = \frac{1}{2\pi\sqrt{L_m\left(\frac{C_m C_o}{C_m + C_o}\right)}} = f_s\sqrt{1 + \frac{C_m}{C_o}} \tag{3.46}$$

Table 3.2 Performance Summary of a 920MHz FBAR Resonator

Model Parameter	Value
fs	910.3MHz
Qs	1807
Rs	~ 3 ohm
fp	917.68MHz
Qp	1438
Rp	~ 2019 ohm

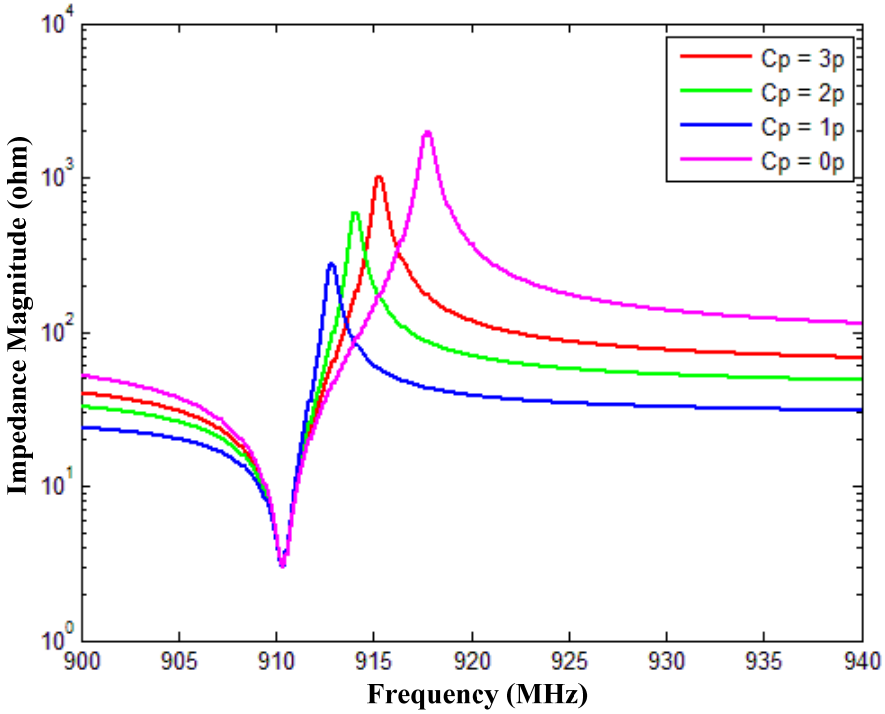

Figure 3.17 Impedance Response of FBAR resonator with Different Shunt Capacitance

$$Q_p = \frac{\omega_p L_m}{R_m + R_{cap}} \tag{3.47}$$

$$Z_p = \left(R_m + sL_m + \frac{1}{sC_m}\right) // \left(\frac{1}{sC_o} + R_{cap}\right) \approx \frac{1}{(\omega_p C_o)^2 (R_m + R_{cap})} \tag{3.48}$$

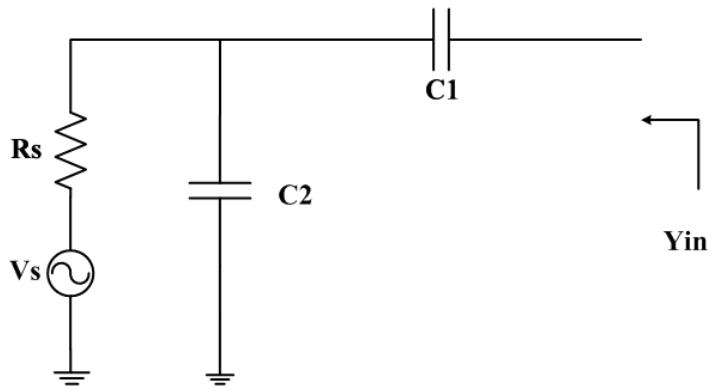

Figure 3.18 Schematic of Capacitive Transformer

Based on the (3.43) ~ (3.48), table 3.2 summarizes the performance of the example FBAR resonator. The above analysis also shows that varying the shunt capacitance Co has a large effect on the parallel resonance and parallel impedance of the resonator while leaves series resonance unchanged [Otis02]. This phenomenon is important as when integrating a FBAR resonator with an IC chip, the parasitic capacitance due to the extra circuitry or wiring parasitic is quite large and can be combined with Co. Figure 3.17 illustrates this effect by shunting the resonator with an additional parasitic capacitance Cp in parallel with Co, varying from 0p to 3p. It shows that Rp decreases quickly with an increase of Cp. Therefore, when the FBAR resonator is used in parallel resonant mode where high Rp is desirable, it is very critical to minimize the extra parasitic capacitance.

3.3.1.2 Capacitive Transformer

There are various ways to build matching network among which capacitive transformer seems attractive since the FBAR resonator itself already provides inductance to resonate with the capacitive network, no extra-large and lossy inductor is needed. Figure 3.18 shows the schematic of a capacitive transformer. From [Lee04], the admittance of network is derived as

$$Y_{in} = \frac{j\omega C_1 - \omega^2 R_s C_1 C_2}{j\omega R_s (C_1 + C_2) + 1} \tag{3.49}$$

With real part

$$G_{in} = \frac{\omega^2 R_s C_1^2}{\omega^2 R_s^2 (C_1 + C_2)^2 + 1} \tag{3.50}$$

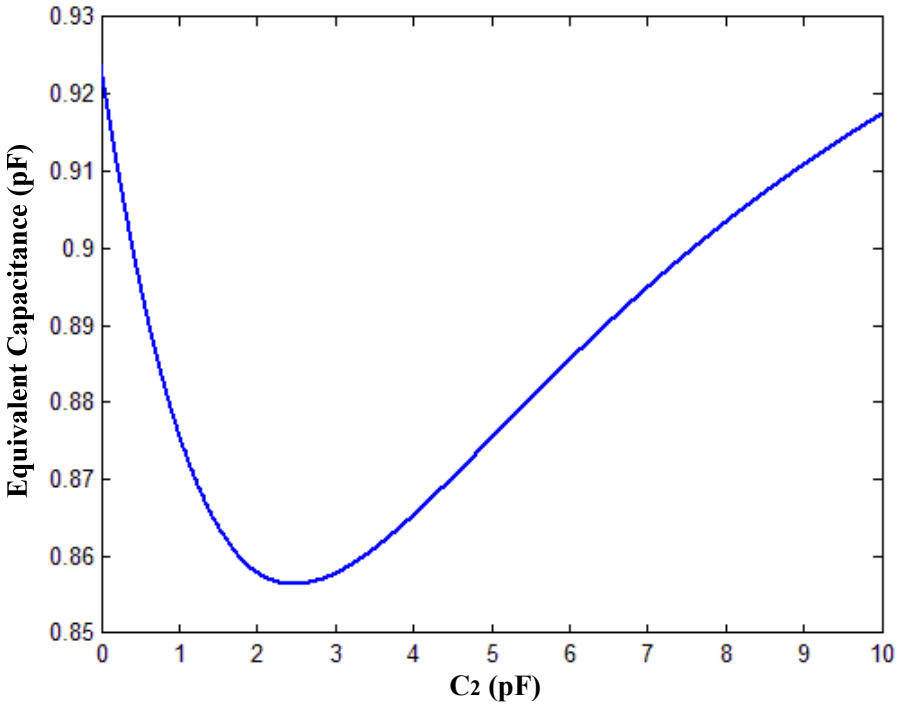

Figure 3.19 Equivalent Capacitance from Capacitive Transformer Network with C_1=1pF, f=915M

And imaginary part

$$B_{in} = \frac{\omega C_1 + \omega^3 R_s^2 C_1 C_2 (C_1 + C_2)}{\omega^2 R_s^2 (C_1 + C_2)^2 + 1} = \omega C_1 \left(\frac{\omega^2 R_s^2 C_2 (C_1 + C_2) + 1}{\omega^2 R_s^2 (C_1 + C_2)^2 + 1} \right) \tag{3.51}$$

For a given C_1 value, the imaginary part of the network admittance will have larger value if C_2 is zero or infinite, with somewhat smaller value at intermediate values of C_2. Figure 3.19 plots the equivalent capacitance from network admittance with fixed value of C_1 while C_2 varying from 0 to 10pF. Note that the maximum deviation is less than 7%. Therefore, the imaginary part of admittance is mainly dominated by value of C_1 which could be combined with FBAR shunt capacitance to determine parallel resonance. This is a major benefit for this network.

Figure 3.20 shows a complete schematic of input matching network. A more complex resonator model including parasitic effects is included. In the prototype, the FBAR chip is simply placed adjacent to the CMOS chip and wire-bonded directly to pads of the CMOS die. In this configuration, the pad capacitance C_{pad} is modeled as 100 fF and the wire bonds (L_{bond}) can be modeled with about 500 pH of inductance. The quality factor of these bonds is quite high due to the short length and low loss, so a Q of 30 is assumed for design. The

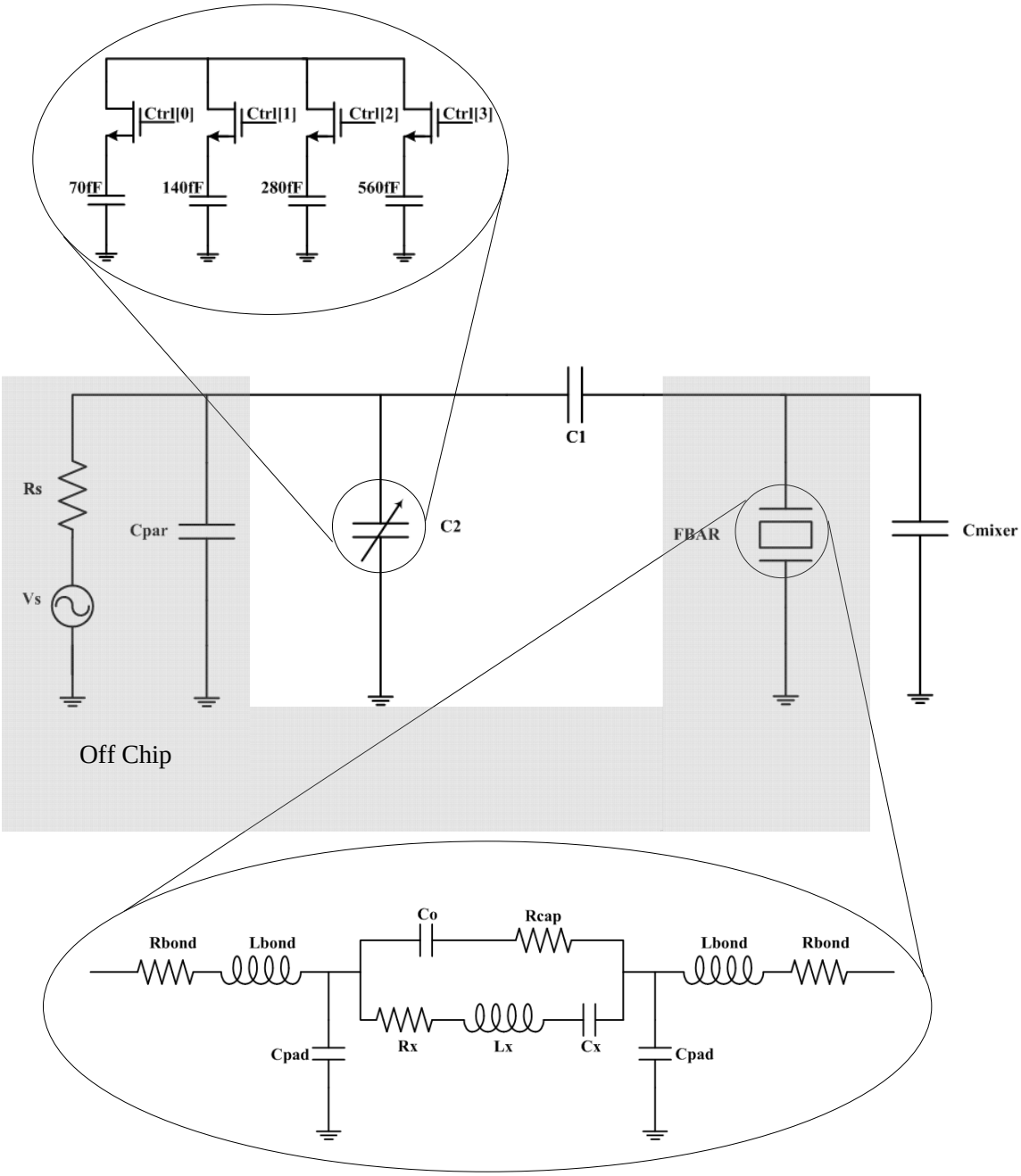

Figure 3.20 Complete schematic of FBAR resonate input matching network with parasitics

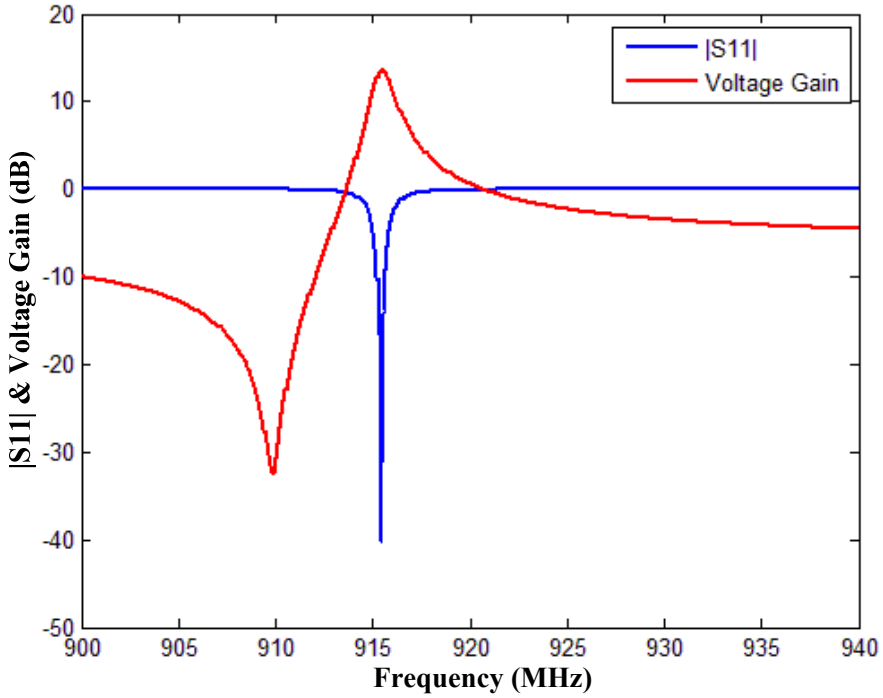

Figure 3.21 Simulated S11 and voltage gain

input capacitance of the following mixer stage C_{mixer} can then be absorbed with the resonator shunt capacitance Co. As Co is about 2pF, the relatively small C_{mixer} has little influence on network response and can be neglected. Transformer capacitance C_1 and C_2 are built with Metal- oxide -metal (MOM) capacitors. Since they connect to an off-chip antenna or RF input source, an extra capacitor C_{par} is used to model the substantial parasitic capacitance arising from chip and printed circuit board (PCB) pads and traces. C_{par} appears in parallel with C_2 and may range from 500fF to 1.5pF.

For matching purpose, the impedance of capacitive transform network at resonant frequency needs to match the parallel impedance of FBAR resonator. One major drawback of this method is that it degrades the noise figure by 3dB. Combining (3.48) and (3.50) togother

$$R_{in} = \frac{\omega_p{}^2 R_s^2 (C_1 + C_2)^2 + 1}{\omega_p{}^2 R_s C_1^2} = R_p = \frac{1}{(\omega_p C_T)^2 (R_m + R_{cap})} \tag{3.52}$$

$$\omega_p = 2\pi f_s \sqrt{1 + \frac{C_m}{C_T}} \tag{3.53}$$

where C_T is the total capacitance in shunt with the resonator $C_T = C_o + C_{pad} + C_1 + C_{mixer}$

With the typical value of FBAR resonator model and estimated parasitics, C_1 is designed to be 1.1pF and C_2 is designed to be 1.5pF with 4 bits switched capacitor tuning network ranging from 0~1pF. Any value of C_{par} between 500fF and 1.5pF can then be accommodated with the tunable C_2. The simulated $|S_{11}|$ and voltage gain of matching network are plotted in figure 3.21, including all parasitics. It shows another benefit of capacitive transformer that it provides an additional 13.5dB passive voltage gain.

3.3.2 Passive Mixer

After matching network, a mixer down converts the RF signal to IF band. The mixer must present relatively high impedance to the matching network to avoid reducing its gain. In this design, a passive mixer is implemented due to its low power consumption. A single-balanced topology is chosen rather than a double-balanced one as it burns less driving power, besides it is able to achieve positive voltage conversion gain instead of loss. Detailed analysis will be derived in the following section.

Figure 3.22 shows the schematic of single balanced passive mixer and its equivalent circuit model is shown in figure 3.23. The NMOS switches in the passive mixer are driven from a ring oscillator. The driven signal is approximately sinusoidal. As the conductance of NMOS in triode region is linear with Vgs, the resulting time-variant switching conductance g(t) resembles a rectified sine wave. However when LO magnitude is large enough, g(t) can be treated as square wave with turn on time ΔT [Zhou05] as shown in figure 3.24.

$$\Delta T = \frac{\int_0^T g(t)dt}{g_{max}} \tag{3.54}$$

With rail-to-rail LO magnitude, variation of ΔT is realized simply by varying the DC level V_{bias} of the driving waveform. The conversion gain of the passive mixer can be derived by considering sampling a sinusoid that is perfectly in-phase with switch conductance waveform g(t) [Cook06]. The output voltage is simply the average of the input voltage while the switch is conducting. The conversion gain is expressed below:

$$G_{conv} = \frac{2 \times \int_{-\frac{\Delta T}{2}}^{+\frac{\Delta T}{2}} \cos(2\pi ft)\, dt}{\Delta T} = \frac{2\sin\left(\pi \frac{\Delta T}{T}\right)}{\pi \frac{\Delta T}{T}} \tag{3.55}$$

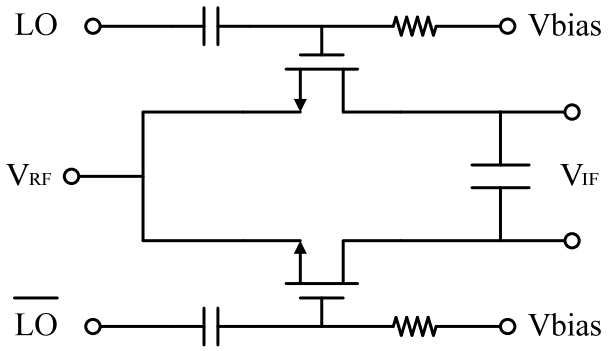

Figure 3.22 Schematic of single balanced passive mixer

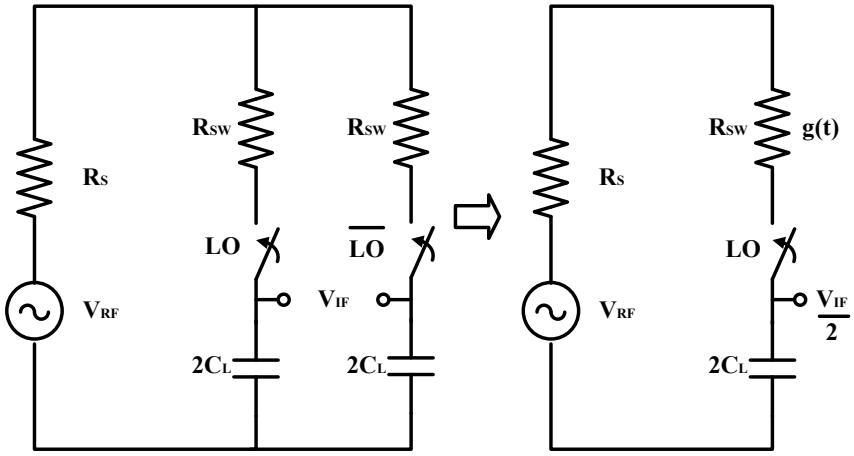

Figure 3.23 Equivalent circuit model for single-balanced passive mixer

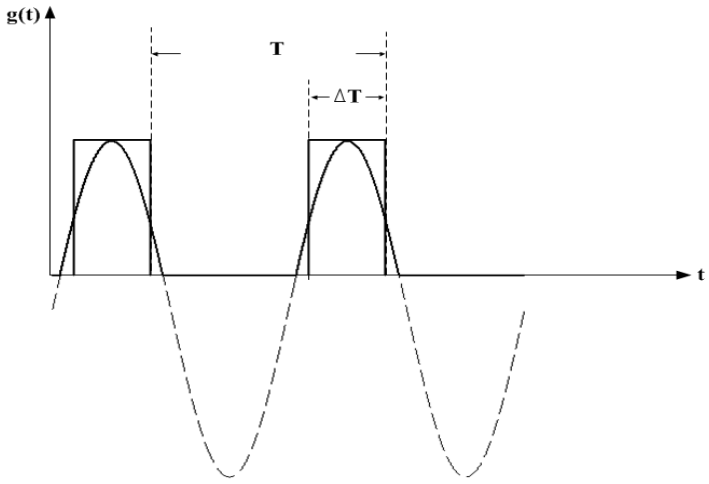

Figure 3.24 Switching conductance waveform

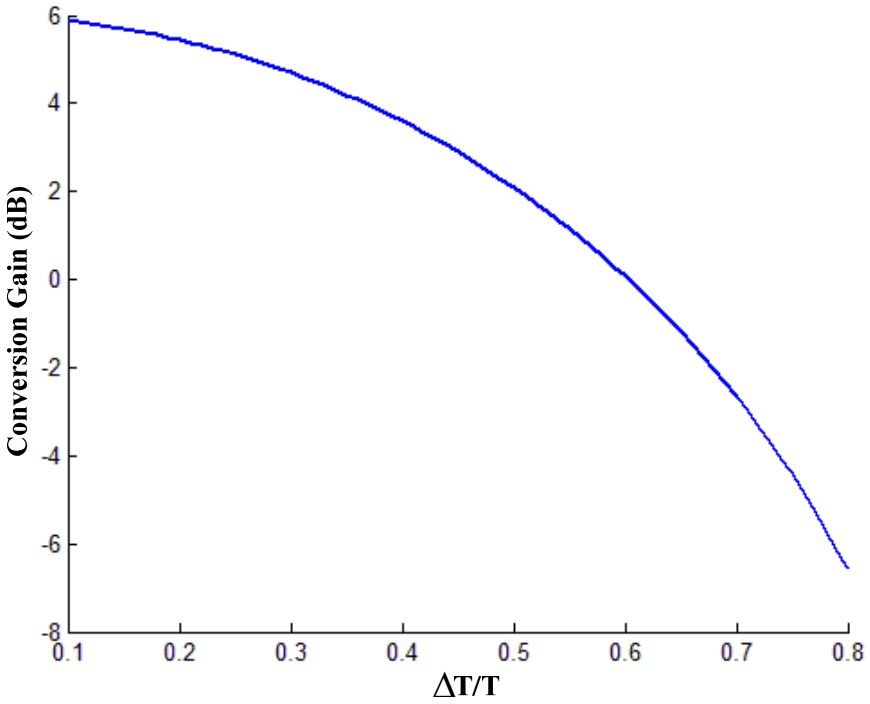

Figure 3.25 Conversion gain of a single balanced passive mixer with different ΔT/T

Figure 3.25 plots the conversion gain of a single balanced mixer with different switch on ratio ΔT/T. For very small ΔT, the conversion gain is high, approaching 6dB and decreases monotonically with an increase of ΔT. When ΔT = ½ T, gain reaches 2.1dB. The conversion gain of a single-balance passive mixer is positive as it is defined in voltage domain not power domain, thus it does not violate the basic physical rule. Note that the loading capacitance C_L is not related to the conversion gain. It defines the bandwidth at the output of mixer which needs to be wider than the interested IF band frequency. The mixer also has gain at the harmonics of the switching frequency. The conversion gain for the n^{th} harmonic is

$$G_{conv,n} = \frac{2\sin\left(n\pi\frac{\Delta T}{T}\right)}{n\pi\frac{\Delta T}{T}} \tag{3.56}$$

Therefore, all n LO harmonics can dump the RF thermal noise to the output. Assuming that the RF thermal noise source is white in the n^{th} harmonic band, the total mixer output noise power is the infinite summation of the noise at harmonics weighted by the conversion gain at each harmonic. The noise of switch resistance R_{SW} is inversely proportional to g_{max}.

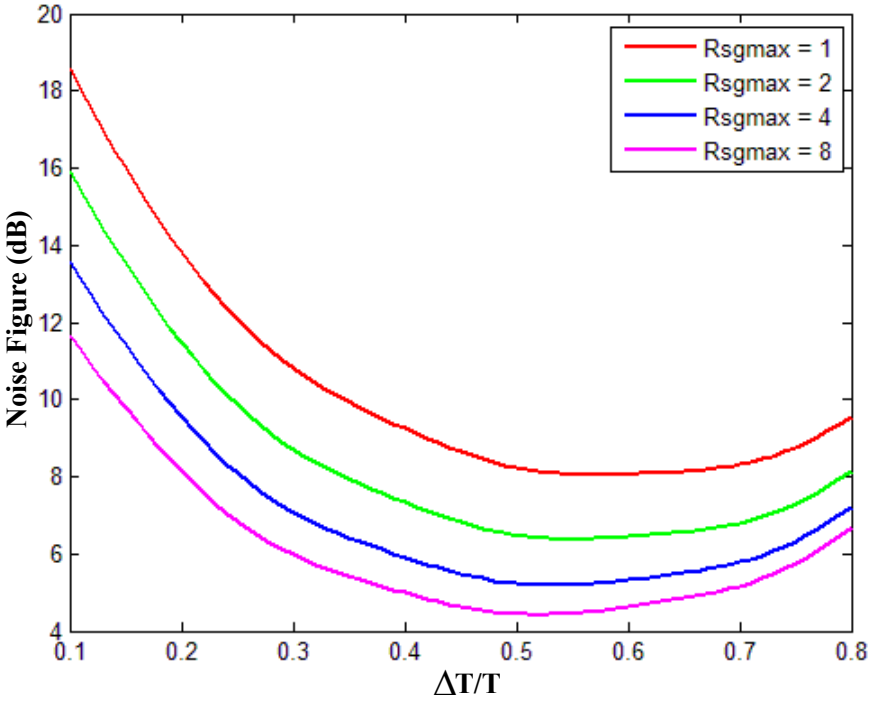

Figure 3.26 Noise figure of a single balanced passive mixer with different $\Delta T/T$ and $R_s g_{max}$

$$\frac{\overline{v_{n,o}^2}}{\Delta f} = 4KT(R_s + \frac{1}{g_{max}}) \sum_{n=-\infty}^{\infty} \left(\frac{2\sin\left(n\pi\frac{\Delta T}{T}\right)}{n\pi\frac{\Delta T}{T}} \right)^2 \tag{3.57}$$

Given the signal conversion gain (3.55), total output noise (3.57), the noise factor of a single balanced passive mixer follows

$$F = (1 + \frac{1}{R_s g_{max}}) \left(2 + 2 \times \sum_{n=2}^{\infty} \left(\frac{\sin\left(n\pi\frac{\Delta T}{T}\right)}{n\sin\left(\pi\frac{\Delta T}{T}\right)} \right)^2 \right) \tag{3.58}$$

Figure 3.26 plots the noise figure of a single balanced mixer with different switch on ratio $\Delta T/T$ assuming $R_s g_{max}$ equals 1, 2, 4, 8 respectively. The noise figure includes up to 5th order harmonics. It shows that when $\Delta T/T$ is much less than 0.3, the noise figure is high due to low average switch conductance and plenty of LO harmonics. When $\Delta T/T$ is much larger than 0.6, the noise figure increases due to less mixing function. It also shows that with an increase of switch conductance, the noise figure can be improved. However this requires larger size of switches which leads to an extra power consumption on LO driving.

The input impedance the mixer also needs to be considered so as not to overload the previous matching network stage to reduce its gain. As the loading capacitance C_L is pretty large which makes the output bandwidth of the mixer much smaller than the RF frequency. One can assume the mixer output voltage holds a quasi-static value during a single conduction period. Thus, the mixer output capacitor could be modeled as an ideal voltage source for this calculation with a DC value equal to the average of the input voltage during the sampling period. [Cook06] Since this circuit model contains no imaginary components, the resulting input impedance is real. The input impedance R_{in} can be derived by calculating the total energy transferred during one complete period. With source impedance R_s, the energy delivered from the source would be:

$$E = \frac{V_{RF}^2}{(R_s + R_{in})} \int_{\frac{-T}{2}}^{\frac{T}{2}} \cos^2\left(\frac{2\pi}{T}t\right) dt = \frac{V_{RF}^2 T}{2(R_s + R_{in})} \tag{3.59}$$

Using the assumptions described in the above paragraph, the actual energy delivered from the source to the mixer is shown below. Note that this calculation must consider the average of both in-phase and orthogonal inputs because the energy delivered, even when the normalized by the period, is dependent on the phase relationship of the input signal to the mixing function.

$$E = \frac{V_{RF}^2}{\left(R_s + \frac{1}{g_{max}}\right)} \int_{\frac{-\Delta T}{2}}^{\frac{\Delta T}{2}} \left[\left(\cos\left(\frac{2\pi}{T}t\right) - \frac{\sin\left(\frac{\pi\Delta T}{T}\right)}{\frac{\pi\Delta T}{T}} \right)^2 + \sin^2\left(\frac{2\pi}{T}t\right) \right] dt$$

$$= \frac{V_{RF}^2 \Delta T}{\left(R_s + \frac{1}{g_{max}}\right)} \left(1 - \frac{\sin^2\left(\frac{\pi\Delta T}{T}\right)}{\left(\frac{\pi\Delta T}{T}\right)^2} \right) \tag{3.60}$$

Therefore, setting (3.59) to (3.60), the result of input impedance R_{in} is shown below.

$$R_{in} = \frac{R_s\left(1 + \frac{1}{g_{max}R_s}\right)}{\frac{\Delta T}{T}\left(1 - \frac{\sin^2\left(\frac{\pi\Delta T}{T}\right)}{\left(\frac{\pi\Delta T}{T}\right)^2}\right)} - R_s \tag{3.61}$$

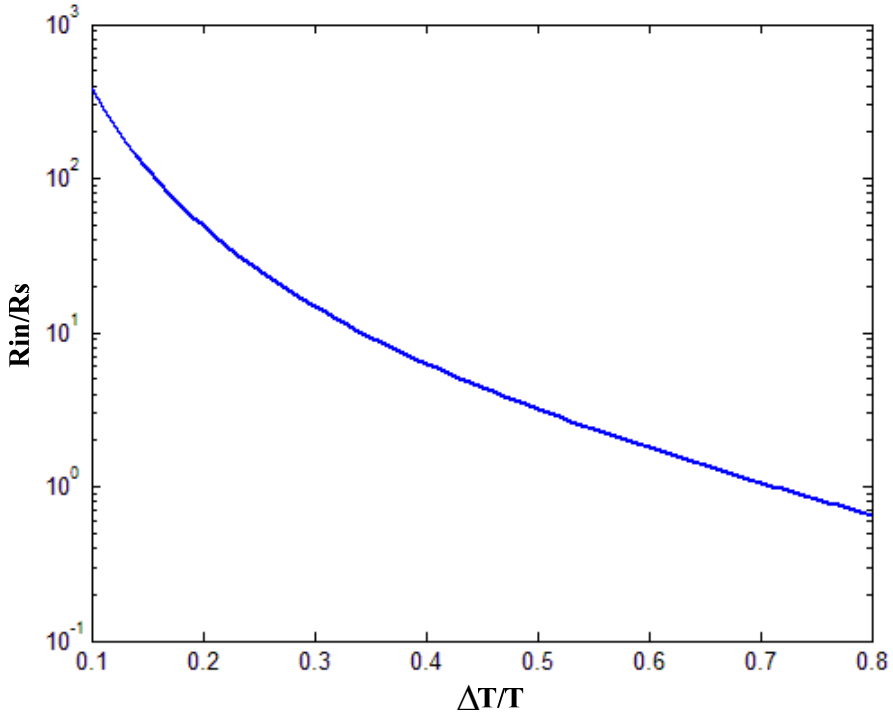

Figure 3.27 Input impedance of a single balanced mixer with different ΔT/T

Figure 3.27 plots the input impedance R_{in} of a single balanced mixer normalized to source impedance R_s. A smaller ratio of ΔT/T should be picked to prevent the mixer taking significant effect on the matching network. Hence, taking voltage conversion gain, noise figure and input impedance into account, ΔT/T is designed to be around 0.4. The single balanced mixer has a simulated conversion gain of 3dB and noise figure of 7.5dB.

3.3.3 Current Starved Oscillator

The LO generation is implemented with a simple 3 stage ring oscillator utilizing the current starved architecture as shown in figure 3.28. Its operation is similar to a typical ring oscillator. MOSFETs M1 and M2 operate as an inverter, while MOSFETs M3 and M4 operate as current source. The current source M3 and M4 limit the current available to the transistor M1 and M2. In other words, the inverter is starved for current. The current is tuned by an off-chip resistor DAC and mirrored to each stage through MOSFETs M5, M6 and M7. The frequency of the ring oscillator can be derived as:

$$T_{osc} \propto \frac{NC_{eff}V_{DD}}{I_{bias}} \Rightarrow f_{osc} \propto \frac{I_{bias}}{NC_{eff}V_{DD}} \tag{3.62}$$

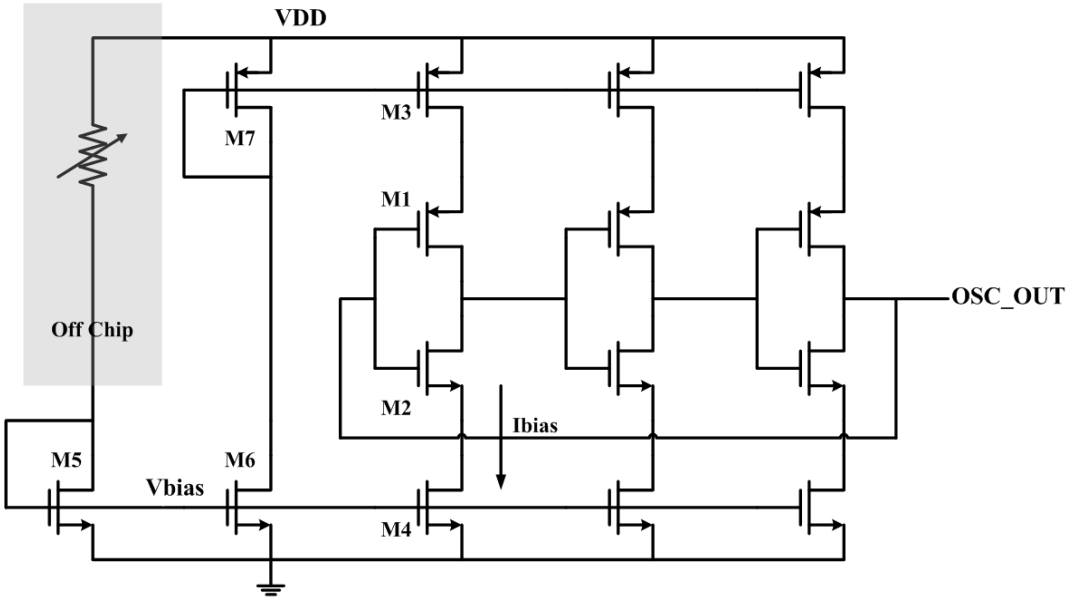

Figure 3.28 Schematic of current starved ring oscillator

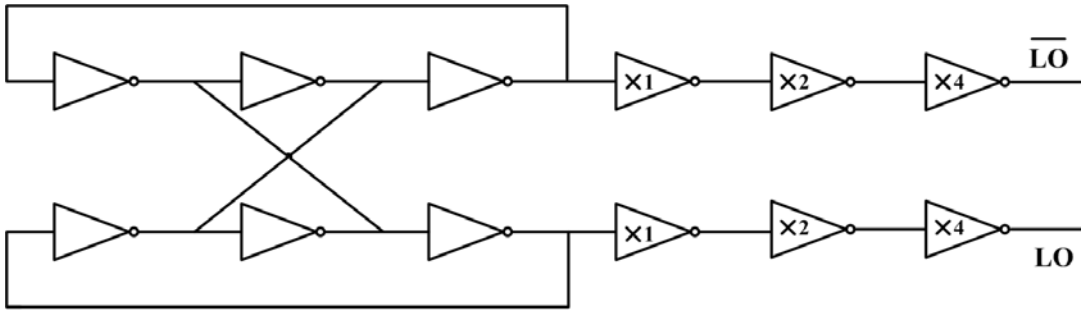

Figure 3.29 Schematic of differential oscillator

where N is the number of stages, C_{eff} is the total capacitance on the drain of M1 and M2. It shows that the frequency of the oscillator can be turned linearly with bias current.

As the single balanced mixer needs two phase of LO, two 3 stage current starved ring oscillators are implemented with second and third stage cross-coupled with each other to align the phase as shown in figure 3.29. The following scaled inverter chain serves as buffer to drive the mixer LO port. Low threshold devices are used to ensure sufficient speed with 0.5V supply. All core devices are sized with minimum size to reduce the effective loading capacitance so as to minimize the total power consumption. With 5 bits resistor DAC which is a simple switched resistor network, the frequency of oscillator can be calibrated within 30MHz of designed frequency. To auto calibrate process, voltage supply and temperature

(PVT) variation, an ultra-low power phase lock loop (PLL) could be included [Abe14]. Its reference clock is supplied by a 32.77 kHz crystal oscillator that can work with lower than 1 μW. To achieve ultra-low power consumption, it sacrifices its phase noise performance which can be tolerated within our proposed architecture. The PLL including the reference clock consumes only 23.8 μW at 925.4 MHz, achieving phase noise of -66.69 dBc/Hz at 1MHz offset.

3.3.4 IF Amplifiers

As specified in architecture design, the IF stages should provide sufficient gain such that the intrinsic characteristic of envelope detection will not degrade the sensitivity performance. Also the gain must be provided across a wide bandwidth due to the inaccuracy of ring oscillator. These requirements are fulfilled by cascading three differential amplification stages with each differential pair biased in the sub-threshold regime for high trans-conductance efficiency (g_m/Id).

The first stage serves as an IF LNA and burns most of the power budget. As shown in figure 3.30, it utilizes a pseudo-differential pair with current reuse topology to minimize the noise figure for a given current. The PMOS and NMOS devices are sized to achieve similar gm so that at very low frequency where the input signal only appears at the NMOS gates and these devices drive diode connected PMOS loads, the amplifier provides approximately unity gain to mitigate accumulated offset voltage. The combination of C and MOS resistor M5/M6 creates a high-pass filter, passing the input signal to the gates of the PMOS devices. Thus, the current required to meet noise constraints is reduced because amplifier utilizes the g_m of both NMOS and PMOS devices in the pass-band. The corner frequency is set around 1MHz to eliminate the effect of flicker noise. This causes a small 1MHz dead zone around the desired frequency, yet it is unlikely that LO frequency lies directly on the input frequency and in that case the LO could be re-calibrated. The second stage adopts similar topology except it uses true differential pair and is optimized for maximum gain-bandwidth product. The last stage is a simple differential pair with small resistive load served as a pre-drive stage for the following envelope detector as shown in figure 3.30.

The three gain stages together produce more than 55 dB of total gain, with each stage consuming 40μA, 3μA and 3μA of current respectively. Figure 3.31 plots the simulated frequency response of the complete IF amplifier. Conner simulations were run to make sure that the amplification would have adequate bandwidth under the worst conditions. The -3 dB bandwidth marked in figure 3.31 verifies that the IF amplifier has high gain across the band from 760kHz to 35MHz, with a peak gain of 55.3dB. When combining matching network, passive mixer together with IF amplifiers, the receiver frontend provides more than 70dB total gain with a noise figure of 12dB.

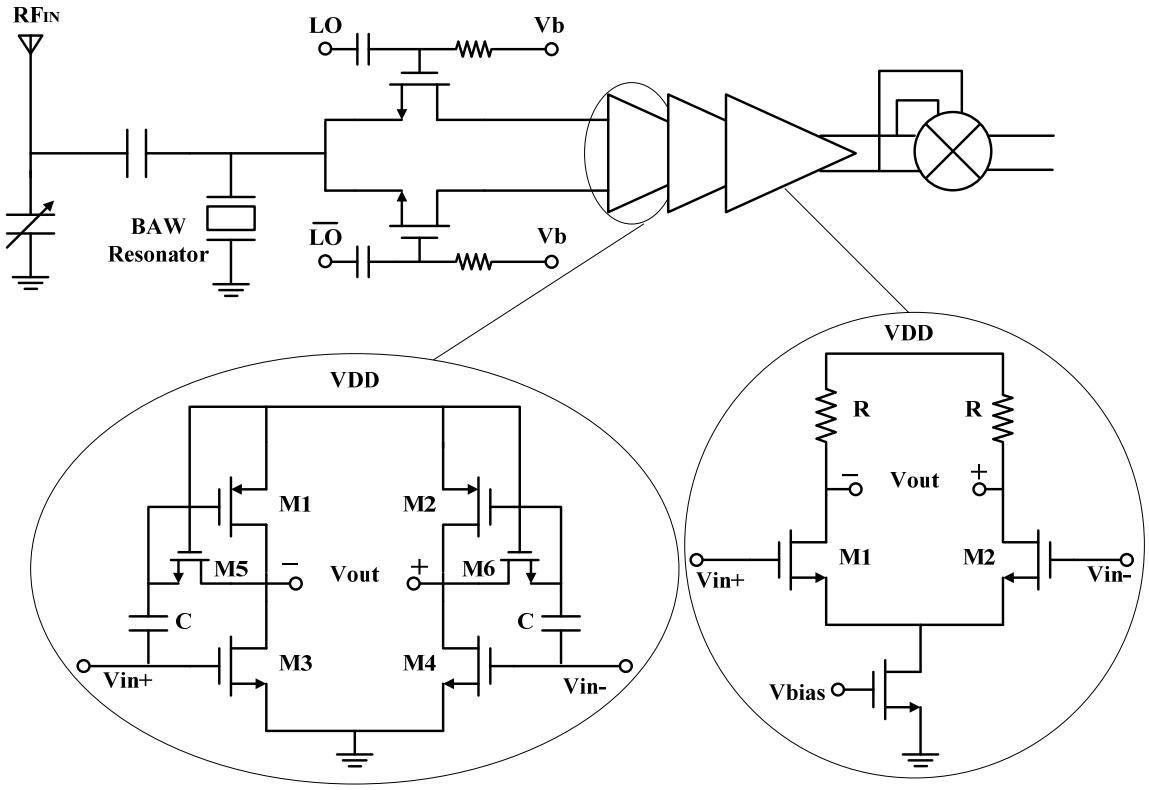

Figure 3.30 Schematic of IF Amplifiers

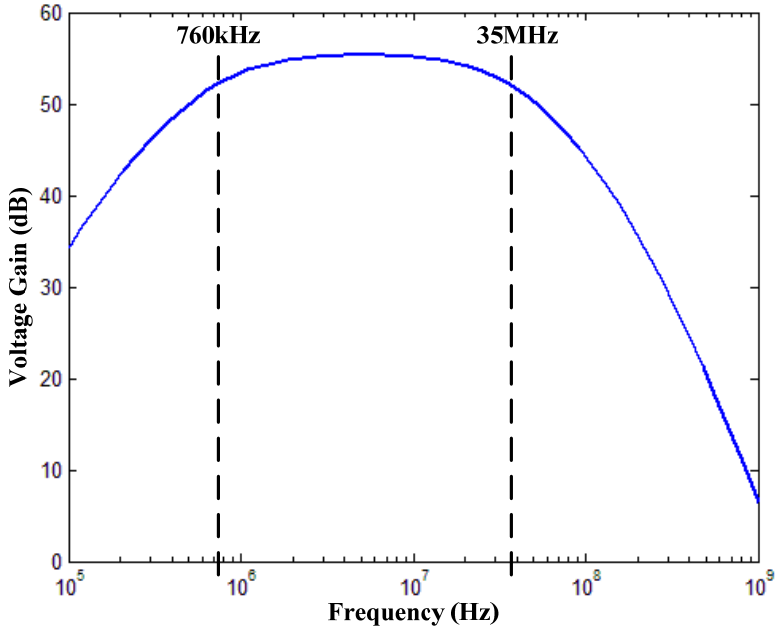

Figure 3. 31 Simulated IF Amplifier Frequency Response

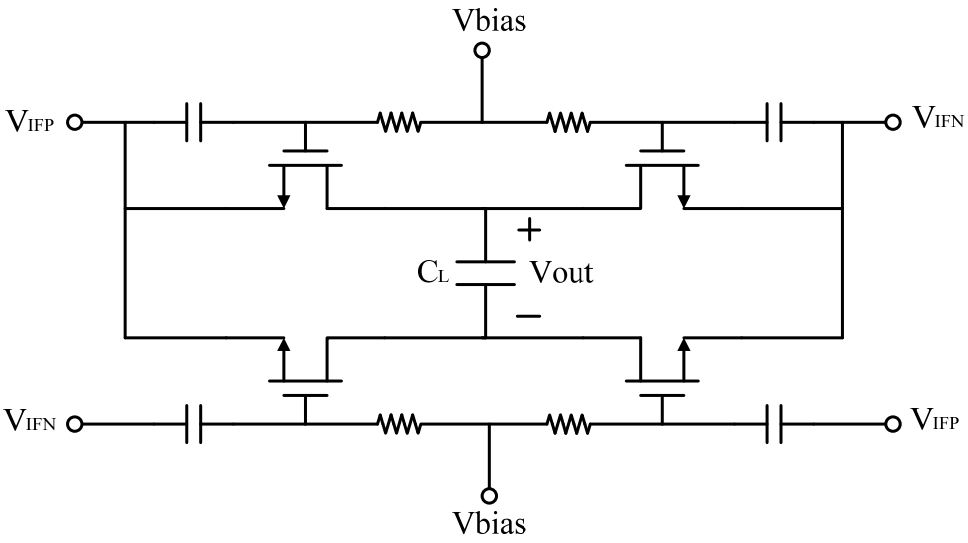

Figure 3.32 Schematic of Envelope Detector

3.3.5 Envelope Detector

The envelope detection circuit is implemented with a self-driven passive mixer structure. [Pletcher08] has proven that it has better performance than the typical differential pairs based envelope detector [Daly07] as it combines the outputs of both halves of the differential input constructively at the output. Moreover, it does not consume any power budget. The complete schematic including biasing is shown in figure 3.32. The IF signal from IF amplifier directly drives the source/drain of MOSFET and is AC coupled to the gate of MOSFET to allow DC biasing of the transistors around the threshold voltage for maximum nonlinearity. To avoid loading the IF amplifier excessively, the MOSFET devices should not be sized too large.

The simulated conversion gain of the envelope detector is shown in figure 3.33. Obviously, the conversion gain is proportional to the input voltage swing. A large input swing is desirable to achieve a high conversion gain so that the noise generated by the envelope detector itself becomes negligible and would not affect the overall sensitivity performance. On the other hand from previous sensitivity analysis, to achieve a sensitivity of -90dBm, the target SWNR at the input of the envelope is around -6dB which means the noise swing should be twice as much as the signal swing. Therefore, the input signal should not be designed too high, otherwise the large noise would push the IF amplifiers into the non-linear region and would degrade the overall performance. In our prototype, the input swing of the envelope detector is chosen to be 100mV and this means the RF frontend should provide around 70dB gain.

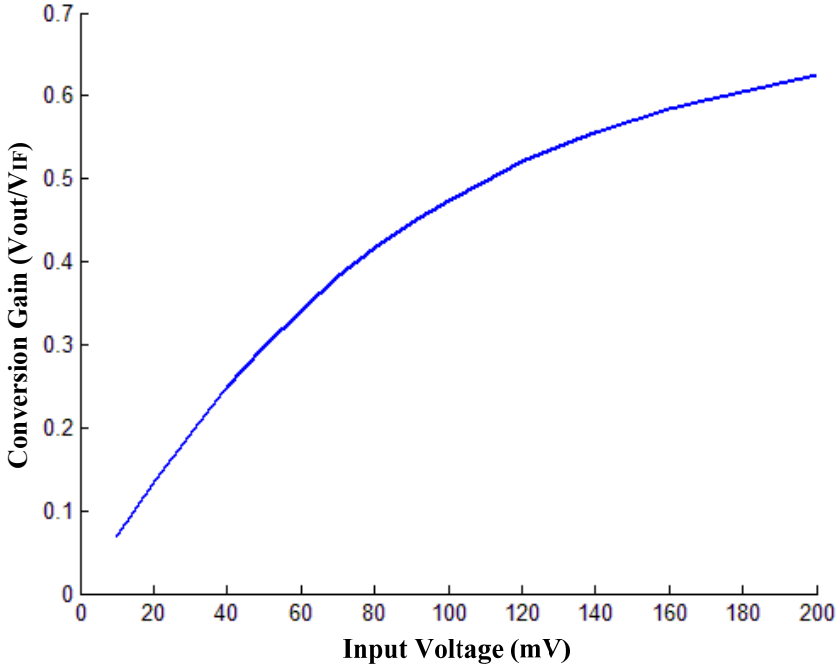

Figure 3.33 Conversion Gain of Envelope Detector

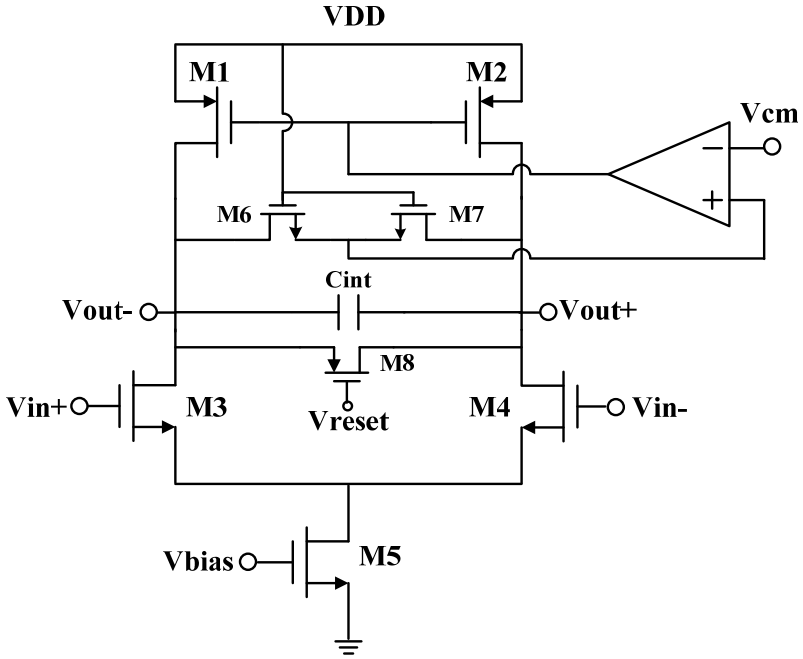

Figure 3.34 Schematic of Integrator

3.3.6 Integrator

The integrator circuit is implemented with Gm-C integrator structure as shown in figure 3.34. The differential source coupled pair M3 and M4 forms a transconductance element converting the input voltage to an output current which flows into the integrating capacitor Cint. The MOS resistors M6 and M7 help to sense the common mode voltage of the output node and set it to Vcm through the common mode feedback (CMFB) circuitry. STB analysis has been performed in Cadence to make sure that CMFB circuit is stable under all different conditions. PMOS M8 is controlled by a periodic signal Vreset to reset the integrator output at the initial phase of each integration period. The unity gain frequency of this integrator is given by

$$\omega_u = \frac{g_{m3,4}}{2C_{int}} \tag{3.63}$$

where $g_{m3,4}$ is the transconductance of input pair M3 and M4. It is evident that ω_u is process dependent and can be controlled by varying the tail current through Vbias.

Ideally the integrator is expected to have an infinite DC gain, however it is not realistic due to the finite output resistance of the MOSFETs. Therefore the dominant pole is no longer equals to zero, rather it is defined by

$$f_p = \frac{1}{2\pi \cdot 2C_{int}(r_{o1,2}//r_{o3,4}//r_{o6,7})} \tag{3.64}$$

where $r_{o1,2}$, $r_{o3,4}$, $r_{o6,7}$ are the output resistance of M1~M4, M6 andM7. This dominant pole needs to be low enough such that it would not affect the whole integration process.

To verify the dominant pole effect of the practical integrator, a matlab model of the entire energy detector is built. Performance comparison has been evaluated between using ideal integrator and practical integrator model. Figure 3.35 shows the matlab simulation result assuming that the dominant pole (f_p) of integrator is 10k and integration time T varies from 10us to 100us. It can be viewed from the figure that when the integrating frequency (1/T) is comparable to f_p, it introduces more than 2.4dB of error in the minimum required SWNR to achieve a certain error rate. This means it degrades the sensitivity performance by 2.4dB. However when 1/T is more than 10 times larger than f_p, the overall performance would not be affected. From previous analysis, the integration time T is designed to be 20us. Therefore the dominant pole of the integrator should be less than 5k.

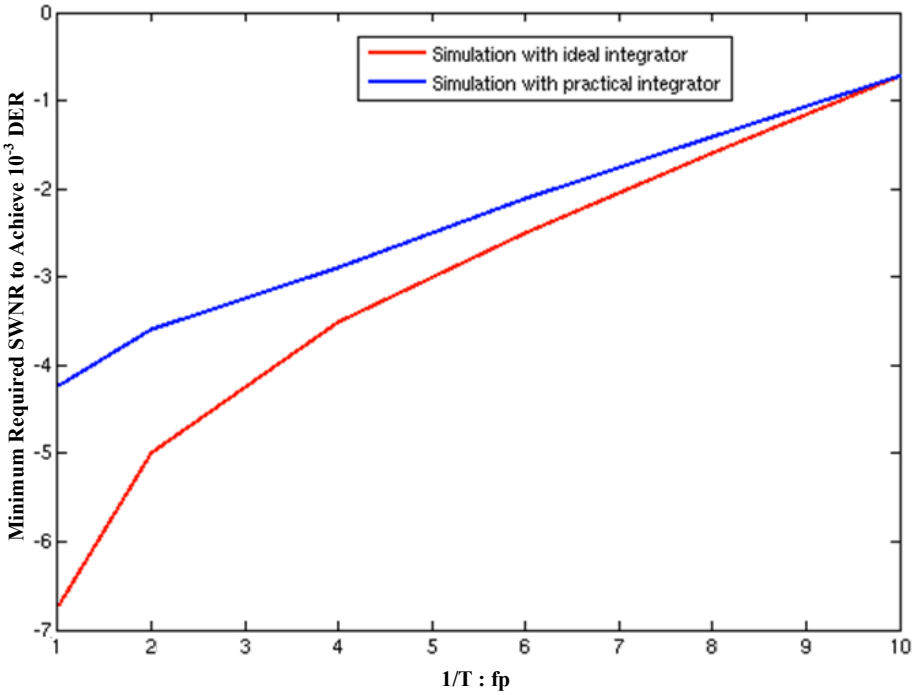

Figure 3.35 Performance Comparison between Using Ideal and Practical Integrator

3.4 Summary

This chapter has presented a guideline for designing an ultra-low power high performance energy detection receiver. It proposes a receiver architecture adopting the "wideband-IF" concept to utilize a low power ring oscillator instead of a LC oscillator for LO generation which results in huge power saving to satisfy the power budget. Meanwhile, it also applies a "noise averaging" concept to reduce the excess noise generated by "wideband-IF" so as to improve the receiver sensitivity to the desired number. A detailed theoretical analysis has been provided and performances with different conditions of design parameters have been demonstrated. Simulation result shows that with 20us integration time, it can effectively remove more than 15 dB of excess noise from 35MHz noise band. With an expected 12dB noise figure due to low current budget, the receiver could achieve sensitivity of -91dBm. The sensitivity can be further improved by 5dB when increasing integration time or decreasing noise bandwidth by 10 times. All of this leads to a tradeoff among achievable sensitivity, system latency and power consumption. Besides theoretical analysis, detailed circuit implementation for each design block of the receiver has been provided. The proposed energy detection receiver can also be used as OOK demodulator in many ultra-low power application to achieve better sensitivity performance.

Chapter 4

Receiver for Address Detection Mode

4.1 Architecture Development

As described in Chapter 2, in address detection mode, the main functionality of receiver is to perform FSK demodulation of the input RF signal. The major performance specification of the receiver remains in low power consumption (400μW), high sensitivity (-90dBm), low data rate (50k) and typical bit error rate (10^{-3}). Since in address detection mode the power dissipation requirement is relaxed to hundreds of microwatts, a high precision LO generation can now be tolerated. On the other hand, for FSK modulation, data information is transmitted through discrete frequency changes of the carrier wave. Thus a high accuracy and low phase noise reference clock is preferred to help distinguish between two discrete frequencies when input signal power is extremely small. As a consequence, the direct conversion architecture and the low-IF architecture as shown in figure 4.1 and figure 4.2 become two suitable solutions for receiver design in address detection mode. Although the direct conversion architecture does not have image problem, it requires phase locking the local oscillator to the carrier frequency. To avoid that, a quadrature down-conversion with I/Q two channels followed by baseband digital signal processing is typically adopted. Yet this requires extra power dissipation for the second channel chain. Therefore considering our low power budget requirement, the low-IF architecture is chosen to build the prototype. In fact, with the advanced high Q MEMS technology, the image problem can be largely relaxed.

Figure 4.3 and figure 4.4 show the proposed receiver architecture and its frequency planning. Like the energy detection mode, the input RF signal first passes through the matching network. With the MEMS resonator embedded, the matching network also provides a high selectivity and helps to eliminate the close interfering signals as well as the image signal. Then the RF signal is down-converted to the fixed IF with a mixer and a FBAR based oscillator. The resulting IF signal is amplified and filtered with gain blocks and

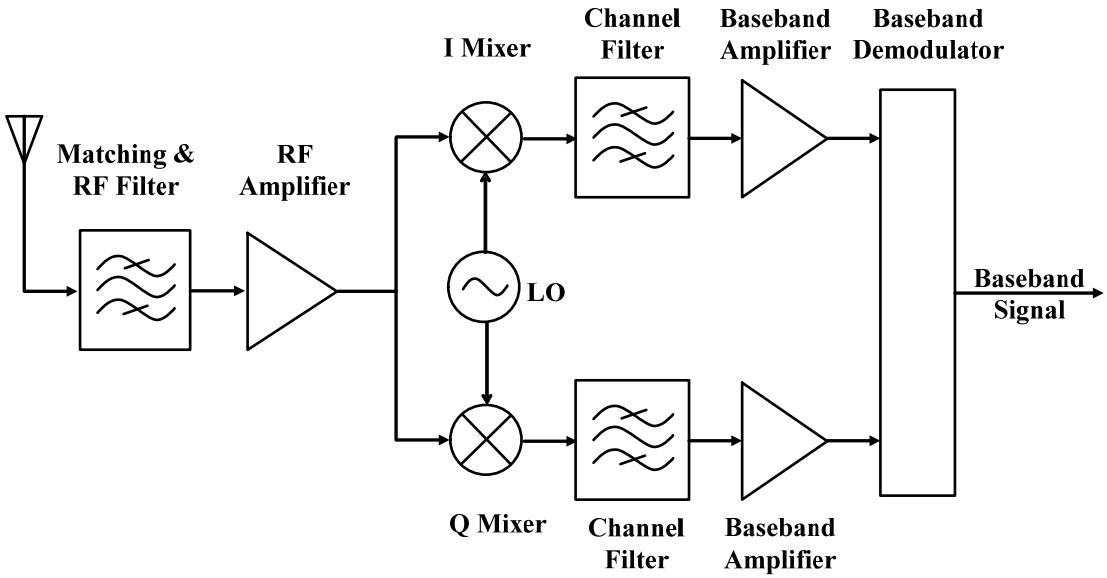

Figure 4.1 Direct Conversion Architecture

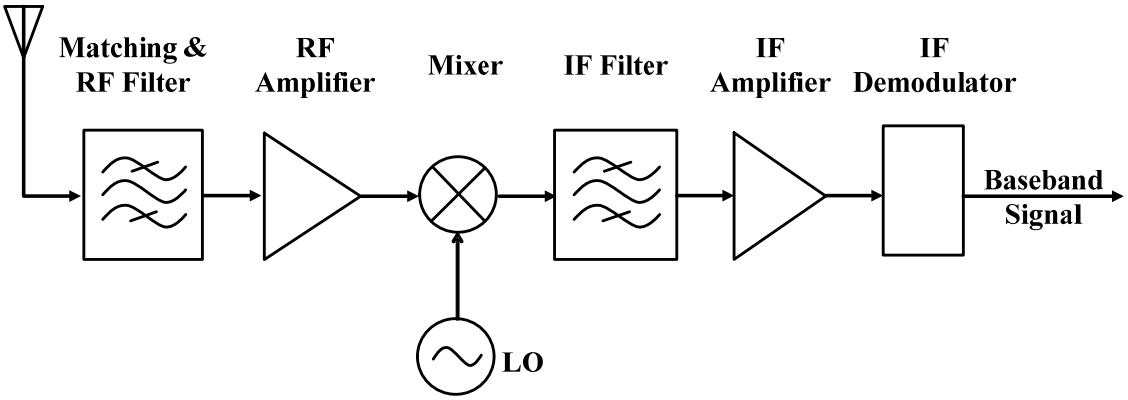

Figure 4.2 Low-IF Architecture

converted to digital signal with a limiter such that it can be further decoded to get its baseband data through a FSK IF digital demodulator. The reference clock used in digital demodulation is divided from the FBAR injection locked oscillator. To simplify the complexity of receiver frontend circuitry, the FSK receiver shares the same matching network, passive mixer and first IF gain stage (IF LNA) with the energy detector. Moreover, the output of FBAR oscillator is injection locked to the three stage ring oscillator for LO generation. It helps to avoid switching between different types of LO generations so as to minimize parasitics and also to save power spent on amplifying the FBAR oscillator output to a rail-to-rail swing. Detailed circuit implement for each block will be described in next section.

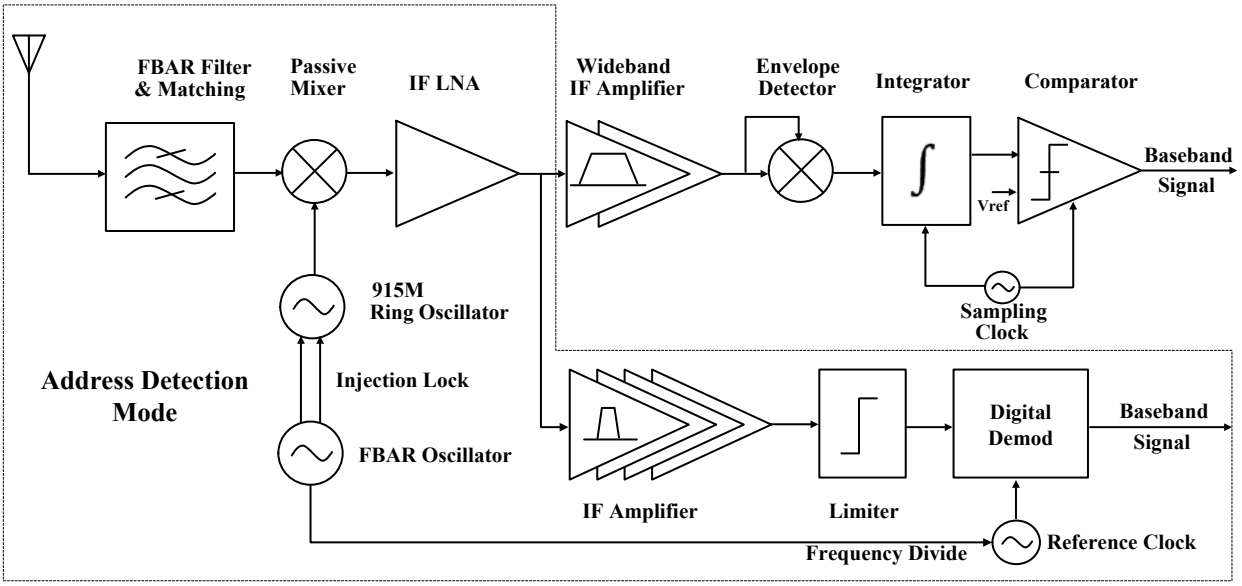

Figure 4.3 Proposed Receiver Architecture in Address Detection Mode

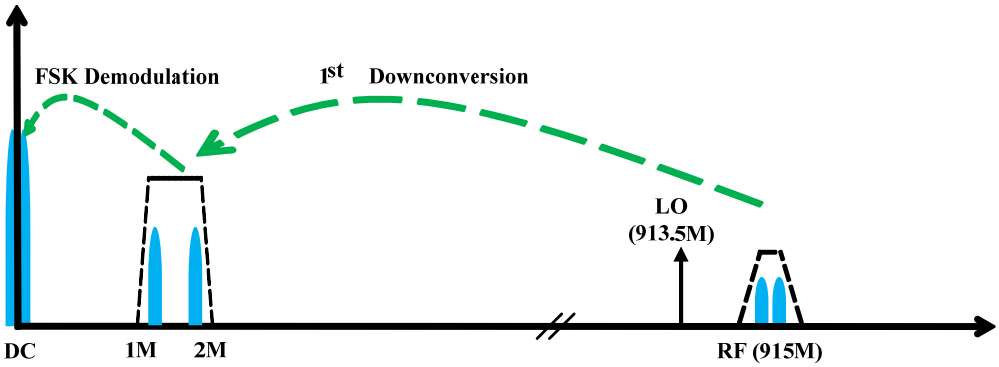

Figure 4.4 Frequency Planning for Receiver in Address Detection Mode

4.2 Circuit Design

This section presents a detailed design of receiver circuitry shown in figure 4.3. As it uses the same matching network, passive mixer and IF LNA with the energy detection receiver which have already been discussed in previous chapter, this section will focus on the circuit implementation of rest blocks. For low power consideration, the entire receiver is also optimized for sub-threshold operation from a single 0.5V supply.

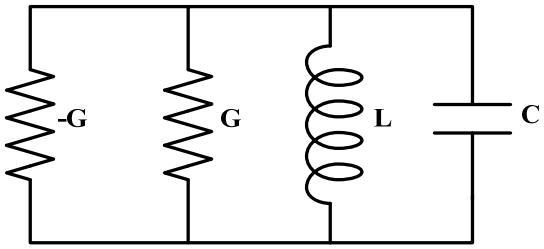

Figure 4.5 Model of an Oscillator

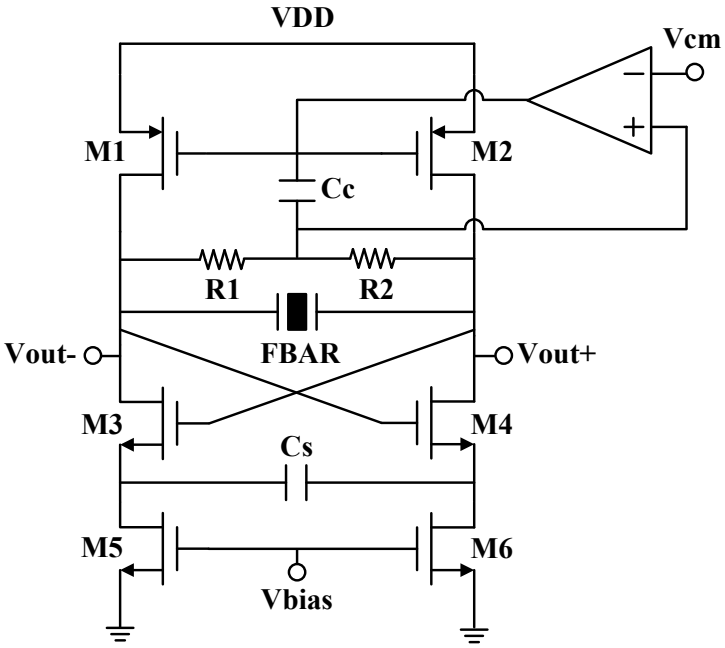

Figure 4.6 Schematic of Differential FBAR Oscillator

4.2.1 Injection Locked Oscillator

A typical oscillator design can be modeled as an equivalent LC circuit in parallel with a conductance G representing the finite quality factor (Q) of the resonator and a negative conductance –G provided by the active circuits to compensate for the resonator loss as shown in figure 4.5. Since G is proportional to 1/Q and a larger negative conductance requires higher current, a higher Q factor results in lower power dissipation. The Q factor of an on-chip inductor in standard CMOS is often less than 20. However as discussed previously, the Q factor of a FBAR resonator could reach several thousands. Besides, it performs inductively between its series and parallel resonance. Therefore, by replacing the

inductor with a FBAR resonator in the oscillator design, a low power and high performance oscillator could be achieved.

Because the ring oscillator is fully differential, the FBAR oscillator will also need to be differential to avoid unbalancing the ring oscillator and disturbing its phase balance. The schematic of a differential FBAR oscillator is shown in figure 4.6. The FBAR resonator is placed in shunt across the cross-coupled pair, providing a high Q response at the parallel resonance to set the oscillator frequency. The cross-coupled pair M3 and M4 yield negative conductance and are sized big such that they are pushed into the weak inversion regime for transconductance efficiency. The resistors R1 and R2 help to sense the common mode voltage of the output node and set it to Vcm through the common mode feedback (CMFB) circuitry. Large resistance is preferred without de-tuning the parallel resonance. Cc is added to improve the stability of CMFB circuitry and STB analysis has been performed in Cadence to make sure that CMFB circuit is stable under all different conditions.

Similar to (3.52) and (3.53), the oscillator frequency and the parallel impedance of FBAR resonator is given by

$$f_{osc} = f_s \sqrt{1 + \frac{C_m}{C_T}} \tag{4.1}$$

$$R_p = \frac{1}{(2\pi f_{osc} C_T)^2 (R_m + R_{cap})} \tag{4.2}$$

where C_T is the total capacitance in shunt with the resonator including the parasitic capacitance from M1~M4 and pads. $C_T = C_o + C_{pad}/2 + C_{par,M1}/2 + C_{par,M3}/2$

Although the FBAR resonator presents high impedance at its parallel resonance, at low frequencies, it presents even higher impedance as shown in figure 3.16. Thus, the circuit would be DC unstable and latch-up like a comparator. One possible way to overcome this problem is to design a high-pass response into the negative conductance of the cross-coupled pair. This can be realized by using separate current sources (M5 and M6) for the cross-coupled pair and coupling the sources through a capacitor Cs [Ruffieux02]. At low frequencies, the cross-coupled pair experiences a large degeneration, reducing the negative conductance. At high frequencies, the sources are connected together, providing full transconductance from the cross-coupled pair. It can be shown that the differential conductance looking down into the cross-coupled pair is given by [Otis05-2]

$$G = -\frac{g_{m3}}{(1 + \frac{g_{m3}}{s \cdot 2C_s})} \tag{4.3}$$

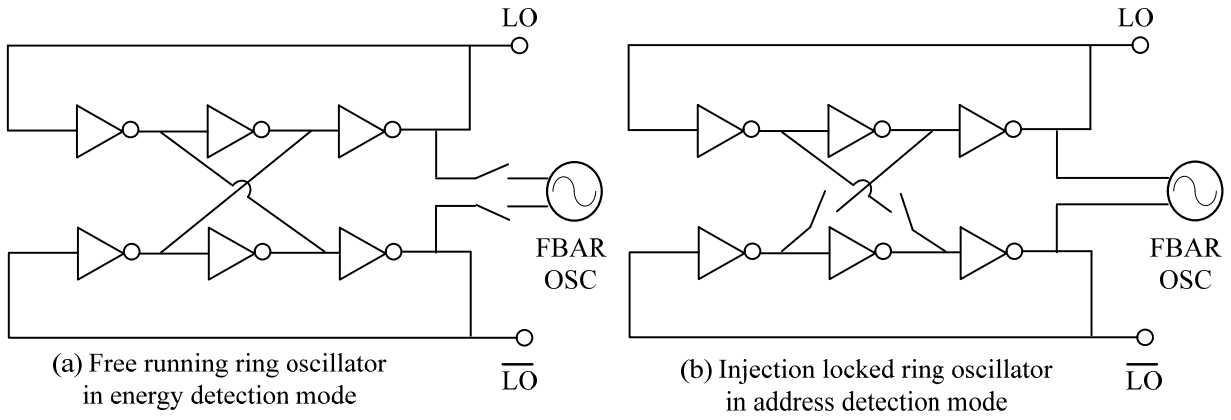

Figure 4.7 Ring Oscillator in Different Working Mode

At high frequencies, the cross-coupled pair provides $-g_{m3}$ of negative conductance and to sustain a stable oscillation, the achievable loop gain ($g_{m3} \cdot R_p$) must be larger than 0dB. Besides, proper choice of Cs is also important for stable and efficient oscillation. When it is high, it increases the loop gain at low frequency and would cause a parasitic oscillation. When it is low, it reduces the oscillator loop gain at the desired resonance and requires extra power dissipation to oscillate. For our oscillator design, Cs=1.6pF is chosen to provide stable operation over the whole frequency range

From circuit simulation, with 200uW power consumption, the differential oscillator is able to provide an output swing of 140mV and it is injection locked to the three stages ring oscillator to drive the passive mixer as shown in figure 4.7. The injection lock procedure is initiated by opening the loop of cross-coupled ring oscillators and closing the MOS switches to inject the current from FBAR oscillator to ring oscillator. As it is a single-end injection, the locking range is given by [Chien07]

$$\frac{\Delta f}{f_{osc}} \leq \frac{1}{N} \cdot \frac{1 + tan^2(\frac{\pi}{N})}{\tan(\frac{\pi}{N})} \left|\frac{I_{inj}}{I_{osc}}\right| \left(1 - \left|\frac{I_{inj}}{I_{osc}}\right|^2\right)^{-\frac{1}{2}} \tag{4.4}$$

where N is the number of stages in the ring oscillator (N=3), f_{osc} is the oscillation frequency (f_{osc} = 915MHz), Δf is the frequency locking range (Δf > 30MHz). Plugging all the numbers into (4.4) yields

$$\left|\frac{I_{inj}}{I_{osc}}\right| \geq 4.2\% \tag{4.5}$$

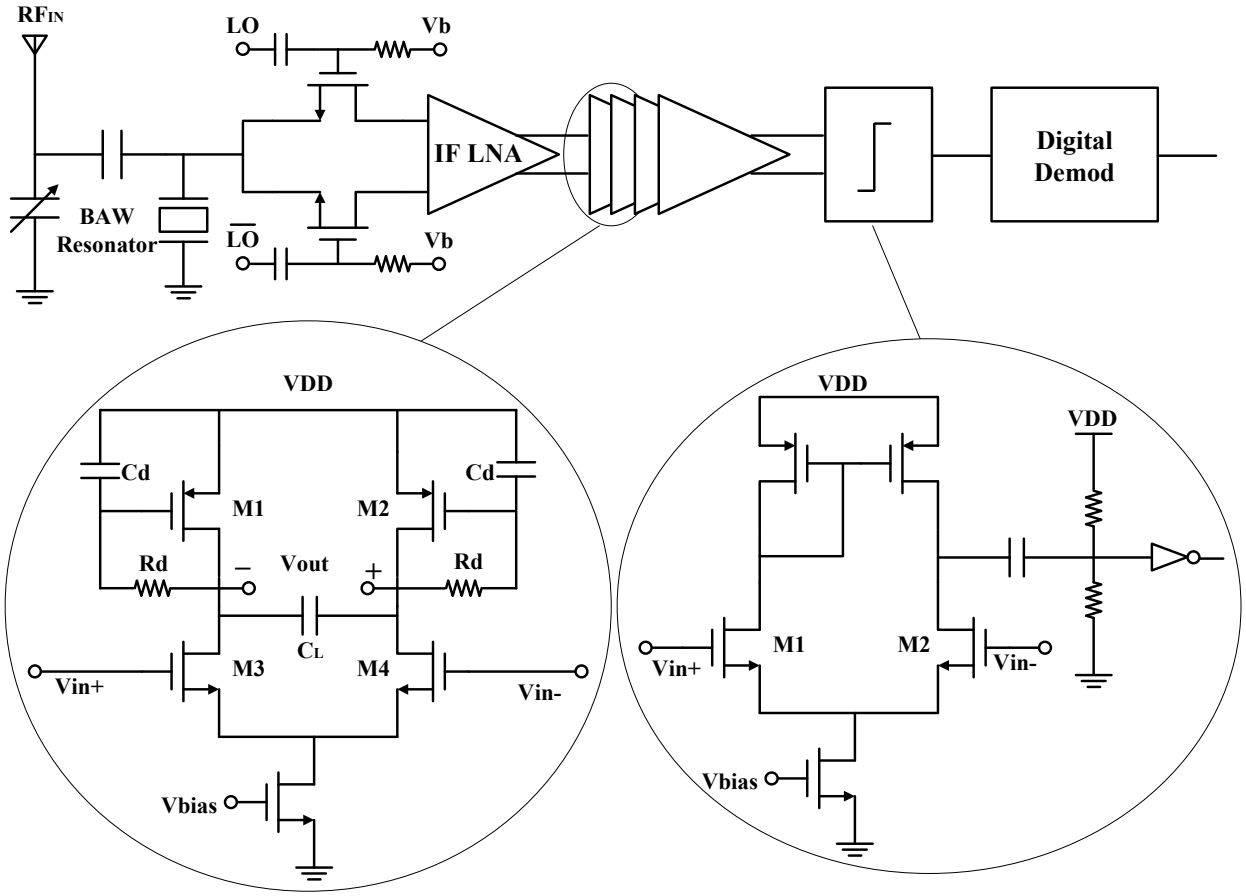

Figure 4.8 Schematic of IF Stages

(4.5) shows a relax requirement to injection lock the ring oscillator. Considering a 250mV oscillation swing, roughly an 11mV input swing is required which is much less than the swing a FBAR oscillator could sustain.

4.2.2 IF Stages

As specified in architecture design, the IF stages should provide sufficient gain as well as adequate bandpass filtering. This is fulfilled by cascading four identical amplification stages with each differential pair biased in the sub-threshold regime for high trans-conductance efficiency (g_m/Id). The bandwidth of bandpass filters is related to frequency deviation of FSK signal. Due to the analysis in 4.2.3, with baseband datarate of 50 kHz and modulation index of 16, the desired frequency deviation in this prototype is 800 kHz. Besides the IF signal is designed to be 1.5MHz. Therefore, the bandwidth of the IF amplifier is required to be 1MHz covering frequency range from 1MHz to 2MHz.

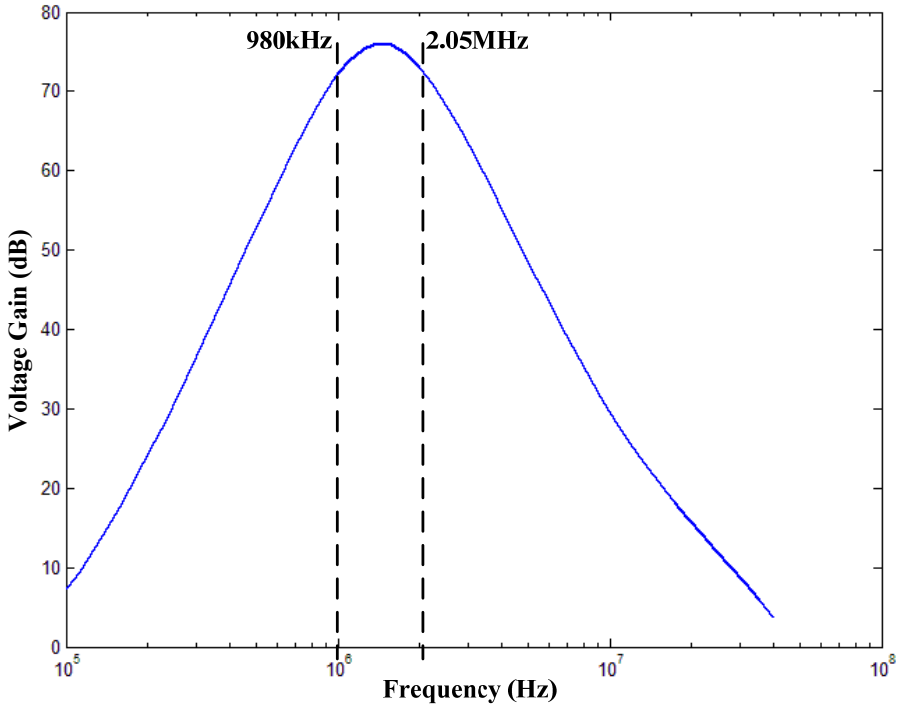

Figure 4.9 Simulated IF Amplifier Frequency Response

The schematic of an IF amplifier is shown in figure 4.8. The PMOS and NMOS devices are sized to achieve similar gm so that at very low frequency where PMOS loads are diode connected, the amplifier provides approximately unity gain to mitigate accumulated offset voltage. Thus, the DC gain through the entire baseband chain is 1 and no DC offset cancellation circuit is required. At high frequency, the PMOS devices serves as active loads and the amplifier provides approximately gain of $gm_3.(ro_1//ro_3)$. The combination of Cd and Rd create a highpass filter with a corner frequency around 1MHz while the upper cutoff frequency defined by C_L and $ro_1//ro_3$ is set around 2.5MHz. To overcome PVT variations, both Cd and C_L are designed to be 4bits programmable capacitor arrays.

With four identical IF amplifiers DC-connected with each other, a total gain of more than 73dB is produced across the pass band, consuming 1μA for each stage. Figure 4.9 plots the simulated frequency response of the complete IF amplifiers. Conner simulations were run to make sure that by tuning the capacitor array, a 1MHz bandpass filter is always guaranteed and the amplification would have sufficient gain under the worst conditions. The -3 dB bandwidth marked in figure 4.9 verifies that the IF amplifier has high gain across the band from 980kHz to 2.05MHz, with a peak gain of 76dB. When combining matching network, passive mixer, IF LNA together with this four-stage IF amplifier, the receiver frontend provides more than 105dB total gain with a noise figure of 13.5dB.

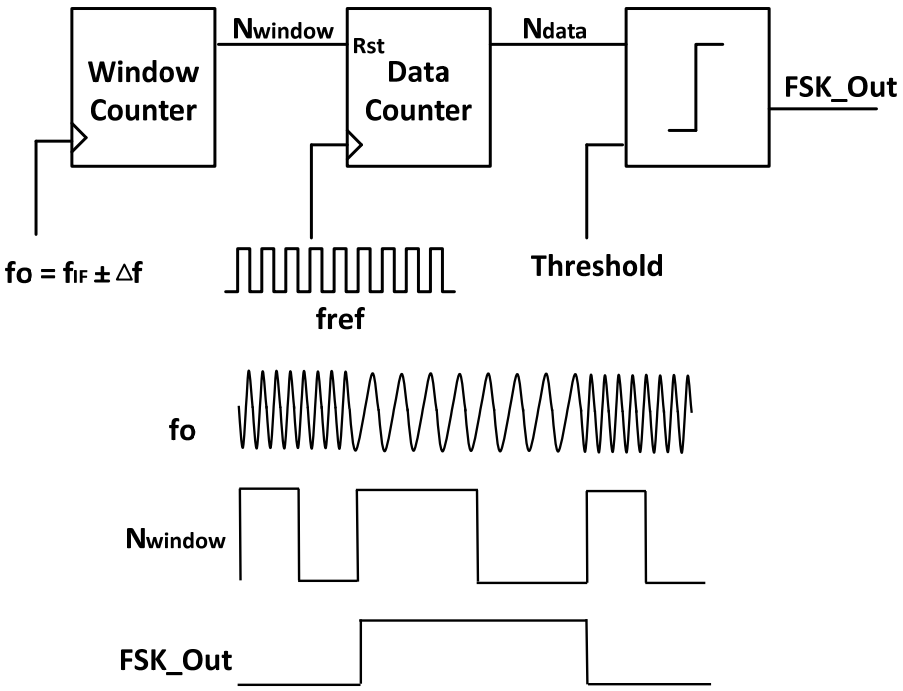

Figure 4.10 Digital FSK Demodulator

After four-stage amplification, a self-biased differential amplifier converts the differential signal to a single-ended one and it is ac coupled to a resistor divider so as to set the DC bias point at mid-rail (250mV), as shown in figure 4.7. Then following inverts help to gain the input up to a rail-to-rail digital FSK signal which could be used in the digital demodulator. Large resistors are preferred such that the divider consumes negligible current meanwhile proper capacitor value is chosen so as not to affect the bandwidth of IF amplification.

4.2.3 Digital Demodulator

Instead of demodulating FSK data in baseband, an IF digital FSK demodulation scheme [Pandey11] is adopted in this receiver design. Figure 4.10 explains the operation of the digital demodulator. The IF output is fed into the "window" counter which operates for N_{window} cycles and gates the "data" counter. A 36MHz clock divided from the FBAR injection locked oscillator is fed into the "data" counter as the reference clock. Obviously, within one measurement window

$$T_{window} = \frac{N_{window}}{f_o} = \frac{N_{data}}{f_{ref}} \quad => \quad N_{data} = \frac{f_{ref}}{f_o} N_{window} \tag{4.6}$$

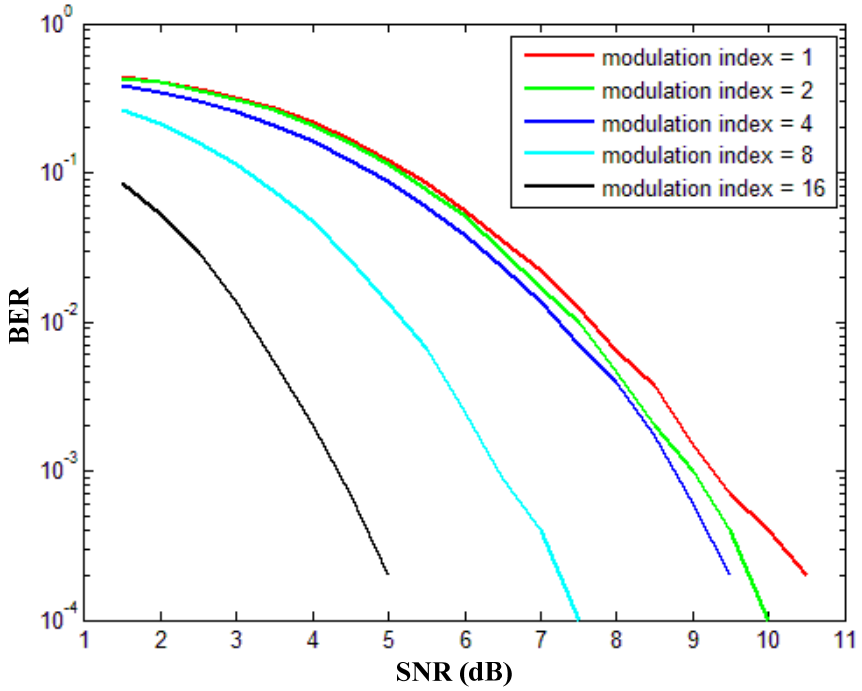

Figure 4. 11 BER Vs SNR for FSK Demodulator with Different Modulation Index

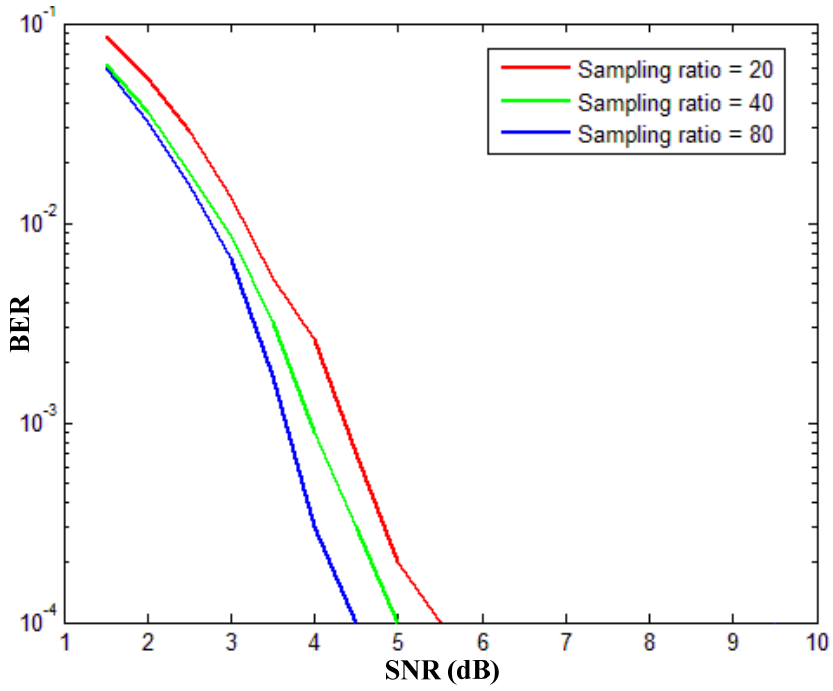

Figure 4.12 BER Vs SNR for FSK Demodulator with Different Sampling Ratio

where N_{window} is the predefined window cycles and N_{data} is the data counter output

A change in the IF frequency will change the N_{data}, therefore the FSK modulated IF signal can be demodulated according to the changes in N_{data}. The resolution of this demodulation scheme is determined by

$$\Delta N_{data} = \left(\frac{f_{ref}}{f_{IF} - \Delta f} - \frac{f_{ref}}{f_{IF} + \Delta f}\right) N_{window} \cong \frac{2\Delta f}{{f_{IF}}^2} \times f_{ref} \times N_{window} \quad (4.7)$$

To correctly demodulate the data

$$T_{window} < \frac{1}{2f_b} \quad (4.8)$$

where f_b is the baseband data rate. Combining (4.7) and (4.8) together

$$\Delta N_{data} < \frac{\Delta f}{f_b} \times \frac{f_{ref}}{f_{IF}} \quad (4.9)$$

Therefore, the resolution of the scheme is related to the modulation index ($\Delta f/f_b$) and the sampling ratio (f_{ref}/f_{IF}). A matlab FSK demodulator model is built to verify the effects of these two design parameters. Figure 4.11 presents the effect of modulation index. Clearly with an increase in modulation index, the minimum required SNR to achieve 10^{-3} BER is reduced. Thus in order to achieve high sensitivity, a high modulation index should be chosen. As the typical bandwidth of FBAR matching network is around 1~2 MHz and required baseband data rate is 50 kHz, the modulation index is designed to be 16. Figure 4.12 shows the effect of sampling ratio. When the sample ratio is increased from 20 to 80, the required SNR is slightly improved. However high sample ratio stands for high power consumption, therefore in this demodulator a low sample ratio of 24 is chosen with IF frequency designed to be 1.5MHz.

4.2.4 Frequency Divider

As described previously, a reference clock of 36MHz is used in the FSK demodulator. This clock is acquired from the division of FBAR injection locked oscillator, thus a frequency divider with dividing ratio of 25 is required in the design. As shown in figure 4.13, two "divide by 5" cores cascade together to form dividing by 25. For power saving purpose, the first core is designed with LVT devices while the second one is designed with SVT devices.

Figure 4.14 shows the schematic of the core. The middle devices form a five-stage ring oscillator which is controlled by Clkin through top PMOS and bottom NMOS. At each

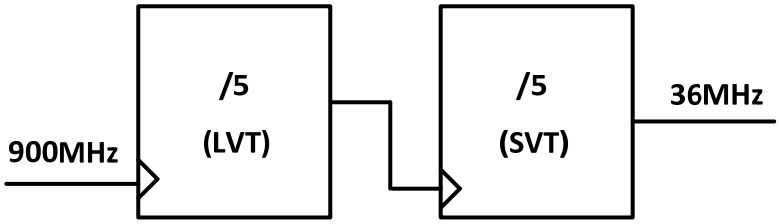

Figure 4.13 Frequency Divider

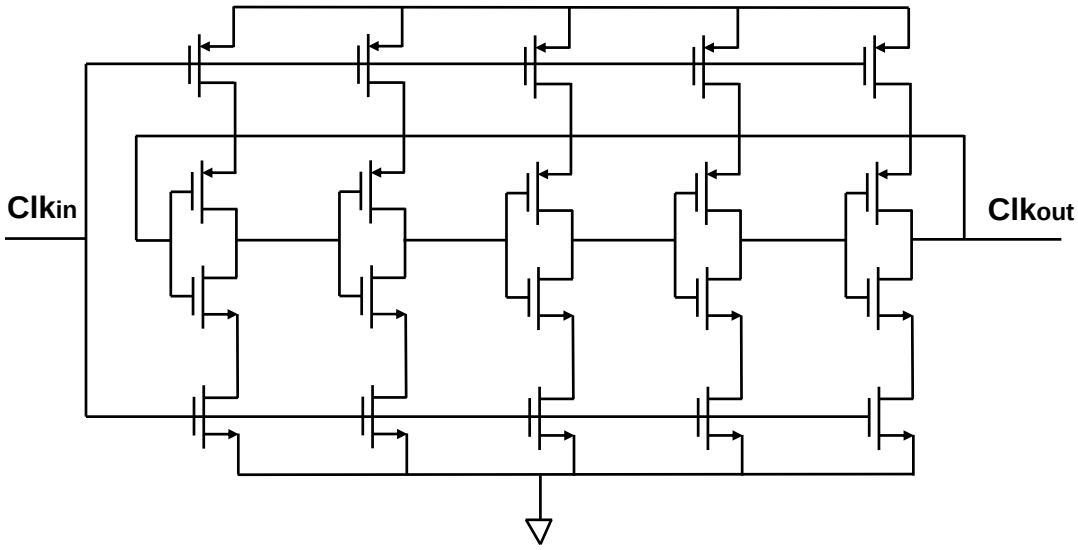

Figure 4.14 Schematic of Dividing by 5 Core

rising/falling edge of Clkin, a single inverter stage operates and it will not propagate to the second stage until next falling/rising edge. Therefore the inverter delay is controlled by half cycle of Clkin and the five-stage ring oscillator performs as a divider with dividing ratio of five. The power consumption of the frequency divider is low, with only 3μW cross all the corners.

4.2.5 Baseband Synchronization

To correctly decode the wake-up frame, baseband synchronization is required. A digital synchronizer based on 16 bits preamble is proposed in this prototype. Figure 4.15 presents its working scheme. It utilizes the 36MHz reference clock to sample the baseband data. By detecting the rising and falling edge, the correct data sample is in the middle between two edge samples. An average of 8 data samples is included so as to eliminate the effect of jitter. The resolution of proposed synchronizer is given by

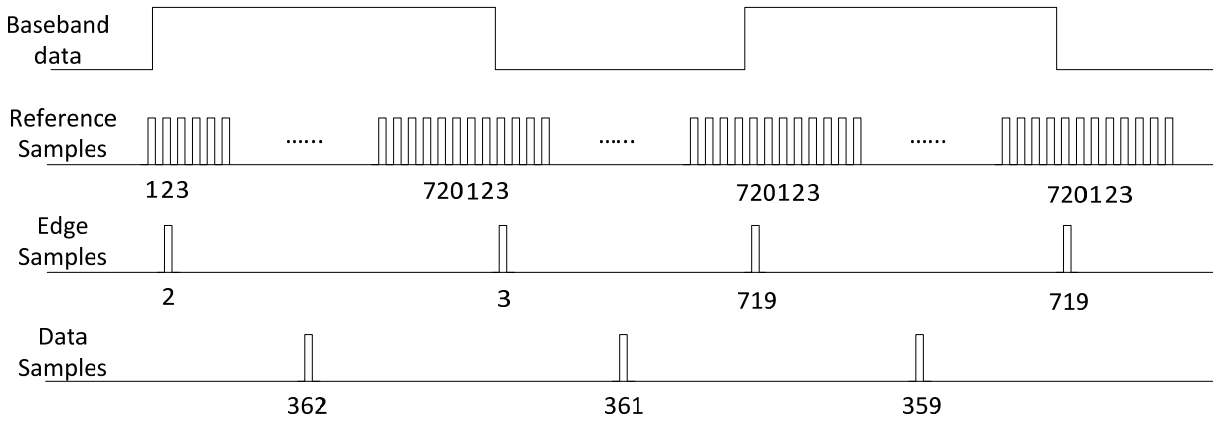

Figure 4. 15 Scheme of Digital Synchronization

$$\text{Err} < \frac{\frac{1}{f_{ref}}}{2 \times \frac{1}{f_b}} = \frac{f_b}{2f_{ref}} \tag{4.10}$$

where f_{ref} is the reference clock frequency (36M) and f_b is the baseband datarate (50k). The resolution is better than 0.07%. When decoding 32bits of device address in the wake-up frame, the clock sample only drifts by 2.23%. Therefore, timing synchronization based on preamble is enough to extract the correct data sample for detecting reset of the wake-up frame.

4.3 Summary

This chapter presents a detailed description of designing a FSK receiver. For integration complexity consideration, the FSK receiver shares parts of the frontend circuitry with the energy detection receiver and the rest circuit blocks have been discussed in details. It has shown that with modulation index of 16 and oversampling of 20, the minimum required SNR to achieve 10^{-3} BER is around 5dB. Together with 13.5dB frontend noise figure and 2MHz IF bandwidth (given some margin for tuning), the receiver is able to achieve a sensitivity of -92dBm.

Chapter 5

Measurement Result

The wake-up receiver prototype is fabricated in TSMC 65nm standard digital CMOS. As shown in figure 5.1, the chip die size is 1.2 mm^2 and it is limited by pad for testing purposes. By using a standard chip-on-board (COB) technique, the CMOS die is glued onto the circuit board and wirebonds are made directly from the chip pads to the landing sites on the PCB. The packaged resonators are also connected to the CMOS die using wirebonds. Two resonators are required for this design with one for the matching network and the other for the FBAR oscillator. Figure 5.2 shows a magnified view of the active die area. The area devoted to active circuitry is small with an area of 0.1 mm^2. The majority of the area is taken by MOM capacitors used in integrator design.

5.1 Frequency Response

The response of input matching network $|S_{11}|$ as well as the energy detection receiver's overall RF-to-baseband gain response versus frequency is plotted in figure 4.3. When measuring the gain frequency response, the reset switch in integrator is turned off such that it works as a low pass filter. Since the resonator bandwidth is much lower than the receiver's, the gain frequency response is mainly dominated by the resonator. Input $|S_{11}|$ is measured to be -11.4dB. Although it is not as well-matched as expected, the quality of the match is sufficient for testing. The peak RF-to-baseband gain occurs at 914.2MHz on the parallel resonance of the FBAR with a -3dB bandwidth around 2MHz. Therefore, the quality factor (Q) of the matching/filtering network is about 457. Compared to the Q of the FBAR resonator which is more than 2000, parasitics detune the network substantially. The gain frequency response also manifests an asymmetric response at parallel resonance of the FBAR. It has higher filtering capability at the left side rather than the right side. Thus for the address detection receiver design, it is better to choose LO less than the parallel resonance frequency such that the image problem can be further eliminated.

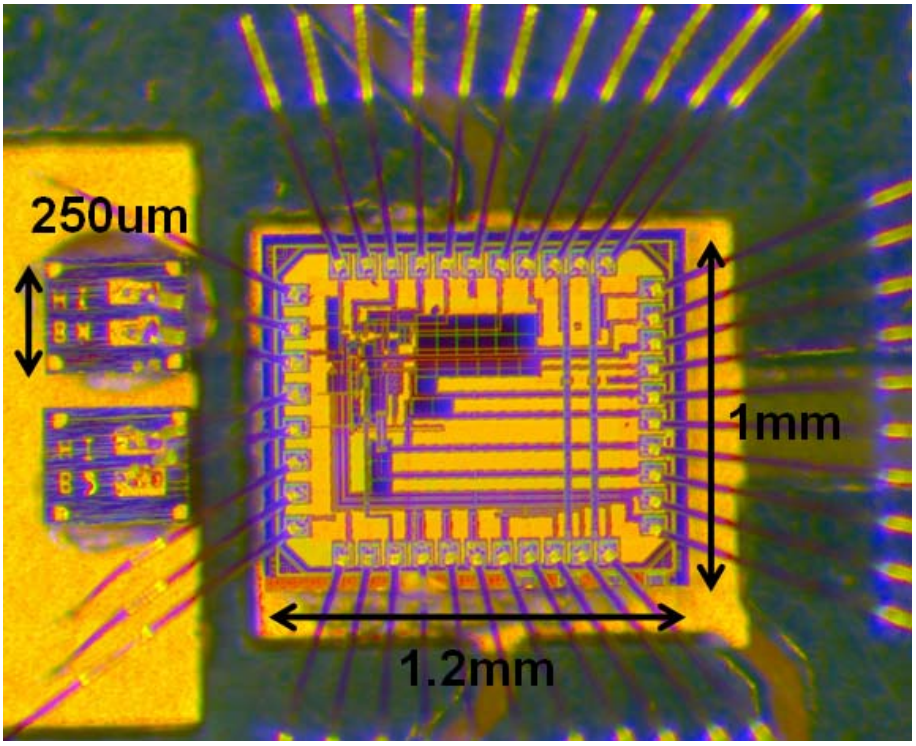

Figure 5.1 Die Photo of Receiver Prototype Bonded to Packaged FBAR Resonators

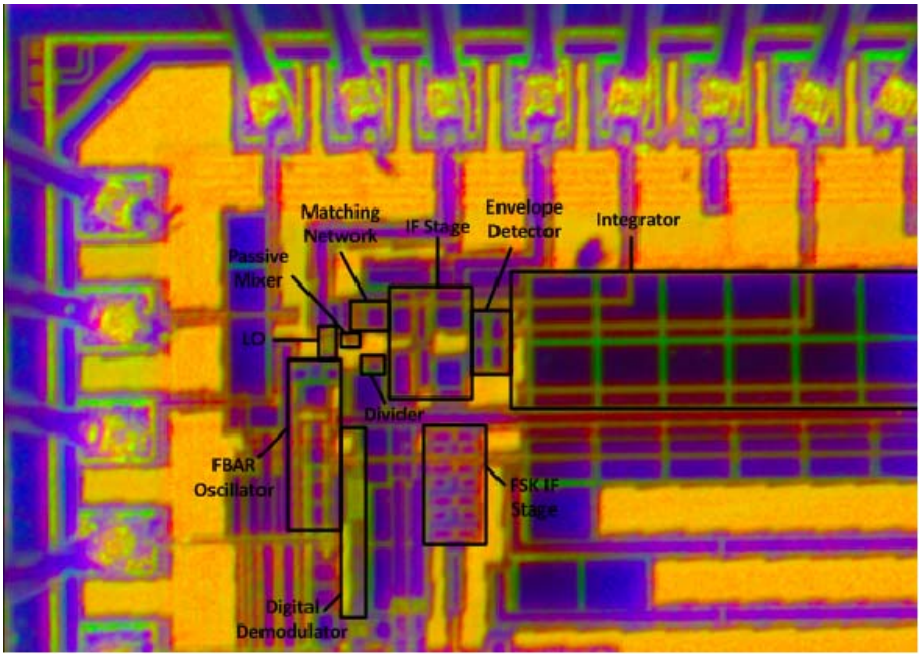

Figure 5.2 Annotated Die Photo

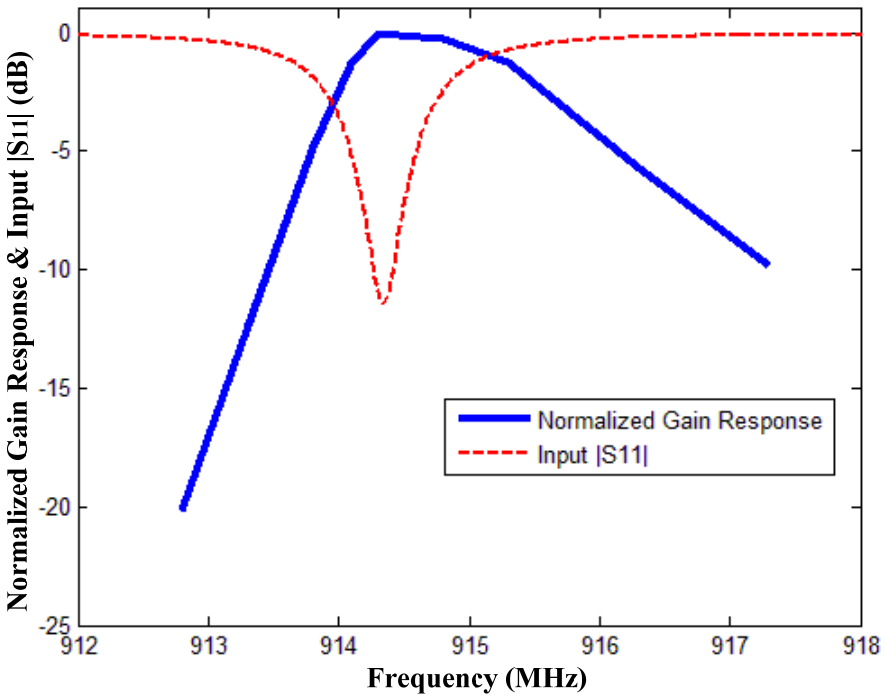

Figure 5.3 Measured $|S_{11}|$ and Gain Frequency Response

5.2 LO Measurement

To measure the LO generation in various operating modes, extra LO buffers along with an open drain buffer are implemented on chip to drive an off-chip 50 ohm instrument. Figure 5.4 presents the measurement result of the free running three-stage ring oscillator. With its bias current varying from 27μA to 46μA, the frequency of the ring oscillator can be tuned linearly from 700MHz up to 1.1GHz. Especially at 915MHz, it draws 36μA from 0.5V voltage supply including biasing network and mixer driving.

Figure 5.5 demonstrates the performance improvement of the injection locking oscillator. Since the cross couple branches of the ring oscillator are broken up in this mode, the ring oscillator itself consumes 6μA less current. However it dissipates an extra 490μA to start the FBAR oscillator for injection locking. When the oscillator is free running, its spectrum can be seen to "wander" during operation, with its center frequency moves around by roughly 5MHz. In addition, a large amount of phase noise from the ring oscillator can be seen from this measurement as a wide range of energy presents near the center frequency. However when the oscillator is injection locked to the FBAR oscillator, it presents a stable oscillation frequency with a smaller frequency span and its phase noise performance has

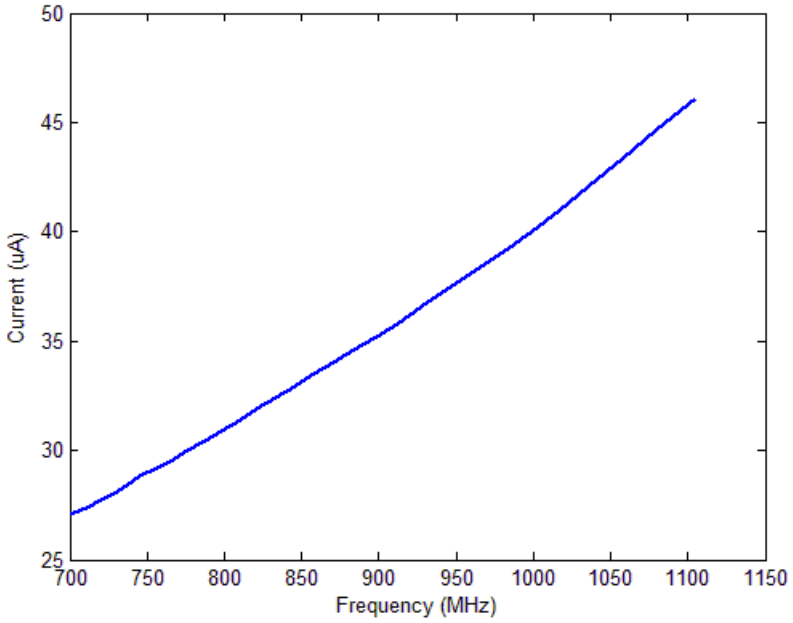

Figure 5.4 Measurement Result of Three-Stage Ring Oscillator

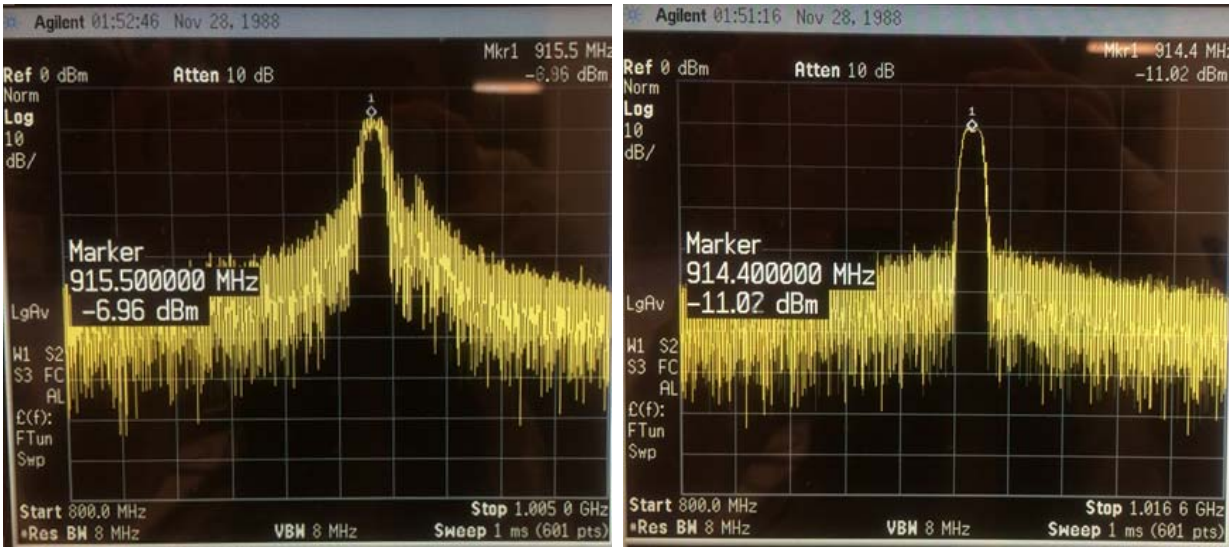

Figure 5.5 Output Spectrum When Oscillator is (left) Free Running and (right) Locked.

been largely improved. Therefore with a total power consumption of 260μW, the ring oscillator is locked to the FBAR oscillator and a clean and stable carrier frequency can be obtained to use in the FSK demodulation.

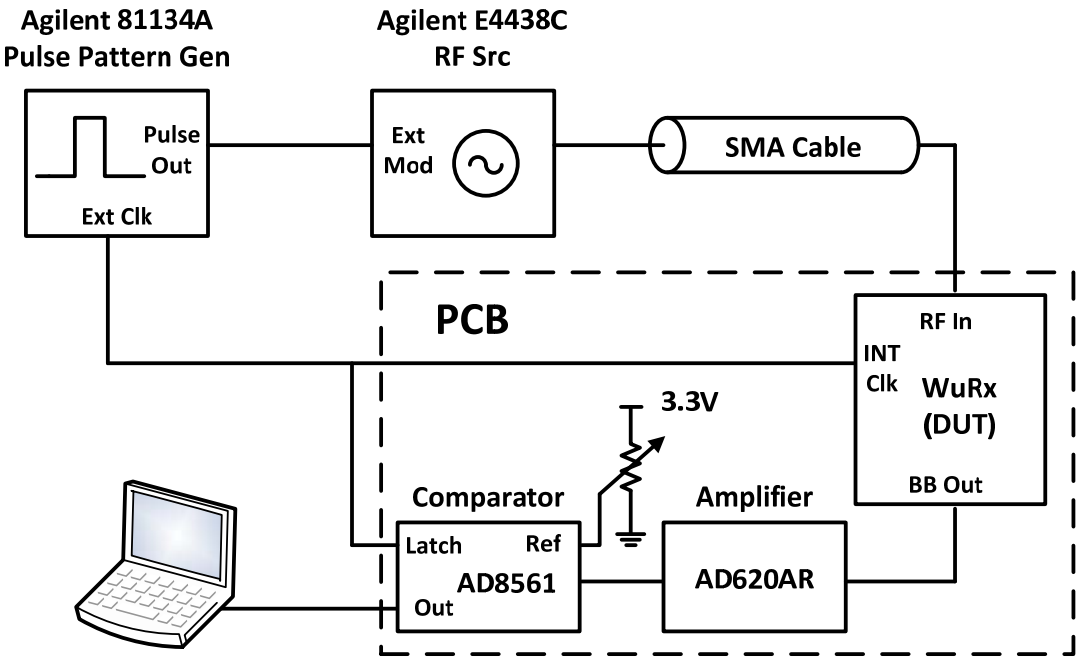

Figure 5.6 Test Setup for P_{FA} and P_{MD} Measurements in Energy Detection Mode

5.3 Receiver Sensitivity in Energy Detection Mode

The receiver sensitivity is measured by modulating the input RF carrier with an OOK bit sequence. Probability of false alarm (P_{FA}) is measured by sending a bit sequence of '0' while probability of miss detection (P_{MD}) is measured by sending a bit sequence of '1'. To drive the off-chip loads, a single stage buffer is included on chip, designed to provide 10 dB of gain while driving off-chip loads up to 15pF. As the buffer is for measurement purposes only, it operates from the 1.2V pad ring supply voltage. An additional tunable 20 dB of gain is provided by a commercial op-amp on the PCB before slicing the raw waveform to generate digital bits. The digital bits are recorded and analyzed through matlab to generate two error rates. An external reference voltage is used as the threshold for slicing. It is tuned to make sure that probability of false alarm and probability of miss detection equal to each other so as to meet the error rate requirement defined in chapter 2. The complete setup for sensitivity measurement is shown schematically in figure 5.6.

Figure 5.7 displays the measured average error rates ((P_{FA}+P_{MD})/2) versus sensitivity of the receiver for different power consumptions. Decision threshold is turned to ensure that P_{FA} equals P_{MD}. With 20µs integration time and 45µW power dissipation (solid red curve),

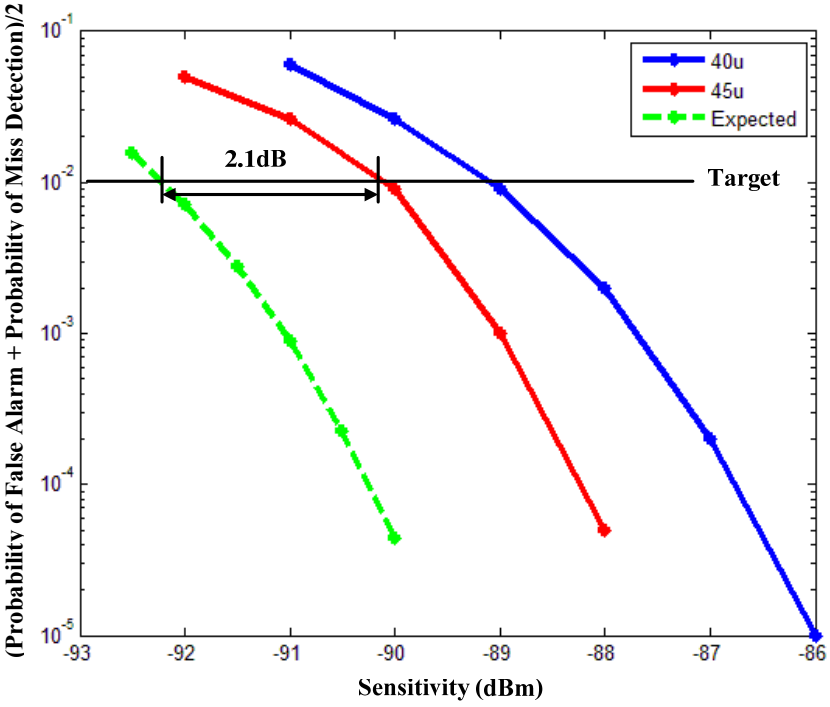

Figure 5.7 Measured Error Rate versus Sensitivity for Different Power Consumption

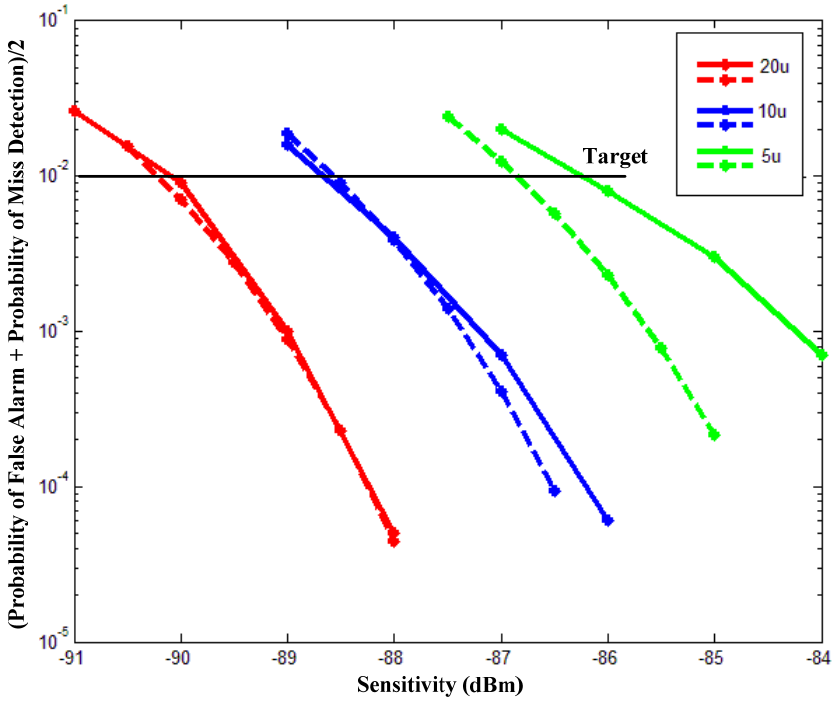

Figure 5.8 Measured Error Rate versus Sensitivity for Different Integration Time

the receiver is able to achieve a sensitivity of -90dBm for 10^{-2} P_{FA} and 10^{-2} P_{MD}. The measured value is pretty close to the expected sensitivity performance (dotted green curve) described in chapter 3, with roughly 2dB difference. This is mainly due to the difference in parameter estimation of FBAR resonators and the process variation of the CMOS transistors. These differences make the frontend noise figure higher than we have expected. If total power dissipation reduces to 40μW (solid blue curve), with 5μW less power spent on the IF LNA, the sensitivity performance would be dropped by 1dB.

Figure 5.8 shows the measured error rates versus sensitivity for different integration time. Solid curves represent the measured data and dotted curves represent the expected performance shifted by 2dB due to an increase in the frontend noise figure. Obviously with 20μs and 10μs integration time, the measurement results match the expected performance really well. However with 5μs integration time, differences occur which is mainly due to the bandwidth limit of the integrator. When integration time is dropped from 20μs to 10μs and 5μs, the receiver sensitivity is reduced from -90dBm to -88.5dBm and -86.5dBm respectively. This result closely matches the performance boundary analysis in chapter 3 that the sensitivity performance is dropped every 1.5dB when decreasing the integration time by two times.

5.4 Receiver Sensitivity in Address Detection Mode

In address detection mode, the receiver sensitivity is measured by modulating the input RF carrier with a FSK pseudorandom bit sequence and checking the bit error rate (BER) at baseband output. Unfortunately the performance of the FBAR resonators donated by Avago Technology is away from what we expected, thus all the parasitic capacitances associated with FBAR oscillator drift the LO away from the desired frequency. Instead of having a designed IF frequency at 2 MHz, a 450 kHz IF is actually required. To achieve the best performance with this low IF frequency, a different modulation index of 6 is applied with two IF FSK frequencies at 300 kHz and 600 kHz respectively. A similar digital demodulator with narrow pulse filtering and dual decision threshold as shown in figure 5.9 is implemented in FPGA so as to reduce the noise affect. The demodulated data is recorded and analyzed in matlab to generate BER result. The complete schematic of sensitivity measurement setup is shown in Figure 5.10.

Figure 5.11 presents the measured BER versus sensitivity of the receiver. The receiver is able to achieve a sensitivity of -74.5dBm for 10^{-3} BER. Compared to the design target, the measurement result is more than 15dB worse from the expectation. This is due to two main reasons. Firstly, according to figure 4.11, a change in modulation index from 16 to 6 causes additional 4dB in the minimum required SNR. Secondly, the low cutoff frequency of the IF

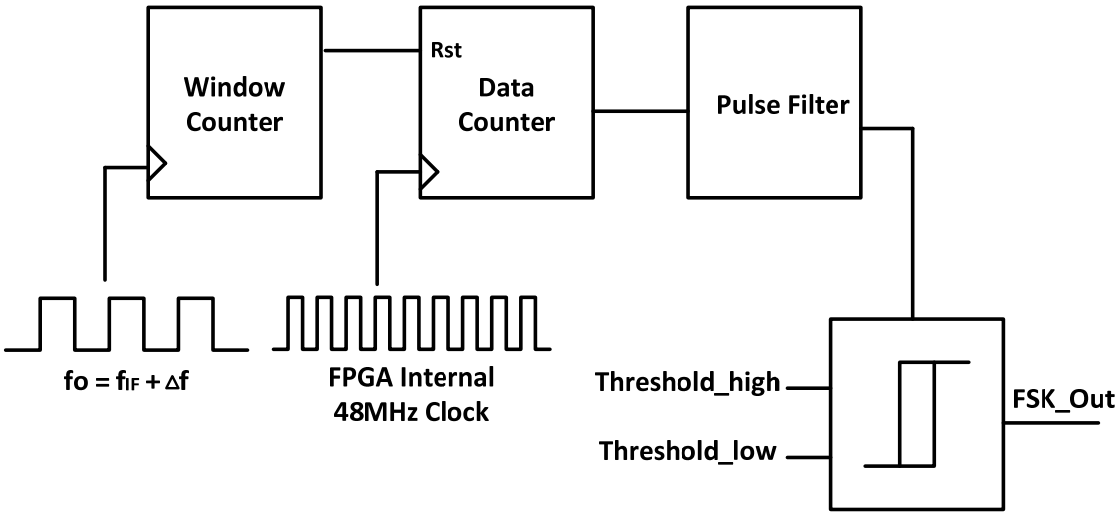

Figure 5.9 Revised FSK Demodulator Implemented on FPGA

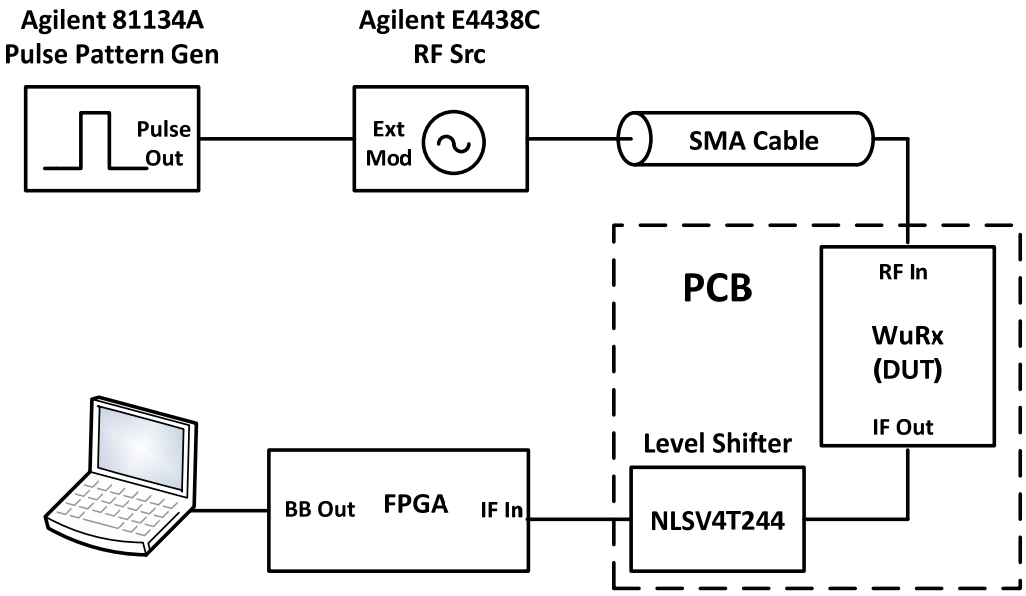

Figure 5.10 Test Setup for BER Measurement in Address Detection Mode

LNA is around 800kHz while the actual two IF frequencies are at 300kHz and 600kHz. This means that the frontend noise figure is much higher due to low frequency filtering in IF LNA. According to the simulation, the noise figure is 23dB integrated from 300kHz to 600kHz which is 10dB higher than the original design.

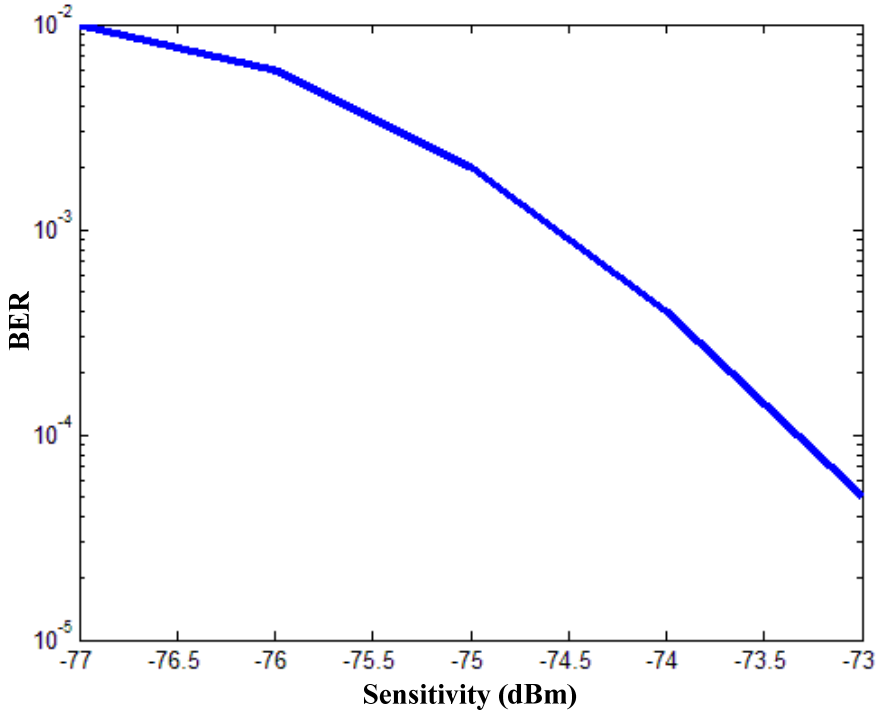

Figure 5.11 Measured BER versus Sensitivity

5.5 Performance Summary

In energy detection mode, the total power consumption of the receiver is 45μW from the 0.5V voltage supply. The LO generation including buffers for mixer driving and the IF LNA consume more than 91% of the total power budget, with 18μW and 23μW respectively. The rest of the circuitry including two stages IF amplifiers and integrator consume another 4μW. The power consumption breakdown is shown graphically in figure 5.12. The complete receiver performance is summarized in table 5.1 and is compared with state-of-the art low power receivers in table 5.2. Clearly, our proposed receiver stands out in terms of ultra-low power consumption and excellent sensitivity performance. The key innovation of this receiver design is to take advantage of "wideband-IF" concept together with "noise averaging". By adopting "wideband-IF", it utilizes low power ring oscillator for LO generation so as to shift the signal amplification from RF to IF side which results in a huge amount of power saving. Meanwhile, it also adopts "noise averaging" concept to eliminate the effect of wideband noise caused by "wideband-IF" so as to improve the sensitivity to the desired number. The proposed technique can also be used in ultra-low power OOK receiver design so as to achieve better sensitivity performance.

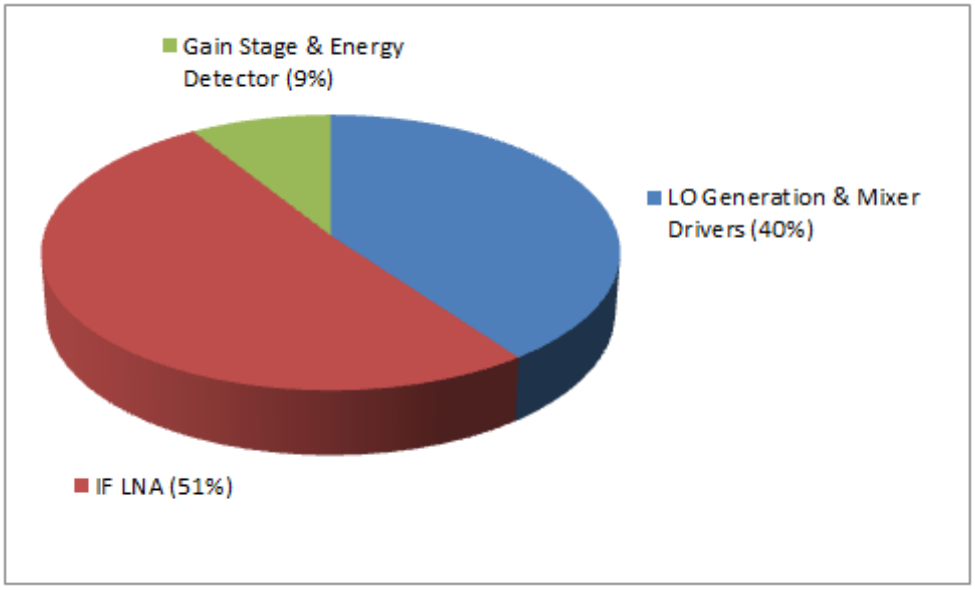

Figure 5.12 Receiver Power Breakdown in Energy Detection Mode

Table 5. 1 Performance Summary of Receiver in Energy Detection Mode

Parameter	Measurement	
Voltage Supply	0.5V	
Carrier Frequency	915MHz	
Active Power Consumption	45μW	
LO Generation & Mixer Driver	18μW	
IF LNA	23μW	
IF Amplifiers	3 μW	
Integrator	1 μW	
Detection Time	20us	
Minimum Frame Length	2 bits	
Sensitivity	-90dBm	-89dBm
Probability of False Alarm	10^{-2}	10^{-3}
Probability of Miss Detection	10^{-2}	10^{-3}

Table 5.2 Performance Comparison of Energy Detection Receiver

	[Pletch09]	[Huang10]	[Huang12]	[Nadeau12]	This Work
Technology	90nm	90nm	90nm	180nm	65nm
Carrier Frequency	1.9GHz	915MHz	915MHz	2.4GHz	915MHz
Power Consumption	52μW	51μW	120μW	180μW	45μW
Detection Time	10μs	100μs	100μs	1μs	20μs
Sensitivity for $(P_{FA}+P_{MD})/2 = 10^{-3}$	-72dBm	-80dBm	-83dBm	-67dBm	-89dBm

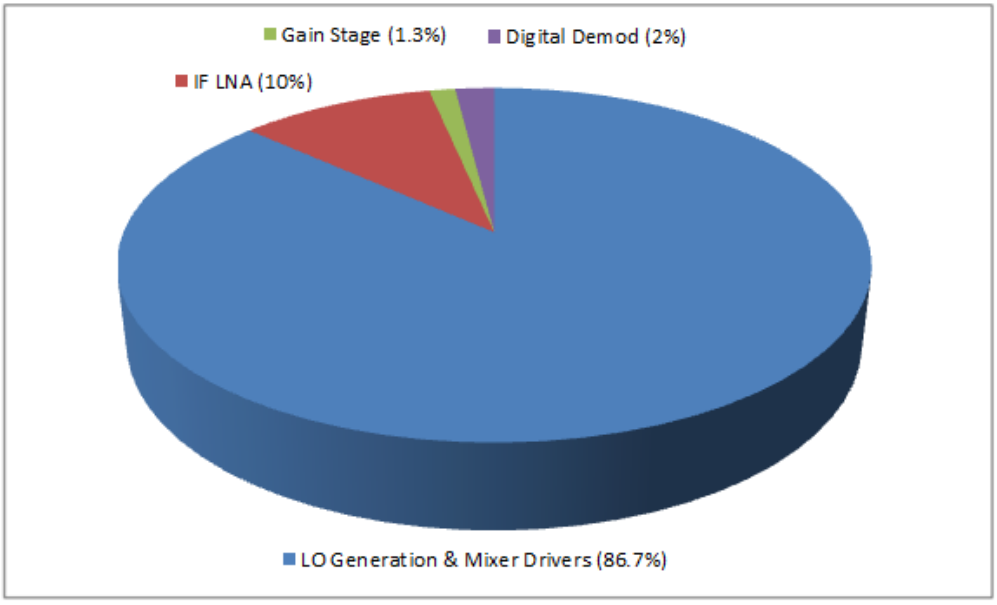

Figure 5. 13 Receiver Power Breakdown in Address Detection Mode

In address detection mode, the total power consumption of the receiver is 300μW from the 0.5V voltage supply. The power consumption breakdown is shown graphically in figure 5.13. As shown in the figure, more than 86% of the total power is consumed by the LO generation, with most of it spent on the FBAR oscillator. The power consumption of a FBAR oscillator is related to the parallel impedance of the resonator. The parallel impedance of the resonator we get is around 1.5k, yet with the development of MEMS technology it can be improved up to 7k [Nelson11], thus the power dissipation of the receiver can be significantly reduced. For the rest of the circuitry, the IF LNA consumes 30μW with an additional 7μW than in energy detection mode so as to improve the sensitivity performance. The IF gain stages consume 4μW and the digital demodulator together with frequency divider consume another 6μW. Besides sensitivity testing, digital synchronization described in chapter 4 is also implemented in FPGA to perform a functionality check of wake-up frame detection. The complete receiver performance is summarized in table 5.3 and is compared with state-of-the art low power FSK receivers in table 5.4. The result in address detection mode is not as promising as in energy detection mode. This is due to the mismatch of two FBAR resonators, the resulting IF frequency is out of the IF LNA bandwidth. However it demonstrates the possibility of building a low power FSK receiver with our proposed architecture.

Table 5. 3 Performance Summary of Receiver in Address Detection Mode

Parameter	Measurement
Voltage Supply	0.5V
Carrier Frequency	915MHz
Active Power Consumption	300μW
LO Generation & Mixer Driver	260μW
IF LNA	30μW
IF Amplifiers	4 μW
Digital Demodulator & Divider	6 μW
Data Rate	50kbps
Frame Length	50 bits
Preamble	16bits
Unique Address	32bits
End of Frame	2bits
Sensitivity	-74dBm
BER	10^{-3}

Table 5. 4 Performance Comparison of Address Detection Receiver

	[Cook06]	[Bae09]	[Bae10]	[Pandey11]	This Work
Technology	130nm	180nm	180nm	130nm	65nm
Carrier Frequency	2.4GHz	400MHz	915MHz	400MHz	915MHz
Power Consumption	330μW	490μW	420μW	44μW	300μW
Data Rate	N/A	250kbps	5Mbps	200kbps	50kbps
Sensitivity for BER = 10^{-3}	N/A	-70dBm	-73dBm	-70dBm	-74dBm

Chapter 6

Conclusions and Future Work

6.1 Research Summary

This dissertation focuses on the architecture and the implementation of an ultra-low power wake-up radio for low activity wireless links. It starts with exploring the high level design considerations and defines the system specifications for implementing a wake-up radio prototype for IEEE 802.15.4g. For reliability and power saving purposes, a two-step wake-up architecture has been proposed including energy detection mode and address detection mode. This architecture relies on low power energy detection mode to achieve ultra-low average power consumption while utilizing address detection mode to enhance the robustness of the wake-up radio. Design metrics in terms of power and latency performance optimization have been provided which serves as a guideline for receiver implementations.

Following that, detailed circuit design of two-step wake-up radio has been presented. In energy detection mode, the receiver architecture adopts "wideband-IF" concept to utilize a low power ring oscillator instead of a LC oscillator for LO generation which results in huge power saving to satisfy the power budget. Meanwhile, it also applies "noise averaging" concept to reduce the excess noise generated by "wideband-IF" so as to improve the receiver sensitivity to the desired number. A detailed theoretical analysis has been provided and performances with different conditions of design parameters have been discussed. The silicon measurement result matches the theoretical expectation pretty well. With 45μW power consumption and 20μs detection time, the energy detection receiver is able to achieve a sensitivity of -90dBm at 10^{-2} target for both false alarm and miss detection error rates. This has demonstrated the possibility of building an ultra-low power radio while maintaining high sensitivity performance.

In address detection mode, a FSK receiver is implemented. It utilized injection locked FBAR oscillator to provide stable and low phase noise frequency reference for FSK demodulation.

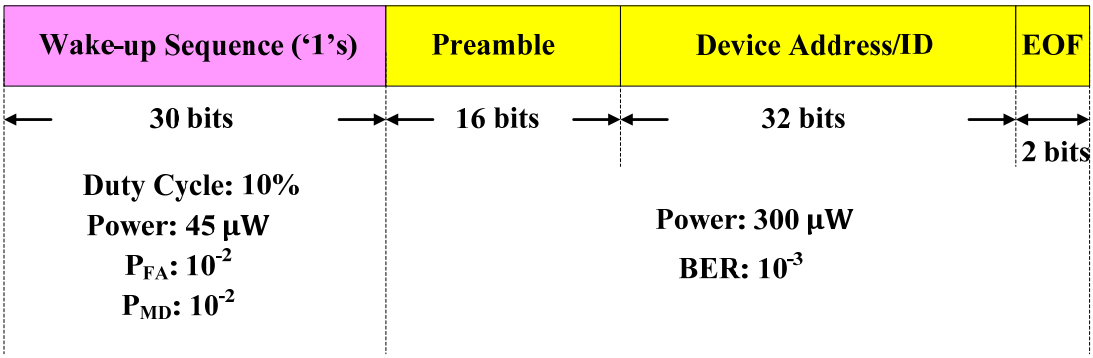

Figure 6.1 A Novel Wake-up Frame Design Example

The resulting radio consumes a total of 300µW to receive 50kbps of data stream with a sensitivity of -74.5dBm at 10^{-3} BER. It is believed that with better matching between two FBAR resonators (one for matching network and another one for FBAR oscillator) to generate correct IF frequency, another 10~ 15dB improvement in sensitivity could be achieved.

6.2 Future Work

The motivation to push the power consumption of wake-up radio further down is likely to continue in the future so as to extend its application integrated with energy harvesting devices. In the current prototype design, the energy detection receiver dominates the average power consumption. To guarantee correct energy detection, it requires two bits in the wake-up frame which is only a small portion compared to 50 bits used for device address checking. Therefore, by increasing the bits number in wake-up frame and duty-cycling the energy detection receiver, the average power consumption could be largely reduced with reasonable delay punishment. Figure 6.1 shows a design example. The wake-up sequence is increased from 5 bits to 30 bits, introducing additional 45% in wake-up latency. However with 3 bits assigned for one detection (one bit for starting up oscillator and two bits for performing energy detection), the energy detection receiver could be duty-cycled as low as 10%. According to (2.1), the average power consumption is decreased from 48µW to 8.5µW, performing more than 82% power reduction.

From the architectural standpoint, one of the limitations of using the wake-up radio remains that current design is fixed to a single channel, limiting its ability to deal with interference. Figure 6.2 shows one possible way to solve the limitation by taking advantage of small sized MEMS resonators. Rather than building a single channel, multiple resonators are used to provide separate frontend filter path. This solution helps to mitigate the

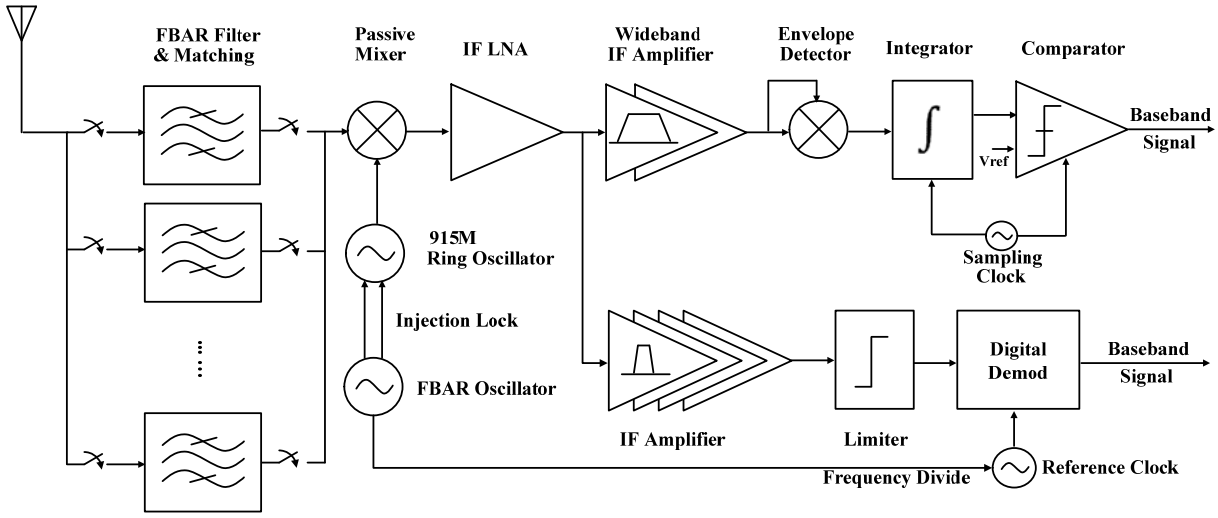

Figure 6.2 MEMS Based Multi-channel Wake-up Radio

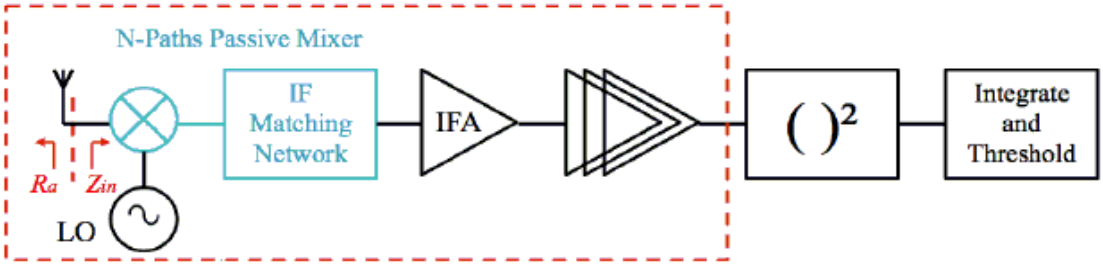

Figure 6.3 Crystal-less Energy Detection Receiver

interference problem without extra power cost.

From the integration and cost standpoint, the use of MEMS resonators is another limitation. To get rid of the off-chip components meanwhile maintaining the same quality fact (Q) of the MEMS filter, an N-path passive mixer based frontend can be adopted in the wake-up receiver design as shown in figure 6.3 [Salazar13]. Due to the "transparency" of the passive mixer, the IF/baseband filter is translated to the RF band-pass filter and its center frequency can be turned by the LO frequency. A preliminary result shows that with a 2-paths passive mixer architecture, the frontend filter is able to achieve a Q of 300 which is comparable to that of a MEMS filter.

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