Demonstration of an Optical Chip-to-Chip Link in a 3D Integrated Electronic-Photonic Platform

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Demonstration of an Optical Chip-to-Chip Link in a 3D Integrated Electronic-Photonic Platform

by Sen Lin

Research Project

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Second Reader

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Abstract

A full optical chip-to-chip link is demonstrated for the first time in a wafer-scale heterogeneous platform, where the photonics and CMOS chips are 3D integrated using wafer bonding and low-parasitic capacitance thru-oxide vias (TOVs). This development platform yields 1000s of functional photonic components as well as 16M transistors per chip module. The transmitter operates at 6Gb/s with an energy cost of 100fJ/bit and the receiver at 7Gb/s with a sensitivity of 26μA (-14.5dBm) and 340fJ/bit energy consumption. A full 5Gb/s chip-to-chip link, with the on-chip calibration and self-test, is demonstrated over a 100m single mode optical fiber with 560fJ/bit of electrical and 4.2pJ/bit of optical energy.

Chapter 1

Introduction

Silicon photonics holds great promise in replacing conventional optical interconnects and electrical interconnects in today's data centers as the bandwidth demand keeps growing. In particular, optical links based on silicon photonics are one of the most promising candidates for the next-generation 400G inter-rack interconnects and 100G intra-rack interconnects in data centers. Recent years have seen great efforts and rapid progress in developing and commercializing silicon photonics technologies from platforms, devices, circuits to systems [1–6]. Optical links based on silicon photonics can achieve lower energy and higher bandwidth density over traditional electrical I/O. Additionally, optical links benefit from distance insensitivity due to the inherently low loss of fibers, allowing for new types of connectivity and network organization in modern digital systems and data-centers. Wavelength-division multiplexing (WDM) may also be realized to place many data channels on a single optical fiber, thereby increasing the bandwidth density while retaining energy efficiency and breaking the I/O pin limitations imposed by the electronics.

To enable full optical links for interconnection networks, high speed and low power optical transmitters as well as high bandwidth and high sensitivity optical receivers are required. These necessitate the need for close integration in order to achieve small parasitic capacitance between electronics and photonic devices. Furthermore, a two-wafer solution is desirable to separately optimize the performance of the photonic components and the CMOS circuits. This work demonstrates for the first time an optical chip-to-chip link built

in a heterogeneous, 3D integration platform using thru-oxide via (TOV) technology [7]. The TOV technology overcomes the challenges of close integration of electronic and photonic components, by simultaneously enabling separate wafer optimization of electronic and photonic components while providing a low-capacitance, high-density connection between the photonic and electronic wafers.

The technical report presents a full optical chip-to-chip link demonstrated in a wafer-scale heterogeneous platform. The majority of the results in this technical report has been published and presented in [8, 9]. In the report, we first intoduce the background of silicon photonics interconnets and platforms in Chapter 2. In Chapter 3, we discuss the detailed system and circuit implementation for 3D integrated silicon photonics transceiver. We also present the measurement results for the transceiver. Full link implementation and measurement results are discussed and analyzed in Chapter 4.

Chapter 2

Background

2.1 Silicon Photonics Interconnects

Compared to conventional optical links, silicon photonics links reduce manufacturing cost dramatically as the modulators and photodetectors are fabricated on standard silicon wafers instead of very expensive III-V wafers. In addition, silicon photonics are generally compatible with CMOS processes, enabling large-scale integration between CMOS circuits and photonic devices. The integration approaches include monolithic integration and wafer-scale 3D integration. Through close integration between electronics and photonics, silicon photonics interconnects achieve high bandwidth density and high energy efficiency. Therefore, silicon photonics holds great promise in replacing conventional optics in datacenters and enhancing capability of CMOS applications as transistor scaling slows down.

On the transmitter side, three types of silicon photonic modulators are of most interest, including microring modulator (MRM), Mach-Zehnder modulator (MZM) and electro-absorption modulator (EAM). Microring modulators and EAMs are much more energy efficient than MZMs due to their compact sizes. As a resonant device, microring modulator has inherent wavelength selectivity and it has unmatched potential for high-speed dense wavelength division multiplexing (DWDM) links. Therefore, we chose silicon microring modulators for the demostration of 3D-integrated silicon photonic interconnets.

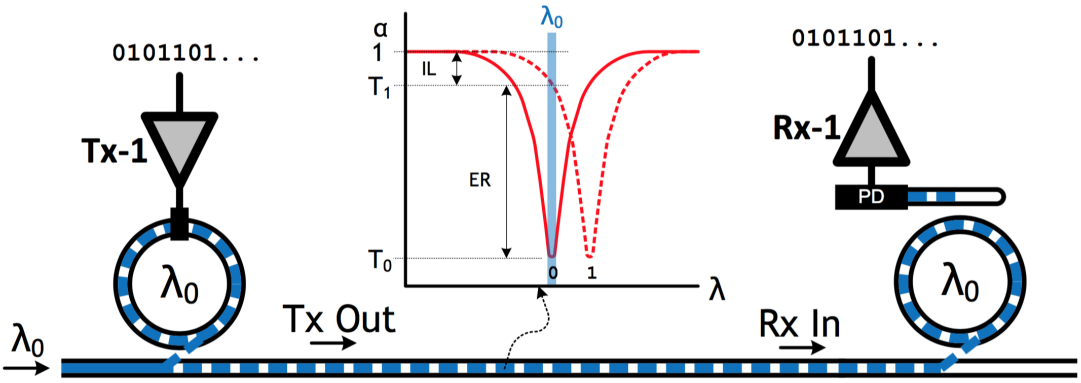

Figure 2.1: A single channel silicon photonic interconnet based on microrings.

Figure 2.1 shows a single channel silicon photonic link based on microrings. Microring modulator has a transfer function of a notch filter in the optical spectrum. It modulates the incoming light from laser by shifting its resonance in and out of the laser wavelenth. Its resonance can be shifted by high-speed voltage drivers for high data rate modulation. Besides data rate, the other two important specifications for optical transmitter are insertion loss (IL) and extinction ratio (ER) as labeled in the same figure. Small IL and high ER could help increase the optical modulation amplitude or reduce the required laser power in the link. They are the key factors for enabling full-link demonstration. In our project, the microring modulator uses a vertical pn junction design [10], which was specifically chosen for reducing IL and increasing ER.

As shown in Figure 2.1, the optical receiver can use a microring filter to receive optical signal at specific laser wavelength. Figure 2.2 shows the system diagram of a microring-based WDM optical link, where a bank of microrings are used for both transmitter and receiver. The microring modulator and filter operate in pairs as depicted in the single channel diagram. Ring tuning controls are implemented on both sides to align the resonance wavelength of the microrings and lock them to the corresponding laser wavelength. The ring tuning controls are critical to microring operations as they can calibrate process variation and compensate real-time temperature fluctations. Detailed implementation and measurement results of a microring thermal tuner are dicussed in following chapters.

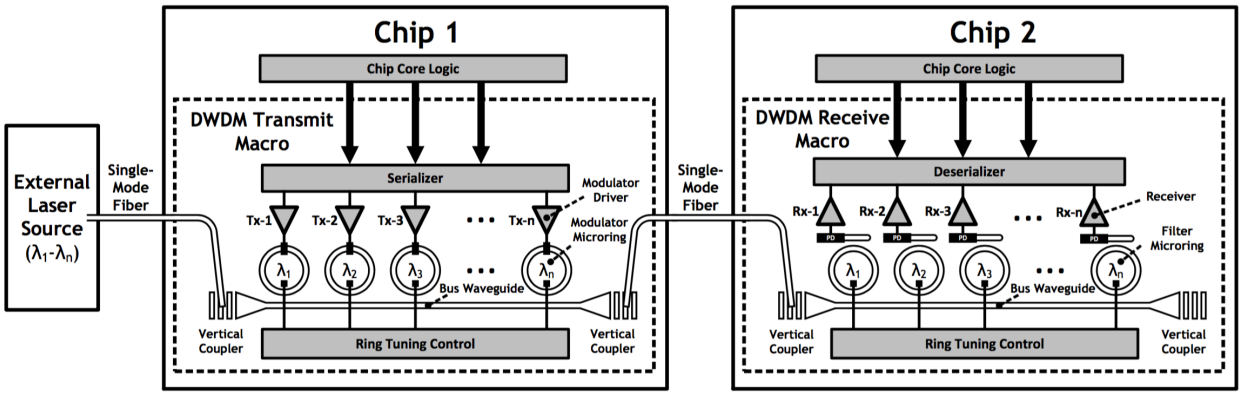

Figure 2.2: System diagram of a microring-based WDM optical link.

2.2 Silicon Photonics Platforms

Silicon photonics interconnects benefit from the close integration between photonics and electronics. The electronic-photonic platforms have two categories, monolithic and heterogeneous platforms. Monolithic integration of silicon photonics and CMOS circuits has been demonsrated in different SOI and bulk processes. One recent milestone in monolithic integration is the demonsration of first single chip computer with photonic I/O in 45nm SOI process [6].

However monolithic integration has its own limitations. First, monolithic integration of silicon photonics into the most energy efficient state-of-art CMOS processes can be expensive and technically challenging. Monolithic integration in FinFET technology has yet been demonsrated. Second, monolithic integration can sometimes imposes additional constraints on photonics design and limit the performance of photonic devices, such as the modulation efficiency of modulator and the responsivity of photodetectors.

Although electronics and photonics are still integrated closely, heterogeneous integration completely decouples photonic process from CMOS process. In this case, transistors and photonic devices can be optimized separately. This approach opens the door to large-scale integration of silicon photonics and advanced bulk CMOS electronics. It also relaxes design constraints on photonic devices and enables optimized photonics with better performance.

Chapter 3

3D Integrated Optical Transceiver

3.1 3D Integration of CMOS and Phtonics

Traditional heterogeneous platforms capitalize on the ability to individually optimize the photonic and electronic macros, an element missing in other forms of integration. However, the large interface capacitance associated with thru-silicon via (TSV) and -bump technologies limits the overall system performance as well as energy-efficiency.

As illustrated in Figure 3.1 and 3.2, in this process, 300mm photonic and electronic wafers are manufactured separately in CNSE 300mm foundry and then bonded face-to-face using oxide bonding. The silicon substrate is then removed on the photonic SOI wafer and TOVs are punched through at 4m pitch to connect the top layer metal of the photonic wafer to the top layer metal on the 65nm bulk CMOS wafer.

For packaging, wire-bonded back metal pads are deposited on top of the selected TOVs. The connection from the CMOS wafer to the photonic device is achieved through the TOVs passivated on top with an oxide layer, which minimizes the parasitic capacitance. Our measurements estimate the TOV capacitance to be 3fF, which enables low-power and high-sensitivity electronic-photonic systems for a variety of applications. This represents an order of magnitude reduction in parasitic capacitance, and two orders of magnitude higher density

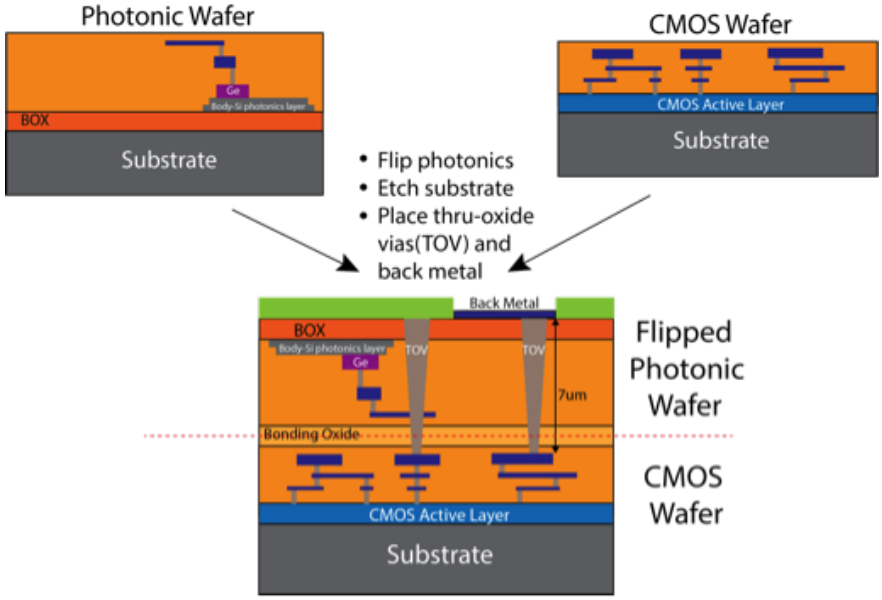

Figure 3.1: Cross-section of 3D heterogeneous integration process

compared to previously demonstrated -bump flip-chip electronic-photonic integration [3].

3.2 Chip Architecture

The optical chip-to-chip link is a part of the wafer-scale heterogeneously integrated technology-development and demonstration platform with low-energy optical transmitters, receivers, and comprehensive backends for performance characterization (Figure 3.3). Apart from containing vertical junction depletion mode microdisk modulators [10] within the photonics die, hetero-epitaxially grown Germanium photodiodes and body crystalline silicon low-loss waveguides are also used to enable electro-optic transceiver functionality. The 16M transistor electronic chip contains 32 Multicell sub-blocks that enable a full self-test of modulators and receivers within the link.

Each Multicell is composed of eight RX as well as eight TX macros, enabling in-situ testing of a wide variety of photonic devices. The Multicell also contains an expansive digital backend infrastructure to enable full, self-contained characterization of each of the eight TX and RX sites. Characterization is accomplished through on-chip, self-seeding PRBS generators and counters. The $2^{31}-1$ length PRBS data sequence gets fed into one of the TX

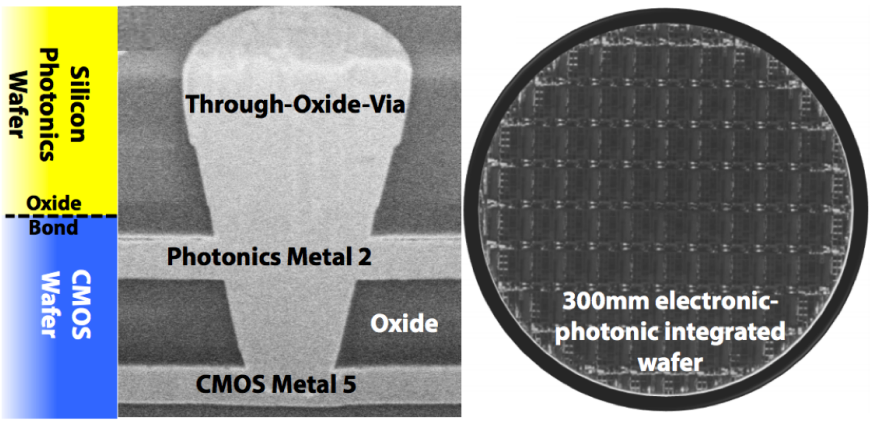

Figure 3.2: Cross-section and top view of the electronic-photonic wafer

macro sites, which serializes the data and drives the resonant modulator device imprinting the data sequence on the light in photonic waveguide. On the RX side, this modulated light is fed into one of the eight RX macros. The output of this RX macro is an eight-channel bus, marking the deserialized input optical data. These eight channels proceed on into the backends bit-error-rate (BER) checkers, which count the total number of errors between the received data from the RX macro and the ideal sequence provided by the seeded PRBS generator. Each of TX and RX sites also contains thermal tuning circuits for stabilizing the resonance wavelengths of microring devices.

3.3 Transmitter Design

The TX macro (Figure 3.4) consists of a tunable vertical junction depletion-mode ring resonator similar to [9, 10] driven by an 8 to-1 serializer and driver head with on-chip PRBS input. The applied reverse-bias voltage to the junction via the driver head depletes free carriers and perturbs the refractive index of silicon, which in turn shifts the resonance wavelength (or frequency) of the optical modulator. The cathode of the modulator diode is connected to 1.2V while the anode is modulated from 0 to 1.2V. The modulator p-n junction is reverse-biased during modulation.

Given that the leakage current is small, the energy is consumed only when the transitions charge the reverse-biased junction capacitor. With a total modulator driver capacitive load

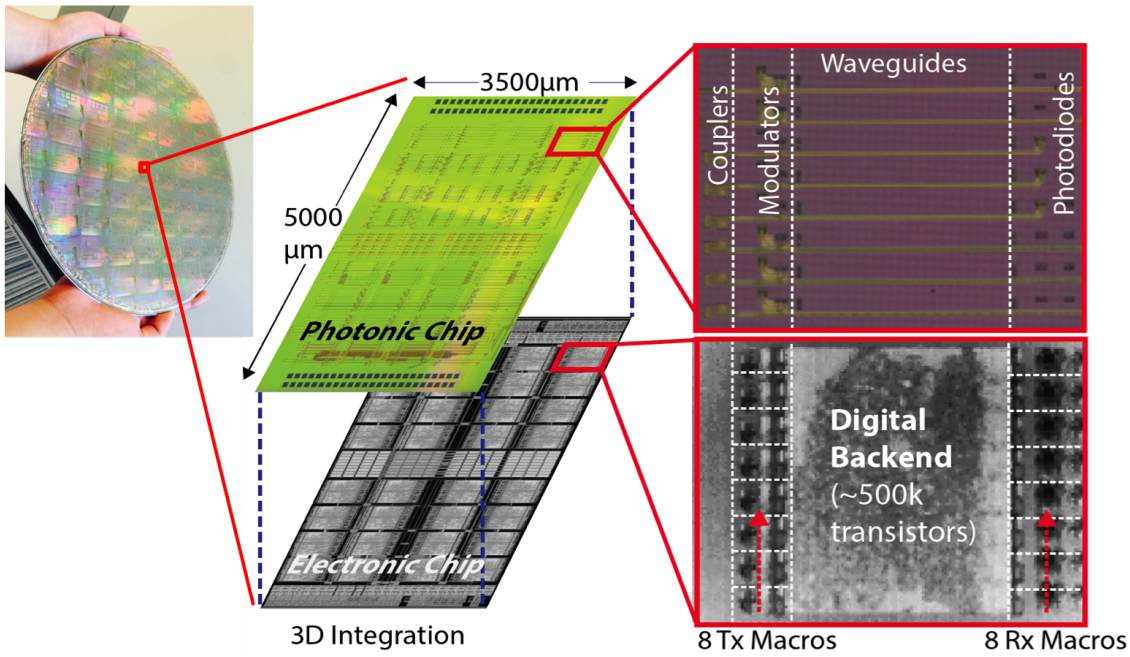

Figure 3.3: Photonic and CMOS die views and Multicell architecture

of 12.4fF (modulator diode and TOV), at 6Gb/s the whole macro consumes 100fJ/b (5fJ/b modulator, 15fJ/b driver, and 80fJ/b serializer).

Heterogeneous integration allows us to use the state-of-the-art ring resonant modulators with a large electro-optic response of 150pm/V (20GHz/V), which enables low power modulation using small voltage swing (1.2V) while still maintaining sufficient extinction ratio (Figure 3.5(a)). Measured from the modulator transmission spectra at 0V and -1.2V dc biases, the device should ideally achieve 6.2dB extinction ratio (ER) and 1.8dB insertion losses (IL). The modulator can also be modulated between a slightly forward-biased regime and depletion regime by lowering the bias voltage of the anode (i.e. -0.2 to 1.0V). This will further improve extinction ratio of the modulator.

A tunable CW laser source was coupled to an on-chip silicon waveguide through a vertical grating coupler. The laser frequency was aligned adjacent to the resonance frequency of the modulator ring (λ 1520nm, see Figure 3.5(a)). The TX circuits drive the 31-bit PRBS sequence into the modulator, achieving the non-return to zero on-off keying (NRZ-OOK) modulation eye at 6Gb/s, as shown in Figure 3.5(b), with 6dB extinction ratio and 2dB of insertion loss, which agrees well with the transmission spectrum. The fast rise-time indicates

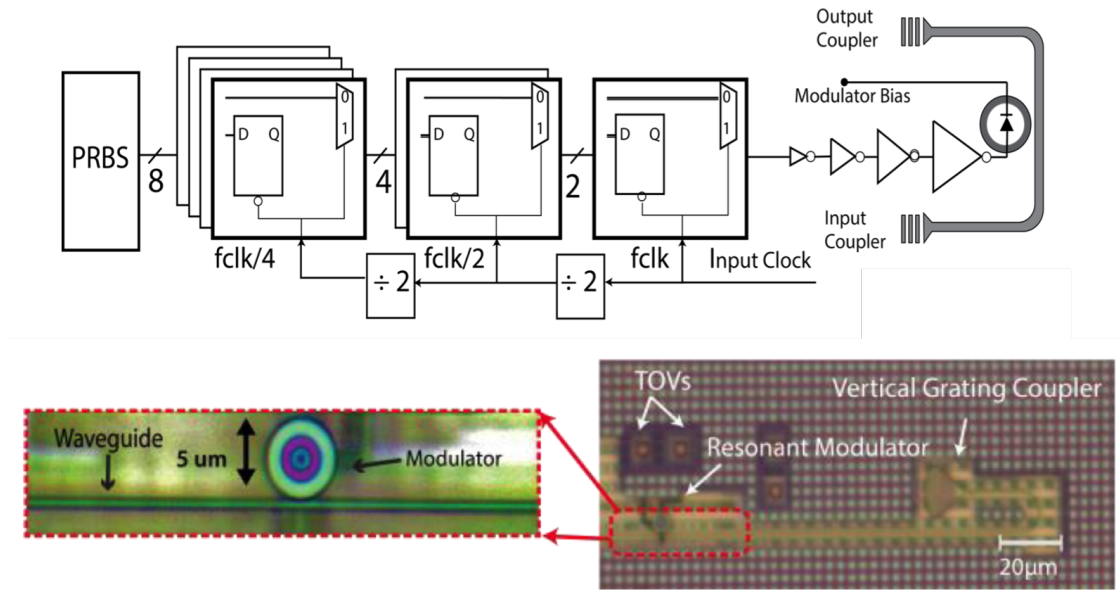

Figure 3.4: Optical transmitter schematic and die photos.

the potential for faster operation, but the results are currently limited by the global high-speed clock distribution network that spans the whole chiplet and supplies the clock to all the Multicell macros.

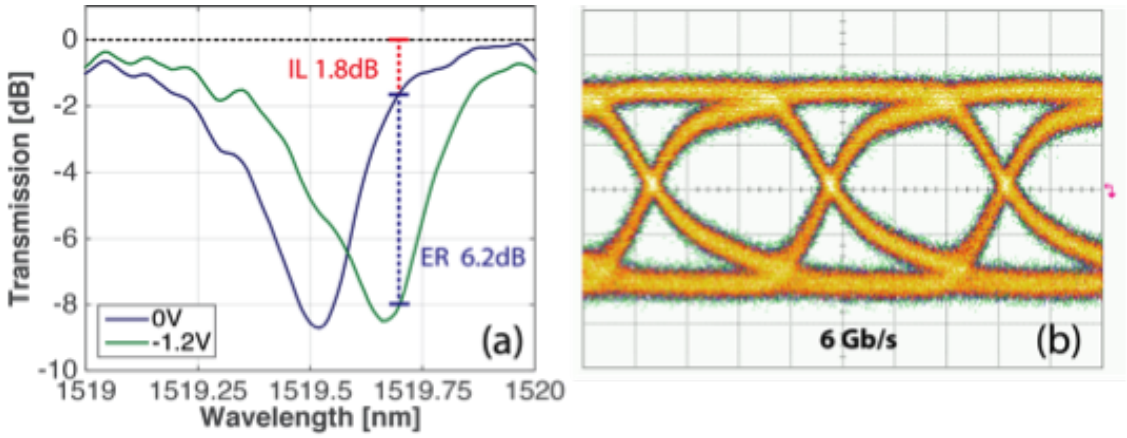

Figure 3.5: Measured modulator transmission spectrum and eye diagram.

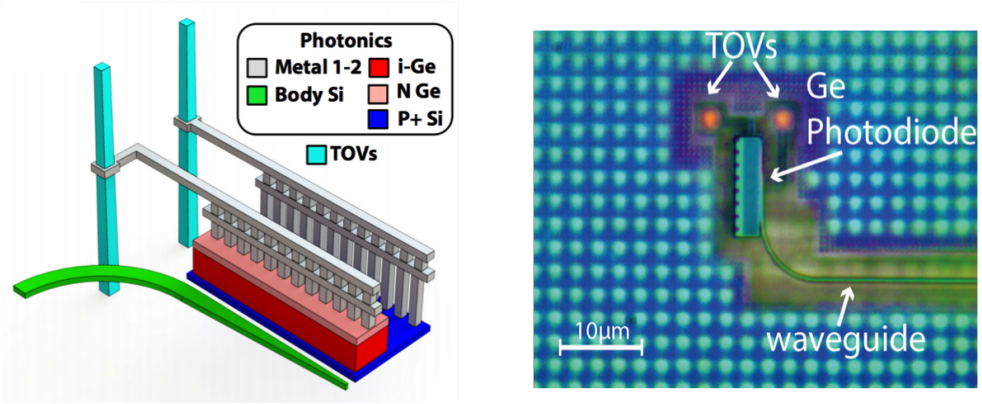

Figure 3.6: 3D render and die photo of Ge photodetector.

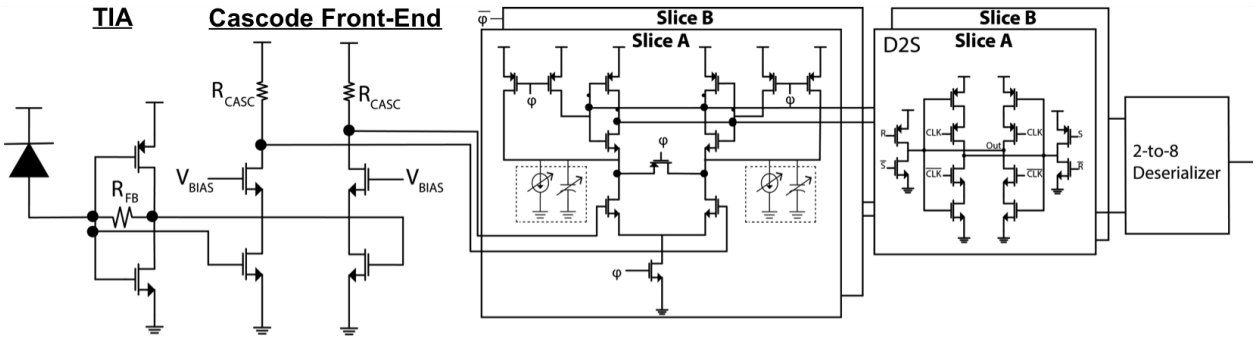

Figure 3.7: Optical receiver schematic.

3.4 Receiver Design

The receiver (Figure 3.6) consists of a Ge photodiode placed on top of the electronics and connected to the receiver circuitry via TOVs with minimal parasitic capacitance. In Figure 3.7, the TIA-based receiver circuit has a pseudo-differential front-end with a cascode pre-amplifier feeding into double-data rate (DDR) sense-amplifiers and dynamic-to-static converters (D2S). The TIA stage with 3kOhm feedback contains a 5-bit current bleeder at the input node, which is set to the average current of the photodiode. This allows the TIA input and output to swing around the midpoint voltage of the inverter. The TIA input and output are directly fed into a cascode amplifier with resistive pull up.

The bias voltage of the cascode is tuned through a 5-bit DAC. Adjusting this bias voltage results in a trade-off between the output common-mode voltage and the signal gain of the cascode stage. More specifically, increasing this bias voltage results in a higher cascade gain

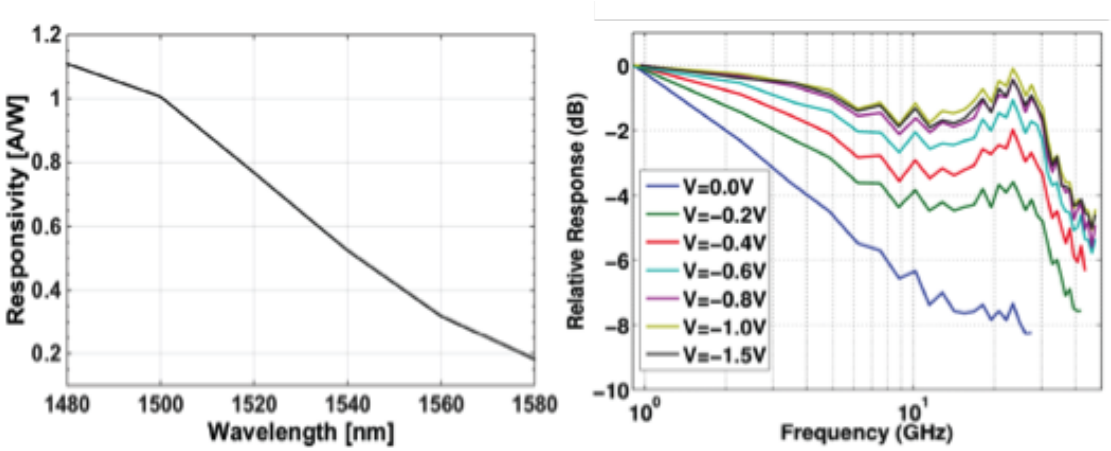

Figure 3.8: Measured photodiode responsivity over 100 nm wavelength range and its frequency response (with 50Ohm load) for different bias voltages.

but lower output common-mode voltage that reduces the sense-amplifier speed. For a given data rate, an optimal bias voltage is determined so as to minimize the overall evaluation time of the sense amplifier. The proceeding sense amplifiers then evaluate the cascode outputs before getting deserialized and fed into on-chip BER checkers. Each sense amplifier has a coarse, 3-bit current bleeding DAC as well as a fine, 5-bit capacitive DAC for offset correction. An external Mach-Zehnder modulator with extinction ratio of about 10dB driven by an FPGA-sourced PRBS sequence is coupled into the chip to enable stand-alone receiver characterization. During the initial seeding phase, the incoming receiver data are used to seed the on-chip PRBS generators for the BER check. The receiver and deserializer achieve 7Gb/s with a BER below 10^{-10}.

The responsivity and bandwidth of this process variant of the Ge photodiode in [9], are shown in Figure 3.8. At 1520nm, the responsivity is 0.73A/W, resulting in optical RX sensitivity of 14.5dBm at 7Gb/s, for electrical sensitivity of 26A. The overall energy consumption is 340fJ/bit. The TIA+cascode pre-amplifier stage consumes 70fJ/bit. The sense amplifier, current plus capacitive correction DACs, and the dynamic-to-static converter together consume 120fJ/bit. Finally, the deserializer consumes 150fJ/bit. Figure 3.9 shows the sensitivity of the receiver as a function of data rate. Additionally, bathtub curves for the two slices of the DDR receiver are also shown.

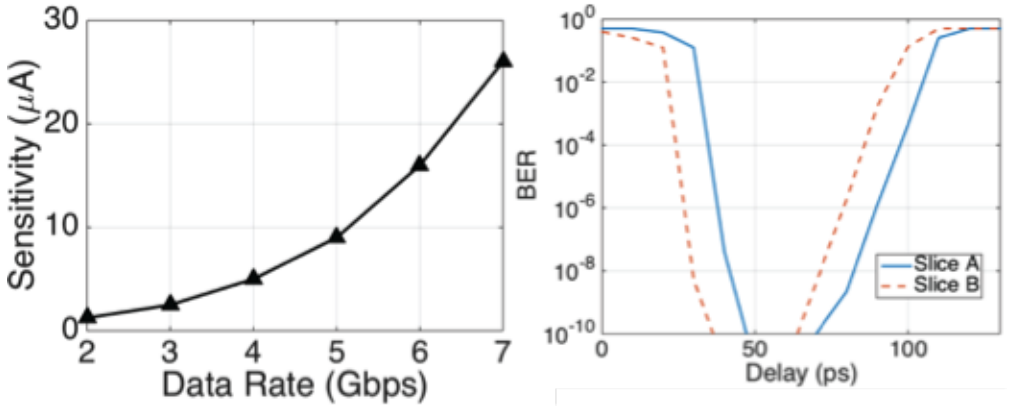

Figure 3.9: Measured receiver average photo-current sensitivity over different data rates and BER bathtub curves for both receiver slices

3.5 Thermal Tuner Design

We designed thermal tuning circuits to stabilize the resonance wavelength of microring resonantors in order to compensate process variations and temperature fluctuations. The thermal tuner for microring transmitters is based on a bit-statitical tuning algorithm [11]. The similar thermal tuning backend is implemented in 65nm process. The system diagram of the tuning backend is shown in Figure 3.10.

As shown in Figure 3.10, a drop port waveguide is weakly coupled to microring resonator to detect power level inside the microring. The photocurrent at the drop port is then integrated and quantized by a ring oscillator based SAR ADC. The power strengths for optical level 1 and 0 can be calculated by the tuning backend based on the knowledge of transmitted data. With the goal to maximize the optical eye opening, a thermal controller actively sets the coefficients for a sigma-delta heater DAC. This heater DAC drives the embedded silicon heater inside the microring and controls the local temperature and thereby the resonance of the microrings. For initial locking, the heater strength is swept to search for the laser wavelength and optimal locking point (Figure 3.11). The optimal heater strength for maximizing optical eye diagram is stored in this initial sweeping process. The heater strength is then reset to this optimal value while the thermal tuning loop continues to thermally lock the microring. The captured eye diagrams in a slowed down thermal locking process show that the thermal tuning loop works as expected.

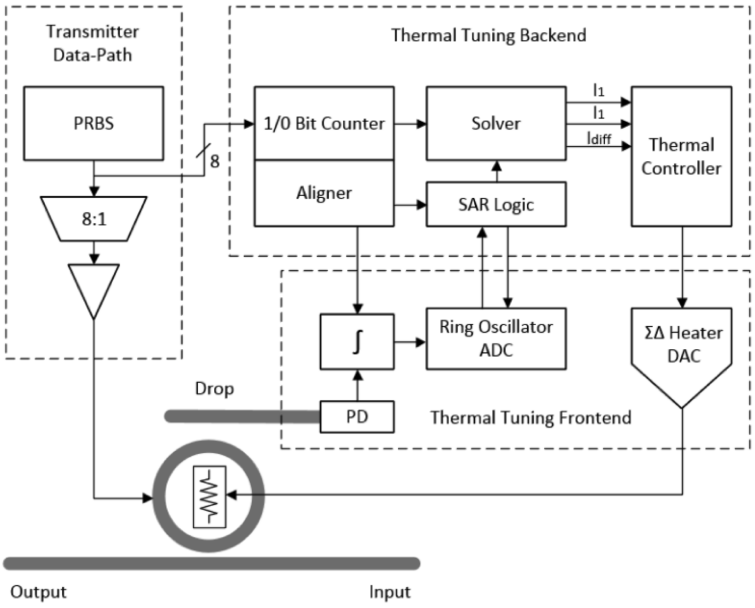

Figure 3.10: System diagram of the thermal tuning loop.

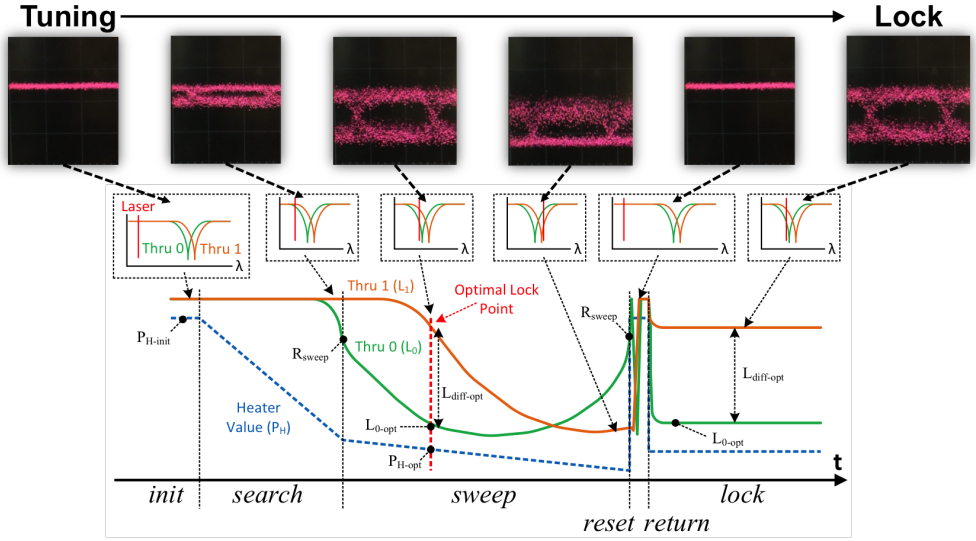

Figure 3.11: Automatic thermal locking process with measured eye diagrams.

Chapter 4

Link Measurement Results

4.1 Link Implementation

A 100-meter optical link operating at 5Gb/s is demonstrated (Figure 4.1) illustrating the functionality of all the required optical and electrical components in this heterogeneous platform. The experiment setup in the lab is shown in Figure 4.2 with transmitter chip and receiver chip mounted on the same optical table.

Figure 4.1 also shows the optical power breakdown per stage within the full link. A CW laser at λ 1520nm is coupled to the on-chip TX macro of Chip 1 using a vertical grating coupler. The coupler results in 7.5dB of loss in optical power. A PRBS generated data within this TX macro are fed into the modulator driver, which in turn modulates the ring resonator. The output of the TX macro including the coupler is the modulated light with 6dB extinction ratio. This light is fed into an optical amplifier providing 8dB of gain. The 8dB amplifier is necessary to mitigate part of the 15 dB chip-to-chip coupler loss in the optical data path (7.5dB per coupler) due to unoptimized coupler designs. The amplifier feeds into the 100 meter fiber proceeded by a 90/10 power splitter. A monitoring scope, using the 10% output, is used to ensure that an optical eye is visible. The 90% output is coupled into the RX macro. The Ge photodiode is used within the RX macro to convert incoming optical data to an electrical bit stream. This photodiode sees 12.3dB and -18.3dB

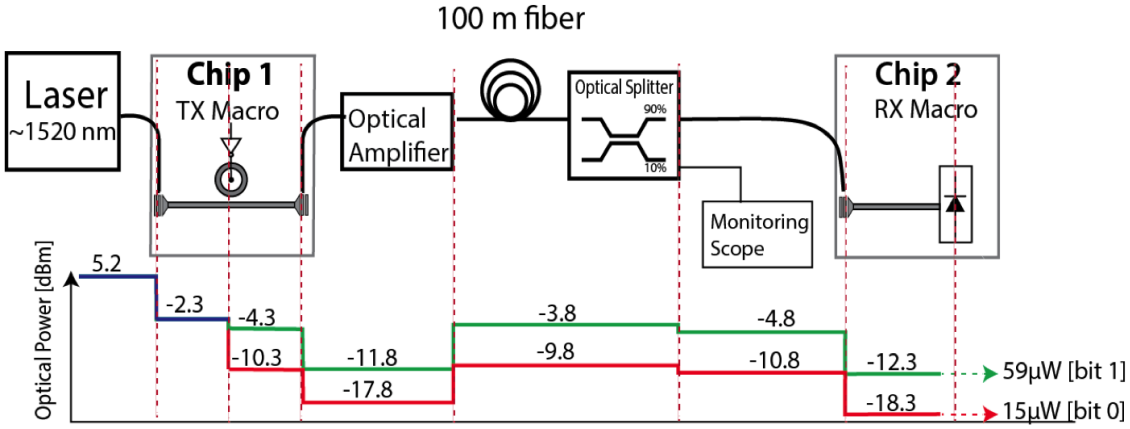

Figure 4.1: Link budget of the full optical link.

optical power for a bit 1 and 0, respectively.

Figure 4.3 shows the output BER plot indicating at least 10^{-10} bit accuracy. This BER plot sweeps two parameters within the RX macro. First, the delay of the RX clock with respect to the TX clock is shown on the x-axis. Second, the corrective capacitor DAC within the receiver sense amplifiers is swept and shown on the y-axis. For particular delays and capacitive DAC values, a steady BER $< 10^{-10}$ is observed, illustrating the margins for the robust operation of the link. The transceiver electrical energy cost is 560fJ/bit and the optical energy cost is 4.2pJ/bit (taking into account the amplifier gain). With optimized couplers (<3dB readily achievable in literature [12]), the required optical energy would scale down to below 0dBm (200fJ/bit) thereby eliminating the need for the optical amplifier.

4.2 Analysis and Comparison

Figure 4.4 shows the electrical power breakdown of TX and RX macros within the link at 5Gb/s data rate. Figure 4.5 presents the comparison to previous non-monolithic electronic-photonic transceiver works.

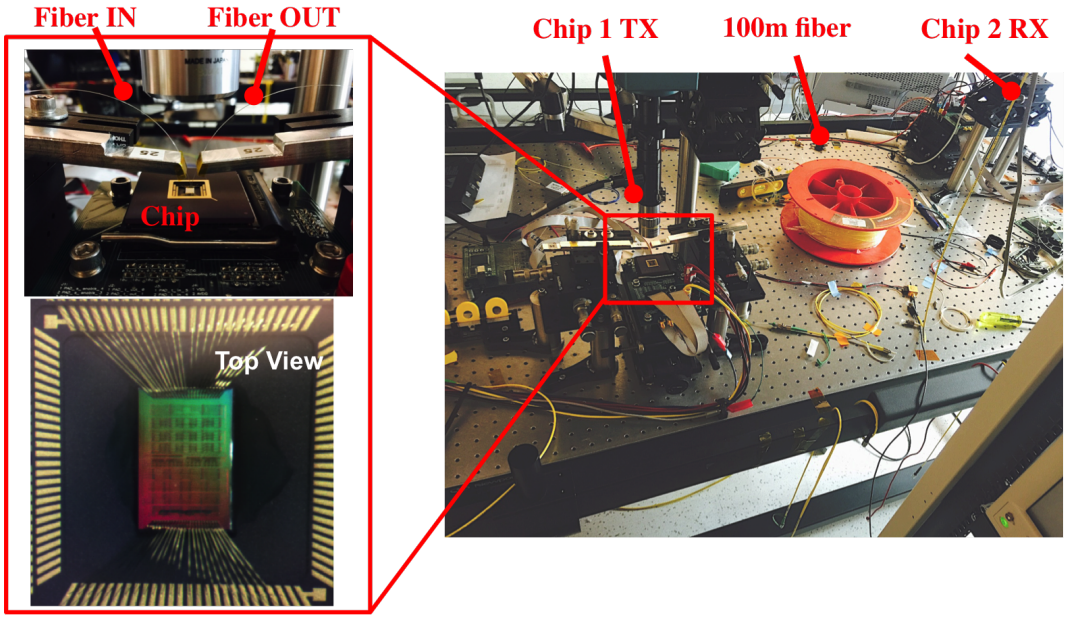

Figure 4.2: Lab setup for full optical link testing.

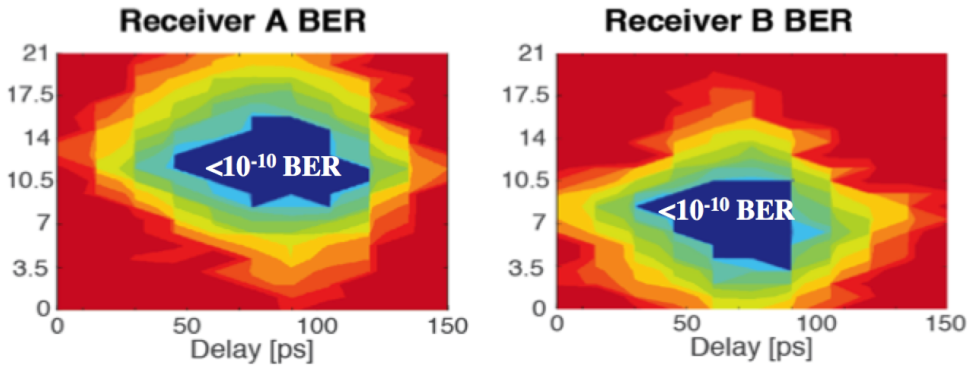

Figure 4.3: Full optical link BER performance.

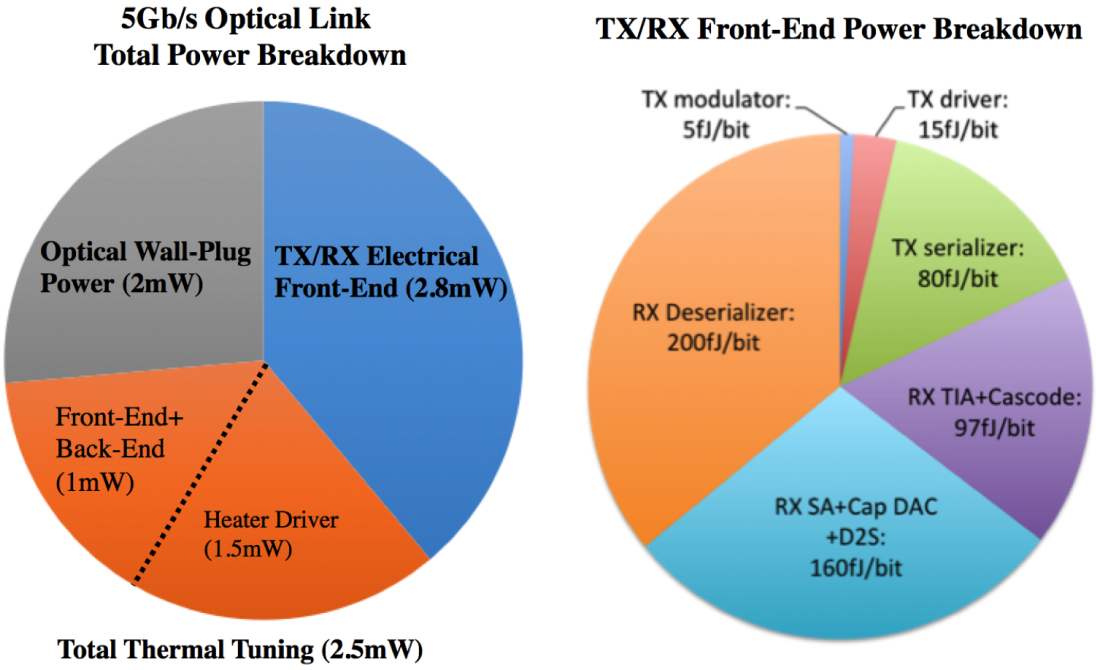

Figure 4.4: Electrical energy breakdown for TX and RX macros in a 5Gb/s link.

	This work	Liu JSSC 2012	Li ISSCC 2013
CMOS Technology	65nm	40nm	65nm
Integration	Flip-Wafer 3D TOV	Flip-Chip µbump	Flip-Chip
RX Data rate [Gb/s]	7	10	8
RX Energy [fJ/b]	340	395	275
RX Area [mm^2]	0.0025	0.02	0.036
$C_{interconnect}$ [fF]	3	30	200
RX Ckt. Sens. [µA]	26	20	53.7
RX Opt. Sens. [dBm]	-14.5	-15	-12.7
TX Data rate [Gb/s]	6	10	5
TX Energy [fJ/b]	100	140	808
TX Area [mm^2]	0.0015	0.0012	0.04
Link DR [Gb/s]	5	10	-
Link Energy [fJ/b]	560	535	

Figure 4.5: Comparison to previous works

Chapter 5

Conclusion

This work demonstrates the first large-scale 3D integrated photonic chip-to-chip link manufactured in a 300mm CMOS foundry. The functional 3D-assembled chips with 16M transistors and 1000s of photonic devices illustrate the high yield of the CMOS, photonic fabrication and 3D integration processes.

A full optical chip-to-chip link is demonstrated for the first time in a wafer-scale heterogeneous platform, where the photonics and CMOS chips are 3D integrated using wafer bonding and low-parasitic capacitance thru-oxide vias (TOVs). This development platform yields 1000s of functional photonic components as well as 16M transistors per chip module. The transmitter operates at 6Gb/s with an energy cost of 100fJ/bit and the receiver at 7Gb/s with a sensitivity of 26μA (-14.5dBm) and 340fJ/bit energy consumption. A full 5Gb/s chip-to-chip link, with the on-chip calibration and self-test, is demonstrated over a 100m single mode optical fiber with 560fJ/bit of electrical and 4.2pJ/bit of optical energy.

Using the same electronic-photonic platform and improved circuits, a new test chip with 25Gb/s per channel DWDM silicon photonic links has been designed and taped out. The 3D integrated electronic-photonic platform holds great promise for future energy-efficient high-speed WDM communication links.

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