An Integrated Multilevel Converter with Sigma Delta Control for LED Lighting

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by

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University of California, Berkeley

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Abstract

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High brightness LEDs have become a mainstream lighting technology due to their efficiency, life span, and environmental benefits. As such, the lighting industry values LED drivers with low cost, small form factor, and long life span. Additional specifications that define a high quality LED driver are high efficiency, high power factor, wide-range dimming, minimal flicker, and a galvanically isolated output. The flyback LED driver is a popular topology that satisfies all these specifications, but it requires a bulky and costly flyback transformer. In addition, its passive methods for cancelling AC power ripple require electrolytic capacitors, which have been known to have life span issues. This dissertation details the design, construction, and verification of a novel LED driver that satisfies all the specifications. In addition, it does not require a flyback transformer or electrolytic capacitors, thus marking an improvement over the flyback driver on size, cost, and life span.

This dissertation presents an integrated circuit (IC) LED driver, which features a pair of generalized multilevel converters that are controlled via sigma-delta modulation. The first is a multilevel rectifier responsible for power factor correction (PFC) and dimming. The PFC rectifier employs a second order sigma-delta loop to precisely control the input current harmonics and amplitude. The second is a bidirectional multilevel inverter used to cancel AC power ripple from the DC bus. This ripple-cancellation module transfers energy to and from a storage capacitor. It uses a first order sigma-delta loop with a preprogrammed waveform to swing the storage capacitor voltage. The system also contains an output stage that powers the LEDs with DC and provides for galvanic isolation. The output stage consists of an H-bridge stack that connects to the output through a small toroid transformer.

The IC LED driver was simulated and prototyped on an ABCD silicon test chip. Testing and verification indicates functional performance for all the modules in the LED driver. The driver exhibits moderate efficiency at half voltage. Although the part was only testable to half voltage, loss models predict that its efficiency would be much higher at full voltage. The driver also meets specifications on the line current harmonics and ripple cancellation.

This dissertation introduces multilevel circuit techniques to the IC and LED research

space. The prototype's functional performance indicates that integrated multilevel converters are a viable topology for lighting and other similar applications.

Dedication

Dedicated to my family and friends, who have been unwavering in their love and support.

Contents

List of Figures

List of Tables

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I would like to give special thanks to my advisor Professor Seth Sanders for all his knowledge, guidance, and support throughout my time Berkeley. Additional thanks to my fellow group members, whose advice and support have proven invaluable on many occasions. Finally, I would like to thank my family and friends, who have encouraged and supported me through the endeavor.

Chapter 1

Introduction to LED Drivers

1.1 The Lighting Industry

Since the invention of the light bulb, lighting has been central to productivity and advancement. Newly electrified communities and industrialized nations both prioritize lighting as the first and most important electrical load to be connected. In 2013, lighting accounted for 17% of the total US electrical energy consumption [1]. As such, there is significant motivation to increase the performance of lighting technology. For the industry, this means increasing the efficiency and efficacy of commercial and residential lamps.

Over the past century, the lighting industry has transitioned through multiple technologies [2]. The earliest technology, the incandescent bulb, established the industry and saw widespread use through the end of the 20th century. Incandescent bulbs operate by the principle of incandescence, in which an electric current heats the tungsten filament until it emits light.

The incandescent bulb's successor, the fluorescent bulb, was also present for much of the 20th century. By 1951, fluorescent lamps were the dominant lighting technology in the US. The helical compact fluorescent lamp (CFL) became available for purchase in 1995, and became popular in the residential sector. The fluorescent bulb contains mercury gas, which emits ultraviolet radiation when subject to an electric current. The ultraviolet radiation is absorbed by the bulb's phosphor coating, which in turn releases visible light through fluorescence. CFLs became popular because they require a third the power and last 5-10 times longer than the incandescent bulb [3–6].

Despite their superior efficiency and life span, CFLs have several notable drawbacks. First, CFLs contain mercury gas, which damages the environment if released [7, 8]. Recycling CFLs requires an extensive and specialized process. Another drawback of the CFL is that it has a lower color rendering index (CRI) than the incandescent bulb [2, 9–11]. The CRI is a metric for how accurately a lamp can render colors. Light sources such as daylight or incandescent lamps have a perfect CRI of 100. CFLs have a CRI in the low 80's, and various colors rendered under a CFL may appear in the wrong shades. The final drawback of CFLs

is that they have a cooler correlated color temperature (CCT). Lamps with a cooler CCT illuminate with a white or blue tone, whereas lamps with a warmer CCT appear as yellow and orange. Many people prefer the relaxing feel of a warmer CCT, and studies show that a cooler CCT may have an adverse effect on sleep [12–14].

Since the early 2000's, the light emitting diode (LED) has transitioned from indicator lights to becoming mainstream in the lighting industry. Today, LEDs are recognized for their efficiency, reliability, and environmental benefits. The LED is a semiconductor diode with a positive-type and negative-type dopant. When the LED is subject to a voltage potential, the electrons and holes at the dopant junction are able to recombine and release energy in the form of light. LEDs use roughly 80% as much power as CFLs and last more than twice as long [3–6]. Many case studies have shown that the combination of efficiency and life span makes LEDs the most economic choice (i.e. lowest life cycle cost) for lighting. LEDs have a slightly greater environmental impact than incandescent bulbs due to a higher concentration of toxic metals (per lumen). However, they are significantly more environmentally friendly than CFLs [7, 8]. Unfortunately, LEDs also suffer a similarly low CRI and color temperature [11]. Some of the more expensive LED lamps can have CRI and color temperatures that are nearly as good as the incandescent lamp.

Since 2010, LED lamps have seen an increase in market share as technological improvements have lowered manufacturing costs. Figure 1.1 shows that by 2030, LEDs are expected to have mostly replaced incandescents and CFLs [1]. Since LEDs will become the cornerstone of the lighting industry, there is great industrial motivation to produce efficient, economic, and high quality LED lamps. This dissertation is centered around enhancing an LED lamp by designing an improved LED driver.
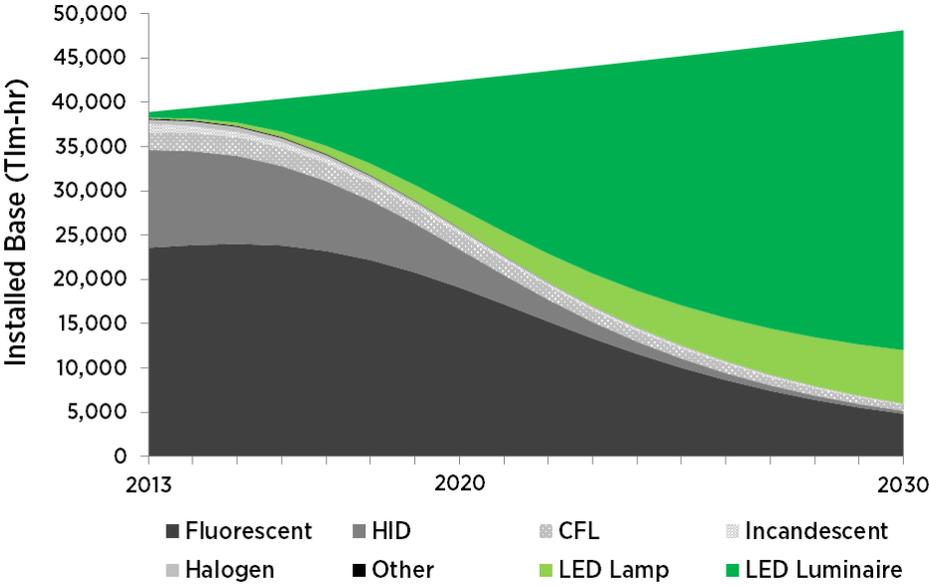
(a)
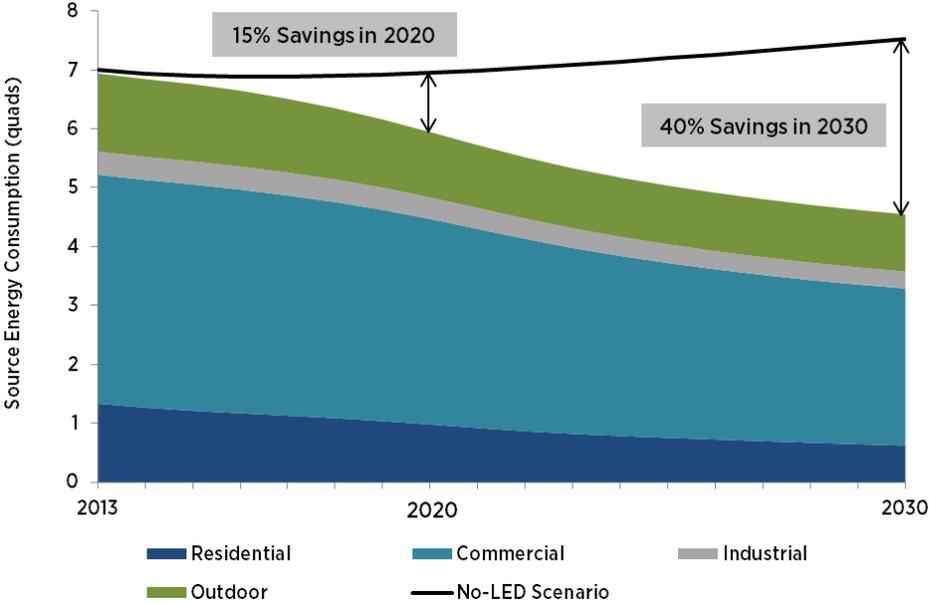
(b)

Figure 1.1: DOE forecast of the lighting industry from 2013 to 2030, taken from [1]. (a) Distribution of installed lighting types over the next decade. By 2030, LEDs are expected to mostly replace all other forms of lighting. (b) Lighting energy consumption over the next decade. Due to the switch to LEDs, lighting energy consumption is expected to decrease by 40%.

1.2   The LED Driver

The LED driver supplies power to the LEDs in a lamp. As shown in Figure 1.2, the driver includes all of the electronics between the building 120 V_{RMS} distribution and the LEDs. LEDs are recognized as the most economic choice for lighting, and so it is important that the LED driver be equally inexpensive, efficient, and reliable.

Other types of lamps have their own methods of providing power to the bulb. The incandescent lamp does not require a driver since a bulb can attach directly to the AC 120 V_{RMS} distribution. Fluorescent lamps require a driver that serves two purposes. On startup, the fluorescent lamp driver is responsible for providing a voltage high enough to ionize the inert gas inside the bulb. Once the gas is ionized, its resistance decreases with current, which leads to an unstable positive feedback. Therefore, the fluorescent lamp driver must also act as a ballast and control the current flowing through the bulb.

There are several technical challenges in driving LEDs that are not present with the incandescent bulb [15–17]. The first is that LEDs require DC power. The incandescent bulb works with either AC or DC since any type of current can heat the filament. However, LEDs block reverse current, and so the driver must rectify the AC input to DC. Rectification can be accomplished with a simple diode bridge. However, many applications and standards
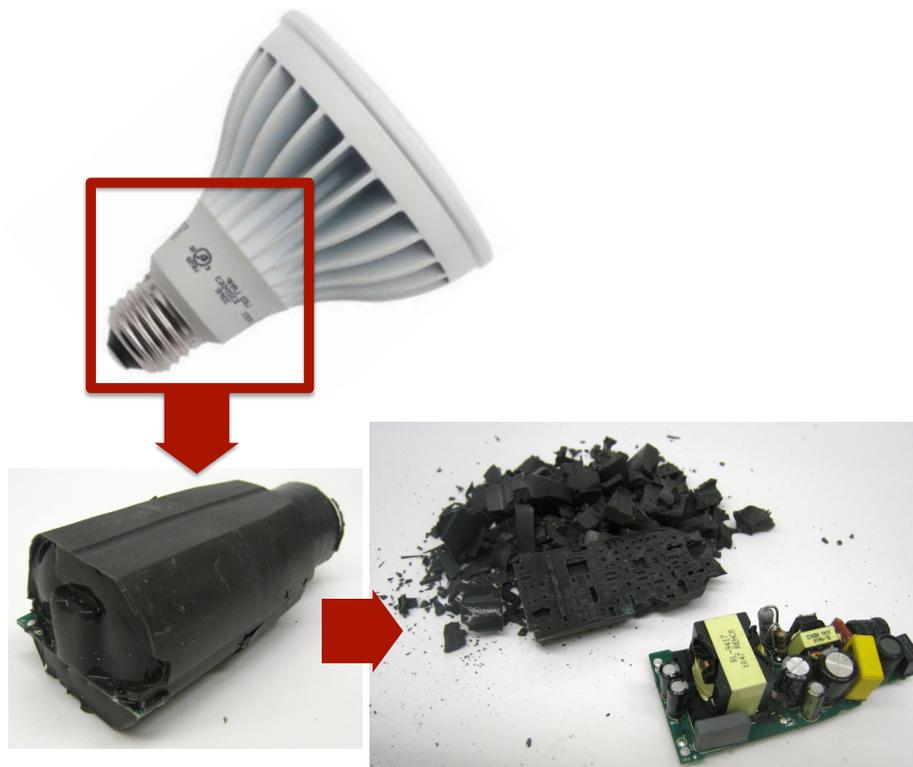
Figure 1.2: Teardown of an EcoSmart PAR30 LED flood light. The driver plug sits inside the base of the housing and connects the glass filled screw socket to the LEDs.

require a high power quality.

Power quality can be evaluated with a metric known as power factor. A perfect unity power factor occurs when the input current is purely sinusoidal and in phase with the input voltage. The incandescent bulb has nearly unity power factor because its load profile approximates that of a resistor. The overall power factor encapsulates both the displacement factor and the distortion factor [18]. Harmonic distortion on the input current is a major concern for higher power LED lamps. It can be measured as the agglomerate of the input current harmonics. The total harmonic distortion (THD) is measured as

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{1.1}$$

where I_n and I_1 represent the n-th harmonic and the fundamental of the input current respectively. The distortion power factor is closely related to the THD, and is measured as

$$\frac{I_{1,rms}}{I_{rms}} = \frac{1}{\sqrt{1 + (\text{THD})^2}} \tag{1.2}$$

where I_{rms} is the root mean square (RMS) of the input current, and where $I_{1,rms}$ is the root mean square (RMS) of the fundamental.

Many standards exist for regulating the power factor and harmonic distortion in loads. For lighting in particular, standards such as IEC 61000-3-2 (US) and EN 61000-3-2 (Europe) specify the acceptable limitations on specific line-current harmonics [19]. As such, it is often important and desirable for the LED driver to be able to perform power-factor correction (PFC). Passive PFC involves using a passive LC filter to remove harmonics from the line current. However, a 60 Hz filter is bulky and expensive, and so passive techniques are almost never used exclusively. Active PFC involves the use of active switching patterns to remove harmonics. Some LED drivers perform PFC through active techniques with the assistance of a small passive filter that is designed to filter out the high switching frequency.

Another technical challenge in driving LEDs is that they have an exponential current-voltage relationship. First consider an incandescent bulb, whose current-voltage relationship approximates that of a resistor. The current through the filament is proportional to voltage, and so the bulb's power (and luminous output) can be controlled by its voltage. However, an LED's current varies exponentially with its voltage, as shown in Figure 1.3. In such a relationship, small deviations in LED voltage can cause large swings in LED current. An LED's brightness varies almost linearly with its current, and so small deviations in voltage can lead to a drastically different luminous output. It is difficult to regulate a driver's output voltage to the degree required. As such, LED drivers must employ precise current control in order to regulate the luminous output of the LEDs.

An additional challenge is that LEDs have a fast luminous response to power ripple. As discussed in Section 1.1, LEDs generate light when charge carriers recombine and release photons. Relative to electrical distribution frequencies, charge recombination is a very fast
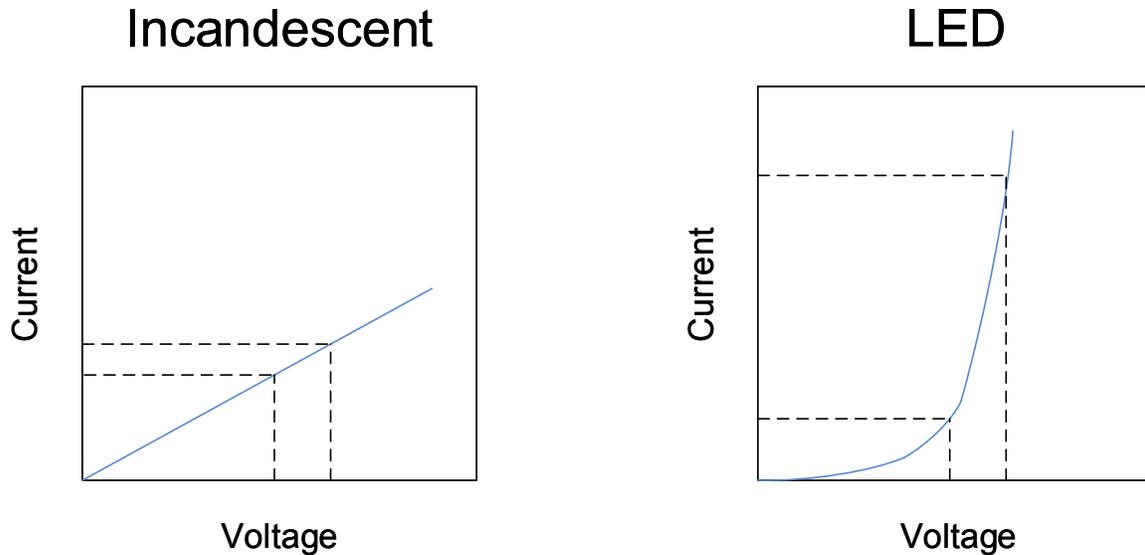
Figure 1.3: Sample plots of current vs voltage for the incandescent bulb and the LED (not to scale). The incandescent bulb has a linear or resistive relationship, and either voltage or current control may be employed to regulate the power. The LED has an exponential relationship. A small deviation in voltage could determine whether the LED is on or off. As such, current control is desirable to regulate LED power.

process. In contrast, the incandescent bulb generates light via incandescence, which occurs after electrical power is converted to thermal energy. Thermal processes such heat transfer tend to be relatively slow. Since the incandescent bulb has a relatively long thermal time constant, it can effectively filter the 120 Hz power ripple from the input.

LEDs have a time constant that is much smaller than that of the AC input. The driver's AC input may transfer 120 Hz power ripple to the LEDs, which may in turn cause 120 Hz LED flicker [20]. Flicker can have an adverse effect on human health including headaches, loss of concentration, and seizures. As such, the LED driver must have a means of reducing power ripple at the LEDs. Ripple and flicker will be further discussed in Section 1.4.

Finally, high brightness LED lamps require careful thermal management. LED life span degrades exponentially with increasing the operating temperature [21]. For safety considerations, the LED heat sink must be galvanically isolated from the power train. Providing a means to galvanically isolate the LEDs allows the LEDs to be directly mounted on the heat sink. Thus, galvanic isolation of the LEDs is a desired circuit function.

1.3 LED Driver Topologies

Over the past decade, the LED industry has matured through the design and improvement of LED driver circuit topologies. This section provides a survey of the various LED driver technologies on the market or in publication. It explains and evaluates how each topology address the design challenges in Section 1.2.

1.3.1 Linear LED Drivers

The linear LED driver, shown in Figure 1.4, is based on the linear regulator [22, 23]. Linear LED drivers are generally smaller and less expensive than other topologies because they do not require bulky magnetics. In addition, linear drivers do not require high voltage switching for operation, and thus inject very little electromagnetic interference (EMI) onto the line. As shown in Figure 1.4, the linear driver can vary the impedance of multiple strings of LEDs in order to control the driver's input impedance. With control over the input impedance, the driver may precisely regulate the input current, thereby allowing it to perform both power-factor correction (PFC) and current regulation.

The most notable disadvantage of the linear driver is its relatively low efficiency. In addition to control loss, the efficiency of a linear regulator is inversely proportional to its voltage conversion ratio. Since the drop across any switch (i.e. M_1 and M_2) is loss, the linear LED driver ultimately suffers low efficiency whenever the string of LEDs is not perfectly matched to the input voltage. Another disadvantage is that the LEDs are not galvanically isolated from the power train, which as explained in Section 1.2, can be a safety concern. Finally, the linear LED driver is difficult to adapt to industry applications with specific input or output impedance specifications.
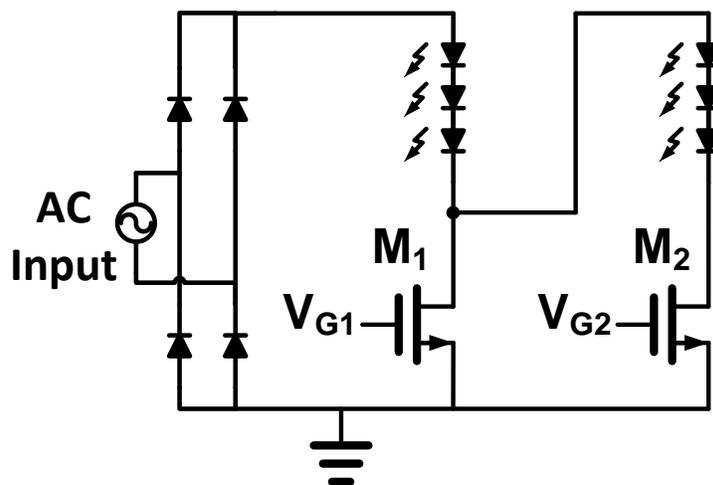
Figure 1.4: The linear LED driver.
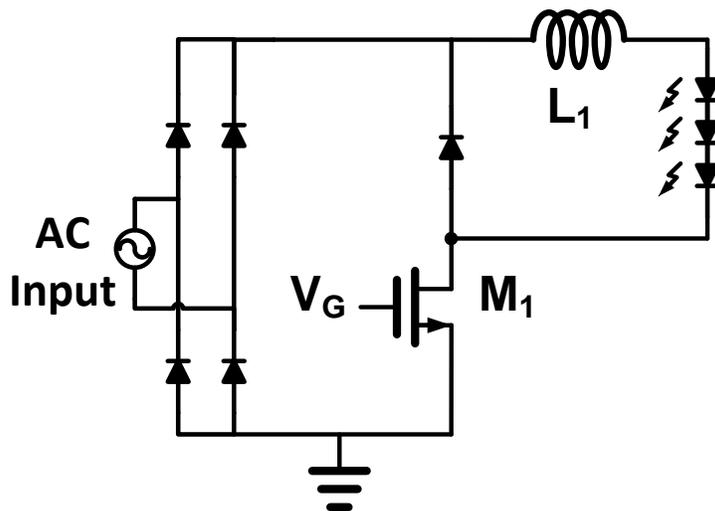
Figure 1.5: The buck-based LED driver.

1.3.2   Switched-Mode LED Drivers

Switched-mode LED drivers perform voltage conversion through high frequency switching. The conversion voltage drop primarily occurs across an inductor, which allows switched-mode converters to be much more efficient than linear regulators. Control over the switching duty cycle allows for output power regulation. A popular switched-mode LED driver is the buck-based driver [16, 24], shown in Figure 1.5. By carefully adjusting the duty cycle and conversion ratio, the converter can simultaneously regulate the current to the LEDs and provide PFC at the input. Other popular switched-mode converter topologies such as the boost converter [25, 26] and the buck-boost converter [27] have also been utilized in LED drivers.

The buck-based LED driver has several disadvantages. First, this topology may require a relatively large inductor (L_1) in order to properly provide PFC and avoid discontinuous condition mode (DCM). In [24], the inductor was sized at 5.5 mH for an 86 kHz design. High frequency switching can reduce the required inductance at the cost of additional gate drive loss. Another drawback is that the main power switch (M_1) must be sized such that it can withstand both the peak line voltage and the LED output current. Finally, the buck-based LED driver is not galvanically isolated at its output. The boost and buck-boost LED drivers allow for larger conversion ratios, but still have the same core disadvantages as the buck LED driver.

1.3.3   Flyback LED Drivers

The flyback LED driver, shown in Figure 1.6, is an isolated buck-boost converter that utilizes the magnetizing inductance in the transformer [16, 28–32]. Due to its efficient switched-mode conversion and galvanically isolated output, the flyback LED driver is currently the
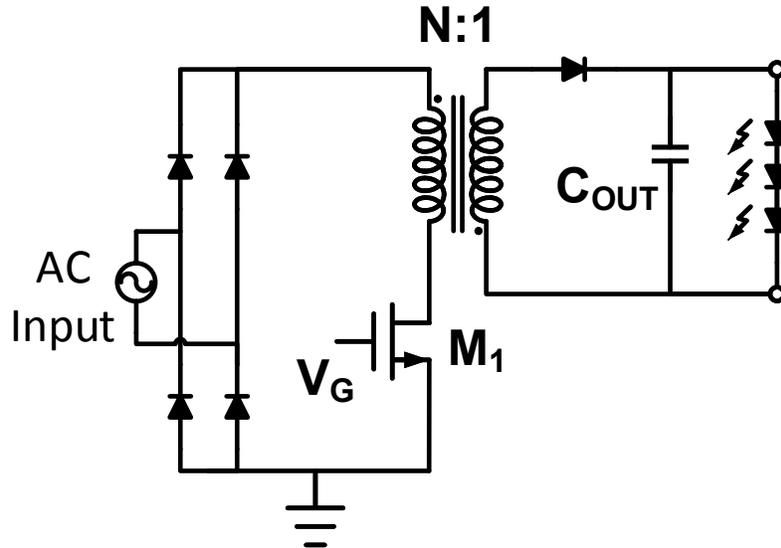
Figure 1.6: The flyback LED driver.

mainstream topology for high brightness LED lamps. As discussed in Section 2.1, this dissertation uses the flyback driver as a baseline for comparison of life span and form factor.

An analysis of the flyback converter's operation in critical conduction mode is shown in Figure 1.7. In this analysis, the flyback transformer is modeled as an ideal transformer with a primary side magnetizing inductance. When the switch turns on, the input voltage is connected across the primary winding and the transformer's magnetizing inductance L_m. The step in voltage across L_m causes the magnetizing current through L_m to ramp up. When the switch turns off, the magnetizing current flows through the ideal transformer's primary winding, ultimately powering the LEDs via the secondary winding.

The disadvantages of the flyback LED driver are in its size and cost. First, the flyback transformer is often bulky and expensive. Since this topology requires the transformer to store energy in its magnetizing inductance, the flyback transformer is larger than an isolation transformer delivering the same V-A rating. One way to reduce the transformer size is to operate in critical conduction mode as shown in Figure 1.7. Critical conduction mode allows the magnetizing current to be reduced and prevents core saturation. The other disadvantage is that the main switch M_1 has to be even larger than that of the buck-based driver. The nominal switch stress can be derived from Figure 1.7c as:

$$S = V_{pk}I_{pk} = (V_{rect} + V_F N)(I_{LED}\frac{2}{N(1-D)}) \tag{1.3}$$

where V_F and I_{LED} are the LED string voltage and current, V_{rect} is the DC rectified line input, and N is the turns ratio. In addition, sizing of M_1 must account for a substantial overshoot voltage at turn-off due to leakage inductance in the flyback transformer.

(a)   (b)

(c)
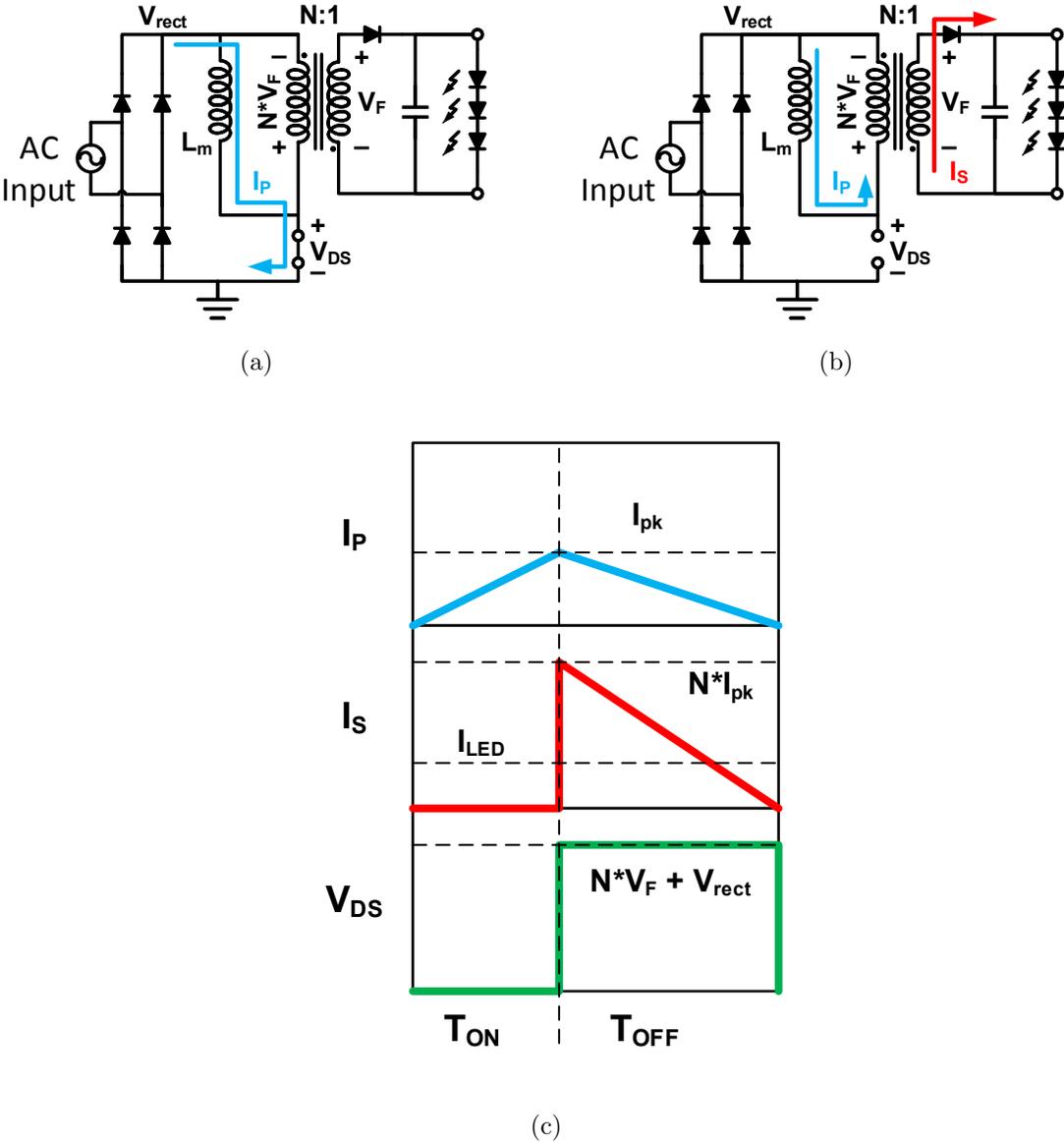
Figure 1.7: Analysis of a flyback LED driver operating in critical conduction mode, as depicted in [28]. (a) Equivalent circuit with switch ON. (b) Equivalent circuit with switch OFF. (c) Current and voltage transients in the flyback converter.

1.3.4   Resonant and Soft Switching LED Drivers

While resonant LED driver topologies have not yet had a major industiral impact, they have become quite prevalent in research [33–35]. Resonant converters often contain a resonant tank at the output. Adjusting the converter's switching frequency can modulate the resonant tank impedance, which ultimately makes it possible to regulate the output current. In certain designs, the resonant tank capacitors can also provide galvanic isolation [34, 35].

Another distinct benefit of the resonant converter is that it allows for soft switching [36–38]. With modern industrial demand on size and efficiency, it is increasingly clear that switching converters greatly benefit from zero voltage switching (ZVS). Zero voltage switching involves the use of resonant techniques to ensure that the drain-source voltage of an open power switch is zero before this device turns on. This is hugely beneficial in ensuring that the device is not blocking and conducting at the same time, thus reducing switch stress
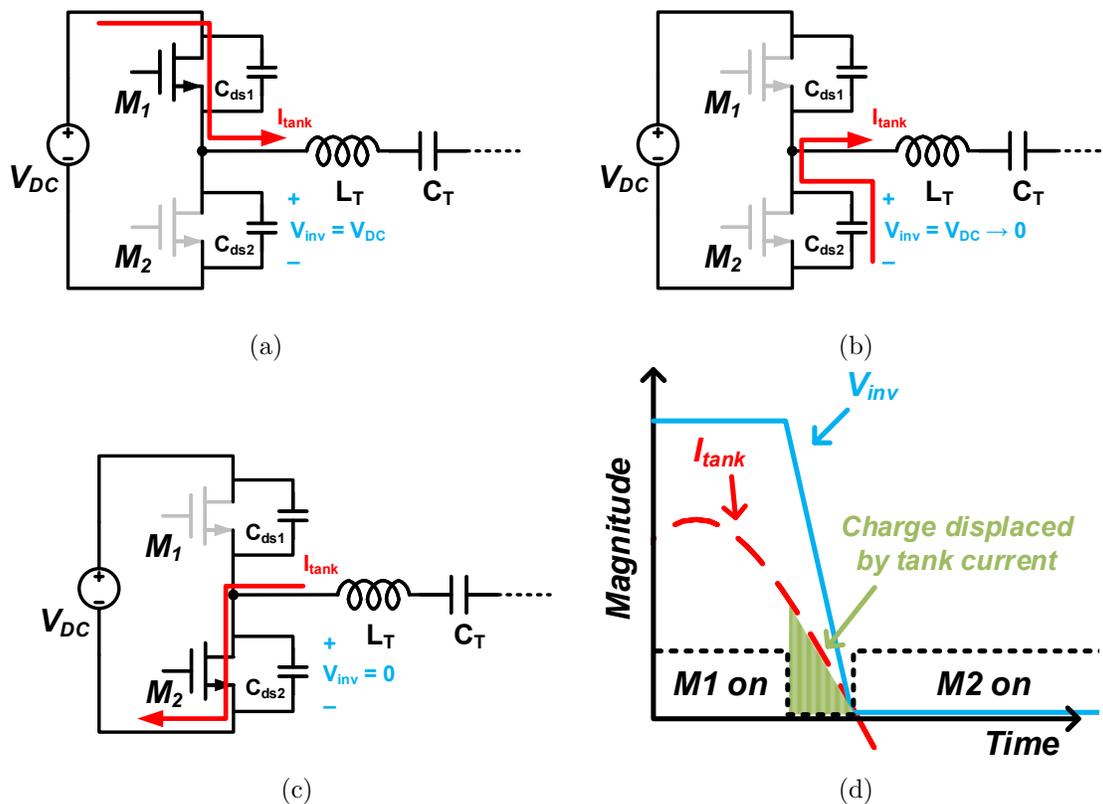
Figure 1.8: Zero voltage switching (ZVS) in a resonant half bridge. (a) When M1 is on, the inverter node V_{inv} is pulled high and the parasitic drain-source capacitance C_{ds2} is charged to V_{DC}. (b) During the dead time, the tank current I_{tank} discharges C_{ds2}. (c) M2 turns on when V_{inv} reaches zero. This way, there is zero voltage across M2 when it turns on. (d) Waveforms demonstrating ZVS.

and preventing shoot-through. Section 3.2.2 and appendix B.1 discuss how soft-switching techniques are important to the LED driver presented in this dissertation.

Even if switch stress is not a concern, ZVS is very beneficial in improving a converter's efficiency. Power MOSFETs often contain substantial parasitic drain-source capacitance C_{ds}. When a switch without ZVS turns on, the parasitic capacitor charge $q = C_{ds}v_{ds}$ flows through the channel as loss. Figure 1.8 illustrates how the resonant inductor can discharge the parasitic capacitance of switch M2 and allow for ZVS. In this case, the switching dead time is tuned based on the resonant frequency of C_{ds} with the tank inductor L_T. During this dead time, C_{ds2} is completely discharged and the drain-source voltage across M2 goes to zero. Once the drain-source voltage across M2 reaches zero, M2 should switch on. It is important to note that if M2 does not turn on as soon as C_{ds2} is discharged, the tank current I_{tank} will have to flow through the reverse diode of M2. Since the reverse diode introduces loss, it is best to turn on M2 exactly when its drain-source voltage is zero.

The final benefit of soft switching is that it reduces the high frequency harmonic switching noise that the converter would otherwise inject onto the line. ZVS smooths the current spikes that would otherwise be present at each switching edge.

Quasi-resonant converters are a type of converter that is mainly designed around soft switching. In many cases, the quasi-resonant converter topology comes from a standard converter topology, but with a small resonant tank near the power switch. Unlike normal resonant converters, quasi-resonant converters do not use a resonant tank to regulate output current. However, they still enjoy the benefits of increased efficiency and reduced EMI. Various quasi-resonant LED drivers have been proposed as soft switching variations of the flyback [39] or boost [40] LED drivers.

1.3.5 Switched Capacitor LED Drivers

Switched capacitor converters have recently been in the research spotlight for low to moderate power conversion. Unsurprisingly, they have been considered for lighting applications [34, 35]. The switched capacitor converter uses an array of switches and capacitors to perform conversion. Its major advantage is that no magnetics are required. As such, the switched capacitor converter is very amenable to integration.

As explained in Section 3.2.2, the output stage of the LED driver presented in this dissertation uses an isolated 4:1 H-bridge stack. For applications that do not require isolation, a 4:1 switched capacitor ladder can be used as an alternative output stage topology. Appendix B.1 directly compares the performance of the H-bridge stack and the switched capacitor ladder.

1.4 Power Ripple and Flicker

Flicker is a steady state oscillation in a lamp's intensity. As mentioned in Section 1.2, flicker is usually due to AC power ripple at the input of a lamp driver. This effect is most severe in LEDs due to their relatively fast luminous response to power. Low frequency flicker can

induce seizures in epileptics [20, 41]. In others, it may induce headaches, eye strain, and a loss of concentration. Humans can only perceive flicker up to 60-90 Hz. However, adverse biological effects may still occur in the presence of lights that flicker up to 200 Hz.

As mentioned in Section 1.2, incandescent lamps are naturally resistant to flicker because incandescence is a thermal process with a relatively slow time constant. Flicker was discovered to be an issue with the introduction of the fluorescent lamp [20, 41]. Early fluorescent lamps were magnetically ballasted and flickered at 120 Hz. Flicker was mitigated by assigning adjacent lamps in a room to different phases of a three-phase distribution. Once the electronic ballast became prevalent, fluorescent lamp flicker was pushed into the 20 kHz range, making it no longer problematic. As shown in Figure 1.9, electronically balasted fluorescent lamps barely have any flicker. In [41], percent flicker is defined as

$$\text{Percent Flicker} = 100\frac{\text{Max - Min}}{\text{Max + Min}} = 100\frac{\text{Max - Min}}{2(\text{Avg})}, \tag{1.4}$$

where Max, Min, and Avg refer to the maximum, minimum, and average luminous output, respectively.

With the introduction and popularity of LED lamps, it has once again become important to take measures to remove flicker. Flicker is a result of AC power ripple. When a lamp operates with unity power factor, its input current is sinusoidal and in phase with the line
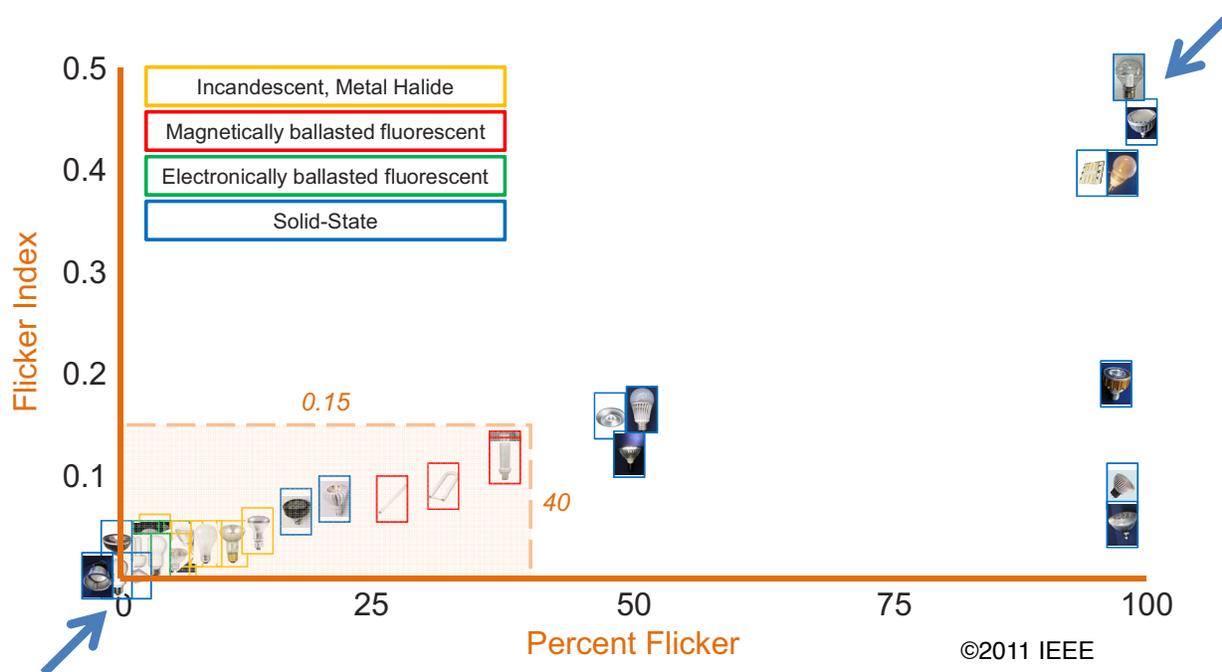
Figure 1.9: Flicker chart from [41] that displays percent flicker and flicker index for different types of lamps. LED lamps may fall on either side of the spectrum, depending on their quality and whether or not they contain ripple cancellation measures.

voltage. It follows that for line voltage $V\sin(\omega_0 t)$ and line current $I\sin(\omega_0 t)$, the input power is:

$$
\begin{aligned}
P_{in} = V\sin(\omega_0 t)I\sin(\omega_0 t) &= \frac{VI}{2} - \frac{VI}{2}\cos(2\omega_0 t) \\
&= P_{LED} + P_{RC}
\end{aligned}
\tag{1.5}
$$

where ω_0 is $2\pi 60$ in the US. The constant P_{LED} term is the average power and represents the desired DC output to the LEDs. The 120 Hz ripple power P_{RC} contributes directly to 120 Hz flicker. Thus, it is desirable to greatly reduce or cancel P_{RC} at the driver's output to the LEDs.

Many LED drivers use passive ripple cancellation. As shown in Figure 1.10a, passive ripple cancellation methods often involve the use of a large DC capacitor bank that filters the ripple power. This capacitor bank may either span the LED string, or reside at an intermediate post-rectification stage.

In order to be large enough to filter the low frequency power ripple, the passive DC capacitor bank often has to be implemented with electrolytic capacitors. Electrolytic capacitors are considerably more cost effective than ceramic capacitors for applications that

(a)

(b)
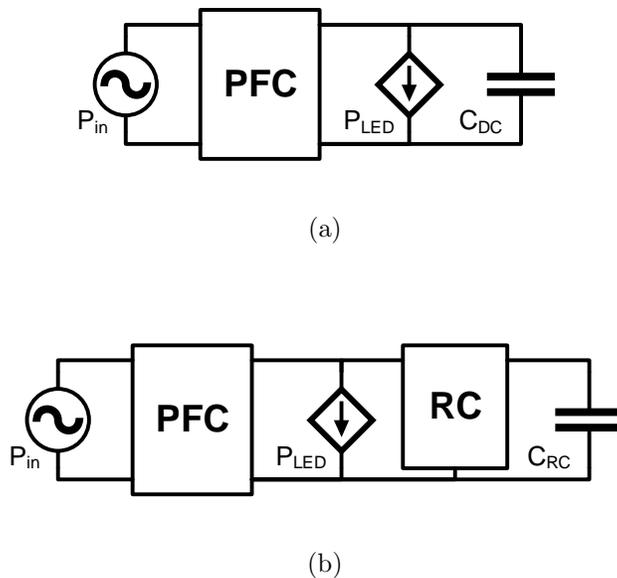
Figure 1.10: Methods for reduction or cancellation of 120 Hz power ripple from the driver's power-factor correction (PFC) input module. It is desirable for the driver's output to the LEDs, P_{LED}, to be constant. (a) Passive ripple cancellation involves the use of a large DC capacitor C_{DC} to filter the ripple. (b) An active ripple cancellation strategy that involves the use of a separate power converter for ripple cancellation. The ripple-cancellation (RC) module includes a storage capacitor C_{RC} that can be much smaller than C_{DC}.

require high capacitance and high voltage rating. However, electrolytic capacitors are a problematic component in LED drivers because they are bulky and have a limited life span [16, 17, 42–44]. Relatively high temperatures speed the evaporation of the liquid electrolyte, which can limit the life of the electrolytic DC capacitor to five years or less. Since the LEDs can last at least twice as long, addressing or removing the electrolytic capacitor is highly desirable. In addition, aging electrolytic capacitors have increasingly high equivalent series resistance (ESR), thus making them a source of loss. Finally, failures such as a short circuit or hydrogen buildup can cause electrolytic capacitors to explode.

In order to eliminate the electrolytic capacitor, there has been a push toward the research and development of high quality LED drivers that employ active ripple cancellation techniques [42, 44–47]. Active ripple cancellation techniques include multiple power conversion stages, discontinuous conduction mode (DCM) [44–46], resonant current control [47], and the addition of a separate ripple cancellation module [42].

The LED driver in this dissertation performs active ripple cancellation with a separate ripple cancellation module, shown in Figure 1.10b. The ripple cancellation module transfers energy to and from a storage capacitor C_{RC}. As shown in Section 1.4, the desired constant output power P_{LED} can be achieved if P_{RC} is transferred to the storage capacitor. In order to transfer power to the storage capacitor C_{RC}, the active ripple cancellation module can swing its voltage. This technique is explained further in Section 3.4.2.

An active ripple cancellation module has the benefit of greatly reducing the required capacitor size. To show this, consider a direct comparison between the passive and active ripple-cancellation strategies. As shown in Figure 1.10, the passive ripple-cancellation strategy requires a central DC capacitor C_{DC}, while the active ripple-cancellation module requires a storage capacitor C_{RC}. In this comparison, the design specifications will allow for a fractional amount of ripple power, F, to pass to the LEDs. As such, $P_{RC}F$ may be transferred to the LEDs, and $P_{RC}(1 - F)$ must be transferred to the DC or storage capacitor. The energy on the DC or storage capacitor is developed from Equation 1.5 as

$$
\begin{aligned}
P_{cap} &= (1 - F)P_{RC} = (1 - F)\frac{VI}{2}cos(2\omega_0 t) \\
E_{cap} &= \int P_{cap} = -(1 - F)\frac{VI}{4\omega_0}sin(2\omega_0 t) + E_{cap,0}.
\end{aligned}
\tag{1.6}
$$

The size of a capacitor capable of absorbing P_{cap} can be derived from the capacitor's energy swing as

$$
\begin{aligned}
\frac{1}{2}CV_{cap,max}^2 - \frac{1}{2}CV_{cap,min}^2 &= 2(1 - F)\frac{VI}{4\omega_0} \\
C(V_{cap,max} + V_{cap,min})(V_{cap,max} - V_{cap,min}) &= (1 - F)\frac{VI}{\omega_0} \\
C = (1 - F)\frac{VI}{\omega_0(2V_{cap,avg})(V_{cap,swing})}
\end{aligned}
\tag{1.7}
$$

where $V_{cap,swing}$ is the maximum allowed peak-peak voltage range the capacitor can swing, and $V_{cap,avg}$ is the average DC voltage of the capacitor.

The passive ripple-cancellation strategy in Figure 1.10a places the DC capacitor across the constant current LED string, such that $V_{cap,avg} = V_{LED}$. Since the allowed ripple power to the LEDs is $P_{RC}F$, $V_{cap,swing}$ must be constrained to $V_{cap,swing} = V_{LED}F$. The required DC capacitor size is thus

$$C_{DC} = \frac{(1-F)}{2F} \frac{VI}{\omega_0 V_{LED}^2} \tag{1.8}$$

The active ripple-cancellation strategy in Figure 1.10b has an uncoupled storage capacitor whose voltage is allowed to swing between ground and V_{LED}. If the ripple-cancellation module is implemented with a buck-boost converter, the storage capacitor voltage may even swing above V_{LED}. For this analysis, the maximum storage capacitor voltage is constrained to V_{LED}, and thus the required storage capacitor size is

$$C_{RC} = (1-F)\frac{VI}{\omega_0 V_{LED}^2} = (2F)C_{DC}. \tag{1.9}$$

The result of this analysis shows that the required size of the passive method's DC capacitor C_{DC} is much larger than the required active method's storage capacitor C_{RC}. Consider the design of a 20 W LED driver with an output stage voltage (P_{LED}) of 180 V, and output ripple equivalent to an incandescent bulb. An A19 incandescent bulb has 6.6% flicker [20, 41], and so the LED driver should be designed for $F = 0.066$. The active ripple-cancellation driver requires $C_{RC} = 1.5\mu F$, and the passive ripple cancellation driver requires $C_{DC} = 12\mu F$. Table 1.1 shows that the passive ripple cancellation driver likely requires an electrolytic capacitor.

Digikey Part	Type	Cap	Voltage	Cost	Dimensions	Volume
565-3243-2-ND	Ceramic	$1.5\mu F$	250V	$1.17	6x5.3x5.5mm	$175mm^3$
565-4657-3-ND	Ceramic	$10\mu F$	250V	$20.75	28.5x7.5x20mm	$4275mm^3$
493-1192-ND	Electrolytic	$10\mu F$	250V	$0.47	314x14.5mm	$4553mm^3$

Table 1.1: Several capacitors for ripple cancellation found on Digikey [48]. The top row is intended for active ripple cancellation, and the bottom two are for passive. The volumetric requirements are much less in active ripple cancellation. For passive ripple cancellation, the cost of a ceramic capacitor is prohibitively high, and its volume is similar to an electrolytic equivalent.

1.5 Outline of Dissertation

This dissertation presents the design and verification of a novel LED driver topology. The driver uses multilevel circuit methods and sigma-delta control to address the design challenges in Section 1.2. It also uses active ripple cancellation, as recommended in Section 1.4.

Chapter 2 presents the design specifications for the driver, and provides an introduction to multilevel circuits and sigma-delta modulation. Chapter 3 presents an in depth description of the circuits and control used in the LED driver. Finally, Chapter 4 explains the method of testing and verification, presents the data and results, and suggests topics for future work.

Chapter 2

Multilevel Converters and Sigma Delta Control

2.1 Project Specifications

The goal of this dissertation is to design a high quality and economic LED driver. In order for this LED driver to be practical, it must overcome the design challenges discussed in Section 1.2. The design specifications for the driver are intended to make it competitive with a high quality commercial flyback LED driver (discussed in Section 1.3.3). These specifications are:

- High efficiency.

- Power-factor correction on 60 Hz AC input.

- Dimming capability and current regulation to the LEDs.

- Galvanically isolated DC power is output to the LEDs.

In order to surpass the Flyback LED driver, a couple of additional specifications are imposed:

- Cancellation of 120 Hz power ripple from input without the use of electrolytic capacitors.

- Smaller form factor (i.e. no flyback transformer).

The LED driver in this dissertation involves multilevel circuit techniques introduced in Section 2.2, and a sigma-delta control strategy introduced in Section 2.3. In Chapter 3, the driver's actual design architecture is discussed in detail.

2.2   Multilevel Converters

Multilevel converters are a class of power converters that distribute the switching functionality and stress over an array of vertically stacked power switches. This dissertation introduces multilevel circuit methods to the integrated LED driver space as a means of addressing the challenges mentioned in Section 1.2 while also reducing the volumetric requirements for passive elements.

As shown in Figure 2.1, multilevel converters are capable of connecting their inverter node to one of several DC levels. The DC levels are maintained on a DC bus, which is usually implemented with actively balanced capacitors. The standard half-bridge inverter in Figure 2.1a can be considered as a two-level inverter, capable of outputting GND or V_{DC}

(a)

(b)
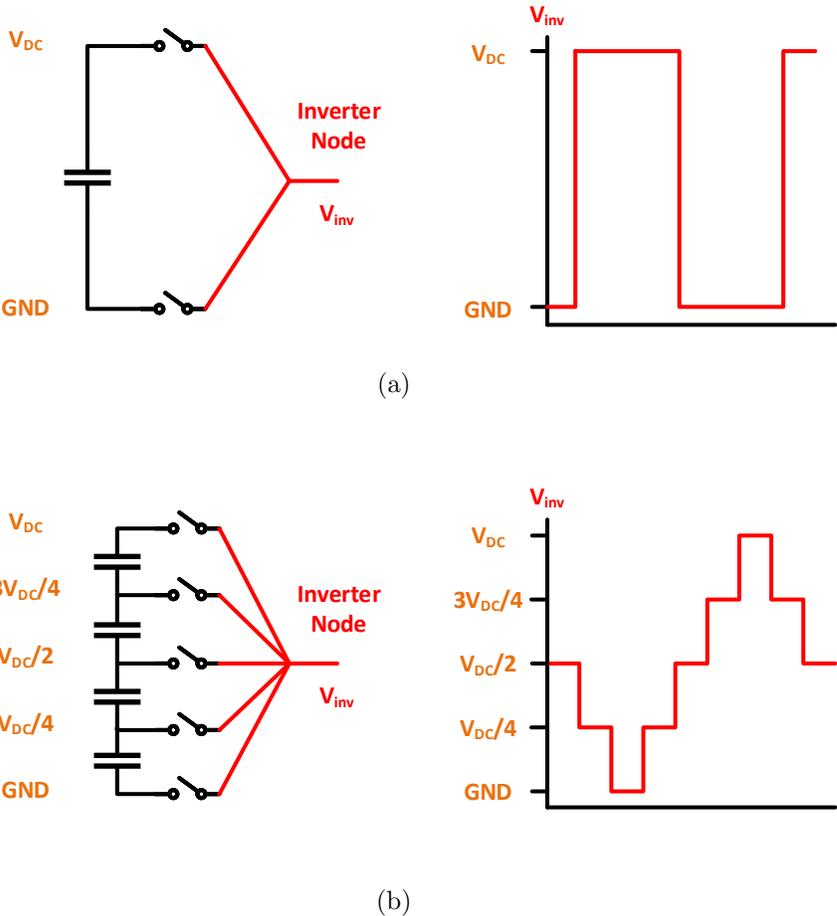
Figure 2.1: Theoretical multilevel converters. V_{inv} can be connected to any of the levels of the DC capacitor bus, producing the output waveforms on the right. (a) Two-level inverter, or half-bridge. (b) Five-level inverter.

at the inverter node. The five-level inverter in Figure 2.1b can set the inverter node output to GND, $V_{DC}/4$, $V_{DC}/2$, $3V_{DC}/4$, or V_{DC}. For linearly spaced DC levels, the number of DC capacitors needed is one less than the number of levels.

Multilevel inverters have become popular in the last decade as a means to utilize lower voltage solid-state switches in high voltage applications [49]. They have the advantage of reducing individual switch stress by distributing a high voltage drop over multiple switches. Multilevel inverters also have the ability to output one of several voltage levels, thus allowing for greatly reduced harmonic content compared to the standard two-level inverter. This feature ultimately allows for the reduction in a converter's switching frequency or passive filtering requirements.

Various multilevel inverter topologies have been proposed, such as the diode-clamped [50], capacitor-clamped [51], and cascaded topologies [52]. Several of these topologies can function bidirectionally. In addition, several of these topologies can be simplified to function as rectifiers, such as the Vienna rectifier [53].

2.2.1 Diode Clamped Multilevel Inverter

The diode-clamped multilevel inverter was the earliest published multilevel inverter topology [50]. As shown in Figure 2.2, the diode-clamped multilevel inverter consists of an array of vertically stacked switches, along with diodes connected to an intermediate DC level. The
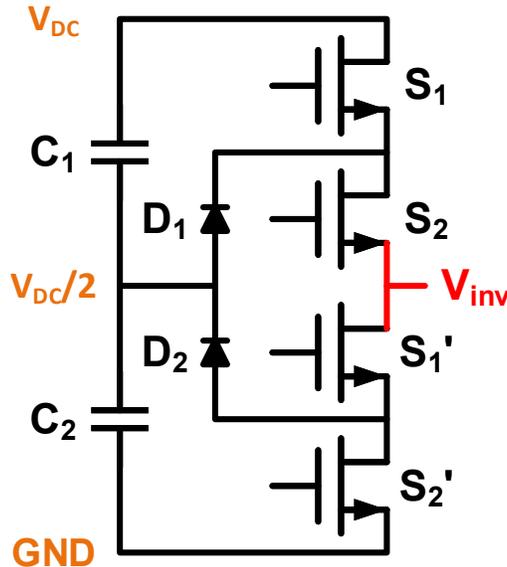
Figure 2.2: Diode clamped three-level inverter. Any switch S_x switches complementary to S_x'.

switch operation is as follows:

- To set V_{inv} to V_{DC}, S_1 and S_2 are both on.

- To set V_{inv} to $V_{DC}/2$, S_1 is off and S_2 is on.

- To set V_{inv} to GND, S_1 and S_2 are both off.

Note that switches S_1' and S_2' are complementary to S_1 and S_2, respectively.

The diode-clamped multilevel inverter is advantageous for its simplicity. The diodes automatically clamp the inverter node voltage as necessary, which allows the switching configuration to be fairly simple. However, there are several notable disadvantages to the diode-clamped topology. First, the DC capacitors C_1 and C_2 must have a means of balancing themselves such that their intermediate level is held constant at $V_{DC}/2$. Second, the diode paths may present a substantial voltage drop, particularly in lower power applications. Replacing the diodes with active switches can increase efficiency at the cost of increased complexity. Finally, when the number of levels increases, the number of series diodes in each chain also has to increase in order to abide by the diode voltage ratings. However, the number of diode chains also increases with the number of levels. Thus the total number of diodes increases quadratically with levels, making the diode-clamped circuit expensive for applications that require many levels.

2.2.2 Capacitor Clamped Multilevel Inverter

The capacitor-clamped multilevel inverter is an alternative multilevel topology that does not require diodes [51]. As shown in Figure 2.3, the capacitor-clamped multilevel inverter is very similar to the diode-clamped inverter, except that the output is instead straddled by a flying capacitor C_F. C_F is ideally biased at the voltage of a DC level. The switch operation is as follows:

- To set V_{inv} to V_{DC}, S_1 and S_2 are both on (S_1' and S_2' are both off).

- To set V_{inv} to $V_{DC}/2$, there are two possible configurations. In one configuration, S_1 and S_1' are both on (S_2 and S_2' are both off). In the other configuration, S_2 and S_2' are both on (S_1 and S_1' are both off).

- To set V_{inv} to GND, S_1 and S_2 are both off (S_1' and S_2' are both on).

The voltage level of the flying capacitor C_F is only affected during the state when V_{inv} is set to $V_{DC}/2$. C_F is charged if S_1 and S_1' are on, and discharged if S_2 and S_2' are on. Proper switching control and toggling between the two switch configurations of the $V_{DC}/2$ state allows for the voltage on C_F to be properly maintained.

The capacitor-clamped multilevel inverter has the advantage of eliminating the diode drop present in the diode-clamped inverter, thus making it theoretically more efficient. However, it requires a more complex control algorithm in order to ensure the proper voltage across C_F.
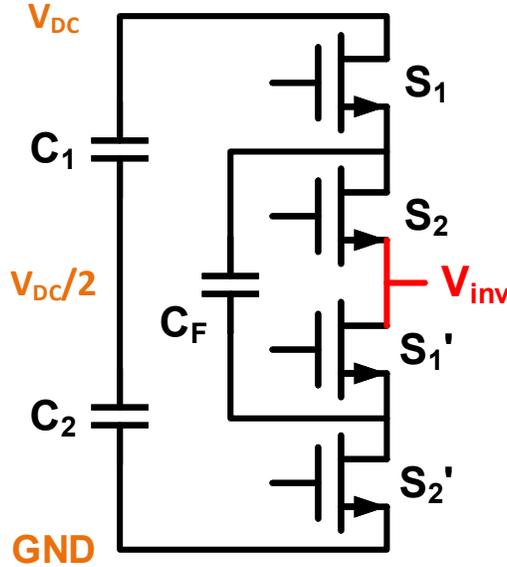
Figure 2.3: Capacitor clamped three-level inverter.

Like the diode-clamped inverter, the capacitor-clamped inverter suffers a similar quadratic scaling problem with the number of required capacitors. Under heavy load conditions, the capacitor-clamped inverter may require an external means of balancing the DC capacitor voltage. However, this requirement can optionally be avoided if C1 and C2 (in Figure 2.3) are combined as a single high voltage capacitor.

2.2.3 Multilevel Topology for an Integrated LED Driver

Since multilevel converters involve many active devices, integrated circuit (IC) technology is a convenient means of producing an efficient low-cost LED driver with small form factor. IC applications often revolve around integrating full systems onto a single chip. However, many silicon processes have device voltage limitations that would present a challenge for the design of fully integrated power systems. As such, it is natural to develop the driver using a multilevel topology so as to reduce voltage stress on each individual power switch. Overall performance may be evaluated with techniques developed in the switched capacitor design frameworks [54, 55].

In this dissertation, the multilevel circuit function is used in two positions, one to provide power-factor correcting (PFC) rectification, and a second to provide bidirectional power flow for ripple cancellation. The generalized multilevel topology [56] is chosen because it addresses both of these functions and admits a fairly regular gate drive pattern. Other choices may very well be advantageous in optimizing die area. The generalized multilevel

topology is further discussed in Section 3.2.1.

2.2.4   Control Scheme for a Multilevel Converter

Several control strategies exist for inverters and active rectifiers. Popular methods include sinusoidal Pulse Width Modulation (PWM), Space Vector Modulation [57], and Selective Harmonic Elimination [58].

This dissertation uses sigma-delta modulation [59] because of its ability to cancel harmonics and its simplicity for single-phase input power. Sigma-delta modulation is further discussed in Section 2.3, and its use in a multilevel converter is discussed in Section 3.4.

2.3   Sigma-Delta Modulation

Sigma-delta modulation is a strategy for converting an analog signal into a digital signal. It is most often used for signal conversion in electronics. Sigma-delta analog to digital converters (ADCs) are useful for their simplicity. If high bandwidth is required, the flash or successive approximation ADC may prove to be a better choice. However, if high resolution and simple hardware are more desirable, sigma-delta modulation is the method of choice.

Sigma-delta modulation is also useful as a control strategy in power electronics. In particular, motor drivers require a modulation method for controlling an H-bridge, which is essentially a 1-bit ADC. Power electronics applications often have relatively low bandwidth requirements, and so the simplicity of a sigma-delta modulation loop is very appealing.

2.3.1   Quantization

In an ADC, the process of signal conversion from continuous to discrete amplitude is known as quantization [60–64]. The ADC can be referred to as a quantizer to emphasize the quantization process.

Every quantization process has a quantization error e, which is the difference between the desired output (i.e. the input) and the actual output of the quantizer. Since the quantization error signal is undesirable, it is known as the quantization noise. As shown in Figure 2.4, the quantizer can be modeled as the sum of the desired analog signal and an undesirable quantization noise.

In order to evaluate the overall accuracy of the quantizer, the total quantization noise power is measured as the variance of the quantization error. It is commonly assumed that the quantization error is uniformly distributed over the quantization step. As such, the quantization noise power is

$$\sigma_n^2 \;\; = \;\; E[e^2] = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 = \frac{\Delta^2}{12} \tag{2.1}$$

where Δ is the quantization step size.

(a) (b)
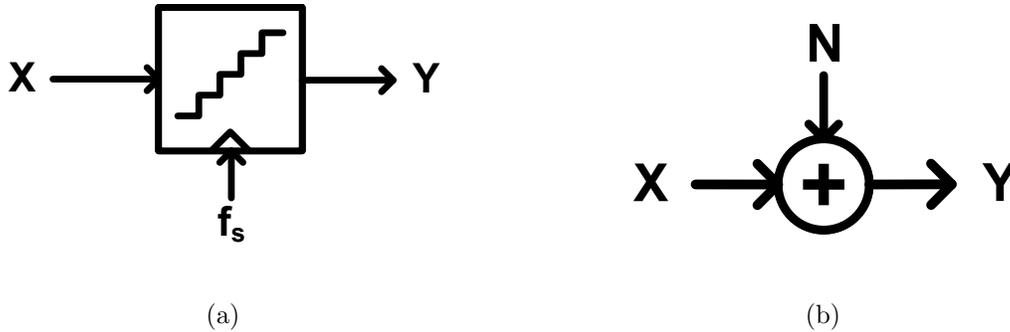
Figure 2.4: (a) A quantizer block with a sampling rate f_s and quantization noise. (b) Equivalent small signal model with a noise input N.

Another common assumption is that the quantization error is a white process. As such, the quantization noise power is spread uniformly over the frequency range. The quantization noise power spectral density is

$$N(f) = \frac{\Delta^2}{12 f_s} \qquad (2.2)$$

where f_s is the sampling frequency of the ADC. If f_s is increased, the noise power is spread more thinly over the spectrum, and thus $N(f)$ decreases.

2.3.2 Noise Shaping with a Sigma-Delta Loop

Sigma-delta modulation invokes closed loop control to shape the noise power spectrum $N(f)$ [60–64]. In practice, the sigma-delta loop functions to push the quantization noise to higher frequencies, after which it can easily be filtered out. Intuitively, the output of the sigma-delta modulator attempts to best approximate the input, as shown in Figure 2.5.

A first order sigma-delta loop is shown in Figure 2.6. The only hardware required is an integrator and a quantizer, thus lending to the simplicity of the control scheme. In power applications, the quantizer is already present as an H-bridge or multilevel converter.

As mentioned in Section 2.3.1, the noise power is analyzed by replacing the quantizer with a noise input. The noise analysis block diagram is shown in Figure 2.6. Evaluating the full loop reveals the signal transfer function $Y(s)/X(s)$ and noise transfer function $Y(s)/N(s)$ to be

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \qquad (2.3)$$

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1}. \qquad (2.4)$$

Input

Output
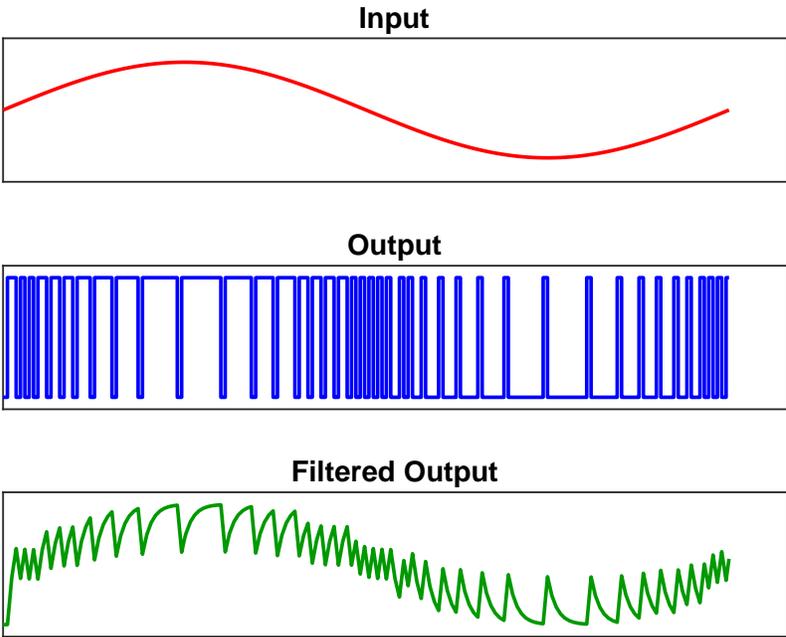
Filtered Output

Figure 2.5: Sample output waveforms of a sigma-delta modulator. The filtered output uses a low pass filter with cutoff frequency at $f_s/2$.
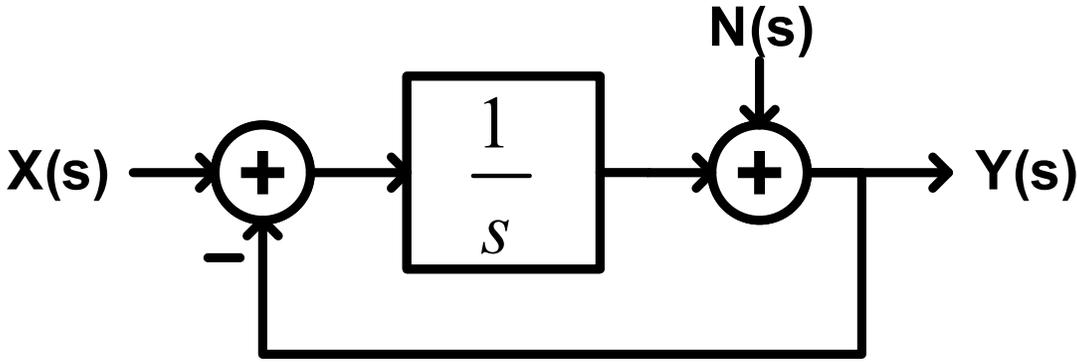
Figure 2.6: Small signal block diagram of a sigma-delta modulator. The input is $X(s)$, the output is $Y(s)$, and the quantization noise input is $N(s)$. The transfer functions in Equations 2.3 and 2.4 can be derived from this block diagram. The filtered output in Figure 2.5 can be obtained by passing $Y(s)$ through a low pass filter.

In other words, the sigma-delta loop acts as a low pass filter for the signal and a high pass filter for the noise. In this way, the noise is pushed to the higher frequencies. It is also necessary to include a low pass filter at the output in order to remove most of the noise.

2.3.3 Higher Order Sigma-Delta Loop

There are several ways to reduce the quantization noise of a sigma-delta modulator [60–64]. First, an increase in the quantizer resolution will decrease Δ, which will decrease the quantization noise power. Second, an increase in f_s will increase the cutoff frequency of the noise transfer function, thus reducing noise in the signal band. Finally, a higher order sigma-delta loop can be implemented.

Higher order sigma-delta loops reduce noise in the signal band at the cost of increased noise at high frequencies. They also require more hardware. However, as shown in Figure 2.7, the noise reduction in the signal band can be quite significant and it is often worth
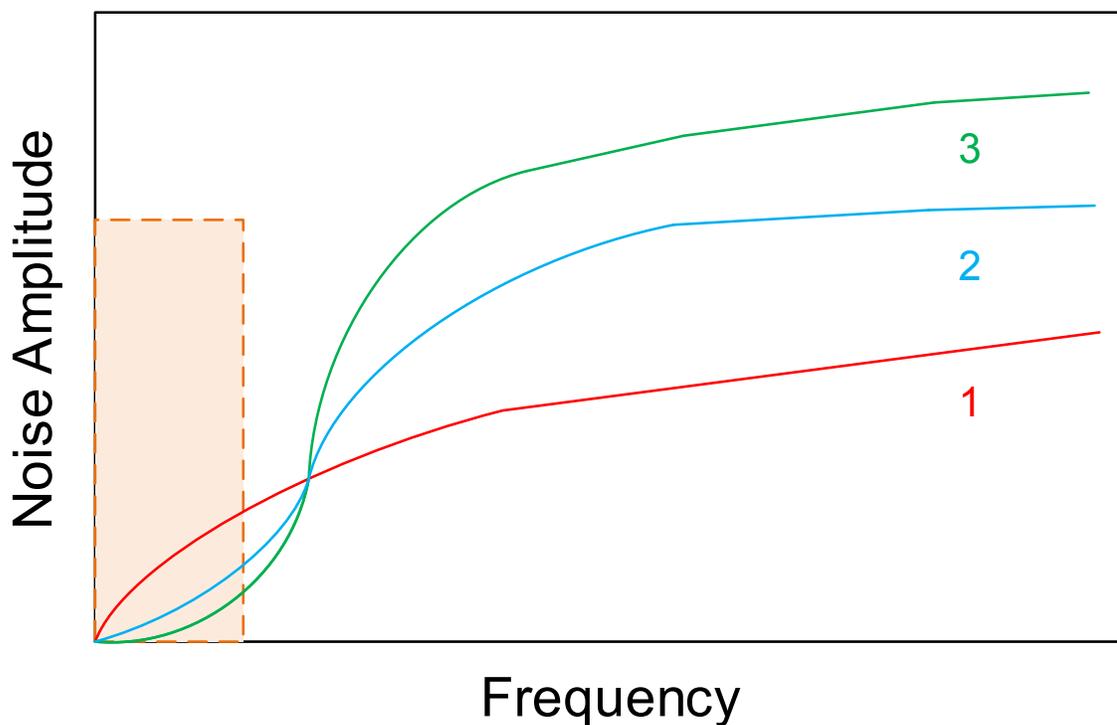
Figure 2.7: Noise transfer function for a 1st, 2nd, and 3rd order sigma-delta modulator. An output low pass filter could be designed to cut out the high frequency noise, as indicated by the orange rectangle. Higher order sigma-delta modulators have lower quantization noise in the signal band, but higher quantization noise at higher frequencies.

using a higher order sigma-delta modulator. In this dissertation, a second order sigma-delta modulator is used for power factor correction, and a first order sigma-delta modulator is used for ripple cancellation. Section 3.4 discusses the design of these sigma-delta modulators.

2.4   Research Contribution

Since LEDs have become mainstream in the lighting industry, compact and high performance LED drivers have become increasingly crucial. This dissertation uses multilevel circuit techniques and sigma-delta control to address the pressing need for a compact and high quality driver. The research results discussed in this dissertation can be used in a variety of other applications at low to moderate power.

In this dissertation, a generalized multilevel converter with sigma-delta control is designed and prototyped for LED lighting. Previous works have detailed the physical construction of diode-clamped or capacitor-clamped multilevel inverters for general power applications [50, 51]. However, very few have built a generalized multilevel converter. Sigma-delta control for multilevel inverters has been simulated in other papers [59, 65–68] but has seldom been put to practice, especially in rectification. Finally, multilevel circuit methods are almost nonexistent in the LED lighting space [69]. This dissertation confirms multilevel topologies as being useful and practical in LED drivers.

Most importantly, this dissertation introduces multilevel converters to the power IC space. DC-DC circuits such as the switched capacitor (SC) circuit have had the recent spotlight in the emerging field of power ICs [34, 54, 55, 70]. However, the research in this dissertation documents one of the first attempts to build a fully integrated multilevel converter, thus introducing a number of engineering benefits and challenges to the fields of multilevel converters and power ICs.

Chapter 3

LED Driver Design Architecture

3.1 Full System Architecture

A block diagram for the complete LED driver is shown in Figure 3.1. The driver contains an input power-factor correction (PFC) rectifier, a ripple-cancellation (RC) circuit, a DC capacitor bus, and an output stage. The PFC rectifier converts the AC line voltage to DC with low harmonic current injection, and provides for input current regulation and dimming. The dimming level is directly controlled by the input current regulation since subsequent stages simply convert this current and feed it to the LED string. Voltage regulation is effected by the LED string voltage-current characteristic. The ripple-cancellation circuit cancels ripple on the DC capacitor bus. Finally, the output stage down-converts the DC bus voltage and uses a small transformer to provide for galvanic isolation.
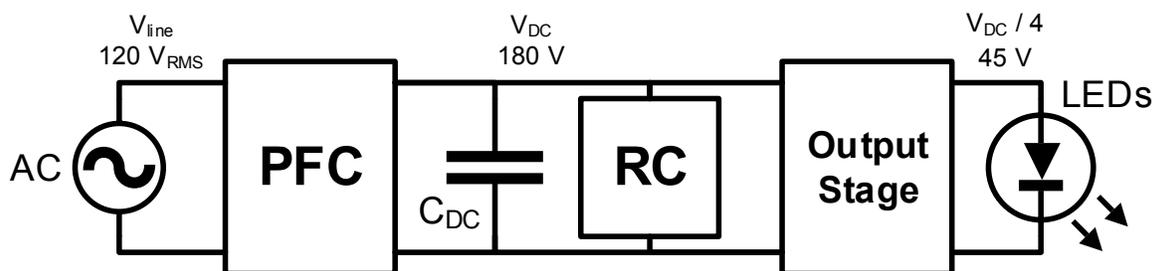
Figure 3.1: Block diagram of the LED driver with power-factor correction (PFC), ripple cancellation (RC), and output stage. C_{DC} indicates the DC capacitor bus.

3.2   Multilevel Switching Topologies

3.2.1   Multilevel Switch Topology for the PFC and Ripple Cancellation Module

The power-factor correction (PFC) rectifier and ripple-cancellation modules use a generalized multilevel topology, as shown in Figures 3.2 and 3.3. Each switching column contains transistors that switch synchronously and alternate in complementary pairs. By switching the various columns high or low, the inverter node can be connected to any of the five DC levels. Each column connects to a set of smaller integrated flying capacitors, which assist in rapidly stabilizing the column voltages and serve as a supply for the gate drivers. This topology is bidirectional, allowing the circuit to be configured as a rectifier or inverter, for PFC and ripple cancellation, respectively. As mentioned in Section 2.2.3, the generalized multilevel topology is chosen for its flexibly and fairly regular gate drive pattern. It can also self-balance the DC capacitor bus such that the voltages across the DC capacitors are equal [56].

The generalized multilevel converter has several degrees of freedom in connecting the inverter node to DC levels 1-3. For example, to access level 1, any one of the four columns must be held high, and the rest are held low. As such, there are four possible switch combinations for level 1: 0001, 0010, 0100, and 1000. Sections 3.3 and 4.4.1 explain how multiple equivalent switch combinations can be a very useful feature.

The power-factor correction (PFC) rectifier functions to enforce unity power factor and control the input power. As shown in Figure 3.2, the PFC rectifier can control the voltage at the inverter node. In this way, the PFC rectifier can set the voltage across the input inductor, and thus control the input current. Fine control over the input current enables harmonic reduction and allows for dimming via current control.

A 60 Hz input current in phase with a 60 Hz input voltage will generate 120 Hz input power. If this power ripple is not canceled from the DC bus, the LEDs will flicker at 120 Hz. Passive ripple cancellation is possible with large electrolytic capacitors on the DC bus. However, as discussed in Section 1.4, the use of electrolytics will increase the size and decrease the life span of the LED driver.

The ripple-cancellation module functions to actively cancel ripple from the DC capacitor bus, thus greatly reducing the required DC capacitor size and obviating the need for electrolytics. As shown in Figure 3.3, the ripple-cancellation circuit is able to transfer energy from the DC capacitor bus to the storage capacitor by precisely swinging the storage capacitor voltage.
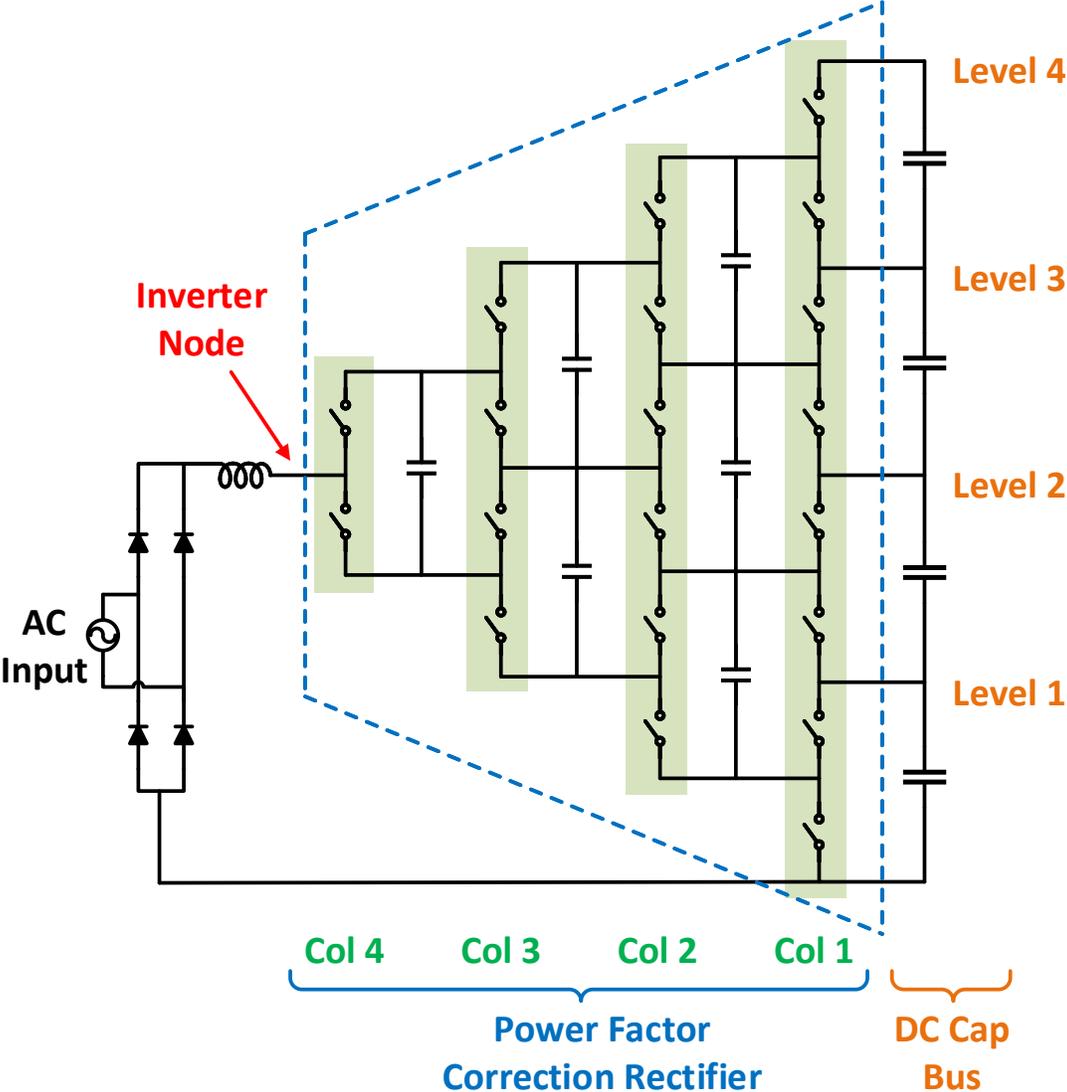
Figure 3.2: Generalized multilevel schematic for the PFC rectifier with switching columns highlighted in green. The DC capacitor bus helps define the DC levels, buffers power flow, and connects to the output stage (not shown here). It is shared with the circuits in Figures 3.3 and 3.4.
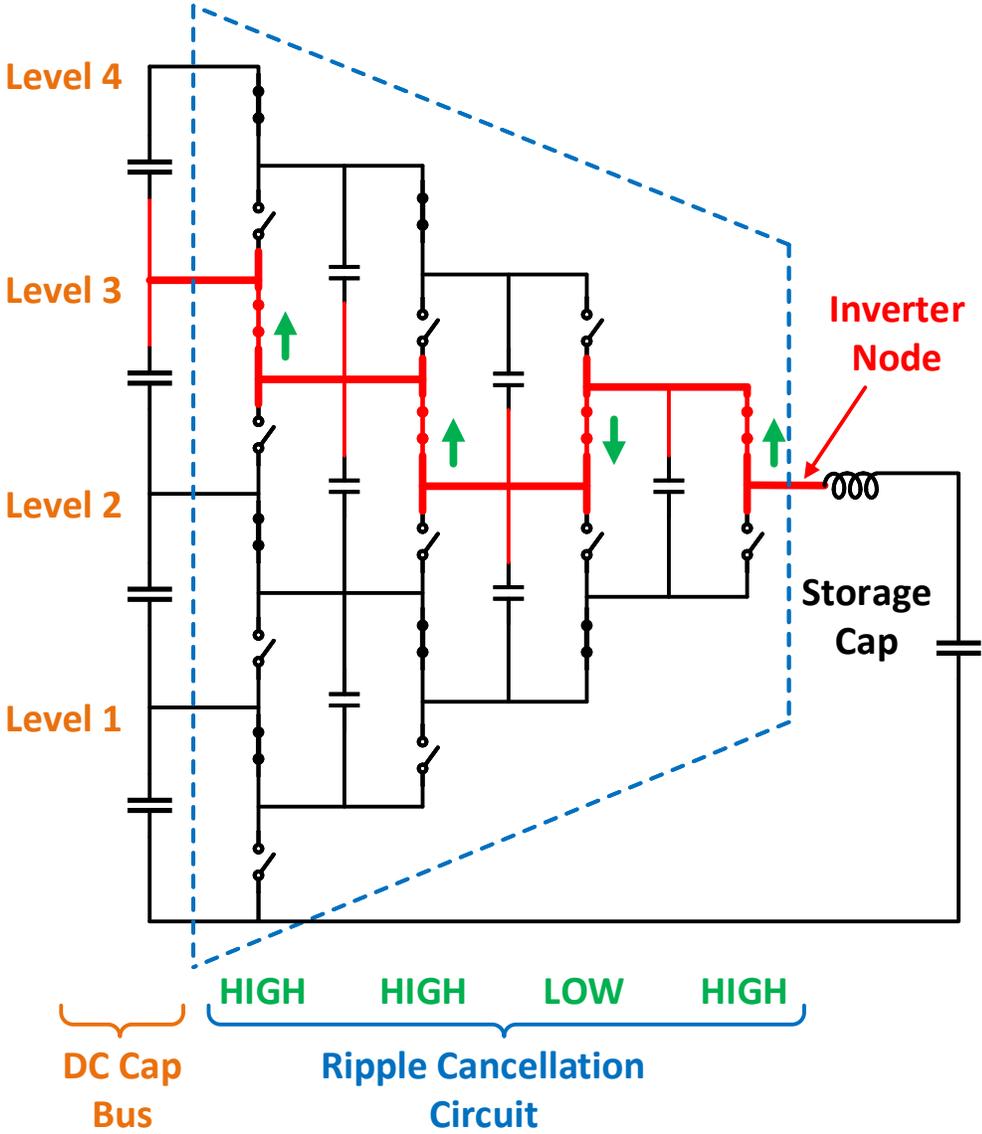
Figure 3.3: Generalized multilevel schematic for the ripple-cancellation module with an example switch configuration for connecting the inverter node to level 3. The DC capacitor bus helps define the DC levels, buffers power flow, and connects to the output stage (not shown here). It is shared with the circuits in Figures 3.2 and 3.4.

3.2.2   Output Stage

As shown in Figure 3.4, power is provided to the LEDs through the output stage, which consists of an array of stacked H-bridges and an output transformer. The output stage functions as a fixed-ratio 4:1 series-parallel step-down circuit, which serves to step the 180 V DC capacitor bus voltage down to the 45 V LED output. Another function of the output stage is to facilitate in balancing the voltage levels on the DC capacitor bus, which is crucial for correct operation of the power-factor correction (PFC) and ripple-cancellation modules.
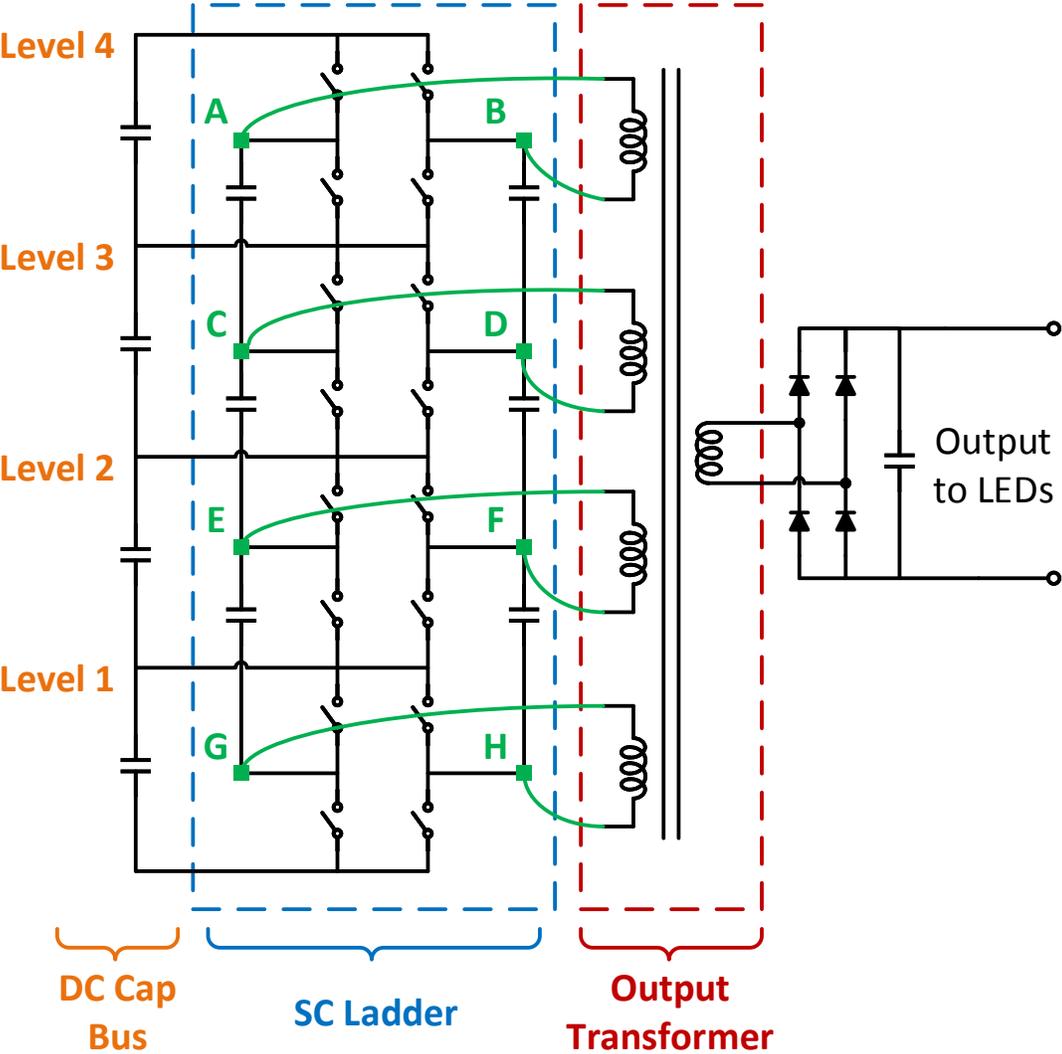
Figure 3.4: The output stage is comprised of an integrated H-bridge stack and an output transformer. The H-bridge stack is clocked at 50 kHz. The DC capacitor bus is shared with the circuits in Figures 3.2 and 3.3.

Alternative DC-DC topologies that provide these functions are discussed in [34].

Each of the inverter nodes in the H-bridge stack is connected to a small isolation transformer. This transformer has four primary windings and one secondary, all of which have the same number of turns. The transformer is useful in galvanically isolating the LEDs from the high voltage circuits, and in facilitating the series-parallel connection of this stage. In addition, it enables soft switching for the H-bridge stack via its leakage and magnetizing inductance. This transformer is not designed to store energy, and so it can be substantially smaller than that of an equivalent flyback converter. Its size is determined by the desired switching frequency of the H-bridge stack. Even with a small toroid, the H-bridge stack can be clocked at 50 kHz or lower.

3.3 Gate Driver Architecture

The dimensions of a power MOSFET are related to its stress handling capability. Its on-resistance and current handling capability are both directly correlated with the device width. The device breakdown voltage is somewhat correlated with its channel length and doping. The MOSFET's parasitic gate capacitance, however, is related to the product of its length
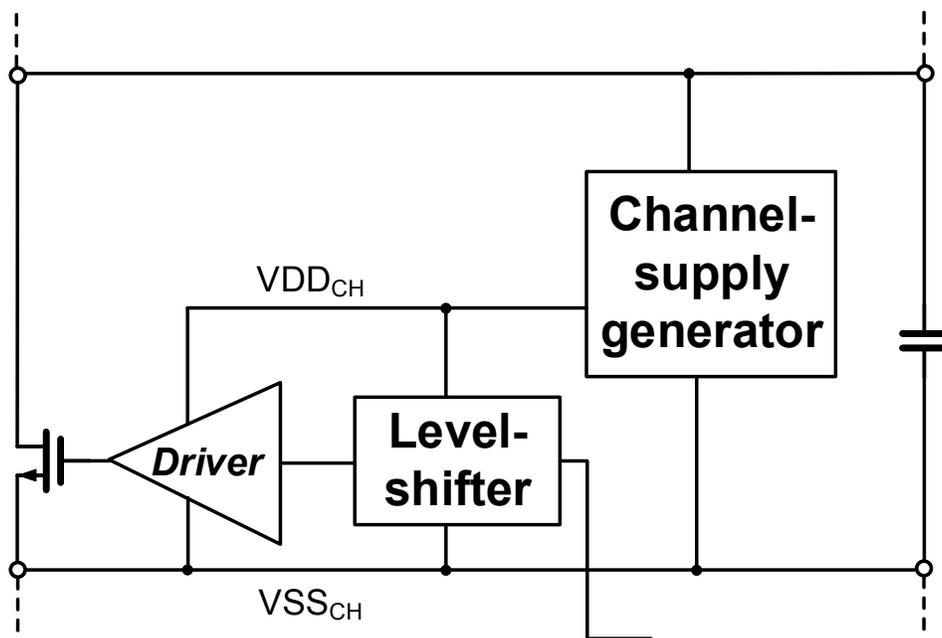
Figure 3.5: The full switching channel for the power LDMOS switch. Each switching channel consists of a high-side channel supply, a level shifter, and a driver (buffer). The channel supply is powered from a DC or flying capacitor and generates the VDD_{CH} voltage at five volts above VSS_{CH}.

and width. High power MOSFET switches have a large device area and high gate capacitance, and so they require gate drivers. In many power applications, the gate driver is packaged separately from the power switch. For an on-chip power converter, the gate drivers are integrated with the N-type LDMOS power switch into a unified switching channel.

The architecture for the switching channel is shown in Figure 3.5. Each channel includes a floating channel supply generator, a level shifter, and a driver. The channel supply uses power from a DC or flying capacitor to create a floating 5 V supply. Its function is to provide power to the level shifter and the driver. The level shifter is responsible for shifting a low voltage digital signal up to the floating voltage domain. Finally, the driver is a buffer that amplifies the floating digital signal with enough power to drive the gate capacitance of the power switch.

The channel supply generator, is responsible for creating a floating supply rail, VDD_{CH}, and regulating it at five volts above the source of the power switch, VSS_{CH}. As shown in
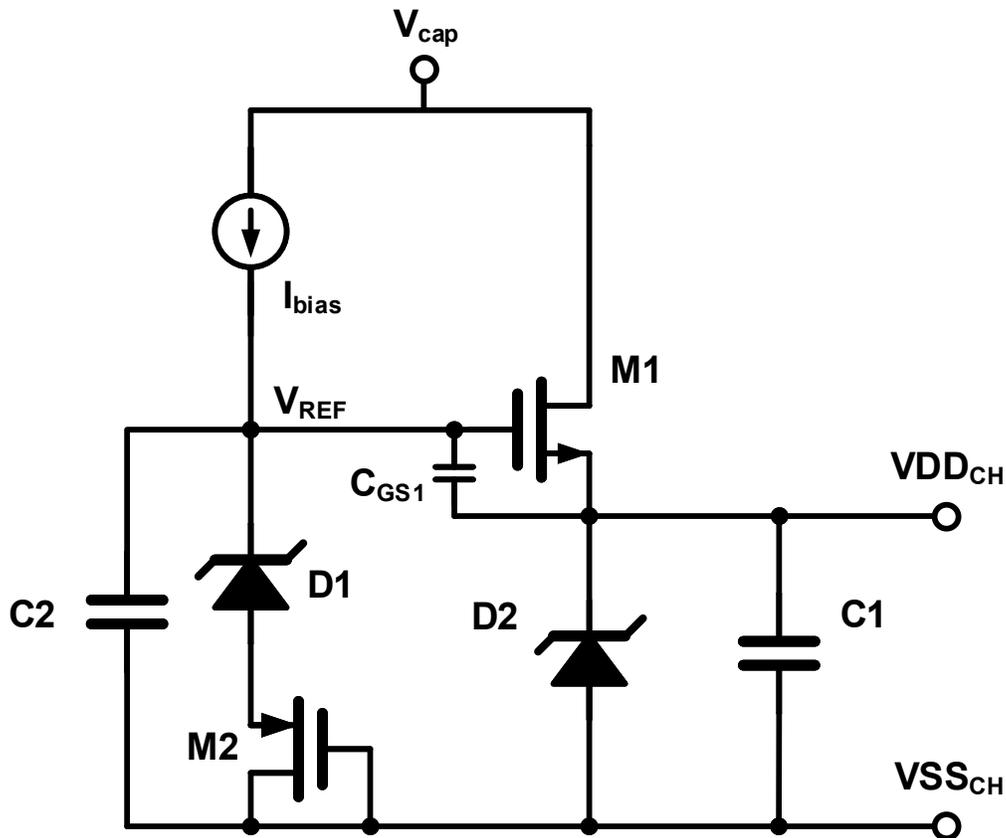
Figure 3.6: The channel supply generator for the switching channel is a low dropout (LDO) regulator. The main LDO power transistor M1 uses circuit feedback to fix the output VDD_{CH} at five volts above VSS_{CH}.

Figure 3.6, the channel supply is a low dropout (LDO) regulator.

For each channel supply, a bias current I_{bias} is generated in the ground domain. In the floating domain, this bias current passes through the 5.6 V zener diode D1, which fixes the reference voltage V_{REF}. The main LDO power transistor M1 uses circuit feedback to fix the output VDD_{CH} at five volts above VSS_{CH}. VDD_{CH} droops whenever the level shifter and driver draw power from the channel supply. A droop in VDD_{CH} increases the gate-source voltage across M1, which ultimately increases the current available to the level shifter and driver.

The other components and devices shown in Figure 3.6 are included for increasing the performance of the channel supply. C1, C2, and D2 assist in stabilizing V_{REF} and VDD_{CH}. They are particularly important in the floating channels that sit on flying nodes. The diode-connected transistor M2 acts as a diode drop, and functions to slightly increase the voltage on V_{REF}. This increase compensates for the gate-source drop of M1.

The level shifter functions to shift a digital signal in the ground domain up to the high-side floating domain. As shown in Figure 3.7, the level shifter is a differential amplifier with a single-ended output. This circuit also uses a positive feedback path to increase the transition speed of the level shifter output. When the differential input switches, the feedback path injects a pulse of current.

The switching channel structure in Figure 3.5 is used for all of the switches except the top
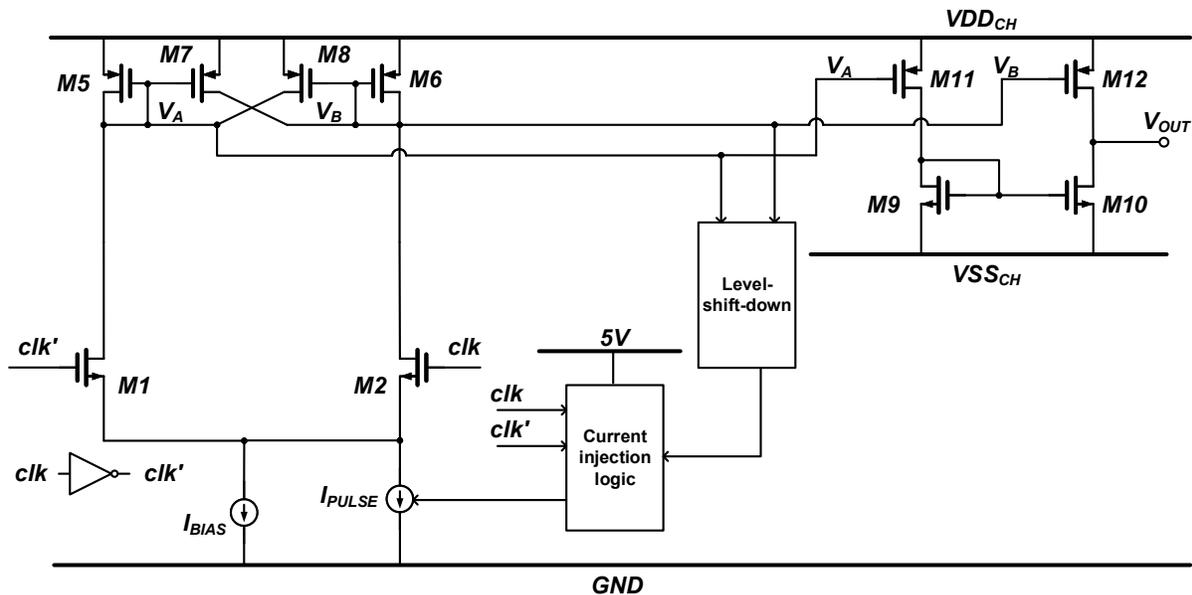
Figure 3.7: The level shifter is a differential amplifier with a single-ended output. This level shifter topology contains a feedback path, which uses current injection logic to inject a pulse of current at the input. The current pulse speeds the transition of V_{OUT}. In this figure, the digital input signal is labeled as clk.

switch of each column in the PFC rectifier, ripple cancellation module, and H-bridge stack (Figures 3.2 to 3.4). The structure in Figure 3.5 requires a flying or DC supply capacitor attached between VSS_{CH} and another node capacitively fixed at a higher voltage. However, such a supply capacitor does not exist for the top switch of each column. For example, consider column 1 in Figure 3.2, with the eight switches numbered from bottom to top. Switches 1, 3, 5, and 7 are supplied by the DC capacitors. Switches 2, 4, and 6 are supplied by the flying capacitors to the left of the column 1 switches. However, switch 8 (top switch) has no DC or flying capacitor supply.

The top switch of each column must bootstrap off a floating capacitor supply, as shown in Figure 3.8. Although column 1 will be used for demonstration, the bootstrapping set up is the same for the other columns. The bootstrapping set up for column 1 uses a channel supply that is modified such that its output, V_{pump}, is fixed 11 V to 12 V above level 3. When column 1 switches low, M7 is closed and the top flying node connects to level 3. During this time, V_{pump} can charge a floating supply capacitor, C_{boot}, through the diode D_{pump}. When column 1 switches high, M8 is closed and the top flying node connects to level 4. At this
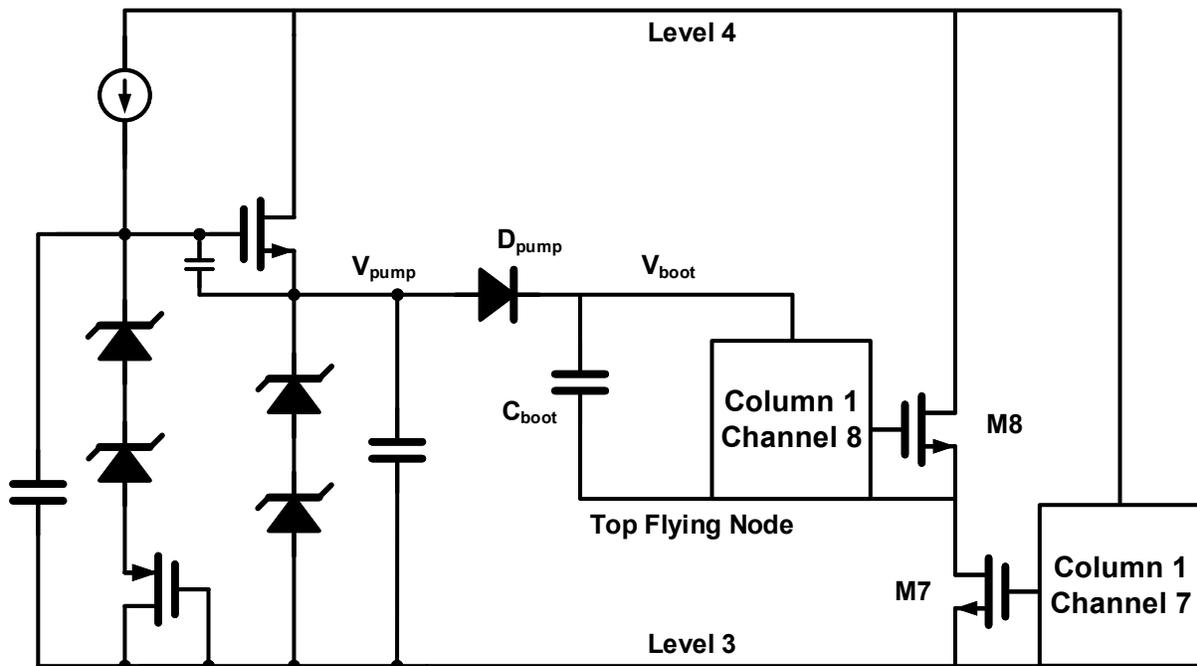
Figure 3.8: This diagram depicts the bootstrapping set up for supplying the top switching channel of column 1. Note that the channel blocks consist of a channel supply, level shifter, and driver. On the left, a modified channel supply maintains the static V_{pump} voltage at 11 V to 12 V above level 3. When M7 is closed, V_{pump} charges C_{boot} through D_{pump}. When M8 is closed (M7 open), D_{pump} blocks current, allowing V_{boot} to be higher than level 4. Channel 8 (the top switching channel) is supplied from C_{boot}.

time, C_{boot} retains its charge because D_{pump} is now blocking. V_{boot} is now at a voltage 11 V to 12 V above level 4, and functions to supply the switching channel for the top switch M8.

If column 1 is held high for too long, leakage through the top switching channel will eventually drain C_{boot}, ultimately causing M8 to open. For this reason, it is important that the columns are constantly switching in order to ensure C_{boot} remains fully charged. As explained in Section 3.2.1, the generalized multilevel converter has several equivalent switch combinations for accessing DC levels 1-3. It is recommended that the converter periodically toggles between these switch combinations in order to ensure that C_{boot} of each column is fully charged.

3.4   Sigma Delta Control

The multilevel converters in the power-factor correction (PFC) and ripple-cancellation modules are controlled via sigma-delta modulation. In this context, the multilevel converter behaves like a quantizer since it can only set the inverter node to one of several quantized levels. Like any quantizer, the multilevel converter produces quantization noise. As previously explained in Section 2.3.2, sigma-delta modulation invokes closed loop control to push the quantization noise to higher frequencies, after which it can easily be filtered out [60]. Intuitively, the output of the sigma-delta modulator attempts to best approximate the input.

As a control scheme, sigma-delta modulation has the distinct advantage of simplicity. Figure 3.9b suggests that a simple first-order sigma-delta control loop could be implemented with a single integrating op-amp. Sigma-delta modulation also has the advantages of closed-loop robustness and stability, assuming that the loop is properly designed. Finally, the quantization behavior of the multilevel converter causes sigma-delta modulation to simply be a very natural and convenient control scheme. PWM is rather difficult and complicated for multilevel converters because a triangle wave must be generated between each level. Techniques such as space vector modulation, and selective harmonic elimination all require intricate and carefully designed control.

3.4.1   Control for the PFC Rectifier

The power-factor correction (PFC) rectifier uses a second order sigma-delta loop to set the line current to best approximate a reference current waveform. As shown in Figure 3.9a, the reference waveform is nominally sinusoidal and in phase with the line voltage. Sigma-delta control is especially useful because its ability to shape quantization noise is necessary for meeting the line-current harmonic specs.

The control loop design in Figure 3.9a allows for the adjustment of the integral gain k_i and the proportional gain k_p. It is often reasonable to set

$$K \quad = \quad (k_i/f_s)(\Delta/\delta) = 1 \tag{3.1}$$

where the quantizer is clocked at frequency f_s, and its quantization levels step by Δ at the output and δ at the input [66, 67]. If $K >> 1$, the quantizer may attempt to switch by more than one level at a time. If $K << 1$, the quantizer output may experience dead zones in which it does not switch when it should. After f_s and k_i are selected, k_p can be chosen to help shape the quantization noise curve.

In this dissertation, $L = 10$ mH, $R_L = 2$ Ω, $k_i = 1e7$, and $k_p = 25$. The signal and noise magnitude for the block diagram in Figure 3.9a is shown in Figure 3.10. The PFC rectifier samples at $f_s = 400$ kHz.
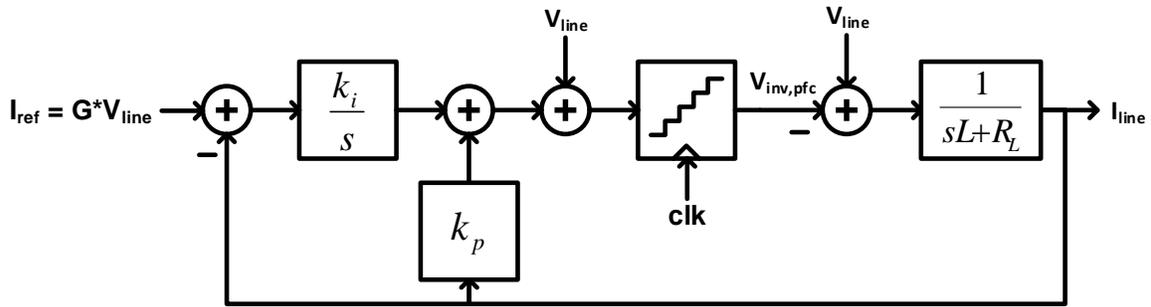
(a)
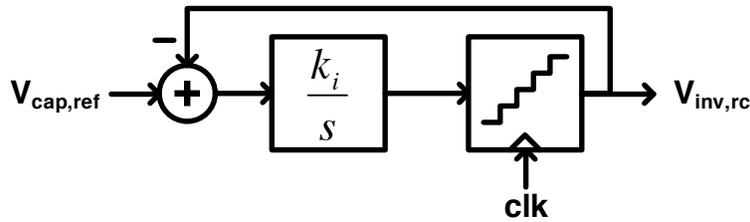
(b)

Figure 3.9: The sigma-delta control loops for the PFC rectifier and ripple-cancellation module. Each loop has an integrator and a quantizer clocked at 400 kHz. (a) A second order sigma-delta loop is used for the PFC rectifier, where the second pole is obtained from the input inductor. The input current I_{line} relates to the voltage across the inductor $V_{line} - V_{inv,pfc}$. (b) A first order sigma-delta loop is used for the ripple-cancellation module. This module uses the sigma-delta loop to set the inverter node of the ripple-cancellation circuit $V_{inv,rc}$ to approximate a preprogrammed waveform $V_{cap,ref}$.
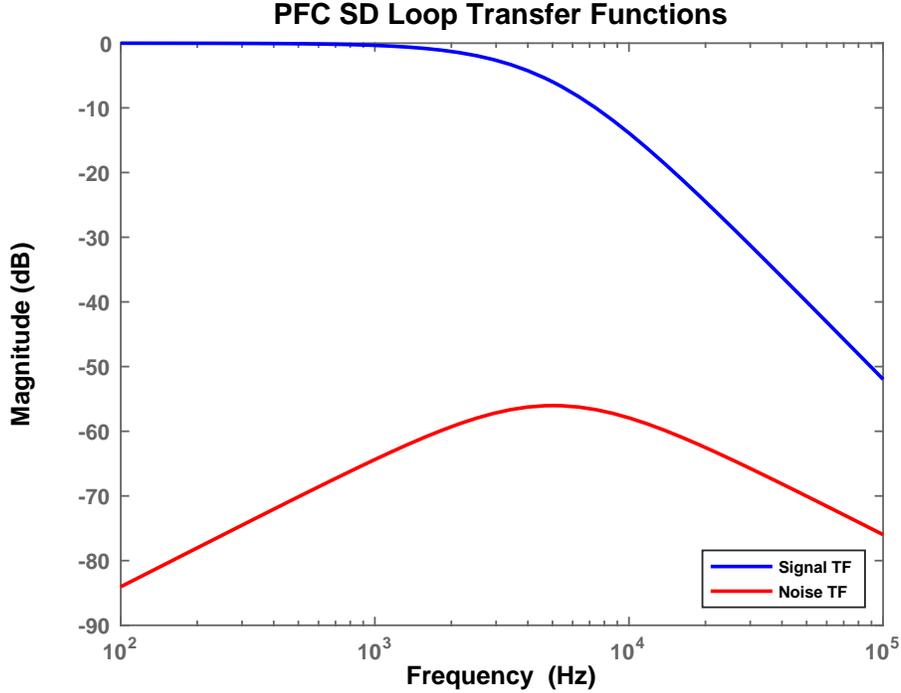
Figure 3.10: The signal (I_{line}/I_{ref}) and noise (I_{line}/N) transfer functions for the block diagram in Figure 3.9a.

3.4.2 Control for the Ripple Cancellation Module

The ripple-cancellation module uses sigma-delta modulation to swing the storage capacitor voltage such that the 120 Hz power ripple is cancelled from the DC bus. The reference waveform for the storage capacitor voltage is developed by a conservation of energy approach [42]. If the line current $I\sin(\omega_0 t)$ is sinusoidal and in phase with the line voltage $V\sin(\omega_0 t)$, the power ripple P_{RC} on the DC bus is developed in Equation 1.5 as

$$
\begin{aligned}
P_{in} &= V_{line}I_{line} = VI(\frac{1}{2} - \frac{1}{2}\cos(2\omega_0 t)) \\
P_{RC} &= P_{in} - P_{LED} = -\frac{1}{2}VI\cos(2\omega_0 t).
\end{aligned}
\tag{3.2}
$$

In this analysis, P_{RC} does not account for losses.

A functional ripple-cancellation module transfers all of the ripple power P_{RC} to the storage capacitor. As such, the ideal voltage waveform $v_{cap,ref}$ on the storage capacitor

is derived from its energy E_{RC} as

$$E_{RC}(t) = \frac{1}{2}C_{RC}v^2_{cap,ref}(t) = \int_{-\infty}^{t} P_{RC}(t)$$

$$v_{cap,ref}(t) = \sqrt{-\frac{VI}{2\omega_0 C_{RC}}\sin(2\omega_0 t) + K} \tag{3.3}$$

for storage capacitance C_{RC}.

The value for K is a design choice that affects the DC level of the storage capacitor. To ensure $v_{cap,ref}$ stays within the voltage bounds V_{max} and V_{min},

$$K = \frac{V^2_{max} + V^2_{min}}{2}. \tag{3.4}$$

For C_{RC} to be minimized, the storage capacitor voltage must swing through its full range. In order for $v_{cap,ref}$ to be able to swing between GND and V_{top},

$$K = \frac{V^2_{top} + 0^2}{2} = \frac{V^2_{top}}{2}. \tag{3.5}$$

At various dimming levels, C_{RC} will be oversized for the amount of input power ripple. As such, the storage capacitor voltage does not swing the full range between GND and V_{top}. It is ideal for the storage capacitor voltage to be as high as possible in order to minimize $I^2 R$ losses through the ripple-cancellation module. For this, it is desirable to set

$$K = \frac{V^2_{top} + (V^2_{top} - \frac{VI}{\omega_0 C_{RC}})}{2}, \tag{3.6}$$

which positions $v_{cap,ref}$ such that its peak is at V_{top}.

In this dissertation, the ripple-cancellation module relies on open-loop control with a look-up table parameterized by dimming level command, eg. power level. Each $v_{cap,ref}$ waveform stored in the look-up table corresponds to one half-period of data. The data is actually the modulation waveform, generated with a system as indicated in Figure 3.9b. In practice, the waveform is triggered by the line voltage zero crossing.

To design an active ripple-cancellation module, it is often desirable to calculate the smallest required storage capacitance, $C_{RC,min}$. This value can be calculated given specifications for the input RMS voltage V, the input RMS current I, and F, the fraction of input power ripple allowed to the load. The calculation follows similar to Equations 3.2 and 3.3 as

$$P_{RC}(t) = P_{in}(t) - P_{LED}(t) = (1-F)P_{in}(t)$$

$$E_{RC}(t) = \frac{1}{2}C_{RC,min}v^2_{cap}(t) = -\frac{(1-F)VI}{4\omega_0}\sin(2\omega_0 t) + K$$

$$E_{RC,swing} = \frac{1}{2}C_{RC,min}V^2_{cap,max} - \frac{1}{2}C_{RC,min}V^2_{cap,min} = \frac{2(1-F)VI}{4\omega_0}$$

$$C_{RC,min} = \frac{(1-F)VI}{\omega_0(V^2_{cap,max} - V^2_{cap,min})}. \tag{3.7}$$

If the storage capacitor voltage can swing over the full DC voltage range, $V_{cap,max} = V_{top}$, $V_{cap,min} = 0$, and the minimum required storage capacitance is

$$C_{RC,min} \quad = \quad \frac{(1-F)VI}{\omega_0 V_{top}^2}. \tag{3.8}$$

The analysis in Section 1.4 shows that for $F = 0.066$, the active ripple-cancellation driver requires $C_{RC,min} = 1.5\mu F$. Table 1.1 shows that a relatively small 250 V, 1.5 μF ceramic capacitor can be found on Digikey for $1.17 [48], and is less expensive in bulk.

Chapter 4

Experimental Results and Data

4.1   Integration and Testing Setup

The full system from Figure 3.1 has been simulated, experimentally tested, and verified. A prototype IC, shown in Figures 4.1 and 4.2, was designed and fabricated on an Analog-Bipolar-CMOS-DMOS (ABCD) high voltage process. The IC contains the circuitry for a multilevel converter and an H-bridge stack. Both circuits use 100 V N-type LDMOS transistors as their power switches, and every power switch requires an integrated switching channel. The transistors can be vertically stacked for multilevel operation as long as the highest voltage on chip does not exceed 220 V.
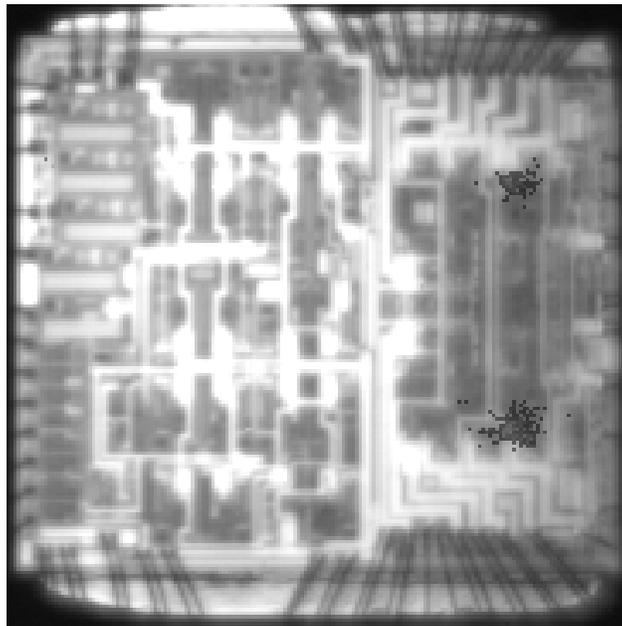
Figure 4.1: Die photo of the prototype IC.
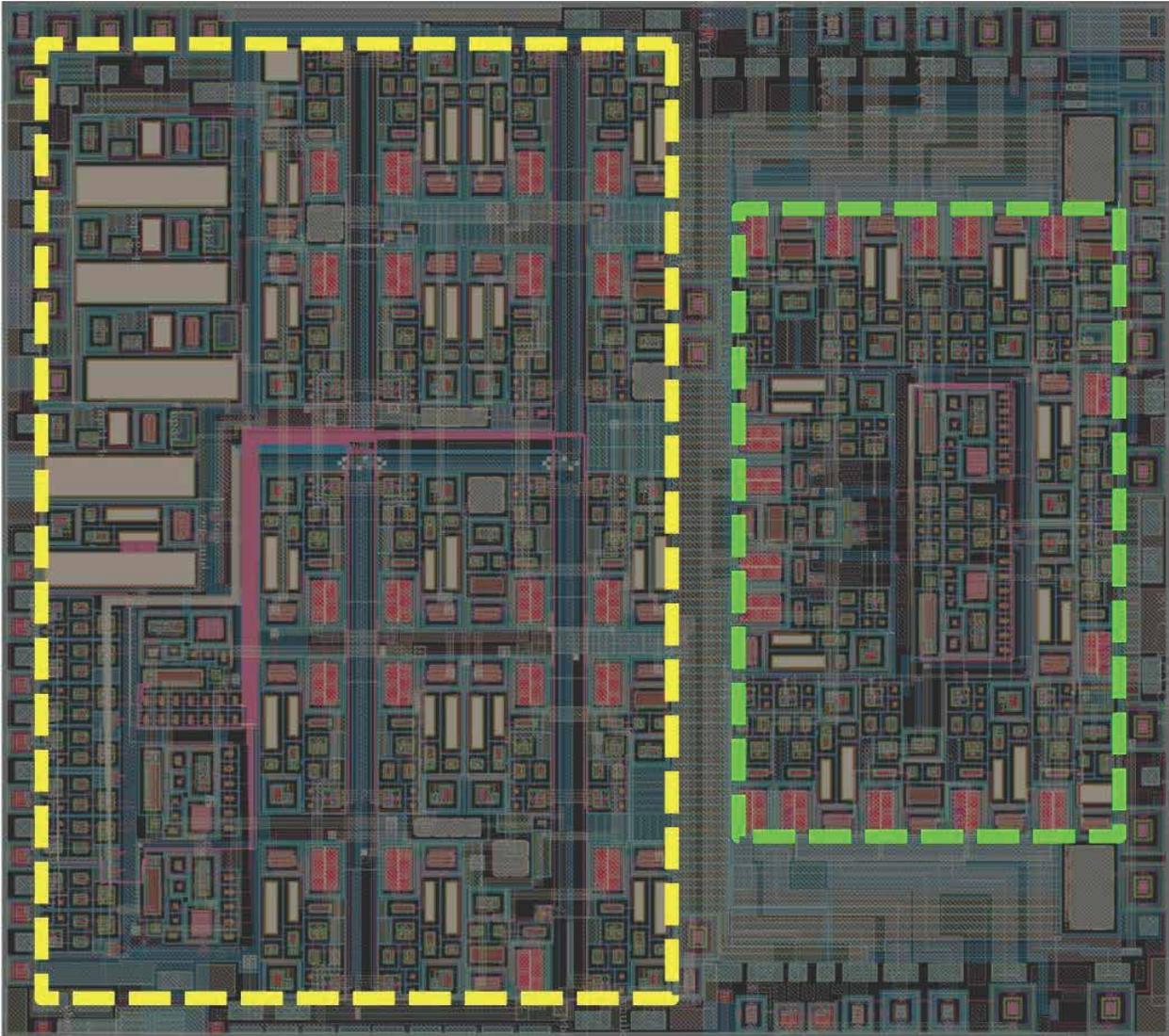
Figure 4.2: The prototype IC layout with dimensions of 7.08mm X 6.28mm. The multilevel converter is on the left (yellow). The H-bridge stack is on the right (green).
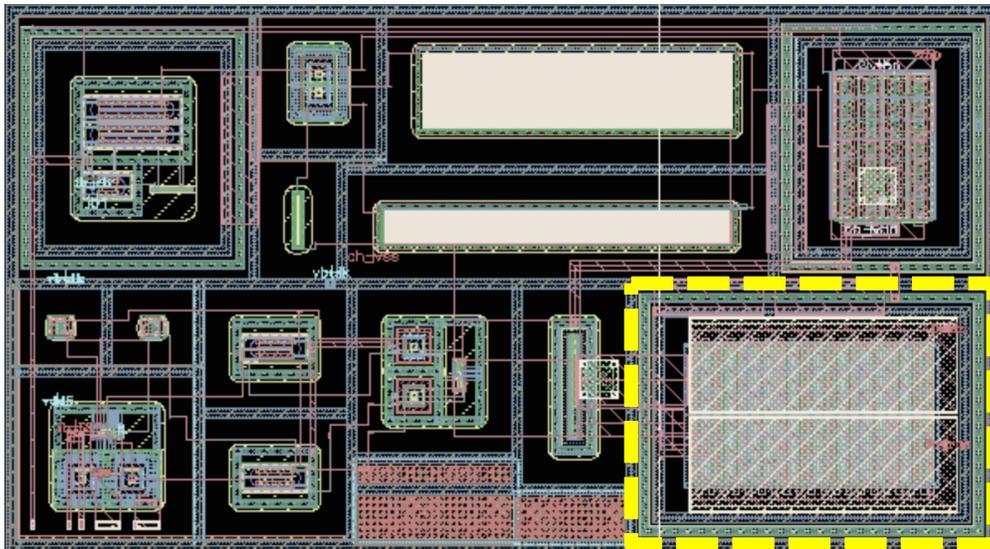
Figure 4.3: The layout for the switching channel with the power LDMOS highlighted in yellow. The channel supply, level shifter, and driver account for roughly 80% of the layout area.
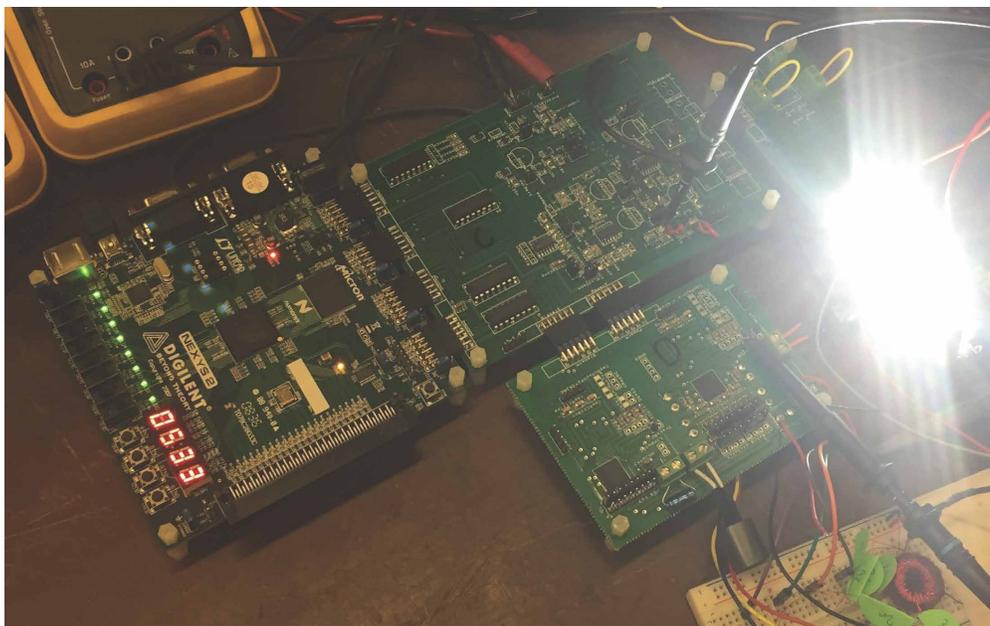
Figure 4.4: Board and lab setup. The power board (lower left of the LEDs) contains two ICs, one for the PFC rectifier and one for the ripple-cancellation module. The FPGA board (left) attaches to the control board (top center). All of the control logic can be integrated in CMOS on the IC.

As shown in Figure 4.3, the area of the power switch accounts for roughly 20% of the total switching channel area. The channel supply, level shifter, and driver all contain low-voltage circuitry. However, these circuits float at a high voltage relative to the substrate, and thus require extensive spacing and guard rings. Various design rules specify the spacing and thickness of guard rings at 8 V, 20 V, 70 V, 120 V, and 220 V.

The test board in Figure 4.4 is implemented on a 2-layer PCB and the system is controlled via off-chip components and a Xilinx Spartan-3 FPGA. These off-chip functions can be readily integrated on a subsequent design turn, and require very small die area. Table 4.1 shows a full list of required external components, not including the pair of multilevel converter chips. These components can be found on the power board, and a mock power board layout is shown in Figure 4.5. The practical production size of the LED driver can be extrapolated from Table 4.1 and Figure 4.5.

Component	Part Number	Desc.	Dim. (mm)	Qty.
PFC Inductor	RFS1317-825KL	8.2 mH 0.25 A	13.3x13.3x16	1
Ripple Canc. Inductor	RFB0810-102L	1 mH 0.35 A	9.5x9.5x11.5	1
Transformer Toroid	C055379A2		18.1x18.1x7.1	1
DC Bus Caps	C3216X7R2A 105K160AA	1 μF 100 V	3.2x1.6x1.3	4
Ripple Canc. Storage Cap	SK052E475ZAR	4.7 μF 200 V	12.7x5.1x14.2	1-2
Input Bridge	DF02S-E3/45	200 V	8.5x6.5x3.3	1
Output Bridge	PD3S160-7	60 V	1.9x1.3x0.7	4

Table 4.1: Power components used in the prototype LED driver.
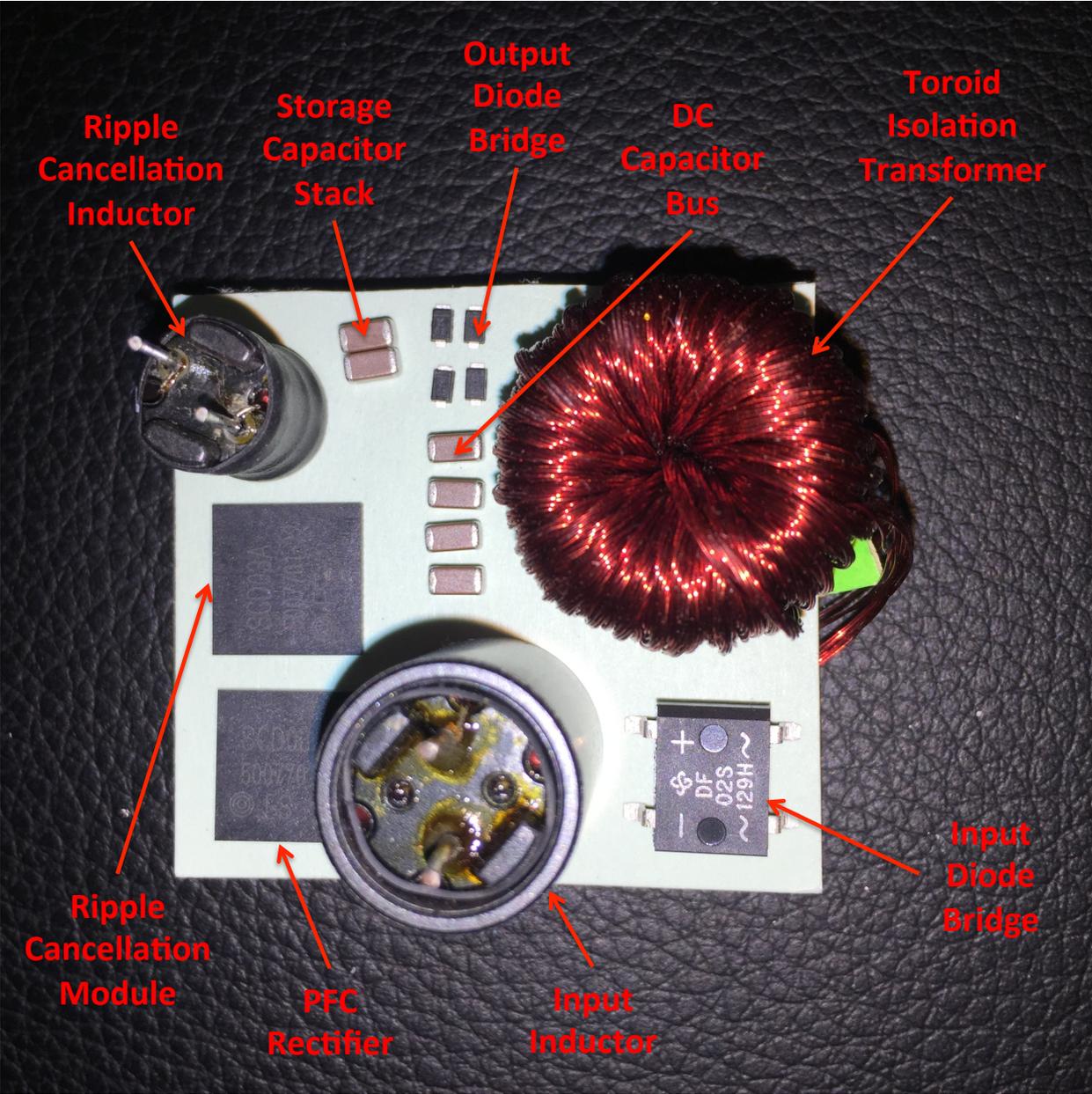
Figure 4.5: A mock layout of the power board with the various components from Table 4.1. Since the digital and analog control can be integrated, these components indicate the total size of the LED driver. For reference, the two IC packages are 1x1 cm, and the card is 4.3x3.8 cm. The layout can be even more tight if the magnetic components are stacked on top of the flat components.

4.2   Testing of Functionality and Waveforms

This section discusses and verifies the functionality of the LED driver. The discussion follows an analysis of the driver's waveforms, along with its voltage and current limits. Note that the prototype IC was designed and fabricated twice. The first test chip was barely functional, and did not produce reliable data. After an extensive failure analysis described in Appendix A, the chip was respun. The driver described in this section and Section 4.3 uses the second test chip.

4.2.1   Waveforms and Functionality

The waveforms in Figure 4.6 demonstrate basic functionality of the PFC rectifier and ripple-cancellation modules. The PLECS simulation waveforms shown in Figures 4.6a and 4.6b can be compared to the experimental scope waveforms, shown in Figures 4.6c and 4.6d. Figures 4.6a and 4.6c show that the power-factor correction (PFC) rectifier can limit harmonics on line current (green) and ensure that it is in phase with the line voltage (yellow). The PFC inverter node (blue) of the PFC is shown to utilize all four levels. Figures 4.6b and 4.6d show that the ripple-cancellation module can cancel AC ripple from the DC capacitor bus. Swinging the storage capacitor voltage (purple) allows the DC voltage at level 4 (green) to be almost entirely devoid of ripple.

4.2.2   Testing Procedure for the Chip Limits

The integrated circuit is divided into two main sections: the multilevel converter, and the H-bridge stack. There are five tests for chip functionality:

- Test 1: the H-bridge stack.

- Test 2: the multilevel converter in inverter mode.

- Test 3: the multilevel converter in rectifier mode.

- Test 4: the closed-loop PFC rectifier with 50 μF DC capacitors.

- Test 5: the closed-loop PFC rectifier with active ripple cancellation.

The first test verifies the functionality of the H-bridge stack and transformer. In this test, a DC power supply is attached across the entire DC capacitor bus (between level 4 and ground) and the chip is clocked externally. A full verification of the H-bridge stack requires probing each of the flying nodes and confirming their waveforms. When a resistor or electronic load (in resistance configuration) is attached to the rectified transformer output, the input and output power can be measured. This test is most conveniently performed first because the H-bridge stack is stand-alone. In addition, the multilevel converter requires a functional H-bridge stack for balancing the DC capacitor bus voltages.
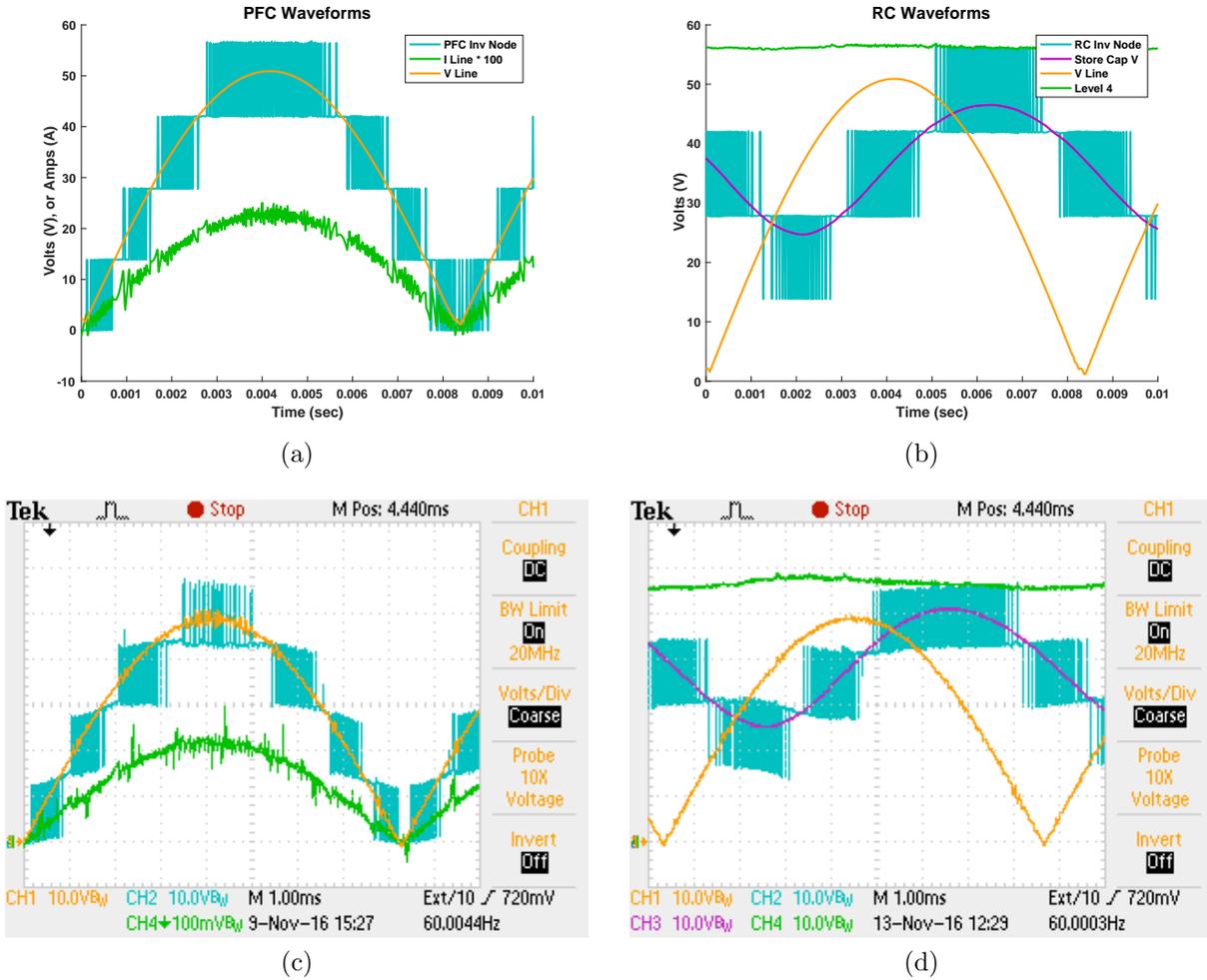
Figure 4.6: Simulated and experimental waveforms that demonstrate the functionality of the power-factor correction (PFC) rectifier and ripple-cancellation module. (a) Simulated PFC waveforms with the line voltage (yellow), line current (green), and the PFC rectifier inverter node of Figure 3.2 (blue). The line current is scaled by 100 for visibility. (b) Simulated ripple-cancellation module waveforms. Waveforms include the line voltage (yellow), the voltage at level 4 of the DC capacitor bus (green), the voltage across the storage capacitor (purple), and the ripple-cancellation module inverter node from Figure 3.3 (blue). (c) Experimental PFC rectifier waveforms from oscilloscope. The line current (green) is measured as the voltage across a 1 ohm current sense resistor. Horizontal divisions are 1 ms. Vertical divisions are 10 V for the line voltage (yellow) and PFC rectifier inverter node (blue), and are 100 mV for the line current (green). (d) Experimental ripple-cancellation module waveforms. Horizontal divisions are 1 ms and vertical divisions are all 10 V.

The second test verifies that the multilevel converter can function as an inverter. In other words, power flows from the DC capacitor bus to the inverter node. Like the first test, the set up requires a DC power supply across the DC capacitor bus, and an external clocking signal for the H-bridge stack. In addition, the column inputs of the multilevel converter are connected to an FPGA. The verification procedure involves configuring the switching columns and verifying that the inverter node voltage is correct. A full verification involves testing every column configuration and probing each of the flying nodes in the multilevel converter. To test the limits of power flow, an electronic load can be connected to the inverter node.

The third test verifies that the multilevel converter can function as a rectifier. In other words, power flows from the inverter node to the DC capacitor bus. In this test, the DC power supply is attached to the inverter node of the multilevel circuit. Like the second test, the switching columns are configured via a digital signal and the H-bridge stack is externally clocked. However, in this test, the DC bus levels depend on the switch configuration and the DC supply voltage. For example, the voltage at level 4, V_{lvl4}, is related to the DC supply voltage V_{sup} as $V_{lvl4} \approx V_{sup} * 4/l$, where l is the level for which the converter is configured. Like the first test, an electronic load at the H-bridge transformer output can verify power flow.

The fourth test verifies that the multilevel converter can function as a PFC rectifier with closed loop control. This test follows the schematic from Figure 3.2, and involves attaching an AC supply to the inverter node via a diode bridge and input inductor. In this test, the driver does not have active ripple cancellation, and so the DC levels must be maintained via passive ripple cancellation. As such, each of the DC capacitors are reinforced with a 50 μF electrolytic. The digital signal for the switching columns is generated by the closed loop sigma-delta controller. An output load is mandatory for this test, since the control loop requires power to flow through the chip. In order to most accurately represent the loading characteristics of LEDs, an electronic load is attached to the output and set to constant voltage configuration.

The fifth and final test verifies the functionality of the active ripple-cancellation module. Since tests 2 and 3 previously confirmed that the integrated multilevel converter is functionally bidirectional, this test mainly verifies the ripple-cancellation control algorithm. The set up is identical to the fourth test, and the verification involves probing level 4 to measure the voltage ripple.

4.2.3 Chip Voltage and Current Limits

Although the waveforms and performance of the second test chip indicate an improvement over the first, it still fails at high voltage. The functionality tests from Section 4.2.2 were administered to the second chip with the following results:

- Test 1: The H-bridge stack functions correctly with light load up to 120 V supply input across the DC capacitor stack. Leakage occurs somewhere in the 120-140 V range, and

the chips often fail above 140 V.

- Tests 2 and 3: The multilevel circuit is functional in inverter and rectifier mode with light load up to 80 V across the DC capacitor stack.

- Test 4: The PFC rectifier functions correctly in closed loop up to an AC input of 55 V_{RMS} ($\approx$80 V DC capacitor stack) for low power, but requires a lower input voltage for high power. For robustness and consistency, data is only reported for operation at input voltages up to 45 V_{RMS}.

- Test 5: The ripple-cancellation module functions correctly in a range consistent with tests 2, 3, and 4.

4.3 Performance

4.3.1 Efficiency and Loss Analysis

Figure 4.7 shows how the efficiency varies over input voltage and current. For reference, the rated input current for a 20 W LED driver is 167 mA_{RMS}. There are several general reasons why the efficiency increases with input voltage. First, conduction losses (such as $R_{DS,on}$ losses) are related to the square of the current. As voltage is increased, ohmic drops become a progressively smaller fraction of the output power. Second, diode drop remains approximately constant regardless of input voltage. The loss in any diode-based power components scales only with current. Third, the gate drive loss remains constant regardless of input power, and becomes less significant at higher power.

The LED driver exhibits a concave relationship between efficiency and current, as shown by the curves in Figure 4.7. This behavior is common among most power converters for similar reasons. A lightly loaded converter with low current is very inefficient because the gate drive loss is relatively high compared to the actual power delivered to the load. However, a heavily loaded converter is also inefficient due to increased proportion of conduction loss. The output power scales with the current, but any ohmic conduction loss increases as the current squared. Ultimately, the peak efficiency occurs when the current is high enough for gate drive loss to become less significant, but low enough that ohmic conduction losses do not dominate.

A comparative analysis with modeled performance is given in Figure 4.8 to inform understanding of the results. For the lower input voltages, the modeled loss (multicolored bar) can be compared with the actual measured loss (dark blue bar). The test part did not function at full rated voltage, but was testable to approximately half of rated voltage. The measured losses were well modeled, though slightly higher than predicted in modeling. The model also predicts that the power switch $R_{DS,on}$ conduction losses in the PFC rectifier and ripple-cancellation circuit are the most significant.

Figure 4.9 compares the modeled and measured performance as a function of input current. While the measured performance exhibits a typical efficiency curve, the modeled loss

exhibits a strictly positive correlation. The loss models for the multilevel converters account for ohmic conduction loss and the CV^2 losses in driving the gate capacitance.
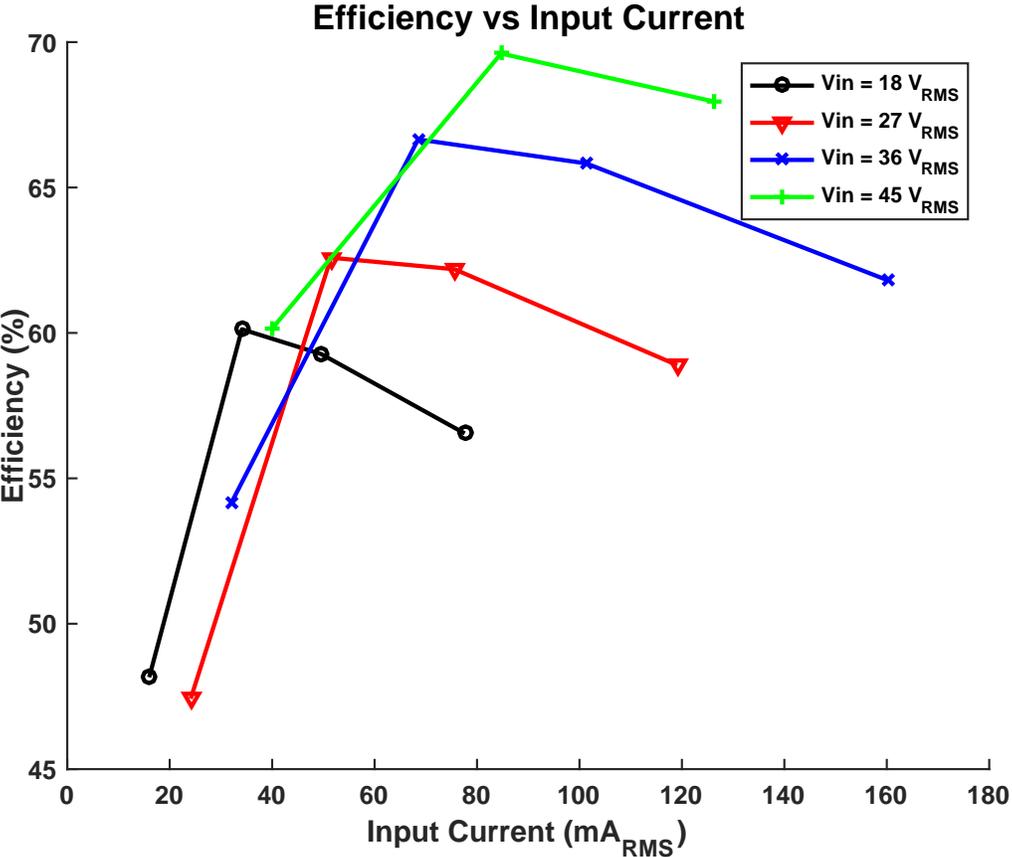
Figure 4.7: Efficiency versus input current (the rated input current is 167 mA). The output voltage was set at the optimal value using an electronic load. In general, the output voltage and current is determined by the total voltage drop of the series LED string.
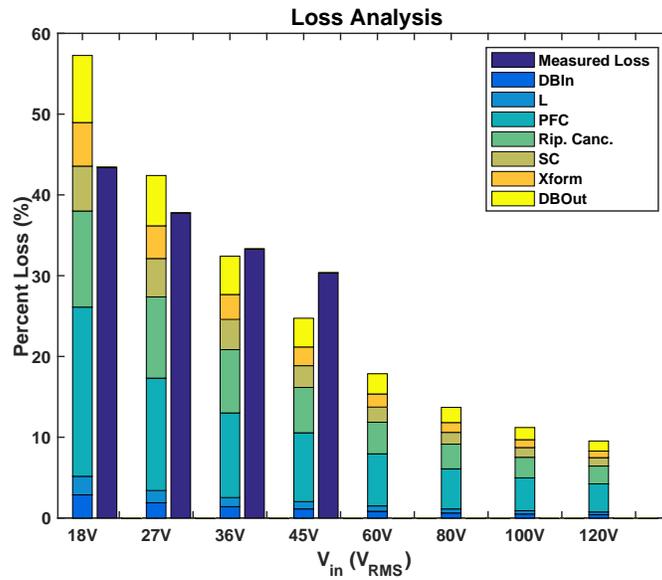
Figure 4.8: Loss versus input voltage. The lower voltages each compare a loss model (left bar) to the actual measured loss (right dark blue bar). The loss model can somewhat provide a projection of how the system would perform. The model and data correspond to operation at close to 80 mA input current.
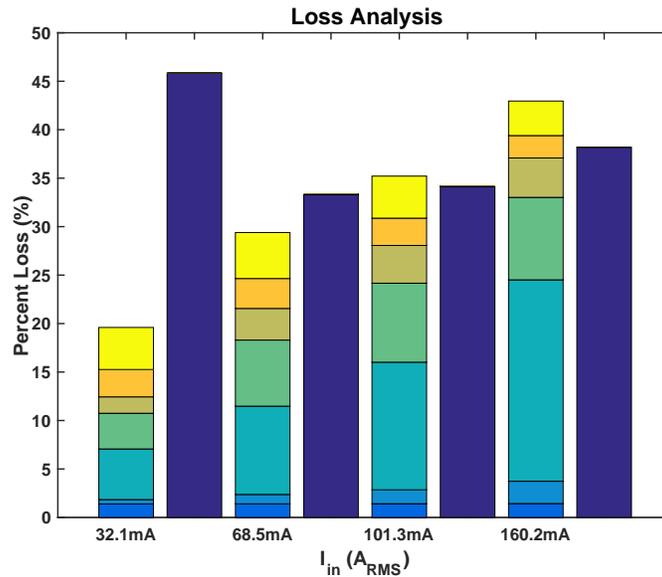
Figure 4.9: Loss versus input current at 36 V_{RMS} input, with same legend as Figure 4.8. The loss model does not properly account for losses in the switching channels, which dominate at light loads.
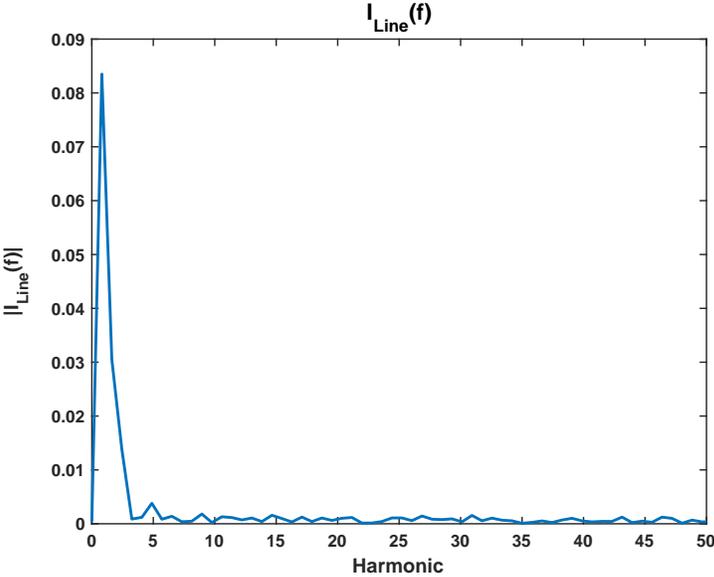
(a)
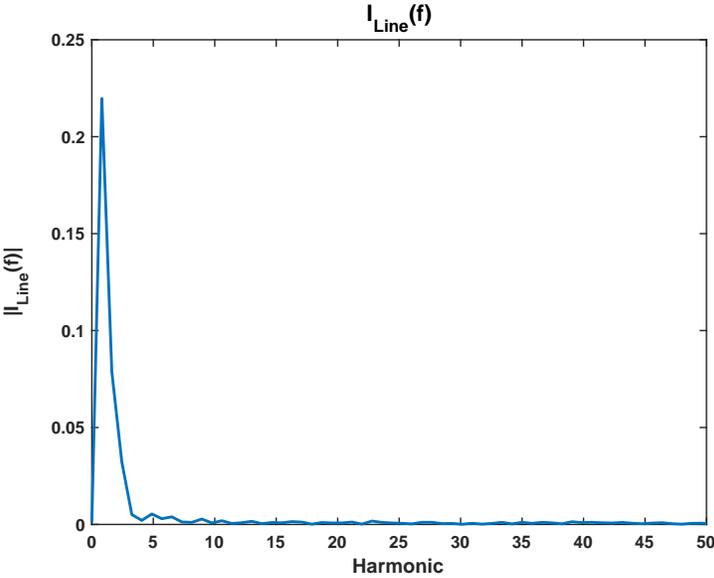
(b)

Figure 4.10: FFT of the line current input I_{Line}. Line current harmonics are all less than 5% of the fundamental. Data is obtained at $V_{\text{in,RMS}} = 36$ V, and (a) $I_{\text{in,RMS}} = 68.5$ mA, or (b) $I_{\text{in,RMS}} = 160$ mA.

4.3.2 Input Current Harmonics

Figure 4.10 shows an FFT of the line current input. Standards such as IEC 61000-3-2 (US) and EN 61000-3-2 (Europe) specify the acceptable limitations on specific line current harmonics [19]. For lighting applications, these standards specify that the fifth harmonic must be less than 10% of the fundamental. In this dissertation, the fifth harmonic is measured to be 2.5% of the fundamental at the rated input current (160 mA$_{RMS}$). Even when dimmed to 68.5 mA$_{RMS}$, the fifth harmonic is 4.6% of the fundamental. Higher harmonics are required to be less than 3% of the fundamental, and these specifications are also met. Ultimately, these results suggest that the IEC specifications can be achieved with a smaller input inductor.

4.3.3 Ripple Cancellation

The ripple-cancellation module is able to cancel 120 Hz input power ripple from the DC capacitor bus. Qualitative evidence of its functionality is visible from the DC level 4 (green) waveform in Figure 4.6d. To quantify the performance of the ripple-cancellation module, the voltage ripple is measured at DC level 4 (the top of the DC capacitor bus). The voltage ripple at the output of the driver can be approximated given the output stage 4:1 step-down conversion.

Figure 4.11 shows that the DC bus ripple voltage has a convex relationship with the output voltage. This relationship is a consequence of the feed-forward control style used in the ripple-cancellation module. The preprogramed storage capacitor waveforms ($v_{cap,ref}$) are derived from a preset DC capacitor bus voltage. When the actual DC capacitor bus voltage deviates from the preset voltage, the amplitude of the storage capacitor voltage swing (v_{cap}) will either be too small or too large. The local minimum of each curve in Figure 4.11 occurs near the ideal DC bus voltage. In a practical setting, the output voltage is regulated by the LEDs, and the preset DC voltage for the preprogramed waveforms can be designed accordingly.

Figure 4.11a shows that the minimum peak to peak ripple is 2.11 V at rated current (160 mA) and 13 V output. The amplitude of ripple is 1.055 V. Given the 4:1 step-down output stage, an output voltage of 13 V translates to a DC capacitor bus voltage of at least 52 V. Thus the percent ripple is at most 1.055 V / 52 V = 2.03%. The LED driver has a luminous output ripple comparable to the 6.6% flicker from an incandescent bulb [20, 41].
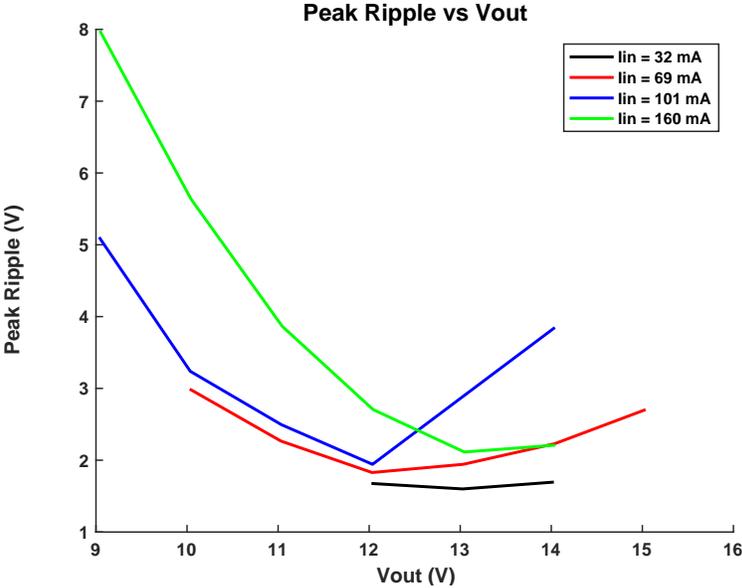
(a)
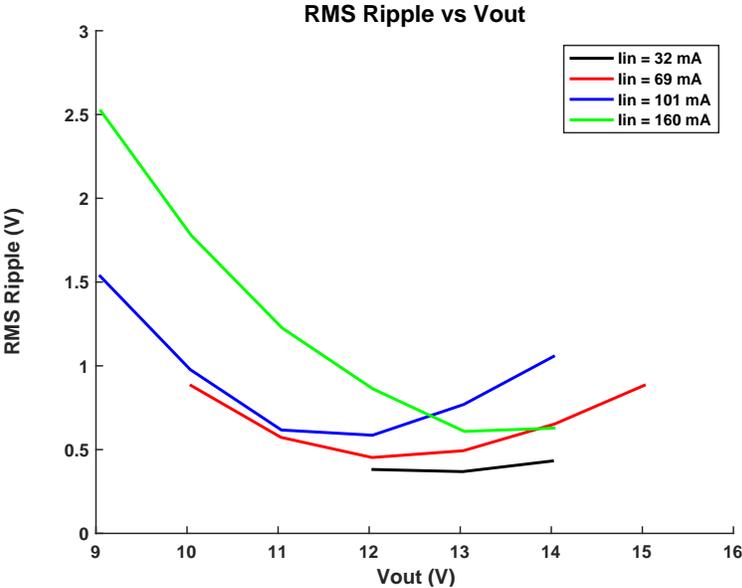
(b)

Figure 4.11: Ripple at the top (level 4) of the DC capacitor bus as a function of the output voltage. Input voltage is 36 V_{RMS}. (a) Peak to peak ripple voltage of DC level 4. (b) RMS of the AC component of DC level 4.

4.4 Future Work

There are several potentially game-changing improvements that could be significant in defining integrated multilevel converters as a viable technology for LED drivers. First, it may be possible to operate this design without the H-bridge stack. Second, half of the gate drivers could be removed if the corresponding power switches were implemented as P-type transistors. Finally, it may be advantageous to implement the multilevel converters with a diode or capacitor clamped topology.

4.4.1 Configuration Without the H-bridge stack

One of the benefits of the generalized multilevel topology is that it does not require external circuitry to balance the DC capacitors[56]. However, the LED driver presented in this
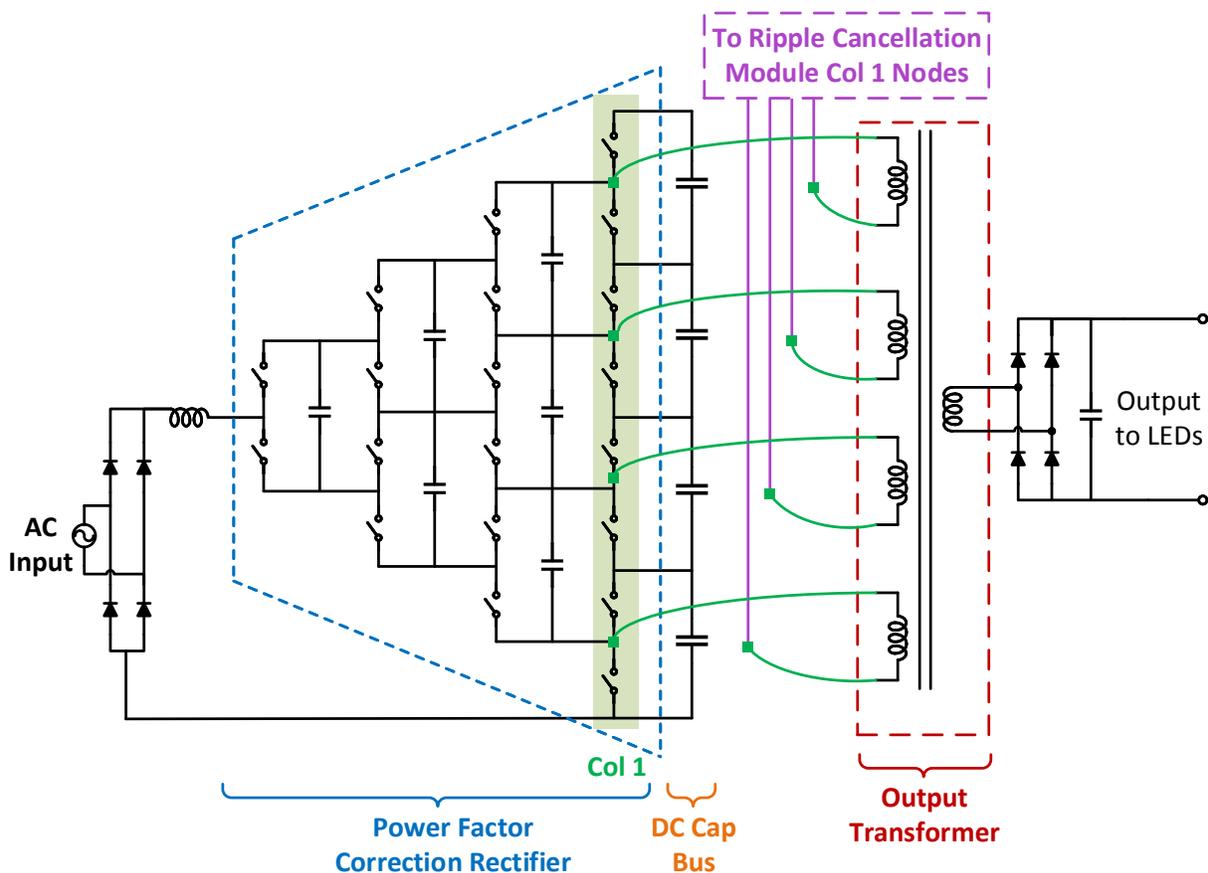
Figure 4.12: Proposed configuration for the LED driver without the H-bridge stack. The transformer windings connect to the column 1 flying nodes of the PFC rectifier and the ripple-cancellation module (not shown).

dissertation balances the DC capacitors using an H-bridge stack and transformer. Future work may involve redesigning the control for the multilevel circuits such that the H-bridge stack can be removed.

The proposed configuration for an LED driver without the H-bridge stack is shown in Figure 4.12. In this configuration, the switches in column 1 of the PFC rectifier and column 1 of the ripple-cancellation module replace the H-bridge stack. The windings of the output transformer are likewise connected to the flying nodes of column 1 on the PFC rectifier and the ripple-cancellation module.

In order for this configuration to function, the switching control for the PFC rectifier and ripple-cancellation circuits must be modified. These multilevel converters now have the additional role of using column 1 to transfer power through the transformer. Column 1 must be clocked at a fixed rate with 50% duty cycle. The clock signal to column 1 of the ripple-cancellation module is complementary to that of the PFC rectifier.

With column 1 reserved for power balance and transfer, each multilevel converter can only use columns 2-4 to set its inverter node voltage. The generalized multilevel converter has several degrees of freedom in connecting the inverter node to DC levels 1-3. Regardless of the state of column 1, there is always a switch configuration that allows the inverter node to access these levels. However, to access level 4 or ground (i.e. level 0), column 1 must be set high or low, respectively. Since column 1 must be clocked with a 50% duty cycle, the inverter node cannot connect to level 4 or ground for more than 50% of the time.

4.4.2 PMOS Power Switches

As explained in Appendix A.6, the chip's functionality issues are caused by the floating channels that sit on flying nodes. Specifically, the VDD_{CH} rail in the switching channel latches below VSS_{CH}. This effect only happens in the floating channels, where the VSS_{CH} node undergoes drastic voltage swings.

Using both NMOS and PMOS power switches allows for a reduction in the number of floating channels. In particular, any of the NMOS switches with a floating source should be replaced with an equivalently sized PMOS. As shown in Figure 4.13, one advantage of a PMOS replacement is that its source can be tied to a fixed level, rather than a flying node. A fixed source allows for a fixed switching channel, which would remedy many of the problems in the channel design discussed in Appendix A.6. The other advantage of a PMOS replacement is that it can share a gate driver with the NMOS switch above. This would mean that M2 (PMOS) and M3 (NMOS) in Figure 4.13 could share a gate driver whose drive voltage swings 5 V above and below the fixed level 1 voltage.

It is important to note that the use of PMOS switches does not completely obviate the need for flying high-side channels. For the H-bridge stack and column 1 of the multilevel converters, PMOS switches can tie the otherwise flying channels to a fixed level. However, columns 2-4 will still have to use flying high-side channels even with PMOS. Nonetheless, using a combined NMOS/PMOS switching channel (as shown in Figure 4.13) would greatly
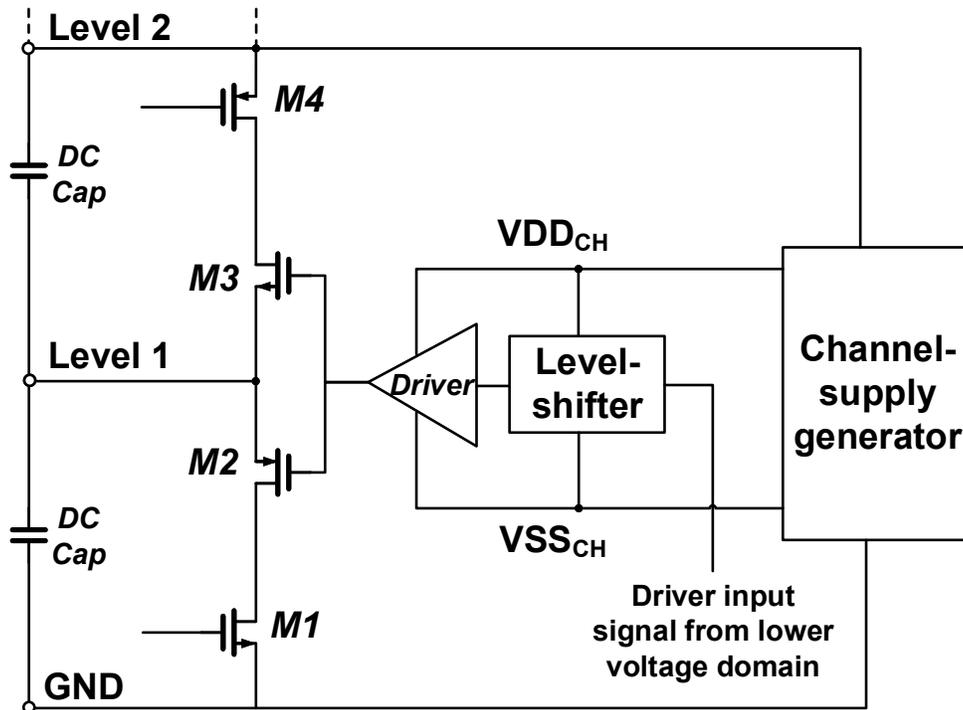
Figure 4.13: Proposed switching channel architecture that uses a complementary PMOS for each of the even numbered switches. The channel supply generator creates the static supply rails VDD$_{CH}$ and VSS$_{CH}$ which are respectively 5 V above and below level 1.

reduce the overall silicon die area. Saved die area can be used to capacitively fortify the mandatory flying high-side channels.

The final benefit of using PMOS is that the top switch of each column no longer requires a bootstrapped supply, previously shown in Figure 3.8. This is advantageous because the columns no longer have to be toggled in order to keep the bootstrap capacitor (C_{boot}) refreshed. In addition, it saves the die area that would have been required for C_{boot}. Note that the switching channel for the top column switch will be different than that of Figure 4.13 because it only drives a single PMOS.

4.4.3   Other Multilevel Topologies

Although the generalized multilevel topology is chosen for its fairly regular gate drive pattern, the other multilevel topologies discussed in Section 2.2 may well be better in reducing silicon die area. As explained in Section 4.1, the IC process isolation requirements cause the switching channels to be very large. A four-level diode-clamped or capacitor-clamped converter only requires eight switches. As shown in Figures 3.2 and 3.3, the generalized multilevel converter requires twenty switches, and thus requires considerably more silicon

die area.

The diode-clamped and capacitor-clamped topologies, shown respectively in Figures 2.2 and 2.3, may both be more conducive to integration. The diode-clamped topology requires fewer switches than the generalized topology, but instead uses a number of passive diodes. Although this topology adds diode drop to the power path, the diode drop is relatively small compared to the typical voltages of an LED driver. The capacitor-clamped topology is another alternative, and is free of diode drop loss. However, the capacitor-clamped topology may require a relatively large silicon die area in order to integrate the extra flying capacitors. To a certain extent, the size of the flying capacitors can reduced if the switching frequency is increased.

It is also important to note the disadvantages to either of the alternative multilevel converter topologies. First, both topologies would require the H-bridge stack in order to balance the voltage on the DC capacitor bus. As such, various configurations like that discussed in Section 4.4.1 do not work with either alternate topology. Second, the alternate topologies do not contain a regular gate drive pattern of flying capacitors. The switching channels in the alternate topologies would require an additional bootstrap capacitor.

Conclusion

LED lamps have become mainstream in the lighting industry due to their efficiency, life span, and environmental benefits. Industrial forces have pushed LED drivers to become efficient, inexpensive, and reliable. This dissertation aims at developing an LED driver that can outperform the industry standard flyback LED driver. Driver specifications include efficiency, power-factor correction, dimming, ripple cancellation, and galvanic isolation.

This dissertation documents the design, fabrication, and testing of an integrated LED driver based on a multilevel topology. The multilevel power-factor correction rectifier converts AC to DC, cancels line-current harmonics, and controls the input power. The multilevel ripple-cancellation module swings the voltage on a storage capacitor in order to cancel ripple from the DC capacitor bus. Both modules are controlled via sigma-delta modulation. Power is transferred to the LEDs via an output stage, which consists of an H-bridge stack and a small isolation transformer.

The multilevel converter and H-bridge stack were designed and fabricated together on a chip. The first chip was barely testable at low voltage and failed at moderate voltage. An extensive series of failure analysis tests were performed on the first chip, involving the use of a thermal camera, thermal microscope, PHEMOS, FIB, and probe station. The problem was determined to be related to the parasitic substrate capacitance on an internal rail of the switching channel. After a respin, the chip was testable at moderate voltage, but still failed at high voltage. At moderate voltage, its waveforms demonstrated intended functionality. A loss analysis model indicates that it would be fairly efficient if it worked at high voltage.

There are several ways in which the LED driver could be improved. First, the multilevel converters could be carefully designed to achieve and replace the functionality of the H-bridge stack. Second, the use of PMOS power switches could decrease the silicon die area and improve performance. Finally, the driver might benefit from a different multilevel converter topology altogether. The LED driver in this dissertation certainly needs to be improved before it can be considered commercially. However, this dissertation demonstrates that a multilevel topology should indeed be considered for use in compact high performance LED drivers.

While multilevel converters have proven to be practical for high voltage electronics, this work demonstrates their potential to be practical in the IC space. The multilevel topology is shown to be particularly useful for expanding the capabilities of any IC process that has devices with a relatively low drain-source breakdown voltage ($V_{DS,max}$). In addition, integrated

multilevel converters are demonstrated for power-factor correction and ripple cancellation in an LED driver. With careful and robust design, integrated multilevel converters show great promise for lighting and household electronics.

Appendix A

First Test Chip and Failure Analysis

This appendix chapter documents the testing and failure analysis of the first test chip. After the problem was identified, the chip was respun. The results in Chapter 4 are for the second chip.

A.1 Functionality Testing Results

The first test chip is testable at low voltage, but fails at higher voltage. Each silicon die yields slightly different voltage limits due to process variation. The voltage limits are marked by two primary voltage thresholds. Below the lower threshold, the chip functions as expected. As the input voltage crosses the lower threshold, an internal leakage path opens, and the input current jumps by roughly 20 mA. Even if the supply voltage is then immediately lowered, the leakage persists until the voltage supply is turned off. The upper voltage threshold occurs when the switch stress due to the leakage path is sufficient to induce device failure. Above the upper threshold, the chip fails.

The tests in Section 4.2.2 had the following results:

- Test 1: The H-bridge stack functions correctly up to 70 V with light load. Leakage occurs somewhere in the 70-90 V range, and the chips often fail above 100 V.

- Test 2: The multilevel circuit functions as an inverter up to 30 V with light load. Even at this voltage, increasing the load current rapidly degrades the flying node waveforms. Leakage occurs somewhere in the 30-40 V range, and the chips often fail above 50 V.

- Tests 3, 4 and 5: These tests were not administered due to failure of test 2.

A series of failure analysis tests were performed in order to determine why the first chip failed. The failure analysis aimed at determining what caused the 20 mA leakage, and how to fix it.

A.2 Thermal Camera Test

The first failure analysis test was to use a thermal camera to determine what part of the chip was experiencing problems. Thermal cameras are useful for revealing regions of high power density in the circuit.

In order to use a thermal camera, the chip must first be decapped. Decapping is a process in which the top of the chip's package is exposed to nitric acid and removed. The end result is a chip whose die is directly visible from the top, but still contains bond wires and a structural package base.

The failure analysis tests all employed the H-bridge stack test, described in Section 4.2.2 as test 1. This procedure was selected because of its simplicity and clear mode of failure. In these tests, the DC voltage input to the decapped chip was ramped up to the leakage threshold around 70 V - 90 V. Thermal camera pictures were taken after the 20 mA leakage was detected.

As shown in Figure A.1, the thermal camera revealed a hot spot on the chip. The hot spot represents a concentration of heat, thus indicating a concentrated power loss most likely related to the 20 mA leakage. Multiple decapped chips were tested in the same way, and each chip revealed a hot spot at the same location. Given these results, the next step was to determine the leakage path.
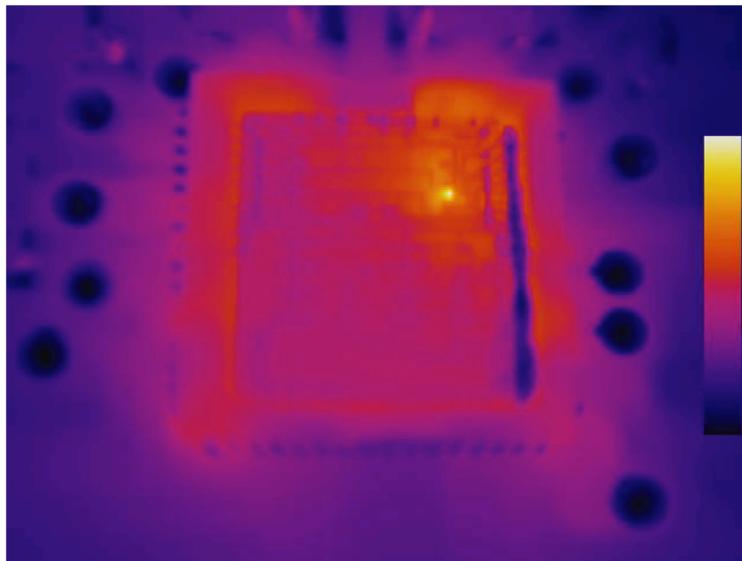
Figure A.1: Thermal camera image of the chip undergoing test 1. The DC input voltage is between 70 V and 90 V. The hot spot indicates the general location of the 20 mA leakage.

A.3   Thermal Microscope Test

The results discussed in Appendix A.2 revealed the general location of a hot spot. Further analysis of the image revealed that the hot spot occurred somewhere within the switching channel of the fourth switch on the right side of the H-bridge stack. However, the thermal camera image lacked the resolution to determine the exact device that was leaking. As such, a thermal microscope was required to determine the problematic device.

The thermal microscope image in Figure A.2 clearly shows the location of the hot spot. The hot spot is located on the main regulator transistor of the channel supply generator, identified previously in Figure 3.6 as M1. While this information does not explicitly determine a leakage path, it narrows down the possibilities. It is very unlikely that any of the other devices in the channel supply are leaking. As such, the leakage path must be through either the level shifter or the driver of the switching channel (shown in Figure 3.5).
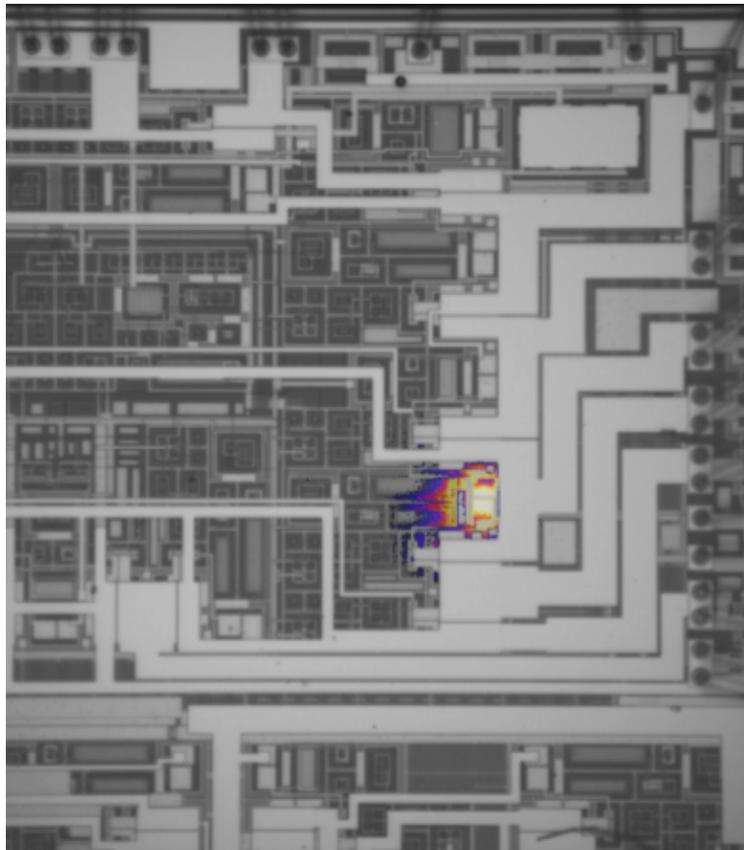
Figure A.2: Thermal microscope image of the chip undergoing test 1. The DC input voltage is between 70 V and 90 V. The 20 mA leakage hot spot has been localized to a specific device.

A.4   PHEMOS Test

A Photon Emission Monitoring System (PHEMOS) was employed for the next phase of failure analysis testing. The PHEMOS is a microscope that can detect photon emissions at a very fine resolution. Photon emissions in integrated circuits come from the recombination of electrons and holes at the junction of any semiconductor device. In this way, the PHEMOS is useful for detecting regions of high current density.

The PHEMOS image shown in Figure A.3 indicates that one of the devices in the switching channel has an exceptionally high current density. Surprisingly, this device is not the transistor that caused the hot spot. Instead, the abnormally high current density is in the driver (buffer) of the switching channel (previously shown in Figure 3.5).

Combined information from the PHEMOS and thermal microscope ultimately reveals the leakage path, shown in Figure A.4. The leakage current discharges a flying capacitor through
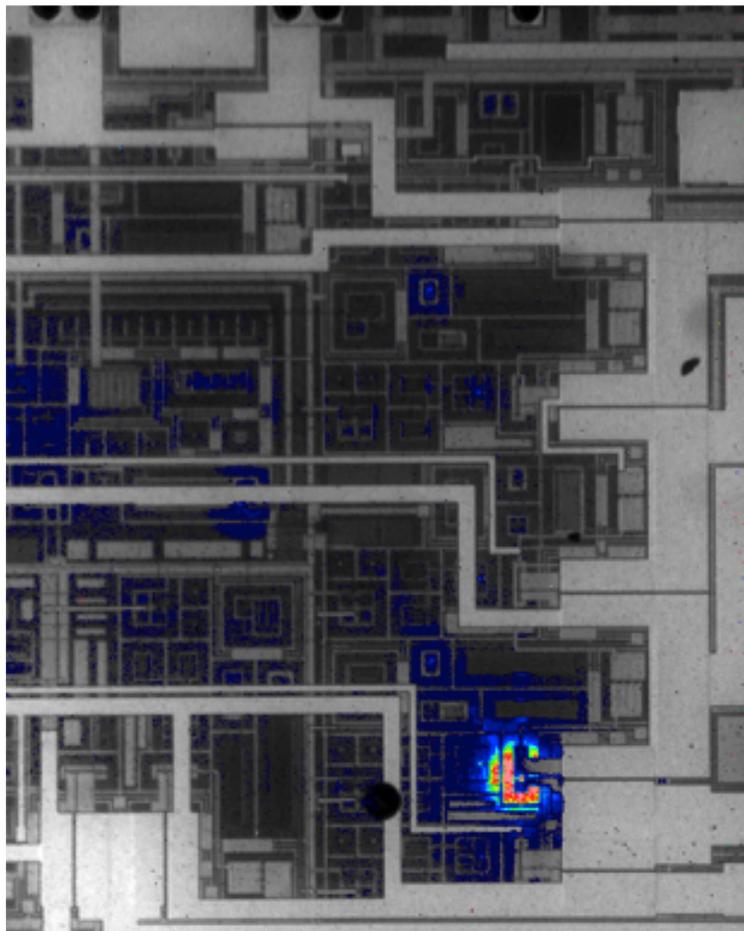
Figure A.3: PHEMOS image of the chip undergoing test 1. There is an abnormally high current density in the driver of the gate driving channel.
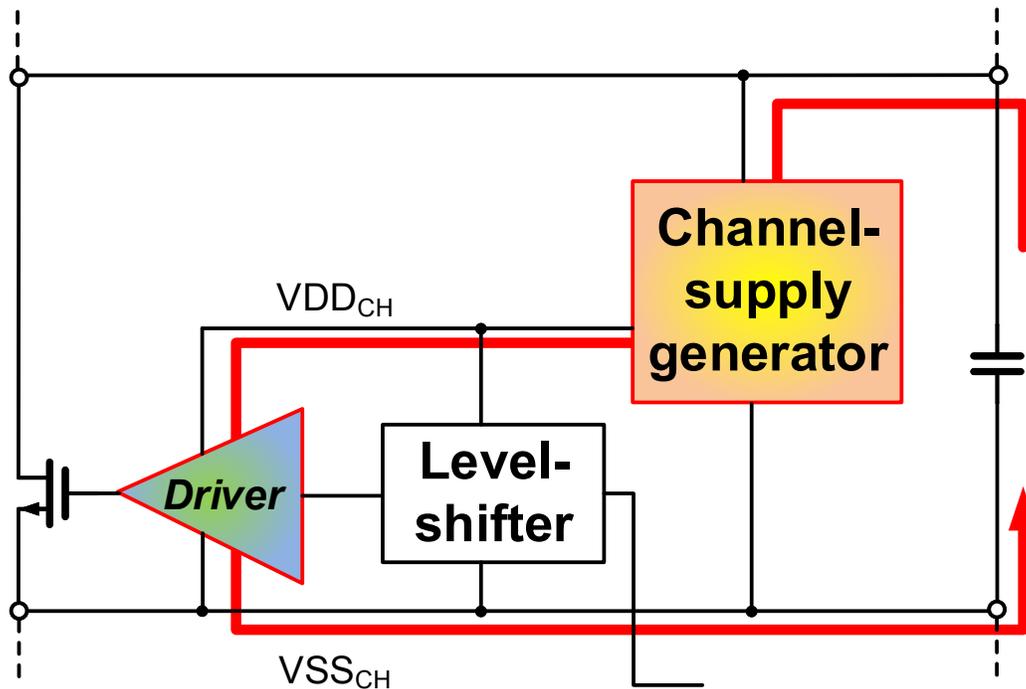
Figure A.4: The leakage current path in the gate driving channel is indicated in red. The thermal microscope detected a large power density in the channel supply generator. The PHEMOS detected a large current density in the driver.

the channel supply and the driver of the switching channel. The main regulator transistor (M1) in the channel supply has a high power density because it has a high drain-source voltage. When the chip is operating at 100 V, each flying capacitor blocks 25 V, and so the drain-source voltage drop across M1 is roughly 20 V. The same current passes through the driver, but the driver's voltage drop is at most 5 V. As such, the driver's leakage power is much lower than that of M1. However, the driver has a higher current density because of its smaller area.

A.5 FIB and Probe Station Testing

Although knowledge of the leakage path revealed which devices were malfunctioning, it was not sufficient to determine the cause. Further testing and analysis with a probe station was required.

Probe stations are useful because they can determine the voltage and waveform of nodes on die. A probe station contains several micromanipulators that can manipulate the needle-like probes to make contact with a metal trace. The probes are connected to an oscilloscope, which can display the voltage waveform of the trace. In general, there are two conditions for
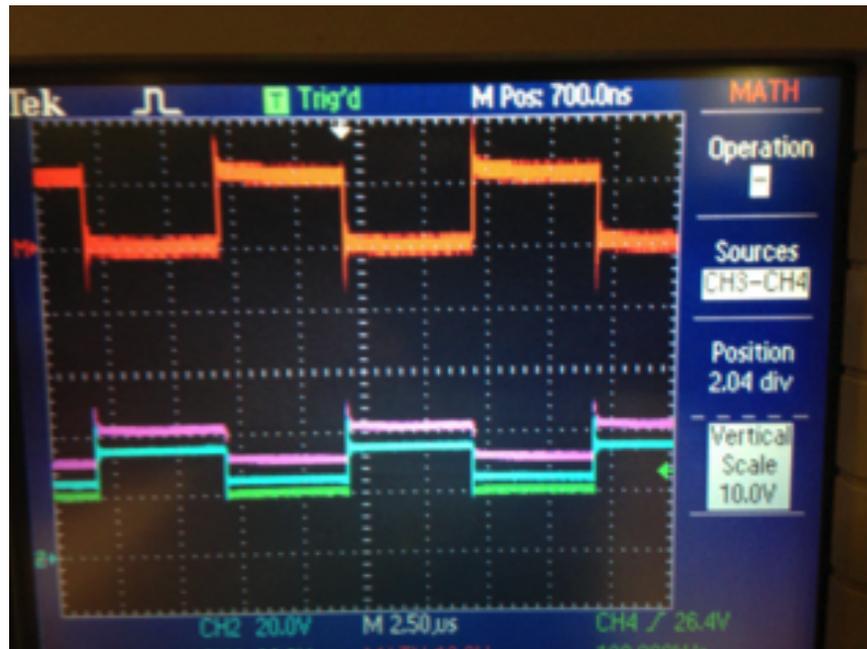
(a)
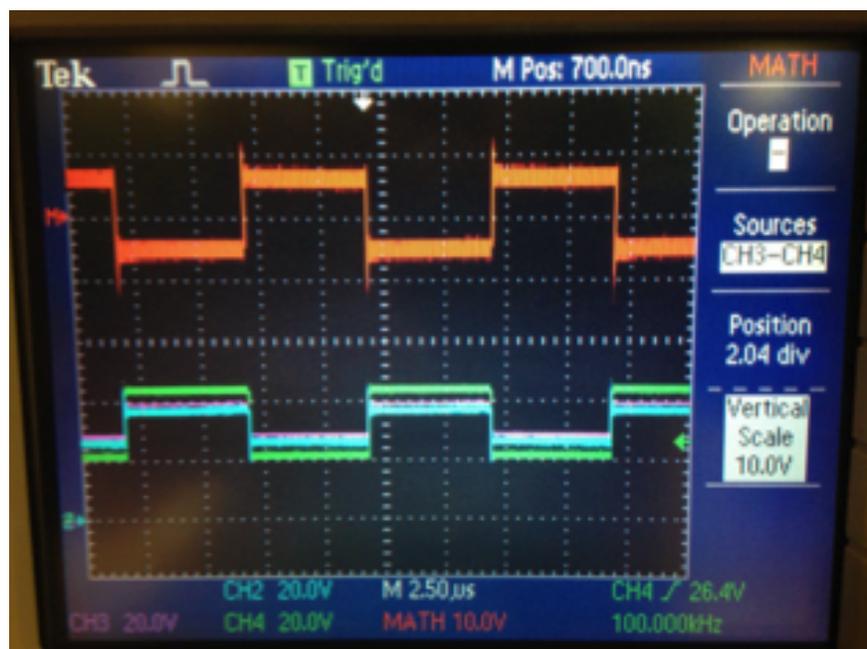
(b)

Figure A.5: Pictures of the oscilloscope hooked to a probe station. Probed nodes are all from the problematic gate driver. VDD$_{CH}$ is indicated in purple and VSS$_{CH}$ is green. Blue is the output of the driver. (*a*) Waveforms of the H-bridge stack test at 85 V without the 20 mA leakage. (*b*) Waveforms of the H-bridge stack test at 88 V with the 20 mA leakage. VSS$_{CH}$ (green) is pulled above VDD$_{CH}$ (purple), and latches for the remainder of the switching cycle.

probing nodes on die. First, the desired node must be on the top layer of metal. Second, the passivation layer must be removed at the desired point of contact. The passivation layer is a light coat of metal oxide that protects the die from corrosion. One option for probing is to pre-design the layout to have test windows without passivation. Alternatively, the entire passivation layer can be chemically removed from a decapped chip.

It was impossible to probe the switching channels because most of their nodes were buried below the top layer of metal. A focused ion beam (FIB) was required in order to tap these nodes to the surface. A FIB can etch through silicon, oxide, and metal with high precision. Once the buried nodes are revealed, it can then fill in the drill-hole with a conductive tungsten deposit. In this way, buried nodes can be tapped to the surface as long as there is a clear path to the node.

A FIB was used to tap various buried nodes to the surface for testing. Figure A.5 shows the results of probing VDD_{CH} and the driver (buffer) output node. These results show a notable difference below and above the leakage threshold. When the 20 mA leakage occurs (Figure A.5b), VDD_{CH} is at a lower voltage than VSS_{CH} for half of the cycles.

A.6 Results of the Failure Analysis

Designing a robust integrated gate driver is very difficult when the power MOSFET has a floating source (VSS_{CH}) that undergoes high-voltage swings. Ideally, the channel supply would maintain VDD_{CH} at a well regulated five volts above VSS_{CH}.

The capacitive coupling between VDD_{CH} and ground is much greater than what the simulation models predicted. This does not cause any problems in the fixed switching channels. However, it is very problematic in the floating channels that experience high-voltage swings. During a switching transient, the parasitic capacitance on VDD_{CH} forces the channel supply to work even harder to sustain a 5 V output. If the voltage swing is sufficiently high, VDD_{CH} will collapse, and VSS_{CH} will swing above VDD_{CH}.

The reverse diodes in the driver transistors conduct when VSS_{CH} is at a higher voltage than VDD_{CH}. Not only does this cause unwanted leakage, but it also latches VDD_{CH} below VSS_{CH}. The sustained leakage causes the voltage across the flying capacitor to collapse on every switching cycle. This behavior drastically decreases the chip's efficiency, and causes catastrophic failure at high voltage.

The most direct way to fix this problem would be to increase the size of capacitor C1 in Figure 3.6, which capacitively couples VSS_{CH} and VDD_{CH}. Unfortunately, there is not enough extra die area to drastically increase C1. Instead, the redesign of the first test chip involved capacitively decoupling the VDD_{CH} and V_{REF} nodes from the substrate as much as possible. Other possible solutions are discussed in Section 4.4.2.

Appendix B

Additional Performance Data

This appendix chapter contains additional performance data that is not necessarily relevant to the LED driver, but may be interesting for other applications.

B.1   Efficiency of the H-bridge Stack

The H-bridge stack is tested alone as described in Section 4.2.2. Like the complete driver, the output stage has a set of efficiency curves, shown in Figure B.3. As explained in Section 4.3.1, the efficiency curves are concave because gate driver losses dominate at low power, and conduction losses dominate at high power.

There are two output stage configurations that were originally considered. First, the H-bridge stack can connect to the load through the transformer. This is the standard configuration, and its benefits are previously explained in Section 3.2.2. The other output stage configuration is to directly load the H-bridge stack by connecting the load across DC level 1 and ground. In this configuration, the transformer and output diode bridge are removed, and the H-bridge stack functions as a switched capacitor charge pump. The direct load configuration requires less hardware, but does not galvanically isolate the LEDs from the power train.

At low voltage, the transformer configuration has a lower efficiency due to the additional conduction loss in the transformer and output diode bridge. However, the transformer configuration performs much better at higher voltage when its benefits outweigh the additional conduction loss. As explained in Section 3.2.2, the transformer allows power to be transferred from all the DC levels instead of just the bottom. In addition, the soft switching benefits from the transformer become more significant at higher power. The direct load charge pump is noticeably less efficient at high current.

The final benefit of the transformer is that it prevents the driver from failing at high power. In direct load configuration, the chip cannot handle a heavy load at high voltage. For this reason, Figure B.1b lacks a 100 V input efficiency curve. The transformer allows
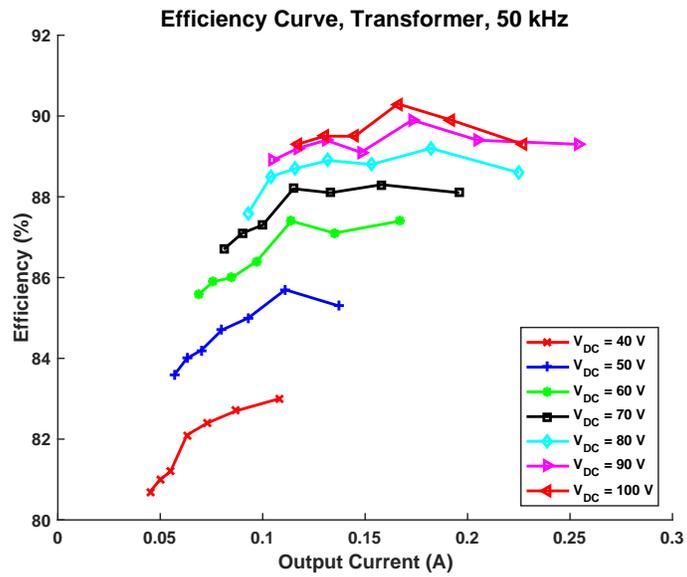
(a)
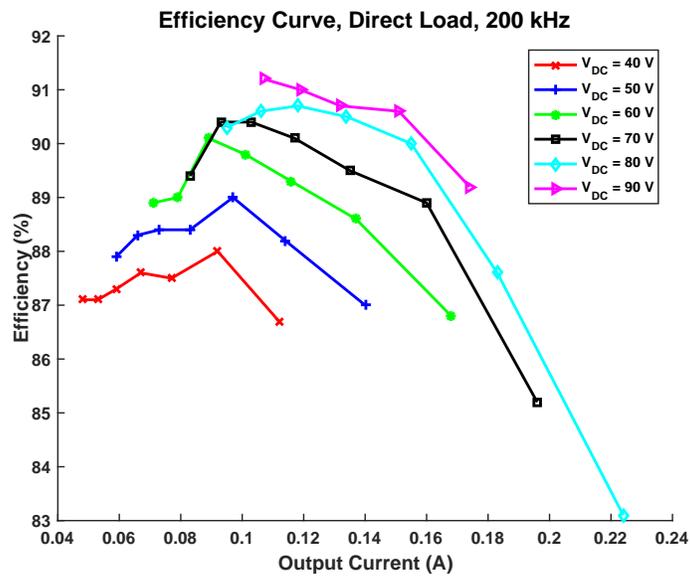
(b)

Figure B.1: The performance curves for the output stage. (a) Direct load, switching at 200 kHz. (b) Transformer output to load, switching at 50 kHz.

for a more gradual switching transition at the flying nodes, which helps prevent $\mathrm{VDD_{CH}}$ in Figure 3.5 from latching below $\mathrm{VSS_{CH}}$ (this mode of failure is explained in Appendix A.6).

Ultimately, the transformer-based output stage configuration was selected for this dissertation. The transformer configuration has many benefits including galvanic isolation and enhanced performance at high power.

B.2 Efficiency and Output Voltage

The output voltage of the LED driver can subtly affect the driver's efficiency. This can be important because the operating point of the output is determined by the type and quantity of LEDs. The relationship between efficiency and output voltage is shown in Figure B.2. Since the driver's power is determined at the input, the output power remains constant. As such, the output current varies inversely with the output voltage. The concave nature of the efficiency curves are previously explained in Section 4.3.1.
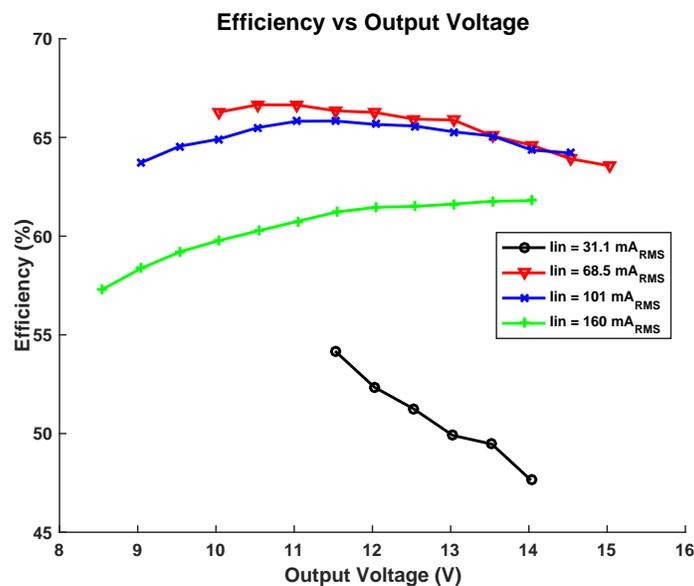
Figure B.2: Efficiency vs output voltage for 36 $\mathrm{V_{RMS}}$ input. The output voltage increases in increments of 0.5 V, and spans the range of correct functionality.

B.3 Performance of Alternate Configurations

The LED driver has several alternative configurations. These configurations can be significant for market scenarios that prioritize cost over quality. The standard configuration represents a high-end product with both ripple cancellation and galvanic isolation. There are two cost-saving variations to the standard configuration. The first involves removing the transformer, as described in Appendix B.1. The second involves removing the ripple-cancellation module and replacing it with a bank of four 50 μF electrolytic capacitors.

In general, using any of the alternate configurations increases the efficiency, as shown in Figure B.3. As described in Appendix B.1, the transformer configuration is less efficient than the direct load configuration at low power, but catches up at high power. However, using the ripple-cancellation circuit is always less efficient than using the electrolytic capacitor bank.
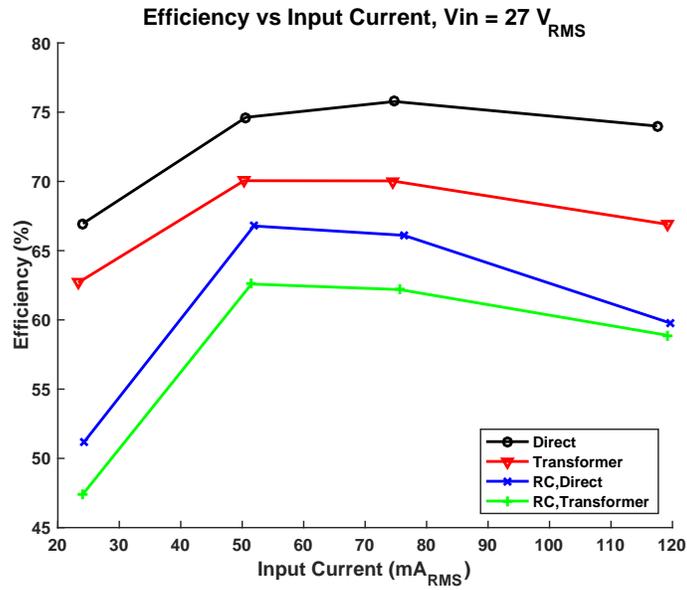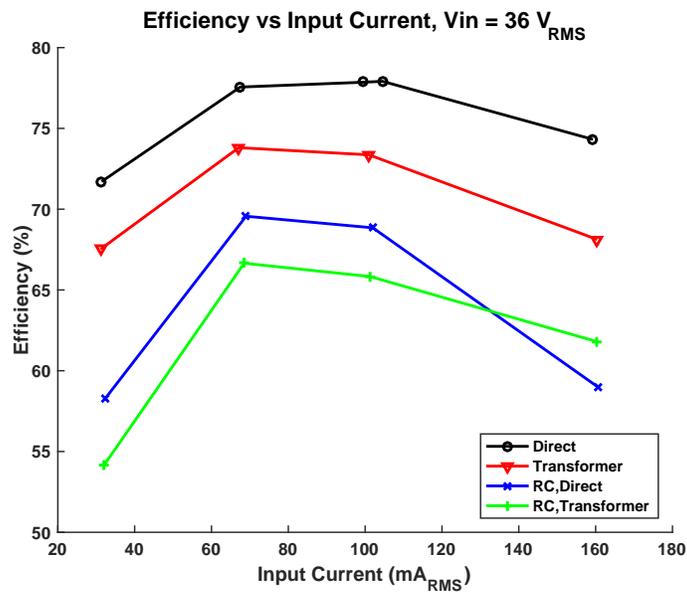
Figure B.3: The performance of alternate configurations at (a) V_{in} = 27 V_{RMS}, and (b) V_{in} = 36 V_{RMS}. The configurations are with direct output or transformer output, and with or without the ripple-cancellation (RC) module. For reference, the standard configuration is "RC,Transformer".

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