III-V Nanolaser Integration with CMOS Electronics and Silicon Photonics

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III-V Nanolaser Integration with CMOS Electronics and Silicon Photonics

by

Fanglu Lu

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Committee in charge:

Professor Constance J. Chang-Hasnain
Professor Eli Yablonovitch
Professor Oscar D. Dubon

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Abstract

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Using optical signal rather than electrical signal to transmit information on silicon-based computer chips, also known as intra-chip optical interconnect, can potentially boost computation speed and reduce energy consumption. This requires a laser source on silicon, which is a challenging task. Almost all commercial semiconductor lasers are made of III-V material because silicon is an inefficient emitter due to its indirect bandgap. Therefore, integration of III-V laser on silicon is a must towards practical optical interconnect. However, both lattice constant and thermal expansion coefficient mismatch between III-V and silicon fundamentally restricted high quality III-V thin film growth on top of silicon substrates. III-V nanostructures on silicon, on the other hand, can overcome this issue thanks to their small footprint and fully relaxed strain from lattice mismatch. As a result, III-V nanolaser becomes a promising candidate as the on-chip light source for optical interconnect.

In this dissertation, our III-V nanopillar lasers experimentally demonstrate integration capabilities with silicon-based electronics and photonics. The nucleation and growth mechanism of InGaAs and InP nanopillars is first studied with characterization observations, unveiling the reason accounting for the high quality nanopillar. The superior crystal quality, together with unique 3D whispering gallery mode, enables the laser oscillation in as-grown nanopillars. To prove the CMOS compatibility, these nanolasers are monolithically grown onto silicon-based transistor chips, without compromising the electronic performance of chips. In addition, horizontal nanopillar growth is developed to integrate nanolasers with silicon waveguides in an end-fire manner. The coupling between laser and waveguide is prominently observed under photoluminescence experiment, serving as a proof-of-concept for integration with more complicated photonic circuits. To avoid laser emission absorbed by silicon, long wavelength lasers are obtained with InP/InGaAs/InP quantum well nanpillars and three novel optical cavities. Detailed laser modeling is also performed to provide guidance for further laser optimization. For electrical pumping, we also explores methods to make perfect nanopillar diodes. Furthermore, an optical link with nanopillar devices and polymer waveguide is shown to be functional to transmit signals on silicon substrate. With these experimental demonstrations, this III-V nanolaser strategy presents a great potential to achieve on-chip laser source.

To my parents, Gaoqiang Lu and HuiFang Fang

for their love and support

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Working in the large "Nanoneedle/Nanopillar" team where material synthesis, fabrication and characterization are closed interleaved, I would never make my way this far in research without the assistance and coordination of my colleagues in Prof. Chang-Hasnain's group. I would like to thank the senior colleagues who mentored me and led me into this exciting research area, including Dr. Roger Chen, Dr. Kar Wei (Billy) Ng, Dr. Thai-Truong Du Tran and Dr. Wai Son (Wilson) Ko. I also want to thank Dr. Chih-Wei (Linus) Chuang and Dr. Michael Moewe for their discovery of nanoneedle, which enabled my following research. At the same time, it has been a great pleasure to have worked with Dr. Fan (Stephon) Ren, Dr. Gilliard Nardel Malheiros Silveira, Dr. Daria Skuridina, Dr. Saniya V Deshpande, Kun (Linda) Li, Hao (April) Sun and Indrasen Bhattacharya. Most of my research outcomes originate from our collaborative work.

Although not covered in this dissertation, I worked on high contrast grating project as well before I switched to "Nanoneedle/Nanopillar" project. This is my true starting point of research and plays a critical role in shaping my research skills. Thus, I would like to thank those who contribute substantially to that part of work: Dr. Forrest G. Sedgwick, Dr. Vadim Karagodsky, Dr. Christopher Chase, Dr. Weijian Yang and Tianbo Sun. Many thanks to other colleagues in the group for making such a pleasant and supportive working environment, particularly to Dr. Yi (Frank) Rao who helped me settle down in US when I first came, James Ferrara who always brought happiness to this group, Li (Andy) Zhu who has been a good friend in life, and Stephen Adair Gerke who helped me with career searching.

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Chapter 1 Introduction

In nature light travels fastest. It has already been used to transmit signal in optical fiber (replacing electrical signal in copper wires) for long-distance communication, which lays the foundation for fast-speed internet worldwide. Researchers also work on making light travel on a much smaller scope -- on a tiny silicon chip which could be of centimeter size. This research area is named as “silicon photonics” and has two tantalizing prospects. The first one is marriage of nano-photonics and nano-electronics on a single silicon chip to achieve complex functionalities otherwise unattainable, such as bio-sensing and lab-on-a-chip. The other prospect is the focus of this dissertation -- optical interconnect.

As we know, the technology behind integrated circuits (ICs), complementary metal-oxide-semiconductor, or simply CMOS, has enjoyed fast revolution governed by Moore’s law [1]. But recent years have witnessed the bottlenecking of micro-processor speed upscaling. One reason for this is that traditional IC chips utilize metal wire to communicate electrical signal between transistors. What if the same paradigm shift from metal wire to optical fiber for telecommunication occurs on the chip? What if we use the optical signal to transmit signals on the chip?

The on-chip optical interconnect offers multiple advantages over electrical method [2]. First, optical interconnect has higher interconnect density. Unlike electrical wires, optics does not have resistive loss physics limiting bit rates, so it can transmit higher data rates over relatively long lines and limited cross sections. In addition, because optics frequency is so high, there is a wide available spectrum allowing wavelength-division multiplexing (WDM) that could increase the total bit rate of a given optical channel. Second, optical interconnect might have lower energy consumption because it is unnecessary to charge the line to the operating voltage of the link [3], [4]. Lastly, optics may be capable of delivering and retaining very precise timing in clocks and signals [5]–[7] because optical signals do not spread substantially over the size scale of a computer chip.

Perhaps the most crucial and challenging component for optical interconnect is an on-chip laser source. Although it is the material cornerstone for the entire micro-electronics empire, silicon is not an efficient light emitter due to its indirect bandgap. On the other hand, group III-V materials are commonly used as active gain medium in optoelectronic applications such as lasers and photodetectors. Thus, integrating these two material systems together becomes the holy grail of achieving lasers on silicon.

Chapter 2 first overviews a variety of earlier research efforts on integrating III-V with silicon and their limitations respectively. Following that, we propose our high quality III-V nanopillar growth on silicon and point out their unique advantages. Detailed discussions about nanopillar nucleation and growth mechanism are subsequently performed with experimental observations, in order to fully understand growth dynamics. Based on that, nanopillar growth site control is experimented and preliminary result will be presented. The material focus of our work is

InGaAs-based nanopillar and InP-based nanopillar, and their superior material quality has already led to laser oscillation on silicon.

In Chapter 3, we start to focus on the integration capability of III-V nanopillar laser. To demonstrate CMOS compatibility, nanonpillar lasers are directly synthesized on transistor chips and the effect of III-V growth on transistor operations will be evaluated. Another important aspect of viable on-chip light source is integration with silicon photonics, as will be discussed in Chapter 4. To couple the nanolaser emission into silicon waveguide, a horizontal nanopillar growth is proposed with an end-fire waveguide coupling mechanism. The coupling effect will be experimentally demonstrated and quantitative coupling efficiency will be calculated. In addition, nanopillar integration with waveguide also provides opportunities to design novel nanopillar laser cavities, to further improve laser performance.

Chapter 5 details efforts of making long wavelength nanopillar laser. To transmit in silicon waveguide, laser light must be transparent to silicon. Hence, an emission wavelength of at least 1.1μm is required. The most promising method is based on InP/InGaAs/InP double heterostructure, where InGaAs layer presents itself as thin quantum well to minimize strain. Tunable emission beyond silicon transparency, depending on indium composition and quantum well thickness, will be shown with these quantum wells. Nanolasers with three different types of optical cavities are subsequently demonstrated, each with silicon transparent wavelength. Furthermore, theoretical study on optical gain model and cavity mode behind these long wavelength nanolaser results is performed, for the sake of further optimizing laser performance and moving towards electrically pumped devices.

Before closing, electrical injection into these nanopillars will be discussed in Chapter 6. For ensemble nanopillars, electrical contacts are relatively easy with typical photolithography and metal evaporation. However, practical laser source requires single pillar devices and thus presents more challenges. In particular, the current shunt path problem is most critical, in order to make a perfect p-i-n diode. Three methods will be presented to kill the shunt path and near-ideal diodes are resulted. Last but not least, a functional optical link based on electrical-driven nanopillar devices will be shown to transmit signals on silicon substrate, proving the great potential for nanopillar functioning as the on-chip light source.

With the integration capabilities with CMOS and silicon-photonics, III-V nanopillar laser becomes one of the most promising platforms for building on-chip light sources. The last missing piece of on-chip optical interconnect might finally be realized and fits into the big picture of making much faster computer chips, enabling next generation of technology boom.

Chapter 2 III-V Nanopillar Growth on Silicon

Optical interconnects on silicon-based electronics offer the tantalizing prospect of cost-effectively satisfying the insatiable need for higher data speeds and lower power consumption in computing [2]. Over the years, there has been a myriad of inspiring breakthroughs in this research field, including modulators on silicon [8], [9], silicon waveguide, photodetectors on silicon [10], [11]. Nevertheless, integrating lasers onto silicon, thus forming indispensable on-chip light sources, still remains a major challenge.

Some recent efforts have focused on directly making group IV lasers on silicon, by either taking advantage of silicon's Raman scattering effect [12]–[14], or engineering strain and doping concentration to improve the radiation efficiency of germanium [15], [16]. These methods are limited by the fundamental fact that group IV materials have indirect bandgaps and thus provide insufficient radiation efficiency.

On the other hand, group III-V materials are direct bandgap materials and serve as the most commonly used active gain medium in optoelectronic devices. Naturally, researchers turned to the heterogeneous integration strategy and tried to physically bond III-V materials onto silicon [17]–[26]. These methods glue the III-V epitaxial layer onto a silicon substrate with an intermediate layer, usually metal, epoxy, dielectric layer or solder balls. III-V lasers on silicon using this bonding technique have been successfully demonstrated [23]–[25], [27]–[30]. However, the complicated surface morphology of CMOS chips makes the large scale alignment of III-V material with silicon substrate very challenging.

People also consider chemical epitaxy of III-V on silicon. Yet, mismatches of both lattice constant and thermal expansion coefficient between these two material systems result in high density of dislocations in III-V thin film, which leads to a poor optoelectronic performance [31]–[33]. The polar nature of III-V thin film on non-polar silicon also facilitates the formation of anti-phase domains, another source of crystal defects [33], [34]. To address these problems, some researchers recently demonstrate lattice-matched Ga(NAsP) thin film grown on silicon substrate [35]–[37]. Despite its indirect bandgap, GaP has the lattice constant closest to silicon among all III-V compounds (only 0.36% mismatch). By alloying arsenic into it, GaAsP becomes direct bandgap material that can emits efficiently. In addition, nitrogen is added into this quaternary alloy GaNAsP such that its lattice constant is exactly matching that of silicon. With this lattice-matched, direct bandgap material on silicon, laser operation on silicon has been obtained [38]. Nevertheless, it is difficult to integrate this kind of laser onto CMOS chips in a back-end-of-line (BEOL) process, due to its high III-V epitaxial temperature around 575ºC [39]. Front-end-of-line (FEOL) integration is also challenging since it will bring III-V contaminants into CMOS process facilities.

A more attractive approach to integrate III-V on silicon is using III-V nanostructure. Thanks to its small footprint, nanostructure can elastically relax the strain from lattice mismatch at the III-V/Si interface, illustrated in Figure 2-1. Thus, high quality single crystalline material can be obtained in the III-V nanostructure. In addition, small area of III-V/Si interface minimizes chances of forming anti-phase domain boundaries. Following this strategy, III-V lasers based on quantum dots on silicon has been achieved under electrical injection recently [40]–[42].

However, these III-V quantum dots still require synthesis temperature much higher than the thermal budget for BEOL integration and thus has limited application for on-chip laser purpose. To obtain practical on-chip III-V laser source, it is of utmost importance to develop low temperature nanostructure growth.

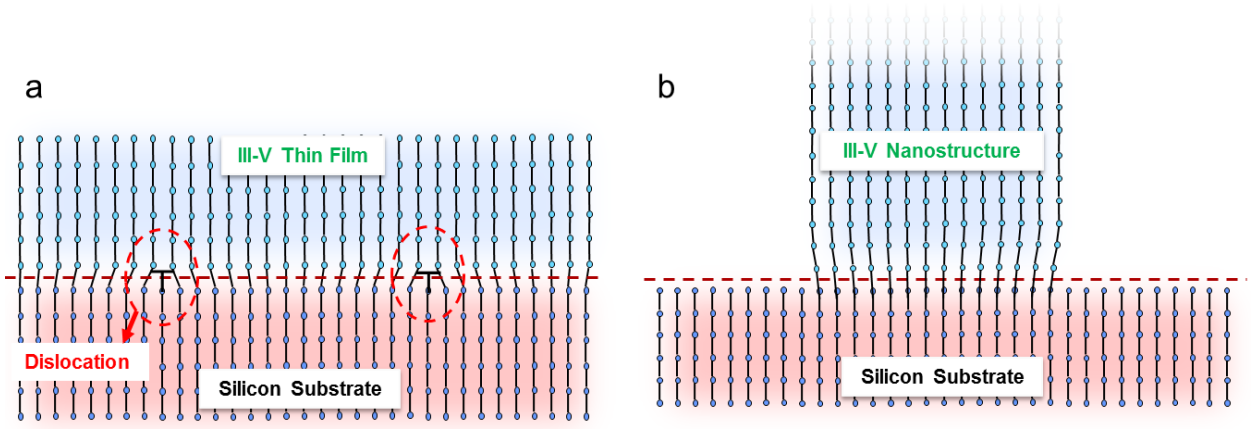


Figure 2-1 Schematic of III-V epitaxial thin film on silicon substrate versus III-V nanostructure on silicon substrate. (a) Due to lattice mismatch, III-V thin film on silicon induces dislocations at the interface that propagate along III-V growth axis, which deteriorates crystal quality. (b) Stress relaxes elastically at the bottom of nanostructure, maintaining superior crystal quality on the top.

Nanowire is a promising candidate for on-chip light source because it can be grown on silicon at relatively low growth temperature with superior optical quality [43], [44]. There are primarily two methods to synthesize nanowires. The first one is vapor-liquid-solid (VLS) growth, which utilizes gold droplet as the catalyst to create super-saturation to drive nanowire vertical growth [43], [45]. The other one is selective area growth (SAG), where silicon substrates are patterned with oxide material to initiate nanowire growth caused by atom affinity contrast between substrate and mask material [46]. Both methods have demonstrated successful III-V material integration on silicon substrate. Yet, there are some limitations when it comes to applying them to make on-chip nanolasers. For VLS growth, the typical catalyst gold is a deep level trap for silicon, which can relentlessly destroy CMOS electronic performance [47]. Additionally, nanowires unfortunately have a critical diameter of a few hundreds of nanometers, beyond which elastic strain relaxation fails and nanowires become defective [48]. With the nanowire critical diameter much smaller than wavelength of interest, their small lateral dimension results in very weak optical confinement, especially at long wavelength. This is not desirable for building a good laser cavity. Besides, small footprint of nanowire leads to a large surface-to-volume ratio, which could result in significant amount of surface non-radiative recombination in III-V without proper surface passivation [49].

To overcome all these barriers along the way towards on-chip laser source, we have developed unique single-crystalline III-V nanopillar/nanoneedle growth directly on silicon substrate by catalyst-free metal-organic chemical vapor deposition (MOCVD) at low growth temperature [50]–[56]. The growth starts with a tiny nanoneedle nucleation seed accommodating the lattice mismatch between III-V material and silicon, allowing high quality single crystalline material to

growth subsequently. Distinct from nanowires, the following growth occurs in a core-shell manner, enlarging the lateral dimension of nanoneedle/nanopillar in a scalable fashion. This results in a footprint of nanoneedle/nanopillar well beyond the critical diameter of nanowires. In short, this metastable growth not only enables high quality nano-material as the gain medium, but also makes nanopillar suitable to construct a large enough optical cavity. Furthermore, The CMOS compatibility is ensured by its gold-catalyst-free nature and synthesis temperature as low as 400ºC-450ºC. Last but not least, MOCVD technique is already commonly applied in optoelectronic industry and thus this scalable monolithic integration technology is highly transferrable.

In this chapter, we will dive deep into more growth details and experimental proofs of nanopillar's high crystal quality. Theoretical and experimental analysis on nucleation and growth mechanism will be also discussed. We limit our discussion mostly on InGaAs-based nanopillar and InP-based nanopillar, partly because they are the ubiquitous material choices of most photonic devices, partly because of our material source limitation. Lastly, the growth site control of nanopillars will be evaluated with our preliminary experimental success.

2.1 InGaAs nanopillar growth

The discovery of nanoneedle came with serendipity. GaAs nanoneedles, as shown in Figure 2-2, were accidentally found to grow on unintentionally roughened region of silicon substrates. Under scanning electron microscope (SEM), these nanoneedles demonstrate hexagonal needle shape with smooth crystal facet surface. High resolution transmission electron microscope (TEM) image further helps reveal the Wurtzite single crystalline phase without any dislocations, as well as its atomically sharp tip. Needless to say, it is the defect-free nature of these nanoneedles that truly motivates us to further study this unique growth, expand our nano-material library to InGaAs nanopillar and InP nanopillar, and fabricate optoelectronic devices based on them.

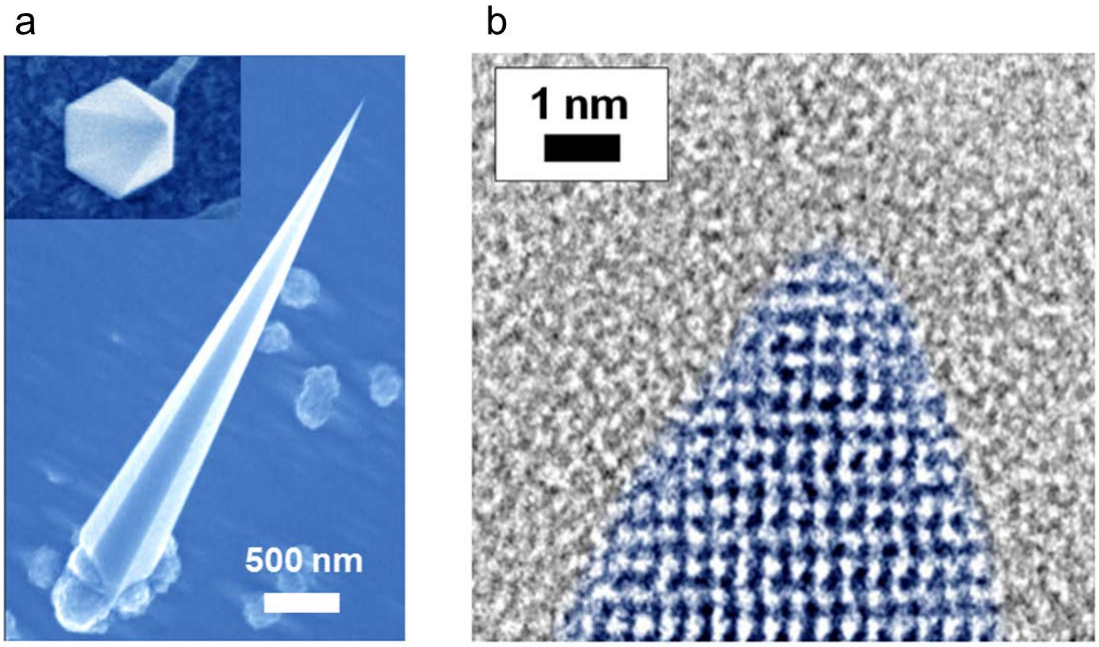


Figure 2-2 Visualization of GaAs nanoneedle. (a) Scanning electron microscope (SEM) image of a typical GaAs nanoneedle. (b) Transmission electron microscope (TEM) image of the atomically sharp tip of nanoneedle.

2.1.1 InGaAs nanopillar growth details

Following our initial discovery of GaAs nanoneedle, we further develop InGaAs naopillar growth because of its wavelength tunability [50]. The typical InGaAs nanopillar structure has an InGaAs core with a GaAs shell as surface passivation layer, as shown in Figure 2-3. The silicon substrate is first degreased and deoxidized, followed by a repeatable method of silicon surface roughening. For that, a special gadget has been devised to create multiple evenly-spaced surface scratches on silicon. Growth is carried out in an EMCORE D75 MOCVD reactor. Tertiarybutylarsine (TBA) is introduced to the reactor at temperatures higher than 200 ^{o}C. Prior to growth, in-situ annealing is performed for 3 minutes at 591 ^{o}C. After annealing, the temperature is reduced to the growth temperature (typically 400-410 ^{o}C for InGaAs nanopillars) for 3 minutes, followed by 2 minutes of temperature stabilization. Triethylgallium (TEGa) and trimethylindium (TMIn) are then introduced to the reactor to begin the 60-minute InGaAs nanopillar core growth. TMIn mole fractions are kept constant at 9.86×10^{-7}, 1.38×10^{-6} and 1.73×10^{-6} to achieve 12, 15 and 20% indium compositions, respectively. The TEGa mole fraction is kept constant at 1.12×10^{-5}. All sources used a 12 l min^{-1} hydrogen carrier gas flow. The TBA mole fraction is 5.42×10^{-4}, giving a V/III ratio of approximately 43. A GaAs shell is then grown around the InGaAs core with the same TEGa and TBA mole fractions used for core growth, with a V/III ratio of 48. Figure 2-4 summarizes temperature change and metal-organic source appearance during a typical InGaAs nanopillar growth run.

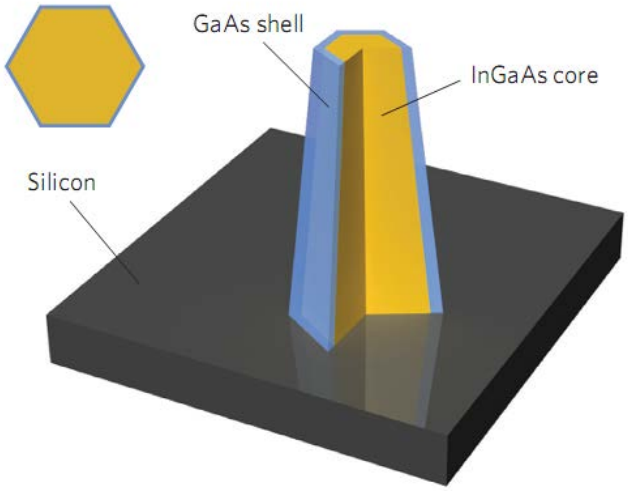


Figure 2-3 Schematic of a vertical InGaAs nanopillar with InGaAs core and GaAs passivation shell on silicon (111) substrate.

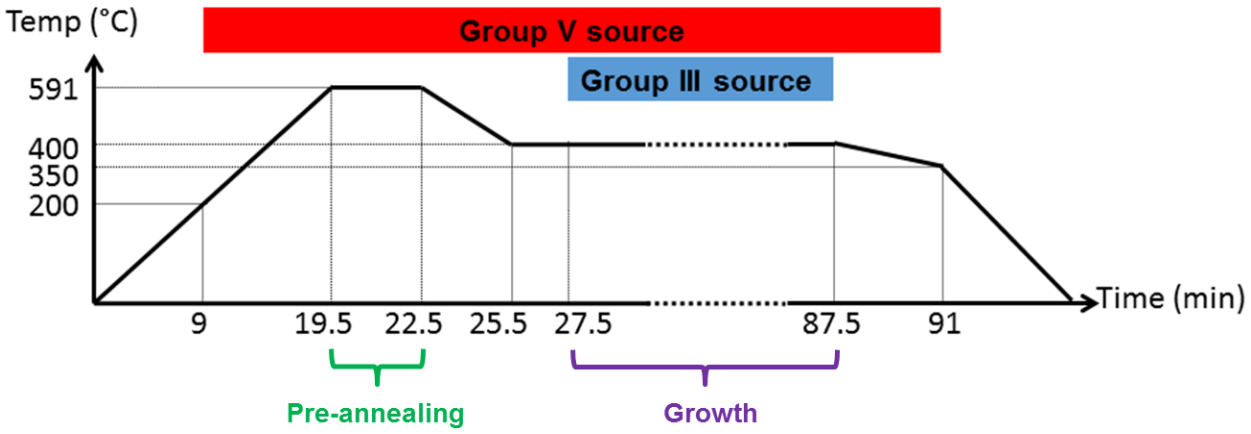


Figure 2-4 Temperature change and metal-organic source appearance during a typical nanopillar growth run. The growth run consists of two stages. In the first stage (pre-annealing stage), the temperature ramps up to 591ºC and only group V source (TBA) flows in. In the second stage (growth stage), the growth temperature is around 400ºC and both Group III source (TMGa and TMIn) and group V source (TBA) flows in.

After the growth, InGaAs nanopillars can be found close to the roughened region. Figure 2-5(a) is the tilt view SEM image of a typical InGaAs nanopillar with GaAs passivation shell on a Si (111) substrate. The nanopillar grows vertically along Si <111> direction with a hexagonal cross section and a small taper angle. The well-faceted hexagonal shape and smooth sidewall are the first indication of excellent crystal quality. Unlike GaAs nanoneedle, InGaAs nanopillar has a flat top. A more zoom-out SEM image Figure 2-5(b) shows several nanopillars with their positions randomly distributed. With the global top view image Figure 2-5(c), the roughened region is observed to be covered with many non-single-crystalline III-V nanostructures, probably due to its trapping effect on the group III source. And the single crystalline nanopillars only grow next to the roughened region (in this image, approximately within 30μm distance from edge of roughened region).

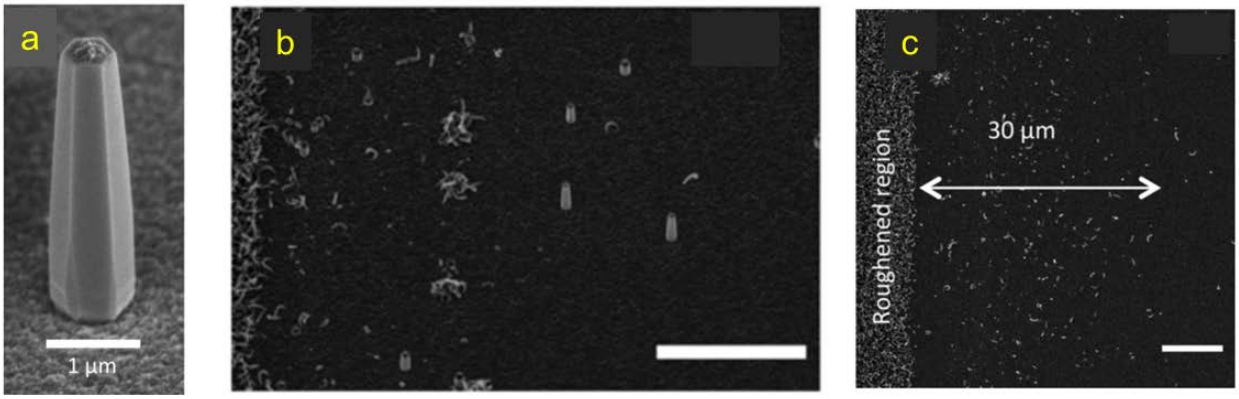


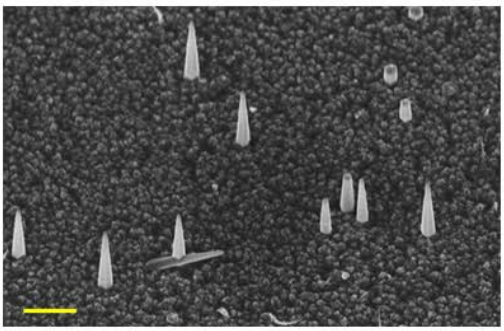
Figure 2-5 SEM images of InGaAs nanopillars. (a) Tilt view SEM image of a typical InGaAs nanopillar. (b) Zoom out tilt view SEM image of several nanopillars close to roughened region. (c) More zoom out tilt view SEM image showing the roughened region together with region where nanopillars grow. Scales bars in b and c represent 10μm.

2.1.2 InGaAs nanopillar nucleation mechanism

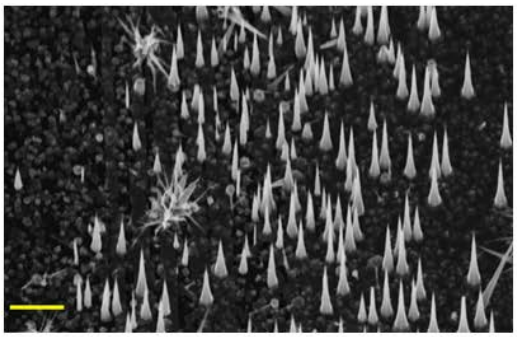
The most critical challenge of nanopillar growth is about precise control of growth site and density. This requires full understanding about nucleation mechanism and growth mechanism of our nanopillar, which will be discussed in depth in this and next sections.

As a preliminary study on the nucleation mechanism, we have looked at our InGaAs nanopillar growth condition in a more detailed manner, as shown in Figure 2-4. It is obvious that the growth run consists of two stages. In the first stage (pre-annealing stage), the temperature ramps up to 591ºC and only group V source (TBA) flows in. In the second stage (growth stage), the growth temperature is around 400ºC and both Group III sources (TMGa and TMIn) and group V source (TBA) are present.

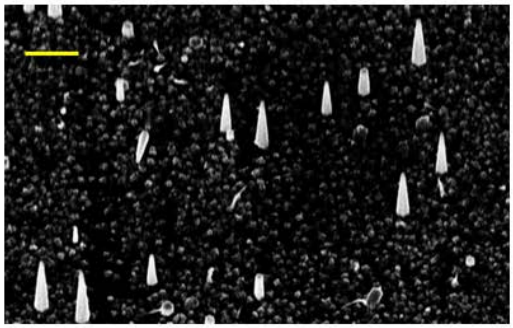
We want to investigate when the nanopillar nucleation occurs in the growth run: is it in "pre-annealing" stage or "growth" stage? Thus, four growth experiments were performed with different TBA flow rates, keeping all the other conditions the same. The first growth has a TBA flow rate of 22sccm (defined as "high TBA") in both pre-annealing stage and growth stage; the second growth has a TBA flow rate of 1.66sccm (defined as "low TBA") in both stages; the third growth has a high TBA flow rate in pre-annealing stage, and yet a low TBA flow rate in growth stage; the fourth growth experiment has a low TBA flow rate in pre-annealing stage, but a high TBA flow rate in growth stage. The growth results are summarized in Figure 2-6. The difference in TBA flow leads to changes in both nanopillar density and nanopillar shape. The nanopillar density should be determined by nanopillar nucleation, while nanopillar shape is determined by nanopillar growth. Comparing Figure 2-6(a) and (b), we see that by changing TBA flow from high to low, the nanopillar density increases, and the nanopillar sidewall changes from straight to curved. Comparing Figure 2-6(a) and (c), the nanopillar density and shape stays the same despite the TBA flow difference during the pre-annealing stage. A comparison between Figure 2-6(b) and (d) confirms this. The most important conclusion is that the nanopillar density is only determined by the growth stage condition. And therefore, the nucleation should occur during the growth stage (not the pre-annealing stage), or more specifically at the very beginning of the growth stage, when the group III source is first introduced into the growth chamber. Thus, it can be derived that the nucleation is driven by the group III metal source, which is indium in our case.



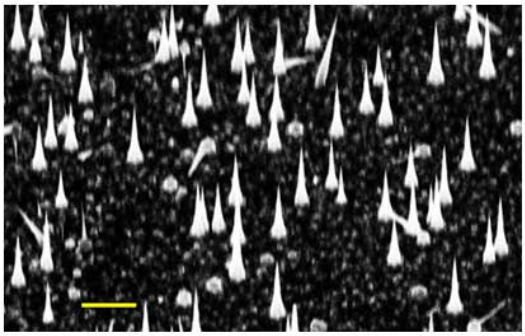
(a) TBA of Pre-annealing and Growth stage: High, High



(b) TBA of Pre-annealing and Growth stage: Low, Low



(c) TBA of Pre-annealing and Growth stage: Low, High



(d) TBA of Pre-annealing and Growth stage: High, Low

Figure 2-6 SEM pictures of growth results with different TBA flow rate (22sccm TBA defined as high flow rate, whereas 1.66sccm defined as low flow rate) in pre-annealing stage and growth stage respectively: (a) high; high. (b) low; low ; (c) low; high; (d) high: low. The scale bars represent 1μm.

To further confirm this "indium-driven nucleation" hypothesis, a series of samples are grown under various V/III ratios in the growth stage. V/III ratio in this experiment is varied by changing group V TBA flow rate while maintaining group III flow rate. Figure 2-7(a)-(c) shows the dependence of nanopillar density on the V/III ratio. With reduced V/III ratio, the nanopillar density increase drastically. Moreover, the nanpillars nucleation much further away from the border of roughened region when TBA flow rate is low. Figure 2-7(d)-(e) illustrates that the nanopillar growth region can be as far as 120μm away from the edge of roughened region with low TBA flow rate, whereas high TBA flow rate only gives 30μm range of nanopillar growth. These results indicate that InGaAs nanopillar nucleation is greatly enhanced by the longer diffusion length of group III source which is a result of lower V/III ratio.

Combining all the observations, we hypothesize that seeding of nanopillars starts with group III cluster formation on the roughened silicon surface. The mechanical roughening serves two functions in the nucleation process. First, it creates an uneven silicon surface, which can trap group III metal cluster. The second function of mechanical roughening is that it removes the surface Si-H bonds formed in wafer deoxidation step, facilitating oxidation of roughened silicon region. It essentially forms a porous native oxide layer in the roughened region. Since III− V cannot nucleate on top of native oxide, group III adatoms tend to cluster into very small droplets.

These nanodroplets diffuse away from the roughened regions to silicon surface and react with As adatoms to form InGaAs nanocrystals. The high super-saturation of adatoms favor the formation of WZ nanostructures with high aspect ratios, which later on evolve into InGaAs needles and pillars [57]. The reduction of V/III ratio leads to longer diffusion length of group III adatoms and thus increases the nucleation density as well as the range of nanopillar nucleation. This nucleation hypothesis agrees well with all the experimental observations in Figure 2-6 and Figure 2-7.

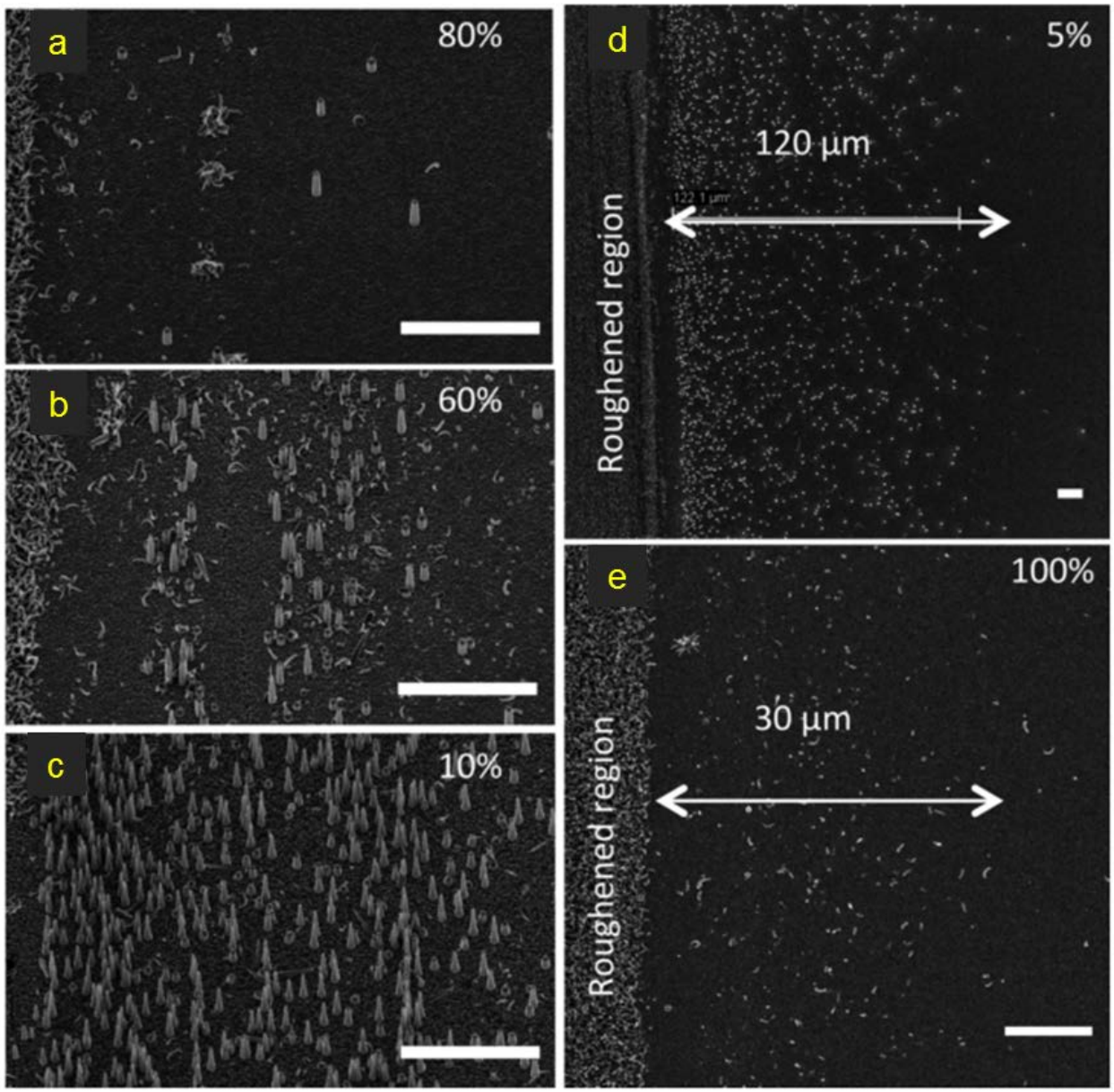


Figure 2-7 InGaAs nanopillar density and growth range versus various V/III ratios. The 100% V/III ratio represents a V/III ratio of 43. The V/III ratio for each SEM is labeled on the top right hand corner. (a-c) Nanopillar density increases drastically as V/III ratio decreases from 80% to 10%. (d-e) Nanopillar growth extends 120µm away from

roughened region with 5% V/III ratio, whereas there is only 30μm growth range with 100% V/III ratio.

2.1.3 InGaAs nanopillar growth mechanism

Although nanopillar nucleation is assisted by metal nanocluster, similar as VLS nanowires, the following growth mechanism of InGaAs nanopillar is completely different from VLS growth. VLS growth requires a catalyst metal droplet to dissolve the reactants and stays at the tip of nanowire during the entire growth process [45]. However, no metal catalyst is ever observed at the tip in our growth, for both GaAs nanoneedle (tip shown in Figure 2-2(b)) and InGaAs/GaAs nanopillar (tip shown in HAADF image Figure 2-8).

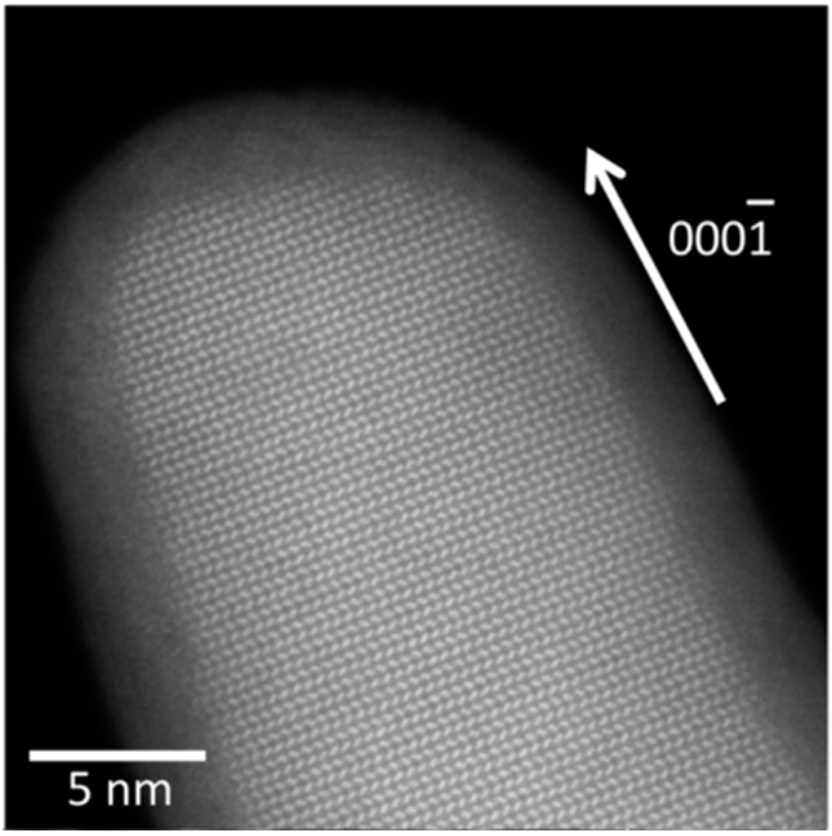


Figure 2-8 High-angle annular dark-field (HAADF) image of the tip of an InGaAs/GaAs nanopillar.

In addition, VLS growth can only elongate nanowire along axial axis with its lateral dimension predetermined by the size of metal droplet. Our nanopillar growth, on the other hand, turns out to be a core-shell growth mode, as illustrated in Figure 2-9. Starting with the nanoneedle seed, nanopillar grows in a layer-by-layer way, not only elongating nanopillar, but also enlarging nanopillar's footprint far beyond critical diameter of nanowires. It is worth noting that vertical growth ceases at a certain point, transforming nanoneedle into nanopillar shape, due to inclusion of indium in the growth.

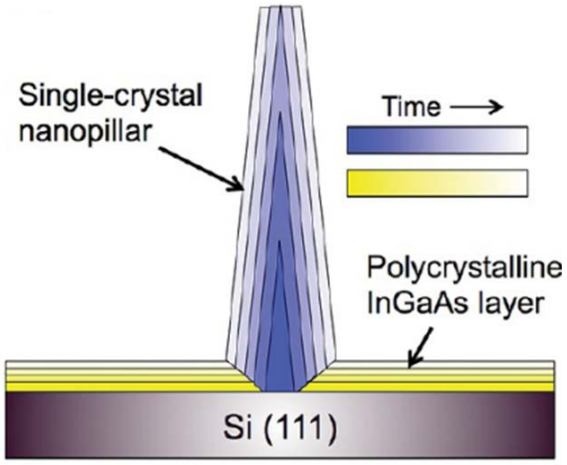


Figure 2-9 Schematic illustrating core-shell growth sequence of InGaAs nanopillar.

To prove the core-shell growth mechanism, time evolution experiment is performed by varying growth time. The results are summarized in Figure 2-10. From the SEM images, nanopillar maintains its hexagonal cross section and slowly transforms from needle seed to pillar shape as growth time increases. The base diameter of nanopillar scales linearly with growth time, resulting a radial growth rate of 0.5μm/hour or so. The length first increases linearly with growth time, but starts to saturate after roughly 30min. The observations match well with core-shell growth mode prediction.

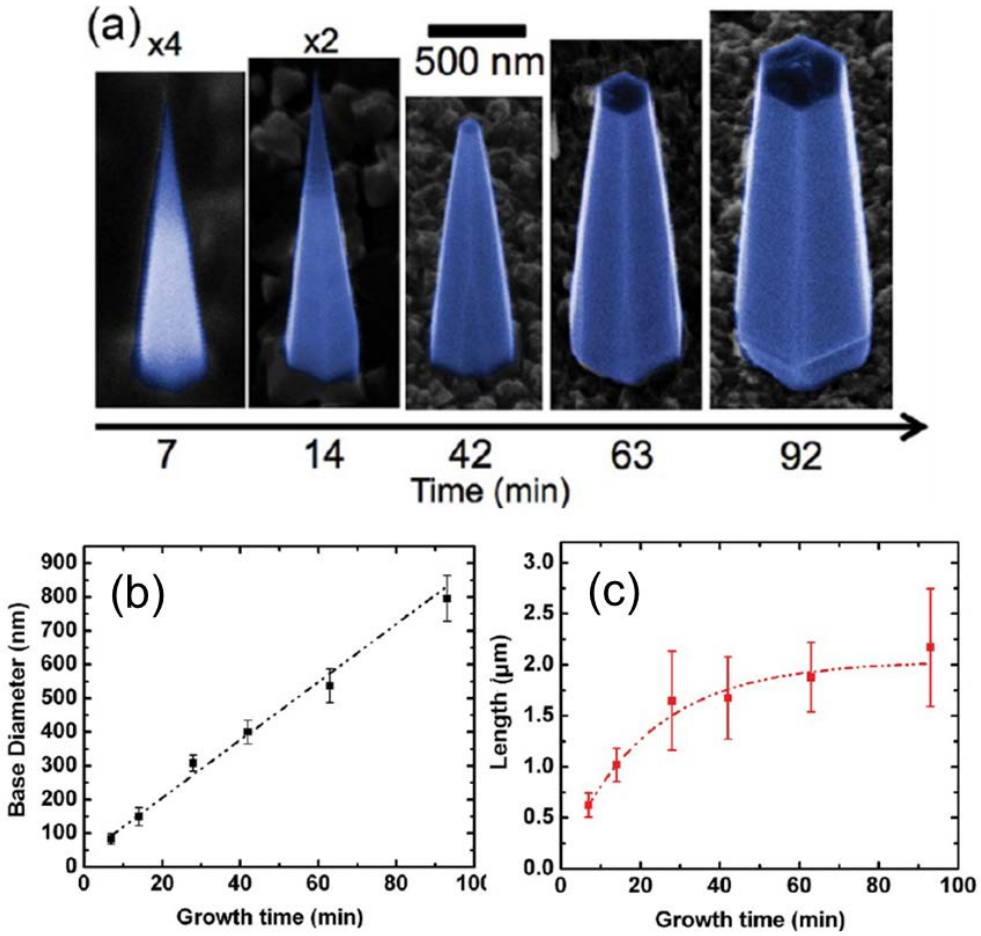


Figure 2-10 Time evolution of InGaAs nanopillar growth. (a) SEM image of nanopillars with different growth time. (b) Base diameters of nanopillars scaling linearly with growth time. (c) Length of nanopillars increasing but saturating at a certain point with increasing growth time.

Thanks to this unique core-shell growth mode, nanopillar can maintain its high crystal quality while scaling lateral dimension of nanopillar up to micrometer size, unlimited by the critical diameter of nanowire. The underlying mechanism is revealed by high resolution TEM image shown in Figure 2-11. Figure 2-11(a) illustrates the configuration of InGaAs nanopillar TEM sample. It is important to notice that a polycrystalline InGaAs material is growing together with the InGaAs-core-GaAs-shell nanopillar. Albeit with bad crystal quality, this poly-InGaAs layer that wets the silicon surface actually plays an important role in forming superior nanopillar crystal quality. Figure 2-11(b) is the overall TEM image of the nanopillar specimen, showing a clear inversely-tapered root at the bottom of nanopillar. This is due to the formation of the poly-InGaAs layer with slower growth rate, which "wraps" around the bottom of nanopillar, as illustrated in Figure 2-9. With zoom-in TEM image Figure 2-11(c), this root has a contact footprint of 50nm on the silicon substrate with 45° taper angle. Stacking disorders and defects are present in the root region. Because the growth occurs only in the lateral direction, these defects terminated horizontally and do not propagate vertically. Hence, the crystal structure far from bottommost stabilizes into a single pure WZ phase, which is energetically favorable due to

a lower number of dangling bonds on the WZ sidewalls [58]. The TEM image Figure 2-11(c) in the nanopillar upper region shows no signs of any stacking disorders and defects. In addition, inverse tapering is crucial in stress relaxation. While the base diameter increases, the inverted-cone taper limits the footprint area to roughly 50nm, somewhat similar to the critical diameter observed in nanowires below which misfit strain can be relaxed elastically [48].

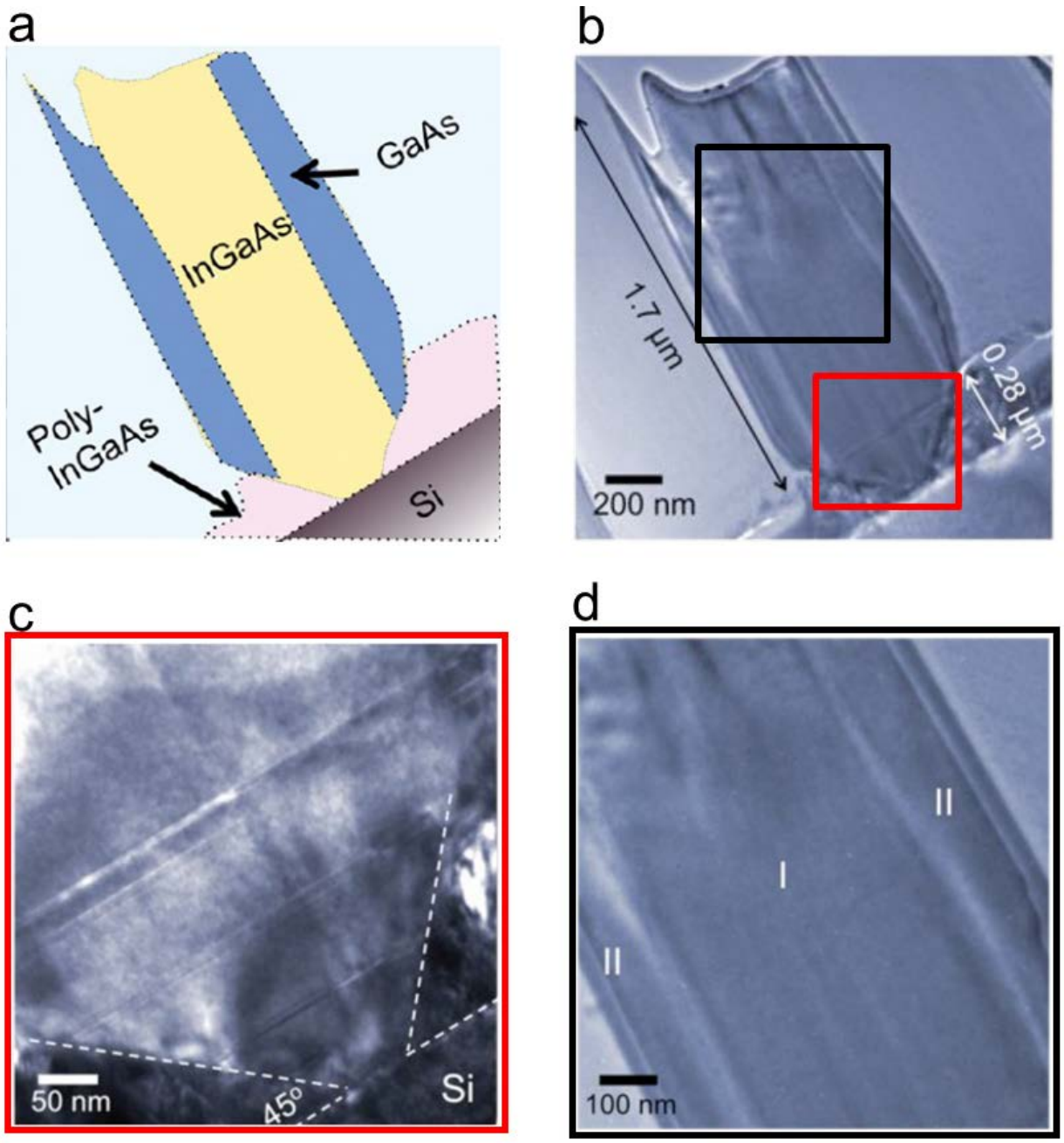


Figure 2-11 TEM images of InGaAs nanopillar. (a) Schematic of TEM sample. (b) Overall TEM image of InGaAs nanopillar. (d) Zoom-in TEM image of nanopillar root. (d) Zoom-in TEM image of nanopillar bulk region.

2.1.4 InGaAs nanopillar optical quality

To check the crystal quality of InGaAs nanopillar, photoluminescence experiment is carried out. Surprisingly, as-grown nanopillar on silicon substrate already demonstrates prominent lasing behavior under optical pumping at room temperature [59], which indicates its superior crystal quality. Figure 2-12 shows the PL spectra of InGaAs nanopillar emission below and above threshold. A prominent lasing mode appears at approximately 950nm above threshold. In the inset are both the L-L curve and the lasing linewidth narrowing curve, revealing a lasing threshold of ~93μJ/cm^{-2}.

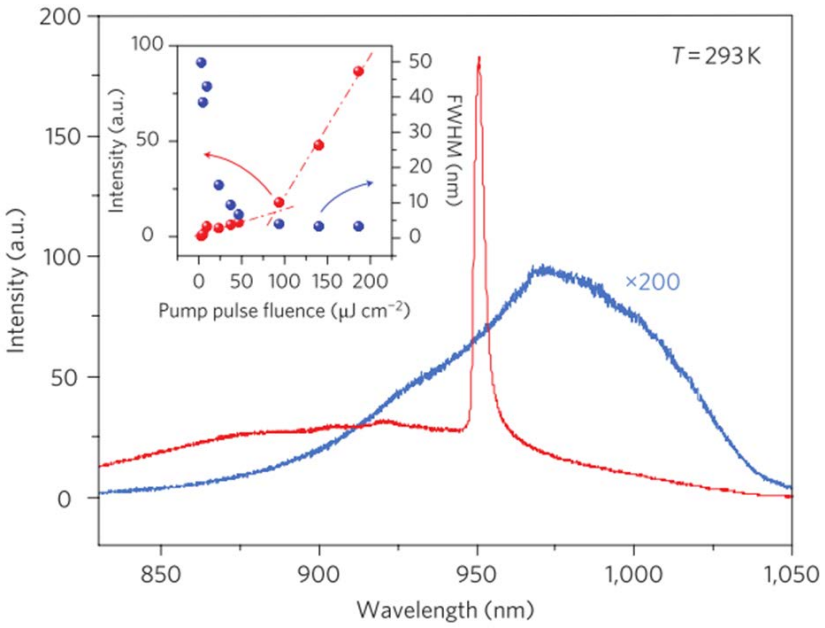


Figure 2-12 Photoluminescence spectra of nanopillar emission below and above lasing threshold at room temperature. The emission below threshold (blue curve) is amplified by 200 times for visibility. The inset shows the L-L curve and the linewidth narrowing above threshold.

The most intriguing aspect of our nanolaser is the optical cavity mode supported by as-grown nanopillar. It is a unique three-dimensional whispering gallery mode, intuitively illustrated in Figure 2-13(a). The mode field pattern is shown in Figure 2-13(b), based on finite-different time domain (FDTD) simulation. The cross sectional field pattern looks similar as conventional whispering gallery mode. However, our mode also has propagation constant along axial axis as well, causing the mode to thread along nanopillar. Both experimental lasing wavelength and emission pattern well match the simulation results of 3D whispering gallery mode [60]. Due to the mode threading propagation, the light hits the InGaAs/Si interface at a glancing angle, resulting in a strong reflection despite a small refractive index contrast between InGaAs and Si. This is why our nanopillar cavity can have high enough quality factor to support lasing behavior.

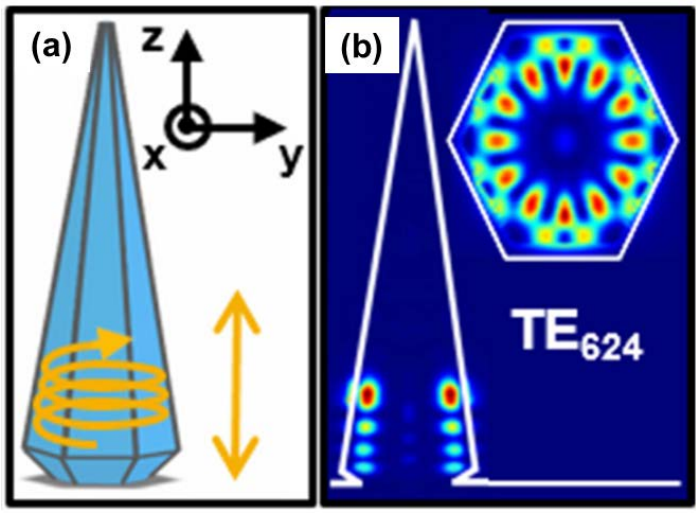


Figure 2-13 Three-dimensional whispering gallery mode. (a) Schematic illustrating mode propagation. (b) FDTD simulation of mode pattern.

2.2 InP nanopillar growth

InP-based III-V compounds are widely used in commercialized optoelectronic devices for silicon transparent applications. In addition, InP has a much lower surface recombination velocity than GaAs-based materials [61], [62] , which makes it a perfect candidate for solar cell application [63]. Hence, we expand our material category to InP nanoneedle/nanopillar using similar synthesis technique [52]. The sample preparation first used is also mechanical roughening, same as InGaAs nanopillar. The metal-organic reactants are trimethylindium (TMIn) and tertiarybutylphosphine (TBP), with a higher growth temperature of ~450°C in order to decompose TBP. We obtain the InP nanoneedle following the same core-shell growth mode, which is confirmed by growth time evolution experiment as in Figure 2-14. The InP nanoneedle is shown to be single crystalline wurtzite phase with superior crystal quality, confirmed by both high resolution TEM study and lasing oscillation behavior shown in Figure 2-15.

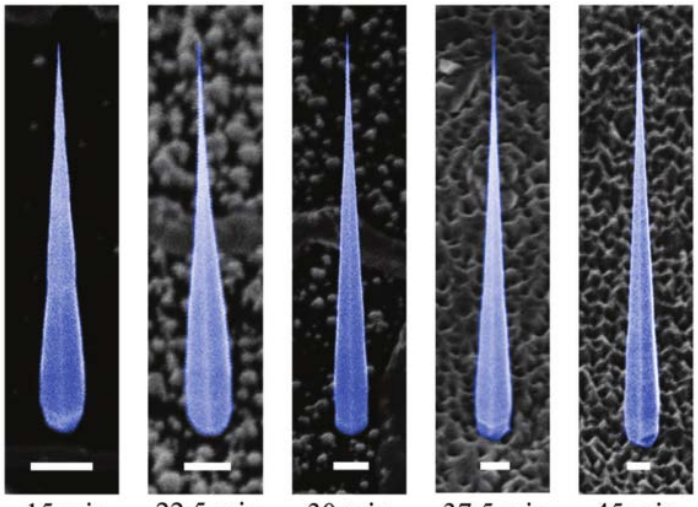


Figure 2-14 SEM images of InP nanoneedle with different growth time. The nanopillar size is kept the same while the scale bar in images is shrinking as growth time increases, confirming that nanoneedle size scales with time while maintaining shape.

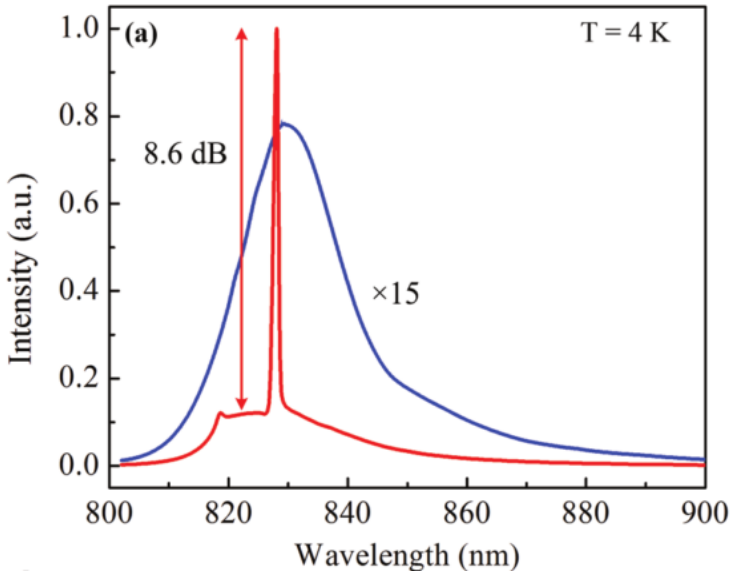


Figure 2-15 PL spectra of an InP nanopillar below (blue curve) and above (red curve) lasing threshold.

Inspired by nanopillar nucleation mechanism analysis performed in section 2.1.2, another more controllable sample preparation is invented to nucleate InP nanopillar. The sample preparation process is illustrated in Figure 2-16. The (111) silicon substrate is first covered by SiO_2 with plasma-enhance chemical vapor deposition (PECVD) technique. Some regions on the substrate are subsequently cleared of SiO_2 by photolithography and SiO_2 wet etching. Next, the sample is etched in tetramethylammonium hydroxide (TMAH) solution heated at 95°C for 5min. TMAH solution etched silicon (111) plane at a very slow rate, only forming a slightly roughened silicon surface. Finally, MOCVD growth is carried out and InP nanopillars grow on the roughened silicon surface.

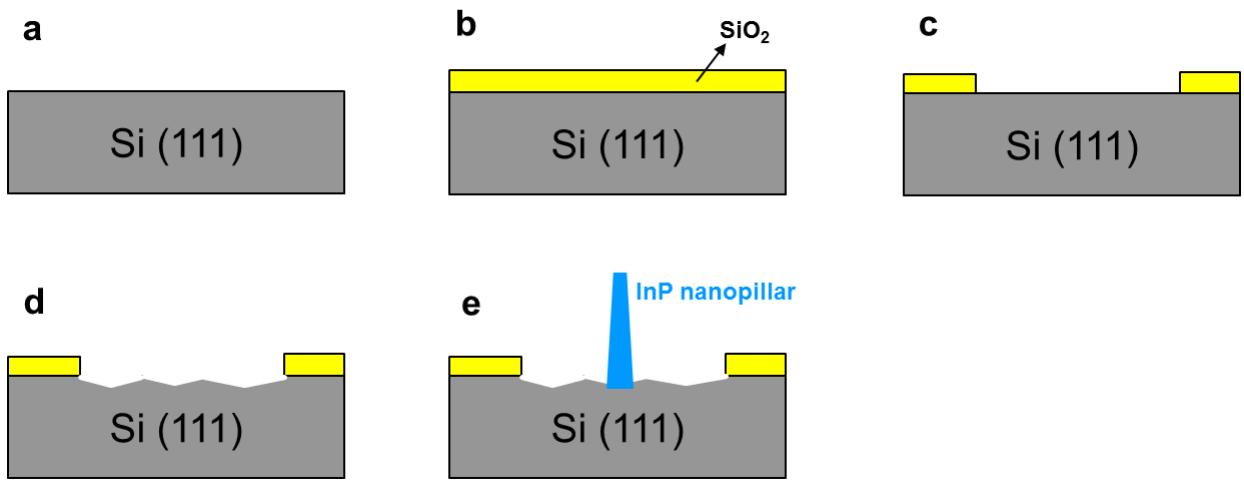


Figure 2-16 Sample preparation process for nucleating InP nanopillar. (a) Si (111) wafer as the growth substrate. (b) SiO_2 deposited by plasma-enhanced chemical vapor deposition. (c) Some regions are cleared of oxide by photolithography and buffered oxide etching. (d) Si surface chemically roughened by Tetramethylammonium hydroxide (TMAH) etching. (e) InP nanopillar growth on the roughened silicon surface.

The above sample preparation process creates both of the key elements for successful nanopillar nucleation: group III metal nanocluster and surface roughening. When indium source falls onto SiO_2, it has to form indium nanocluster because III-V crystal cannot nucleate on top of oxide. These indium nanoclusters diffuse to silicon surface which is chemically roughened by TMAH. They subsequently nucleate on silicon surface to form single crystalline InP seed. These indium nanoclusters are even observable after the growth. Figure 2-17 shows the top view SEM image at the boundary of Si and SiO_2 after nanopillar growth. InP nanopillars grow on Si surface, together with some polycrystalline InP islands with poorer crystal quality. More interestingly, there are a large number of ball-shape clusters present on top of SiO_2 surface. We suspect that these are indium balls because metal prefers to form ball-shape cluster on SiO_2. Energy-dispersive X-ray spectroscopy (EDS) technique is utilized to determine the composition of these ball-shape clusters. As a control experiment, EDS is first probed on the polycrystalline InP island. As shown in Figure 2-18(a), both indium peak and phosphorus peak are observed. However, when EDS is performed on the ball-shape nanoclusters on top of SiO_2, only indium peak is present, as shown in Figure 2-18(b). This convincingly proves that these nanoclusters are pure indium balls, which is consistent with our nucleation hypothesis.

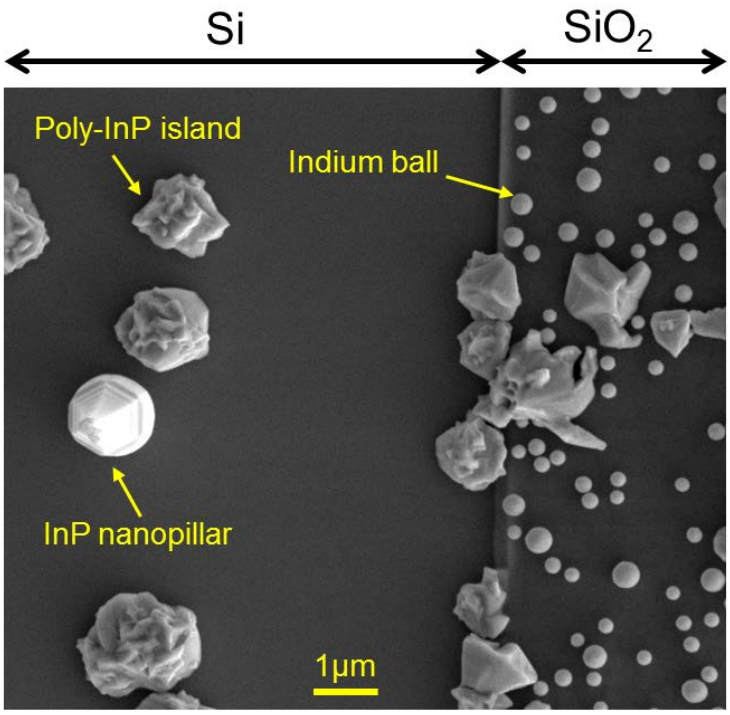
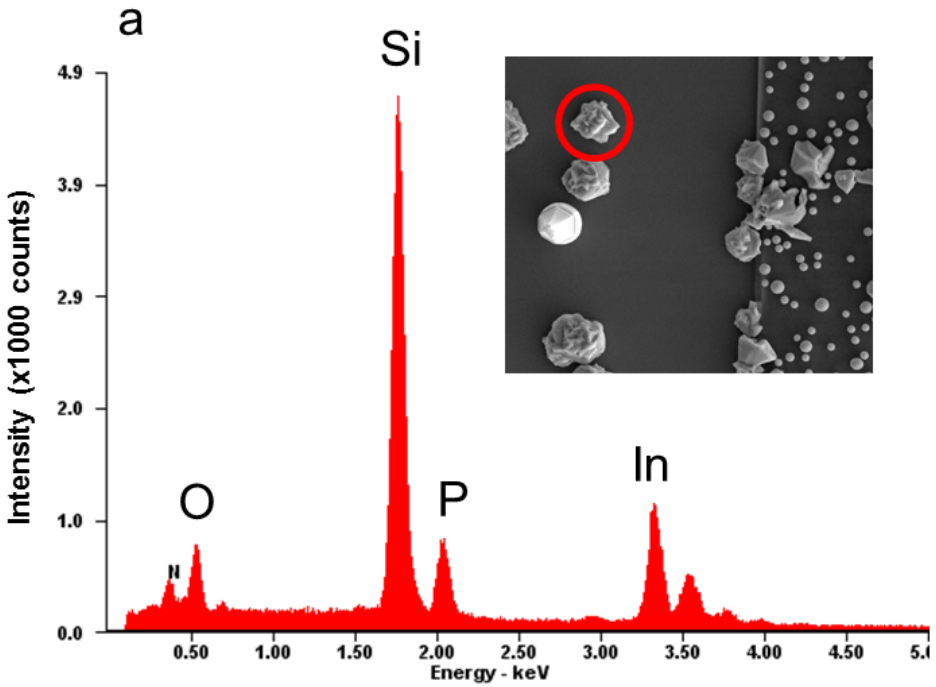


Figure 2-17 Top view SEM image of both Si region and SiO_2 region after nanopillar growth. InP nanopillars grow on top of Si region, whereas many indium nanoclusters are present on top of SiO_2 region.



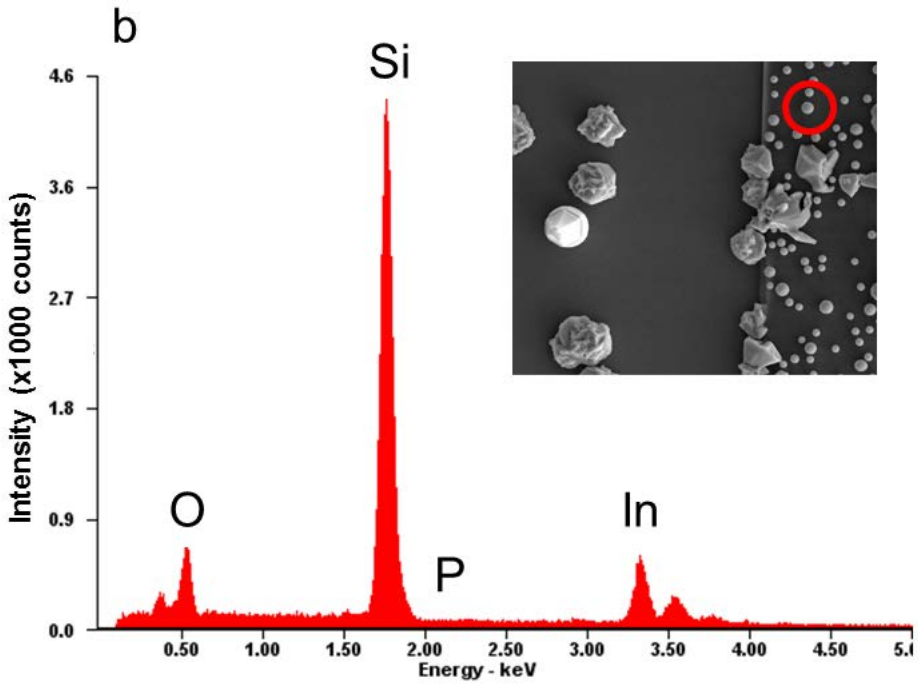
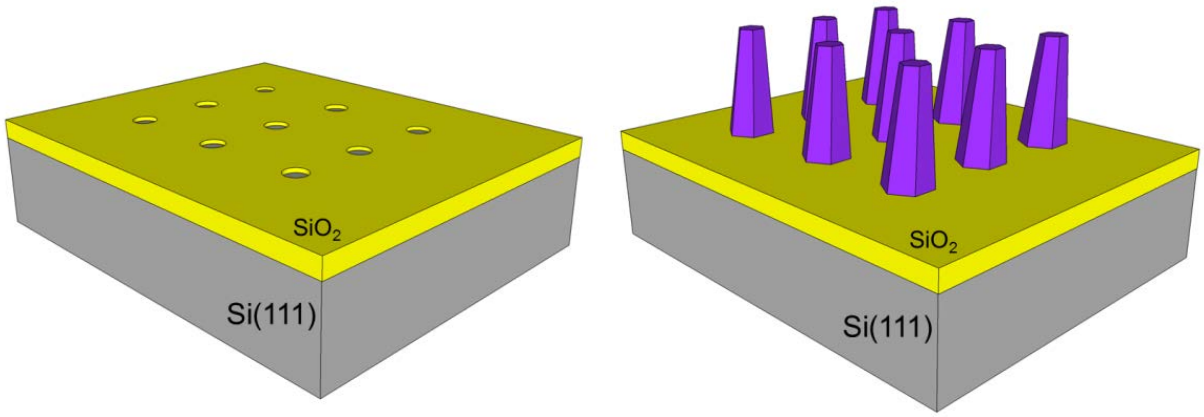


Figure 2-18 Energy-dispersive X-ray spectroscopy (EDS) results to analyze elemental composition. (a) Probe on poly-InP island. (b) Probe on ball-shape nanocluster on SiO2 surface

2.3 Nanopillar growth site control

As shown in Figure 2-6, nanopillar growth sites are random for spontaneous growth. This is not at all desirable for device fabrication or mass production. In order to control the growth site, a common approach is to use patterned substrates, as illustrated in Figure 2-19. The working principle is that by selectively etching openings on the SiO_2 or SiN_x mask, nanostructure nucleation will only occur inside the opening where Si is exposed. In this way, nanopillar growth sites are pre-defined. This method has been used extensively to create arrayed nanowires, also known as selective area growth [46]. However, selective area growth is usually very sensitive to growth condition (V/III ratio and temperature), as well as substrate pattern (period, opening size, opening shape). Although various growth conditions and patterns have been experimented, we have difficulty finding good condition for InGaAs nanopillar selective area growth. Nevertheless, with InP nanopillar, it is relative easy to find a good condition to obtain preliminary selective area growth result, probably due to the fact that indium atoms have large surface affinity contrast between on Si and on SiO_2.

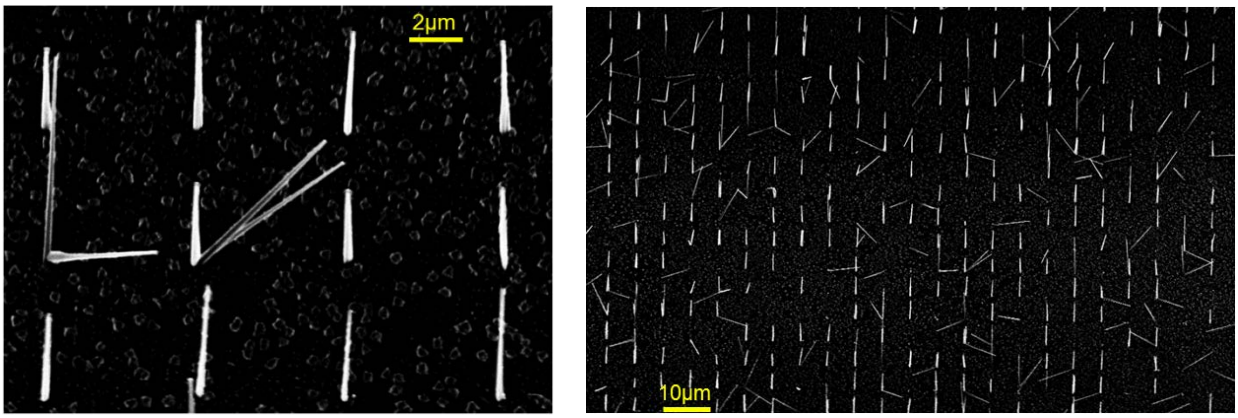


(a) (b)

Figure 2-19 Schematic of selective area nanopillar growth. (a) patterned Si(111) substrate before growth. (b) site-controlled nanopillar array after growth. The purple color tapered pillars respresent III-V nanopillars.

The SiO_2 mask thickness is approximately 100nm, deposited by plasma-enhanced chemical vapor deposition. The patterns are generated by deep-ultraviolet lithography, followed by buffered oxide etch. To find the optimum pattern parameters, the basic patterns are an array of circular openings with different opening diameters and different spacings (or periods). The opening diameter varies from 240nm to 400nm with 20nm increment, whereas the spacings are designed as 0.8μm, 1μm, 3μm, 6μm, 10μm, 20μm, 50μm. The sample is subsequently put into MOCVD growth chamber for InP nanopillar synthesis.

Figure 2-20 is a 30 degree tilt view SEM image of a typical site-controlled growth result. Under this perspective, each vertical InP nanopillar along Si (111) direction is a vertical line with bright color. Figure 2-20(a) shows a 3-by-4 array of openings with 380nm opening size and 6μm spacing. No nanopillars are grown on top of SiO_2 region, attesting to superior selectiveness of this growth. Moreover, each of almost all openings only has one vertical nanopillar in it. But some openings do have some slanted nanopillars inside. This is due to the multiple degenerate Si {111} directions that InP nanopillar could grow along. Figure 2-20(b) is the zoom-out view of a larger array, where an array of vertical nanopilars is observed with limited number of openings without any nanopillars grown.



(a) (b)

Figure 2-20 30° tilt view SEM image of a typical site-controlled growth result. (a) zoom-in image; (b) zoom-out image.

From the growth perspective, it is intriguing to see how nanopillar evolves for site-controlled growth. Hence, TEM image is taken to unveil the secret at the bottom of site-controlled InP nanopillar, as shown in Figure 2-21. It is clear that nanopillar fills up the SiO_2 opening and grows outside the opening in a core-shell manner. Even on top of SiO_2, InP nanopillar still has wurtzite crystal phase with high crystal quality due to the lateral growth.

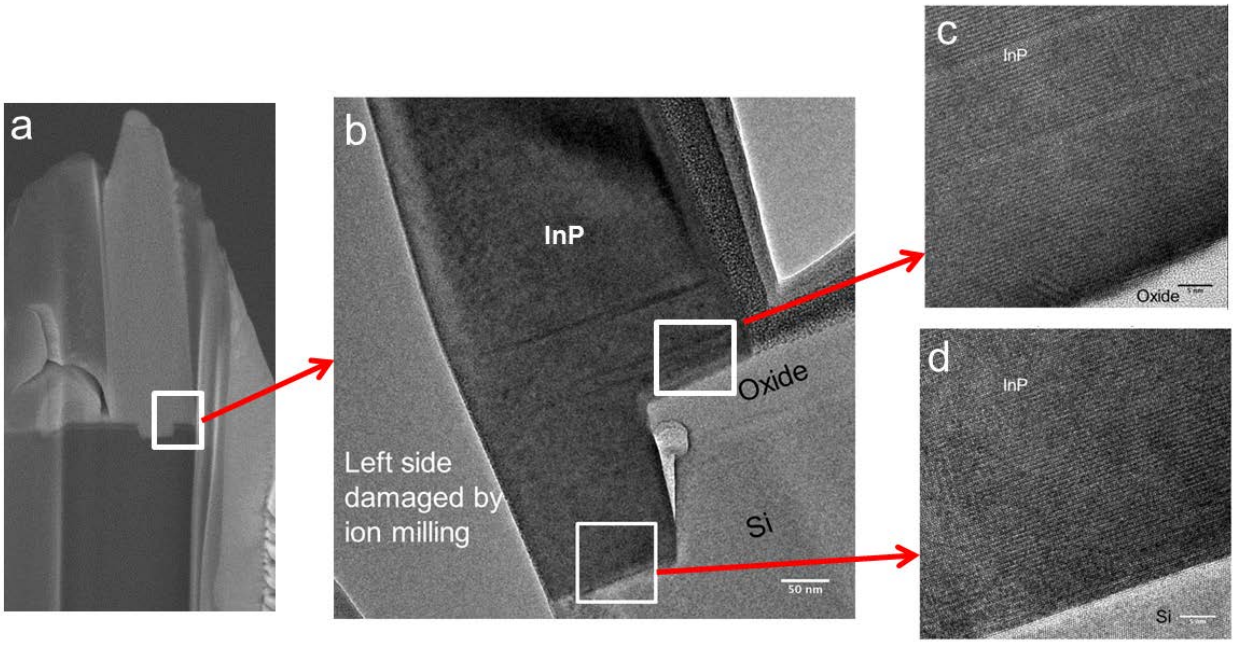


Figure 2-21 TEM image of site-controlled InP nanopillar by SiO_2 pattern. (a) Zoom out view of TEM. (b) Zoom in view of the root of InP nanopillar. (c) Interface between InP and SiO_2. (d) Interface between InP and Si.

One key metric to evaluate the efficacy of site-controlled growth is the yield of growth. We define the "site control yield" as the number of vertical nanopillars divided by the number of

openings. In SEM image Figure 2-22 with an array of 400 openings, 262 upright nanopillars are counted in total, thus giving a yield of 66%. Further optimization of growth condition can be performed to boost this site control yield.

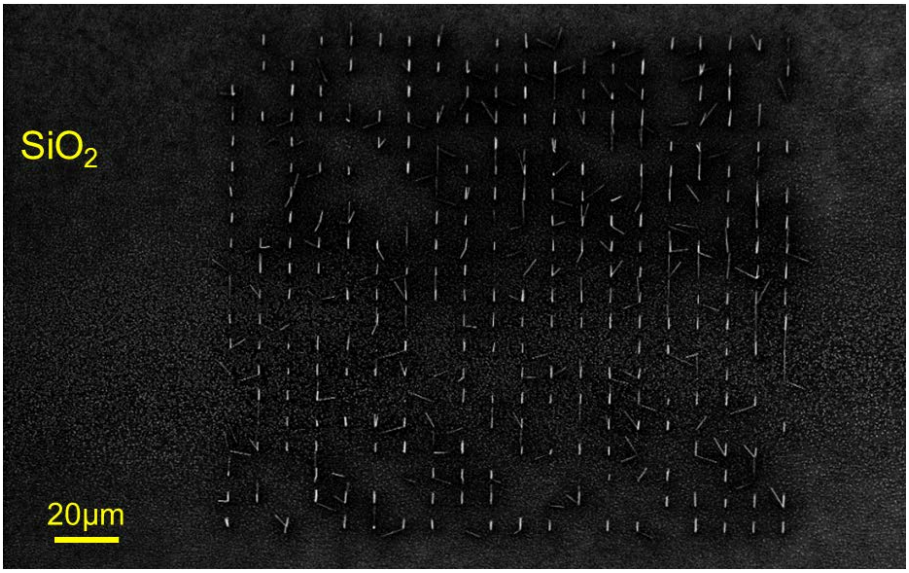
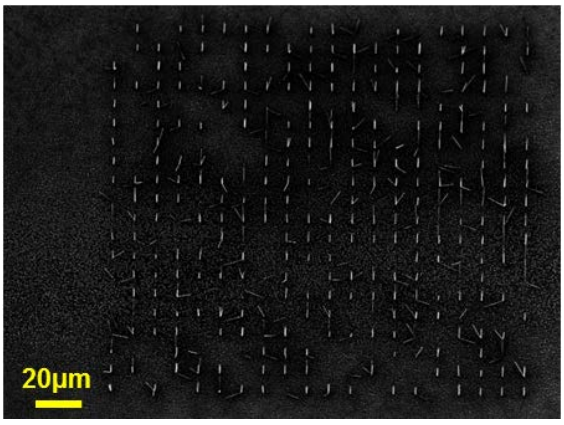
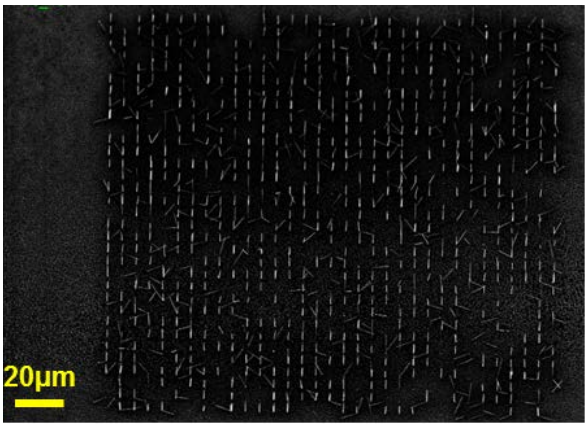


Figure 2-22 SEM image of one 20x20 array of site-controlled InP nanopillars to calculate the site control yield.

The effect of spacing on the site control growth is also studied by looking at patterns with different spacings, as shown in Figure 2-23(a-d). As the spacing decreases from 10μm to 1μm, the site-controlled growth results maintain high selectivity, while the site control yield drops a little. However, the density of nanopillars is greatly enhanced because of dense-packing of openings with smaller spacing. For the purpose of practical application, large spacing patterns will be ideal for making an array of single pillar devices, like laser diodes or photodetectors, whereas small spacing patterns are desired for high density optoelectronics application, such as III-V nanostructure photovoltaics.



(a)



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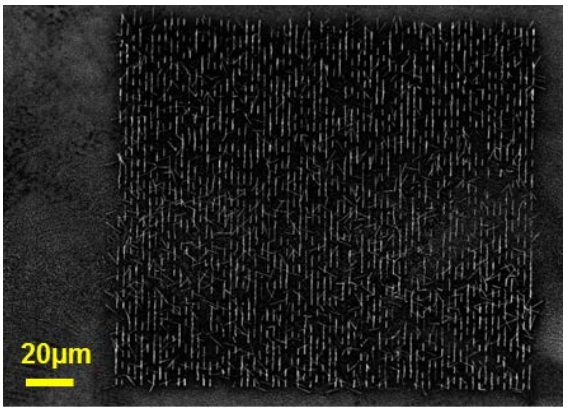

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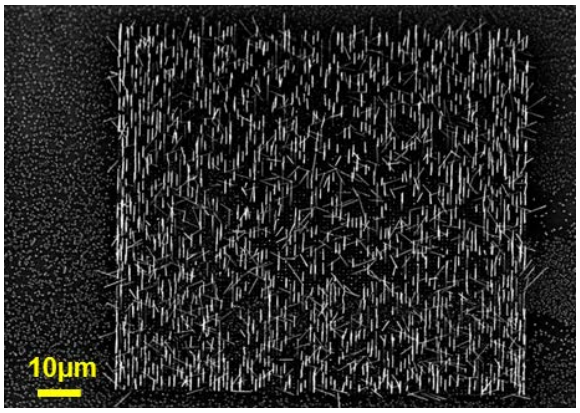
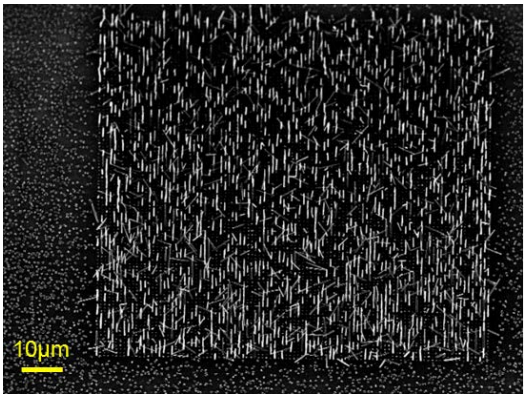


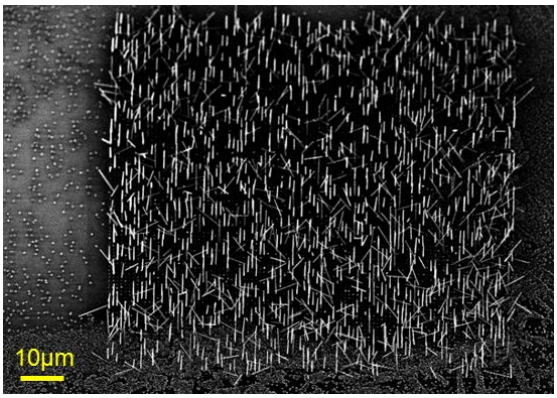
(d)

Figure 2-23 SEM images of site-controlled growth results for different opening spacing. (a) 10um spacing; (b) 6um spacing; (c) 3um spacing; (d) 1um spacing.

In addition, pattern opening size is shown to be a critical parameter for site-controlled growth, based on the results in Figure 2-24. Figure 2-24(a-c) are the figures with the same spacing, but with different opening sizes of 300nm, 280nm, 260nm, respectively. It is prominent that when the opening size falls below a critical value (280nm in this situation), the density of needles drop dramatically.



(a)



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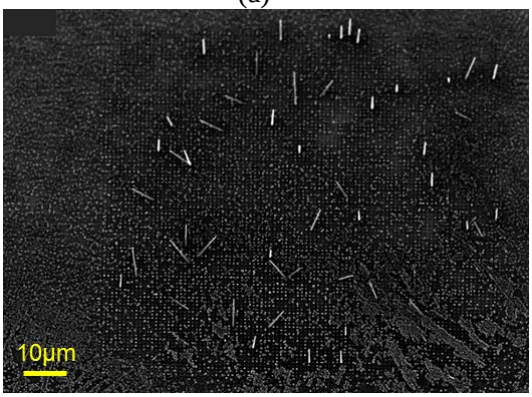

(c)

Figure 2-24 SEM images of site-controlled growth results for different opening size. (a) 300nm opening size; (b) 280nm opening size; (c) 260nm opening size

2.4 Summary

In this chapter, we first motivate our work by analyzing all the state-or-art strategies of integrating III-V material with silicon and point out the advantages of our "III-V nanopillar on silicon" method: (1) superior crystal quality; (2) low growth temperature; (3) no metal catalyst. All these unique attributes are highly desirable to create practical nanolasers with CMOS compatibility.

Based on experimental observations, a hypothesis is made about nanopillar nucleation. We believe there are two key elements contributing to nanopillar nucleation: metal nanocluster and surface roughness. Metal nanoclusters are formed due to surface oxide and then diffuse to silicon regions where surface roughness "traps" clusters and form III-V nucleation seed. Two sample preparation methods, both mechanical roughening and chemical roughening, agrees well with this hypothesis and successfully nucleates high density of InGaAs and InP nanopillars.

Following the nucleation, nanopillar growth occurs in a core-shell manner. Hence, dislocations are only contained at the inversely-tapered root and the top part of nanopillar has no defect. The superior crystal quality is confirmed by as-grown nanopillar's lasing behavior under optical pumping at room temperature. A unique 3D whispering gallery mode is also discovered to enhance the bottom reflection at the InGaAs/Si interface in spite of little refractive index contrast. InP nanopillars are also grown with high optical quality, following the same scalable core-shell growth mechanism.

Finally, nanopillar growth site control is achieved by patterning Si substrate with SiO2 mask. Nanopillars only grow in the SiO2 openings and a 66% site control yield has been obtained. Further growth optimization is needed to further understand the growth and increase site control yield.

Chapter 3 Nanopillar Laser Integration with CMOS Electronics

Optical interconnect requires that laser can be placed onto CMOS chip without affecting its electrical performance. Our nanopillar laser inherently has the potential to integrate with CMOS electronics in a back-end-of-line (BEOL) manner. First, our nanopillar growth is free of gold-catalyst, compared to traditional VLS nanowire growth. This avoids the contamination of gold as deep level trap for silicon transistors. Second, our nanopillar growth temperature is only 410ºC, well within the thermal budget for BEOL processing [39], ruling out the possibility of dopants over-diffusion in transistors. To experimentally demonstrate the CMOS-compatibility, we investigate the influence of InGaAs nanopillar growth on the performance of (100)-silicon-based functional metal-oxide-semiconductor field effect transistors (MOSFETs) [55].

3.1 Nanopillar growth on MOSFETs

Our experiments start with a standard (100)-silicon wafer consisting of n-channel MOSFETs with various gate lengths and widths. The transistor chip is product of an undergraduate micro-fabrication course at Berkeley, using relatively older generation of fabrication process such as ultra-violet light photolithography, thermal oxidation and thermal diffusion. The process flow of transistor fabrication is shown in Figure 3-1 but the fabrication details are out of this dissertation's scope. As the end result, the transistor has SiO_2 as the gate dielectric material, doped poly-silicon as the gate material, and aluminum as the metal contact. Needless to say, they are not state-of-art transistors, but still suffice to serve as a proof of concept to demonstrate CMOS-compatibility.

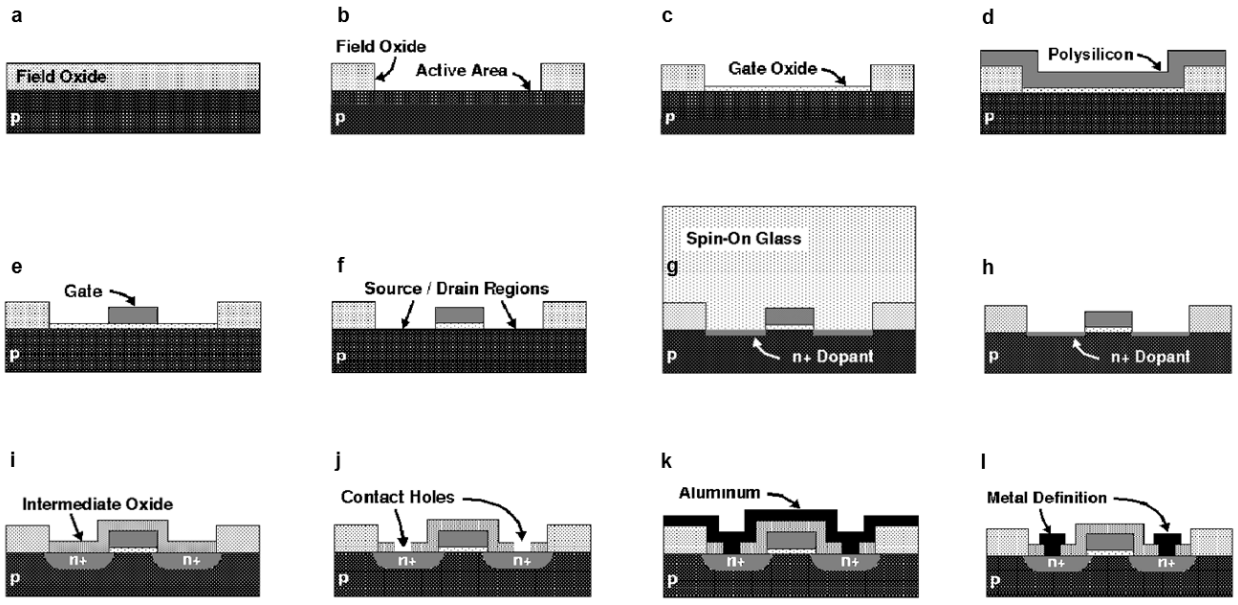

Figure 3-1 Fabrication process flow of n-channel MOSFET. (a) Field oxide layer formation by thermal oxidation. (b) Defining active area by photolithography. (c) Gate oxide formation by thermal oxidation. (d) Poly-silicon deposition. (e) Defining gate

region by photolithography and etching. (f) Clear source and drain region gate oxide by buffered oxide etching. (g) and (h) Source and drain region doping by spinning on dopants-containing spin-on glass and thermal drive-in process. (i) Intermediate oxide formation by thermal oxidation. (j) Defining contact holes by photolithography and etching. (k) Metal contact formation by aluminum thermal evaporation. (l) Metal definition by photolithography and etching. Metal contacts are also annealed after definition.

After the MOSFETs were fabricated, they were fully characterized before nanopillar growth for comparison. A parameter analyzer was used to measure the I_{ds}-V_{gs} and I_{ds}-V_{ds} curves of the transistors. Threshold voltage was extracted from these I-V curves by the second derivative method.

The aluminum metal contacts were subsequently removed from the MOSFETs by wet chemical etching (80% phosphoric acid, 5% acetic acid, 5% nitric acid and 10% water at an elevated temperature of 50 ºC), exposing the gate and source/drain regions of the transistors. The gate region consists of n-type doped polycrystalline silicon, while the source/drain region is made of n-type doped (100)-silicon. A 100-nm-thick silicon dioxide layer was then deposited onto part of the wafer to protect selected MOSFETs from III-V material deposition for the purposes of after-growth MOSFET fabrication. The SiO_2 deposition was done by plasma-enhanced chemical vapor deposition at 350 ºC under a pressure of 0.9 Torr and at 25W radio frequency power, with a gas flow of 100 sccm silane, 100 sccm argon and 800 sccm nitrous oxide.

Afterwards, the wafer was loaded into the MOCVD chamber for nanopillar growth. The growth condition here is similar as that discussed in Chapter 2. On the oxide-protected part, III-V materials were removed using diluted piranha solution (sulfuric acid:hydrogen peroxide:water=1:8:40). Next, contact holes were defined by photolithography. Aluminum was sputtered onto the chip with 300 W DC power and 5 mTorr pressure. Next, lithography and aluminum etching were used to define the new aluminum contacts. Finally, the metal contacts went through rapid thermal annealing at 350 ºC for 30 seconds in a nitrogen environment. The fabrication process flow is summarized in Figure 3-2.

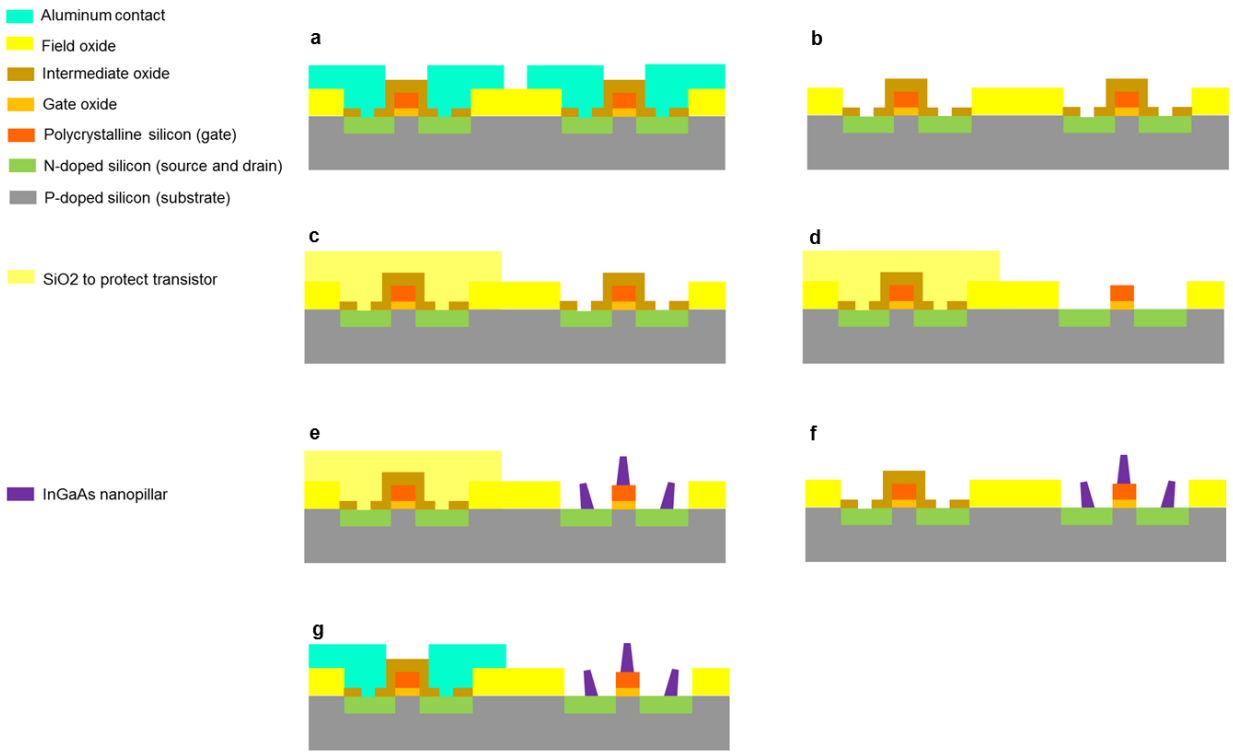

Figure 3-2 Fabrication process flow of integrating InGaAs nanopillars onto transistor chip. (a) Cross-section schematic of fabricated transistor chip with two transistors depicted to demonstrate integration process. The right-hand-side transistor will be used to grow InGaAs nanopillar, whereas the left one will be characterized to see transistor performance before and after nanopillar growth. (b) Removing aluminum metal contacts by wet etching with aluminum etchant (80% phosphoric acid, 5% acetic acid, 5% nitric acid and 10% water). (c) Covering selected transistors with SiO2 to avoid III-V material deposition. (d) Removing intermediate oxide of other transistors to fully expose gate, source and drain regions. (e) Growth of InGaAs-core-GaAs-shell nanopillar by MOCVD on transistors. (f) Removing protection SiO2. (g) Defining new aluminum contacts with lithography and metal etching.

Figure 3-3 shows a schematic illustrating the nanopillars grown on a MOSFET. Figure 3-4(a) and 3-4(b) show scanning electron microscope (SEM) images of InGaAs/GaAs core-shell nanopillars grown on both the gate region and the source/drain region of the transistor. The nanopilar consists of a 630-nm-diameter InGaAs core as the active region, surrounded by a 110-nm-thick GaAs shell layer serving as a surface passivation layer. The structure and growth method are similar to those on (111)-silicon reported in [59]. What is new and most extraordinary here is the fact that micron-sized pillars are grown on polycrystalline silicon with the same core-shell structure, tapered hexagonal pillar shape, growth rate and wurzite crystalline phase. The detailed discussion about nanopillar growth and material characterization is in reference [54].

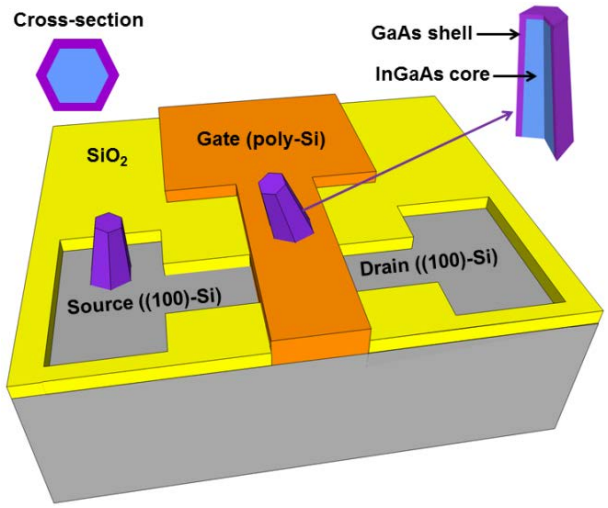

Figure 3-3 Schematic of nanopillars grown on a MOSFET. Each nanopillar has a tapered hexagonal shape and consists of an InGaAs core and a GaAs shell. The nanopillars grow on both the gate and source/drain regions with a random orientation. The gate region consists of n-type doped polycrystalline silicon, while the source/drain region is made of n-type doped (100)-silicon.

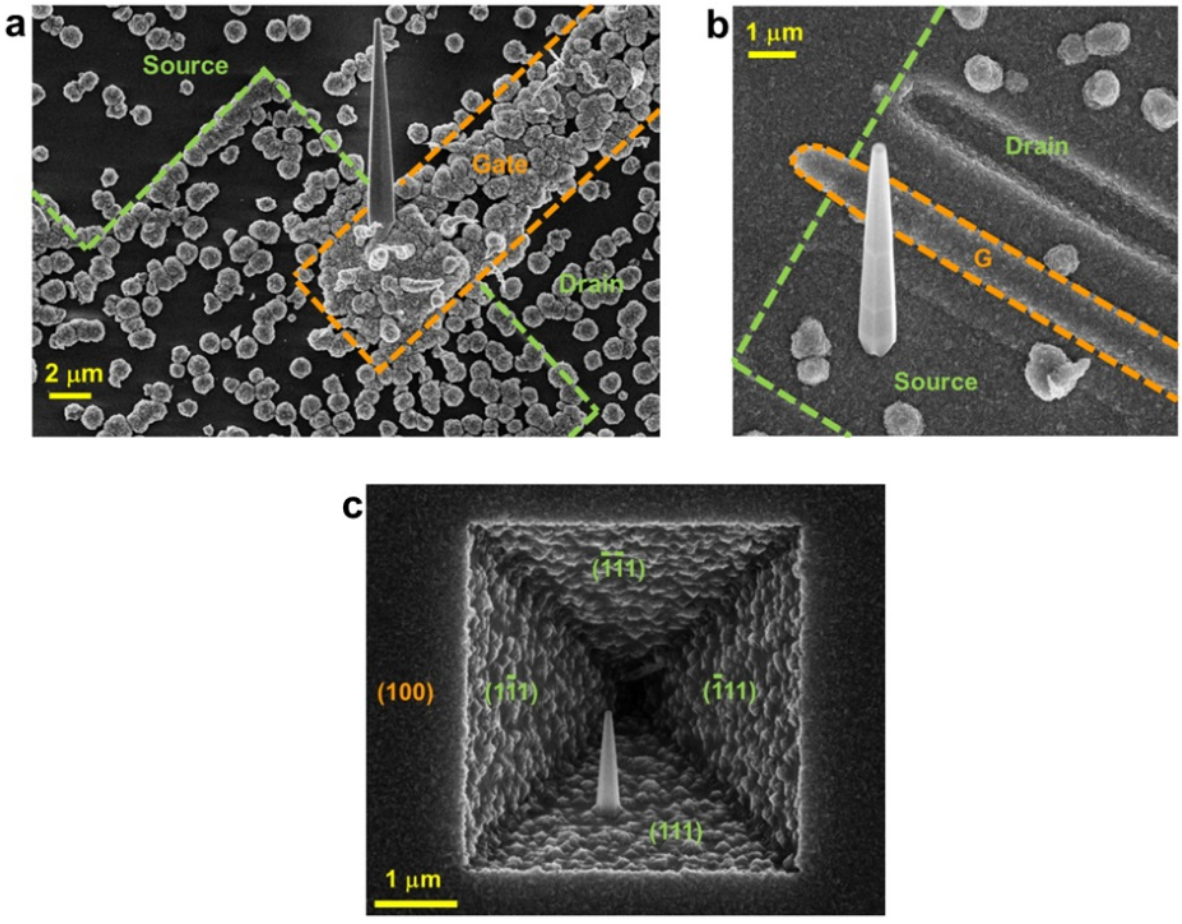

Figure 3-4 SEM images of nanopillar growth. (a) The nanopillar grown on gate region (labeled Gate) of a MOSFET. (b) The nanopillar grown on source region of a MOSFET (gate region is labeled G). (c) The nanopillar grown inside an inverted pyramid on a (100)-silicon substrate. The pyramid, with four degenerate silicon (111) planes, is created by silicon anisotropic etching with tetramethylammonium hydroxide.

The orientation of nanopillars on the gate region is random, due to multiple grain orientations inside the polycrystalline silicon. The surface of the (100)-silicon is somewhat rough as a result of the fact that the metal contacts had been annealed and then etched. As such, nanopillars on the source/drain region do not align in any particular direction. For future optimization, the metal deposition/annealing/etch step will not need to be part of the heterogeneous integration process. Under such circumstances, the nanopillars are expected to grow along the [111] crystal direction of silicon, and it will be possible to precisely control the nanopillar growth orientation on (100)-silicon substrates. As an example, we etched part of the (100)-silicon substrate to expose silicon (111) planes using an anisotropic silicon etchant (tetramethylammonium hydroxide). We show that nanopillars can grow on silicon (111) planes with a predetermined orientation. As shown in the SEM image in Figure 3-4(c), a nanopillar is grown inside an inverted pyramid comprised of four degenerate silicon (111) planes, exactly following the [111] crystal direction of silicon.

It is critical to point out that nanopillar does not necessarily need to be right on top of transistor in the actual laser-transistor integration. Nanolaser just needs to be on the transistor chip to serve as the on-chip light source. Nevertheless, the proof-of-principle experiment here directly positions nanopillars on gate/source/drain regions of transistors to provide a straight-forward and convincing demonstration.

3.2 Nanopillar lasing characteristics

The superior quality of the nanopillars grown on polysilicon or the source/drain (100)-silicon is attested by the laser performance metrics. Lasing is achieved using an optical pump (120-femtosecond titanium:sapphire pulses at a wavelength of 765 nm) at room temperature. Figure 3-5(a) shows the laser output power as a function of pump power (L-L curve) for a typical nanopillar laser. The clear S-shape curve is a standard signature of lasing. The threshold power of 600 μW indicated at the kink of S-shape curve corresponds to a power density of 5.8kW/cm^2. An average output power of 0.5 μW or pulsed peak power of 573 μW is achieved. The spectra below and above threshold are shown in Figure 3-5(b) with the lasing wavelength at around 980 nm (1.26 eV) and a side-mode suppression ratio of approximately 13 dB. Moreover, nanopillar emission patterns below and above lasing threshold shown in Figure 3-5(c) demonstrates clear speckle patterns after nanopillar climbs over lasing threshold. Combining all the evidences, we are confident to claim that high quality nanopillar lasers can be grown on MOSFET chips using our unique MOCVD growth.

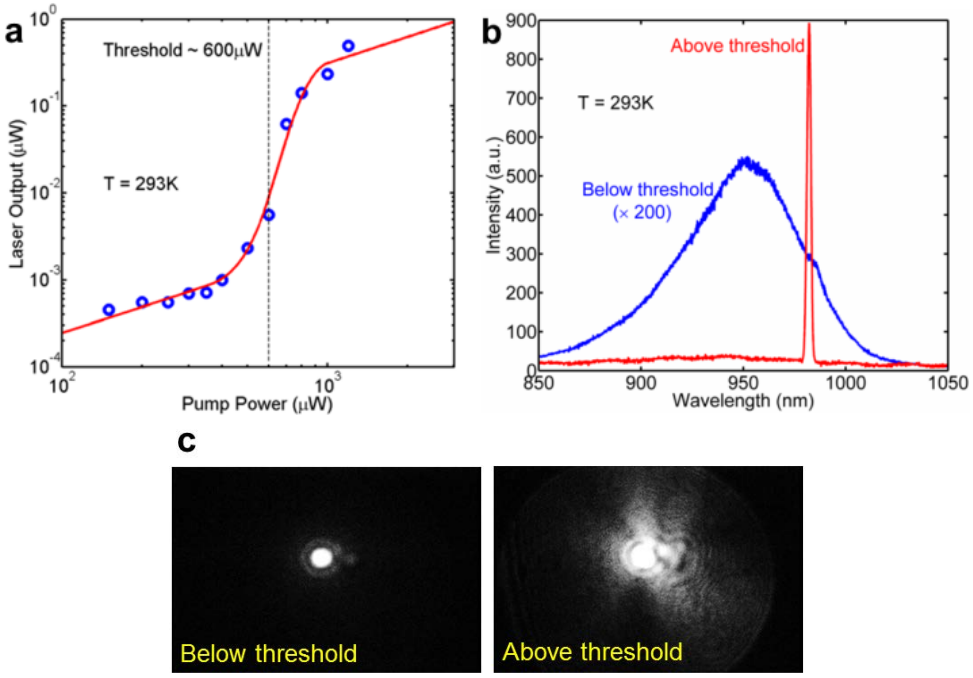

Figure 3-5 Nanopillar laser oscillation. (a) L-L curve of a nanopillar laser at room temperature. The blue circles are experimental data, while the red curve is the S-shape fit. The threshold pump power is approximately 600 μW. (b) Room-temperature nanopillar emission below (blue) and above (red) threshold. For visibility, the emission below threshold is magnified by 200 times. The side mode suppression ratio of the lasing peak is about 13 dB. (c) Near field images of nanopillar emission below and above lasing threshold.

3.3 MOSFET performance before and after nanopillar growth

The characterization of the MOSFET before and after nanopillar growth demonstrates that the growth has almost no adverse effect on the MOSFET performance. Figure 3-6(a) and 3-6(b) show typical transfer characteristics and output characteristics of a transistor before and after the nanopillar laser growth. Both I-V curves show minimal changes due to the MOCVD growth. Even after the growth, the transistor exhibits a respectable on/off current ratio of 47 dB, a subthreshold swing of approximately 140 mV per decade, and a maximum transconductance of 200 μS at a V_{ds} of 2.5 V. Systematic measurement shows that 59 out of 60 transistors offer near-constant performance after growth, resulting in a high yield of 98.3%. Statistical analysis has also been carried out on 50 transistors with the same annealing condition. Figure 3-6(c) shows a histogram plot of transistor threshold voltage before (dark dashed line) and after (red solid line) the nanopillar growth. On average, the threshold voltage only shifts by 3.0% after nanopillar growth.

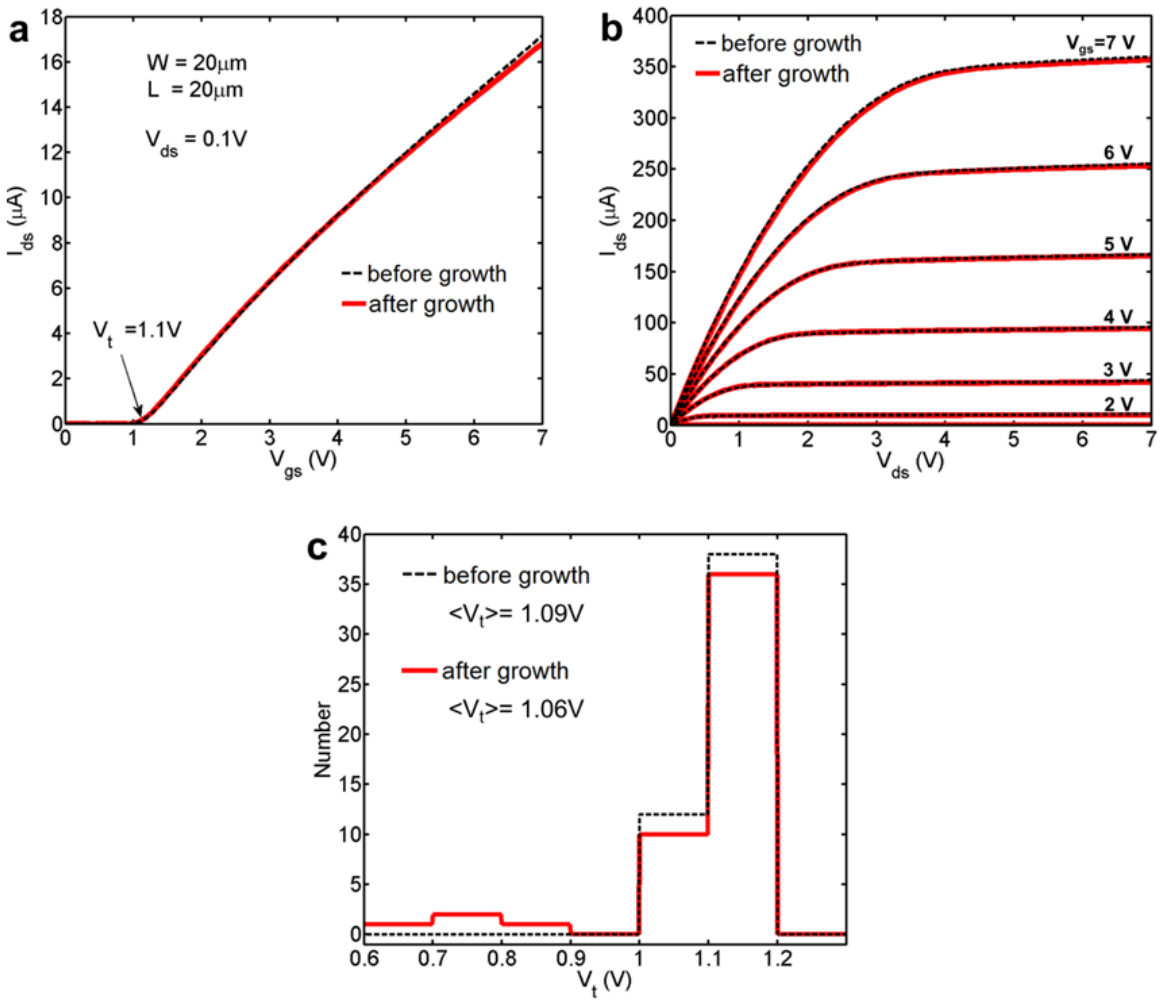

Figure 3-6 Transistor performance before and after nanopillar laser growth. (a) Transfer characteristics of a transistor (gate width 20 μm, gate length 20 μm) before and after nanopillar growth. V_{gs} represents the voltage between gate and source region, and Ids represents the current flowing from drain region to source region. At V_{ds} = 0.1 V, the threshold voltage is about 1.1 V. (b) Output characteristics of the same transistor before and after nanopillar growth. V_{ds} represents the voltage between drain and source region. (c) Histogram plots of the transistor threshold voltage before (dark dashed line) and after (red solid line) nanopillar growth for a sample of 50 different transistors. The average threshold voltage before growth is 1.09 V, while the average threshold voltage after growth is 1.06 V.

3.4 Summary

In summary, using a unique low-temperature and catalyst-free nanopillar growth technique, we demonstrate the first nanolasers monolithically grown on silicon-based MOSFETs. Excellent lasing performance is obtained at room temperature. The group III-V nanopillar growth process has minimal impact on the performance of the transistors, and shows great promise as a CMOS-compatible growth method. This work paves the way for the heterogeneous integration of

nanophotonics, in particular lasers, directly onto silicon wafers that consist of nearly completed electronic circuits.

Chapter 4 Nanopillar Laser Integration with Silicon Photonics

Optical interconnects require not only lasers as enabling devices, but also integration into silicon photonic circuitry with high coupling efficiency. Thanks to its growth direction preference along <111> silicon direction, our nanopillar laser offers a promising laser-waveguide integration configuration on Si(110) substrate. In this chapter, we will discuss how we take advantage of nanopillar growth orientation to integrate nanopillar lasers with silicon waveguides in an end-fire coupling manner. Horizontal nanopillar based novel cavity resonator designs are also discussed.

4.1 Nanopillar growth orientation

As mentioned in earlier chapters, our nanopillars have a preferential growth direction along <111> crystal direction of silicon, due to their unique pure wurtzite crystal structure. Thus, nanopillars grow vertically on (111)-silicon substrates. On (100)-silicon substrates, anisotropic silicon etchant, such as tetramethylammonium hydroxide (TMAH), can be used to create {111} silicon crystal planes. TMAH has a significantly slower etching rate along Si <111> directions than other crystal directions; as a result, TMAH etching stops at {111} Si planes and forms four possible degenerate {111} Si planes, depending on etching mask patterns. Thereafter, nanopillars grow on these {111} Si planes and thus have a fixed slanted angle of approximately 54.7º. More interestingly, vertical (1-11) Si plane can be created on Si (110) substrates with the same anisotropic Si etching. Subsequent III-V growth results in horizontal nanopillars. Figure 4-1 summarizes the configurations of nanopillar growth on different orientation silicon substrates -- Si(111), Si(100), and Si(110). Top view SEM images of nanopillar growth on different substrates are also shown respectively.

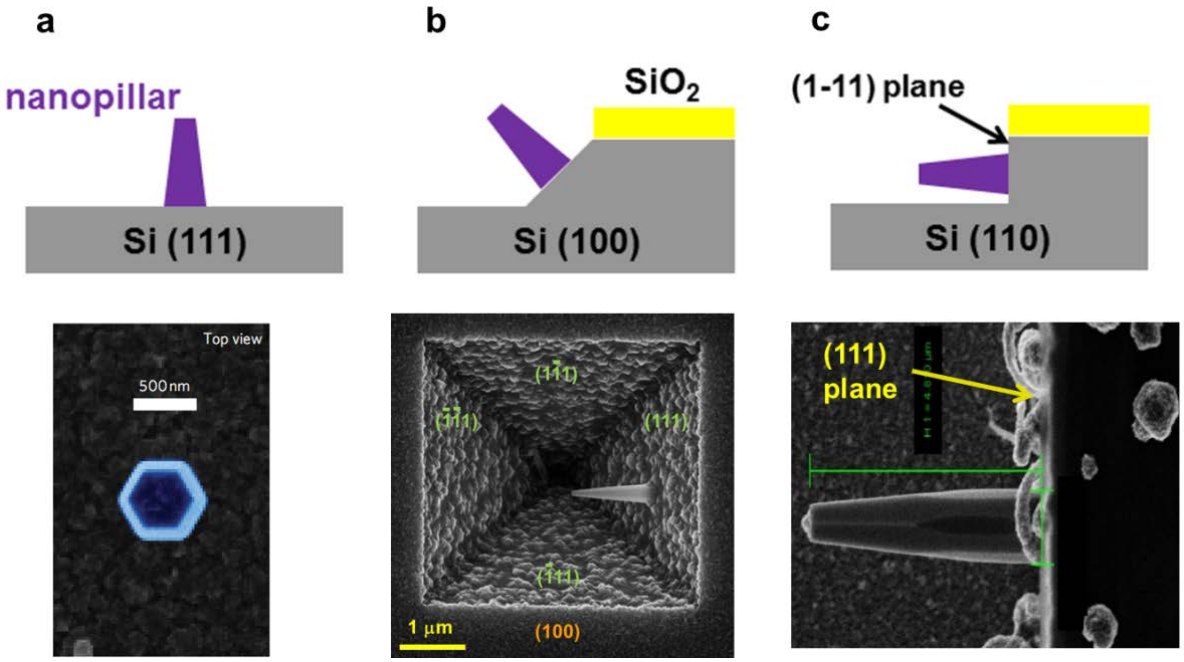

Figure 4-1 Schematics and top view SEM images of nanopillar growth on different Si substrates (a) vertical nanopillar on Si(111) substrate; (b) slanted nanopillar on Si(100) substrate; (c) horizontal naonpillar on Si(110) substrate.

Nanopillars with different orientations enable us to observe light emission from different perspectives. For instance, horizontal nanopillar emission exhibits emission pattern from the bottom of nanopillar otherwise unobservable with vertical nanopillars. Figure 4-2 shows the FDTD simulation of nanopillar emission, as well as the experimental emission image from a horizontal nanopillar. The emission from the bottom of nanopillar is very significant, inspiring us to utilize horizontal nanopilars for silicon waveguide integration as discussed in the following section.

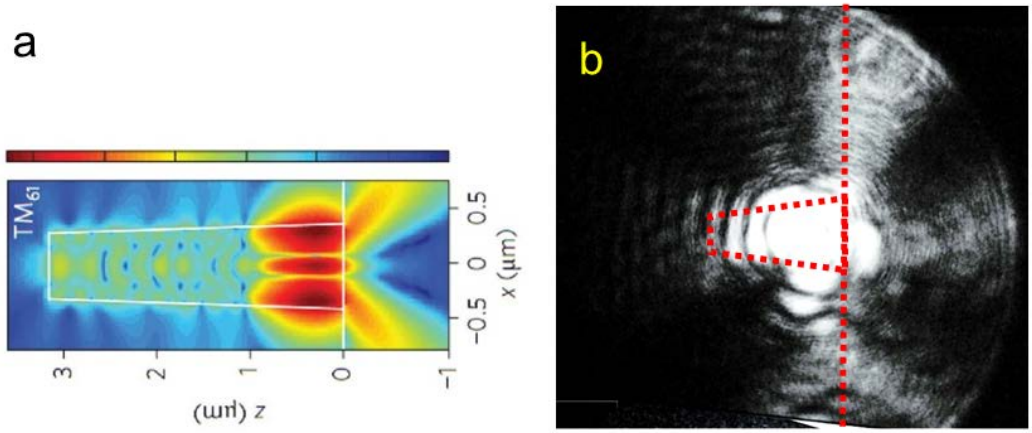

Figure 4-2 Nanopillar emission from the bottom of nanopillar. (a) FDTD simulation of nanopillar emission pattern. The nanopillar is outlined with white lines. The emission from the bottom of nanopillar is significant. (b) Optical image of horizontal nanopillar emission. The nanopillar and Si interface are outlined in red dash lines. The emission from the bottom of nanopillar is consistent with the simulation result.

4.2 Horizontal nanopillar grown on silicon waveguide

As discussed in previous section, significant amount of light emits from the bottom of nanopillar. Therefore, end-fire coupling with silicon waveguides is made possible with horizontal naonpillars, as illustrated in Figure 4-3. In this configuration, the light emitting from bottom of nanopillar can potentially couple into and propagate along silicon waveguides.

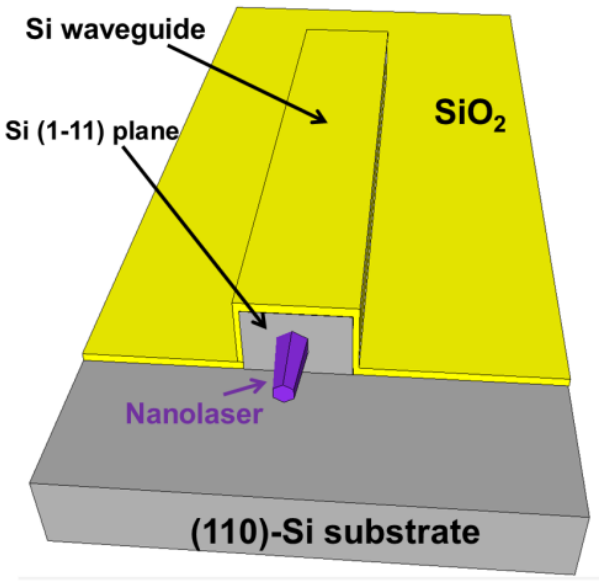

Figure 4-3 3D schematic of a horizontal nanopillar on a silicon waveguide. The nanopillar has a hexagonal shape with a small taper angle. It is comprised of an InGaAs core as the gain region, and a GaAs shell as the passivation layer. The silicon waveguide is formed by plasma dry etching on a (110)-silicon substrate. With SiO2 serving as the mask layer, a vertical (1-11) plane is created by anisotropic silicon etchant on the front end of the waveguide. As a result, the nanopillar grows horizontally on the vertical silicon (1-11) plane.

The fabrication process starts with a (110)-silicon wafer, on which the waveguides are defined by plasma dry etching. The orientation of waveguides must be along one of <111> Si orientation to facilitate formation of vertical {111} Si planes. A 200-nm-thick silicon dioxide mask layer is deposited onto the wafer by plasma-enhanced chemical vapor deposition, and then patterned to expose the front end facet of the waveguide. The wafer is subsequently treated with anisotropic silicon etchant tetramethylammonium hydroxide (TMAH) at 90^{o}C. Because the etch rate of silicon (1-11) plane is much slower than other crystal plane, the waveguide front end facet turns into a vertical silicon (1-11) plane. After that, MOCVD growth is carried out to grow the horizontal nanopillar on the waveguide front end. Figure 4-4 summarizes the process in 3D schematics.

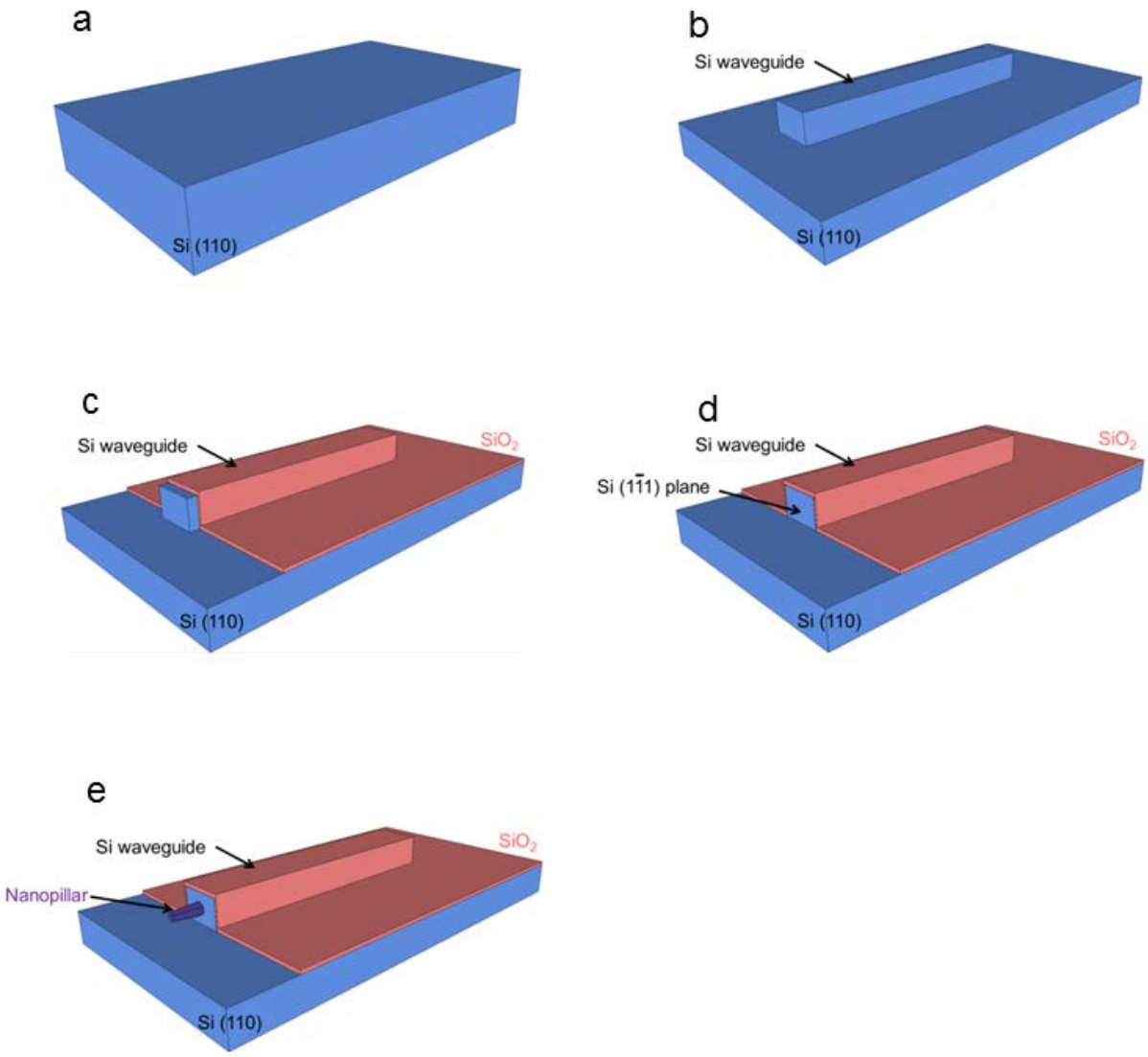

Figure 4-4 3D schematics of nanopillar-waveguide integration fabrication process. (a) Si(110) wafer as the starting point. (b) Waveguide definition by plasma dry etching. (c) Oxide deposition and etching to cover most part of Si waveguide but leave the front end portion uncovered. (d) Formation of vertical Si(1-11) plane by anisotropic Si etching with TMAH. (e) MOCVD growth of horizontal nanopillar.

Figure 4-5 shows an SEM image of a horizontal nanopillar as-grown on a silicon waveguide. The waveguide is of 4μm width, 5μm height, and 27μm length. The nanopillar has a diameter of 800nm and a height of 1.8μm. The islands sitting on top of SiO_2 are III-V clusters, due to parasitic III-V material growth. Further growth condition optimization will be necessary to minimize the island formation. Alternatively, they can be lifted-off by SiO_2 etching.

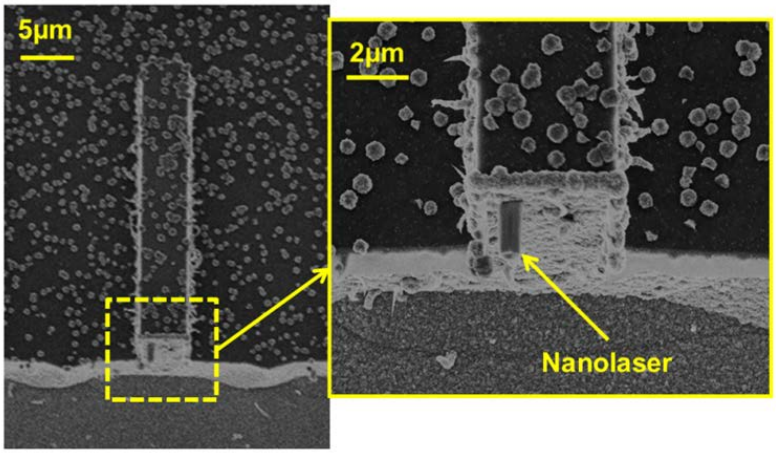

Figure 4-5 SEM picture of a nanopillar on a silicon waveguide under 20º tilt view. The silicon waveguide is of 4μm width, 5μm height, and 27μm length. The nanopillar has a diameter of 800nm and a height of 1.8μm.

Since nanopillar growth here is still spontaneous growth, precise nanopillar position on waveguide is not yet achieved. It could also be possible that multiple nanopillars grow on one single waveguide. In the future, to reconcile this issue, growth site control of horizontal nanopillar should be developed, possibly using the patterned growth technique depicted in Figure 4-6.

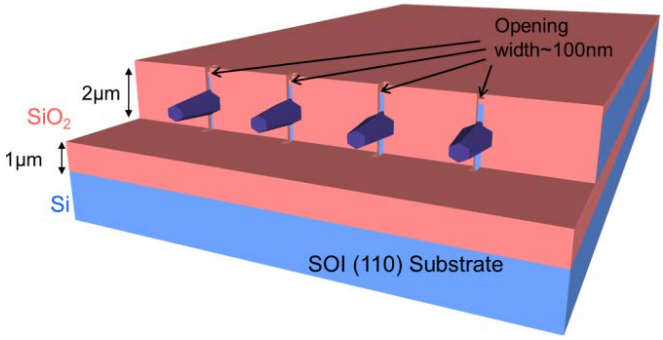

Figure 4-6 3D schematic of controlling horizontal nanopillar growth site.

4.3 Horizontal nanopillar lasing characteristics

On horizontal nanopillars, lasing is achieved with an optical pump (140-femtosecond titanium:sapphire pulses at a wavelength of 750nm) at low temperature of 4K. The spectra below and above threshold are shown in Figure 4-7(a) with the lasing wavelength at around 915nm and a side-mode suppression ratio of approximately 20dB. Figure 4-7(b) shows the laser output power as a function of pump power (L-L curve) for a typical nanopillar laser. The threshold power of 120μW corresponds to a power density of 1.2kW/cm^2. An average output power of 8.7μW or pulsed peak power of 10mW is achieved. This comparable performance with vertical nanopillar proves that nanopillar with horizontal orientation still maintains high crystal quality and superior optical characteristics.

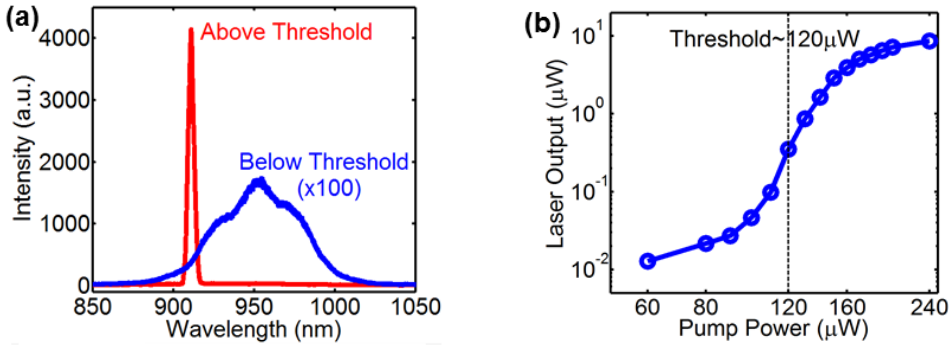

Figure 4-7 Nanopillar laser oscillation. (a) Nanopillar emission at 4K below (blue) and above (red) threshold. For visibility, the emission below threshold is magnified by 100 times. The side mode suppression ratio of the lasing peak is about 20dB. (b) L-L curve of a nanopillar laser at 4K. The blue circles are experimental data. The threshold pump power is approximately 120μW.

4.4 Laser-waveguide coupling results

To demonstrate the coupling between laser and waveguide, a 45° inclined facet on the back end of waveguide was created by focused ion beam (FIB) technique, such that laser light at the back end of silicon waveguide can be reflected upwards and readily observed. Figure 4-8(a) illustrates a 3D schematic of the characterization idea. An SEM image from a tilted side view after the FIB process is shown in Figure 4-8(b).

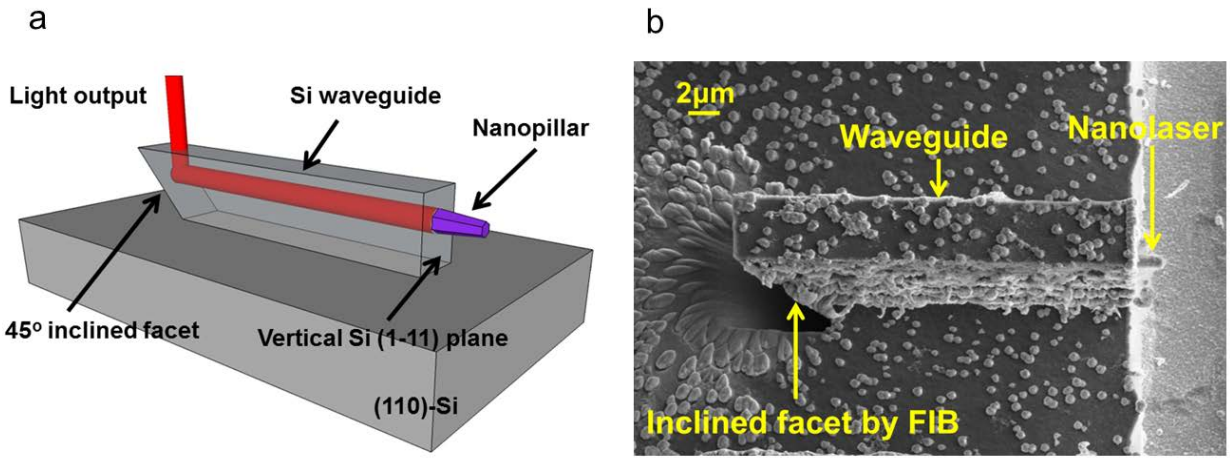

Figure 4-8 Nanopillar laser emission coupled into waveguide. (a) 3D schematic of laser-waveguide coupling; (b) SEM picture of the waveguide with an 45° inclined back end facet created by focused ion beam (FIB) technique.

Figure 4-9 shows the corresponding nanopillar emission pattern at the front end and the waveguide light output at the back end of waveguide, when optically pumped both below and

above lasing threshold. The strong waveguide light output serves as a convincing proof that the laser light indeed couples into the waveguide in an end-fire manner.

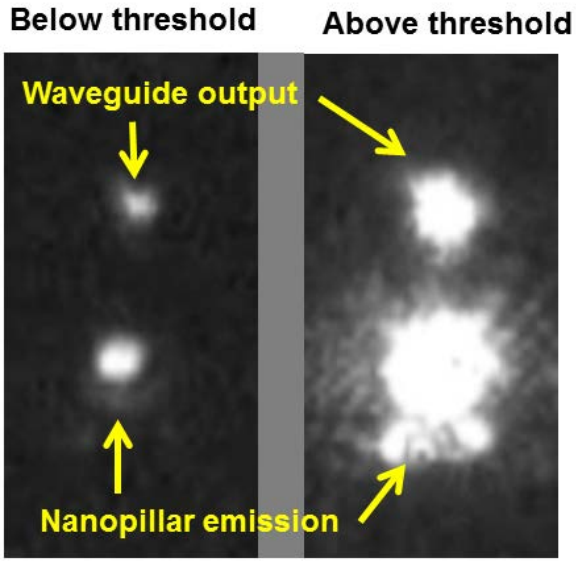

Figure 4-9 Nanopillar emission at the front end of Si waveguide and waveguide output emission at the back end of Si waveguide, for (a) below lasing threshold and (b) above lasing threshold.

To quantify the coupling efficiency (defined as the optical power coupled into waveguide divided by total nanopillar emission power), the analytical model as shown in Figure 4-10 is utilized. We use P_{total} to represent total nanopillar emission power, P_{couple} to represent power coupled into waveguide, P_{front} to represent power that is detected at the front end of waveguide, P_{back} to represent the waveguide output power that is detected at the band end of waveguide.

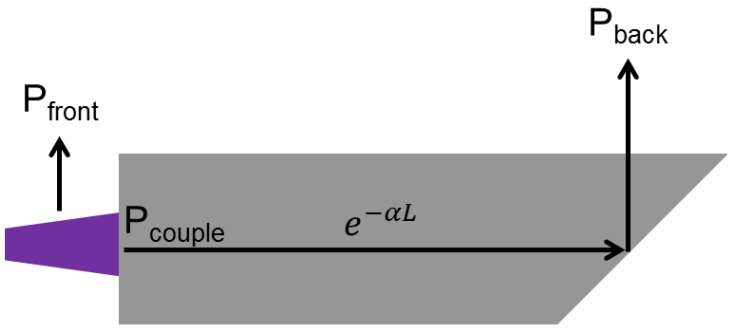

Figure 4-10 Schematic model to calculate the coupling efficiency η.

By definition, the coupling efficiency η

$$\eta = \frac{P_{couple}}{P_{total}} \qquad (4\text{-}1)$$

Since at the 45° inclined back end facet, light incident angle defined in ray optics exceeds critical angle, total internal reflection occurs. Thus, P_{couple} can be calculated from the waveguide output P_{back} by also considering waveguide loss $e^{-\alpha L}$, where α is the absorption coefficient in Si at the wavelength of 915nm and L is the length of waveguide (~27μm).

$$P_{couple} = P_{back} e^{\alpha L} \qquad (4\text{-}2)$$

P_{total} can be obtained from the nanopillar emission P_{front} detected under microscope at the front end of waveguide. However, the microscope is only detecting part of P_{total} from one side of nanopillar. Let's define the ratio $\beta = P_{front}/P_{total}$, where β can be obtained by performing 3D nanopillar simulation. Then we can back-calculate P_{total}

$$P_{total} = \frac{P_{front}}{\beta} \qquad (4\text{-}3)$$

Substitute equation (4-2) and (4-3) back into (4-1), we get

$$\eta = \beta \times e^{\alpha L} \times \left(\frac{P_{back}}{P_{front}}\right) \qquad (4\text{-}4)$$

3D nanopillar simulation obtains a β value of 21.38%. The absorption loss factor $e^{\alpha L} = \frac{1}{0.838}$. The ratio between P_{back} and P_{front} can be estimated from the ratio of integrated intensity from the microscope image, as in Figure 4-9. Figure 4-11 shows the ratio under different pump power. The P_{front}/P_{back} ratio almost maintains a constant level, probably because the large cross section of Si waveguide facilitates multi-mode coupling and can couple all the light no matter it's below or above lasing threshold. On average, this ratio is approximately 50.7%. Combining all the data, we obtain a coupling efficiency η of 13%, which means at least 5.3μW average power, or equivalently 6.1mW pulsed peak power can be coupled into the silicon waveguide. This efficiency is higher than a similar literature where nanowire laser couples to a photonics crystal waveguide [64].

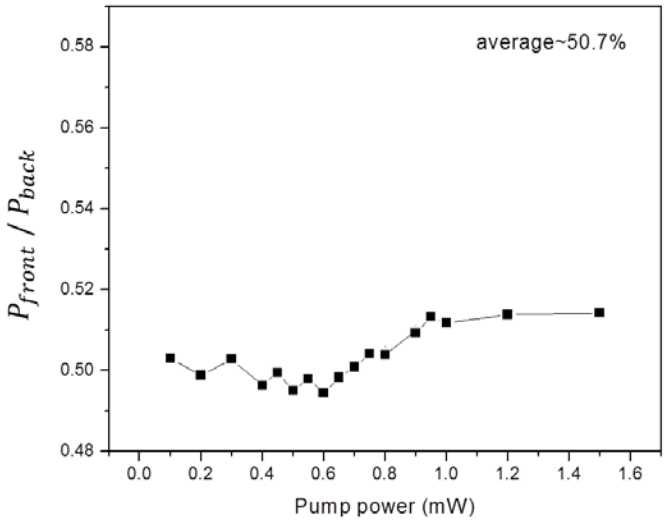

Figure 4-11 P_{front}/P_{back} ratio as a function of pump power.

4.5 Horizontal nanopillar on silicon-on-insulator (SOI) substrate

The aforementioned Si waveguide on Si(110) substrate has no bottom light confinement and might induce light leakage into substrate. Thus, horizontal nanopillar growth on (110) SOI substrate is also investigated, where the buried oxide layer can provide bottom confinement. The Si device layer is 2μm-thick with (110) orientation, whereas the buried oxide (BOX) layer is 1μm thick. The fabrication process and growth techniques are similar as discussed in section 4.1. Figure 4-12(a) illustrates several horizontal nanopillars grows on the vertical Si(1-11) plane of (110) SOI substrate. A tilt-view SEM image showing such horizontal nanopillar is shown in Figure 4-12(b).

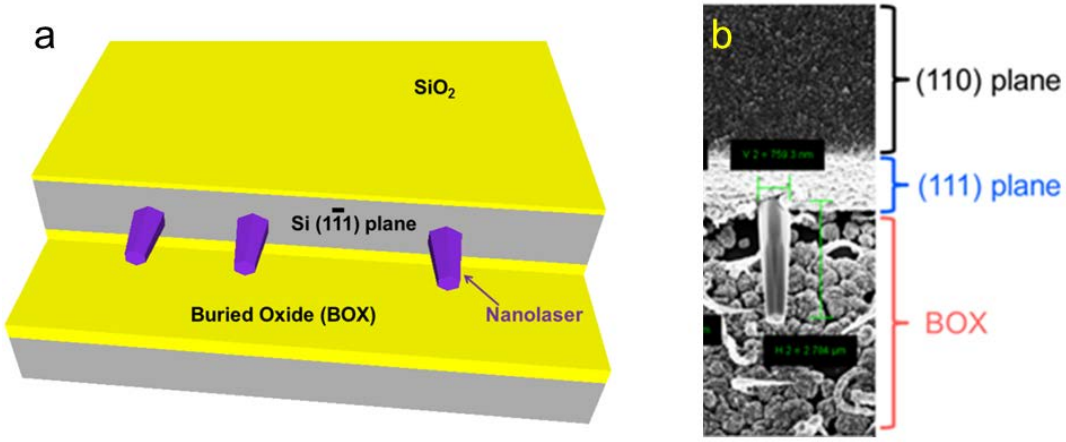

Figure 4-12 Horizontal nanopillar growth on (110) SOI substrate. (a) 3D schematic. (b) Tilt-view SEM image.

As preliminary characterization on coupling effect of SOI substrate, similar optical pumping experiment is performed on horizontal nanopillar on SOI. Figure 4-13(a) is a top-view SEM

image of two horizontal nanopillars growing on one side of Si(110) mesa. One of the nanopillars is optically pumped and a prominent coupling output is observed 10μm away on the other side of Si(110) mesa (shown in Figure 4-13(b)). This qualitatively demonstrates a respectable coupling efficiency, even without SOI waveguide or 45º inclined facet, which we attribute to the outstanding bottom light confinement by buried oxide layer. Therefore, we believe high efficiency coupling between nanolaser and silicon waveguide can be obtained by implementing SOI waveguide with optimized dimensions.

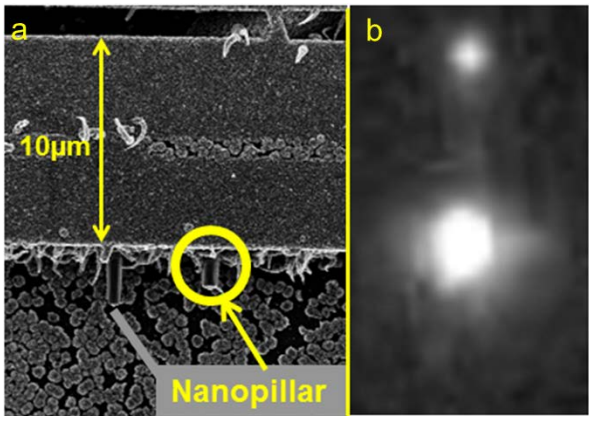

Figure 4-13 Horizontal nanopillar coupling on SOI substrate. (a) Top-view SEM image. (b) Nanopillar emission and coupling emission image. The bottom spot is emission directly from the nanopillar, whereas the top spot is coupling output after light propagate 10μm in the Si(110) mesa.

4.6 Horizontal nanopillar enabled cavity resonator

Horizontal nanopillar not only enables laser-waveguide coupling, but also opens up new optical cavity design possibilities for nanopillar laser. As examples, two new horizontal-nanopillar-based optical cavity designs will be discussed.

With horizontal nanopillar growing on waveguide, it is possible to etch silicon waveguide to form a distributed Bragg reflector (DBR), serving as an external cavity mirror. The concept is depicted in Figure 4-14. To enhance coupling of reflected light by DBR back into nanopillar, dimension of waveguide front end facet is matched with nanopillar and a waveguide taper is introduced to adiabatically change cross section dimension of waveguide. To prove the idea, 3D FDTD simulation is performed on the structure with detailed dimensions shown in Figure 4-15(a). In the simulation setting, the nanopillar is simplified as a cylinder with metal coated on top to enhance top reflection. As shown in Figure 4-15(b), cavity spectrum manifests many high Q cavity resonances with equal wavelength spacing, which is an indication of Fabry-Perot optical modes. One of the optical cavity resonances at the wavelength of 1080nm, whose Q factor is as high as 1550, has a field profile shown in Figure 4-13(c). The field decaying in the DBR region clearly shows high reflection provided by DBR. Most of field intensity lies inside nanopillar region, rather than silicon region, suggesting a high optical confinement factor or effective gain. All these are beneficial for lasing performance. Another major advantage of such external cavity is easiness of tuning cavity wavelength by simply adjusting the DBR position. Therefore,

wavelength multiplexing can be potentially achieved using multiple external cavity nanopillar lasers shown in Figure 4-16.

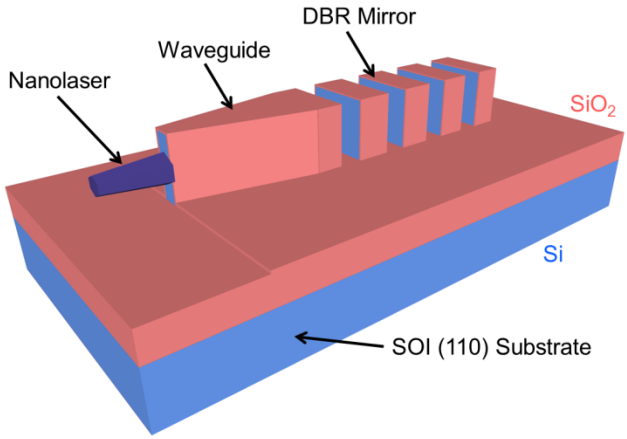

Figure 4-14 3D Schematic of horizontal nanopillar integrated with an external DBR mirror. The nanopillar is grown on (110) SOI subsrate. The DBR consists of alternating Si and air layers. Dimension of waveguide front end facet is similar as footprint of nanopillar. Waveguide taper is introduced to vary waveguide dimension adiabatically.

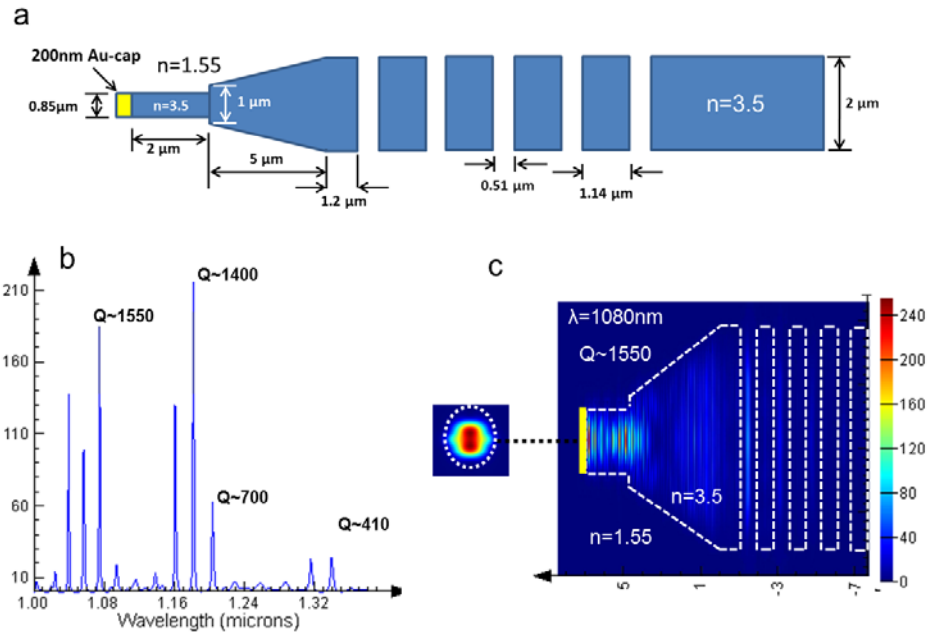

Figure 4-15 3D FDTD simulation of nanopillar integrated with DBR mirror. (a) Schematic showing all the key simulation parameters. The top of nanopillar is coated with gold metal to enhance top reflection. (b) Cavity spectrum. Multiple high Q cavity resonance is observed in the spectrum. (c) Field profile of cavity resonance at the wavelength of 1080nm.

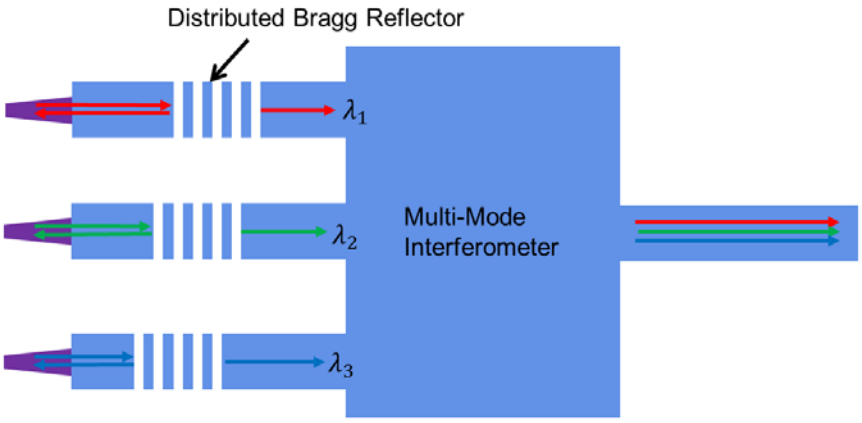

Figure 4-16 Top view schematic of wavelength multiplexing of several external cavity nanopillar lasers. The different emission wavelength is achieved by positioning DBR at different position, forming different cavity resonances.

Another novel cavity resonator is illustrated as in Figure 4-17(a). It is a horizontal nanopillar sandwiched by two thin silicon fins, forming a natural Fabry-Perot cavity. Figure 4-17(b) is a top view SEM image of a 15μm-long as-grown InP-based nanopillar, bridging two silicon waveguides. The nanopillar starts to grow on one silicon waveguide and stops horizontal growth when it hits the other nanopillar. The nanopillar consists InGaAs quantum wells inside and thus emits at silicon transparent wavelength (will be discussed in Chapter 5). As shown in Figure 4-17(c), PL measurement on such structure reveals prominent Fabry-Perot modes, which proves the concept of such cavity resonator. We believe further thinning of Si fins will result in lasers based on such cavity resonator.

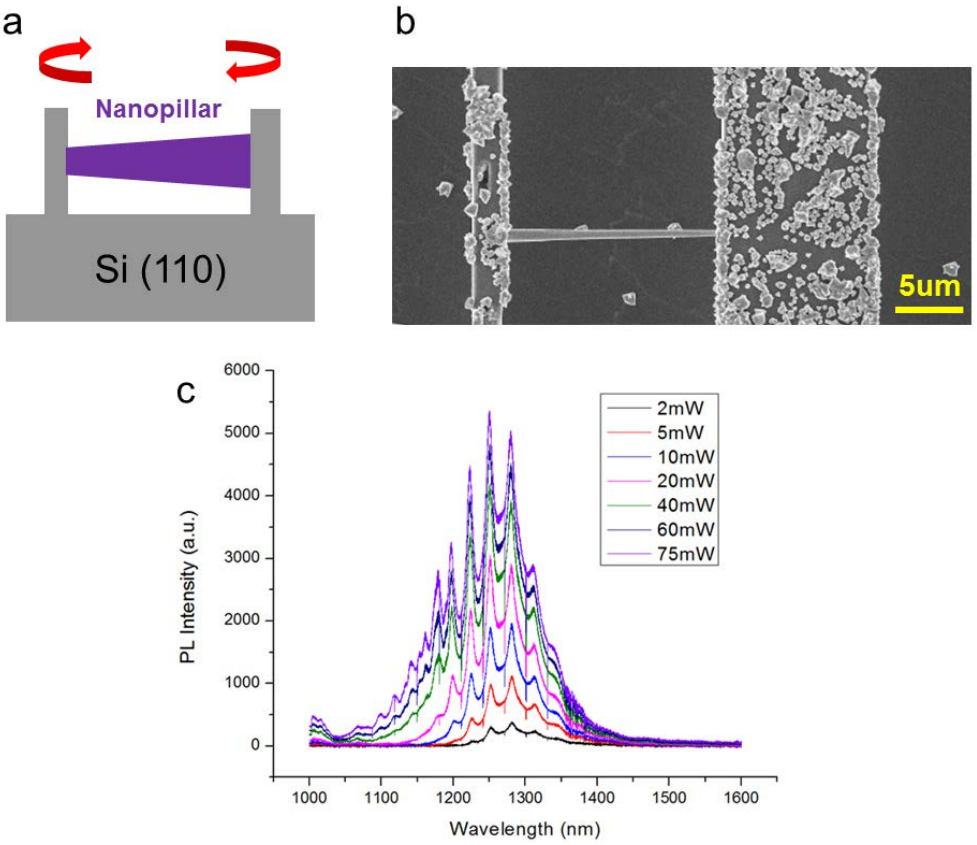

Figure 4-17 (a) Schematic of nanopillar sandwiched by two Si fins. The thin fins provide high Si-air interface reflection and form a horizontal Fabry-Perot cavity. (b) Top view SEM image of horizontal nanopillar bridging two silicon waveguides. (c) PL spectra of horizontal nanopillar sandwiched by two Si waveguides. Clear Fabry-Perot cavity modes are observed.

4.7 Summary

In this chapter, we discuss the tantalizing prospect of integrating nanopillar laser with silicon photonics seamlessly. The cornerstone of this is the unique horizontal nanopillar growth on Si (110) or SOI (110) substrate, enabled by anisotropic Si etching technique. Horizontal nanopillars exhibit as good optical quality as their vertical counterparts, which is confirmed by their lasing oscillation behavior. End-fire coupling between horizontal nanopillar laser and Si waveguides is directly proved by etching Si 45º inclined facet and micro-PL experiment thereafter. The coupling efficiency is calculated to be as high as 13% based on the relative intensity of the laser light speckle and the waveguide output in the near field image. Horizontal nanopillar growth is also achieved on (110) SOI substrate, where buried oxide can greatly enhance bottom light confinement. In addition, horizontal nanopillar enables a novel class of cavity resonator designs, such as external DBR cavity and double Si-fin cavity. The future work could be continued on the integration of horizontal nanopillars with more complex silicon photonics circuits, consisting of optical modulators, optical amplifiers and photodetectors on silicon substrates.

Chapter 5 Nanopillar Long Wavelength Laser

Practical optical interconnects requires a laser source on silicon that operates at a silicon-transparent wavelength, so as to minimize absorption loss when laser light propagates in silicon waveguide. However, all direct-bandgap semiconductor materials that can emit beyond 1.1μm are severely lattice-mismatched to silicon (see Figure 5-1), prohibiting high quality gain material epitaxial growth on silicon substrates.

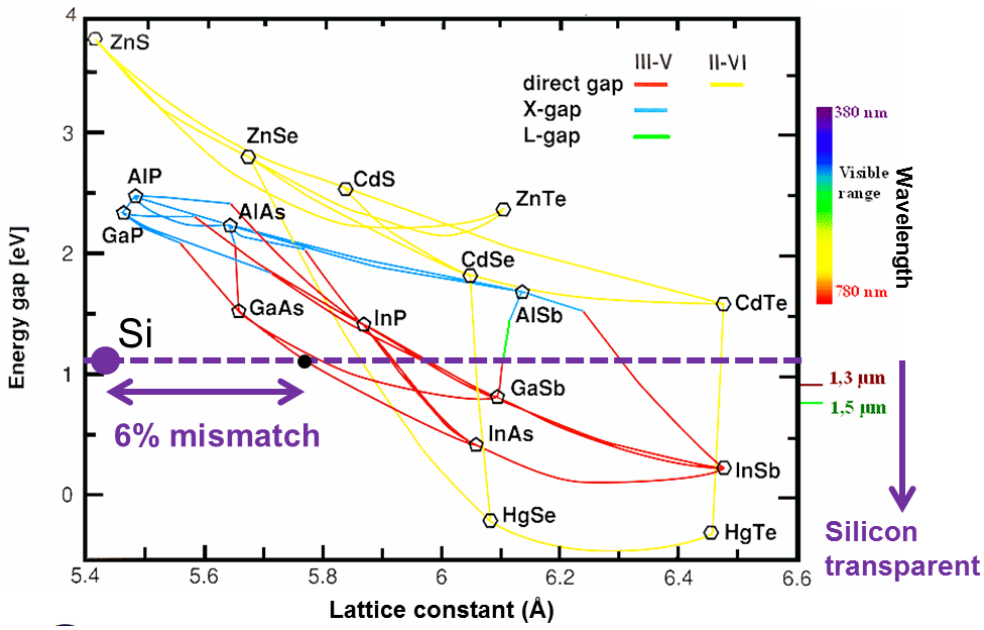

Figure 5-1 Bandgaps and lattice constants of most common III-V and II-VI semiconductors. As comparison, silicon is labeled as purple dot in the plot. The materials that have bandgap smaller than Si (1.1eV), or have silicon transparent emission, are severely lattice-mismatched to silicon (at least 6%).

To circumvent this problem, some researchers focused on bonding group III-V lasers onto a silicon substrate [27]–[29]. Other people turned to group IV lasers on silicon, by engineering strain and doping concentration to enhance radiation efficiency of germanium [15], [16]. InAs/GaAs quantum dot laser on silicon is also demonstrated recently [40], [41]. But all these approaches implement the traditional edge emitting laser structure and thus have very large footprint (at least hundreds of square micrometers to form Fabry-Perot cavity). This is too luxurious for direct integration with nano-electronics, considering the costly real state on IC chips.

On the other hand, semiconductor nanowire has a small footprint varying from tens of nanometers to hundreds of nanometers, enabling heterogeneous integration of III-V material and Si [65] without lattice-mismatch-induced dislocations. Nevertheless, their small lateral dimension results in very weak optical confinement, especially at long wavelength. Therefore, most nanowire lasers demonstrated so far emitted at visible wavelength [66]–[70] or ultraviolet wavelength [71], [72]. Very few GaAs-based nanowire lasers can operate at around 900nm [73]–

[75]. Only one laser at silicon-transparent wavelength was reported using GaSb nanowire [76]. Besides, all nanowire lasers so far are transferred onto extrinsic substrates (usually on silicon dioxide or sapphire substrates) after growth, thus preventing monolithic integration with silicon substrates.

In this chapter, we will discuss our efforts of making long wavelength (λ>1.1μm) nanopillar laser. The first strategy we use is InGaAs-based nanopillar by simply increasing indium composition of InGaAs. A graded indium composition structure is needed to accommodate the lattice mismatch between different indium composition layers. However, this approach is fundamentally limited by lattice mismatch and emission wavelength fails to reach well beyond 1.1μm.

For the other strategy, we demonstrate the first quantum-well (QW)-on-nanopillar laser as-grown on silicon with silicon-transparent emission, by directly synthesizing high quality InP/InGaAs/InP nanopillar. The cornerstone of our nanolaser is InGaAs quantum wells with superior quality as the gain media, revealed by high resolution transmission electron microscopy (TEM).

Due to its unique core-shell growth mode, nanopillar can scale up to micron size in lateral dimension while maintaining superior quality in the bulk [53]. With nanopillar's close-to-micrometer diameter, light can be confined well inside nanopillar. Thus, transferred nanopillar onto extrinsic substrate, possessing a natural horizontal Fabry-Perot cavity, already demonstrates lasing behavior, attesting to high quality of quantum wells. Furthermore, as-grown nanopillar laser on SOI substrates is also obtained, thanks to the bottom reflection enhancement by the buried oxide. With the capability of tuning gain media bandgap by changing indium composition in InGaAs QWs, our nanolaser emission can range from 1.1μm up to 1.3μm. In addition, we show a novel resonator structure with Si undercut-etching to increase cavity Q value. This also leads to as-grown long wavelength nanopillar laser on Si substrate.

Moreover, modeling of long wavelength lasers is performed not only to understand lasing behavior, but also to provide guidelines of further optimizing laser as well as developing electrically-pumped nanolasers.

5.1 InGaAs-based long wavelength laser

Most InGaAs-based nanopillars discussed in previous chapters has nominal 20% indium composition InGaAs core with a GaAs passivation shell. Thus, the emission wavelength is approximately 900nm. To reach silicon transparency at cryogenic temperature, a nominal 30% indium composition is the minimum requirement. However, it is not straightforward to directly increase indium composition because lattice constant of InGaAs is very sensitive to indium composition. Figure 5-2 shows a schematic of 30% indium InGaAs nanopillar and several tilt-view SEM images. As illustrated in Figure 5-2(a), the nanopillar has a 20% InGaAs core to initiate nucleation, a 30% InGaAs as the gain material, as well as GaAs shell as passivation. The SEM image Figure 5-2(b) shows that nanopillar surface is filled with wrinkles, indicating bad quality material resulting from large strain. In some nanopillars, large strain inside nanopillar even leads to internal cracking of nanopillar, as shown in Figure 5-3(c). It is hypothesized that

the strain comes from the mismatch between 20% InGaAs and 30% InGaAs, as well as between 30% InGaAs and GaAs. As a result, these nanopillars have very weak emission and fail to lase at long wavelength.

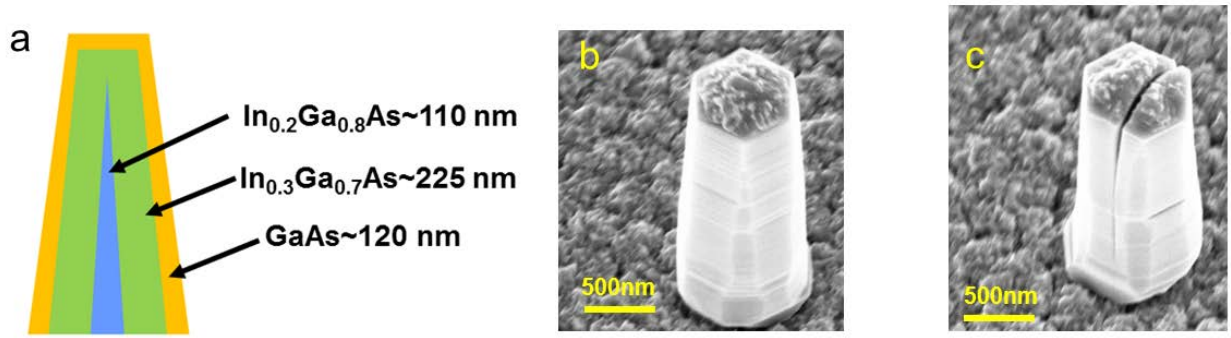

Figure 5-2 (a) Schematic of 30% indium composition InGaAs nanopillar, consisting of 20% InGaAs core, 30% InGaAs gain region, and GaAs shell. (b) Tilt-view SEM image of 30% InGaAs nanopillar with surface wrinkles, indicating inferior material quality due to large internal strain. (c) SEM image of 30% InGaAs nanopillar cracking from inside due to large strain.

To overcome this issue, both double heterostructure and indium composition grading are applied, as illustrated in Figure 5-3(a). This new structure adds two 25% InGaAs on both sides of 30% InGaAs to adiabatically vary indium composition and reduce the strain with 20% InGaAs core as well as GaAs shell. As a result, the SEM image of such structure demonstrates very smooth crystal surface, which is indicative of superior crystal quality, as shown in Figure 5-3(b). Thus, lasing behavior is readily achieved under optical pumping. The PL spectra under different pumping power are shown in Figure 5-4(a), with prominent lasing peak. Most of nanopillars lase at 1030nm, whereas some nanopillar lasers emit beyond 1.1μm due to indium composition inhomogeneity among nanopillars (shown in Figure 5-4(b)).

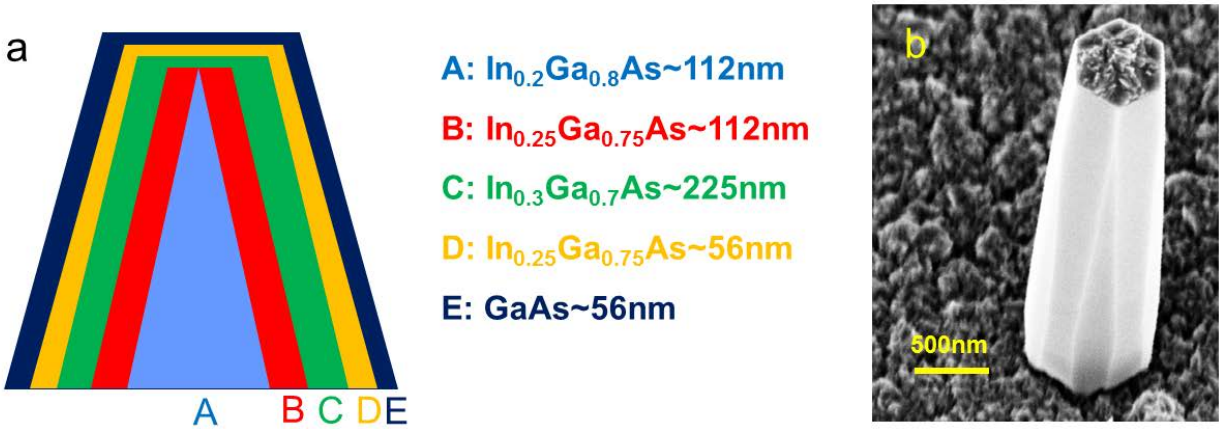

Figure 5-3 30% InGaAs nanopillar with both double heterostructure and indium composition grading (a) schematic of 30% InGaAs nanopillar. (b) Tilt view SEM image of nanopillar with smooth surface, indicating good material quality.

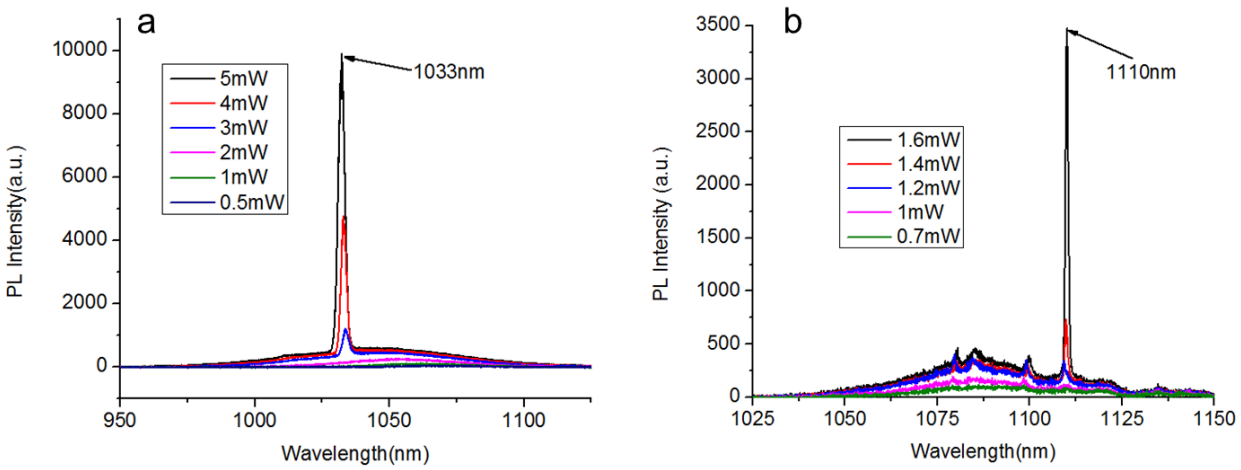

Figure 5-4 PL spectra of 30% InGaAs nanopillar laser. (a) Nanopillar laser with 1030nm lasing wavelength. (b) Nanopillar laser with 1110nm lasing wavelength.

Although silicon transparent lasing is achieved based on InGaAs nanopillar, this strategy has limited potential to scale to longer wavelength due to its fundamental barrier of lattice mismatch. Therefore, we will discuss the more promising strategy using InP-based nanopillars in the following sections.

5.2 InP nanopillar with InGaAs quantum wells

InP/InGaAs material system is commonly used to make bulk lasers at telecommunication wavelength. InP is a superior surface passivation material, while InGaAs serves as the gain material with bandgap lower than 1.1eV. Therefore, we investigate the possibility of growing InP nanopillar with InGaAs quantum wells. Note that quantum wells are used to reduce any possible strains between InP and InGaAs although in theory it is possible to have long wavelength emission with InGaAs material lattice-matched with InP by careful engineering of indium composition. The schematic of our nanopillar structure is illustrated in Figure 5-5(a). First, InP nanopillar grows vertically along Si (111) direction. In a core-shell way, InGaAs quantum well(s) is subsequently incorporated onto InP. Another InP layer is finally capped as the surface passivation layer. In the cross-section view, quantum well will show up as a hexagonal ring in this InP/InGaAs/InP heterostructure. Figure 5-5(b) shows the 30º tilt view scanning electron microscopy image of a nanopillar, with a typical diameter of ~800nm and a height of 6-7μm. To visualize the quantum well(s) inside nanopillar, cross-sectional transmission electron microscopy (TEM) analysis is utilized. Figure 5-5(c) is the cross-sectional TEM image of a nanopillar with single quantum well inside. Due to atomic mass difference, InGaAs quantum well distinguishes itself from InP as a brighter hexagonal ring. The thickness of quantum well is measured to be ~5nm. The interface between InP and InGaAs is very sharp without any defects or dislocations, attesting to the superior quality of InGaAs quantum well. To provide enough gain for lasing behavior, multiple quantum wells might be necessary. Thus, double quantum wells and five quantum wells structures are also grown and evaluated in TEM, as shown in Figure 5-5(d-e). The inset of Figure 5-5(e) is a zoom-in TEM image of five quantum well structure, where each

quantum well is well separated by InP barrier layer of ~5nm thickness and maintains high crystal quality.

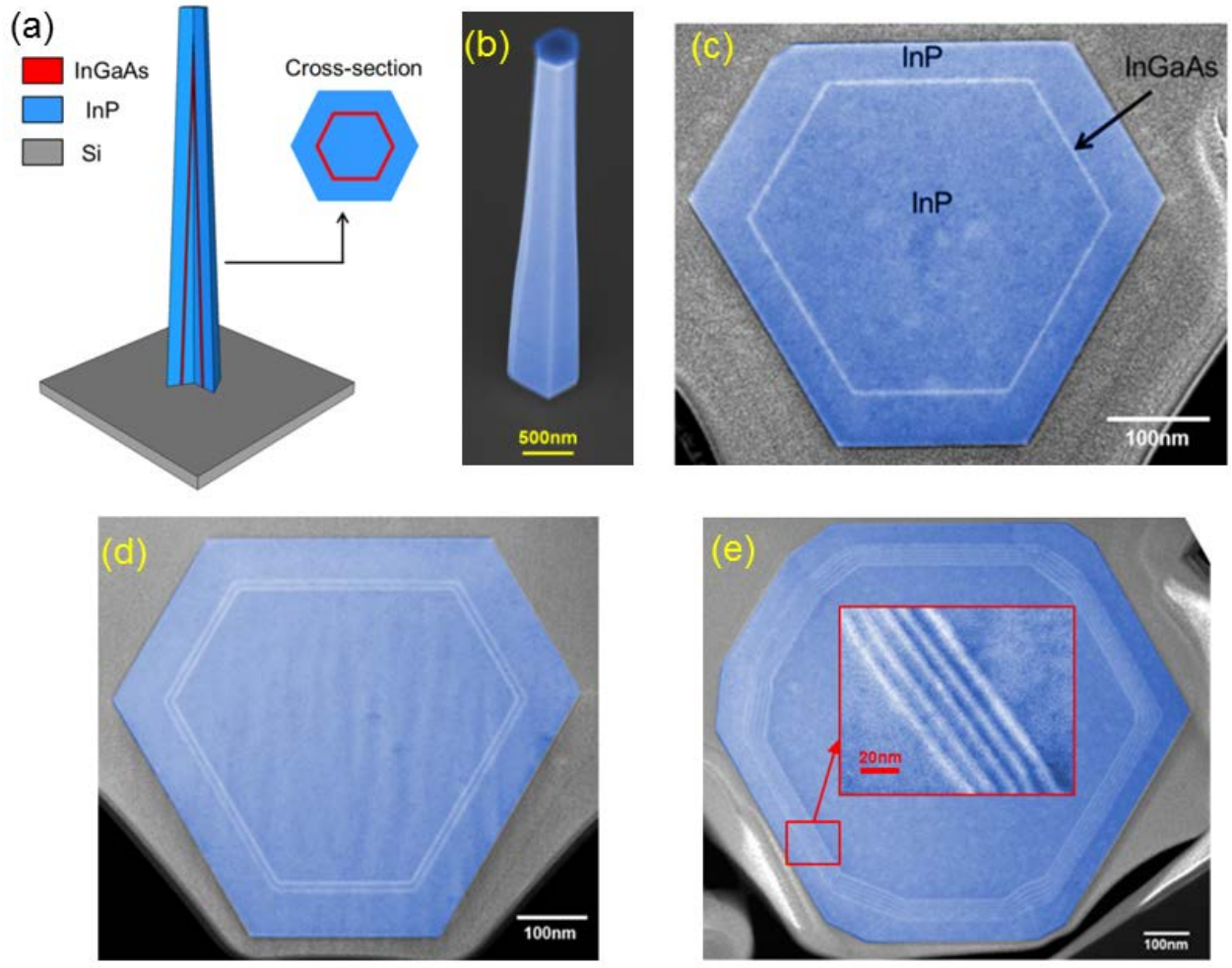

Figure 5-5 (a) Schematic of an InP/InGaAs/InP nanopillar on a silicon substrate. The structure is a result of our unique nanopillar core-shell growth mode (b) Tilt-view SEM image of a typical nanopillar with a diameter of 800nm and a height of 6-8μm (c) Cross-sectional TEM of a single quantum well (QW) structure. The contrast between InGaAs and InP comes from atomic mass difference. The thickness of quantum well is measured to be ~5nm (d) Cross-sectional TEM of double QWs structure (e) Cross-sectional TEM of a five QWs structure with the inset zooming in to the five well-separated quantum wells.

Photoluminescence (PL) experiment was subsequently performed on as-grown InP/InGaAs/InP nanopillars to check optical characteristics of quantum wells. Figure 5-6(a) shows the PL spectra of nanopillars with different indium composition in InGaAs single quantum well. The indium composition control is achieved by varying trimethylindium (TMIn) gas flow rate during the growth of InGaAs quantum well. Under ultra-low pump power so as to eliminate band filling effect, the emission peak wavelengths are all above 1100nm, which is transparent to silicon substrate. As indium composition increases, emission wavelength shifts towards longer

wavelength. By tuning growth time of quantum well layer, thickness of quantum well is also tuned to evaluate the quantization effect, as shown in Figure 5-5(b). From finite quantum well model, the quantization energy will increase as the thickness of quantum wells reduces, leading to a shorter wavelength emission. The PL measurement results show that as quantum well thickness reduces from 5nm to 1.3nm, wavelength blue-shifts approximately 200nm. This is consistent with detailed finite quantum well analysis in section 5.6.1.

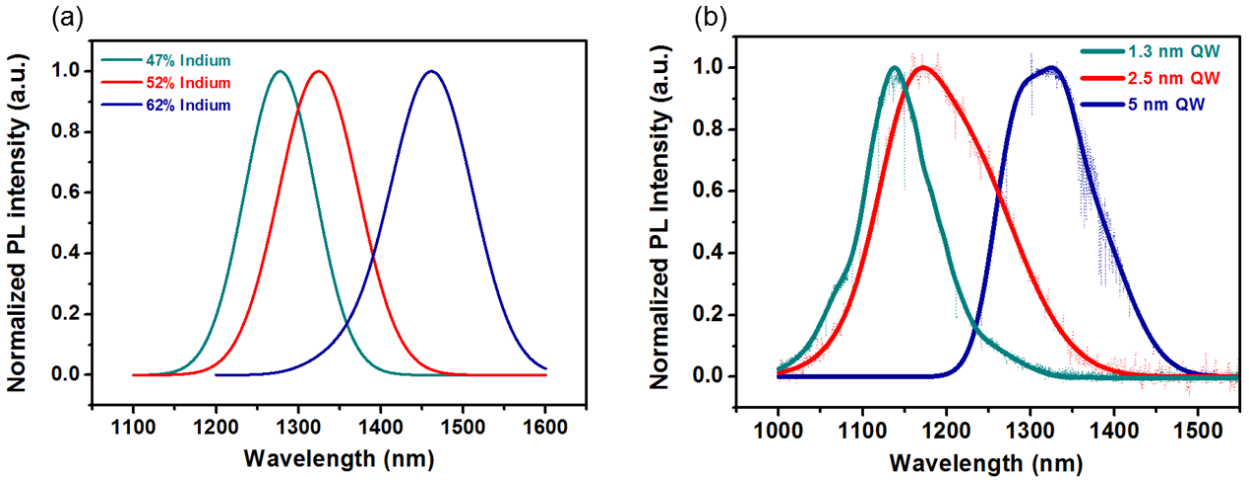

Figure 5-6 (a) Normalized photoluminescence (PL) spectra of InP/InGaAs/InP nanopillars with different indium compositions in InGaAs quantum well. The indium composition is controlled by trimethylindium (indium source) flow rate into the growth chamber (b) Normalized PL spectra of InP/InGaAs/InP nanopillars with different InGaAs quantum well thicknesses. The thickness is controlled by InGaAs layer growth time.

5.3 Transferred nanopillar laser

Due to the fact that InP has a lower refractive index than silicon, the reflection at the bottom of nanopillar is poised to be modest, leading to a relatively low quality factor optical cavity. To enhance the optical feedback, as-grown InP nanopillar with five InGaAs quantum wells was transferred to sapphire substrate by mechanical wiping. In the lying-down nanopillar, semiconductor-air interfaces at both top and bottom of nanopillar provide strong reflection, forming a horizontal high Q Fabry-Pérot cavity. This is also the typical configuration for studying nanowire lasing behavior, as illustrated in the inset of Figure 5-7(a).

Lasing at the wavelength of 1300nm is achieved using an optical pump (120-femtosecond titanium:sapphire pulses at a wavelength of 900 nm) at cryogenic temperature. Figure 5-7(a) shows the spectra below and above lasing threshold. Under low pump power (blue curve in Figure 5-7(a)), Fabry-Pérot modes are clearly observed, with a distinctive feature that optical mode wavelengths are equally spaced. The mode spacing $\Delta\lambda$ is measured to be 17nm, matching the theoretical value determined by:

$$\Delta\lambda = \frac{\lambda^2}{2n_g L} \qquad (5\text{-}1)$$

, where n_g is the group index and L is cavity length. When pump power climbs over lasing threshold, one of the Fabry-Pérot modes at the wavelength of ~1300nm dominates the spectra with a side mode suppression ratio of 16.4dB.

Several other evidences further attest to the lasing behavior. First, as shown in the red trace in Figure 5-7(b), PL emission intensity plot as a function of pump pulse fluence evidently demonstrates a kink, highlighting the lasing threshold of this transferred nanopillar. Next, blue trace of Figure 5-7(b) shows that full-width-at-half-maximum (FWHM) linewidth of the lasing mode at ~1.3μm narrows to only ~1nm above lasing threshold. Finally, near filed image above threshold (the inset of Figure 5-7(b)) shows the interference pattern between the top and bottom end facet emission from the nanopillar, confirming the spatial coherence of light.

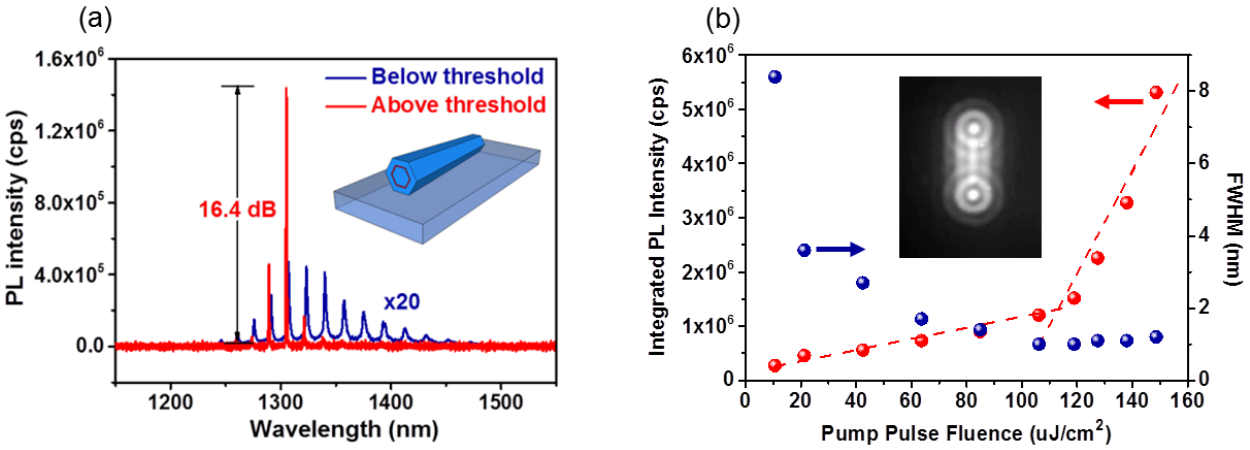

Figure 5-7 (a) Photoluminescence (PL) spectra of a transferred nanopillar below and above lasing threshold. The emission below threshold is amplified by 20 times for visibility. The inset is a schematic of a transferred nanopillar onto sapphire substrate. The PL experiment was conducted at low temperature of 4K and under 900nm pulse pump laser (b) Integrated PL intensity and full-width-at-half-maximum (FWHM) of the lasing mode at ~1.3μm as a function of pump pulse fluence. The inset is the near field image of the nanopillar emission above lasing threshold.

5.4 As-grown nanopillar laser on SOI substrate

Although lasing behavior of transferred nanopillar corroborates its superior quality, as-grown nanopillar laser is of more momentous significance towards monolithic integration with silicon electronics, simply because the position of as-grown nanopillar is better controlled. Furthermore, sub-micrometer footprint of as-grown nanopillar minimizes the area of lasers on a chip and also enables high density nano-photonics on silicon. To build a vertical high Q Fabry-Pérot cavity, nanopillars are grown onto a silicon-on-insulator (SOI) substrate, where the Si-SiO_2 interface enhances the bottom reflection of the nanopillar. In the SOI substrate, the buried silicon dioxide layer is ~2μm thick, whereas the silicon device is as thin as ~500nm, such that reflected light at Si-SiO_2 interface can goes back to nanopillar cavity and contributes to cavity feedback. The inset in Figure 5-8(a) illustrates the as-grown nanopillar configuration. Under the same optical

pumping condition as transferred nanopillar laser, lasing at the wavelength of 1140nm is successfully obtained on the as-grown nanopillars on SOI, as shown in the Figure 5-8(a). Figure 5-8(b) is the PL emission intensity of the lasing mode as a function of excitation intensity in the log-log scale, also known as L-L curve. The red eye guide curve prominently demonstrates an S-shape, which is a compelling indication of lasing. Also, near field image above lasing threshold, as in Figure 5-8(d), exhibits clear speckle pattern, as compared to that below lasing threshold (Figure 5-8(c)) where only spontaneous emission spot is observed. Furthermore, with the same structure, by just tuning the indium composition in InGaAs QWs, nanopillar lasers at different wavelength are achieved, ranging between 1.1μm and 1.3μm. The corresponding lasing PL spectra are shown in Figure 5-9. We believe longer wavelength up to 1.6μm is possible provided that the nanopillar is grown to the appropriate size to form a high Q cavity.

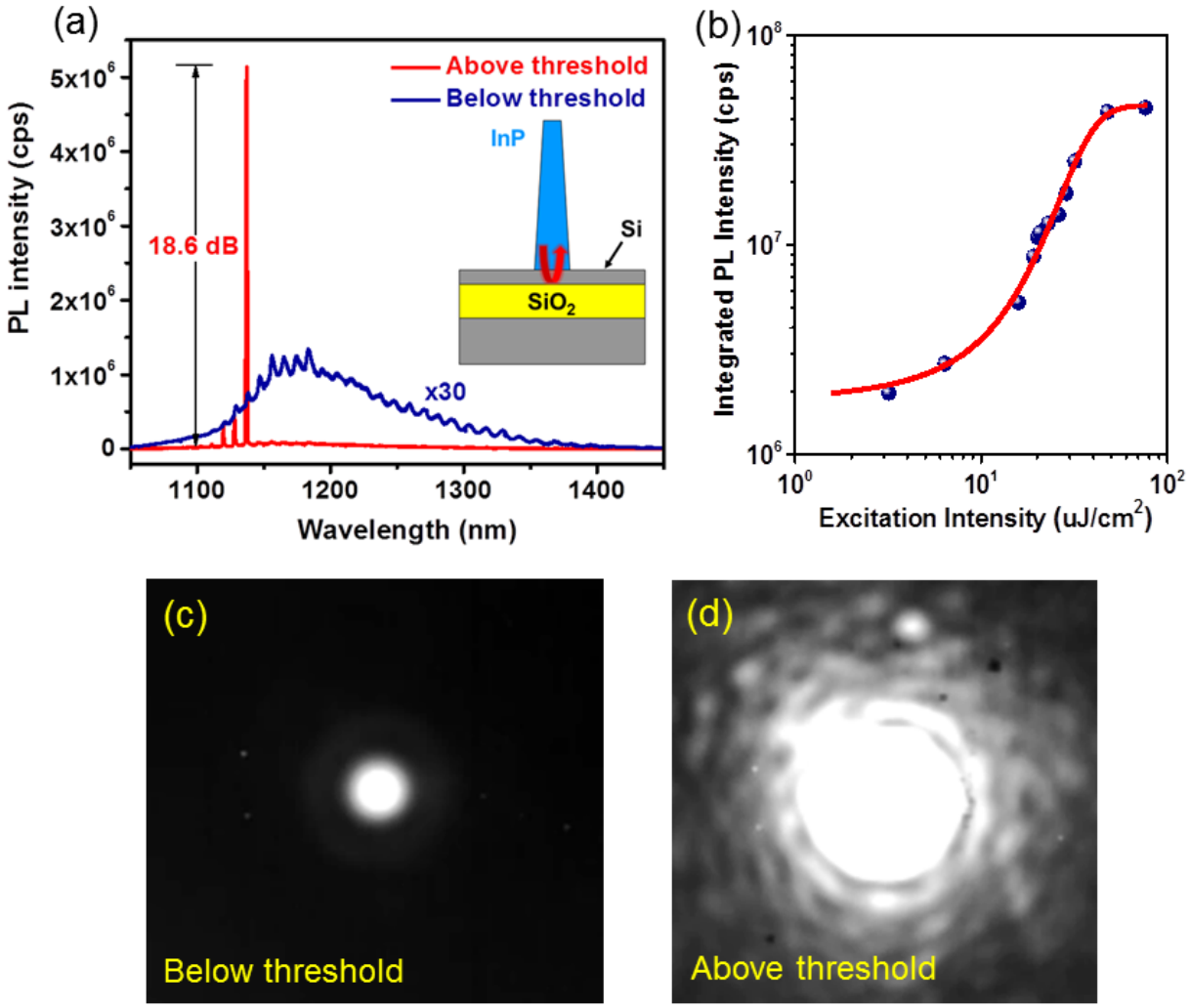

Figure 5-8 (a) Photoluminescence (PL) spectra of an as-grown nanopillar below and above lasing threshold. The emission below threshold is amplified by w0 times for visibility. The inset is a schematic of an as-grown nanopillar on SOI substrate. The PL experiment was conducted at low temperature of 4K and under 900nm pulse pump laser (b) Integrated PL intensity of the lasing mode a function of pump excitation intensity in

log-log scale (c) near filed image of nanopillar emission below threshold (d) near field image of nanopillar emission above threshold

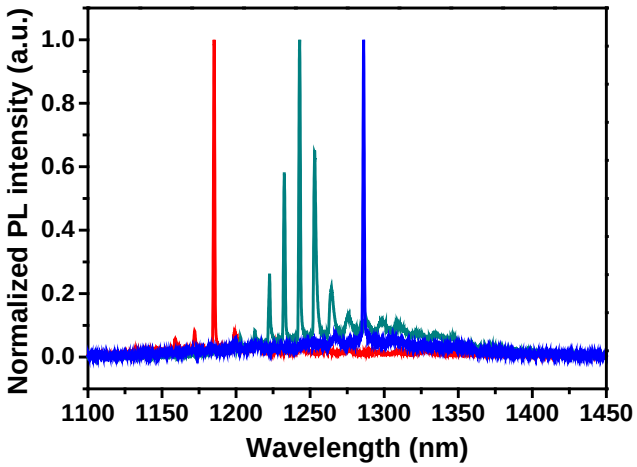

Figure 5-9 Photoluminescence (PL) spectra of as-grown nanopillars on SOI substrates with different lasing wavelength when pumping above threshold. The lasing wavelength is tuned simply by changing the indium composition in InGaAs QW active gain region.

5.5 As-grown nanopillar laser with undercut on Si substrate

Aside from nanopillar on SOI, an alternative novel cavity structure to enhance bottom reflection is also proposed in Figure 5-10(a). The structure can not only provide high Q optical cavity, but also possess a major advantage in terms of electrical property, which will be discussed in Chapter 6.

The key to creating such cavity structure is isotropic selective etching of Si by plasma mixture of 90% SF_6 and 10% O_2. Because InP is resistant to such plasma etching, nanopillar serves as a natural hard mask and a Si undercut underneath InP nanopillar can be formed. To intuitively understand how this structure can enhance bottom reflection, we will look at the field distribution of the supported cavity mode. As shown in Figure 5-10(b), the cross section field distribution is a six-fold symmetry high order mode with intensity peaks close to edge of nanopillar. Therefore, when it hits the interface between InP and Si interface with an undercut, it cannot propagate into silicon substrates because mode intensity peaks cannot lie in low index region of air. Light has no choice but to reflect back to nanopillar. This reflection, in essence, is governed by severe mode mismatch between nanopillar region and Si undercut region.

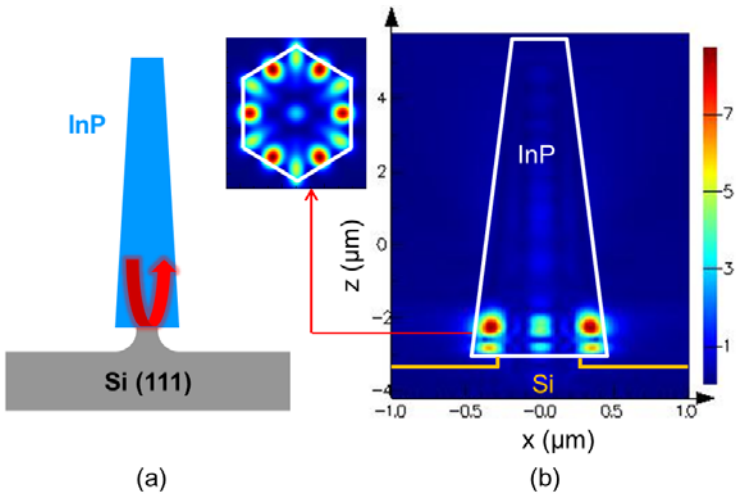

Figure 5-10 (a) Schematic of a silicon undercut structure. (b) Field profile of a cavity mode in this structure based on 3D FDTD simulation. The modes are concentrated at the bottom of nanopillar because of the nanopillar taper. Due to the large diameter, the mode is at the side of nanopillar. Upon reaching InP-Si interface, the mode is reflected due to mode mismatch resulting from the undercut.

Based on 3D FDTD simulations, optical cavity Q can be calculated for different undercut amount. For simplicity, the pedestal resulting from undercut is modeled as a cylinder with the radius r, whereas the radius at the bottom of nanopillar is 0.4μm. Figure 5-11 shows optical cavity Q factor Q as a function of Si undercut radius r. As a comparison, Q factor is around 80 without any Si undercut. When the radius is below 0.35μm (which means undercut is more than 50nm on each side), quality factor Q increases to 300 or so. However, if undercut is too small (less than 50nm), it is almost equivalent to on plain Si substrate. In short, as long as Si undercut is large enough to induce mode mismatch, cavity resonance Q can improve by more than three-fold.

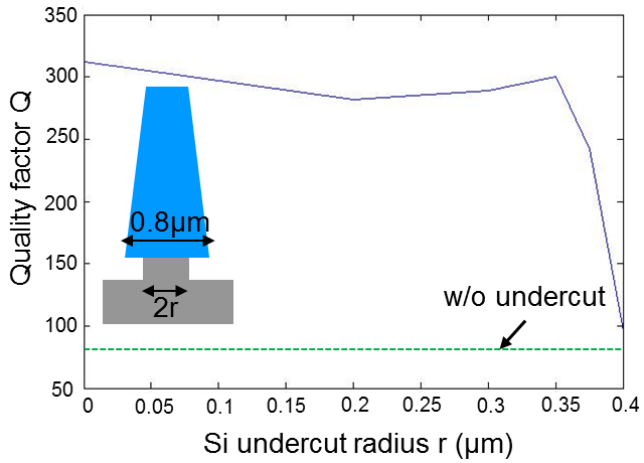

Figure 5-11 Optical cavity quality factor Q of undercut structure as a function of Si undercut radius r. The bottom radius of nanopillar is 0.4μm. The pedestal formed by

undercut is simplified as a cylinder with radius of r. Without any Si undercut (nanopillar directly sits on Si substrate), the quality factor Q is only 80, whereas sufficient Si undercut boost the Q to 300 or so.

Figure 5-12 shows a typical tilt-view SEM image of silicon undercut etching result. The Si undercut region is highlighted in blue. As seen in Figure 5-12, the InP nanopillar remains intact after the Si etching. However, to ensure that InP nanopillar crystal quality is not affected by Si plasma etching, time-resolved photoluminescence (TRPL) experiment is performed to measure the carrier lifetime of nanopillar before and after Si etching. Figure 5-13 is the extracted carrier lifetime from TRPL measurement under different pump laser power before and after undercut. It is obvious that the carrier lifetime of InP nanopillar maintains at the same level after Si undercut, confirming that Si etching has minimal effect on nanopillar. Therefore, this Si etching does not require any mask and is as simple as any self-aligned etching processes. The amount of undercut is controlled by the etching time. Thus, systematic etching experiment has been performed to obtain controllable and repeatable silicon undercut etching.

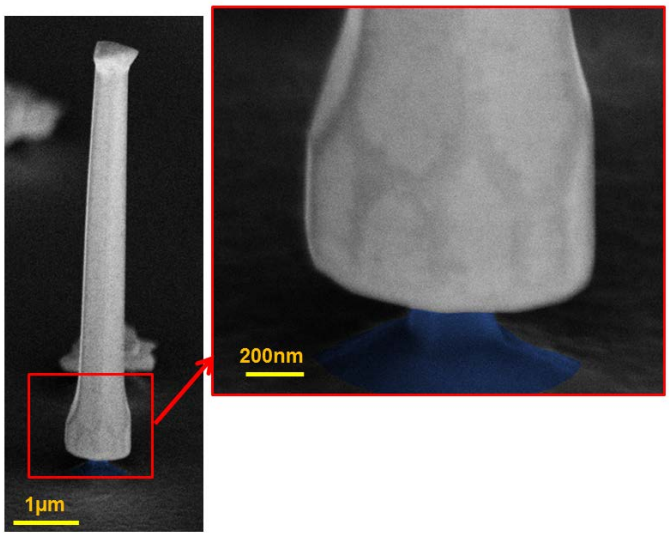

Figure 5-12 A typical tilt-view SEM image of an InP nanopillar after silicon undercut etching. Zoom-in SEM image shows the small Si pedestal resulting from the Si undercut etching, with the Si undercut portion colorized in blue.

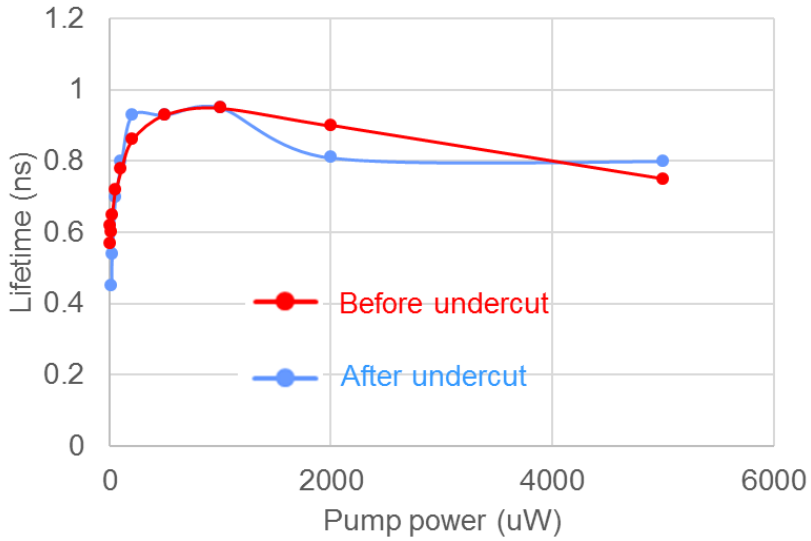

Figure 5-13 InP nanopillar lifetime as a function of optical pump power. The red curve is the lifetime before Si undercut, whereas the blue curve is the lifetime after Si undercut. Lifetime almost maintains its level before and after Si undercut, indicating minimal Si undercut effect on InP nanopillar.

By incorporating multiple InGaAs quantum wells into this novel high Q undercut cavity, long wavelength nanolaser was achieved at low temperature under optical pulsed pumping. Figure 5-14 is the PL spectra below and above threshold, with the lasing wavelength at around 1.2μm. To further confirm the lasing behavior, L-L curve was plotted in Figure 5-15 with a typical S-shape near the threshold. Also, prominent speckle pattern was observed in near field image when pumped above lasing threshold, as shown in the inset of Figure 5-15. It is worth noting that before the Si undercut as-grown InP/InGaAs/InP nanopillar does not show lasing behavior, which indicates that the undercut etching dramatically enhances cavity Q.

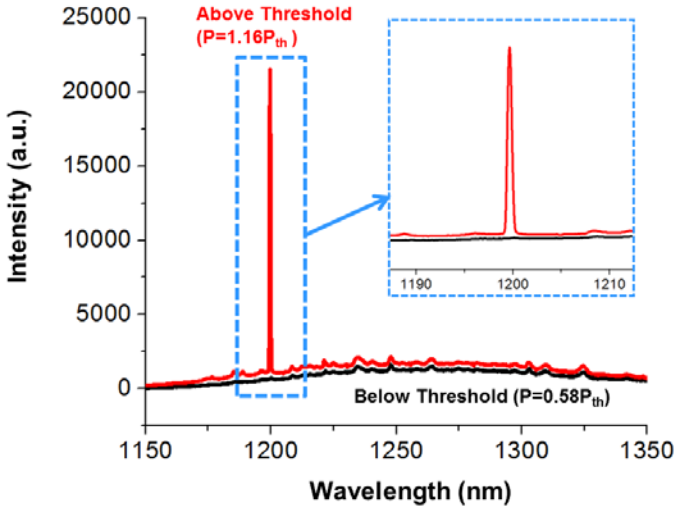

Figure 5-14 Photoluminescence spectra below and above lasing threshold for undercut nanopillar structure. The experiment was conducted at low temperature of 4K and under 900nm pulse pump laser.

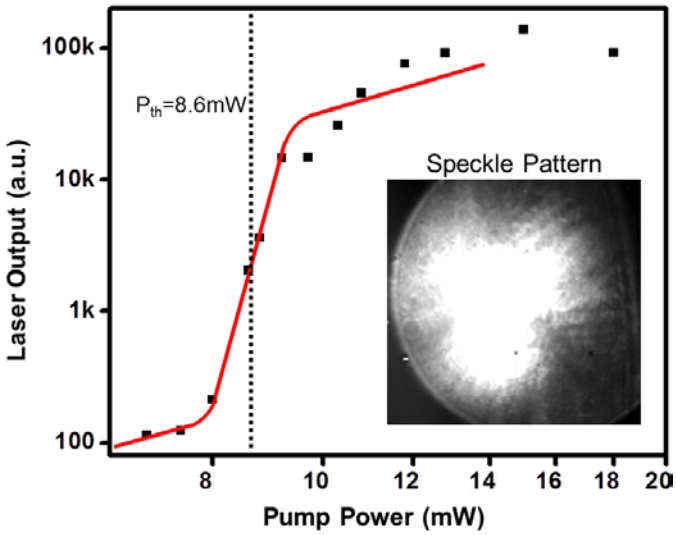

Figure 5-15 Laser output as a function of pump power in log-log scale(L-L curve). The red S-shape eye guide is a strong evidence of laser oscillation. The inset is the speckle pattern observed in near field when nanopillar is pumped above lasing threshold.

Interestingly, by using a 100x attenuator, the fine feature of mode pattern when nanopillar is above lasing can be resolved under microscope, as shown in Figure 5-16(a). Unlike the fundamental lasing mode commonly seen in conventional lasers, this mode pattern with a void exists in the center is clearly a higher order transverse mode. This is consistent with mode simulation result shown in Figure 5-10(b), where mode intensity peaks are close to edge of nanopillar. However, it is difficult to tell the exact mode order it is exciting due to microscope image resolution limit. To further evaluate the polarization characteristics, a linear polarizer is used with different orientation angles. As in Figure 5-16(b-e), different polarizer directions results in different lasing mode patterns. Comparing them to the theoretical polarization of TE and TM modes in Figure 5-16(f), it is obvious to identity that the lasing mode at 1200nm is TE-polarized.

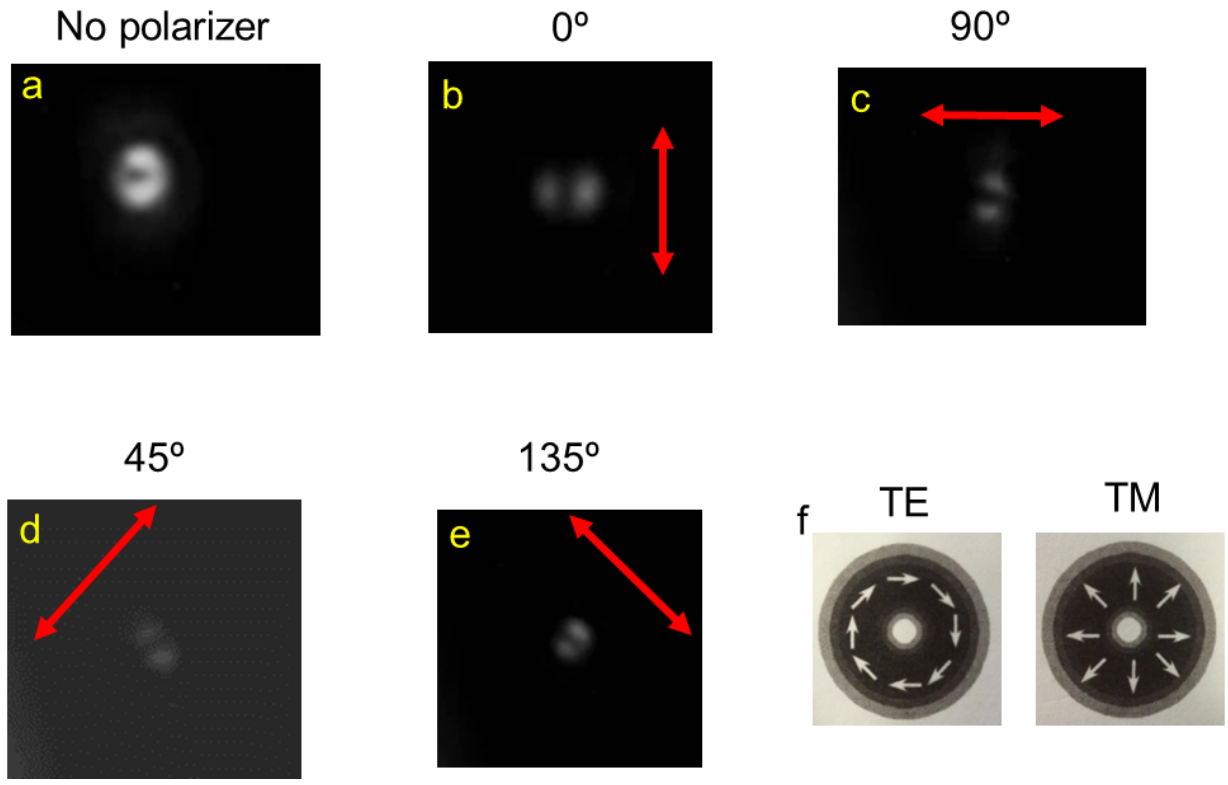

Figure 5-16 Microscope image of nanopillar emission pattern above lasing threshold with and without linear polarizer. (a) No linear polarizer; (b) Linear polarizer aligned at 0°, as indicated by the red arrow; (c) Polarizer orientated at 90°; (d) Polarizer orientated at 45°; (e) Polarizer orientated at 135°; (f) Theoretical polarization of TE and TM modes.

This long wavelength nanopillar laser with Si undercut also demonstrates extraordinary nonlinear effect. The lasing light at 1200nm induces second harmonic generation, which leads to laser emission at 600nm, as shown in PL spectrum Figure 5-17(a). This is very unique in the sense that traditional second harmonic effect only doubles the frequency of pump laser light, whereas in our case nanolaser light output gets frequency doubling nonlinear effect instead. This could be due to the strong nonlinear coefficient of the pure wurtzite crystal phase, but detailed theoretical analysis will be needed. To double check the second order nonlinear effect, the laser intensity at 1200nm versus the second harmonic generation (SHG) intensity at 600nm is plotted in Figure 5-17(b). The quadratic power dependence convincingly proves that the 600nm laser emission is a product of SHG.

Similar polarization experiment is also carried out to verify polarization of SHG emission, with results shown in Figure 5-18. The overall microscope image (Figure 5-18(a)) of SHG laser is shown to be a higher order mode with intensity void in the center, similar as 1200nm laser emission. However, with different polarization directions, the microscope images (Figure 5-18(b-e)) emerge as predicted by polarization description of TM polarized light in Figure 5-18(f). As the nanopillar is single crystalline wurtzite phase, the TE polarization of 1200nm laser emission and the TM polarization of 600nm SHG are determined by the selection rules dictated by the 6mm point group second-order susceptibility tensor. Wurtzie phase crystal only

has non-zero second order susceptibilities of $\chi^{(2)}_{ccc}$, $\chi^{(2)}_{caa}$ and $\chi^{(2)}_{aca}$, where c-axis is along the vertical nanopillar growth direction and a-axis is perpendicular to the vertical growth direction [77]. The TE polarized fundamental light (at 1200nm) only has polarization along a-axis. With $\chi^{(2)}_{caa}$, it will generation second harmonic light polarized along c-axis, thus forming TM polarization SHG light at 600nm. We believe this result can potentially open up new applications such as miniaturized compact green lasers integrated on silicon substrates.

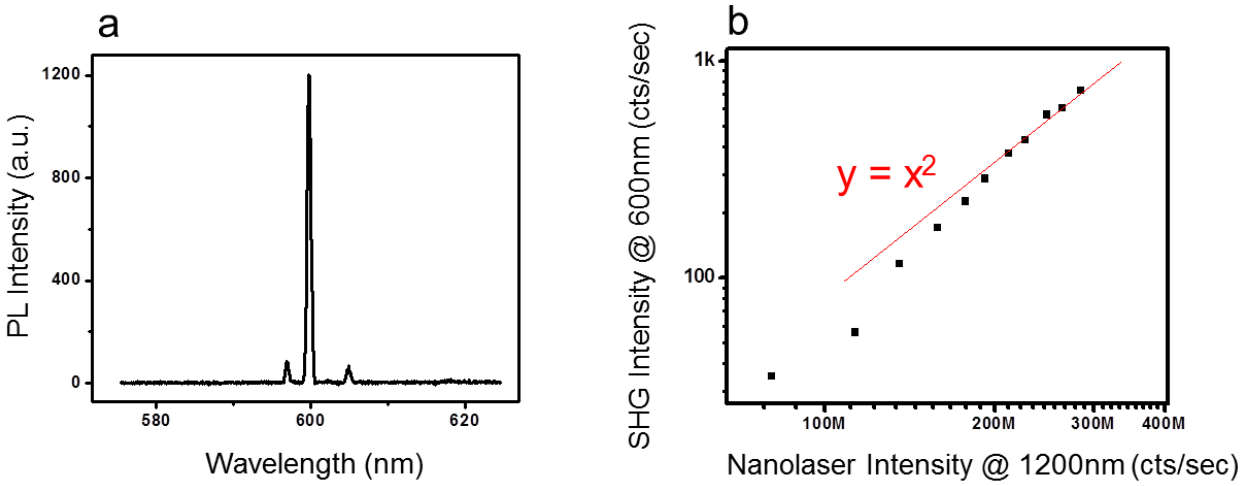

Figure 5-17 (a) Photoluminescence spectrum of the second harmonic generation, with a lasing peak at 600nm. (b) SHG intensity at 600nm versus the nanopillar laser output intensity at 1200nm. The square law relation confirms that 600nm emission comes from SHG.

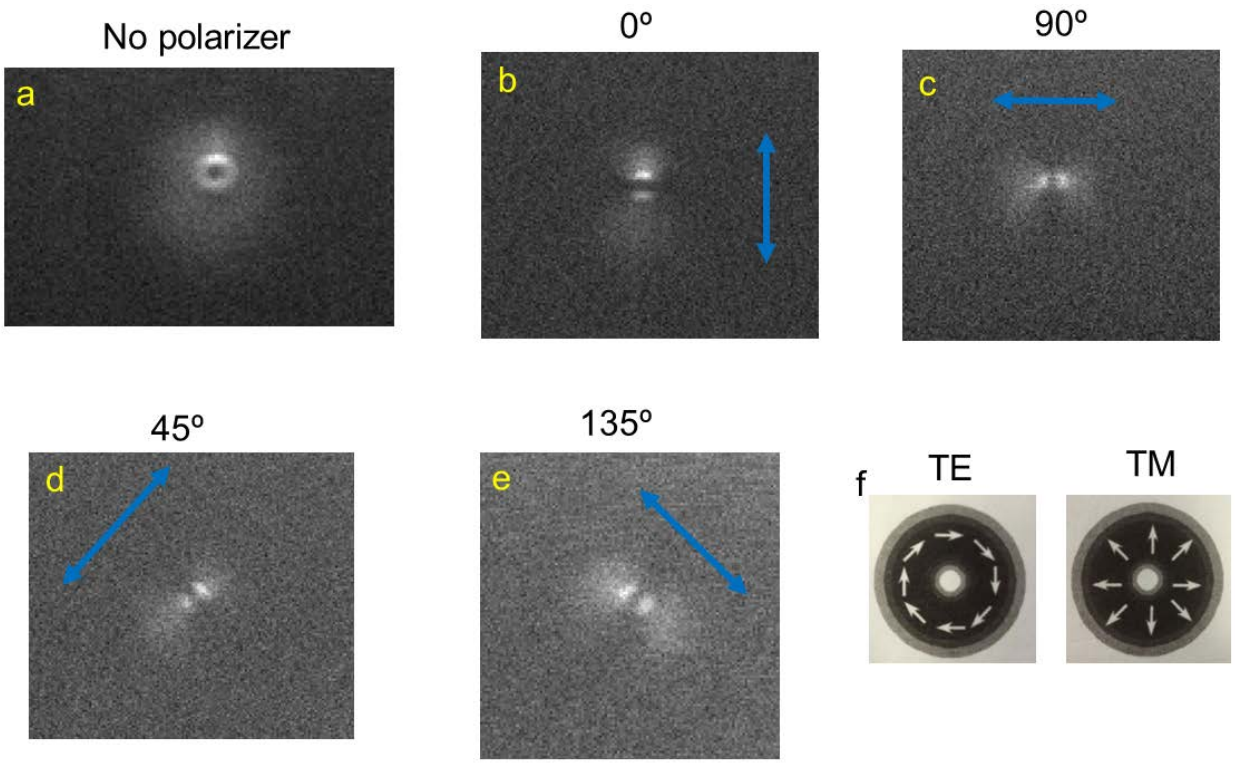

Figure 5-18 Microscope image of nanopillar second harmonic generation emission patterns with and without linear polarizer. (a) No linear polarizer; (b) Linear polarizer aligned at 0°, as indicated by the blue arrow; (c) Polarizer orientated at 90°; (d) Polarizer orientated at 45°; (e) Polarizer orientated at 135°; (f) Theoretical polarization of TE and TM modes.

5.6 Modeling of long wavelength laser

Previous sections experimentally demonstrate long wavelength nanopillar lasers with different optical cavity structures. However, to further optimize laser performance and to move towards electrically pumped device, it is crucial to understand optical gain model and cavity model behind these experimental data. Thus, detailed theoretical modeling of long wavelength laser will be performed in this section.

5.6.1 Quantum well emission

We first analyze the emission wavelength of the InGaAs quantum well sandwiched by InP barriers. The band structure is illustrated in Figure 5-19. A quantum well finite barrier model [78] is utilized to analyze this double heterostructure. However, as a first order analysis, no strain effect on the quantum well is considered at this point. Also, all used material parameters shown in Table 5-1 are based on Zincblende phase crystal due to the lack of conclusive material data of Wurtzite phase crystal. Thus, it is expected that the results might not be very accurate but they can still provide theoretical guidance for our further study.

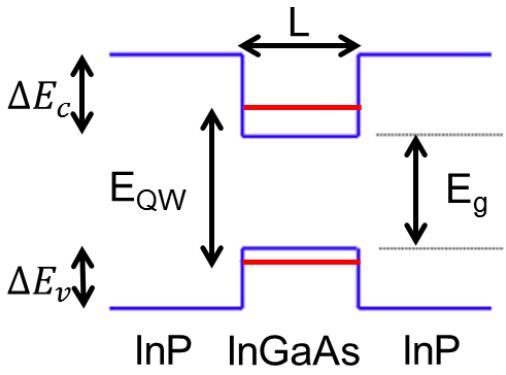

Figure 5-19 Bandgap structure of InP/InGaAs/InP double heterostructure. L is the width of InGaAs quantum well; E_g is the InGaAs material bandgap; ΔE_c is the conduction band offset; ΔE_v is the valence band offset; E_{QW} is the actual bandgap between the lowest quantized energy levels in conduction band and valence band, as illustrated in red.

Table 5-1 Material parameters of InP and InGaAs with different Ga composition x at room temperature

	InP	$In_{1-x}Ga_xAs$
Electron affinity (eV)	4.38	4.9-0.83x
Band gap (eV)	1.34	$0.36+0.63x+0.43x^2$
Electron effective mass ($\times m_0$, m_0 is the electron mass)	0.08	$0.023+0.037x+0.003x^2$
Heavy hole effective mass ($\times m_0$)	0.6	0.41+0.1x

Based on Table 5-1, the conduction band offset ΔE_c can be calculated from the difference of electron affinity between InP and InGaAs. Similar is the calculation of valence band offset. Then the lowest quantized energy levels in both conduction band and valence band can be calculated. Finally, the actual bandgap E_{QW} is the summation of InGaAs material bulk band gap and quantization energy in conduction band and valence band.

Figure 5-20(a) shows the calculated quantum well emission wavelength for $In_{0.53}Ga_{0.47}As$ (which is lattice-matched with InP) versus quantum well thickness. Quantization effect is clearly observed with emission wavelength changing versus width, especially when quantum well is thin. In particular, we evaluate the quantum well thickness inhomogeneity and how that would affect emission broadening by looking at the zoom-in TEM image of InP/InGaAs/InP single quantum well. In TEM image Figure 5-20(b), measured QW thickness varies from 4.5nm to 5.5nm. This 1nm variation in thickness result in 32nm emission wavelength shift, as seen in Figure 5-20(a). It explains the broad spectrum of single well emission in Figure 5-6 due to quantum well thickness inhomogeneity. To make quantum well thickness more uniform, further growth condition optimization will be necessary.

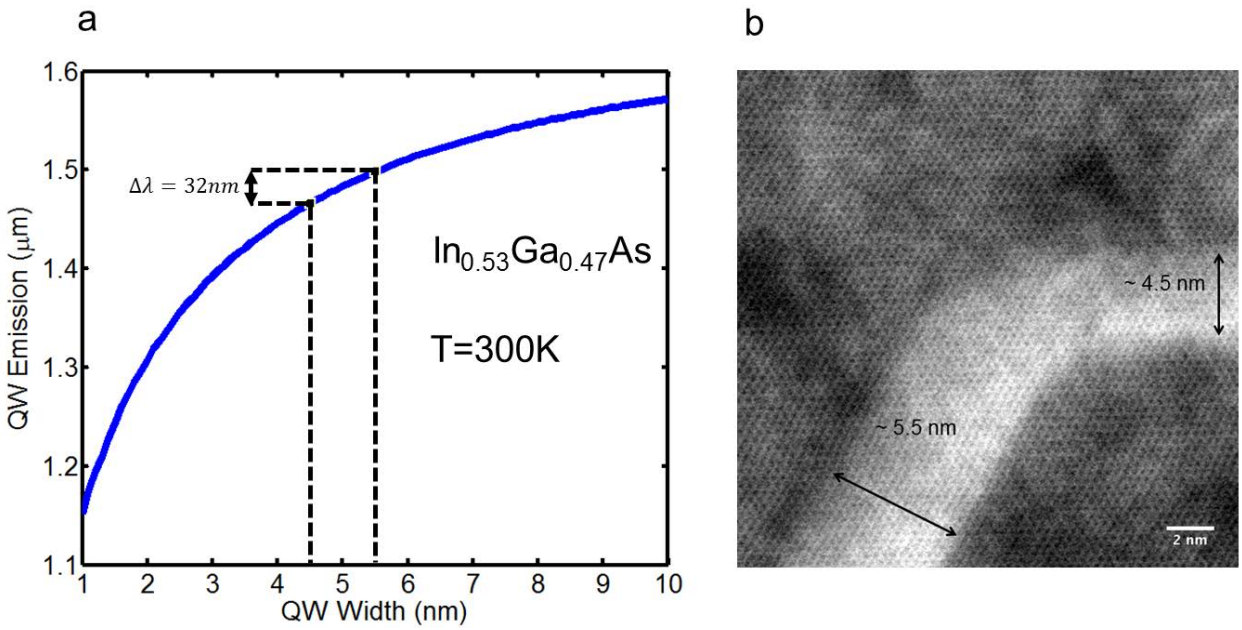

Figure 5-20 (a) $In_{0.53}Ga_{0.47}As$ quantum well emission wavelength as a function of quantum well width. (b) Zoom-in TEM image of quantum well with thickness varied from 4.5nm to 5.5nm.

In order to best match the quantization effect in PL measurement shown in Figure 5-6(b), the quantum well emission versus width at the In composition of 38% is plotted together with experimentally measured PL wavelength for different InGaAs quantum well thickness samples. The result is shown in Figure 5-21. Althought 38% InGaAs best matches the trend of experimental quantization effect, measured PL wavelength has large variation, due to both thickness inhomogeneity and composition inhomogeneity from nanopillar to nanopillar. To enable room temperature continuous wave laser and electrical pumping, growth optimization effort will be needed to reduce the inhomogeneity.

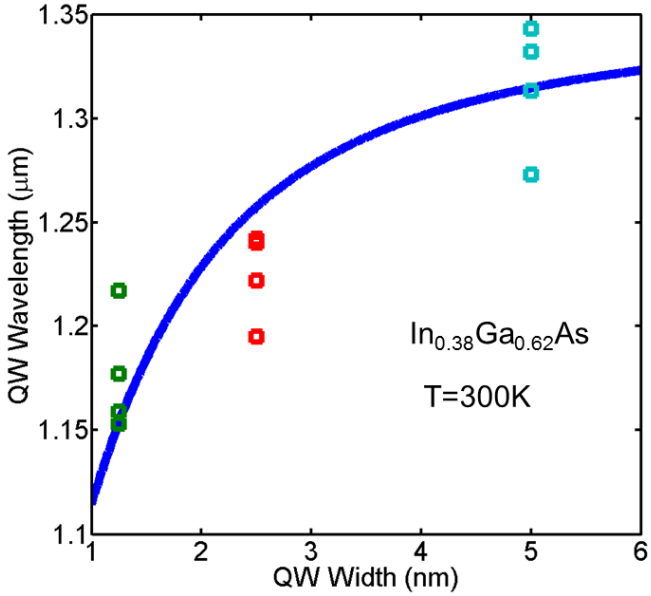

Figure 5-21 $In_{0.38}Ga_{0.62}As$ quantum well emission wavelength as a function of quantum well width, together with experimental data of PL emission wavelength for 1.25nm, 2.5nm, 5nm thick quantum wells.

5.6.2 Quantum well gain modeling

A gain model is built upon standard analysis from [78]. Based on the fundamental Fermi's golden rule describing photon generation by electron-hole recombination, a QW gain spectrum can be derived as

$$g(\hbar\omega) = \frac{\pi e^2}{n_r c \varepsilon_0 m_0^2 \omega} |M|^2 \int_0^\infty \rho_r (f_c - f_v) \frac{\hbar/\pi\tau_{in}}{(E_g + E - \hbar\omega)^2 + (\hbar/\tau_{in})^2} dE \qquad (5\text{-}2)$$

,where e, n_r, c, ε_0, m_0 and ω are elementary charge, refractive index, vacuum light speed, vacuum permittivity, electron mass and frequency of the electronic transition, respectively. M is the optical matrix element. f_c and f_v are the Fermi distribution functions for electrons and holes, respectively. ρ_r is the 2-dimensional reduced density of states for quantum well material:

$$\rho_r = \frac{m_r}{\pi\hbar^2 L_z} \sum_{n=1}^{\infty} H(\hbar\omega - E_{hn}^{en}) \qquad (5\text{-}3)$$

,where m_r is the reduced effective mass, $\hbar$ is the reduced Planck constant, L_z is the thickness of quantum well, and E_{hn}^{en} is the energy of n^{th} quantization level transition from conduction band to valence band (see section 5.6.1 for calculation of E_{hn}^{en}). Function $H()$ is a Heaviside step function.

Equation (5-3) also considers intraband scattering that in effect broadens the spectrum in actual experiments. This is done by a convolution between the unbroadened spectrum and a Lorentzian function characterized by τ_{in}. τ_{in} is the intraband carrier scattering life time and has been obtained by fitting spontaneous emission spectrum with the value around 40fs [59]. Using this value and typical material parameters for InGaAs quantum well (use 45% indium composition as an example) in Table 5-2, gain spectra can be calculated for different carrier densities, as shown in Figure 5-22.

Table 5-2 Material parameters for $In_{0.45}Ga_{0.55}As$ quantum well

m_e	$0.042m_0$
m_h	$0.455m_0$
m_r	$0.038m_0$
$E_p \left(\lvert M\rvert^2 = \frac{m_0 E_p}{6}\right)$	23.78eV

E_g	0.82eV
τ_{in}	40 fs
n_r	3.7
L_z	5 nm

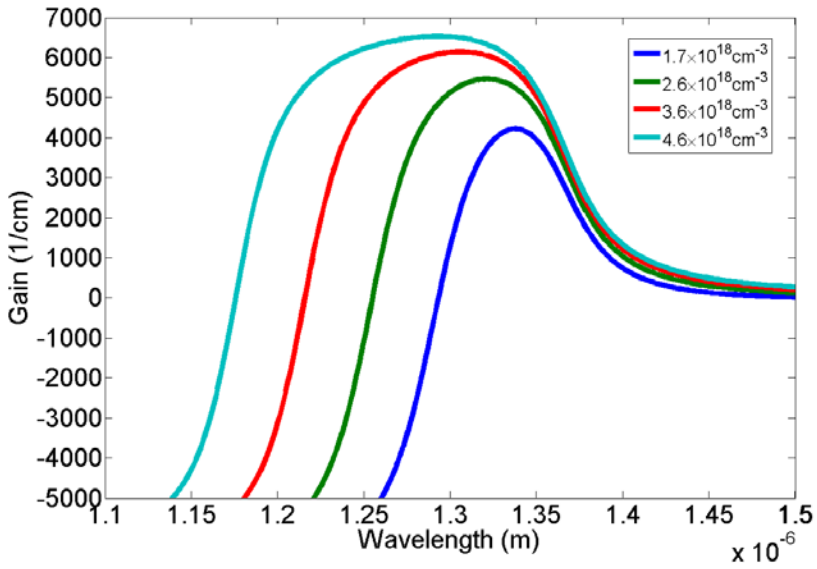

Figure 5-22 Gain spectra of InGaAs quantum well for different carrier densities at T=4K. The gain has been calculated for a temperature of 4 K since most experiments are performed at cryogenic temperatures in a cryostat

Now that gain spectra under different carrier densities are obtained, the maximum gain versus carrier density is plotted in Figure 5-23. We further fit this curve using a logarithmic gain model:

$$g(N) = g_0 \ln\left(\frac{N}{N_{tr}}\right) \qquad (5\text{-}4)$$

, where N_{tr} has a physical meaning of transparency carrier density. The fitted parameters are $g_0 = 3100cm^{-1}$, and $N_{tr} = 5 \times 10^{17}cm^{-3}$. Compared to the bulk InGaAs gain model [59], quantum well gain model demonstrates higher gain at the same carrier density level but higher transparency carrier density.

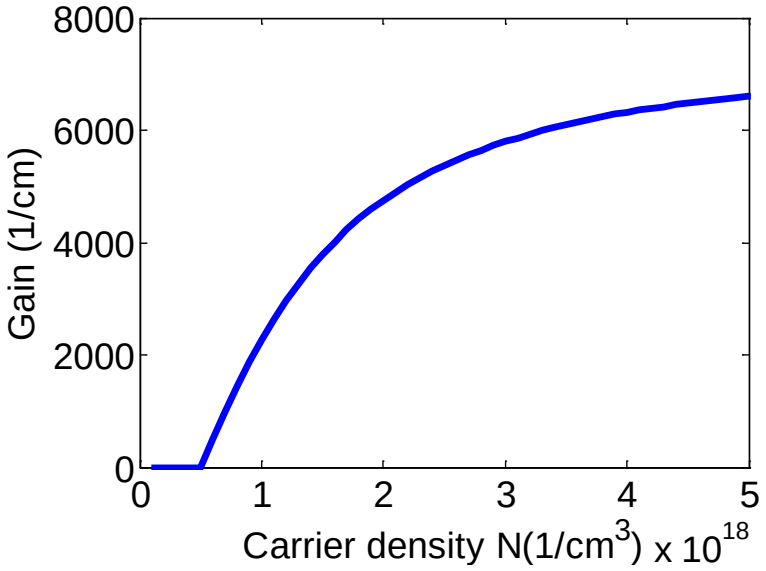

Figure 5-23 Quantum well maximum gain versus carrier density. It is fitted by a logarithmic gain model

5.6.3 Lasing threshold analysis

Able to generate quantum well gain model, we can further analysis the lasing threshold condition for quantum well laser and evaluate how certain key parameters affect the lasing threshold. Multiple quantum well threshold condition is given by [78]:

$$\mathrm{n_w} \times \Gamma_\mathrm{w} \times \mathrm{g_w}(\mathrm{N_{th}}) = \frac{\omega}{\mathrm{v_g Q}} \qquad (5\text{-}5)$$

On the left side of equation is the total gain, where n_w is number of quantum wells, Γ_w is the confinement factor for each quantum well, and g_w is the gain for each quantum well and is a function of carrier density. On the right hand side is the total loss, define by the group velocity v_g and cavity quality factor Q. Next, we substitute gain model equation (5-4) into equation (5-5) and obtain the threshold carrier density N_{th}:

$$\mathrm{N_{th}} = \mathrm{N_{tr}} \times \exp\left(\frac{1}{\mathrm{n_w \Gamma_w g_0}} \times \frac{\omega}{\mathrm{v_g Q}}\right) \qquad (5\text{-}6)$$

Finally, threshold lasing current J_{th} under electrical injection can be obtained:

$$\mathrm{I_{th}} = \mathrm{A} \times \mathrm{n_w} \times \mathrm{L} \times \mathrm{q} \times \frac{\mathrm{N_{th}}}{\eta \times \tau} \qquad (5\text{-}7)$$

, where A is the electrical injection area, L is the quantum well width, η is the carrier injection efficiency and τ is the carrier lifetime.

For traditional quantum well edge emitting laser, optical confinement factor Γ is defined in a straightforward fashion because its lasing transverse mode is the waveguide fundamental mode:

$$\Gamma_0 = \frac{\int_{\text{active region}} |\mathrm{E}|^2 \mathrm{dxdy}}{\int_{\text{everywhere}} |\mathrm{E}|^2 \mathrm{dxdy}} \qquad (5\text{-}8)$$

However, for nanopillar structure, optical confinement factor Γ_w is a non-trivial parameter to obtain due to the multiple-mode nature of nanopillar. Figure 5-24 are the mode patterns of the first few transverse modes of hexagonal cross section with 0.8μm diameter. These modes are distinct from each other and have very different confinement factors. So the key question is: which mode is the lasing mode? Intuitively, in the situation of transferred nanopillar, the mode that has the highest reflection at the nanopillar-air interface should construct the highest Q cavity and thus has the highest probability of lasing. Therefore, 3-dimensional FDTD simulation is performed to calculate the reflection when the modes hit the interface between nanopillar and air. The fundamental HE_{11} mode has a reflection of 29.7%, which is consistent with the ray optics approximation $(n-1)^2/(n+1)^2$. Surprisingly, higher order modes possess a much higher reflection: TE_{01} mode has 66.7%; HE_{21} mode has 39.7%; TM_{01} mode has 68.9%. This is consistent with mode reflection analysis of nanowire laser [79]. The unique reflection property for nanostructure can be attributed to the fact that higher order modes have higher mode mismatch with eigenmodes in air and thus induce higher reflection. Based on interface reflection, TE_{01} and TM_{01} modes are the best candidates for lasing. However, from Figure 5-16(a), TE_{01} mode pattern best matches the microscope image of experimental mode pattern, so we consider TE_{01} mode the actual lasing mode in our later analysis.

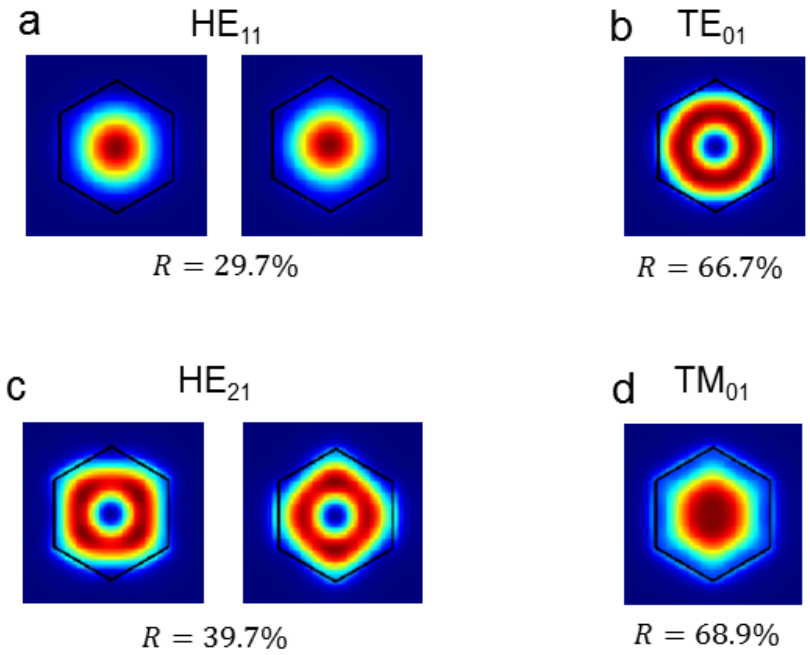

Figure 5-24 Mode patterns of the first few transverse modes of hexagonal cross section. The border of nanopillar is outlined in black. The diameter of the heagon is 0.8μm, while

the wavelength of the modes is around 1.3μm. (a) Two degenerate HE_{11} modes with 29.7% reflection at the semiconductor-air interface; (b) TE_{01} mode with 66.7% reflection; (c) Two degenerate HE_{21} modes with 39.7% reflection; (d) TM_{01} mode with 68.9% reflection.

Further complicating calculation of optical confinement factor, it has been studied that the definition of nanostructure's optical confinement factor is slightly different from bulk laser [80]:

$$\Gamma = \frac{n_g}{n}\Gamma_0 \qquad (5\text{-}9)$$

, where n_g is the group index of gain material, n is the refractive index of the background gain medium, and Γ_0 defined in equation (5-8) is the ratio of the energy in the active region to the energy in the entire cavity, or the conventional definition of confinement factor. The role of group index n_g in equation (5-9) can be understood that if the mode travels with a slower group velocity (i.e., higher group index), it is interacting with the gain medium more and thus has higher overlap with gain region. This is especially important when we evaluate higher order modes because higher order modes usually possess high group index. With FDTD simulation, the optical confinement factors for different modes are plotted in Figure 5-25. It is expected that the confinement factor varies with quantum well position because of the mode intensity distribution inside nanopillar, so the curves are plotted versus quantum well position from the center. Note that the radius of the nanopillar is 0.4μm. With their mode patterns plotted on the side, the first four modes are evaluated: HE_{11} mode, TE_{01} mode, HE_{12} mode and TM_{01} mode. In this figure, TE_{01} and HE_{12} modes, with donut shape field pattern, have their maximum Γ when quantum well is positioned closer to nanopillar edge, whereas HE_{11} and TM_{01} modes have their maximum Γ when quantum well is closer to center. In addition, TE_{01} and HE_{12} modes have higher maximum Γ of 2.7% or so, because the hexagon ring of quantum well better match the field intensity maxima of donut shape field pattern. We will use this Γ_w=2.7% in equation (5-6) since the lasing mode is TE_{01} mode.

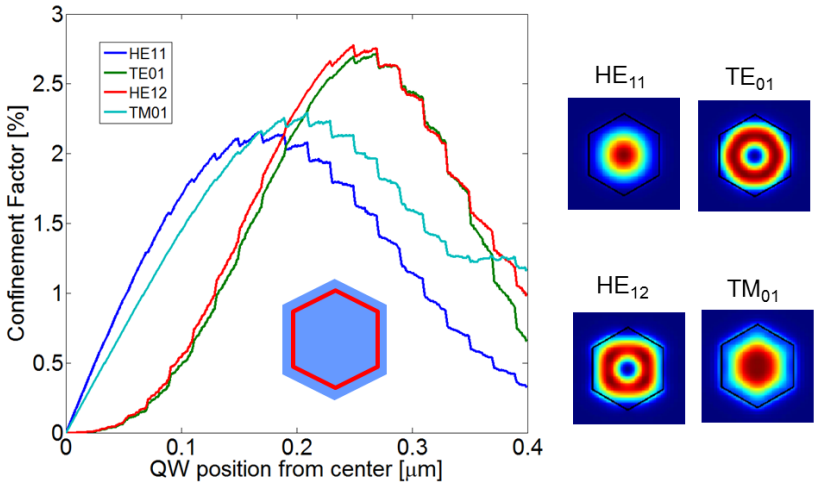

Figure 5-25 Optical confinement factors for different modes as a function of quantum well position. The inset illustrates quantum well (in red) position in nanopillar in cross

section view. The first four modes of hexagonal cross section are evaluated: HE_{11}, TE_{01}, HE_{12} and TM_{01}.

Coming back to our purpose of analyzing threshold current density I_{th} based on equation (5-7), we use some typical parameters reported in literature and other parameters that are based on our previous analysis, as shown in Table 5-3. Note that the current injection area A is the total surface area of a typical nanopillar structure with 6um height, 800nm bottom diameter and 400nm top diameter.

Table 5-3 Parameters for calculation of threshold current density I_{th}

Lasing wavelength λ	1.3μm
Group index n_g	4.2
Quantum well thickness L	5nm
Confinement factor Γ_w	2.7%
Transparent carrier density N_{tr}	$5 \times 10^{17} cm^{-3}$
g_0	$3100 cm^{-1}$
Current injection efficiency η	10%
Carrier lifetime τ	4ns
Current injection area A	$1.13 \times 10^{-11} m^2$

With the parameters listed in Table 5-3, assuming that number of quantum wells incorporated n_w is 5, the relation between threshold current I_{th} and cavity Q can be plotted in Figure 5-26. It can be seen that nanopillar cavity needs to have a Q of at least 200 to achieve sub-milliampere lasing operation. With higher cavity Q, the threshold current reduces; however, Q factor beyond 500 does not significantly decreases threshold current. Thus, we aim to design a nanopillar optical cavity with roughly 500 Q factor to achieve lasing behavior.

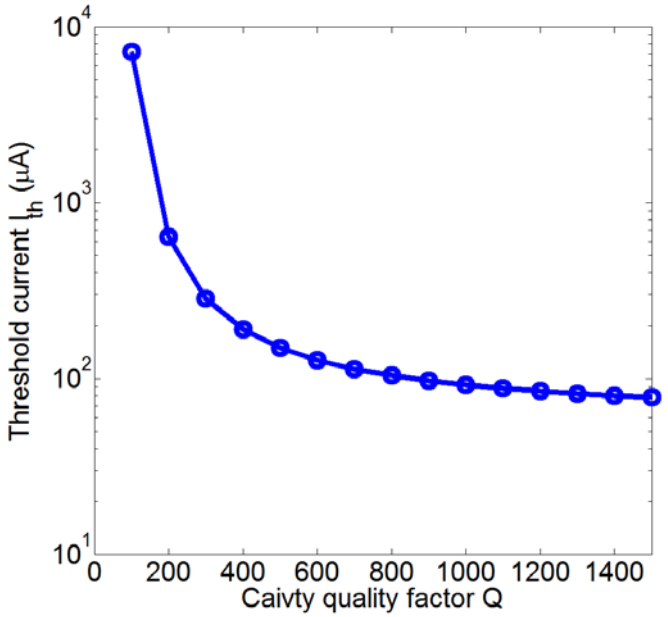

Figure 5-26 Threshold current as a function of cavity quality factor Q. The nanopillar laser structure has 5 quantum wells inside.

Relation between lasing threshold and number of quantum wells can be also studied. Assuming a Q factor of 500, Figure 5-27 shows the threshold current with different number of quantum wells. When there is only single quantum well inside, threshold carrier density N_{th} skyrockets because $N_{th} \propto exp\left(\frac{1}{n_w}\right)$. On the other hand, when there are more than 5 quantum wells, threshold current also increases because $I_{th} \propto n_w$. Thus, the optimum number of quantum wells is between 3 quantum wells and 5 quantum wells. This trend agrees well with conventional quantum well lasers [78].

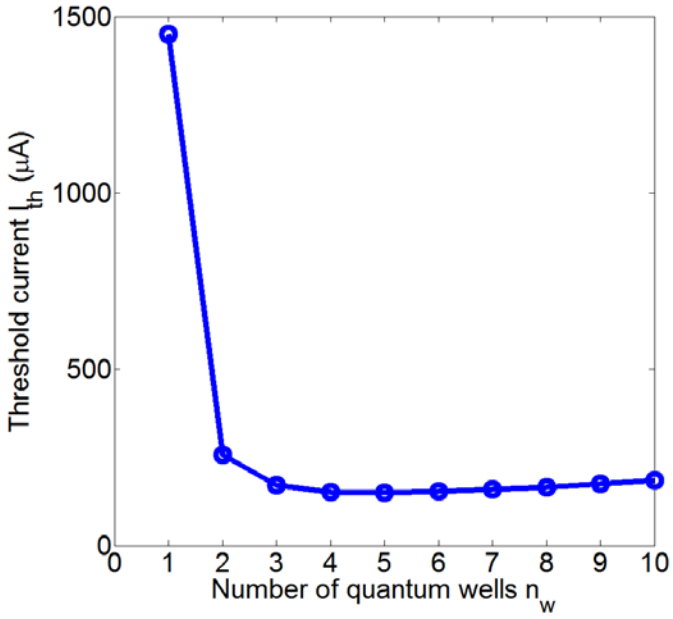

Figure 5-27 Threshold current as a function of number of quantum wells. An optical cavity Q factor of 500 is assumed in the plot.

5.6.4 Hakki Paoli analysis

The typical Fabry-Perot cavity spectra in transferred nanopillar laser (Figure 5-7(a)) offers a possibility of analyzing the optical gain experimentally. Based on the method proposed by Hakki and Paoli [81], gain spectra can be obtained by measuring the depth of modulation, caused by the Fabry-Parot resonance, in the emission spectrum. The depth of modulation r_i is defined as:

$$\mathrm{r_i} = \frac{\mathrm{P_i}+\mathrm{P_{i+1}}}{2\mathrm{V_i}} \qquad (5\text{-}10)$$

, where P_i and P_{i+1} are two consecutive peak values of a Fabry-Perot spectrum, and V_i is the intermediate valley value.

The corresponding net gain G_i is obtained from:

$$\Gamma\mathrm{G_i} = \frac{1}{\mathrm{L}}\ln\left(\frac{\mathrm{r_i^{\frac{1}{2}}}+1}{\mathrm{r_i^{\frac{1}{2}}}-1}\right) + \frac{1}{\mathrm{L}}\ln\mathrm{R} \qquad (5\text{-}11)$$

,where Γ is the optical confinement factor, L is the Fabry-Perot cavity length, and R is the mirror reflectivity. For the transferred nanopillar laser with Fabry-Perot behavior, the length of nanopillar is measured to be 11.7μm, i.e. $L = 11.7\mu m$. Assuming the lasing transverse mode is HE_{11} mode in transferred nanopillar, the reflectivity R is 29.7% based on mode simulation results shown in Figure 5-24. Figure 5-28 shows the extracted modal absorption spectra under different optical pump power readouts based on Hakki-Paoli method. The positive side of vertical axis represents modal absorption ($\Gamma\alpha_i$), while the negative side represents modal gain (ΓG_i). It is obvious that all the curves intersect horizontal axis at approximately λ=1430nm, indicating the band gap edge wavelength is 1430nm. As pump power increases, optical gain becomes higher and gain bandwidth becomes larger, all consistent with theoretical gain spectra analysis [78]. The threshold pump power for lasing is 40mW based L-L curve. From Figure 5-28, at the threshold lasing power of 40mW, the maximum modal gain is 300cm^{-1} at the wavelength of 1300nm or so (which is indeed the lasing mode wavelength). Thus, we conclude that $\Gamma g_{th} = 300cm^{-1}$. Further, optical cavity Q can be obtained from:

$$\Gamma\mathrm{g_{th}} = \alpha = \frac{2\pi\mathrm{n_g}}{\lambda\mathrm{Q}} \qquad (5\text{-}12)$$

Using values from Table 5-3, Q is calculated to be 677.

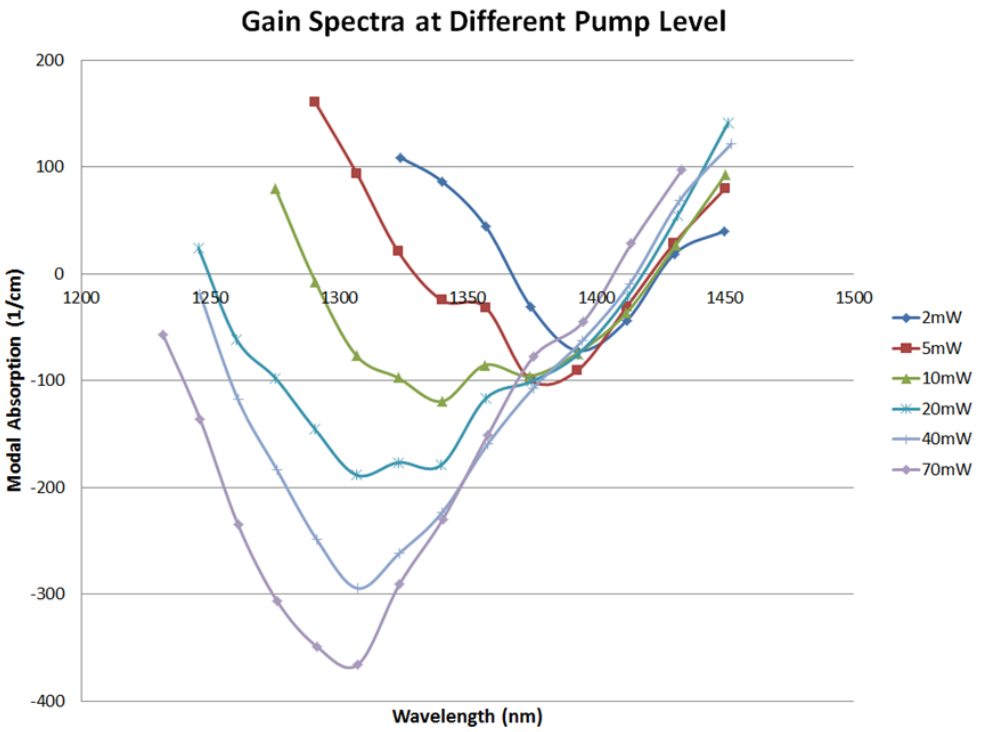

Figure 5-28 Modal absorption spectra under different optical pump power based on Hakki-Paoli method. The negative side of vertical axis means modal gain, while the positive side means modal absorption.

5.7 Summary

In conclusion, we have explored two strategies of making long wavelength nanopillar laser with emission transparent to silicon. The first one is built upon the InGaAs graded core-shell structure to gradually increase indium composition to achieve 1.1μm wavelength laser. However, this method is fundamentally limited by the lattice mismatch induced strain and cannot readily scale to telecommunication wavelength such as 1.55μm.

The other strategy is based on InP/InGaAs/InP double heterostructure, where InGaAs layer presents itself as thin quantum well to minimize strain. As the active gain material, multiple InGaAs quantum wells were proved to be of superior quality by high resolution TEM. Quantum wells also enable convenient wavelength tuning by adjusting the quantum well indium composition and QW thickness. Thanks to its unique core-shell growth mode, nanopillar can scale its large diameter up to micrometer size without introducing any defects, leading to large optical cavity to confine photons at long wavelength. Nanolasers with three different types of optical cavities are subsequently demonstrated. Inspired by nanowire lasers, transferred InP/InGaAs/InP nanopillar lying down on extrinsic substrate (sapphire in our case) is a natural horizontal Fabry-Perot resonator. Thus, optically-pumped laser oscillation is obtained with clear Fabry-Perot attributes. By growing nanopillar on SOI substrate, a vertical Fabry-Perot cavity is created with bottom mirror enhance by Si-SiO2 interface of SOI substrate. Therefore, as-grown nanolasers are achieved at different wavelength ranging from 1.1μm to 1.3μm. Another novel

cavity structure takes advantage of silicon selective etching to create silicon undercut to enhance bottom reflection. Not only 1200nm nanolaser is achieved, but its strong second harmonic effect generates a 600nm laser emission.

Finally, theoretical study on optical gain model and cavity mode behind these long wavelength nanolaser results is performed, for the sake of further optimizing laser performance and moving towards electrically pumped device.

Chapter 6 Electrically-driven Nanopillar Devices

So far, nanolaser integration with CMOS electronics and silicon photonics has been demonstrated. The next step is undoubtedly transitioning from optically-activated laser towards electrical-driven devices. This involves doping control, device structure design and fabrication process. Needless to say, it is extremely challenging for nano-devices. In this chapter, we will discuss our effort of tackling these technical barriers and some preliminary results of electrically-injected nanopillar devices.

6.1 Ensemble nanopillar LED and APD

As a first step, ensemble nanopillar devices, with electrical current injecting into multiple nanopillars, are first developed [82]. Thanks to its core-shell growth mode, nanopillar can form radial n-i-p structure with in-situ doping on n-doped Si substrate, as shown in Figure 6-1. The reverse p-i-n nanopillar structure on p-doped Si can be obtained similarly. The in-situ doping is achieved with diethylzinc (DEZn) as acceptor source and diethyltellurium (DETe) as donor source.

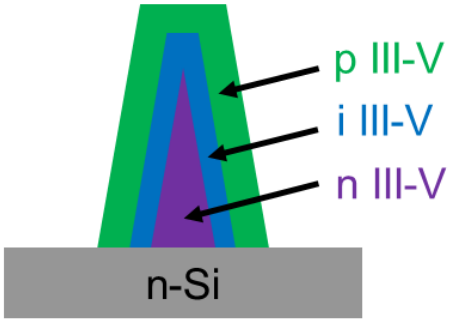

Figure 6-1 Schematic of an as-grown n-i-p III-V nanopillar on n-doped silicon substrate.

The device structure for ensemble nanopillar-based light emitting diode is shown in Figure 6-2(a). A spin-on-glass (SOG) layer is put on substrate to isolate metal contact from silicon substrate. Subsequently, top contact metal is deposited at a tilted angle such that one side of nanopillar can emits light under forward bias. The other contact is on the bottom of n-doped silicon substrate. Electrical measurement on these GaAs-nanopillar-based ensemble devices confirms diode-like I-V curve as in Figure 6-2(b). It is a proof that in-situ doping successfully forms a nanopillar diode.

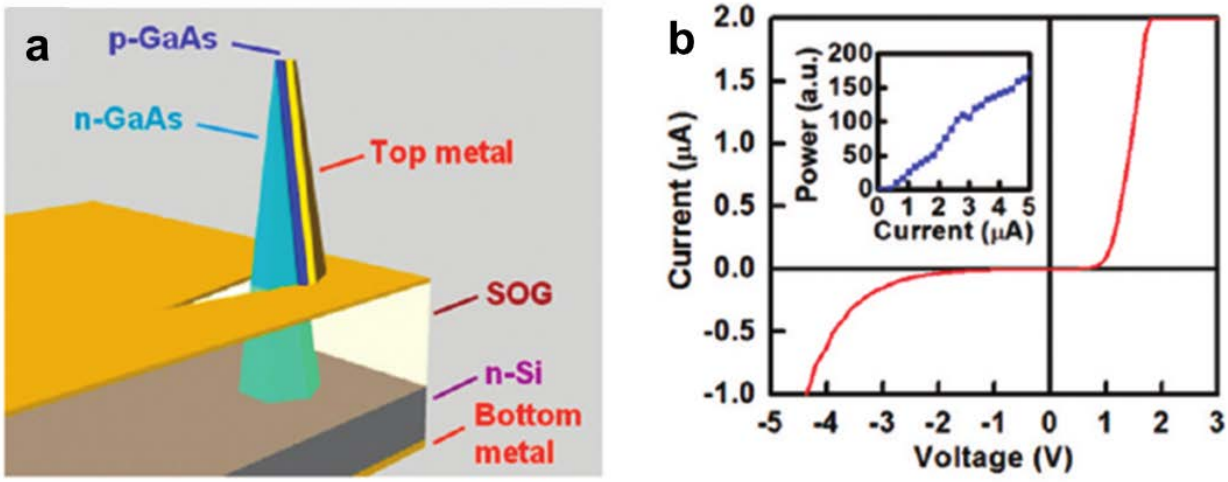

Figure 6-2 Ensemble nanopillar-based light emitting diode. (a) Schematic of device structure. (b) Device I-V curve with the inset showing emission optical power versus forward bias current level.

6.2 Shunt path minimization for single-pillar device

To achieve nanolasers on silicon, electrically-driven device based on single nanopillar is necessary. With the aid of electron-beam lithography technique, fabrication process has been developed to register position of single nanopillar and to make metal contact on it [83]. However, the most challenging fabrication issue turns out to be how to remove the shunt path from the shell of nanopillar to the silicon substrate, as illustrated in Figure 6-3. Ideally, we expect the electrical current to flow through p-type III-V, intrinsic III-V, n-type III-V, and finally into n-type Si substrate. Yet, since p-dope III-V nanopillar shell directly sits on n-dope silicon, current has the option to directly flow from p-shell to n-substrate. This current shunt path reduces electron-hole recombination in intrinsic III-V layer and is detrimental to performance of nanolasers as well as other optoelectronic devices. Three methods have been explored to minimize the effect of shunt path.

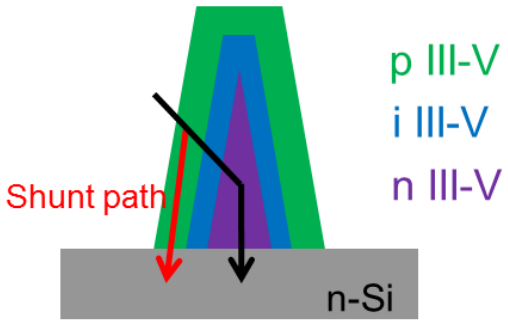

Figure 6-3 Schematic illustrating current shunt path from p-doped III-V nanopillar shell to n-doped silicon substrate. The black arrow is the ideal current path, while the red arrow indicates the shunt current path.

6.2.1 III-V shell etching

The most intuitive way to kill the current shunt path is to etch away the p-doped III-V shell at the bottom of nanopillar, as shown in Figure 6-4. As an example, dry etching ($SiCl_4$ gas) and 1:1:30 H_2SO_4:H_2O_2:H_2O have been used to etch (In)GaAs material. By proper etching time, nanopillar shell can be removed completely. The detailed process can be found in reference [84].

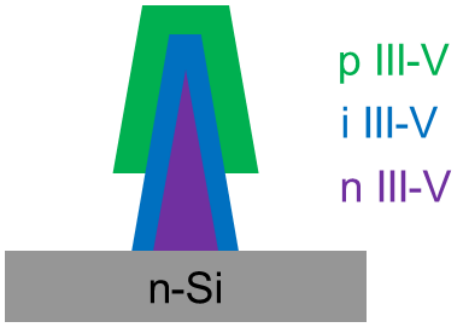

Figure 6-4 Schematic of a III-V nanopillar with p-shell etched at the bottom.

Using this method, InGaAs nanopillar diode has been successfully fabricated. Figure 6-5(a) is the I-V curve of the device in semi-log scale, showing a typical diode behavior. Furthermore, electroluminescence (EL) experiment is carried out and resonance mode peaks are observed in the spectra under different pumping current, as shown in Figure 6-5(b). Electrically-pumped lasing is not obtained yet, due to the need of further optimization of optical cavity and metal thickness.

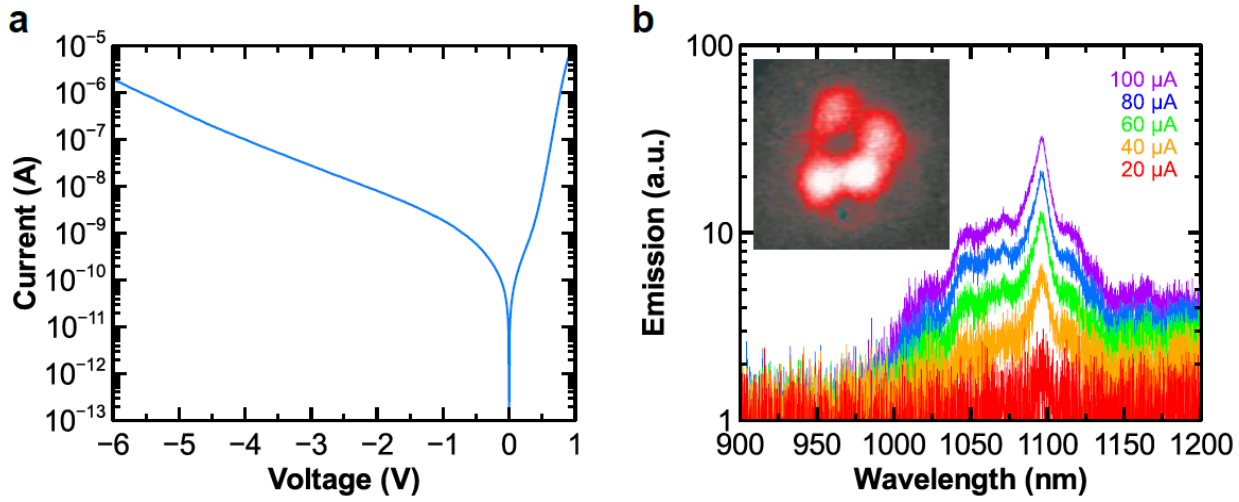

Figure 6-5 Characterization of InGaAs nanopillar diode with III-V shell etching. (a) Diode I-V curve. (b) Electroluminescence (EL) spectra under different pumping current. The inset is the microscope image of nanopillar EL emission.

This method, however, has some limitations. First, etching process on the III-V shell will leave surface defects on the nanopillar and increase undesired surface non-radiative recombination.

Also, etching of wurtzite phase InP turns out to be inefficient and uncontrollable, limiting this method's application in InP nanopillar devices.

6.2.2 Regrowth

The other strategy to remove shunt path is to utilize "regrowth", or secondary growth to avoid III-V shell contacting substrate. It involves two growth steps, is illustrated in Figure 6-6. The initial growth step only has n-doped III-V core and intrinsic shell. Then a mask layer is deposited everywhere except the top portion of nanopillar. Finally, the regrowth is performed to grow the p-doped region to avoid contacting the substrate.

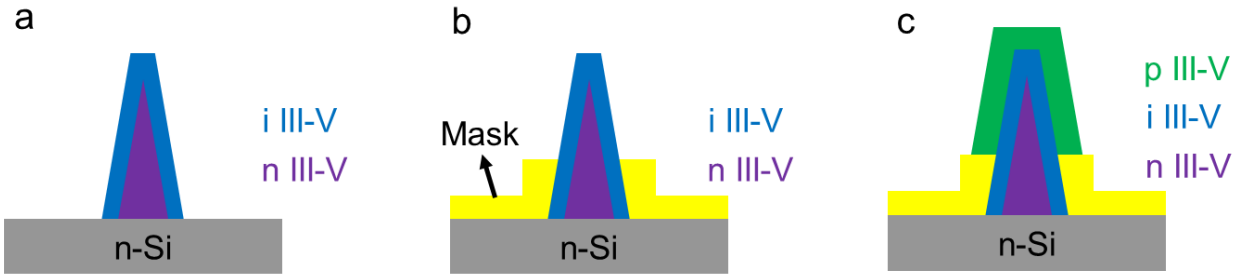

Figure 6-6 Regrowth process of III-V nanopillar. (a) Initial growth of nanopillars consisting of n-doped core and intrinsic shell. (b) Mask material covering everywhere except the top of nanopillar. (c) Regrowth of p-doped III-V to avoid contacting substrate.

We have used the regrowth method with InP nanopillars, where the optimum mask material is one layer of SiO_2 followed by one layer of amorphous silicon. Figure 6-7(a) shows the SEM image right before regrowth, where the bottom portion of InP nanopillar is covered by SiO_2 and amorphous silicon mask. After the regrowth, as shown in Figure 6-7(b)-(c), the upper portion of nanopillar becomes larger while maintaining smooth surface, indicating high quality quality.

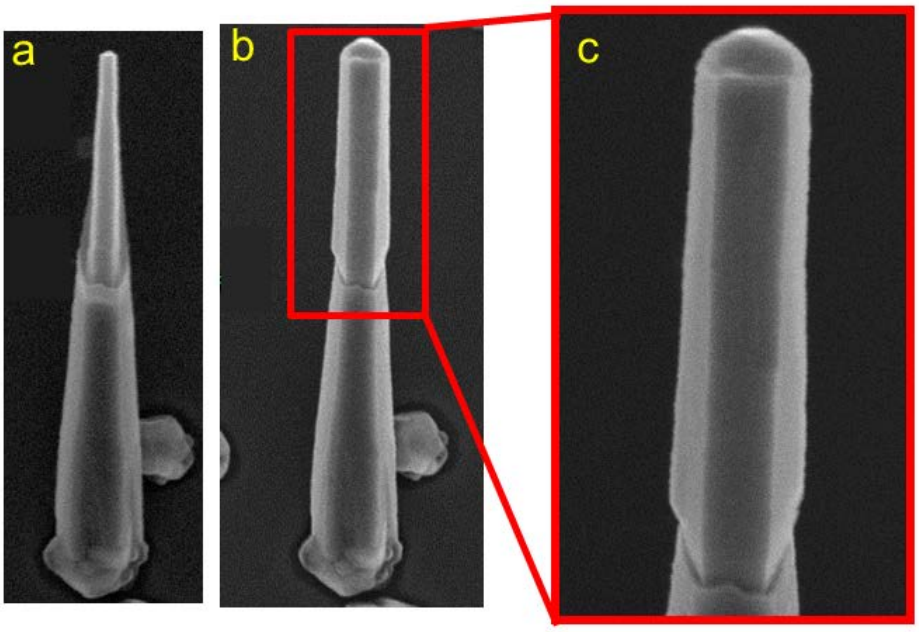

Figure 6-7 SEM images of InP nanopillar regrowth result. (a) SEM image of a nanopillar right before regrowth. (b) SEM image of the same nanopillar after regrowth. (c) Zoom-in SEM image of the regrowth portion.

Based on regrowth, InP nanopillar diode is fabricated. Figure 6-8 shows the I-V curve of regrowth diode structure, as well as that of nanopillar without regrowth. The regrowth structure I-V is much more close to ideal diode I-V curve, with a record low dark current of 10^{-14}A due to the minimized shunt path effect.

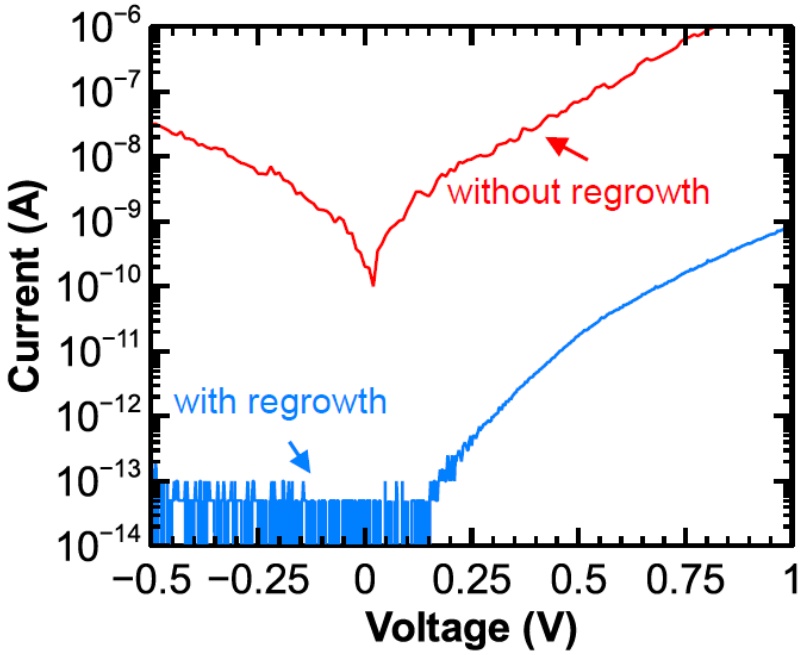

Figure 6-8 I-V curves of InP diodes with (blue curve) and without (red curve) regrowth structure.

6.2.3 Si undercut etching

Si undercut structure, aforementioned in section 5.5, also has the capability of killing the current shunt path, as shown in Figure 6-9. By etching away the silicon underneath the nanopillar, p-doped is no longer in contact with silicon substrate, thus killing the shunt path. The details about Si undercut etching process have been discussed in section 5.5.

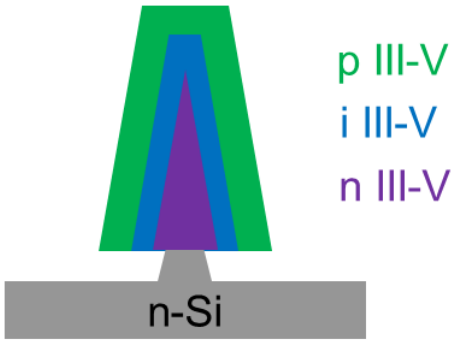

Figure 6-9 Schematic of a Si undercut nanopillar structure.

To prove the effect of Si undercut etching, I-V curves are measured on undercut devices and non-undercut devices for comparison. The results are plotted in Figure 6-10. It is obvious that without silicon undercut, the shunt path makes the I-V curve more symmetric and results in large leakage current under reverse bias. In contrast, with the help of Si undercut, I-V curve shows prominent rectifying behavior and has much lower dark current.

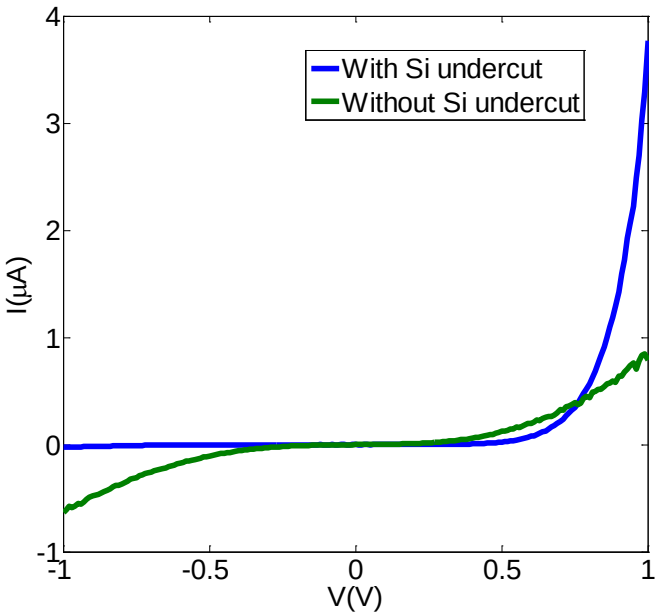

Figure 6-10 I-V curves of InP nanopillar diodes with (blue curves) and without (green curve) Si undercut.

6.3 On-chip optical link

With the capability of making electrical contact on nanopillar diode devices, including both light emitter and photodetector [82], we move forward and build a proof-of-concept optical link on silicon substrate [83]. As shown in Figure 6-11(a), two nanopillars are contacted by metal and connected by polymer waveguide. One of the nanopillar is the nano-emitter, which convert electrical signal into optical signal. Then the optical signal coupled into the polymer waveguide and propagates towards the other end of waveguide. The other nanopillar device serves as the nano-detector, converting received optical signal into electrical signal. This resembles the architecture of a full optical link based on nano-resonator devices. Figure 6-11(b) is the SEM image of finished nanopillar based optical link. The two ends of polyer waveguide have taper such that the coupling between nanopillar and waveguide can be maximized. It is worth noting that both nano-emitter and nano-detector are half coated by metal and the optical windows for both needs to face to each other for this link to function.

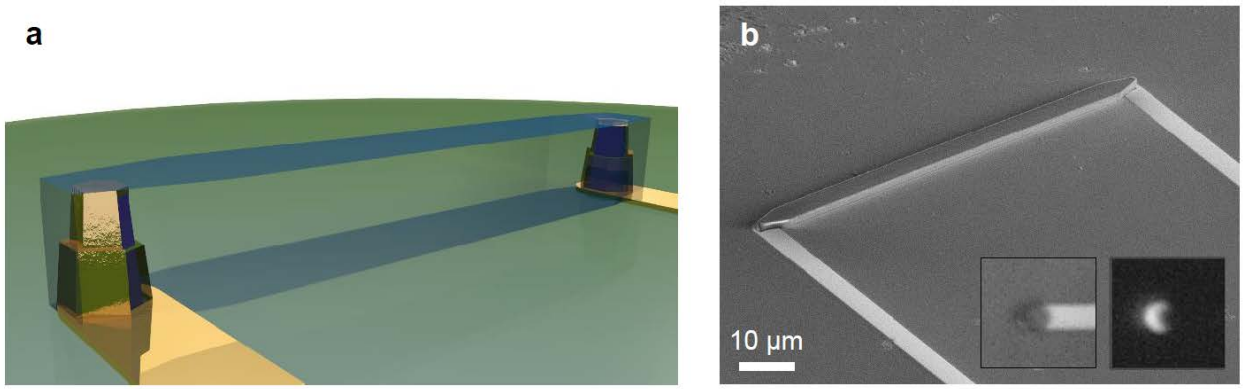

Figure 6-11 Optical link based on nanopillar devices on silicon. (a) Schematic of two nanopillar devices connected by polymer waveguide on silicon. (b) SEM image of an optical link on silicon. The inset is the microscope image of the nanopillar emitter and its light emission pattern.

The characterization of this optical link involves modulating the nano-emitter with certain electrical signal and detecting the nano-receiver for any response. Figure 6-12 is the nano-photodetector signal when nano-LED is modulated under dc or ac condition. Clearly, the signal has been successfully transmitted from sender to receiver. This is the first optical link demonstration on silicon substrate.

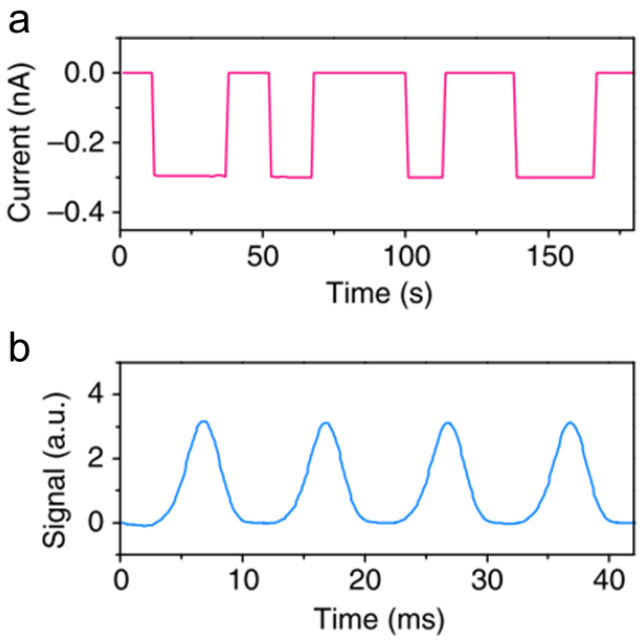

Figure 6-12 Optical link data transmission demonstration. (a) Photocurrent detected by the nano-receiver when nano-LED is turned on and off. (b) Signal received by the photodiode when a 100Hz signal is sent by the LED.

6.4 Summary

In summary, ensemble devices are fabricated with in-situ doped nanopillar diode structure. Furthermore, three different methods are explored to solve the current shunt path problem when fabricating single nanopillar devices. All three methods lead to significant reduction of shunt path current leakage and can be applied in different situations. Finally, a full functional optical link has been demonstrated with InGaAs nanopillar devices and polymer waveguide, serving as a proof of concept that our nanopillars have the potential to empower on-chip optical interconnects.

Chapter 7 Conclusion

On-chip optical interconnect has the great expectation of empowering faster-speed and lower-energy next generation computing. Hopefully, this dissertation has delivered a convincing message that III-V nanolaser is very promising to become the on-chip light source, the most critical component for interconnect.

The story started our unique superior quality III-V nanopillar growth on silicon at low growth temperature with no metal catalyst. Based on experimental observations, a hypothesis was made that nanopillar nucleation was initiated by metal nanocluster and surface roughness. Both mechanical roughening and chemical roughening sample preparation methods confirmed this hypothesis and successfully nucleated InGaAs and InP nanopillars. With these understandings, nanopillar growth site control was achieved by patterning Si substrate with SiO_2 mask. The nanopillar growth was proved to be very controllable due to its core-shell growth mode. And the nanopillar crystal has no twinning defect since all dislocations are contained at the root. Hence, as-grown nanopillar's lasing behavior under optical pumping at room temperature was obtained, thanks to the 3D whispering gallery optical mode.

Using this unique low-temperature and catalyst-free nanopillar growth technique, we demonstrated the first nanolasers monolithically grown on silicon-based MOSFETs. Excellent lasing performance was obtained at room temperature. More importantly, the group III-V nanopillar growth process had almost no influence on the performance of the transistors, and showed great promise as a CMOS-compatible growth method.

We further discussed the prospect of integrating nanopillar laser with silicon photonics. The cornerstone of this is the unique horizontal nanopillar growth on Si (110) or SOI (110) substrate, enabled by anisotropic Si etching technique. Lasing oscillation confirmed the good quality of horizontal nanopillars. End-fire coupling between horizontal nanopillar laser and Si waveguides was directly proved by etching Si 45º inclined facet and micro-PL experiment thereafter. The coupling efficiency was calculated to be as high as 13%. Horizontal nanopillar growth was also achieved on (110) SOI substrate, where buried oxide can greatly enhance bottom light confinement. In addition, horizontal nanopillar enabled a novel class of cavity resonator designs, such as external DBR cavity and double Si-fin cavity.

Also, we have explored two strategies of making long wavelength nanopillar laser with emission transparent to silicon. The first one is to use InGaAs graded core-shell structure to gradually increase indium composition to achieve 1.1μm wavelength laser. However, this method is fundamentally limited by the lattice mismatch induced strain and cannot readily scale to telecommunication wavelength such as 1.55μm. The other strategy is based on InP/InGaAs/InP double heterostructure. As the active gain material, multiple InGaAs quantum wells were proved to be of superior quality by high resolution TEM. Quantum wells also enabled convenient wavelength tuning by adjusting the quantum well indium composition and QW thickness. Thanks to the core-shell growth mode, nanopillar can scale its footprint up to micrometer size without causing any defects, forming large optical cavity to confine photons. Nanolasers with three different types of optical cavities were subsequently demonstrated. Inspired by nanowire lasers, transferred InP/InGaAs/InP nanopillar lying down on sapphire substrate is a natural

horizontal Fabry-Perot resonator. Thus, optically-pumped laser oscillation was obtained with clear Fabry-Perot attributes. By growing nanopillar on SOI substrate, a vertical Fabry-Perot cavity was created with bottom mirror enhance by Si-SiO_2 interface of SOI substrate. Therefore, as-grown nanolasers were achieved at different wavelength ranging from 1.1μm to 1.3μm. Another novel cavity structure took advantage of silicon selective etching to create silicon undercut to enhance bottom reflection. Not only 1200nm nanolaser was achieved, but its strong second harmonic effect generated a 600nm laser emission. Finally, theoretical study on optical gain model and cavity mode behind these long wavelength nanolaser results was performed, for the sake of further optimizing laser performance and moving towards electrically pumped device.

In the last part, ensemble devices were fabricated and tested with in-situ doped nanopillar diode structure. Furthermore, three different methods were explored to solve the current shunt path problem when fabricating single nanopillar devices. All three methods resulted in significant reduction of shunt path current leakage and can be applied in different situations. A full functional optical link has been also demonstrated with InGaAs nanopillar devices and polymer waveguide, serving as a system-level proof of concept that our nanopillars have the potential to empower on-chip optical interconnects.

In conclusion, we not only demonstrated laser oscillation of III-V nanopillar, but also experimentally showed integration strategy with CMOS electronics and silicon photonics. As far as we know, this presents the most viable method to achieve on-chip light source for intra-chip optical interconnect.

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