Closed Loop Digital LDO Linear Controller

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Agenda

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- Architecture
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- Details of Closed Loop LDO
- Discussion
- Challenges
Problem Statement

Want to build a closed loop digital LDO linear controller that provides constant $V_{out}$ regardless of variable $V_{in}$ with:

1. At least 75% current efficiency when $I_{Load}=0.35mA$
2. 100mV regulation range
3. High clock frequency
4. Stable/Constant $V_{out}$
• Low dropout regulators (LDOs) are effective ways to regulate an output voltage that is powered from a higher input voltage.
• A basic LDO involves a variable resistor (can be implemented by using PMOS transistors), I_Load, C_Load, and a controller.
• The job of the controller is to keep the output voltage constant even with variable input voltage. If the load current (I_Load) increases, the variable resistor should decrease to increase the current flow from the input through the resistor to the output and vice versa in order to make Vout remain constant.
• The controller detects the deviation of the Vout from its desired value and responds accordingly to either increase or decrease the variable resistor’s value to keep the Vout constant.
Architecture

Closed loop design of digital LDO with digital controller (Decision maker and Decision executer), 2 Comparators and Pmos devices (binary coding power gates which has 8 different size), CL, IL:

<table>
<thead>
<tr>
<th>comp_out</th>
<th>m_out</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 : 0</td>
<td>Up : 100 = 4</td>
<td>Count up</td>
</tr>
<tr>
<td>11 : 3</td>
<td>Down : 010 = 2</td>
<td>Count down</td>
</tr>
<tr>
<td>01 : 1</td>
<td>Hold : 001 = 1</td>
<td>Steady state</td>
</tr>
<tr>
<td>10 : 2</td>
<td>Hold : 001 = 1</td>
<td>Steady state</td>
</tr>
</tbody>
</table>

Input of Comparators:

- COMP_out (output of comparators)
- m_out (output of decision maker)
- Z (output of decision executer)
• The job of two comparators is to detect the position of Vout and feed the information into the decision maker block.
• The decision maker block takes that information and decides if Vout should go up, down, or stay hold within Vref_h and Vref_l.
• The decision maker feeds this information into the 8 bit binary counter or decision executer which physically changes the value of power gate code <7:0> (input of the Pmos devices) and thus Vout.
• An example: when Comp_h=0 (Vref_h> Vout, or Vout is lower) and Comp_l=0 (Vref_l> Vout, or Vout is lower) → Decision maker output=Up → Decision executer output = Power gate code<7:0> +1. Thus, Power gate code counts up from its previous value by turning on more Pmos devices.

Combined truth table of digital controller of LDO:

<table>
<thead>
<tr>
<th>comp_out (output of comparators)</th>
<th>m_out (output of decision maker)</th>
<th>Z (output of decision executer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00=0</td>
<td>Up=100=4</td>
<td>Count up: Power gate code&lt;7:0&gt; +1</td>
</tr>
<tr>
<td>11=3</td>
<td>Down=010=2</td>
<td>Count down: Power gate code&lt;7:0&gt; -1</td>
</tr>
<tr>
<td>01=1</td>
<td>Hold=001=1</td>
<td>Steady state</td>
</tr>
<tr>
<td>10=2</td>
<td>Hold=001=1</td>
<td>Steady state</td>
</tr>
</tbody>
</table>
Continued....

- Pmos device unit size: W=210nm, L=32nm
- Vin=1.05V
- C_Load=200pF

- Proposed Metrics:
  1. Current efficiency= 75-99% for 0.35mA current load (RL=3KΩ)
  2. Regulation range= 100mV
  3. Clk frequency=1MHz - 1GHz
  4. Vout being stable within regulation range
Testbench and RTL code

```verilog
module decoder;
input [3:0] comp_out, //comp_out
input clk,
input resetb;
output reg [2:0] m_out, //decision maker output (up down hold)
output reg [7:0] Z; //decision executor output or power gate code

always @ (posedge clk)
begin
  if (comp_out == 2'b00) m_out = 3'b100; //output-up
  else if (comp_out == 2'b11) m_out = 3'b100; //output-down
  else m_out = 3'b001; //when comp_out=2'b01 or 2'b10 output=hold
end

//decision maker
always @ (posedge clk)
begin
  //Extra cycles to flush out any initial X's
  $display("X");
  //Input and output events on clock rising edge
  $display("X");
end

//initial begin
$monitor("\n   \$monitor("It **Mam through all test vectors**");\n\$finish;\nend

endmodule
```
Results

Gate Level Schematic of LDO controller (using IC compiler):

Layout of LDO controller (using IC compiler):
In figure above, when Vout is between Vref_l & Vref_h, comp_out=01=1, m_out is Hold or 001=1, and Z is at steady state=35 which means the controller works and when used in the closed loop LDO, the Vout looks like the graph on the right where Vout is constant/stable between Vref_h and Vref_l.
Details of Closed Loop LDO

1. Comparator, decision maker, decision executer output waveform when Vout is increasing at 0.5us:

Comp_out=00, m_out=100 (Up), pg code is counting up from 7 to 8 to higher # and therefore Vout is increasing
Continued....

2. Comparator, decision maker, decision executor output waveform when Vout is decreasing at 1.2us:

Comp_out=11, m_out=010 (Down), pg code is counting down from 9 to 8 to lower # and therefore Vout is decreasing
3. Comparator, decision maker, decision executor output waveform when Vout is steady at 6μs:

Comp_out=01, m_out=001 (Hold), pg code is at steady state at 8 and therefore Vout is constant.
Discussion

1. Current Efficiency:
   • Using Invx1_rvt standard cells, clock frequency=111MHz, C_Load=0.01fF, supply voltage=1.05V power consumption of the digital controller was= 90uW after APR
   • The current leakage = power consumed by controller/Vin = 90uW/1.05V = 85.7uA. Therefore current efficiency = I_Load/(I_Load+I_Leak) = 0.35mA/(0.35mA+.0857mA) = 0.80 → 80% which is within proposed metrics

2. Regulation Range:
   In this design I was able to achieve voltage range=80mV between Vmin=0V and Vmax=Vin. This turned out to be even better than expected value (100mV)

3. Clock Frequency:
   For the full closed loop LDO, clk period was=6ns→clk freq=0.17GHz which meets the proposed metrics
4. Vout Stability:

With the closed loop, the voltage profile looks like the figure below, where Vout is stable/constant between Vref_l=620mV and Vref_h=700mV.
Challenges

1. Vout was increasing above Vref_l and Vref_h even though Z_in<7:0> was steady:
   • The reason was the current of Vout was too low compared to the pmos gates. So the current of a single pmos at Vds=700mV was measured and multiplied by 128 (because the biggest pmos size is 128x) which was equal to ~30uA*128=3840uA=3.8mA. That means I_Load<3.84mA→RL>0.3KΩ. First RL=1KΩ was chosen but RL=3KΩ gave better Vout curve. The lower the I_Load the easier it is for the pmos gates to match the current with it.
   • Still Vout was too high, so clk frequency was lowered by 3x and step size was decreased which made Vout to be in between Vref_l and Vref_h.

2. Vout was too rough and limit cycling (Vout is limited by the resolution of LSB) occurred:
   • CL was increased by 2x (200pf) which made Vout smoother. Voltage range (between Vref_l and Vref_h) could have increased also to fix this issue.
Thank you!

Questions???