Photonic Links -- From Theory to Automated Design

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This PhD came at a very opportune time in my life. On the one hand, I began this journey with a more refined sense of judgment, thought, and knowledge than, say, when I entered undergrad. On the other, I still consider myself young enough to mold, adapt, and grow to the people and environment around me. Putting that together, the people I bonded with during the last five years are special in not only being unique, exceptionally talented, loving, and hilarious but also having the ability to teach and change me for the better.

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by

Krishna Tej Settaluri

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Abstract

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Recent advancements in silicon photonics show great promise in meeting the high bandwidth and low energy demands of emerging applications. However, a key gating factor in ensuring this necessity is met is the utilization of a link design methodology which transcends the various levels in the hierarchy, ranging from the device and platform level up to the systems level. In this dissertation, a comprehensive methodology for link design will be introduced which takes a two-prong approach to tackling the issue of silicon photonic link efficiency. Namely, a fundamentals-based first principles approach to link optimization will be introduced and validated. In addition, physical design trade-offs connecting levels in the architectural hierarchy will also be studied and explored. This culminates in an intermediate goal of this dissertation, which is the first-ever design and verification of a full silicon photonic interconnect on a 3D integrated electronic-photonic platform. To proceed and further enable the rapid exploration of the link design architectural space, the analog macros for a majority of this dissertation were auto-generated using the Berkeley Analog Generator (BAG). With these key design tools and framework, performance bottlenecks and improvements for silicon photonic links will be analyzed and, from this analysis, the motivation for a new, single comparator-based PAM4 receiver architecture shall emerge. This architecture not only showcases the tight bond in dependency between high-level link specifications and low level device parameters, but also shows the importance of physical design constraints alongside fundamental theory in influencing end-to-end link performance.