The IMPACT Center

Addressing Challenges for Future IC Design and Manufacture

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Outline

- The Landscape
  What is happening today & what we imagine will happen tomorrow

- The IMPACT Center
  Who we are & what we do

- A Tasting
  Five Research Projects

- A Success Story
  Equipment Control for optimized across wafer CD uniformity

- Opportunity Beckons
  Clip calculus as a new paradigm
The Evolving Landscape

- **New Technologies**
  - Multiple patterning, Immersion, metal gates …

- **New Materials**
  - Zr-doped TaOx, MoN, WN …

- **Design/Manufacturing Interface breakdown**
  - Need data driven models of manufacturing for design
  - Need design aware manufacturing practice

- **More fabless companies**
  - Need to deal with foundries, manage information
  - Model of manufacturing becomes even more important

- **Complexity is the new bottleneck**
The Target – 22 nm and beyond

- **Expected technologies**
  - Quadrupole/Quasar illumination
  - Immersion Litho
  - Double patterning
  - Non-planar devices
  - Exotic gate materials
  - New transistor designs

- **Tools that will be necessary**
  - Distributed Computation: parallel or cellular processors
  - Data mining, Machine Learning, fast parameter extraction
  - Modeling expertise to capture effects at various space and time scales
  - Process expertise to drive modeling effort
  - Design expertise to impact electrically relevant performance
Three Challenges

- You don’t always get what you want
- Interactions and The Radius of Influence
- The Computation Bottleneck
What you ask for …
What you get ...
You don’t always get what you want

- Manufacturing realities cannot be modeled by simple rules

- Partial solution – better predictive “models” of the manufacturing process, hierarchical abstractions
  - Models must be simple enough to run very, very fast
  - Link Manufacturing model upstream to EDA tools
  - Static timing, RC extraction, power/noise/area optimization
The Radius of Influence

OPC/RET changes at center of red zone affects AD patterns across red area
The Radius of Influence

- OPC/RET will get even more computationally expensive
- Design rules will become extremely complex
- Interactions across features
- Interactions between layers
- Interactions among processes

Partial solution – Filter through design & process
- Concentrate on design-critical hotspots
- Concentrate on process sensitive hotspots
- Automated hot-spot detection and repair
- Mask fragmentation for multiple patterning/exposure
The Computation Bottleneck

- Design cycle iterations are expensive
- Process models must be run very fast
- Design rules are now 2000+ pages!

- Partial solution – stress scalability and computation in all aspects of our research
Our Response – the IMPACT Project

- IMPACT  [http://impact.berkeley.edu/](http://impact.berkeley.edu/)  
  Integrated Modeling Process And Computation for Technology

- Long term, pre-competitive, interdisciplinary research
- Supported by 21 leading Companies and State of California
- 17 Faculty + 23 Grad Students + 5 Post-docs + 3 Undergrads
- 9M$ budget

- Major Equipment Donations
  - Centura 200 epitaxial tool from Applied Materials
  - EM Suite Simulation Package from Panoramic Technologies
  - Wafer/Mask processing credits: Spansion, SVTC, Dupont, Photronics
The Industry Team – Thanks!
# The Faculty Team

<table>
<thead>
<tr>
<th>Name</th>
<th>Dept/Inst</th>
<th>Inst</th>
<th>Research Areas</th>
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<tbody>
<tr>
<td>Alon, Elad</td>
<td>EECS</td>
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<td>Chang, Jane</td>
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<td>Dornfeld, David</td>
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<td>Neureuther, Andrew</td>
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<td>Chemical-Mechanical Planarization</td>
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Five Inter-connected Research Themes:

- Lithography: Andy Neureuther
- Novel Technologies: Tsu-Jae King-Liu
- CMP: Dave Dornfeld
- Etch: Jane Chang
- Design-Manufacturing Interface: Puneet Gupta
Litho: Through-Focus fast-CAD

Pattern matching

Att-mask 90° edge effects

Compact model though focus

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DMI: Non-Rectangular Gate Modeling

- **Four components**
  - Poly gate imperfections: well-studied (SPIE’05)
  - Active rounding: (ASPDAC’08)
  - Line-end shortening: (DAC’07)
  - Line-end tapering: (PMJ’08)

- **Key elements**
  - Equivalent length/width models
  - Separate modeling for Ion and Ioff

- **Use Models**
  - Design power/performance analyses
  - Interactions with design rules and OPC
  - Shaping transistor channels for better devices

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<th>nominal</th>
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<td>leakage (nW)</td>
<td>138.69</td>
<td>83.49</td>
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<td>clk→q (ps)</td>
<td></td>
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<tr>
<td>fall</td>
<td>70.57</td>
<td>68.54</td>
<td>2.9</td>
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<tr>
<td>rise</td>
<td>76.07</td>
<td>74.07</td>
<td>2.6</td>
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<tr>
<td>setup time (ps)</td>
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<td></td>
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<tr>
<td>fall</td>
<td>20.43</td>
<td>18.08</td>
<td>11.5</td>
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<tr>
<td>rise</td>
<td>42.71</td>
<td>35.01</td>
<td>18.0</td>
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Case Study: DFF
Plasma: Surface, Feature, Reactor Scale Models

- Particle-in-cell, Monte Carlo collision
- Molecular dynamics simulations and expts
- Monte Carlo feature scale model coupling with reactor model

Energy and angle of all species

Fundamental surface reactions

Origin of surface evolution

Couple models at various scales to understand plasma-surface interaction and predict profile evolution

Low DC Low \( W_b \) High DC Low \( W_b \) Low DC High \( W_b \)
Comprehensive CMP Modeling

Integrated chemo-mechanical modeling of material removal

Data structure for capturing multiscale behavior: tree based multi-resolution meshes

Pattern Evolution Model for HDPCVD STI

Chip Layout

Pattern density

Evolution
Transistor Design for Reduced Variability

- **Very steep retrograde doping** is needed to reduce $\sigma_{VT}$ due to RDF
  - Engineer the channel material ($\text{Si}_{1-x}\text{Ge}_x$) to control dopant diffusion.
- **Evolve the planar MOSFET into a tri-gate structure**
  - Improve channel gate control, improve robustness to process-induced variations, improve transistor performance

**Planar MOSFET:**

**Tri-Gate MOSFET:**

Gate electrode covers 3 sides of the channel

**Simulated I-V Curves:**

- **atomistic doping** (100 cases)
- **continuum doping** (nominal case)
A Success Story – CD Control

- Critical Dimension (CD)
  - Width of printed lines
  - Varies across wafer, and wafer-to-wafer
  - greatly influenced by post-exposure bake and etch

- CD variability is the performance metric for pattern transfer

- Want: to reduce CD variability

- How? Making each process step spatially uniform is not possible

- Our approach: Control
  manipulate PEB temperature spatially to compensate for downstream systematic across-wafer CD variation due to etch
- Temperature sensors
- Unprecedented Spatial and temporal resolution
- Used to model PEB plates and effect of temp on CD
- Models are used for Control
The Value of Control

- Post-Exposure-bake
  - Key process step
  - Directly impacts critical dimension uniformity

- Control spatial temperature of bake plate
  - Yesterday ± 0.3 °C → Today ± 0.15 °C
  - Result: 1 nm reduction in CD spread

- Benefit: mid-sized fab in 1st year of product lifecycle
  - ~$3/die * 200 die/wafer * 20,000 wafer/mon * 12 mon/yr
  - = 144 M$ per year !!
CD Uniformity Control

Before

2.3 nm

Mean = 3.8 nm

After

1.0 nm

Mean = 3.5 nm
Opportunity Beckons – Clip Calculus

- Basic Assertion:
  Working with clips is more efficient and natural than distances/rules

- Potential opportunities for clip calculus
  - Faster printability analysis
  - Inverse Litho

- Clips
  - Could be non-rectangular
  - Standard cells, macros, etc ...
  - Core “Central” part of a clip
  - Context “Outer” part of a clip
  - Library Collection of clips

- Core & Context depend on target application
  - Ex: DRC, OPC, Printability analysis

- The problem: algorithms to efficiently deal with clips
Ex: DRC

- Current Practice
  - DRC brick is 2,000 pages and exploding
  - Conventional rule-based DRC at 22nm will be unmanageable
- Alternatives: Work with clips not distances
  - Leverage the speed of pattern match
  - Produce library of good, bad, or graded patterns
  - Use library to detect and correct new design layouts
- Open problems
  - Clip-based DRC, Hybrid Rule-Clip DRC,
  - Redundancy removal in rules, Correction!
- Core and Context
  - Core is the region that is DRC clean given the fixed Context
  - Context may not be DRC clean as that depends on Context(Context)
- Use Case
  - Library of known DRC clean (in core) clips
  - In a mask M, use PatternMatch against library L
  - Can eliminate the core of every matched clip
  - Will have to do DRC on remaining areas
Clip Metrics

- What is a good metric on the space of clips?
- Difficult problem
- Must also extend to Alternating PSM, Attenuating PSM
- Metric must also be computable in the language of rectangles

- Standard pixel based metrics fail: \( k_{c_i} \cdot c_j k^2 = \# \text{ of disagreeing pixels} \)
  - Treats each pixel independently
  - Does not respect proximity
- When are two clips similar?
  - If the images in Silicon of the core of both clips are similar

- Suggests that we need application dependent weightings
  - Exposure & Dose sensitivity analysis will have different weights
Some Computational Problems

Mask $M$, clip $c$, library $L = \{ c_k \}$, $N =$ number of clips

1. **ExactMatch**: Find all instances of $c$ in $M$
2. **RoughMatch**: Find all sub-patterns $p$ in $M$ with $k p_1 \ldots c_k \cdot 2$
3. **VolFind**: Find Area(core union)
4. **WhereNext**: Find largest rectangle not covered by clips
5. **ExactTile**: Tile $M$ with core of clips drawn from library i.e. choose tiling to maximize Area(core union)

For 3 & 4 we have $N \log(N)$ algorithms with $N \log(N)$ pre-processing time

- Many other very interesting problems
  - Net-list covering by clips
  - Dynamic programming for inverse lithography
- These are all problems in CS, with a twist
  - Must compute based on rectangles, respect hierarchy
  - Must work on huge problems
In Summary…

- The IC revolution will continue
- The method of designing ICs will have to change
- Design and Manufacturing Interaction is much more complex
- Challenges include
  - Design & Process Complexity
  - Modeling & Computation

- IMPACT will play a key role
  - Technological value to our sponsors
  - Real educational experience for our students
  - Multi-disciplinary cutting edge research opportunities for our faculty

http://impact.berkeley.edu/
Feedback: poolla@berkeley.edu
# Research Theme A – Litho

<table>
<thead>
<tr>
<th><strong>Objective</strong></th>
<th>Invent a range of approximate-but-fast models based on first principles for assessing manufacturing realities upstream in the design flow</th>
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<tbody>
<tr>
<td><strong>Key Projects</strong></td>
<td>- Simulation of electromagnetic effects of mask edges  &lt;br&gt; - Compact models for through-focus modeling &lt;br&gt; - Process parameter specific electrical devices and circuits  &lt;br&gt; - Litho-aware decomposition for double patterning</td>
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## Research Theme B – DMI

<table>
<thead>
<tr>
<th>Objective</th>
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<tbody>
<tr>
<td>ƒ Increase design predictability, decrease manufacturing cost and yield</td>
<td>Increase design predictability, decrease manufacturing</td>
</tr>
<tr>
<td>ramp time</td>
<td>cost and yield ramp time</td>
</tr>
<tr>
<td>ƒ Leverage unexplored interactions between design and manufacturing</td>
<td>Leverage unexplored interactions between design and manufacturing</td>
</tr>
<tr>
<td>ƒ Build design-usable models of process and use them to analyze/optimize</td>
<td>Build design-usable models of process and use them to analyze/</td>
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<tr>
<td>design</td>
<td>optimize design</td>
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<thead>
<tr>
<th>Key Projects</th>
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<tbody>
<tr>
<td>ƒ Variation modeling in BSIM compact models</td>
<td>Variation modeling in BSIM compact models</td>
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<tr>
<td>ƒ Leakage modeling, monitoring and optimization in presence of variability</td>
<td>Leakage modeling, monitoring and optimization in presence of</td>
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<tr>
<td></td>
<td>variability</td>
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<tr>
<td>ƒ Impact of variations on power of mixed-signal circuits</td>
<td>Impact of variations on power of mixed-signal circuits</td>
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<tr>
<td>ƒ Modeling and optimizing for pattern-dependent variations in standard</td>
<td>Modeling and optimizing for pattern-dependent variations in</td>
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<tr>
<td>cell designs</td>
<td>standard cell designs</td>
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<tr>
<td>ƒ Design-aware mask inspection</td>
<td>Design-aware mask inspection</td>
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<tr>
<td>ƒ Comprehensive chip-scale variability modeling</td>
<td>Comprehensive chip-scale variability modeling</td>
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## Research Theme C – Plasma

<table>
<thead>
<tr>
<th>Objective</th>
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<tr>
<td>Couple models at various scales to understand plasma-surface interaction and predict profile evolution</td>
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<table>
<thead>
<tr>
<th>Key Projects</th>
</tr>
</thead>
<tbody>
<tr>
<td>▪ Develop fast algorithms to determine energy and angular distributions of all plasma species</td>
</tr>
<tr>
<td>▪ Develop fundamental models for plasma-surface interactions</td>
</tr>
<tr>
<td>▪ Develop predictable profile simulator for etch and deposition processes</td>
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# Research Theme D – CMP

| Objective | Identify key influences of chemical and mechanical activity including the coupling of CMP/polishing  
|           | Develop an integrated model of CMP material removal  
|           | Verify model thru simulation and test, as a platform for model based process optimization |
| Key Projects | Determine fundamental mechanics of the electro-chemical removal of material  
|           | Comprehensive model of CMP material removal (including pattern dependency, prior deposition processes, material induced variations etc)  
|           | Establish mechanical elements of CMP material removal via FEM (incl: pad, abrasive/slurry/device/surface interaction)  
|           | Understand effects of slurry chemistry on abrasive agglomeration/dispersion and material nano-hardness |
# Research Theme E – Novel Technologies

<table>
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<tr>
<td>- Investigate advanced transistor designs, materials, and processes to</td>
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<tr>
<td>reduce variability and enhance performance of bulk CMOS technology</td>
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<tr>
<td>- Develop prediction and abatement methods for systematic variations</td>
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<tr>
<td>due to lithography, CMP, and etch processes</td>
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<table>
<thead>
<tr>
<th>Key Projects</th>
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<tbody>
<tr>
<td>- Transistor design optimization for robustness to variations</td>
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<tr>
<td>- 3-D strain engineering for enhanced performance</td>
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<tr>
<td>- Dopant profile engineering via heterostructures</td>
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<tr>
<td>- Scatterometry-based parameter extraction for calibration of OPC, CMP,</td>
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<tr>
<td>and etch processes</td>
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<tr>
<td>- Optical metrology for <em>in-situ</em> process monitoring</td>
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<tr>
<td>- Dynamic adaptive metrologies strategies</td>
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</table>
Some computational problems ...

- There are other very interesting problems
  - Net-list covering by clips
  - Library generation
  - Dynamic programming for inverse lithography

- These are all problems in CS, with a twist
  - Must compute based on rectangles
  - Must respect hierarchy
  - Must work on huge problems

- Clip-based paradigms have good potential
  - OPC re-use
  - Faster DRC, RC extraction, printability analysis
  - Faster hot-spot detection and repair
  - Fast mask fragmentation for multiple-patterning

- Many challenging problems
  - Metrics
  - Use cases
  - Fast Algorithms
Plasma: Research Integration

Ion Angular and Energy Distribution (Particle in Cell modeling: M. Lieberman)

Species Distribution (Reactor-Scale Modeling: D. Graves and J. Chang)

Photoresist Reaction Mechanism (Beam Experiments: D. Graves)

Profile Evolution (Feature Scale Modeling: J. Chang)

LER issue for 193nm PR

- Define testbeds for research integration (LER, Gate Stack Etch, PVD ….. etc.)

IMPACT • 38

Litho: Electrical Test Patterns & Circuits

Collaborative Platform for DfM

Multi-Student Test Masks

Novel Leakage Testing

On-Line Database Sim/Exp

IMPACT • 39
Segmented Bulk MOSFET for Reduced Variability

- Multi-gate structures provide for improved control of short- and narrow-channel effects, and reduce STI-induced stress effects
- Steep retrograde channel doping reduces $V_T$ variation due to SDF
- Segmented bulk MOSFET combines these features to reduce variability in performance, while retaining compatibility with strained-Si, high-k/metal gate & active body biasing technologies

![Graphs showing comparison between Planar Bulk MOSFET and Segmented Bulk MOSFET](image)

$\sigma_{VT} = 27.1 \text{ mV}$

$\sigma_{VT} = 10.1 \text{ mV}$

- Planar Bulk MOSFET
  - $L_G = 20\text{nm}$
  - $EOT = 0.9\text{nm}$
  - $V_{DS} = 1\text{V}$

- Segmented Bulk MOSFET
  - 100 atomistic simulations

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IMPACT • 40

Segmented Bulk MOSFET for Reduced Variability

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IMPACT • 40