The Future of Devices & Chips: A Blast from the Past?

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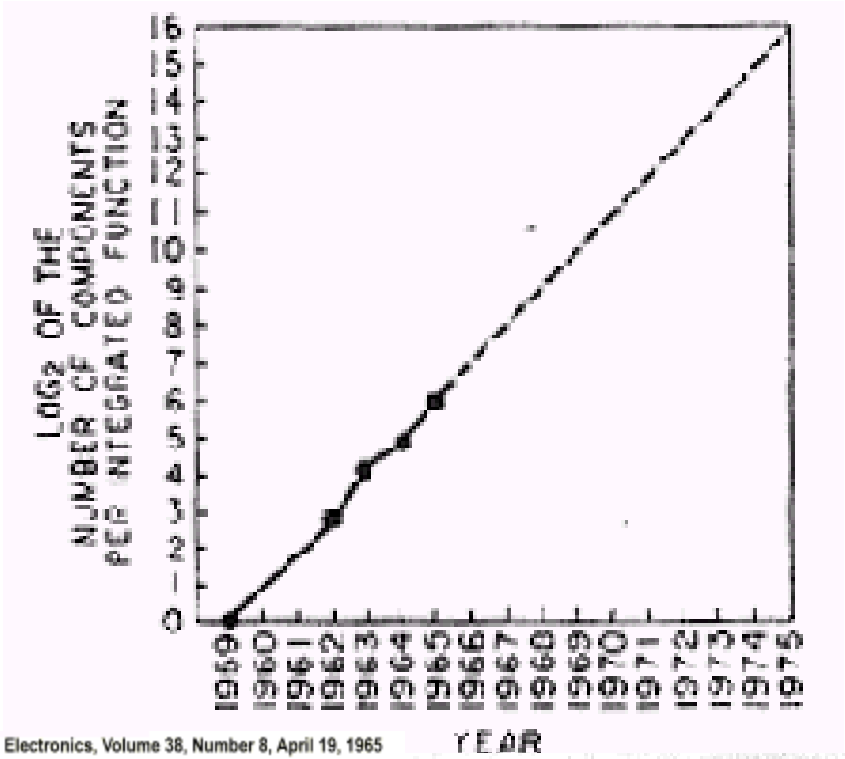
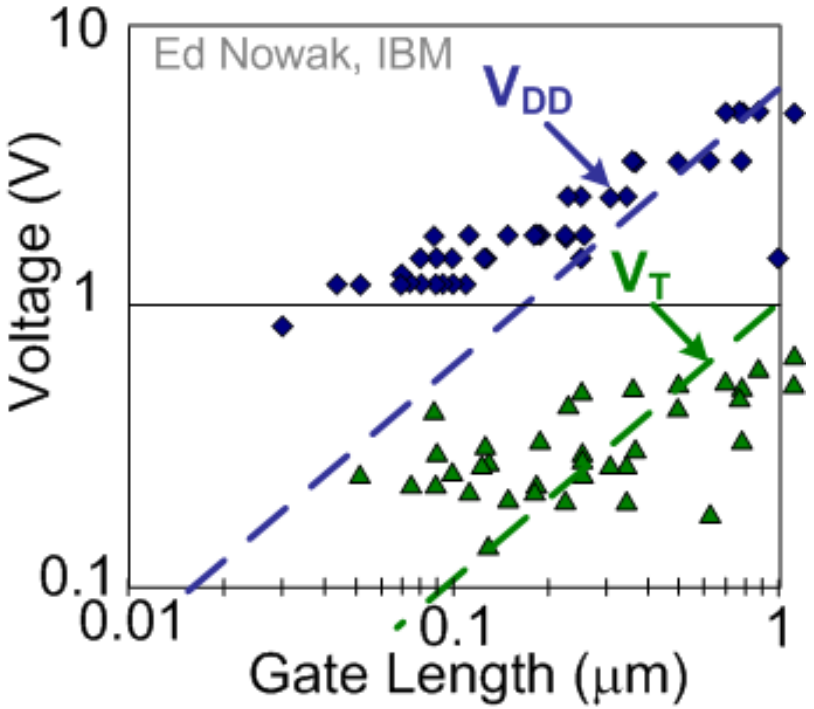
Moore's Law and Original Issues



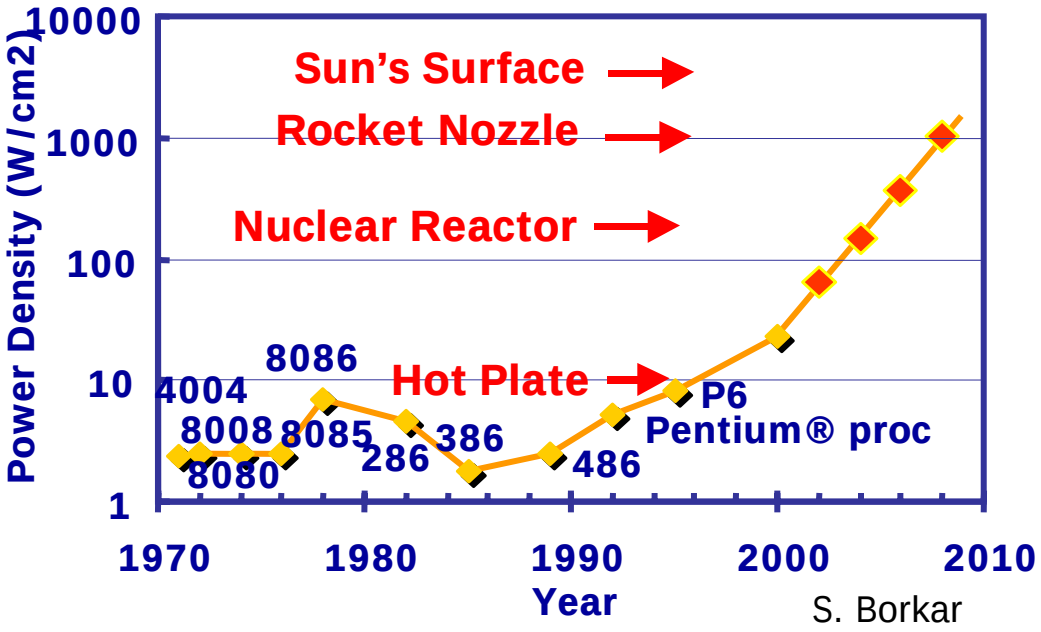
Electronics, Volume 38, Number 8, April 19, 1965

- Design cost
- What to do with all of the functionality possible
- Power dissipation

Power Consumption…



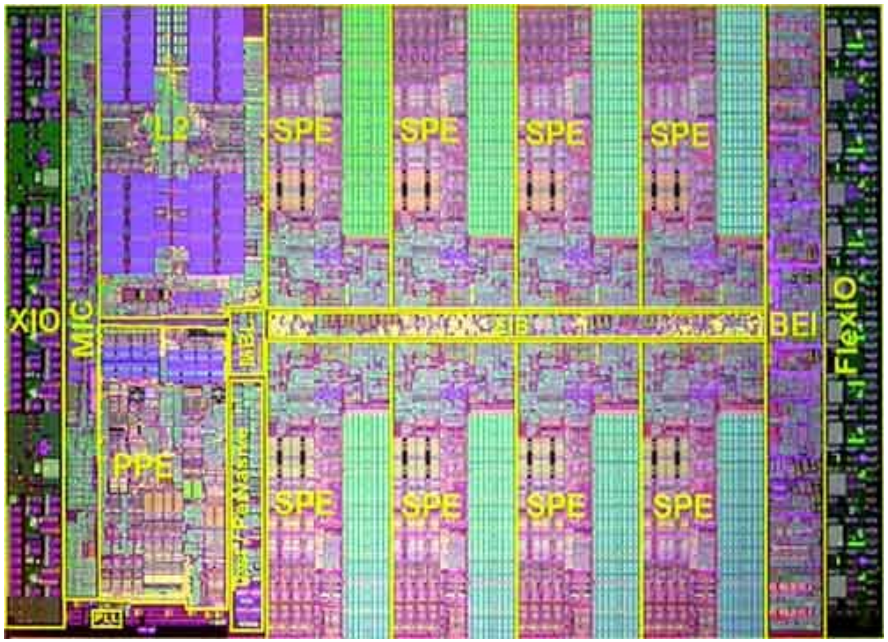
Power Density Prediction circa 2000

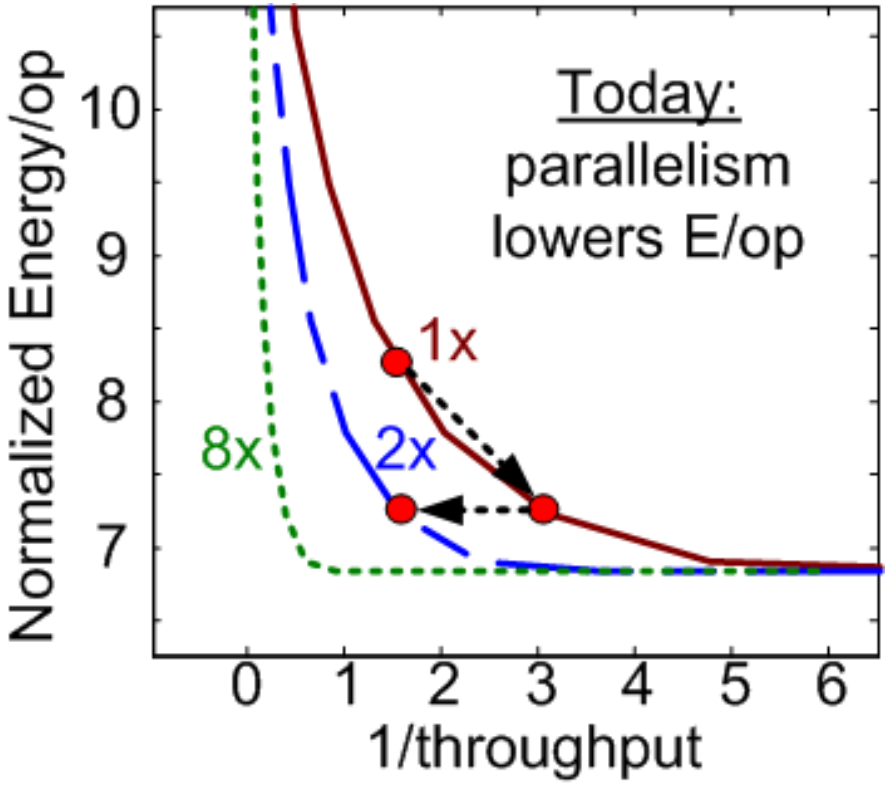


S. Borkar

- Since ~2000 supply voltage (Vdd) stuck at ~1V
  - Leakage stops you from lowering threshold (Vth)
- Leads to very poor power scaling
  - 1kW chips?

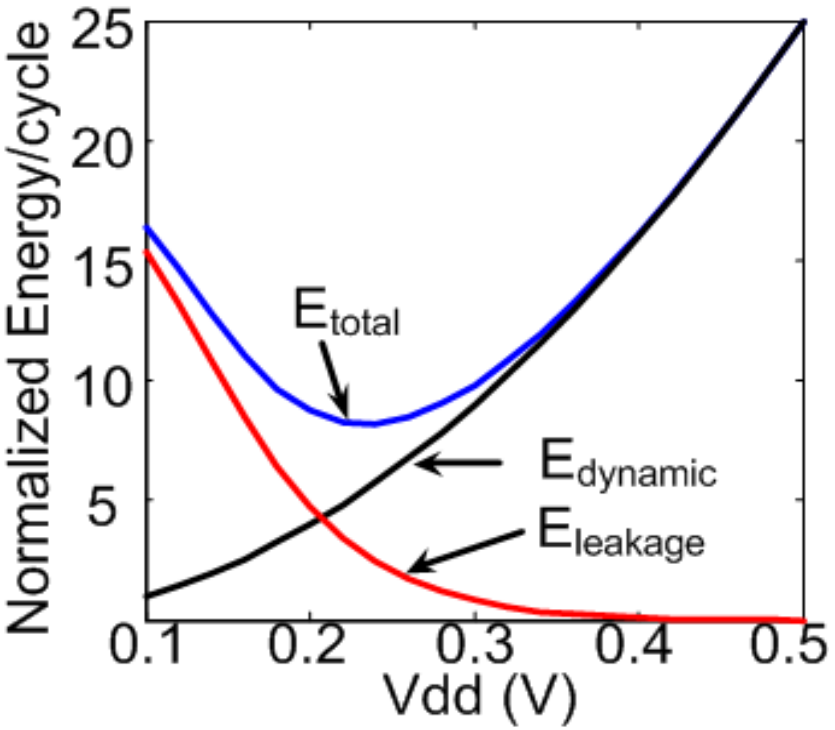
Parallelism to the Rescue

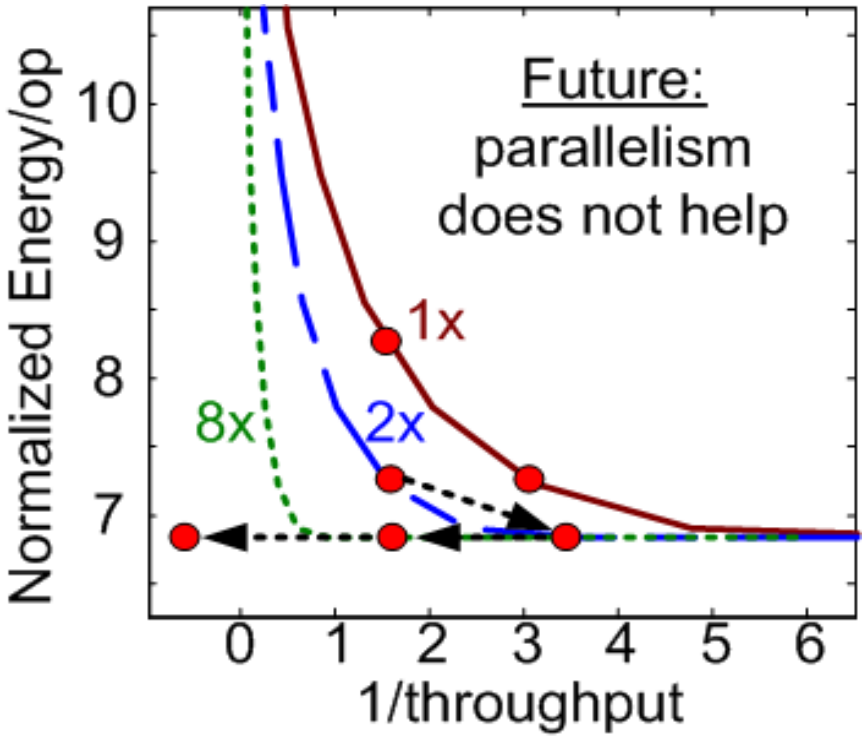




- **Parallelism allows slower, more energy-efficient units while maintaining performance**
- **Will this last forever?**

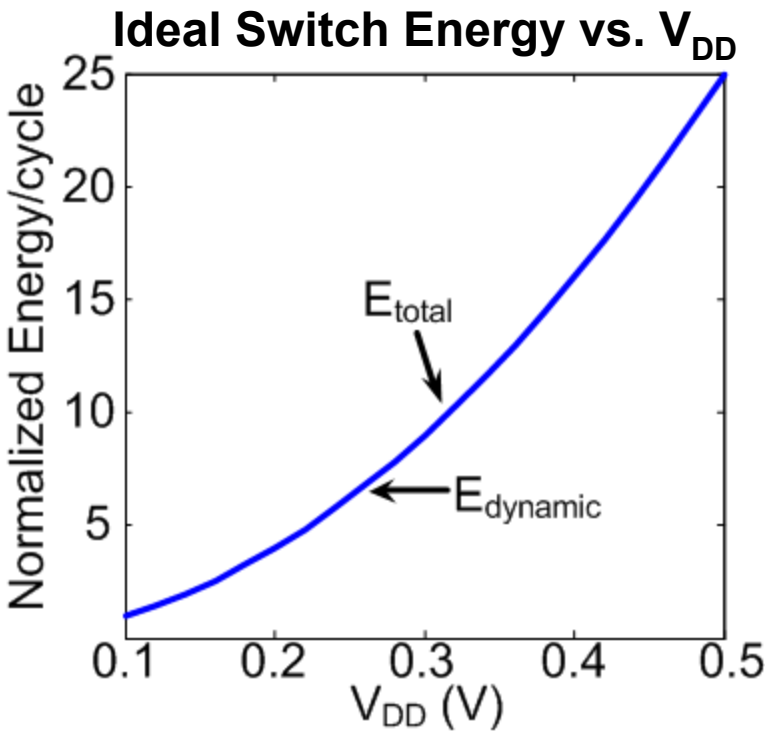
Where Parallelism Doesn't Help

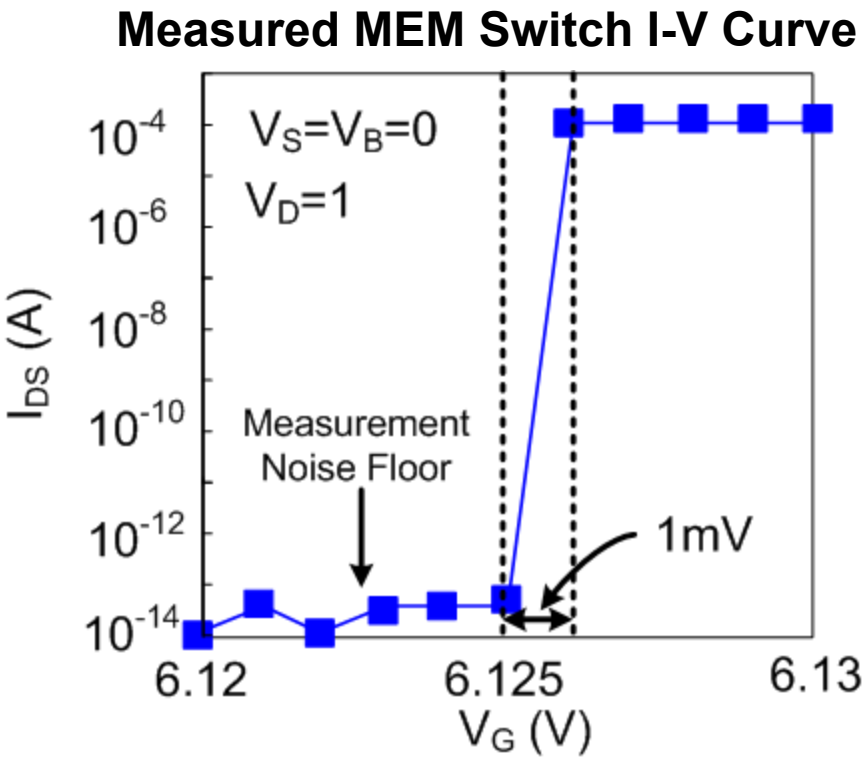




- **CMOS circuits have an absolute minimum energy/op**
  - **Need to balance leakage and active energies**
- **Limits energy-efficiency, no matter how slowly the circuit runs**

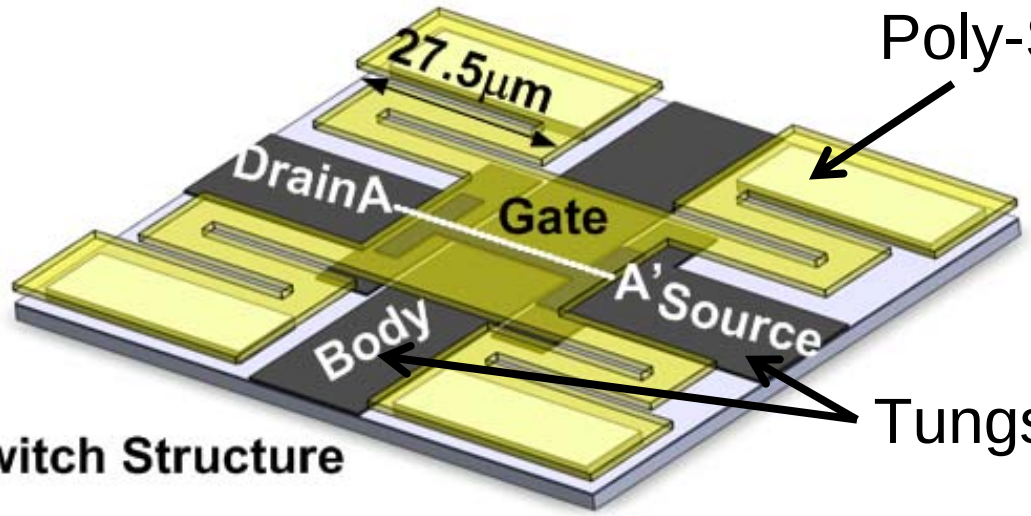
What if There Was No Leakage?





- **Supply voltage decreases → energy decreases**
- **Mechanical switches don't leak, turn on abruptly**
  - **Potential pathway to continued scaling**

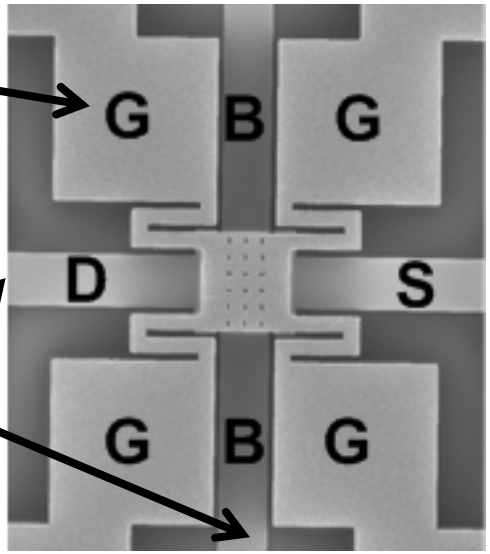
Switch Structure & Operation

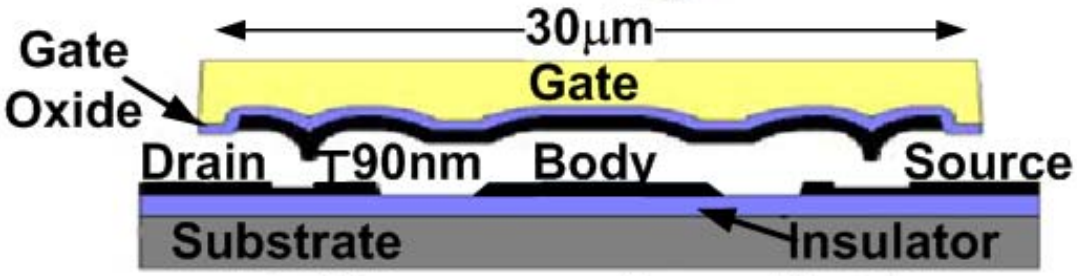


Switch Structure

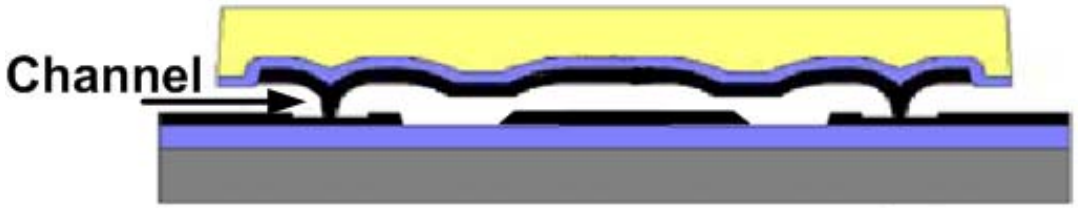
Poly-SiGe

Tungsten





A-A' cross-section: *off*-state



A-A' cross-section: *on*-state

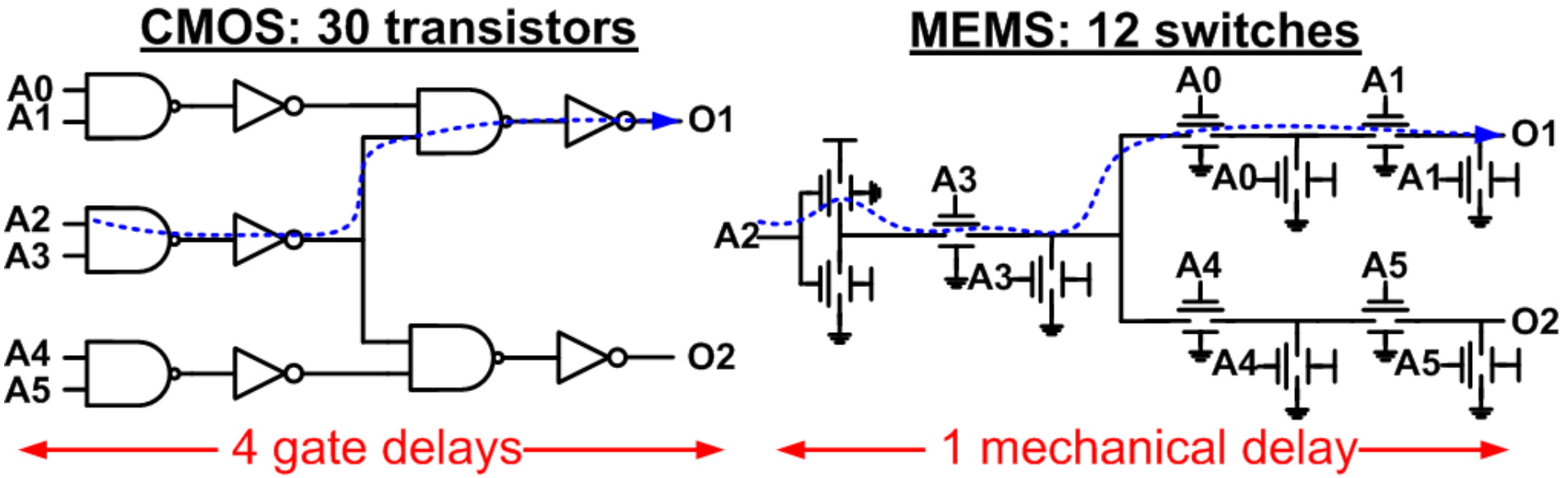
OFF Switch:

$|V_{gb}| < V_{po}$ **(pull-out)**

ON Switch:

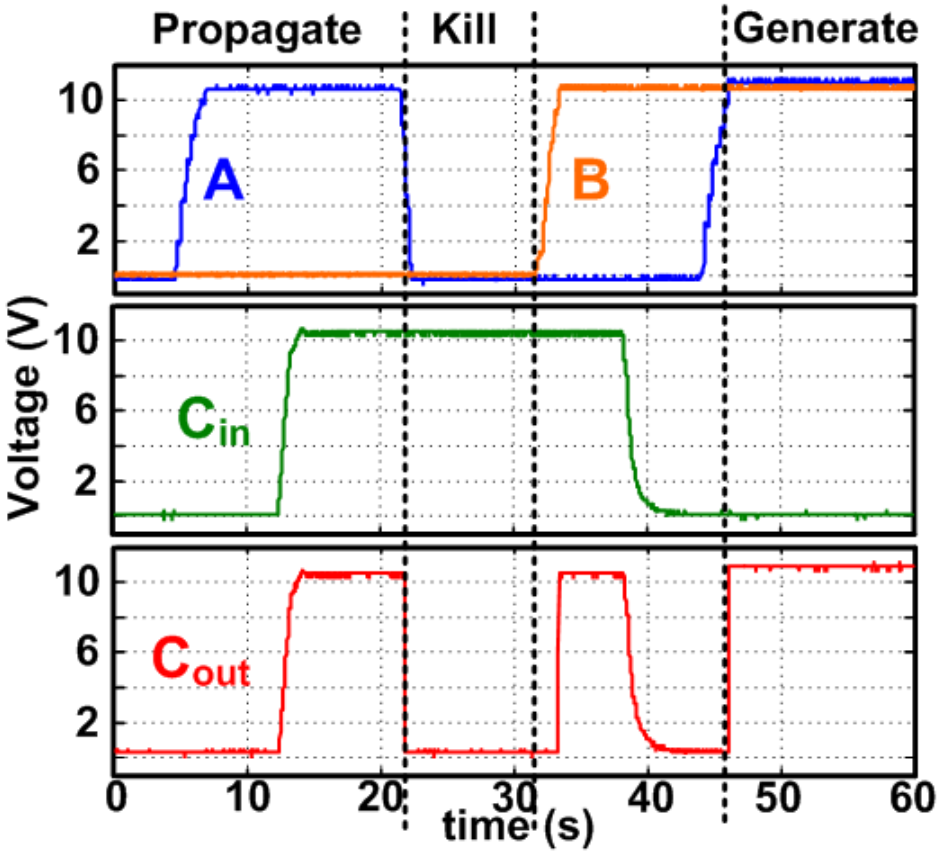
$|V_{gb}| > V_{pi}$ **(pull-in)**

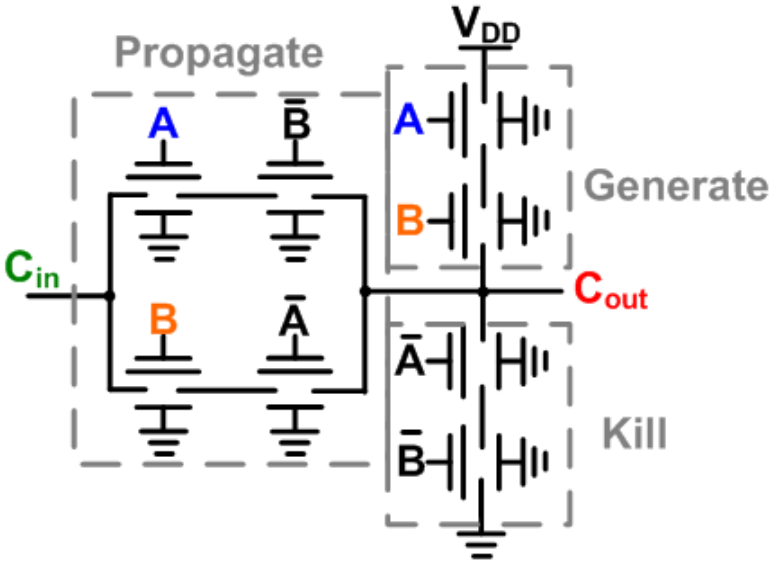
Relay Logic



- Relay delay dominated by mechanical motion
- So, implement logic as a single complex gate
  - All devices move at the same time
- Improves area, device count, performance

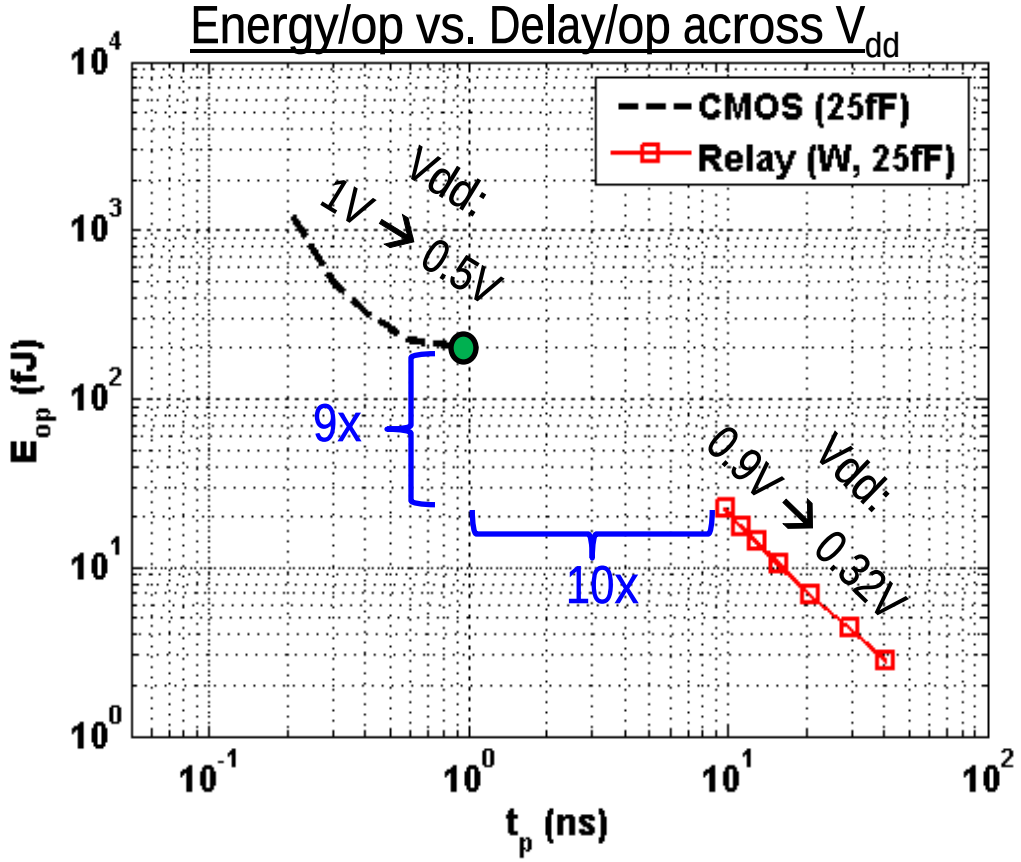
Logic Demonstration





- Relays built with 1μm lithography - clearly not yet competitive with CMOS…
  - What does it take to get there?

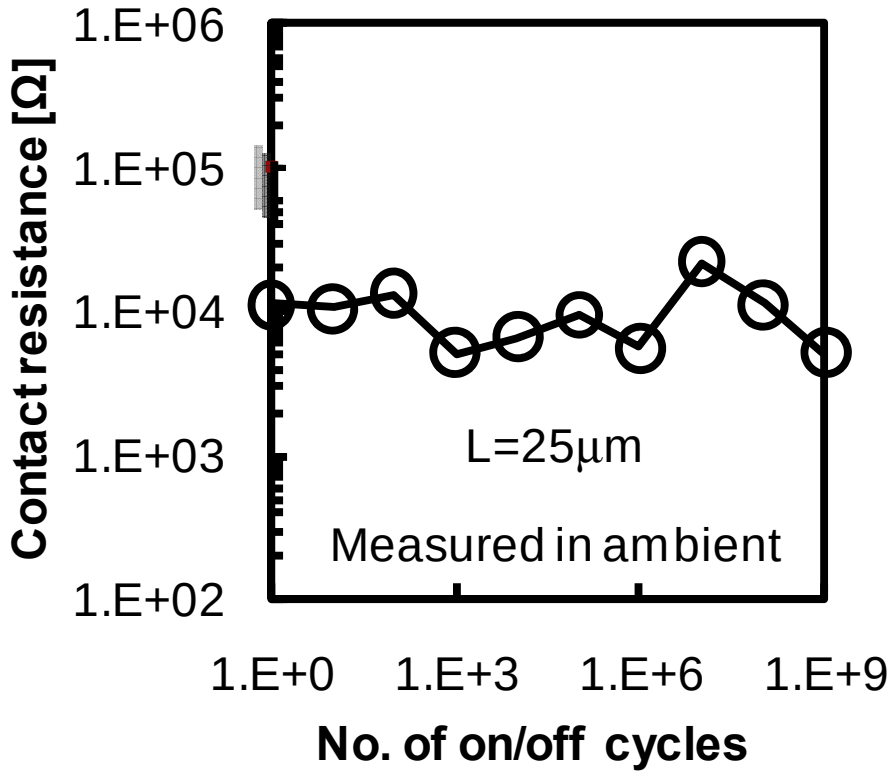
Scaling and Comparing to CMOS

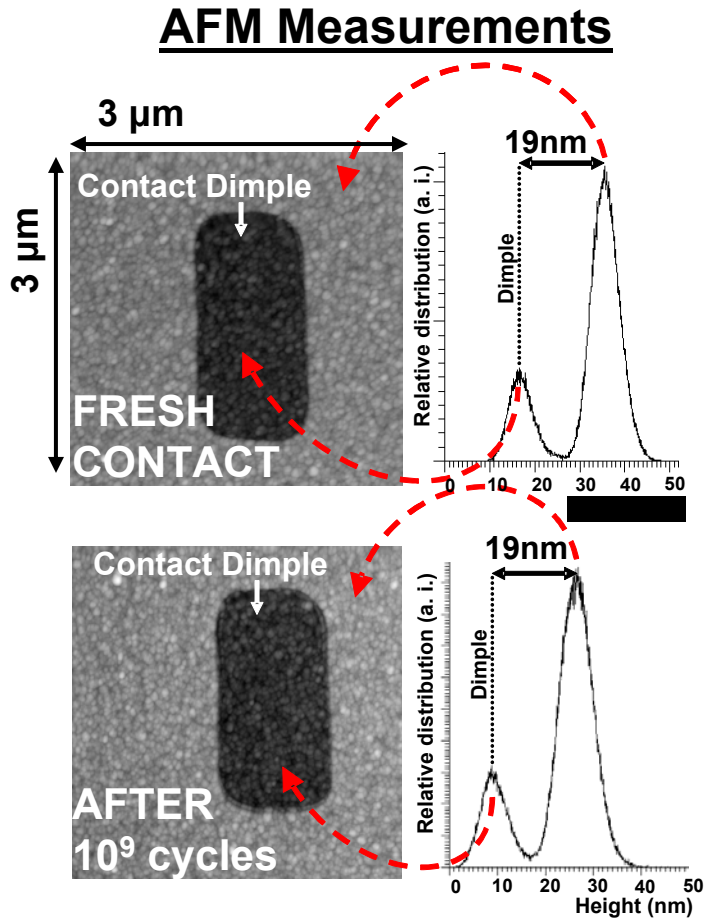


- Scaling similar to CMOS
  - Smaller = faster, lower voltage, lower power
- At 90nm, simulated relay adders are:
  - >9x lower E/op
  - >10x greater delay

- Reminder: parallelism enables high throughput
  - Even with slower individual elements

Relay Reliability



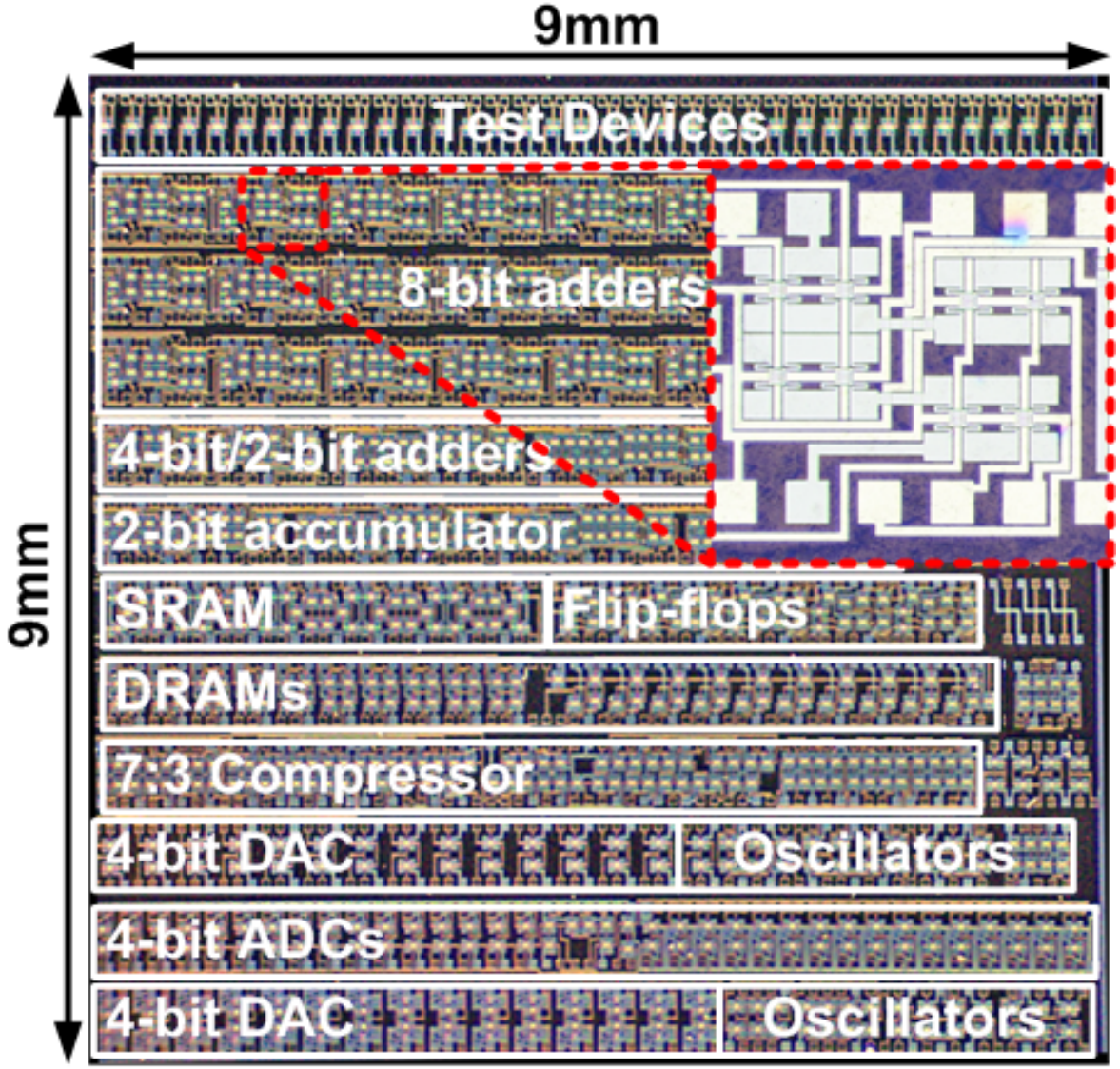


- **Increase contact resistance to improve reliability**
  - **Delay dominated by mechanics anyways**
- **Measured > 60 billion cycles so far**

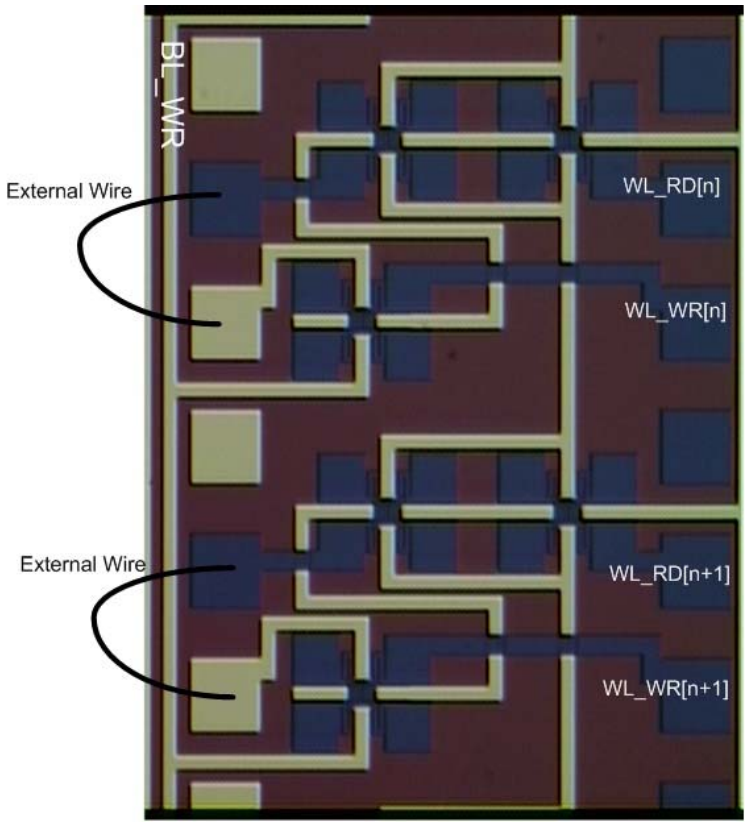
[H. Kam et al., IEDM 2009]

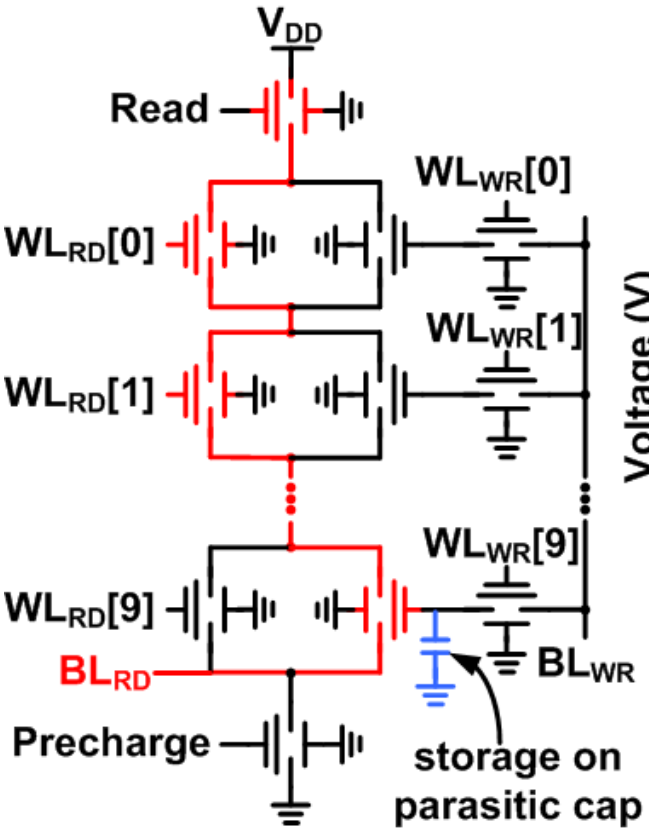
Circuit Demonstration Test-Chip

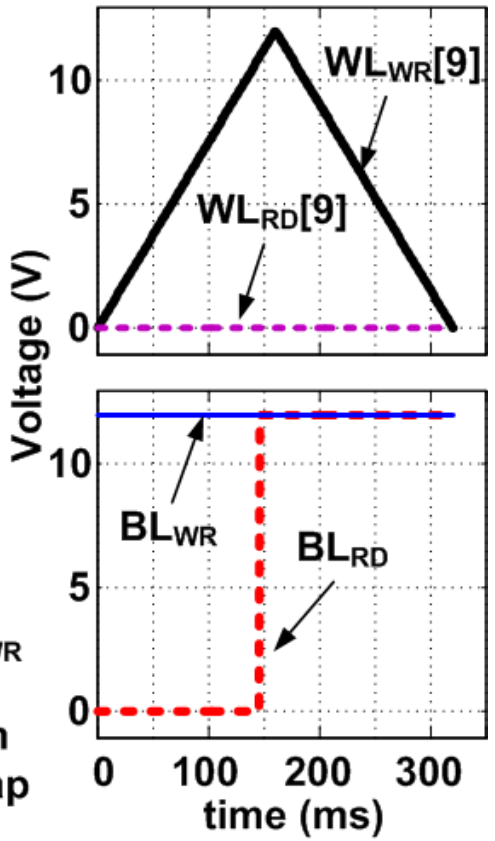
- Test devices
- Logic
- Timing Elements
- Memory
- I/O



Relay DRAM

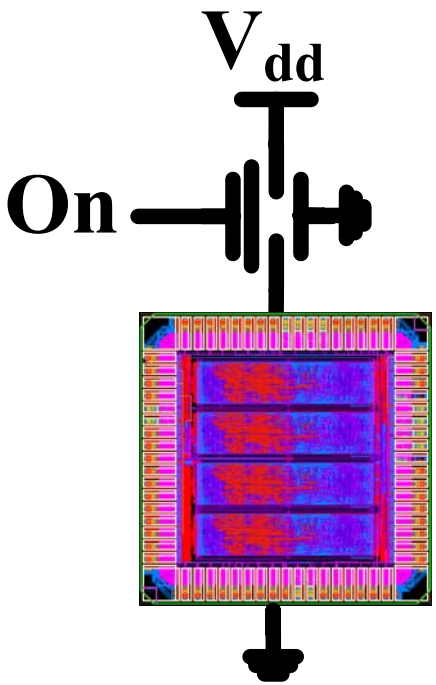


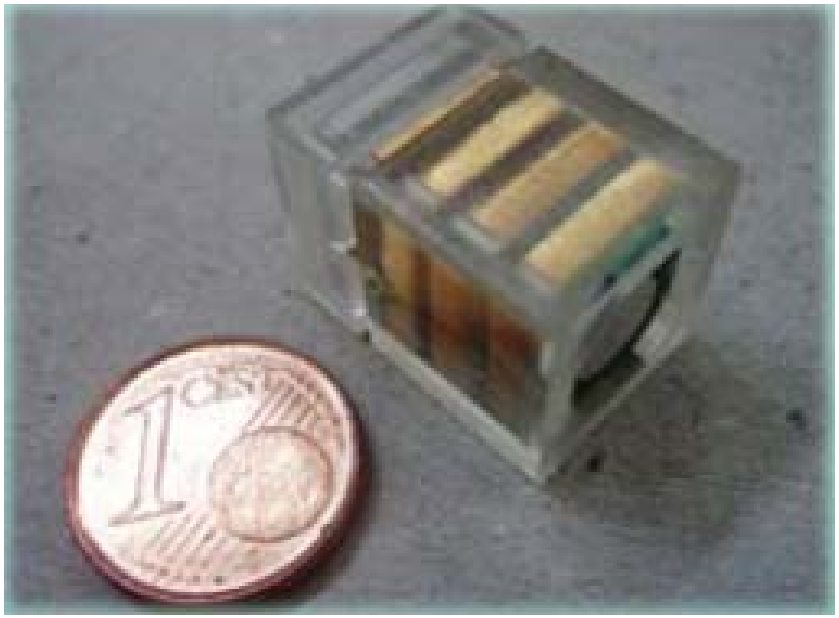




[F. Chen et al., ISSCC 2010]

Near-Term Driver: Power Gating

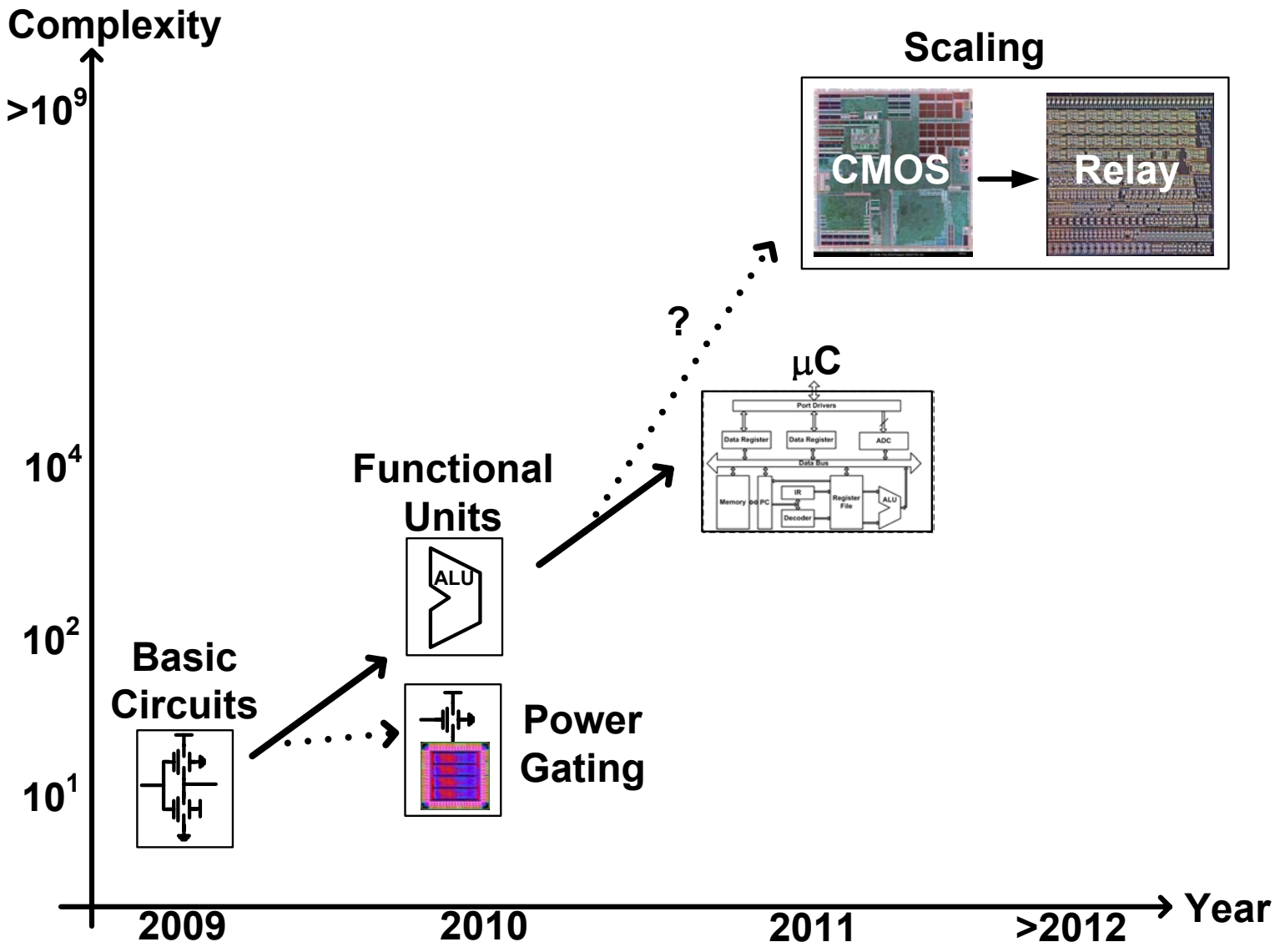




[Picocube, Rabaey]

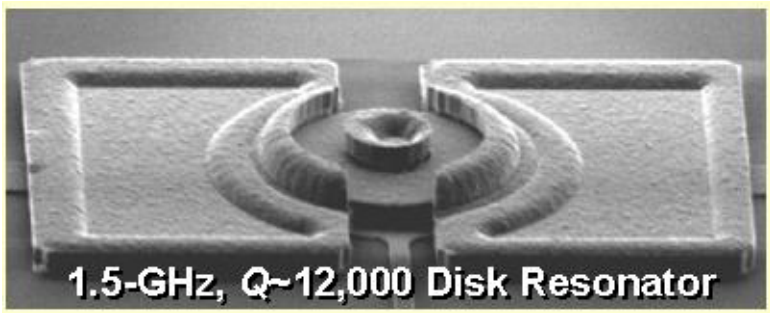
- Leakage of inactive CMOS circuits often limits embedded devices' lifetime
- Relay power gates could eliminate leakage

Roadmap: Back to the Future?

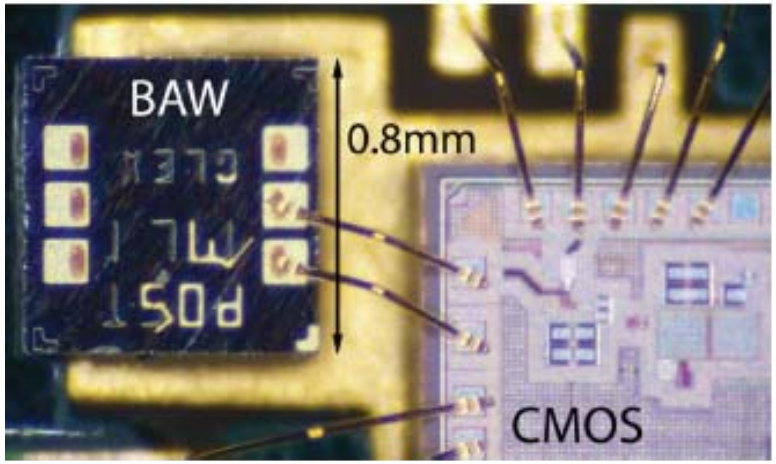


Final Note: Rethinking Scaling

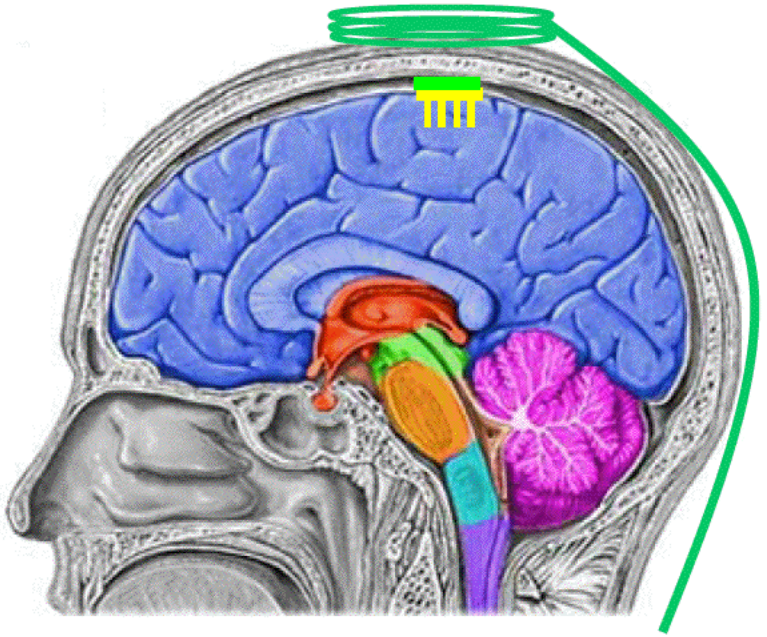
- Many exciting new apps based on mobility and sensing
- Innovation and cost driven by functionality – not just computing…



[Nguyen, UCB]



[Rabaey, UCB]



[Venkatraman, Carmena, UCB]